Monolithic Integration of 1.55 Micron Photodetectors with GaAs Electronics for High Speed Optical Communications

by

Hao Wang

Submitted to the Department of Materials Science and Engineering in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electronic Materials

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 1998

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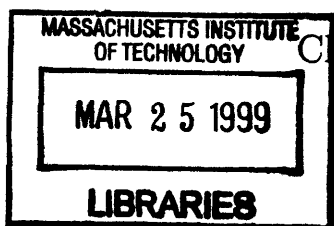
Author ....
Department of Materials Science and Engineering
August 7, 1998

Certified by ....
Clifton G. Fonstad
Professor of Electrical Engineering
Thesis Supervisor

Certified by ....
Eugene A. Fitzgerald
Associate Professor of Electronic Materials
Thesis Supervisor

Accepted by ....
Linn W. Hobbs
John F. Elliott Professor of Materials
Chairman, Departmental Committee on Graduate Students



Science

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Abstract

Integrated optoelectronics has shown exciting promise for high speed optical communication systems. For better system performance and lower cost, monolithic optoelectronic integrated circuits (OEICs) are highly desirable. A novel optoelectronic integration technology for high performance OEICs was proposed and partially developed and termed Aligned Pillar Bonding (APB) process.

The work began with applying GaAs-based Epitaxy-on-Electronics (EoE) technology to integrate matched pairs of 1.55 micron InGaAs photodetectors with high speed GaAs electronics, which requires the direct growth of InGaAs on lattice-mismatched GaAs substrates using molecular beam epitaxy (MBE).

A customized OEIC chip was designed and fabricated. Lattice-mismatched MBE growth was studied and InGaAs photodetectors on GaAs were produced using the relaxed buffer growth. However, the device performance and uniformity deteriorated significantly from those on lattice-matched InP substrates, and thus unsuitable for high speed OEICs.

Aligned pillar bonding (APB) process was hence proposed. APB integrates lattice mismatched materials using aligned, selective area wafer bonding at reduced temperature. The photonic device structures are grown on their lattice matched substrates under optimal growth condition. These structures are patterned into pillars, aligned and bonded into the designated wells on the electronic chips. Subsequent substrate removal and device fabrication results in high density OEICs.

1.55 micron InGaAs photodetectors on GaAs were demonstrated using reduced temperature Pd-assisted wafer bonding, resulting in superior device performance. While the conventional dry etching techniques are impractical to pattern the desired deep pillars, electron cyclotron resonance (ECR) enhanced reactive ion etching (RIE) of InP using chlorine/helium chemistry has been developed, resulting in fast, deep, smooth, and highly anisotropic etching at room temperature. The etching character-

istics have been calibrated for both InP and GaAs. Fast etching of InGaP, InAlAs, AlAs, and GaP has also been demonstrated. The etched pillars were subsequently bonded onto a OEIC chip, and initial study of small area pillar to well bonding was performed.

APB allows independent optimization of both photonics and electronics for OEIC integration, inherits the wealth of the existing electronics industry, maintains good planarization and high density, permits low parasitics and high performance, and is naturally compatible with large scale manufacturing.

Thesis Supervisor: Clifton G. Fonstad
Title: Professor of Electrical Engineering

Thesis Supervisor: Eugene A. Fitzgerald
Title: Associate Professor of Electronic Materials

Acknowledgments

Science and engineering are richly collaborative endeavors. During my four-year stay at MIT, I had the privilege of working with a cadre of talented professors, graduate students, engineers, and scientists in the field of optoelectronics. My slightest sense of accomplishment today is indebted to the flow of ideas and mutual encouragement from so many exceptional colleagues. I appreciate all of their efforts which help me get the chance to humbly share some of my reflections in this thesis.

My sincerest thanks go to my advisor, Professor Clifton G. Fonstad, Jr., for his financial support during most part of my stay at MIT, for his lending me a few Epitaxy-on-Electronics projects as the vehicles carrying me through the education, for his showing concerns at many difficult times, and most importantly, for the intellectual challenges he brought to me in my professional development as a graduate student. I am grateful also to Professor Eugene A. Fitzgerald, my co-advisor, for the talent and insight on heteroepitaxy he first brought to the campus since his joining MIT, and then to this thesis work via many members in his intelligent and dynamic group.

I would like to thank Professor Lionel C. Kimerling and Professor John B. Vander Sande for their supervision and advice on this thesis. I will remember the joy I had in Professor Kimerling's class on optoelectronics, and the delightful conversations with Professor Vander Sande.

I have enjoyed learning with fellow groupmates, both the present and the past. Especially, I wish to thank: Dr. Krishna V. Shenoy for introducing me to the Epitaxy-on-Electronics (EoE) technology as well as the Self Electro-optic Effect Devices (SEEDs), and for his initial training on the group MBE; Dr. Paul S. Martin for showing me the example of his solid spectrum of MBE growth techniques and device processing skills; Joseph F. Ahadian for his continuous dedication to the development of the EoE technology after Krishna left and for his help with the design of MIT OEIC5/LL MORX1 chip; Dr. Rajni J. Aggarwal for her advice on MBE growth of SEEDs on Caltech OEIC chips; Dr. Yakov Royter for his assistance on

growth well cleaning for the EoE-SEED project; Dr. Lung-Han Peng for showing me how to use his optics setup and how to do FTIR measurement; Professor Sheila Prasad for her gentle presence in the group; Norio Iizuki for his help on the MBE system; Donald Crankshaw for his assistance in the initial Pd-bonding experiment and showing me how to use the bonding furnace; Wojcieck Giziewicz for his energetic participation of optical measurement and setting up the Hall measurement, RHEED detector, and many other gadgets; other group members who helped me directly and indirectly in the course of this thesis research and to whom my appreciation always exists regardless of expression.

Robert Deming, Vitesse Semiconductor Corp., sent me the layout of his transimpedance amplifier which relieved me from circuit design and had me focused on the process development. I would like to thank Dr. Jeffray C. Livas, Dr. Roe Hemenway, Jr., and Dr. Mark Kuznetsov, MIT Lincoln Laboratory, for offering their time and facilities to pursue the 1.55 μm photodetector integration. Jeff gave me a 1.55 μm laser for the detector measurement along with many insights on high-speed testing. Roe continued the supervision and encouragement and I will always remember his wisdom. Mark's being calm and available to help added my sincere gratitude towards Lincoln Laboratory, which provided financial support for this research.

I would like to thank my friend Minghao Qi for many late nights spent together doing SEM and for his AFM calibration of my dry etched samples, which was essential for the development of the Aligned Pillar Bonding (APB) process. Minghao has been a great moral support and source of encouragement to me and I wish him the very best.

Dr. Mayank T. Bulsara and Andrew Y. Kim in Prof. Fitzgerald's group were very helpful with material characterizations. Mayank did TEM calibration for two critical samples of mine and was my guide to several material characterization facilities. Andy grew more than 10 micron thick InGaP layer for me to conduct dry etching study and loan me his spread sheet to make my X-ray calculation easier. Dr.

Jurgen Michel in Prof. Kimerling's group was very instrumental in helping me use the cathodluminescence facility there.

Without the Microsystem Technology Laboratory (MTL), the development of the APB process would have been impossible. I am greatly indebted to Dr. Vicky Diadiuk and many other MTL staff, especially, Joseph M. Walsh, Barry Farnsworth, Paul S. Tierney, and Kurt Broderick. The Technology Research Laboratory (TRL) at MTL was a true oasis with the highest intellectual intensity in Cambridge. Serving as a member in the Processing Technology Committee (PTC) directed by Vicky was a great learning experience to me. Working with many brilliant graduate students in the lab has been my honor and pleasure. I wish to thank many lab users for their willingness to swap equipment reservation time with me when I desperately needed it.

I should thank Dr. Gale S. Petrich for his care-taking of the microlab, and Olga Arnold for her lending me the lab key for the weekends and kindly reminding me to have a buddy.

Dr. Jiafu Luo and Professor Demetri Psaltis from Caltech enriched my graduate study through our collaboration on EoE-SEED. With the collaboration on Faraday-Stark effect, Zachary Lee and Professor Don Heiman expanded both the spectrum of my research and the list of equipment I have access to. I enjoyed very much working with Jiafu and Zach in these two unique and fruitful projects.

My delightful experience at MIT also comes from Professor Kirk D. Kolenbrander and students in the class of 3.15, fall term 1997. Prof. Kolenbrander's being supportive turned my odd assignment of teaching assistantship into a truely joyful adventure. The students in my recitation class were so bright and I am proud of all of them and would like to devote myself in the field of optoelectronics for them.

I would also like to thank Gloria L. Landahl for her assistance at various phases of my stay in the Department of Material Science and Engineering, for her care-taking of my paychecks, and for her guidance of the format and official progress of this thesis.

Seemingly indirect, but very important input both to me and to my thesis research was from several professors at the University of Michigan, to whom I only had chance today to formally express my gratitude. Professor Pallab K. Bhattacharya converted me from a theoretical physics graduate to a devoted researcher in the area of experimental semiconductor optoelectronics. I always remembered his efficient and hard working style. Professor Dimitris Pavlidis taught me everything about GaAs MESFET fabrication which benefited me in many aspects of my thesis research at MIT. I wish to thank Professor Roy Clarke for granting me the fellowship during my stay at the University of Michigan which helped me spend my first year in a foreign country efficiently in building up the necessary knowledge foundation.

I wish to thank Dr. Tadao Ishibashi at NTT for our private communications on the design of Uni-traveling Carrier Photodiodes; Dr. Ken D. Pedrotti at Rockwell Science Center for his teaching on optical receiver design and many insights in the review of OEIC technologies. I also appreciate Professor Rajeev J. Ram's joining MIT, bringing in many new ideas and research attractions. I wish to thank Dr. Dong Chen, my former college classmate, for his willingness to master the microscopic photography for me.

My sincere thank also goes to my dear friend Li Zhang, who helped me a great deal during the course of my writing of this thesis. I am grateful for all her care and encouragement.

My parents are those who gave me the most valuable heritage and ultimately the strength for me to explore the world. The respect for intellectual achievements and scholarly endeavor was imprinted by them during my childhood. They taught me not to be limited by arbitrary boundaries and how to appreciate the true power in a man. I am extremely grateful to them.

Finally, this thesis is dedicated to my wife, Olivia X. Wang, for her unfaltering belief in me, and for her endless love and support. She makes my life meaningful.

Contents

Abstract 3

Acknowledgments 5

List of Figures 13

List of Tables 20

1 Introduction 21

1.1 Motivations for Optoelectronic Integration 22

1.1.1 Markets for Optical Communication Components 22

1.1.2 Advantages of Optoelectronic Integration 26

1.2 Existing Optoelectronic Integration Processes 27

1.2.1 Technical Challenges 27

1.2.2 Various Integration Approaches for Optical Receivers 30

1.2.3 Performance Review of Demonstrated Receivers 32

1.3 Thesis Background 38

1.3.1 A High Speed Optical Receiver System at Lincoln Lab 38

1.3.2 Integration of High Speed Optical Receiver 42

2 Design of 1.55μm Photodetectors **44**

2.1 p-i-n Photodetectors 45

2.1.1 General Statement of the Transport Problem 47

2.1.2 Linearization of the Transport Equations 49

2.1.3 Calculation Results 51

2.2 MSM Photodetectors 55

2.2.1 General Description 55

2.2.2 Simulations and Design Guidance 57

2.3 Uni-Traveling-Carrier Photodetectors 61

2.3.1 The Invention of the UTC-PD 61

2.3.2 Theoretical Analysis 62

2.3.3 Heterojunctions with Flat Valence or Conduction Band 69

2.3.4 Improved Design and Response of a UTC-PD 72

2.4 Summary 76

3 1.55μm Photodetectors Grown on GaAs **79**

3.1 Lattice Mismatched Crystal Growth 80

3.1.1 Dislocations Associated with Mismatched Growth 81

3.1.2 Dislocation Reduction Techniques 84

3.2 Development of the Relaxed Buffer Structure 86

3.2.1 Material Characterization 86

3.2.2 Relaxed Buffer Development 91

3.3 Evaluation of 1.55μm Photodetectors on GaAs 94

3.3.1 Fabrication 96

3.3.2 Detector Performance 97

3.4 Summary 102

4 Integration via Epitaxy-on-Electronics 106

4.1 Epitaxy on Electronics Integration Technology 107

4.2 MIT-OEIC5/LL-MORX1 Chip 109

4.2.1 Performance and Stability of GaAs Electronics 109

4.2.2 GaAs OEIC Chip Design 112

4.2.3 Available OEIC Circuits 112

4.2.4 Amplifier Performance 118

4.3 EoE Integration Process 119

4.3.1 Chip Cleaning 119

4.3.2 Reduced Temperature MBE 123

4.3.3 EoE Material Evaluation 125

5 Aligned Pillar Bonding on Electronics 129

5.1 Wafer Bonding and Wafer Fusion 130

5.2 Aligned Pillar Bonding Process 132

5.2.1 Aligned Pillar Bonding on Electronics 132

5.2.2 Process Requirements for APB 134

5.2.3 Palladium Assisted Bonding 137

5.3 Reactive Ion Etching of InP Based Materials 140

5.3.1 Needs of Deep Fast Isotropic Dry Etching 140

5.3.2 Difficulties with InP Dry Etching 141

5.3.3 Electron Cyclotron Resonance (ECR) Enhanced RIE 144

5.3.4 Fast Deep Etching of InP at Room Temperature 147

5.3.5 Fast Deep Etching of GaAs and Other III-V Semiconductors . 154

5.4 1.55 μm Photodetectors Bonded on GaAs 158

5.5 Aligned Pillar Bonding on OEIC5 Chips 162

6 Conclusions and Future Research **170**

6.1 Accomplishments 170

6.2 Possible Directions for Future Research 173

Bibliography **176**

List of Figures

1.1 An Optoelectronics Industry Development Association (OIDA) projection of the world market for optoelectronics components for telecommunications. 23

1.2 1992 market and 1997 market forecast for fiber optic componants for North America. 24

1.3 1997 market forecast for fiber-optic components for North America. . 25

1.4 Comparison of OEIC receivers realized using InGaAs HBTs, InGaAs JFETs, InGaAs MISFETs, InGaAs HEMTs, and GaAs MESFETs. . 37

1.5 Receiver results for monolithic OEICs and other hybrid approaches. . 38

1.6 Block diagram of a optically amplified, high speed DPSK communication receiver system. 39

1.7 Block diagram of the proposed DPSK demodulator front-end. The current goal is to replace the $3in \times 4in$ hybrid dual-balanced detector-transimpedance-amplifier module with a monolithic OEIC chip of greatly reduced size. 40

2.1 Operation of the p-i-n photodiodes. 46

2.2 Transit time frequency response comparison between p-side and n-side illuminated p-i-n photodiodes. 52

2.3 Optimal intrinsic layer thickness for several given areas of p-i-n photodiodes. 53
2.4 Constant 3-dB bandwidth contours in the area and intrinsic-layer-thickness plane for the $In_{0.53}Ga_{0.47}As$ 1.55μm p-i-n photodetectors. . . 54
2.5 The design curves for $In_{0.53}Ga_{0.47}As$ MSM photodetectors. For given geometry of the detectors, the corresponding responsivity and 3dB bandwidth are shown. 56
2.6 Capacitance for MSM photodetectors in comparison with p-i-n photodetectors. 59
2.7 External quantum efficiency of the AR-coated MSM detectors. 60
2.8 Optimal finger spacing for several given areas of MSM photodiodes. . 60
2.9 Band diagram of a Uni-Traveling-Carrier Photodiode. 62
2.10 Electron distribution in the absorption layer of a Uni-Traveling-Carrier Photodiodes. 66
2.11 Calculated photoresponse of a Uni-Traveling-Carrier Photodiode and a conventional p-i-n photodiode. 68
2.12 Calculated 3-dB bandwidth (f_{3dB}) for UTC-PDs. 68
2.13 Ideal band diagram of a UTC-PD. 70
2.14 Sample flat valence design for GaAs/AlAs heterojuctions. 72
2.15 Sample flat valence design for InAlGaAs/InGaAs heterojuctions. . . . 73
2.16 Electron distribution in the absorption layer of a flatband UTC-PD. . 75
2.17 The improved 3dB bandwidth for a flatband UTC-PD. 75

3.1 Schematic of lattice-mismatched epitaxial layer on top of a substrate. 82
3.2 Schematic of misfit and threading dislocations in partially relaxed epilayer. 83
3.3 Schematic of the Bede triple crystal X-ray diffraction set-up. 86

3.4 The enhancement of the angular resolution by the triple axis diffractometry. 88
3.5 Reciprocal Space Mapping for Sample 9449 from 004 planes. 89
3.6 224 glancing exit Reciprocal space map for Sample 9449. 89
3.7 Multiple X-ray rocking curves for Sample 9614. 90
3.8 Structure of graded short-period superlattice buffer. 92
3.9 Sample 9449: p-i-n grown on GSSL buffer. 93
3.10 Sample 9446: p-i-n grown on the linearly graded buffer. 93
3.11 Cross sectional TEM for Sample 9449. 95
3.12 Cross sectional TEM for Sample 9446. 95
3.13 Cathodluminescence for Sample 9446 and Sample 9449. 96
3.14 Dark current comparison for the linearly graded buffer and the GSSL buffer. 97
3.15 Reciprocal space mapping for Sample 9614 from 004 planes. 98
3.16 224 glancing exit reciprocal space map for Sample 9614. 98
3.17 Dark current comparison for the linearly graded p-i-n photodetectors grown at different grading rates. 99
3.18 The dark current of 50 detectors grown on the lattice matched InP substrate. 100
3.19 The dark current of 50 detectors grown on the lattice-mismatched GaAs substrate. 100
3.20 The photo currents for Sample 9610 grown on the lattice matched InP substrate. 101
3.21 The photo currents for Sample 9614 grown on a lattice-mismatched GaAs substrate, using a linear graded buffer with a grading rate of 10%In/μm. 101

3.22 Leakage current density as a function of compositional grading rate. . 103

4.1 Optoelectronic circuit fabrication flow using the E-o-E integration technology. 109

4.2 Schematic of Vitesse's HGaAs MESFET structure. Four layers of metal interconnects are implemented using the conventional state-of-the-art silicon interconnect technology (Jim Mikkelson, private communications).111

4.3 Metal-layer sheet resistance after 5-hour thermal cycles. 113

4.4 Circuit layout of MIT OEIC5/LL MORX1 chip. 114

4.5 Circuit layout of the polarization diversity receivers on MIT OEIC5/LL MORX1 chip. 116

4.6 Circuit layout of the dual balanced receivers on MIT OEIC5/LL MORX1 chip. 116

4.7 Circuit layout of the single detector receivers on MIT OEIC5/LL MORX1 chip. 117

4.8 Circuit layout of the process control module and microwave testing cell on MIT OEIC5/LL MORX1 chip. 118

4.9 Circuit layout of DGW array, LED driver, and dual balanced detectors on MIT OEIC5/LL MORX1 chip. 119

4.10 The bandwidth of a fabricated transimpedance amplifiers on MIT OEIC5/LL MORX1 chips. 120

4.11 Illustration of epitaxy-on-electronics (EoE) integration of monolithic optical receivers. 122

4.12 Dielectric Growth Well (DGW) cleaning process. 123

4.13 Installed Hydrogen cracker in MIT solid source MBE system. 126

4.14 Comparison of the cathodluminescence from the bulk monitor Sample 9614 and the material grown in a big street well on the OEIC5 chip. . 128

4.15 The Surface Morphology of Sample 9614. 129
4.16 The Surface Morphology of Materials in a 100×100μm Growth Wells on OEIC5 Chip. 129
4.17 The Photograph of a PDRx cell after EoE growth on the OEIC chip. 130
4.18 The cathodluminescence from four adjacent growth wells on the OEIC5 chips. 130

5.1 Aligned Pillar Bonding (APB) on electronics Process. 135
5.2 Photolithography misalignment caused by the thermal expansion coefficients mismatch. 138
5.3 Conductivity comparison for Pd assisted wafer bonding. 141
5.4 The conventional parallel plate reactive ion etching configuration. . . 146
5.5 The Electron Cyclotron Resonance (ECR) enhanced Reactive Ion Etching (RIE) Configuration. 148
5.6 InP pillar etched in Cl_2/He chemistry with surface roughness. 150
5.7 Deep InP pillar with smooth surface. 151
5.8 InP etch rate as a function of ECR Power. 152
5.9 InP etch rate as a function of RF power. 152
5.10 InP etch rate as a function of pressure. 153
5.11 InP etch rate as a function of chlorine composition. 153
5.12 High aspect ratio InP dry etching demonstrated by Cl_2/He chemistry. 154
5.13 AFM image of the etched InP surface. 155
5.14 GaAs etch rate as a function of ECR Power. 157
5.15 GaAs etch rate as a function of RF power. 157
5.16 GaAs etch rate as a function of pressure. 158
5.17 GaAs etch rate as a function of chlorine composition. 158
5.18 GaP etch by Cl_2/He chemistry. 159

5.19 InGaP etch by Cl_2/He chemistry. 159
5.20 The structure of a p-i-n photodetector designed for bonding in the APB process. 160
5.21 Dark current statistics for 1.55μm photodetector Sample EPIHao bonded onto GaAs. 161
5.22 Photo response for the 1.55μm photodetector Sample EPIHao bonded onto GaAs. 162
5.23 I-V characteristics showing the reverse breakdown voltage for three kinds of photodetectors. 163
5.24 Comparison of the sharpness of the reverse breakdown. 163
5.25 Proof of the alignment (1): the impression of the pillars at the bottom of the wells due to the mechanical and thermal compression. 165
5.26 Proof of the alignment (2): the impression of the chip circuit onto the pillar wafer due to the mechanical and thermal compression. 165
5.27 Proof of the bonding (1): the materials bonded into the wells. After the substrate removal, surface preserved well. 166
5.28 Proof of the bonding (2): the Smallest pillar (13μm square) has been bonded to the smallest well (25μm square). 167
5.29 Proof of the pillar protection: the resist coverage on the chip after the resist reflow. 168
5.30 Proof of the Pd-assisted pillar bonding (1): InGaAs pillars of various sizes are bonded onto Pd-coated GaAs. 169
5.31 Proof of the Pd-assisted pillar bonding (2): The 4μm InGaAs alignment mark is transferred onto GaAs. 169
5.32 The SEM image of the InGaAs pillar bonded onto Pd-coated GaAs at 350°C. 170

6.1 Chlorine based RIE etch of a vertical cavity surface emitting laser structure. 176

List of Tables

1.1 Performance for monolithically integrated optical receivers on InP. . . 35

1.2 Performance of monolithically integrated optical receivers on GaAs. . 36

4.1 Vitesse HGaAs process evolution: MESFET performance (Jim Mikkelson, private communications). 112

Chapter 1

Introduction

Integrated optoelectronics using III-V compound semiconductor technology has shown exciting advances for applications in optical telecommunication systems [1, 2, 3]. Most commercial integrated optical communication components including optical transmitters and receivers are hybrid assemblies. When the broadband, high data rate network is approached, these hybrid units tend to be very expensive and subject to reliability problems. The development of monolithic optoelectronic integrated circuits (OEICs) fulfilling the tasks for high speed communication systems is thus highly desirable.

The needs and markets for high speed optical communication components, along with the technological advantages are discussed in Section 1.1. A brief review of the challenges for monolithic integration and the current status of monolithic optical receivers are given in Section 1.2. In Section 1.3, the research background of the thesis is outlined.

1.1 Motivations for Optoelectronic Integration

1.1.1 Markets for Optical Communication Components

In the past 30 years, the invention of long-lived semiconductor laser diodes, along with the development of low-loss optical fiber and practical optical amplifiers have ushered in a new era for optical communication. Optical fiber systems have been implemented across oceans and continents, while free-space systems are used to provide high data-rate communication links between satellites at geosynchronous distances. Optical communications, along with microwave and wireless technologies, are enabling the construction of high-capacity networks with global connectivity.

Motivated by the expectation that high quality, full-motion video and multimedia services will be demanded of future networks, high data rate optical broadband networks have been undergoing extensive development. Integrated optical communication components such as optical transmitters and receivers, typically hybrid assemblies, have demonstrated good performance and some of them are commercially available. The goal of most research on these components so far is to produce the best performance possible, and the cost of the resulting products is generally high.

In order to provide universal service, the broadband networks must extend to the individual subscribers' residences and businesses. The optical fiber entering the local business and residential markets or "subscriber loops" presents a greater opportunity for optoelectronic components, with the device performance criteria less stringent than for most other telecommunication applications. The required number of optical communication units is very large because of the large number of residential and business subscriber locations. It has been estimated that the mass market potential will become considerable by the year 2015 due to the extensive penetration of the fiber in the loop. Figure 1.1 shows the future revenue growth due to

optoelectronic transmitter-receiver pairs for telecommunications assuming discrete components. This projection, dominated by the new market for the fiber in the loop, indicates revenues due directly to optoelectronic components of more than $1 billion within about a decade and rising rapidly thereafter.

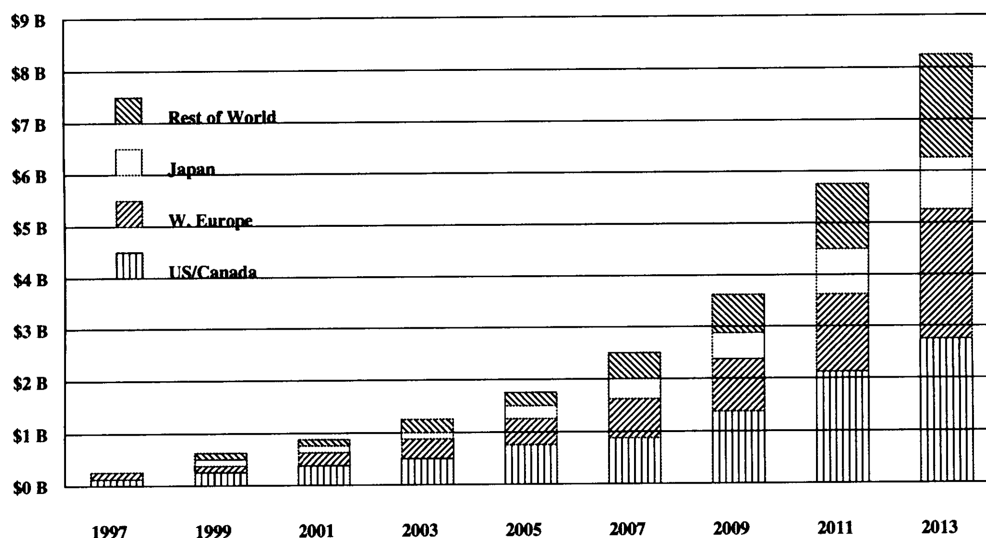

Figure 1.1: An Optoelectronics Industry Development Association (OIDA) projection of the worldwide market for optoelectronics components for telecommunications. This is projected to become a multi-billion-dollar market as OEIC technology matures for volume production [4].

Figure 1.2 shows the fiber optic component market for 1992 and 1997 in North America. 1997 market forecast for active and passive fiber-optic components is shown in Figure 1.3 with specific details on the technologies involved and on the compounded annual growth rate for each component. The active OEIC components including both transmitters and receivers show particularly strong growth.

Although research on optical communication components is often driven by achieveing the best performance possible, the practical implementation of most lightwave networks is limited by cost. The development of cost-effective and reliable optical communication units is therefore highly desirable. When the high speed networks

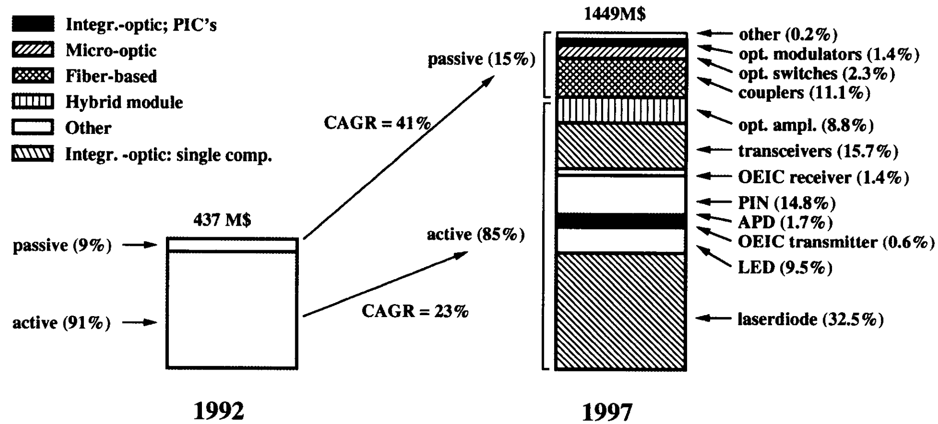

Figure 1.2: 1992 market and 1997 market forecast for fiber optic componants for North America [5]. The CAGR (compounded annual growth rate) percentages, divided into passive and active components, express compound annual growth rate for 1992–1997. Keys to the abbreviations in the figure are : PIC–photonic integrated circuits, OEIC–optoelectronic integrated circuits, PIN–pin photodiode, APD–avalanche photodiode, LED–light-emitting diode.

are pursued, the best approach tends to be the monolithic optoelectronic integrate circuits (OEICs) because of the drastically increased hybrid packaging expense for high speed modules.

It is worth noting that even in the performance-driven optical networks such as free space optical links for satellites at geosynchronous distances, the monolithic OEICs will also be quite desirable since the hybrid units are usually bulky and would impose siginificant weight burden on the satellites. It is our view that the strength of OEIC technology lies more in the important functionality attained through their unique ability to provide enhanced capability at low cost than in individual component performance.[1]

[1] Historically, this was the experience on electronics as well: IC technology lagged far behind discrete component technology for record performance, during the entire period of its meteoric rise to electronic market dominance.

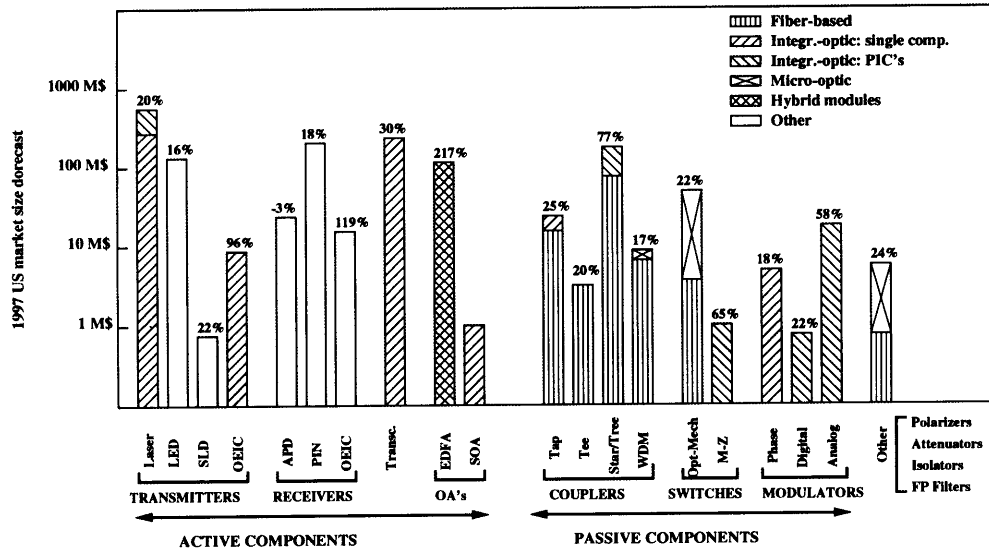

Figure 1.3: 1997 market forecast for fiber-optic components for North America [5]. Specific technologies used for the components are shown. The CAGR percentages for 1992–1997 are given for each type of the components considered. Keys to abbreviations not mentioned earlier in Figure 1.2 are: SLD–super luminescent diode, Transc.–transceiver, EDFA–Erbium doped fiber amplifier, SOA–semiconductor optical amplifier, WDM–wavelength division multiplexer, MZ–Mach-Zehnder, FP–Fabry–Perot, OA–optical amplifier.

In this Ph.D thesis research, we pursue the novel monolithic integration of high speed optical receiver, one of the most important optical communication compoenents, which will occupy a significant part in the future hardware market for the broadband optical network. The following discussion will focus on the advantages and difficulties of monolithic integration of optical receivers. Details will be given in the following section.

1.1.2 Advantages of Optoelectronic Integration

Optoelectronic integrated circuits (OEIC) composed of photodetectors integrated with transistors on the same substrate promise to provide several advantages over their discrete and hybrid counterparts; among these are enhanced performance, higher density, ease of manufacturing, and greater complexity and functionality.

Performance enhancement of OEIC receivers is provided by the better noise immunity than that of discrete components, due to the on-chip interconnections and lack of stray capacitance and bond-wire inductance, which in turn allows for higher operating speed and greater sensitivity.

The integration density is achieved by eliminating the chip-to-chip connection and packaging which are indispensible in the hybrid integration combining optoelectronic devices and integrated circuits in the same package or substrate. In the hybrid units, the device density of the resulting optoelectronic integrated circuits (OEICs) is relatively low. Numerous applications, especially wavelength division demultiplexing, require high density arrays of detectors and electronic logic. Hybrid integration is inherently limited in the integration density it can offer.

Manufacturing improvements accrue from the use of the photolithographically defined and monolithically produced combinations of both detectors and transistors, which eliminates labor-intensive packaging steps; at high speed the benefits are even greater because of the reduced packaging cost. For applications such as WDM, or multichannel optical interconnects, arrays of transmitters and receivers are desired. Costs for the fiber attachment to the monolithic OEIC arrays can be lowered because the entire fiber array can be aligned to the optical devices in a single step. This will drastically reduce the packaging cost for optoelectronic modules since the major part of the cost currently is accrued during fiber positioning and attachment.

Better reliability is achieved in OEIC technology due to more uniform and repro-

ducible devices, lower coupling parasitics, and the allowance of using more sophisticated matching and equalization schemes with less effort and cost.

Combination of greater functionality with the receiver element produces further gains. For example, a complete receiver demodulator including an automatic gain control (AGC) amplifier, a clock recovery circuit, decision circuits, and an output driver could be of considerable system advantage.

1.2 Existing Optoelectronic Integration Processes

1.2.1 Technical Challenges

Several technological difficulties unique to optoelectronic integration, however, have been historically troubling OEIC development. Overcoming these difficulties is essential if monolithically integrated optoelectronic devices are ever to compete successfully, and in time replace, the hybrid optoelectronic circuits now in wide spread use. The various difficulties presented in the current optoelectronic integration schemes are as follows.

Independent Optimization of Photonic and Electronic Components

The generally contradictory material requirements of photonic and electronic devices demand that functionally difference device layers be segregated in different regions of the chip, both in the plane of, and perpendicular to, the substrate. For those OEICs made in the same epitaxial layers, some areas are fabricated into photonic devices and other areas into electronics. The inability of optimizing both photonics and electronics at the same time becomes a concern since high performance optoelectronic systems require both state-of-the-art optical and electronic characteristics.

Planarization and Photolithography

Even in the stacked epitaxial growth approaches which allow for better independent optimization of photonic and electronic components, the selective etching often creates several micron high steps in the topology which make high-resolution lithography extremely difficult.

Device Interfacing

In addition to electrical interfacing to external circuitry, optoelectronic devices must be designed to facilitate optical interfacing to the transmission medium- typically an optical fiber of very small core diameter. In hybrid modules, this often involves labor-intensive alignment and attachment.

Available Electronics

Another major difficulty with monolithic integration is that the most widely used, well developed material for integrated electronics, silicon, is not useful for many optoelectronic devices and thus one must either monolithically integrate III-V optoelectronic devices on silicon, or utilize III-V electronics. Monolithic integration of (In, Al, Ga)(As, P) heterostructures on silicon (a process generically called GaAs-on-Si) has attempted to make use of the wealth of today's existing silicon BiCMOS electronics integrated circuit technology. Unfortunately, III-V epitaxy on silicon (or vice versa) is made difficult by the facts that the lattice constants of GaAs and Si differ by 4%, and that the thermal expansion coefficients differ by almost 50%. The lattice mismatch can be overcome by special growth initiation techniques and interfacial buffer layers, but the thermal mismatch is more troublesome. Significant numbers of defects (and even cracks) are introduced as GaAs-on-Si structures are cooled from the growth temperature to room temperature, and the III-V layers are under severe

tension, which reduces device lifetimes dramatically, reduces reliability, and in general adversely affects performance.

Manufacturability

Recently, advances have been made using so called epitaxial liftoff and flip-chip bonding[2] which essentially bond independently optimized photonic devices, usually based on the III-V compound semiconductors, on the electronics which is often CMOS circuits. The technological difficulties incurred here are the reduction of the level of integration and lack of manufacturability. To produce large-scale, high-density OEICs with high yield and low cost is indeed a major challenge.

Process Development

A number of monolithic approaches involve growing both electronic and photonic materials before processing any of them. An important problem with the epitaxy-first approach is that pursuing it involves simultaneous development of sophisticated fabrication technologies for optoelectronic devices and integrated circuits. The task is enormous and as a practical matter only small scale OEICs have been demonstrated following this approach.

Successful monolithic integration technique must address the afore mentioned technological challenges and take full advantage of the mature electronics industry in order to impact the commercial systems, which require uniformity, reliability, and manufacturability. Although these problems can be difficult to solve, one expects that concerted efforts aimed at their solution will result not only in high-performance

[2]These techniques are not exactly monolithic in nature. They are somewhere in between the hybrid and monolithic. However, they are widely considered as viable options for optoelectronic integration.

integrated optoelectronic circuits, but also in the enhancement of discrete photonic device technology, as has been indeed the impact of electronic integration on discrete electronic componentry.

Detailed comparison between various monolithic integration schemes specific for optical receivers is given in the following section.[3]

1.2.2 Various Integration Approaches for Optical Receivers

The major approaches that have been pursued to combine devices with different layer structures are: dual use layer structures, sequential growth and etching, selective area growth, heteroepitaxy, epitaxial liftoff, and flip-chip bonding.

One approach to the integration is to choose device structures which are easily and naturally compatible. One example is the use of metal-semiconductor-metal (MSM) photodiodes constructed using interdigited electrodes and GaAs MESFETs on semi-insulating GaAs substrates [6]. For this approach, no additional process steps are required; the photodetector can be made using gate metal and the standard implant steps required to make the MESFETs. An additional advantage of this approach comes from the very low capacitance of the MSM structure. However, the major disadvantages are the decreased detector quantum efficiency due to the shadowing of the absorption region by the interdigited contacts, and the inability for this material system to work in the wavelength range from 1.3μm to 1.55μm for fiber optic communications.

An alternative and similarly compatible process is to use PIN detectors integrated with HBTs [7, 8]. The PIN detector can be made using the transistor collector layers as the absorption region for the PIN and the collector and the base contacts of the HBTs as cathodes and anodes. Similarly, the HBT may be used directly as a

[3]The review methodology was originally presented by Dr. K. D. Pedrotti in a SPIE course note.

phototransistor to yield a high performance, easily integrated photoreceiver. These approaches also suffer from compromises that must be made between the electronic and optical devices. In general as the collector absorption layers are decreased in thickness, the transistor speed increases while the detector quantum efficiency decreases.

The next simplest technique is to use a single epitaxial growth consisting of the epilayers needed for each device stacked on top of one another [9, 10, 11, 12]. During subsequent processing the unused top layer is removed where appropriate. This allows the use of optimized layer structures for each device but often results in degraded performance due to capacitive coupling between the doped device layers. If this procedure is used on planar substrates, then a nonplanar surface results after etching, which can be troublesome for fine line lithographic process. To avoid this problem, the epilayer growth is often initiated on substrates which had grooves etched to the appropriate depth so that the completed circuit will be planar. Sometimes, this approach is referred as "epi-in-the-well" [13, 14, 15].

To eliminate the parasitic coupling between the device layers described above, a number of multi-step epitaxial process have been used. Typically one layer is grown and then etched away where it is not needed. The epilayer for the next device is grown and then removed from the top of the first layer. A number of variations including selective area growth fit essentially in this same category [16, 17, 18]. One problem with this approach is that the wafer preparation before the regrowth step is very critical if one wishes to grow high quality layers in the second growth step. Depending on the devices and material system, the thermal cycling can also degrade device performance.

Another similar, but more challenging strategy, is to take the above approach, together with the use of lattice-mismatched compounds that are each best suited

for the device of interest. An example of this would be to use a silicon substrate for the electronics and then grow III-V epilayers on top for the emitters and detectors [19, 20, 21]. Heteroepitaxy is a rapidly advancing and dynamic field, although devices such as lasers grown this way have exhibited poor lifetime and the photodetectors have high dark currents. The chief cause of problems with this technique is due to both thermal and mechanical mismatch between different material layers, generation and propagation of dislocations from the interface between the two different materials will ultimately degrade the device layers. These then serve as generation and recombination centers which adversely affect device performance and lifetime.

One way to ensure that dislocations will not propagate is to grow each different device structure on its own matched substrate, then remove the devices from one of the substrates and transfer to the other. This technique, also known as Epitaxial Liftoff (ELO), has demonstrated the capability to transfer optical and electrical devices without degradation from one type of substrate to another [22, 23].

A somewhat similar approach, is to use flip-chip bonding to package devices directly on top of one another using indium or solder bonds [24]. This has the advantage of using well-developed technology that can precisely place tested optimized devices together in a way that realizes most of the advantages that are expected through integration; chiefly low parasitics and a compact and rugged assembly. In addition, only slight modification is needed for devices that are currently in production, making this a strong competitor for the OEIC integration. Unfortunately, the scale of the integration via this approach is limited and the manufacturability is low.

1.2.3 Performance Review of Demonstrated Receivers

The difficulty of monolithic integration on silicon, and steady advances in the levels of electronic integration demonstrated on III-V substrates have led to a shift of emphasis

to monolithic integration on either gallium arsenide or indium phosphide. In these material systems, many of the technical obstacles that originally existed have been overcome for OEIC receivers, as good performance has been achieved using a variety of technology and approaches.

OEIC Result (I): Monolithic Optical Receivers on InP

Since long distance communication usually demands the working wavelength to be 1.55μm for the lowest fiber attenuation, the material system for these applications under most investigation is InP-based. The main problem that faced integration here is the relatively poorer quality of the available electronic devices. High quality Schottky barriers could not be made in this material system thus MESFET technology can not be simply developed for InP. Alternative approaches such as Metal Insulator Semiconductor Field Effect Transistors (MISFETs) and Junction Effect Transistors (JFETs) were first tried. MISFETs have been limited by interface traps at the semiconductor-insulator interface resulting in device instabilities. JFETs have been more successful but in general have not exhibited the best high-speed performance, mostly due to the difficulty in producing the short gate lengths required for high transconductance and low input capacitance. To get around these problems, thin layers of InAlAs, on which good Schottky barriers can be formed, have been used on top of InGaAs channel layers to produce high quality short gate MESFETs and HEMTs (sometimes called Modulation Doped Field Effect Transistors (MODFETS) and Heterojunction Field Effect Transistors (HFETs)). Recently the use of HBTs in this material system has attracted interests because of their high performance, relative ease in lithographic processing, lack of sensitivity to surface conditions, and compatibility with detectors [7, 8].

The relative performance of receivers based on these technologies is listed in Table

1. A scatter plot of OEIC receiver sensitivity vs. demonstrated bit rate is shown in Figure 1.4, where the OEIC approaches are categorized according to the electronic technology that was used to realized the integration. So far the best high speed performance has been obtained using InP HFETs. At lower bit rates the JFETs are very competitive with HEMT-based integration following right behind, but their large gate lengths and lower f_T's limit their performance at high bit rates.

OEIC Results (II): Monolithic Optical Receivers on GaAs

The majority of the optical receivers on GaAs have been fabricated using MSM detectors and MESFETs. This combination takes advantage of the well-developed GaAs MESFET technology and is very easy to be integrated since MSM detectors are completely process compatible with the MESFET fabrication. The use of GaAs substrate makes the working wavelength limited to the 850nm-870nm range which is suitable for the applications in optical interconnects and short distance optical links. In the literature, the receiver sensitivity is seldom reported for these OEIC receivers, often because the receiver is not intended for use with noise limited signals, when more than adequate optical power is usually available.

Table 2 lists the recent results achieved on GaAs substrates. In the scatter plot of OEIC receiver sensitivity vs. demonstrated bit rate shown in Figure 1.4, it seems that the demonstrated monolithic GaAs-based receivers have poorer performance at the low bit rates than those based on InP but, at the high bit rate, some GaAs-based receivers did demonstrate competitive performance.

OEIC Result (III): Monolithic vs. Hybrid Comparison

Figure 1.5 illustrates the fact that relative to other hybrid integration schemes, monolithic OEICs have consistently under-performed with regard to bit-rate sensitivity

Technology (InP-based)	Reference	Speed (Gbps)	Sensitivity (dBm)	f_T (GHz)	Detector Diameter (μm)	Quantum Efficiency (%)	Detector Capacitance(fF)
PIN-MISFET	Antreasyn 1989[25]	0.6	-25.4	29	35		
	Mattera 1989[26]	2.4	-18.2	38	35		300
PIN-JFET	Blaser 1992[27]	2.4	-29.5	8	20	80	150
	Park 1992[28]	2.0		1.8	80	45	350
	Akahori 1991[29]	0.62	-33.6	10	20	85	80
	Uchida 1991[30]	0.62	-34.7	10	20	85	80
	Lo 1991[31]	0.25	-37	7	40	82	180
PIN-HEMT	Akahori 1994[9]	15 GHz	-14.5		15	85	80
	Akatsu 1993[32]	10	-17.3	25	20		
	Lee 1992[33]	6	-21.2	14		.89	60
	Berger 1992[34]	1	-29.6	24	30 × 40	48	190
	Akahori 1992[35]	10	-16.5	25	20	85	90
	Lai 1991[36]	6.4		72	28		50
	Yano 1990[37]	1.2	-30.4	18	20	76	80
	Hong 1991[38]	1.2	-25		MSM	48	75
PIN-HBT	Lunardi 1995[7]	20	-17.0	70	15 × 15	85	50
	Chandrasekhar 1993[39]	5	-22.5	52	30 × 30	52	200
	Chandrasekhar 1992[40]	10	-15.5	71	40 × 40	59	200
	Chandrasekhar 1991[41]	5	-18.8	32	40 × 40	63	200

Table 1.1: Performance for monolithically integrated optical receivers on InP.

Technology (GaAs-based)	Reference	Speed (Gbps)	Sensitivity (dBm)	f_T (GHz)	Detector Diameter (μm)	Quantum Efficiency (%)	Detector Capacitance (fF)
PIN-HBT	Pedrotti 1991[42]	17	-12	60	20	35	52
	Pedrotti 1991[43]	9	-17.5	60	20	35	52
MSM-MESFET	Yamanaka 1992[44]	5	-6.9		80X73	30	
	Pedrotti 1990[45]	2	-15	14	100X100		100

Table 1.2: Performance of monolithically integrated optical receivers on GaAs.

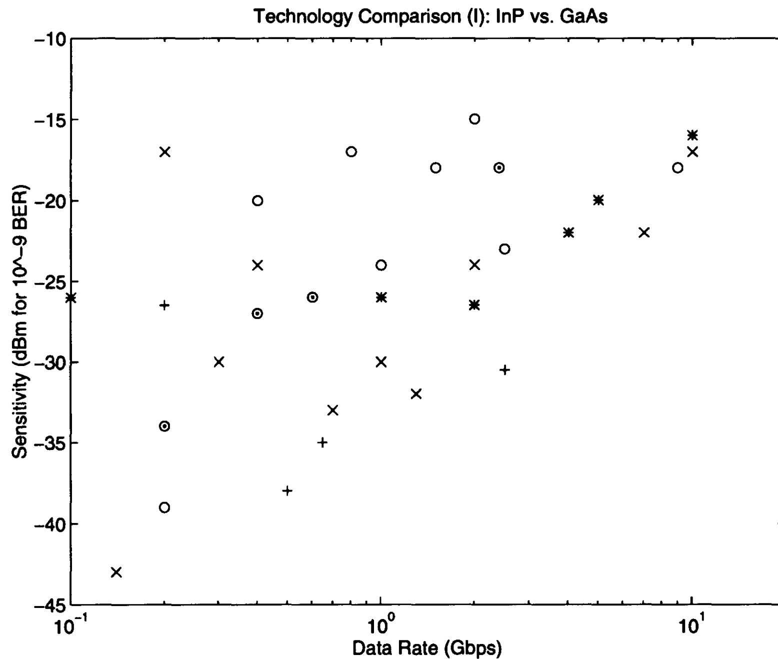

Figure 1.4: Comparison of OEIC receivers realized using InGaAs HBTs ($*$), InGaAs JFETs ($+$), InGaAs MISFETs ($\odot$), InGaAs HEMTs ($\times$), and GaAs MESFETs ($\circ$). The sensitivity listed here is the optical power required to achieve a bit error rate of 10^{-9}. The closer a receiver is to the lower right-hand corner, the better its performance.

product. Erbium doped fiber optical amplifiers (EDFAs) and APDs both provide a cleaner source of gain than electrical amplifiers and assist the hybrid versions of receivers to outperform others. Even the hybrid PIN receivers outperform monolithic OEICs. This is mostly due to the ability to use the best electronic devices and optical detectors unconstrained by the requirement to be monolithically integrated. So far, inferior electronic device performance has overshadowed the advantages that should be realized by the OEICs. Again, the true advantages of the OEICs that may be decisive in their commercial introduction could well be lower costs and easier packaging.

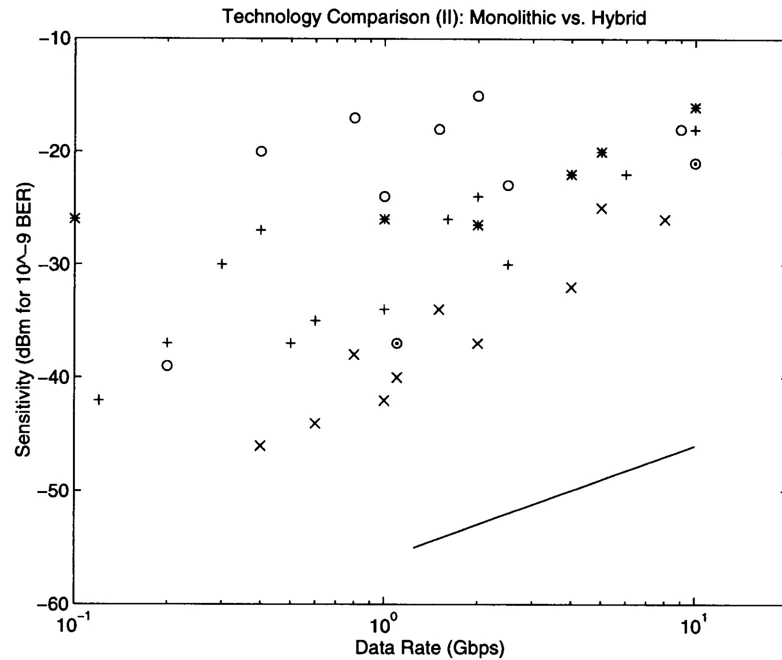

Figure 1.5: Receiver results for monolithic OEICs and other hybrid approaches. The performances are evaluated based on their bit rate and sensitivity. The technology categories are: GaAs MESFET OEICs (o); InGaAs HBT OEICs ($*$); InGaAs FET OEICs (+); PIN Hybrids ($\odot$); APD Hybrids ($\times$); optical amplifier hybrids($\oplus$). The solid line in the bottom right corner is the quantum limit for an ideal receiver.

1.3 Thesis Background

1.3.1 A High Speed Optical Receiver System at Lincoln Lab

Figure 1.6 shows a block diagram of the experimental communication system for the testing of the proposed monolithic receivers. The testing signal is generated by the transmitter, which is based on a master oscillator power amplifier architecture, with the split functions of high speed modulation and high optical power generation between different devices that have been separately optimized. In other words, an external modulator is used to allow the master laser to be chosen without regard to its modulation properties. The phase modulator was implemented with a $LiNbO_3$ Mach-Zehnder, which results in a modulation format very similar to differential phase

shift keying (DPSK).

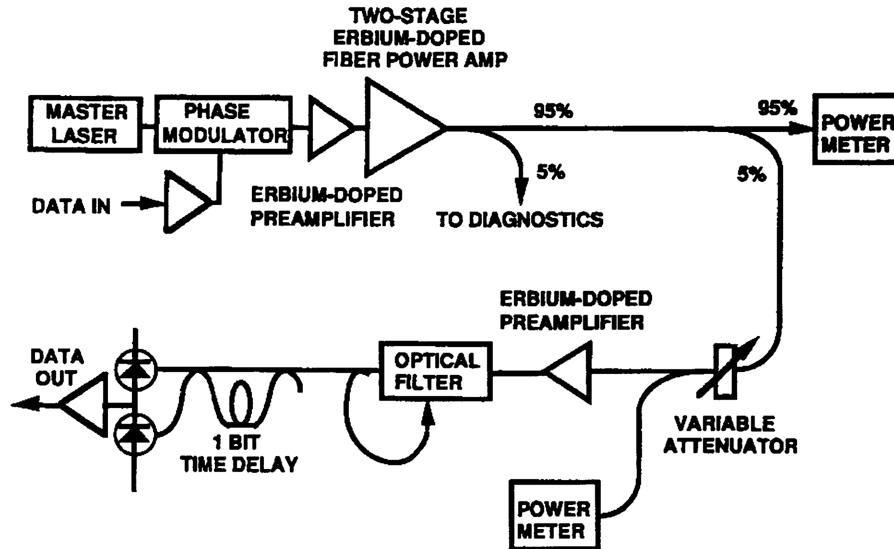

Figure 1.6: Block diagram of a optically amplified, high speed DPSK communication receiver system [46, 47].

A two stage erbium-doped fiber amplifier, pumped by a tapered-gain-region semiconductor pump laser at 980nm, acts as the optical power amplifier. Each stage is pumped by a pair of lasers which are polarization multiplexed. A low power amplifier was inserted between the external modulator and the input to the two-stage power amplifier to boost the master laser signal to the 5 mW level needed to saturate the power amplifier.

Right after the optical amplifier, there is an isolator (not shown in the Figure 1.6) which is polarization dependent to eliminate the amplified spontaneous emission in the polarization orthogonal to the signal and to lower the power level incident onto the tunable fiber Fabry-Perot pre-filter so as to reduce the possibility of optical power damage. By using polarization-dependent filtering after the optical preamplifier, the receiver sensitivity is increased at the cost of having to control the input polarization.

The DPSK receiver consists of a backward-pumped erbium-doped fiber amplifier (EDFA), an optical filter, a Mach-Zehnder interferometer with a 1-bit delay in one arm, and dual balanced receiver, the output of which was amplified with a 50Ω amplifier and sent to a bit error detector.

Figure 1.7 shows the detailed block diagram for the receiver front end. After the 1-bit delay line, the optical signal is fed into the dual balanced photodetectors. The generated photocurrent is converted into voltage through the first stage electrical amplifier which is a transimpedance amplifier. Then the preamplified signal goes through second stage amplifier which is either an automatic gain control (AGC) amplifier or a limiting amplifier. Finally, the following clock recovery and decision circuits will extract the information out from the fully amplified data stream.

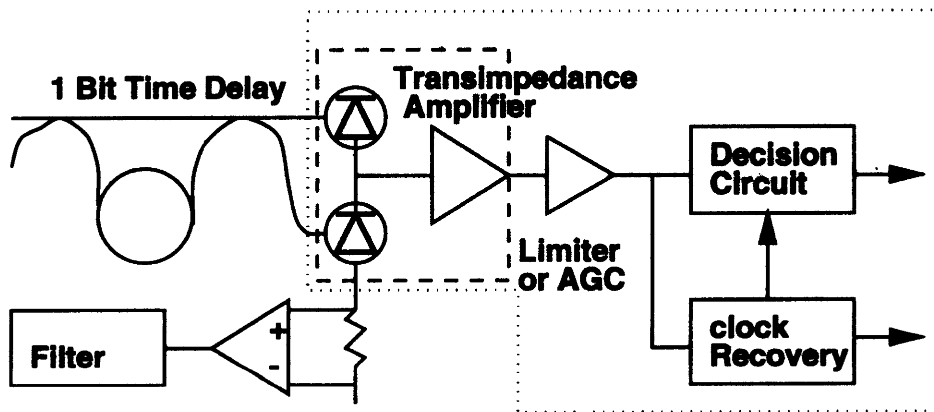

Figure 1.7: Block diagram of the proposed DPSK demodulator front-end. The current goal is to replace the $3in \times 4in$ hybrid dual-balanced detector-transimpedance-amplifier module with a monolithic OEIC chip of greatly reduced size. Eventually, the additional signal processing electronics such as the clock recovery, limiter, and the decision circuit can also be integrated once the technology has been established.

In this front-end architecture, the dual balanced photodetectors are favored. The

balanced receiver have been shown to be useful in suppressing local oscillator (LO)[4] excess intensity noise [48]. In addition, such a receiver requires less local-oscillator power than does a conventional single-detector receiver so that it can efficiently use the available signal and local oscillator power. This advantage is particularly important for high-bit-rate optical heterodyne systems, since the receiver thermal noise increases rapidly in typical PINFET front end as the intermediate frequency is increased. Hence, to ensure that LO shot noise dominates thermal noise (as desired for maximum sensitivity), LO power must be increased for high-speed applications so that a receiver sensitivity very close to the quantum limit can be achieved.

In the current configuration of the DPSK dual balanced optical receiver front end, several hybrid packages are included for the 1-bit delay line, the dual balanced receiver and the preamplifier, and the AGC/clock recovery/decision circuits. The construction of these packages often involve substantial amount of time and effort, and the resulting packages usually have extensive sizes.

For example, the balanced detector and pre-amp package has a size of 3in by 4in. In the course of the construction of this package, tedious labor is used to carefully align the fiber to each of the two detectors individually, followed by the equally time-consuming effort for responsivity matching between two detectors.

In this thesis research, the dual balanced photodetectors will be monolithically integrated with a transimpedance amplifier. The monolithic integration of twin-detectors can exhibit significant advantages; it is obvious that well balanced coupling efficiency to both detectors can be obtained by a single alignment procedure. This will minimize the effort for the alignment and achieve superior performance at a greatly reduced size.

Another advantage is that, in the proposed monolithic process, two photodetectors

[4]The input optical signal is beaten by a local laser called local oscillator to utilize the heterodyne technique. The transmitter in the experimental system described in the Figure 1.6 no longer exist.

are fabricated in close proximity, thus sensitivity and optical and electrical path length can be well balanced between the two. The equalization of the path length is of great importance at high signal bit rates at which the time delay difference limits the performance. It also minimizes the connections inductive and capacitive effects which limit the electrical response in the high frequency range and usually produce poor balance.

Eventually, the rest of the signal processing circuits including AGC, clock recovery, and decision circuits can also be included in the same chip therefore reducing the inductive and capacitive effects incurred in the current packaging and connection, and eliminating the bulky size of the current system. Once this proposed technology is developed, the integration of more complete VLSI OEICs will be straightforward.

1.3.2 Integration of High Speed Optical Receiver

Generally, an optical receiver's front-end design can be categorized into four basic configurations: (1) resistor termination with a low-impedance voltage amplifier; (2) high-impedance amplifier; (3) transimpedance amplifier; (4) noise-matched or resonant amplifier. We shall compare the pros and cons of the first three options for our construction of optical receivers. The last one is not considered here.

The front-end of an optical receiver responds to an optical signal by generating a photocurrent with a photodetector. The photocurrent is then converted to a voltage. Electronic signal processing stages process the recovered voltage to extract the desired information.

The principle attraction of the low-impedance voltage amplifier front-end is its simplicity and potential for wide bandwidth. In the simplest optical receiver front end, the photodiode can be either AC coupled or DC coupled to a low impedance voltage amplifier. One drawback of an AC coupled front-end is that low-frequency

components in the photocurrent that may contain useful information can be lost. In some cases, because reduction in low frequency information is intolerable, DC coupling is required. However the DC coupled amplifier with high gain and wide bandwidth can be very challenging to construct because of exacting feedback stabilization and power supply requirements.

The thermal-noise associated with the load resistor dominates the receiver noise in the resistor-terminated low-impedance voltage amplifier front-end. The high-impedance amplifier is an approach that substantially reduces the effect of the thermal-noise of the load resistor, resulting in improved sensitivity. The basic principle is to load the current-source with as large an impedance as possible, which maximizes the amount of voltage developed at the input of the amplifier, the idea being that since the voltage is maximized, the effects of any amplifier noise source will be reduced. The ability to realize a high impedance is ultimately limited by the capacitance present in the circuit. In order to obtain a flat receiver passband, the response must be equalized. In general, the high-impedance receiver results in the lowest noise baseband front-end that can be realized without extraordinary effort [49].

A front-end architecture that provides a good compromise between the low-noise characteristics of the high-impedance front-end and the wideband nature of the low-impedance voltage amplifier front-end is known as the transimpedance amplifier (TIA). The amplifier utilizes shunt feedback around a inverting amplifier to stabilize the amplifier's transimpedance. Since the feedback stabilizes the transimpedance and since the transfer function of an optical front-end is inherently a transimpedance, this amplifier is particularly useful in optical communication receivers.

Chapter 2

Design of 1.55μm Photodetectors

Several types of photodetectors have been employed, to various degrees, for lightwave applications. In roughly ascending order of structural complexity, the lightwave photodetectors are photoconductors, metal-semiconductor-metal (MSM) photodiodes, p-i-n photodiodes, phototransistors, and avalanche photodiodes (APD). Photoconductors and phototransistors have not been widely utilized for either monolithic or hybrid lightwave receivers. Photoconductors are limited by their relatively slow speed of response, and phototransistors have not exhibited a performance advantage compared to the p-i-n/FET combinations. Avalanche photodiodes, on the other hand, have been successfully implemented in many hybrid receiver circuits. However, APDs have not been incorporated into monolithic receiver OEICs. One reason for this is the complexity of the APD structure. The APDs that have achieved the best performance, such as the separated absorption and multiplication (SAM) APD, are multilayer structures and their performance is very sensitive to the parameters of the constituent layers. In addition, the high bias voltages, temperature stabilization, and rigorous bias control required by APDs have made them unattractive for the development of monolithic OEICs. At present, monolithic receivers rely almost entirely on p-i-n photodiodes

or MSM photodetectors. Most recently, a novel Uni-Traveling-Carrier PhotoDiode (UTC-PD) has been proposed as a device for achieving both high output and fast response and become a potential candidate for the ultra high-speed OEICs.

In this Chapter, the theoretical analysis of three kinds of photodetectors, namely p-i-n photodetectors (Section 2.1), MSM detectors (Section 2.2), and uni-traveling carrier photodetectors (UTCPD)(Section 2.3), are presented. The derived design curves for both p-i-n photodetectors and MSM photodetectors are displayed. Also in Section 2.3, a new design scheme applying the bandgap engineering is proposed for the uni-traveling carrier photodetectors. The optimal design of flatband UTCPD potentially can yield even faster photoresponse than the present UTCPDs.

2.1 p-i-n Photodetectors

The p-i-n photodiode has become the most widely deployed photodetector for all lightwave applications including OEICs. The performance characteristics of p-i-n photodiodes, such as noise, bandwidth, dark current, and photoresponse, are well understood and documented. Since the depletion layer thickness can be tailored to optimize the quantum efficiency and frequency response, the p-i-n structure is usually quite versatile for a wide range of specifications. The high quantum efficiency as well as the low dark current make the p-i-n photodetector an ideal candidate for the proposed monolithically integrated optical receiver.

Figure 2.1 displays the details of the p-i-n photodiode operation. The impinging light produces hole-electron pairs in the semiconductor. Pairs produced in the depletion region, or within a diffusion length of it, will eventually be separated by the electric field, leading to the current flow in the external circuit as carriers drift across the depletion layer.

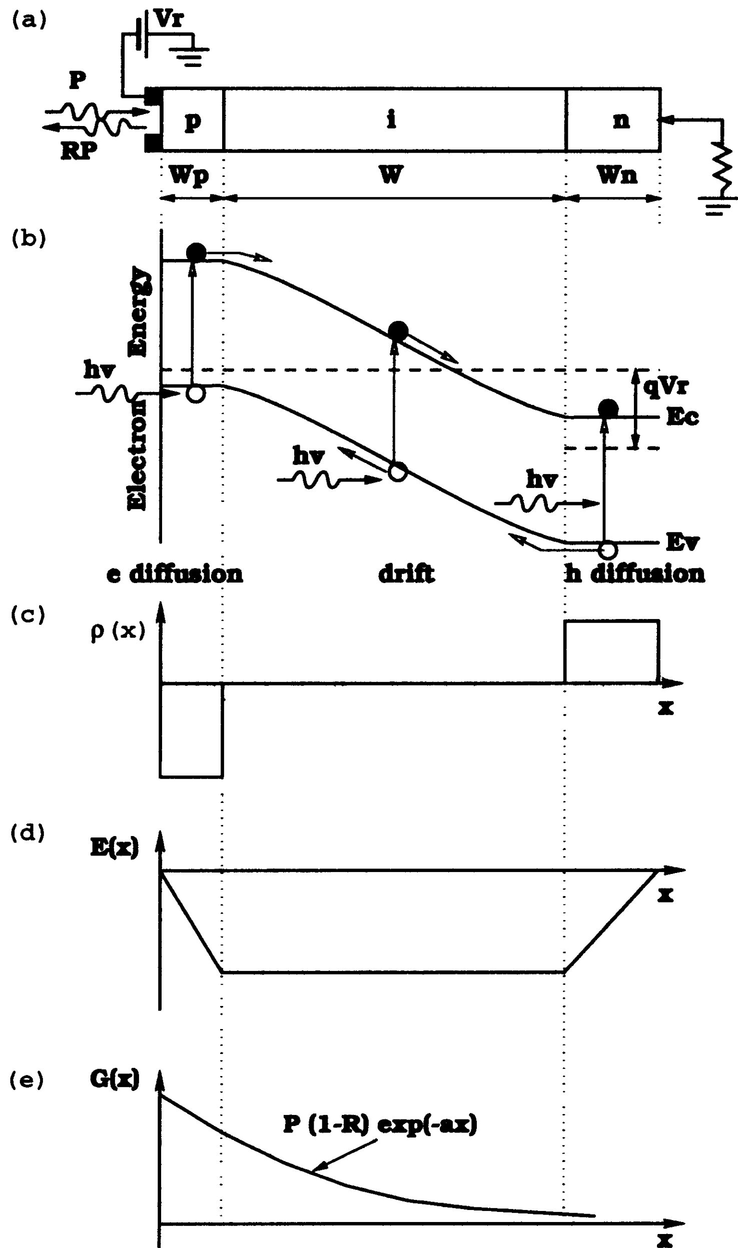

Figure 2.1: Operation of the p-i-n photodiodes. (a) Cross sectional view of a reverse-biased p-i-n photodiode under optical illumination from the p+ side. (b) Energy band diagram under reverse bias. (c) The charge density $\rho(x)$ under depletion approximation. (d)The static electric field profile $E(x)$. (e)Carrier generation rate $G(x)$.

2.1.1 General Statement of the Transport Problem

The equations for carrier transport in the intrinsic region of a reverse-biased p-i-n diode are the continuity equations for electrons and holes:

$$\frac{\partial n}{\partial t} = G - \frac{n - n_0}{\tau_0} + \frac{1}{q}\nabla \cdot \mathbf{J_n} \tag{2.1}$$

$$\frac{\partial p}{\partial t} = G - \frac{p - p_0}{\tau_0} - \frac{1}{q}\nabla \cdot \mathbf{J_p} \tag{2.2}$$

where n and p are densities of the holes and electrons; p_0 and n_0 are the equilibrium densities of the holes and electrons; G is the volume rate of generation of pairs; q is the electronic charge; and τ_0 is the carrier lifetime in the semiconductor; $\mathbf{J_n}$ and $\mathbf{J_p}$ are the hole and electron current densities, including both drift and diffusion terms, and are given by:

$$\mathbf{J_n} = q\mu_n\mathbf{E} + qD_n\nabla n \tag{2.3}$$

$$\mathbf{J_p} = q\mu_p\mathbf{E} - qD_p\nabla p \tag{2.4}$$

where D_n and D_p are the electron and hole diffusion coefficients; μ_n and μ_p are the electron and hole mobilities; and **E** is the electric field present in the depletion region.

The total current in the i region is given by:

$$\mathbf{J} = \mathbf{J_n} + \mathbf{J_p} + \epsilon\epsilon_0\frac{\partial \mathbf{E}}{\partial t} \tag{2.5}$$

where ϵ is the dielectric constant of the semiconductor material, ϵ_0 is the permeability of free space, and the third term on the right is the displacement current density.

After the electron and hole pairs are generated in the depletion region, the external applied electric field will tend to separate the pairs and move them towards opposite directions. Space charge results since the motion of the carriers takes time and usually

is asymmetric. In order to take into consideration the space charge perturbation on the electric field, the Poisson's equation must be satisfied:

$$\nabla \cdot \mathbf{E} = \frac{q}{\epsilon\epsilon_0}(p - n) \tag{2.6}$$

The presence of space charge will make the continuity Equation 2.1 and 2.2 coupled and nonlinear. This becomes clear when we plug the expressions for the current densities and Poisson's equation into 2.1 and 2.2:

$$\begin{aligned} \frac{\partial n}{\partial t} &= G - \frac{n - n_0}{\tau_0} + \nabla \cdot [\mu_n n \mathbf{E} + D_n \nabla n] \\ &= G - \frac{n - n_0}{\tau_0} + \mu_n \mathbf{E} \cdot \nabla n + \mu_n \frac{q}{\epsilon\epsilon_0} n(p - n) + D_n \nabla^2 n \end{aligned} \tag{2.7}$$

$$\begin{aligned} \frac{\partial p}{\partial t} &= G - \frac{p - p_0}{\tau_0} - \nabla \cdot [\mu_p p \mathbf{E} - D_p \nabla p] \\ &= G - \frac{p - p_0}{\tau_0} - \mu_p \mathbf{E} \cdot \nabla p - \mu_p \frac{q}{\epsilon\epsilon_0} p(p - n) + D_p \nabla^2 p \end{aligned} \tag{2.8}$$

However, under usual physical conditions of interest, the equations can be linearized and the analytical solutions can be obtained. Since the illumination comes from only one side of the p-i-n photodetectors, in majority applications, the problem is simply one dimensional. The transport equations described above then transform to:

$$\frac{\partial n}{\partial t} = G - \frac{n - n_0}{\tau_0} + \mu_n E \frac{\partial n}{\partial x} + \mu_n \frac{q}{\epsilon\epsilon_0} n(p - n) + D_n \frac{\partial^2 n}{\partial x^2} \tag{2.9}$$

$$\frac{\partial p}{\partial t} = G - \frac{p - p_0}{\tau_0} - \mu_p E \frac{\partial p}{\partial x} - \mu_p \frac{q}{\epsilon\epsilon_0} p(p - n) + D_p \frac{\partial^2 p}{\partial x^2} \tag{2.10}$$

2.1.2 Linearization of the Transport Equations

Following the phenomenological argument proposed by G. Lucovsky et al. [50], it can be shown that the perturbation of the field resulting from light generated space charge is negligible for normal operation of the p-i-n photodiodes. The space charge generates a self electric field in the intrinsic region, opposing the field due to the external bias. Considering the p-i-n structure as a parallel plate capacitor with the plate separation equal to the thickness L of the intrinsic region, the magnitude of the external field and the self electric field can be compared.

To maintain the external field E_0, the charge stored on one plate of the capacitor is given by $Q = \epsilon\epsilon_0 E$. For the given electron-hole pair generation rate G per unit volume per second, the space charge stored in the intrinsic region in the steady state can be estimated to be $qLG\tau_{n(p)}$, where $\tau_{n(p)}$ is the transit time for the carrier to sweep out from the intrinsic region, i.e., $\tau_n = L/(2\mu_n E_0)$ for electrons and $\tau_p = L/(2\mu_p E_0)$ for holes. In order to make the perturbation on the field small, it is required that $Q \gg qLG\tau_{n(p)}$. This is equivalent to the condition of:

$$E_0^2 \gg \frac{L}{2\mu_{n(p)}\epsilon\epsilon_0} J_L \tag{2.11}$$

where J_L is the photocurrent density in the diode, and $J_L = qGL$.

For $In_{0.53}Ga_{0.47}As$ p-i-n photodetectors, with an i region thickness of $1.5\mu m$, an electron mobility of 10000 cm^2/Vs, and a hole mobility of 240 cm^2/Vs, the Equation 2.11 becomes $E_0 \gg 2.73 \times 10^5 J_L$, with E_0 in V/m, and J_L in A/m^2. It is usually customary and advantageous to operate these diodes at biases which produce the electric field of about 10^5V/cm and saturate the carrier drift velocity, then the above condition is easily satisfied for photocurrent densities as large as 10 A/cm^2. If the field perturbation by photo generated carriers is small, the $\nabla \cdot \mathbf{E}$ terms or the $(p-n)$

terms in Equation 2.7 and 2.8 can be neglected.

On the other hand, the recombination terms $(n - n_0)/\tau_0$ and $(p - p_0)/\tau_0$ in Equation 2.9 and 2.10 can also be neglected if the carrier transit time is much smaller than the carrier recombination lifetime in the intrinsic region. For $In_{0.53}Ga_{0.47}As$ photodiodes, the lifetime is $10^{-9}s$ while the hole transit time to cross 1.5μm intrinsic region at the saturation velocity of $5 \times 10^6 cm/s$ is about $3 \times 10^{-13}s$. The light generated carriers are swept out of the i region before any appreciable recombination can occur.

Next, let us compare the magnitude of the diffusion current density to the total current density. To do so, we need to estimate the quantity $(p - n)$. Again, the space charge accumulation is estimated as $qGL\tau_{n(p)} = qGL^2/2\mu_{n(p)}E_0$. For most semiconductors including $In_{0.53}Ga_{0.47}As$, $\mu_n \gg \mu_p$ therefore, $(p - n) \approx p$. Then only photo-generated holes are considered in the charge accumulation. Therefore, $\int_0^L qp(x)dx = qGL^2/2\mu_p E_0$. If we assume that the photo generated holes are linearly distributed in the i region, we can estimate hole densities as $p(x) = (G/\mu_p E_0)x$. Then the diffusion current term compared with the total photo current of qGL results:

$$\frac{qD_p \nabla p}{qGL} = \frac{D_p}{\mu_p E_0 L} = \frac{kT/q}{E_0 L} \tag{2.12}$$

It is now clear that the diffusion current may be neglected provided that the applied reverse bias is much larger than kT/q, which is about $26mV$ at room temperature.

Finally, the continuity equations can be simplified to be the following linear equations for the one-dimensional case:

$$\frac{\partial n}{\partial t} = G + \mu_n E \frac{\partial n}{\partial x} \tag{2.13}$$

$$\frac{\partial p}{\partial t} = G - \mu_p E \frac{\partial p}{\partial x} \tag{2.14}$$

And the current density is given by:

$$J = q(\mu_p p + \mu_n n) + \epsilon\epsilon_0 \frac{\partial E}{\partial t} \tag{2.15}$$

2.1.3 Calculation Results

The above equations can be easily solved for most practical occasions, and most frequently, the two cases where the light is incident on either the p side or the n side. The frequency response of current density to the sinusoidal variation of the incident lights are obtained for these two cases [50]:

If the light is incident on the p side of the p-i-n structure,

$$\begin{aligned} \frac{J}{J_0} = 1 & + \frac{Ae^{i\omega t}}{[\alpha L + (i\omega L)/\mu_p E_0]} \left[1 - \frac{\alpha L e^{-\alpha L}}{1 - e^{-\alpha L}} \frac{1 - e^{-i\omega L/\mu_p E_0}}{i\omega L/\mu_p E_0}\right] \\ & + \frac{Ae^{i\omega t}}{(i\omega L/\mu_n E_0) - \alpha L} \left[1 - \frac{\alpha L}{1 - e^{-\alpha L}} \frac{1 - e^{-i\omega L/\mu_n E_0}}{i\omega L/\mu_n E_0}\right] \end{aligned} \tag{2.16}$$

If the light is incident on the n side of the p-i-n structure,

$$\begin{aligned} \frac{J}{J_0} = 1 & + \frac{Ae^{i\omega t}}{[-\alpha L + (i\omega L)/\mu_p E_0]} \left[1 - \frac{\alpha L}{1 - e^{-\alpha L}} \frac{1 - e^{-i\omega L/\mu_p E_0}}{i\omega L/\mu_p E_0}\right] \\ & + \frac{Ae^{i\omega t}}{(i\omega L/\mu_n E_0) + \alpha L} \left[1 - \frac{\alpha L e^{-\alpha L}}{1 - e^{-\alpha L}} \frac{1 - e^{-i\omega L/\mu_n E_0}}{i\omega L/\mu_n E_0}\right] \end{aligned} \tag{2.17}$$

$J_0 = qG(1 - e^{-\alpha L})$ is the normalization factor for both equations. It is evident from the above solutions that the detectors illuminated from the p-side will have faster transit time response than those illuminated from the n-side, since in the former case, it is mostly the electrons that will travel across the i region. In $In_{0.53}Ga_{0.47}As$ photodetectors, the saturation velocity for electron is usually as twice faster as that of holes.

Figure 2.2 shows that the p-side illuminated p-i-n photodiodes have faster transit

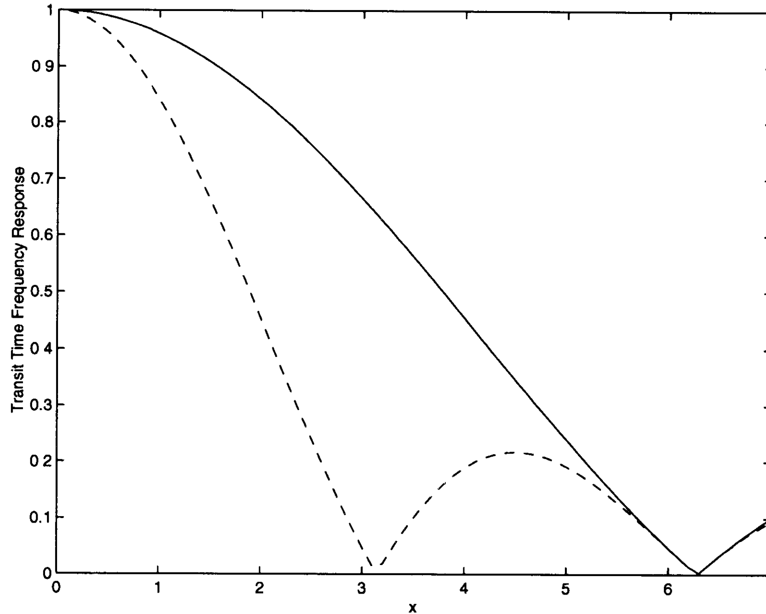

Figure 2.2: Transit time frequency response comparison between p-side and n-side illuminated p-i-n photodiodes. The solid line is for p-side illuminated while the dashed line is for the n-side illuminated. The x axis is based on the normalized factor $x = \omega\tau_n = \omega L/2\mu_n E_0$ for p-side illuminated and $x = \omega\tau_p = \omega L/2\mu_p E_0$ for n-side illuminated.

response. This is especially important for devices with thicker intrinsic region where the asymmetric light injection and carrier transportation will exhibit greater effect. For uniformly illuminated devices, the transit response falls between the above two cases and has moderate speed.

The above transit-time consideration suggests the use of thin intrinsic layers to achieve fast response knowing that the quantum efficiency will be traded off. However, in practical applications, the inherent capacitance of the detectors plus any parasitic capacitance causes the bandwidth to decrease for very thin intrinsic layers since it takes time to charge and discharge these capacitance. Consequently, for any given device area, there is an optimal intrinsic layer thickness that yields the maximum

bandwidth. This is displayed in Figure 2.3. The compromise between the transit time constraint and the RC time constraint is commonly involved in a good OEIC design.

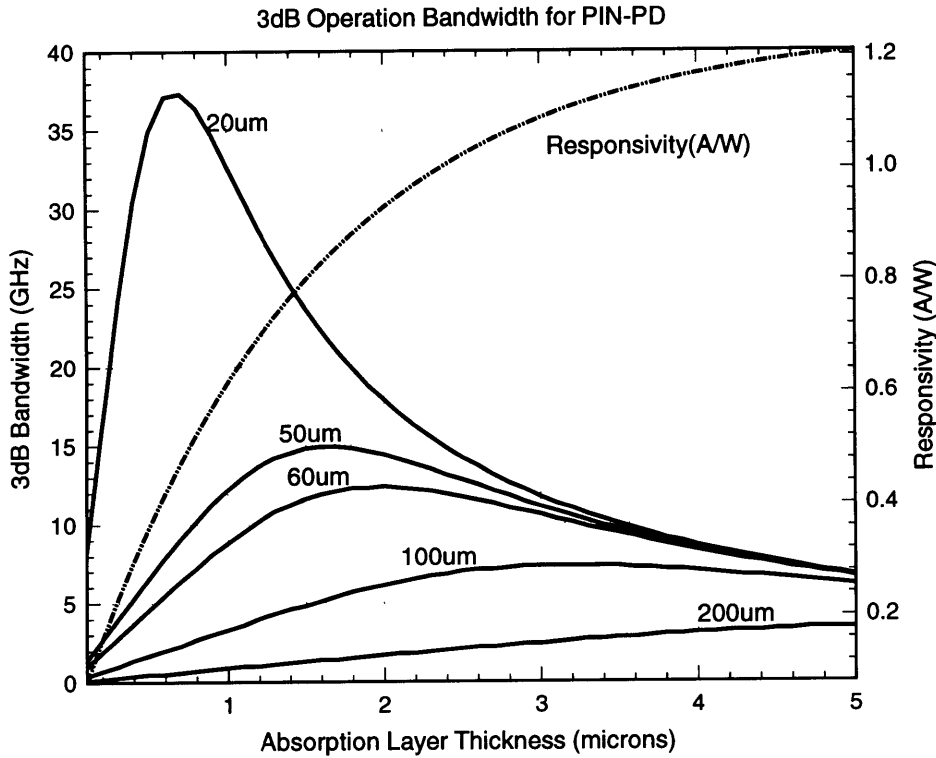

Figure 2.3: The design curves for $In_{0.53}Ga_{0.47}As$ PIN photodetectors. For given geometry of the detectors, the corresponding responsivity and 3dB bandwidth are shown.

In the calculation of Figure 2.3, it is assumed that the sum of the load resistance (R_L) and the detector serious resistance (R_S) equals 50Ω. The parasitic inductance is assumed to be zero and the detector capacitance is estimated using parallel plate capacitor model.

The tradeoff between the speed and quantum efficiency of the p-i-n photodetectors is plotted in Figure 2.4. For the specific cases in the later development of this thesis work, the intrinsic layer thickness for the fabricated p-i-n photodetectors is about

1.5μm, which corresponds to a quantum efficiency of 56% without the anti-reflection (AR) coating. For the usual device sizes of 25 $\sim$ 200μm in diameter, the bandwidth of about 1 $\sim$ 15 Ghz is expected.

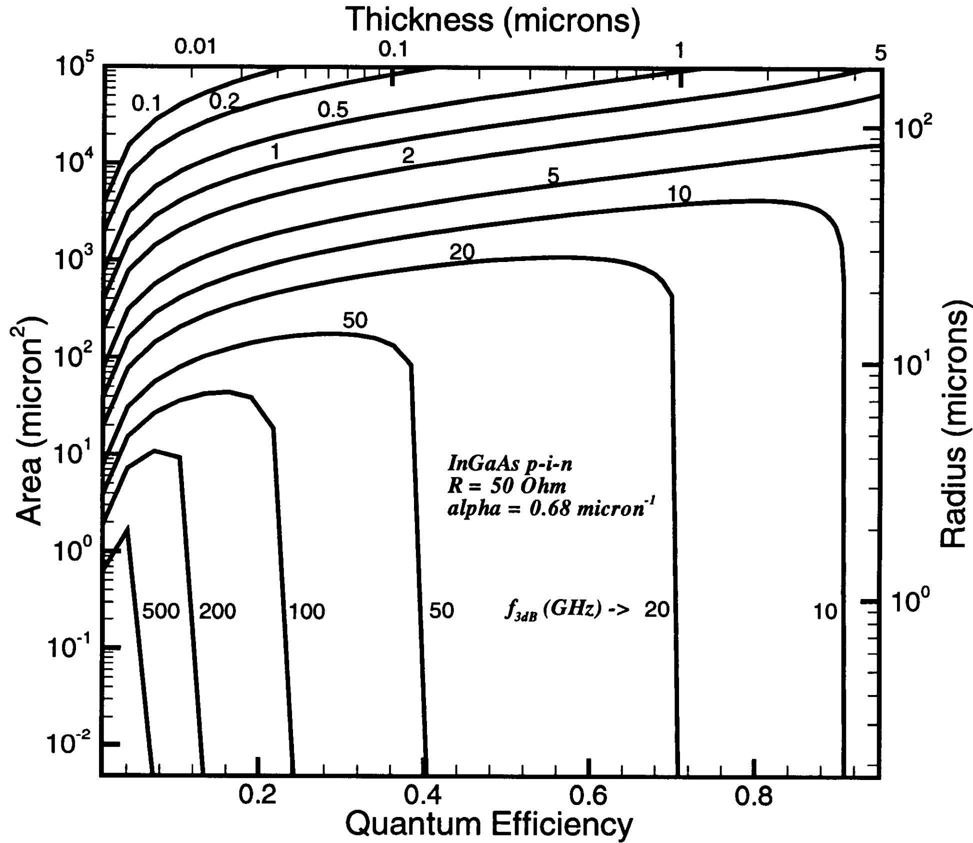

Figure 2.4: Constant 3-dB bandwidth contours in the area and intrinsic-layer-thickness plane for the $In_{0.53}Ga_{0.47}As$ 1.55μm p-i-n photodetectors. The parameters used in this calculation are: $\alpha = 0.68\mu m^{-1}$ for 1.55μm wavelength; $v_n = 7.0 \times 10^6$ cm/s and $v_p = 6.5 \times 10^6$ cm/s; and $\epsilon = 13.9$ for 1.55μm. AR-coating was assumed.

2.2 MSM Photodetectors

2.2.1 General Description

Another candidate for OEICs is the Metal-Semiconductor-Metal (MSM) detector. High-performance GaAs MSM's for use in the 0.8μm wavelength have proven easy to fabricate since good-quality Schottky barrier ($\sim 0.7V$) can be readily obtained on GaAs. Unfortunately, undoped InGaAs has a low Schottky barrier height ($\sim 0.2V$). This means that direct deposition of the electrodes on InGaAs gives detectors an unacceptably large leakage current even at low biases.

The positive attributes of the resulting MSMs are numerous. The principle advantage, derived from the simplicity of the planar contact configuration, is the compatibility with MESFET and HEMT circuitry. In addition, MSM photodiodes are relatively easy to fabricate, they do not add any processing difficulties to the OEICs. They also exhibit very low capacitance which permits relatively large-area device with negligible contribution to the total front-end capacitance. The bandwidth of MSMs can be very high for sufficiently narrow electrode spacing.

However, there are a few limiting factors in the performance of MSMs, such as higher dark current and lower quantum efficiency. It has been difficult to obtain low dark current in an MSM because the lateral current flow can be significantly influenced by the semiconductor surface or heterojunction interfaces.

A structure of 1.55μm MSM photodetector is illustrated in Figure 2.5. The detector consists of a set of interdigited electrodes deposited on a photoabsorbing semiconductor layer. Impinging photons generate electron-hole pairs in the semiconductor. The electric field due to the potential difference applied across the electrodes sweeps out these photocarriers. The corresponding flow of charge in the external circuit produces an electrical signal.

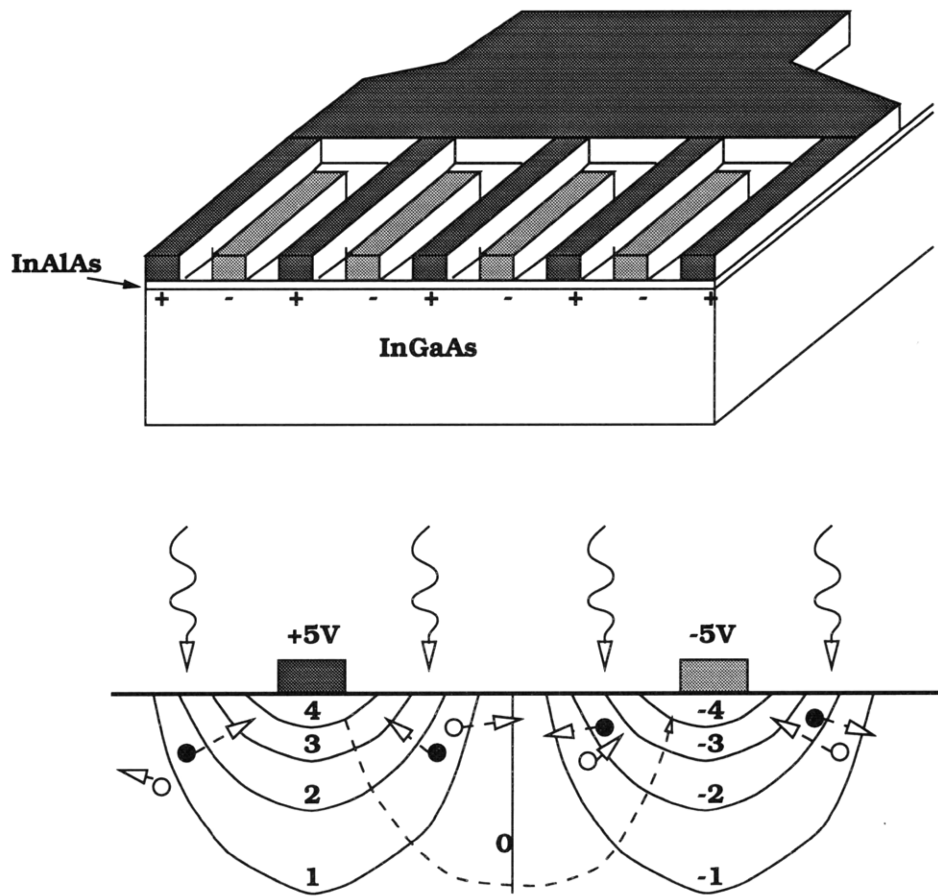

Figure 2.5: The design curves for $In_{0.53}Ga_{0.47}As$ MSM photodetectors. For given geometry of the detectors, the corresponding responsivity and 3dB bandwidth are shown.

2.2.2 Simulations and Design Guidance

A detailed analysis of the MSM photodetector operation involves the determination of the field distribution which amounts to solving Poisson's equation in two dimensions. A complete study for the MSM operating at both low and high levels of light intensity usually requires solving both Boltzmann's transport and Poisson's field equation self-consistently [51, 52].

On the other hand, at moderate input optical power level, the field perturbation by the photon-generated carriers can be ignored. Lim and Moore [53] used the conformal mapping and charted out the electric field distribution for the periodic structure exhibited in a MSM detector. Their result was used by Soole and Schumacher [54, 55] to analyze the transit time behavior of InGaAs-based MSM photodetectors. Later on, Gvozdić et al. [56] proposed a simpler conformal mapping to obtain an analytical expression for the electric field in MSM photodetectors. In their analysis, the semiconductor was considered to be intrinsic and the bulk carrier concentration was ignored. The thickness of photoabsorbing layer was assumed to be semi-infinite and the thickness of the metal electrodes was negligible.

Following Soole and Schumacher's analysis on transit time behavior as well as Lim and Moore's result on electric field/capacitance of MSM detectors, similar design guidance can be obtained for MSM configurations and implementation.

The capacitance of a MSM is given by [53]:

$$C = \frac{K(k)}{K(k')}\epsilon_0(1+\epsilon)\frac{A}{T} \tag{2.18}$$

where ϵ is the relative dielectric constant of the semiconductor, A is the interdigited area, $T = s + w$ is the period of the electrode with the finger width w and finger

spacing s, $K(\kappa)$ is the complete elliptic integral of the first kind,

$$K(\kappa) = \int_0^{\pi/2} \frac{1}{\sqrt{1-\kappa^2 \sin^2 \phi}} d\phi$$

$$k = \tan^2 \frac{\pi w}{4(s+w)}$$
$$k' = \sqrt{1-k^2}$$

Using Equation 2.18, the capacitance for three finger spacings, 1, 2, and 3μm, has been derived and plotted in Figure 2.6. It seems that MSM capacitance is a strong function of the finger spacing (s) rather than the finger width (w). For comparison purposes, the capacitance of p-i-n diodes with intrinsic layer thickness 0.5μm and 2.0μm is also plotted. It is evident that the capacitance of MSM diodes is much smaller than that of p-i-n diodes, which is the reason why the bandwidth of a receiver front end incorporating MSM detectors will usually be limited by transit time response rather than by RC response.

The external quantum efficiency is determined by the electrode structure and the thickness of InGaAs. If the electrode is opaque, the electrodes with finite width will block away partial input of the light. Taking into account this shadowing effect and the finite thickness of InGaAs, plus the loss due to the Fresnel reflection from the air-semiconductor interface, the total quantum efficiency is given by:

$$\eta_e = (1-R)\frac{s}{s+w}(1-e^{-\alpha t}) \tag{2.19}$$

where R is the Fresnel reflectivity which could be zero if anti-reflection coating is used; α is the absorption coefficient; t is the thickness of InGaAs layer.

Using Equation 2.19, the external quantum efficiency of InGaAs MSM detectors for several different electrode structures is calculated and displayed in Figure 2.7.

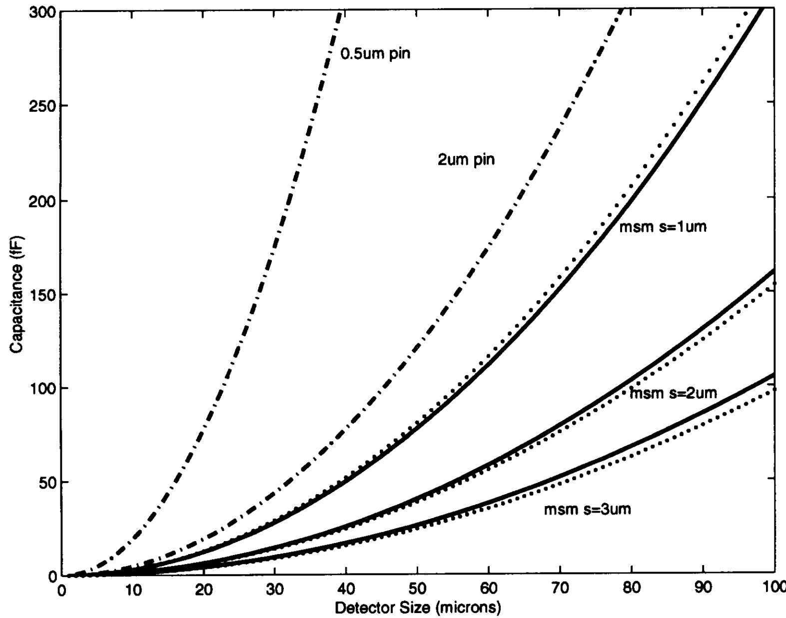

Figure 2.6: Capacitance versus detector size for 1, 2, 3 μm spacing MSM's. the solid lines are for 1μm wide electrodes, and the dotted lines for 0.5μm electrode widths. The capacitance of p-i-n with 0.5μm and 1.0μm intrinsic layer thickness is also plotted for comparison.

Without tedious carrier motion modeling, considering the electrode spacing (s) in a MSM as the counterpart of the intrinsic layer thickness (t) in a p-i-n diode, the transit-time frequency response for MSM can be approximated in similar fashion as it is done for uniformly illuminated p-i-n photodiodes. Assuming a load of 50Ω, the optimal MSM electrode configuration along with the achievable 3dB bandwidth, is displayed in Figure 2.8 for several given device areas.

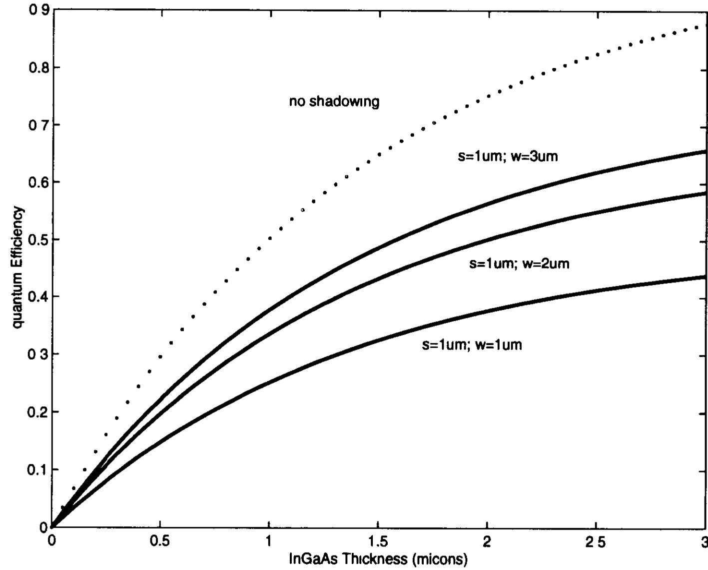

Figure 2.7: External quantum efficiency of the AR-coated MSM detectors as a function of the InGaAs thickness and the electrode structure. The calculation is based on 1.55μm wavelength with $\alpha = 0.68 \mu m^{-1}$.

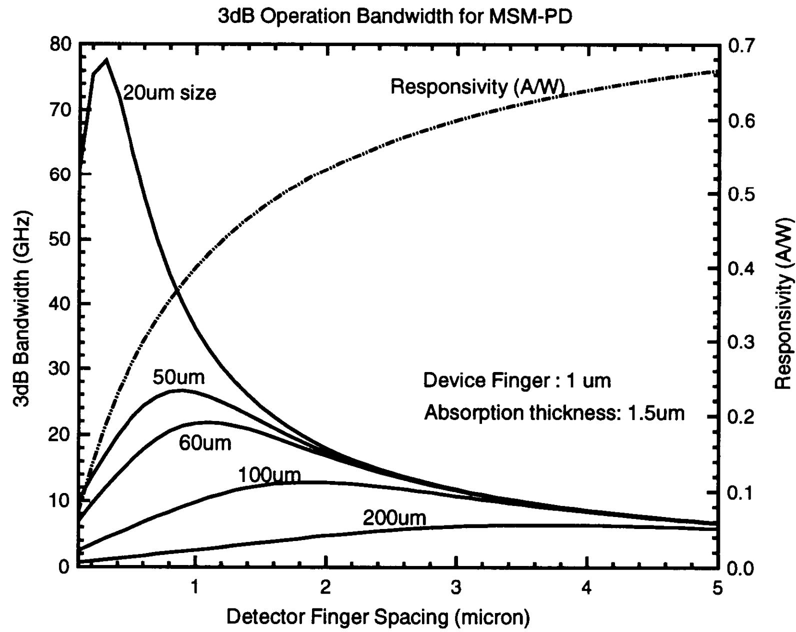

Figure 2.8: The design curves for $In_{0.53}Ga_{0.47}As$ MSM photodetectors. For given size and geometry of electrodes for the MSM detectors, the corresponding responsivity and 3dB bandwidth are shown.

2.3 Uni-Traveling-Carrier Photodetectors

2.3.1 The Invention of the UTC-PD

Design and optimizations have been made to improve the heterostructure p-i-n photodiodes in recent years. For scaled ultrafast p-i-n photodiodes, the transit time tends to be the dominant factor limiting the frequency response. It is then desirable to reduce the carrier transit time in order to improve the response. On the other hand, higher saturation current is important for better system implementation. For the conventional p-i-n photodetectors, achieving higher output photocurrent requires use of a larger area which is contradictory to the frequency response because of a larger RC time constant. Therefore, to suppress the field perturbation due to the large densities of photo generated carriers is the key to increase the photocurrent output.

Ishibashi et al. demonstrated a new design of photodetectors [57, 58] called Uni-Traveling-Carrier Photodiodes (UTC-PDs) where only electrons are the traveling carriers. The benefit comes as two-fold. On the one hand, utilizing the velocity overshoot effect of electrons [59], the electron velocity can be as high as 4×10^7 cm/s which is four times faster than the electron saturation velocity. The electrons thus are swept out of the depletion layer even more quickly than in conventional p-i-n photodiodes. On the other hand, in the traditional p-i-n photodetectors, space charge effect is dominated by holes due to their slower velocity. Getting holes out of the picture of the carrier transportation shall enhance the saturation current of the diodes.

The band diagram of such a UTC-PD is given in Figure 2.9. The active layer of the detector now consists of a p-type absorption layer and a wide-gap carrier collection layer. The photo-generated electrons will diffuse or drift into the collection layer while excess holes are swept out as conduction current in a quasi-neutral medium. The doping density in the absorption layer is carefully chosen, low enough in order

not to reduce both the light absorption coefficient and the electron mobility, but still high enough to be capable of driving higher current.

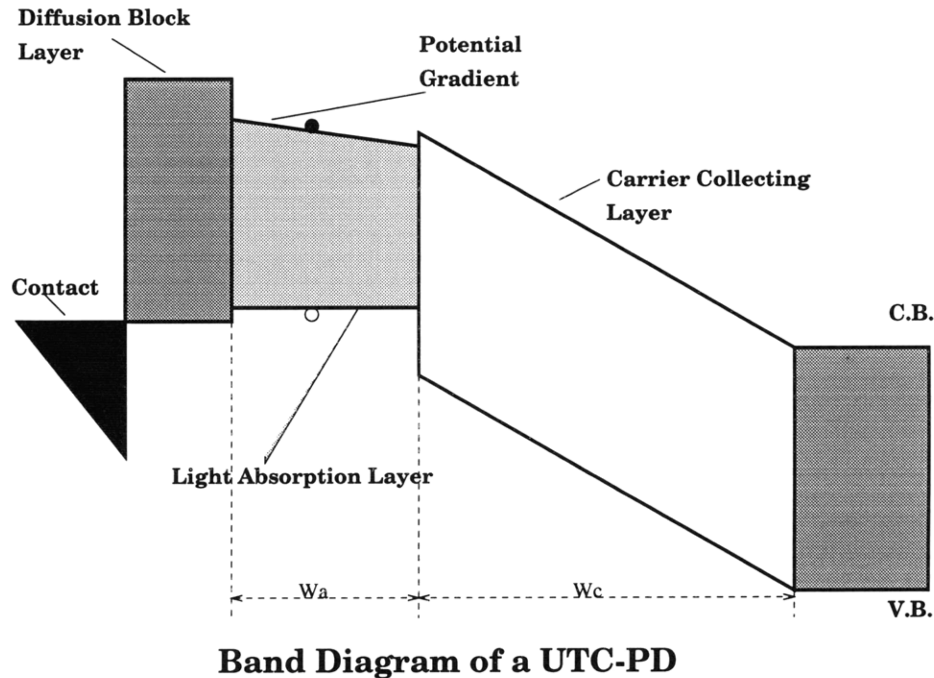

Figure 2.9: Band diagram of a Uni-Traveling-Carrier Photodiode. The wide-gap diffusion blocking layer is used to prevent photo-generated electron back diffused into anode.

Since the electron transports through the collection layer at the overshoot velocity, the delay of the transit in the collection layer only plays a secondary role. The major concern in the detector design is focused on the absorption layer where the electrons move at much slower pace.

2.3.2 Theoretical Analysis

Assuming the UTC-PD has a simplified structure with only an absorption layer (thickness W_A) and a collection layer (thickness W_C). The total current density J_{tot} is the

sum of the electron current J_n, hole current J_h, and displacement current $\epsilon\epsilon_0(\partial E/\partial t)$:

$$J_{tot} = \frac{1}{W_A + W_C} \int_0^{W_A+W_C} \left(J_n + J_h + \epsilon\epsilon_0 \frac{\partial E}{\partial t} \right) dx \tag{2.20}$$

Since there is no hole current in collection layer, the integration of $\partial E/\partial t$ over the entire diode length is zero in a short circuit condition, the total current can be rewritten as:

$$J_{tot} = \frac{1}{W_A + W_C} \int_0^{W_A} (J_n + J_h)\, dx + \frac{1}{W_A + W_C} \int_{W_A}^{W_A+W_C} J_n dx \tag{2.21}$$

The current components J_n and J_p are obtained by solving Equation 2.9 and 2.10, which can be rewritten to explicitly contain the electric field terms:

$$\frac{\partial n}{\partial t} = G - \frac{n - n_0}{\tau_0} + \frac{\partial}{\partial x} \left[\mu_n n(E_0 + E) + D_n \frac{\partial n}{\partial x} \right] \tag{2.22}$$

$$\frac{\partial p}{\partial t} = G - \frac{p - p_0}{\tau_0} - \frac{\partial}{\partial x} \left[\mu_p p(E_0 + E) - D_p \frac{\partial p}{\partial x} \right] \tag{2.23}$$

$$\frac{\partial E}{\partial x} = \frac{q}{\epsilon\epsilon_0}(p - n) \tag{2.24}$$

where E_0 is the existing quasi field which we will discuss in greater details later; E is the electric field induced by the photon-generated carriers. In our previous treatment for p-i-n photodetectors, E was neglected for the low level of light injection.

Since holes are majority carriers in the absorption region, $p \approx p_0$ as long as doping density p_0 is sufficiently high. Under the same condition, the hole drift current predominates over the hole diffusion current produced by the photon-generated holes. For electrons, either the quasi field can be designed to be much large, or under the small signal assumption for now, the drift term caused by the field perturbation E can

be ignored in comparison with the drift term due to E_0. The effect of E on electron transport should become important at high-level carrier injection. Nevertheless, the Equation 2.22 and 2.23 are reduced to:

$$\frac{\partial n}{\partial t} = G - \frac{\Delta n}{\tau_0} + \frac{\partial}{\partial x}\left[\mu_n \Delta n E_0 + D_n \frac{\partial \Delta n}{\partial x}\right] \tag{2.25}$$

$$\frac{\partial p}{\partial t} = G - \frac{\Delta p}{\tau_0} + \frac{\partial}{\partial x}\left[\mu_p p_0 E\right] \tag{2.26}$$

where Δn and Δp are photon-generated carrier densities. The equations are decoupled and linear. Both the electron density $n(x)$ and the electron current $J_n(x)$ can be calculated independent of the hole distribution. On the other hand, the hole current J_p changes complementarily with the change of the electron current J_n and the displacement current $\epsilon\epsilon_0(\partial E)/(\partial t)$ since the current continuity must be satisfied and $J_n + J_p + \epsilon\epsilon_0(\partial E)/(\partial t)$ should be constant at any position. Therefore, once the electron distribution current density in the absorption layer is determined, the total current response of the UTC-PD is determined.

Using the current continuity condition and the approximation of $J_p(x) = q\mu_h p_0 E(x)$, the total current response given by Equation 2.21 can be expressed for small sinusoidal signal solely in terms of the electron current $J_n(x,\omega)$ [58]:

$$\begin{aligned} J_{tot} &= \frac{1}{W_A + W_C}\int_0^{W_A} J_n(W_A,\omega)\left[1 - \frac{i\omega\tau_R}{1+i\omega\tau_R}\left(1 - \frac{J_n(x,\omega)}{J_n(W_A,\omega)}\right)\right] dx \\ &+ \frac{W_C}{W_A + W_C} J_n(W_A,\omega)\left[\frac{\sin(\omega\tau_C/2)}{\omega\tau_C/2}\right]\exp(-i\omega\tau_C/2) \end{aligned} \tag{2.27}$$

where $\tau_R = \epsilon\epsilon_0/\sigma = \epsilon\epsilon_0/q\mu_p p_0$ is the dielectric relaxation time of the absorption layer; $\tau_C = W_C/v_n$ is the electron traveling time in the collection layer. The task then is to calculate $J_n(x,\omega)$.

For the uniform illumination, the static electron distribution can be derived from Equation 2.28:

$$D_n \frac{\partial^2 n}{\partial x^2} - \mu_n E_0 \frac{\partial n}{\partial x} - \frac{n}{\tau_0} + G = 0 \tag{2.28}$$

where the photo-generated electron density Δn is replaced with n since $\Delta n = n - n_0 \approx n$. The generation solution obtained for the last equation is given by:

$$n(x,0) = C_1 \exp(m_1 x) + C_2 \exp(m_2 x) + G\tau_0 \tag{2.29}$$

where

$$m_1, m_2 = \frac{\mu_n E_0}{2D_n}\left[1 \pm \sqrt{1 + \frac{4D_n}{\tau_0 \mu_n^2 E_0^2}}\right]$$

C1, and C2 are constants determined by boundary conditions on the two sides of the absorption layer. In their original work, Ishibashi et al. considered the fact that there is a potential barrier at the absorption/collection hetero-interface so that the electron density can not be zero at the heterojunction. Instead, they postulate that the process for electron to cross the heterointerface is a thermionic-emission process with a thermionic emission velocity of $v_{th} = \sqrt{2kT/\pi m^*}$ (where k is Boltzmann constant and m^* is electron effective mass) in addition to the drift velocity that electrons acquire in the absorption region. The resulted constants C_1 and C_2 are then determined to be:

$$C_1 = \frac{1}{\Delta}\begin{vmatrix} \mu_n E_0 G\tau_0 & D_n m_2 - \mu_n E_0 \\ -v_{th} G\tau_0 & D_n m_2 e^{m_2 W_A} + v_{th} e^{m_2 W_A} \end{vmatrix} \tag{2.30}$$

$$C_2 = \frac{1}{\Delta}\begin{vmatrix} D_n m_1 - \mu_n E_0 & \mu_n E_0 G \tau_0 \\ D_n m_1 e^{m_1 W_A} + v_{th} e^{m_1 W_A} & -v_{th} G \tau_0 \end{vmatrix} \tag{2.31}$$

$$\Delta = \begin{vmatrix} D_n m_1 - \mu_n E_0 & D_n m_2 - \mu_n E_0 \\ D_n m_1 e^{m_1 W_A} + v_{th} e^{m_1 W_A} & D_n m_2 e^{m_2 W_A} + v_{th} e^{m_2 W_A} \end{vmatrix} \tag{2.32}$$

For InP/InGaAs UTC-PD, the static electron distribution is calculated and displayed in Figure 2.10.

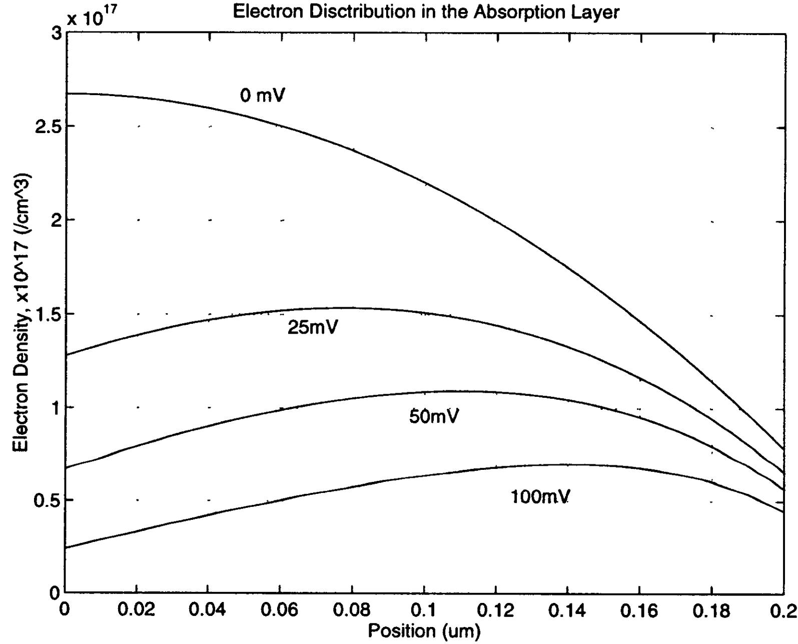

Figure 2.10: Electron distributions in the absorption layer of a Uni-Traveling-Carrier Photodiodes for four different potential gradient over the absorption layer.

The parameters used in the calculation are $\mu_n = 4000 cm^2/Vs$, $v_{th} = 2.5\times10^7 cm/s$, $W_A = W_C = 0.2\mu m$, and $G = 10^{29}/cm^3$.

To derive the frequency response, time-dependent Equation 2.22 is solved with all variables treated to have a small-signal perturbation that include $\exp(i\omega t)$. When

the electron transport in the absorption layer is dominated by diffusion, the dynamic electron concentration is approximated as:

$$\begin{aligned} n_{x,\omega} &= e^{i\omega t}\left[C_3\left(e^{\sqrt{(1+i\omega\tau_0)/\tau_0 D_n x}} + e^{-\sqrt{(1+i\omega\tau_0)/\tau_0 D_n x}}\right) + G\tau_0/(1+i\omega\tau_0)\right] \\ &\approx e^{i\omega t}\left[C_3\left(1 + x^2(1+i\omega\tau_0)/2\tau_0\right) + G\tau_0/1 + i\omega\tau_0\right], \\ C_3 &= -\frac{G\tau_0/(1+i\omega\tau_0)}{D_n W_A\left((1+i\omega\tau_0)/\tau_0 D_n\right)/v_{th} + (1 + W_A^2(1+i\omega\tau_0)/2\tau_0 D_n)} \end{aligned} \quad (2.33)$$

Then the approximated photocurrent is given by:

$$\begin{aligned} J_n(x,\omega) &= q\left[D_n \frac{\partial n(W_A,\omega)}{\partial x}\right] \\ &= -\frac{qGW_A}{1 + \left(W_A/v_{th} + W_A^2/2D_n\right)/\tau_0 + i\omega\left(W_A/v_{th} + W_A^2/2D_n\right)} \end{aligned} \quad (2.34)$$

The calculated frequency response for a UTC-PD is shown in Figure 2.11 along with a traditional p-i-n with corresponding structure. Also displayed in the Figure 2.11 is how the frequency response varies with the degree of velocity overshoot in a UTC and p-i-n.

Variation of the $3dB$ bandwidth as a function of absorption layer thickness $W_A = W_C$ is shown in Figure 2.12 along with that of the conventional p-i-n. It is shown that, without the quasi field in the absorption layer to enhance the electron diffusion, the UTCPD has no advantage over the conventional p-i-n photodiodes. With the build-in quasi field in excess of 100 mV, which can be easily achieved by either the dopant grading of two orders of magnitude across the absorption layer, or the compositional grading producing a energy bandgap difference of 100 meV across the absorption layer, the response of a UTCPD is faster than a p-i-n diode as long as the absorption thickness is thinner than 0.25μm. All calculation is performed for InGaAs p-i-n lattice matched to InP.

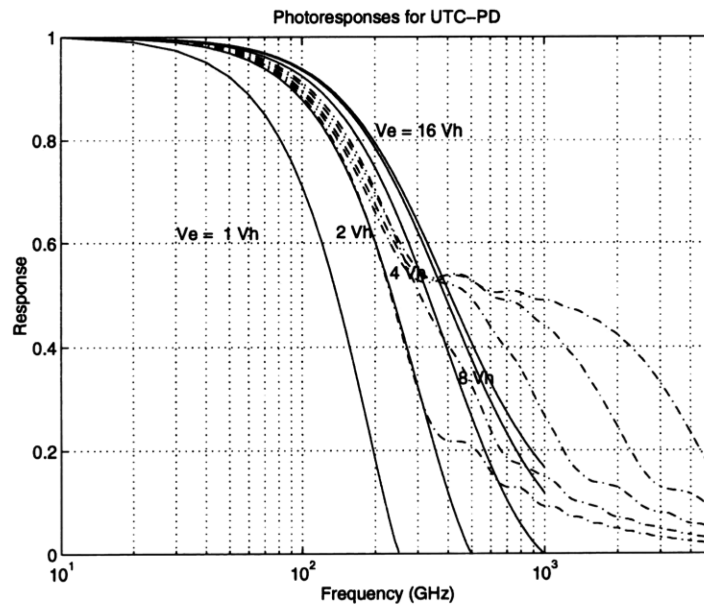

Figure 2.11: Calculated photoresponse of a Uni-Traveling-Carrier Photodiode and a conventional p-i-n photodiode. The potential gradient in the absorption layer of UTC-PD $\phi = 100mV$. Solid lines are for the UTC-PD while dotted lines are for p-i-n diodes. v_e is the electron overshoot velocity and v_h is the hole saturation velocity.

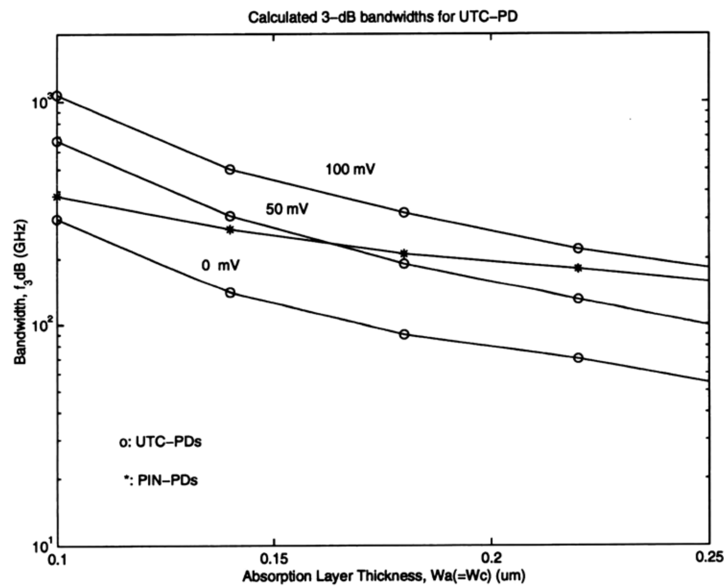

Figure 2.12: Calculated 3-dB bandwidth (f_{3dB}) for UTC-PDs with absorption layer thickness W_A ranging from $0.10\mu m$ to $0.40\mu m$. Results for conventional p-i-n PDs are also shown for comparison.

2.3.3 Heterojunctions with Flat Valence or Conduction Band

As we described in the last section, the band discontinuity at the absorption layer/collection layer heterointerface introduced a thermionic emission process which is ultimately a limitation on the detector response.

Based on the desired carrier transportation, the ideal band diagram for UTC-PD is illustrated in Figure 2.13. The flat conduction band edge at the absorption/collection interface helps sweep the electrons into the collection layer in a much faster fashion. The flat valence band edge at the absorption/dffusion barrier interface will impose less resistance for hole current.

In the detector demonstrated by Shimizu et al. [60], the p-InGaAsP barrier was carefully chosen at the contact layer side to minimize the valence band offset to facilitate the hole current, while the conduction band offset is sufficiently high to prevent electron diffuse back to the anode. At the collection layer side, the material choice was less optimized. A multiple layer undoped thin structure (starting from the p-type absorption layer, there are 20Å undoped InGaAs, 20Å undoped InP spacer layer, and 100Å n-type InP cliff layer) is used to minimize the effect of conduction band discontinuity.

However, with the advancement of most recent bandgap engineering, the flat band heterojunction becomes possible. Motivated to design low resistive p-type Distributed Bragg Reflectors (DBRs), several groups have demonstrated the feasibility of flat-band heterostructures both experimentally and theoretically [61, 62, 63, 64].

Using modulation doping of continuously graded isotype heterojunctions, one can realize arbitrary band edge variations, and the relationship between the doping profile and the grading function is analytic. Especially, a perfectly flat majority (or minority) carrier band edge can be realized by appropriate doping of any continuous grading scheme in isotype heterojunctions [63]. The carrier density as a function of

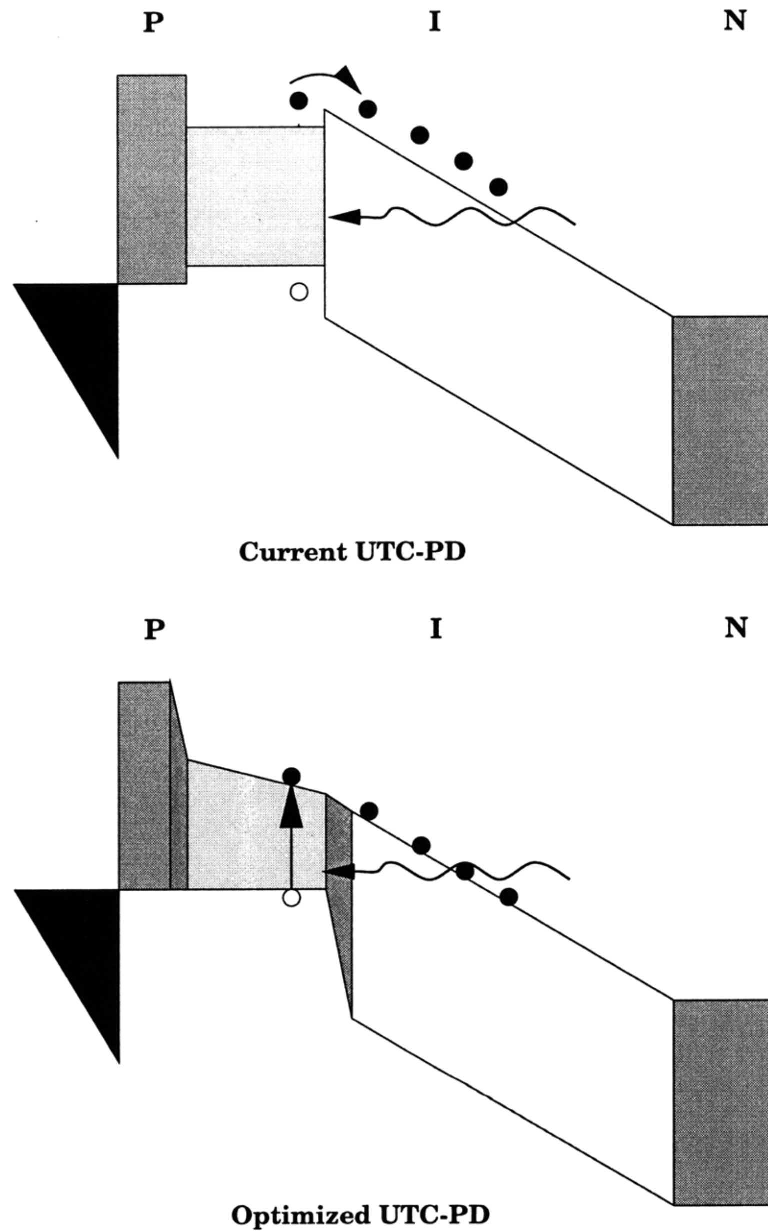

Figure 2.13: Ideal band diagram of a UTC-PD. (a)Recently demonstrated UTC-PD. Notice the discontinuity of the hetero-interfaces between top contact layer and absorption layer, and between absorption layer and collection layer. (b)An optimized band diagram.

the potential energy expressed in term of the valence band edge is given by:

$$\rho(x) = \frac{1}{q}\frac{d}{dz}\left[\epsilon(z)\frac{d}{dz}\left(E_V(z) + \Delta E_V(z)\right)\right] \tag{2.35}$$

where z is the physical distance across the heterointerface, ΔE_V is the difference in bandgap energy across the heterointerface.

The net ionized impurity distribution $N_D^+ - N_A^-$ that correspond to the specified band profile and space-charge distribution is given by:

$$N_D^+ - N_A^- = \rho/q - p + n \tag{2.36}$$

with the ionized deep-level distribution ignored.

The net ionized impurity distribution required for this type of heterojunction is obtained from Equation 2.35 and 2.36 by setting $dE_V(z)/dz = 0$:

$$N_D^+(z) - N_A^-(z) = \frac{1}{q^2}\frac{d}{dz}\left[\epsilon(z)\frac{d\Delta E_V(z)}{dz}\right] - p(z) \tag{2.37}$$

Hence, the doping profile $(N_D^+(z) - N_A^-(z))$ is determined by the material composition grading $(\Delta E_V(z))$ to satisfy the flat band condition $(dE_V(z)/dz = 0)$.

Assuming a parabolic graded heterojunction modeled as:

$$E = \begin{cases} E_c(z_1) + \frac{\Delta E_c}{2(z_2-z_1)^2}(z - z_1)^2 & \text{for } z_1 \leq z \leq z_2 \\ E_c(z_1) + \Delta E_c - \frac{\Delta E_c}{2(z_3-z_2)^2}(z - z_3)^2 & \text{for } z_2 \leq z \leq z_3 \end{cases} \tag{2.38}$$

A sample modulation doping profile required for a flat-band-edge potential is then displayed in Figure 2.14 for GaAs/AlAs material system.

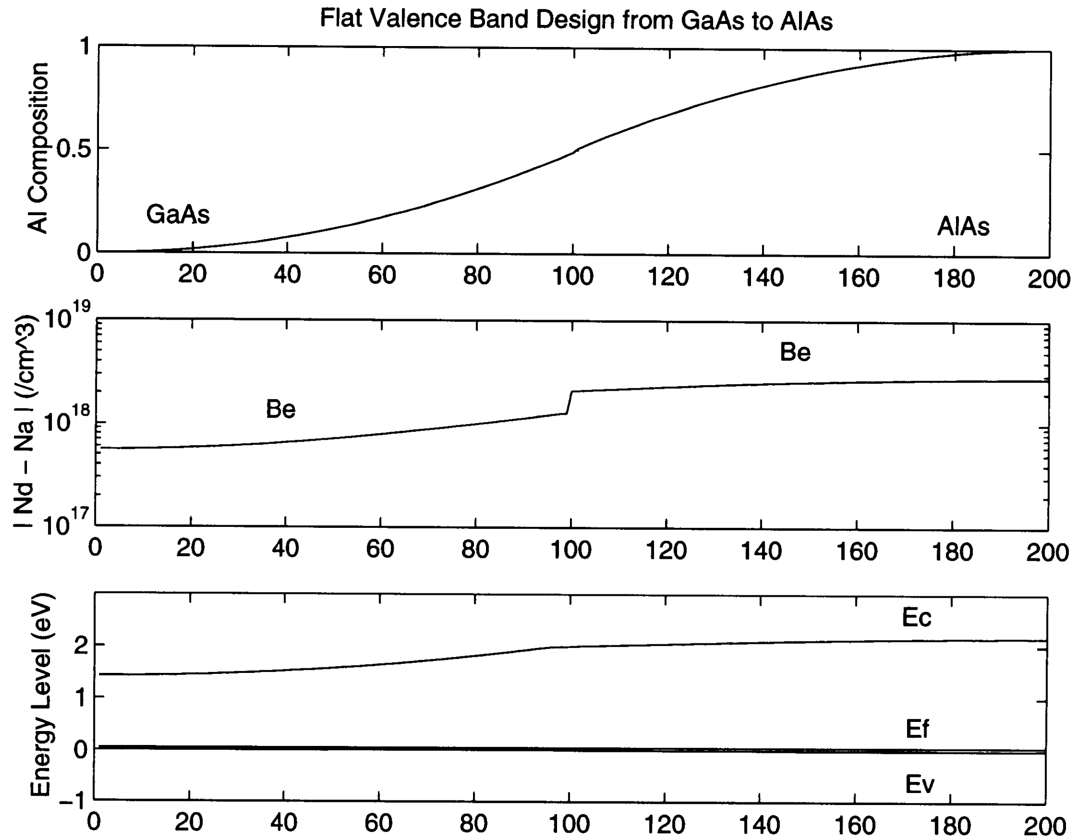

Figure 2.14: Sample flat valence design for GaAs/AlAs heterojuctions. The composition grading and the doping modulation are given for the flat valence band.

2.3.4 Improved Design and Response of a UTC-PD

To apply the principles outlined in the above subsection, we performed the calculation for InGaAs/InAlGaAs materials system. The flat valence band can be achieved by specific doping profile across 100 monolayers of deposition, as displayed in Figure 2.15. For this particular case, InAlAs replaces InP as the collection layer. Even though electron mobility in InAlAs is slower than that in InP and the electron transport is made more complicated by the inter valley transition effect in the conduction band of InAlAs, the flat band design is still very useful to optimize the performance

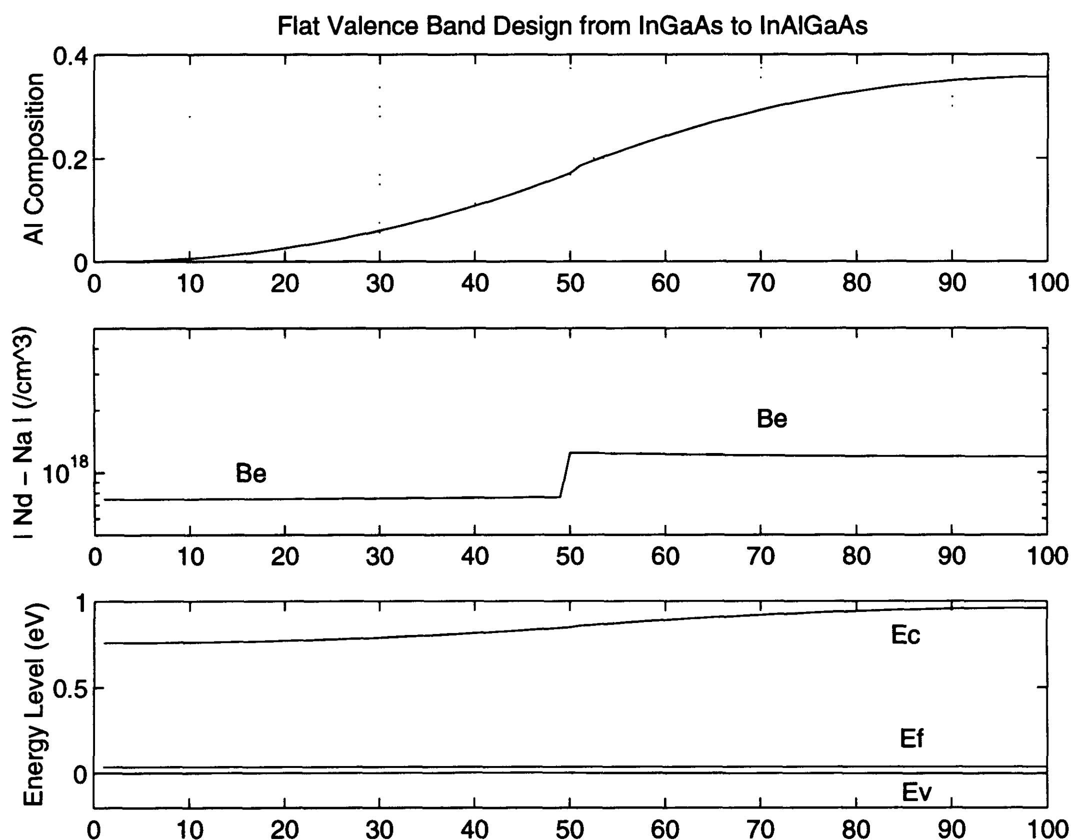

Figure 2.15: Sample flat valence design for InAlGaAs/InGaAs heterojuctions. The composition grading and the doping modulation are given for the flat valence band.

of InAlAs/InGaAs photodetectors. A similar design can be done for n-type heterojunctions as well as different material systems such as InGaAsP/InGaAs for improved frequency response.

If there is no conduction band discontinuity at the absorption/collection interface, the electron transport at that interface will no longer be governed by thermionic emission process. The boundary condition for Equation 2.28 thus becomes $n(W_A) = 0$. The solution is still in the form given by Equation 2.29 and 2.30, except the constants C_1, C_2 are given by:

$$C_1 = \frac{1}{\Delta}\begin{vmatrix} \mu_n E_0 G\tau_0 & D_n m_2 - \mu_n E_0 \\ -G\tau_0 & e^{m_2 W_A} \end{vmatrix} \tag{2.39}$$

$$C_2 = \frac{1}{\Delta}\begin{vmatrix} D_n m_1 - \mu_n E_0 & \mu_n E_0 G\tau_0 \\ e^{m_1 W_A} & G\tau_0 \end{vmatrix} \tag{2.40}$$

$$\Delta = \begin{vmatrix} D_n m_1 - \mu_n E_0 & D_n m_2 - \mu_n E_0 \\ e^{m_1 W_A} & e^{m_2 W_A} \end{vmatrix} \tag{2.41}$$

Figure 2.16 displays the electron distribution in the absorption layer of the flatband UTCPDs. We can see that the overall electron density is reduced from the level displayed in Figure 2.10, which means faster sweeping out of the photon-generated electrons.

The effect of the faster depletion of the photon-generated carriers is shown in the elevated frequency response. Figure 2.17 gives the comparison of the further improvement of the operating speed of the flatband UTCPD over the normal UTCPD and a conventional p-i-n photodiode.

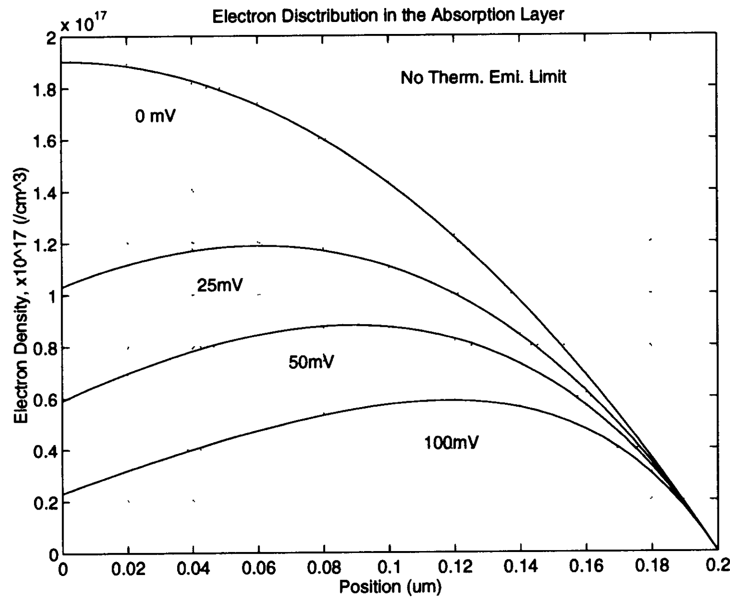

Figure 2.16: Electron distribution in the absorption layer of a flatband UTC-PD. The flat conduction band edge at the absorption/collection interface makes the electron transport across the interface no longer limited by thermionic emission process. This results lower electron density in the absorption layer and faster response.

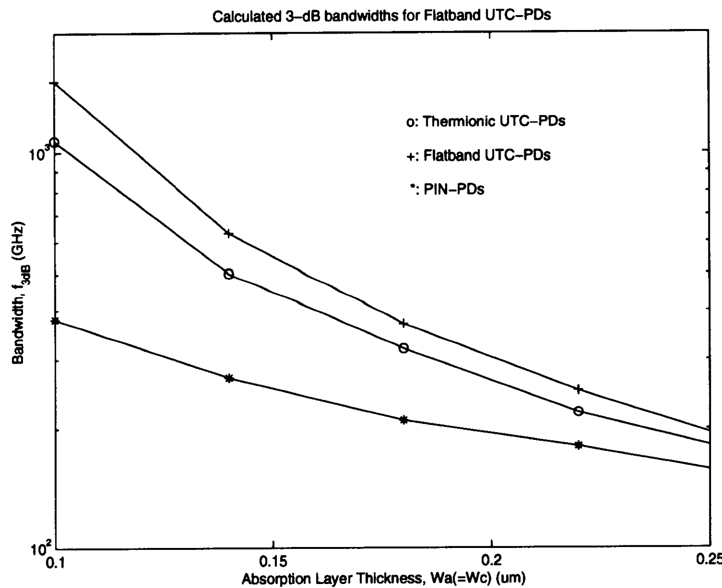

Figure 2.17: The improved 3dB bandwidth for a flatband UTC-PD. The bandwidth for a similar conventional p-i-n photodiode and a similar heterojunction UTC-PD with band discontinuity are also shown for comparison purposes.

2.4 Summary

The p-i-n photodetector has been widely deployed in many OEICs. The etched mesa structures for p-i-n photodiodes generally result in low dark current. High responsivity is obtained for a p-i-n detector with a sufficiently thick absorption layer.

For the 1.55μm p-i-n InGaAs photodiodes, a responsivity higher than 0.6A/W is obtained for an absorption layer thickness of more than 1 micron. For any given size of a p-i-n photodetector, there is an optimal absorption thickness determined by both RC constant of the device junction and the transit time of the photo-generated carriers. Light illumination from the p-side of the photodiode is preferred for its high speed operation since the slower moving holes travels shorter distance.

MSM photodetectors are attractive due to their ultra-low capacitance, their planar structures, and their processing compatibility with MESFET electronics. The interdigited electrodes can be made in the same processing step as the MESFET gate metal.

For the lateral detector size of 75 microns, the capacitance of a MSM detector with 2 microns of finger spacing is six times lower than that of a p-i-n photodiode with 2 microns of absorption layer thickness. Faster response than that of a p-i-n detector results from the much lower capacitance for the same detector size. This makes it possible to make larger area detectors with sustained fast response.

However, the electrodes are often opaque so that the external quantum efficiency is reduced for a MSM photodiode. To achieve more than 0.5 A/W responsivity, a finger spacing of more than 1.5 microns is required. The electrode shadowing effect can be leveraged by using transparent electrodes and/or ultra-thin fingers by submicron lithography.

For 1.55μm light detection, undoped InGaAs has a low Schottky barrier height ($\sim 0.2V$), which tends to induce larger dark current for the MSM detector. InAlAs

cap layer can be used to enhance the Schottky barrier height.

Uni-traveling Carrier Photodiodes can support larger photocurrent than the other two detector structures. This could ultimately benefit the integration of ultra-fast optical receiver front-end with improved system performance by eliminating the amplifier noise bottle neck for high bit-rate communications.

The faster response in a UTC-PD is achieved by using only electrons as traveling photocarriers. The absorption layer is thus no longer an intrinsic but a p-type InGaAs layer. Photo-generated holes are immersed in the majority carrier current in the absorption layer. Only electrons diffuse to the collection layer and form the photocurrent. Since electrons are diffusing through the absorption layer, the thickness of the absorption layer and in turn the external quantum efficiency is limited. This also requires a quasi-field built in the absorption layer to help electrons sweep out. To exceed the bandwidth of the p-i-n photodetectors, an absorption layer thickness of less than 2000Å and a finite quasi-field are required for a UTC-PD. However, with sufficient AR coating, the external quantum efficiency can still be as high as 0.5 A/W.

By replacing the depletion layer with wider bandgap material such as InP, the device dark current can be reduced for a UTC-PD from that in a p-i-n photodiode. This is evident by comparison with the intrinsic carrier density in InGaAs ($n_i = 3.1\times10^{11}cm^{-3}$) and InP ($n_i = 1.2\times10^{8}cm^{-3}$). Lower intrinsic carrier density reduces dark current by both the carrier diffusion which is proportional to n_i^2 and the thermal generation which is proportional to n_i.

For the optimal performance of a UTC-PD, both the graded absorption layer and the flat-band hetero-interface are required. More elaborated crystal growth is thus involved. To achieve the advantageous quasi-field in the absorption region, dopant grading and/or composition grading are needed. For the flat-band hetero-interface, compositional grading is needed. These band-gap engineering could further improve

the operation speed of the UTC-PD from the demonstrated 150GHz to more than 300GHz.

In this thesis research, the p-i-n structure is selected as the candidate for the integration. The decision was made based on the simplicity of the fabrication and the higher responsivity. These eventually help the evaluation of the material growth of InGaAs on GaAs. On the other hand, reliable fabrication of MSM photodiodes on campus requires elaborated development irrelevant to many material issues to be addressed. It is believed that optimized materials benchmarked by the best performance in a p-i-n photodiode will result in the optimal performance for MSM detectors. Moreover, the optimal growth sequence developed for p-i-n structures can be simply applied for the growth of 1.55μm UTC-PD structures.[1]

[1]The concept of UTC-PD and its optimal design were developed after the thesis research went well down the road and the implementation of a flat-band UTC-PD requires significant amount of MBE growth in addition.

Chapter 3

1.55μm Photodetectors Grown on GaAs

The integration of 1.55μm detectors on GaAs through direct growth requires the heteroepitaxy of $In_{0.53}Ga_{0.47}As$ on GaAs. The incompatibility between these two material systems mainly due to the difference in lattice constants poses problems in achieving good quality heterostructures. The feasibility of OEIC integration of InP-based materials such as InGaAs with GaAs substrates through direct epitaxy techniques depends on the quality of the film, as well as ultimately on the performance of the devices.

This chapter outlines the material issues involved in such a heteroepitaxy technique (Section 3.1), along with the development of the growth structure and its characterization (Section 3.2), and the final detector performance (Section 3.3). It is concluded in Section 3.4 that even though workable devices can be produced through direct epitaxial growth on GaAs, the performance of the resulting devices are not yet suitable for high performance receiver integration.

3.1 Lattice Mismatched Crystal Growth

In the most reliable semiconductor heterostructure devices, the semiconductor layers have different bandgaps, but very closely matched lattice constants, such as in AlGaAs/GaAs and InGaAsP/InP systems. This lattice-matching provides immunity from the creation of misfit dislocations which commonly form at mismatched interfaces. However, only very limited choices of band offsets, and electrical/optical properties exist for the lattice-matched systems, which in turn limit the design options for both discrete and integrated electrical and optical devices. If high quality, low defect density growth can be extended to lattice-mismatched systems, a much wider selection of band gaps and band offsets would be available, leading to novel device and integration structures [65, 66, 67].

Since InGaAsP and InGaAs can both emit and absorb in the 1.3 to 1.55μm wavelength region, which corresponds to the low dispersion and low loss regions of conventional optical fibers, InP-based optoelectronic devices have been a natural choice for fiber applications. This wavelength simply can not be reached by the lattice-matched wider bandgap AlGaAs/GaAs/GaInP material systems. For a long time, people generally have believed that InP is the only suitable material system for telecommunication applications.

Unfortunately, even though InP-based materials often present superior electronic properties [1], InP-based electronics is very immature and lagging in development.

On the other hand, GaAs-based electronics today offer much more advanced high speed IC technology in both analog and digital domains. Vitesse, one of the leading companies in GaAs digital IC manufacturing, has achieved very large scale GaAs Ics, and made it very similar to silicon VLSI. The company now is capable of demonstrat-

[1] InP has lower electron mass, higher mobility, higher peak electron velocity, higher thermal conductivity, larger electric breakdown field than GaAs.

ing integration levels which approach the state of the art in silicon. Therefore, the ideal electronics for high speed 1.55 μm data communication applications are GaAs-based due to the inability of silicon BiCMOS to accommodate III-V optoelectronics with sufficiently low defect density.

This will require combining InGaAs, which presents the best optical performance for 1.55μm applications, together with GaAs, which currently offers the best available high speed electronics. The technological constraint set upon this material system is the 4% lattice mismatch between them. How to overcome this large lattice mismatch and obtain high optical quality material becomes a major challenge.

3.1.1 Dislocations Associated with Mismatched Growth

For lattice mismatched heteroepitaxy, the unit cells or so called lattice constants of the heterogeneous materials are not the same size in equilibrium. During the epitaxy process, strain develops due to such structural differences. When the thickness of the film is small, or more precisely, is smaller than a critical thickness for a given mismatched system, pseudomorphic growth is possible, where the elastic lattice deformation in the epi-film accommodates the induced strain (Figure 3.1(a)). However, when the film thickness surpass the critical thickness, the increasing strain energy stored in the film exceeds the energy of dislocation formation and misfit dislocations are generated at the film-substrate interface to yield the minimum overall energy. Thus beyond the critical thickness, the lattice mismatch is accommodated by both elastic strain and misfit dislocations(Figure 3.1(b)).

If all of the misfit dislocations are only at the film-substrate interface(Figure 3.2(a)), and when only the active layer quality is concerned, dislocations far away from the active layer are seemingly harmless to many applications. However, dislocations can not terminate abruptly in the film; they need to either propagate to the edge or the

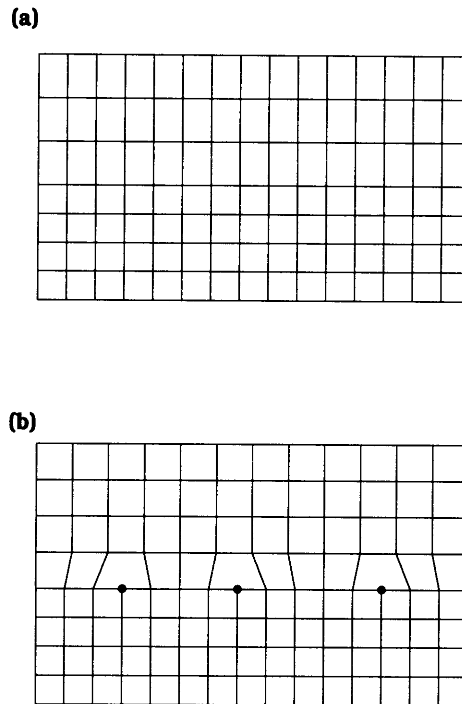

Figure 3.1: Strained epitaxial layer on a substrate: (a)Pseudomorphic growth, i.e., entirely strained epi-layer; (b) a partially relaxed layer where misfit dislocation forms (marked as dot in the plot).

surface of the film, or to be eliminated by other dislocations with opposite Burgers vectors. Unfortunately it is found often to be the case that the dislocations climb up to terminate at the surface of the film, and form threading dislocations crossing the device layer(Figure 3.2(b)). For the mismatch as large as 4% between $In_{0.53}Ga_{0.47}As$ and GaAs, film growth beyond the critical thickness often results in a high threading dislocation density and poor material quality. How to reduce the density of these dislocations in the films becomes one of the most important issues to face.

The origin of the afore-mentioned dislocations are mainly from four categories of sources [67]: (1) Substrate dislocations which thread into the epilayer and, after the growth exceeds the critical thickness, can glide laterally and form misfit dislocation

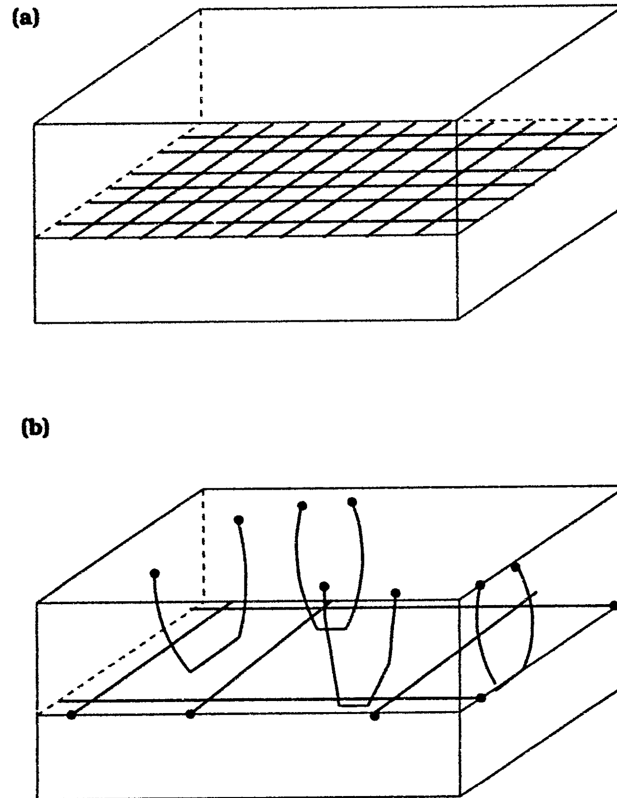

Figure 3.2: Misfit and threading dislocations in partially relaxed epilayer: (a)a typical misfit dislocation network at the interface; (b)Mandatory termination of the misfit dislocations at the surface generates threading dislocations across the device layer.

segments. (2)Homogeneous half loop nucleation creates a radial shaped dislocation which can expand downwards to the interface and form a misfit segment with two threads. However, the activation energy for this nucleation is high for low misfit systems. (3) Heterogeneous half loop nucleation results from the substrate surface imperfections such as particulates, impurities, and possible mechanical damages, which generate stress perturbation and lower the activation energy for half-loop nucleations. (4) The dislocation interactions can either increase the threading dislocation density by repulsive interactions or annihilate threading dislocations by attractions between

two dislocations.

3.1.2 Dislocation Reduction Techniques

Dislocations are detrimental for optoelectronic devices. Dislocation cores assist the fast diffusion of dopants. When they run across the electrical junction, they often increase leakage current and even act as shorts when the dislocation density is high. Besides, dislocations scatter carriers and reduce their mobilities and thus degrade the frequency response of the optical devices. For light emitters, the presence of a high density of dislocations often induces dark-line defects (DLDs) leading to the failure of the devices [68, 69, 70].

Various techniques are introduced to reduce the defect density in the device layers. One technique is to grow thick buffer layers and anneal after growth [71]. The post growth annealing increases the dislocation interaction so that dislocation annihilation dominates. However, the annealing temperature is usually high and not allowable for EoE integration as we shall describe in Section 4.2.

Another popular way to reduce threading dislocation density is to use the strained-layer superlattice (SLS) [65]. Alternating layers of semiconductor materials with different lattice parameters are deposited on a high dislocation density substrate material or previously grown layer. The goal of SLS is to create strain to force threading segments to the edge of the wafer, thus acting as a dislocation filter. However, for the growth on bulk substrates, the dislocations only move a small distance and rarely reach the edge of the wafer. Thus the SLS mechanism only wiggles the dislocations back and forth to increase their chances for interactions and mutual annihilations. The achievable reduction of the threading dislocation density can only be a factor of two or three.[2]

[2]Professor Fitzgerald, private communications.

Recently, a reduction in substrate growth area before the deposition of the mismatched semiconductor has been shown to drastically reduce dislocation density [72, 73, 74]. This works best when the strain in the epilayer is low and both homogeneous dislocation nucleation and nucleation on the mesa sidewalls are unlikely to occur. For a smaller area, chances of the existence of heterogeneous sources are smaller and both misfit and threading dislocations can be reduced. Moreover, each misfit dislocation now travels through a much shorter distance to terminate at the edge of the mesa rather than at the epilayer surface. Thus the probability of generating threading dislocations could be reduced.

However, the EoE process requires growth in small wells rather than on small area mesas. It is unclear whether the sidewall of the well serves as a dislocation annihilation center or dislocation nucleation center. Careful study needs to be done to evaluate how this reduction scheme works with the Epitaxy-on-Electronics.

Finally, a widely adopted technique is the relaxed buffer growth [67, 75]. Slow compositional grading prevents the system from being in a high strain state. Thus, dislocation nucleation can be minimized. Higher growth temperature is preferred to promote dislocation gliding to help efficient strain relaxation. The threading dislocation also has a higher probability of being involved in an annihilation interaction due to their increased moving distance. Low strain also reduces the chance for dislocation pinning.

In the epitaxy-on-electronics integration scheme, the depth of the growth well is about 6.5 μm which sets a lower limit of the grading rate. Compositional grading lower than 10% In/μm seems impractical. The on-chip electronics set the upper limit of the growth temperature at 470°C which does not promote favorable dislocation gliding. However, even though the epitaxy-on-electronics technique sets restricted process window, it is still promising and worth attempting.

3.2 Development of the Relaxed Buffer Structure

As discussed in the last section, for E-o-E integration, the most practical means to reduce the dislocation density is to utilize the relaxed buffer structures. The development of the optimal relaxed buffer by MBE given the restricted growth temperature (less than 470°C) and desired thickness (6.5μm) was investigated first. The material parameters were then measured by various techniques. The quality of the materials, and of the relaxed buffer underneath, was assesssed.

3.2.1 Material Characterization

The strain, lattice tilt, and the composition of the heterostructures were mainly determined using triple-crystal high resolution X-ray diffractometry. The setup of the Bede triple axis diffraction (TAD) system used in this work is sketched in Figure 3.3.

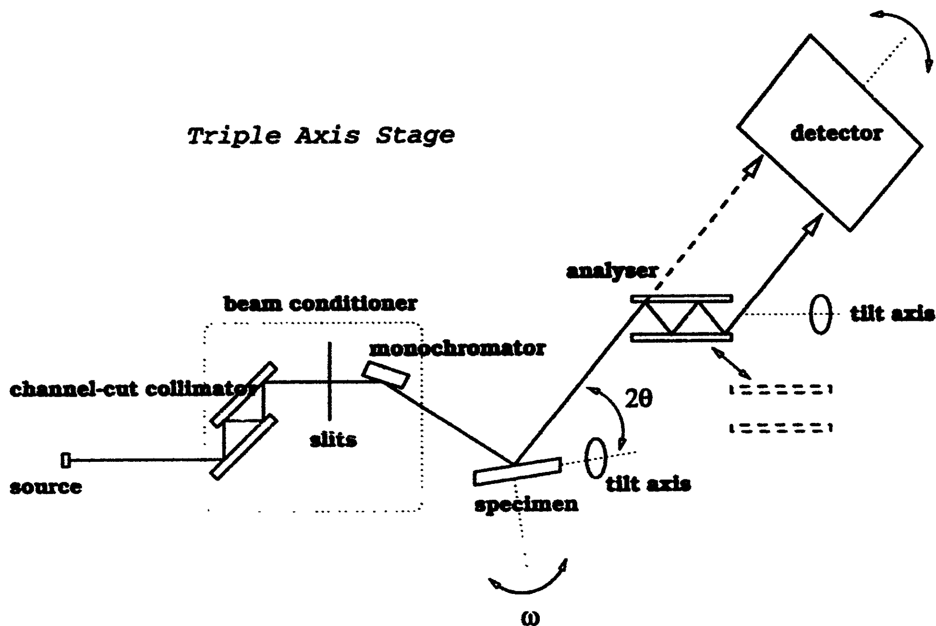

Figure 3.3: Schematic of the Bede triple crystal X-ray diffraction set-up.

The first crystal is the beam conditioner, which consists of a channel-cut collimator and a monochromator crystal, both typically made out of silicon. The X-ray beam generated from the source passes through the conditioner with a certain amount of axial divergence. The specimen is the second crystal in the system. The first two crystals (beam conditioner and the specimen) constitute a double axis system. The detector integrates the scattered x-ray signal from the specimen with all angles allowed by its aperture. The first two crystals alone are unable to distinguish very small angular variations in the diffracted beam due to small composition, strain and tilt variations. In the Bede triple axis diffraction (TAD) system, the third crystal, called the analyzer crystal, is introduced before the detector. The resolution is thus enhanced since the third crystal acts as an additional channel-cut collimator. Such an enhancement is displayed in Figure 3.4, where the triple crystal x-ray rocking curve resolves structures in the epilayer peak, whereas the double crystal X-ray rocking curve does not.

The biggest functional advantage of a TAD system is the ability to do reciprocal space maps (RSMs), which provide information about the mosaic spread, epilayer tilt, parallel and perpendicular lattice constants, and hence strain and the degree of relaxation. Assuming the validity of Vegard's law, the composition of the film is also determined [76]. One example of the RSM for a p-i-n structure developed is shown in Figures 3.5 and 3.6. The q_{001} axis is proportional to the vertical lattice constants while the q_{110} is proportional to the in-plane lattice constants. There is little difference in q_{001} direction between the substrate and the epi-layer, which indicates that the epitaxial layer is not tilted in this sample. The accurate determination of the material composition requires knowledge on the possible tilt present in the epi-film since tilt results in an underestimated perpendicular lattice constant and overestimated in-plane lattice constant. Moreover, if there is a large amount of tilt in the

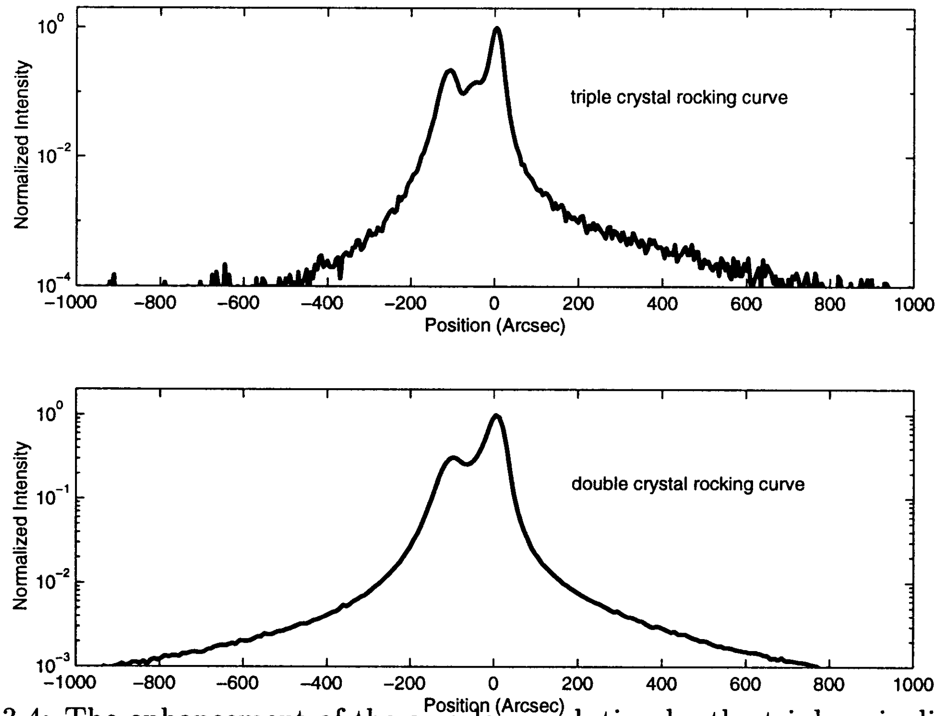

Figure 3.4: The enhancement of the angular resolution by the triple axis diffractometry. The two epilayer peaks are on the left. Notice three peaks have been resolved in the triple axis diffraction while only two peaks in double crystal diffraction.

epi-layer, the top surface is no longer the symmetric crystallography plane, hence device performance may be modified due to different surface density of states. From the 224 glancing exit map, all the information about the composition, and the degree of relaxation is resolved. For the particular sample displayed in Figure 3.6, the degree of relaxation was over 97% and the composition is $In_{0.52}Ga_{0.48}As$. However, reciprocal space mapping is a time-consuming experiment and thus quite expensive for many cases. Provided the degree of relaxation is known, one $\theta/2\theta$ X-ray rocking curve from the symmetrical planes plus one from the asymmetric planes can provide enough information about the material composition. Figure 3.7 shows the symmetrical rocking curve taken from 004 planes and asymmetric rocking curve taken from 224 planes for both glancing exit and glancing incidence conditions. Assuming a 98% relaxation

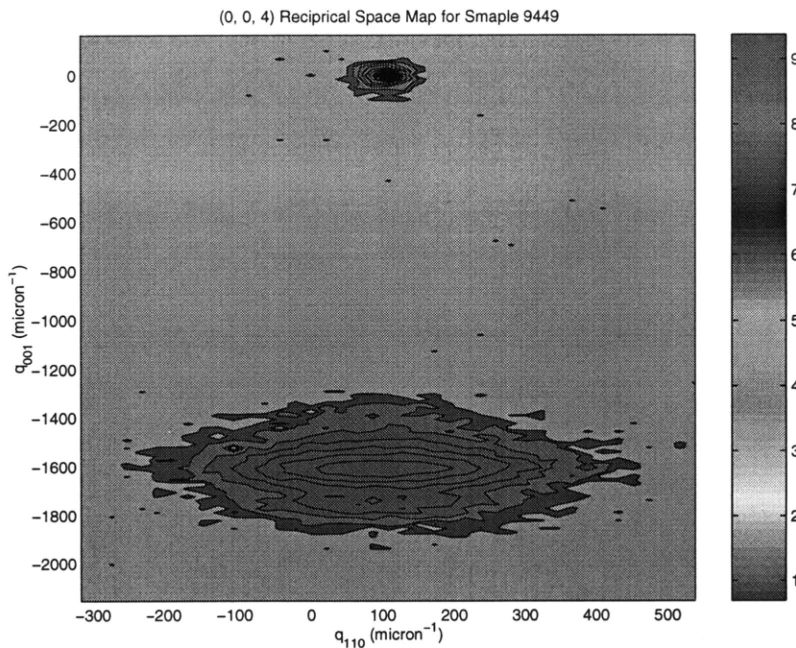

Figure 3.5: Reciprocal Space Mapping for Sample 9449 from 004 planes. The color code bar on the right hand side is the diffraction intensity in logarithm scale.

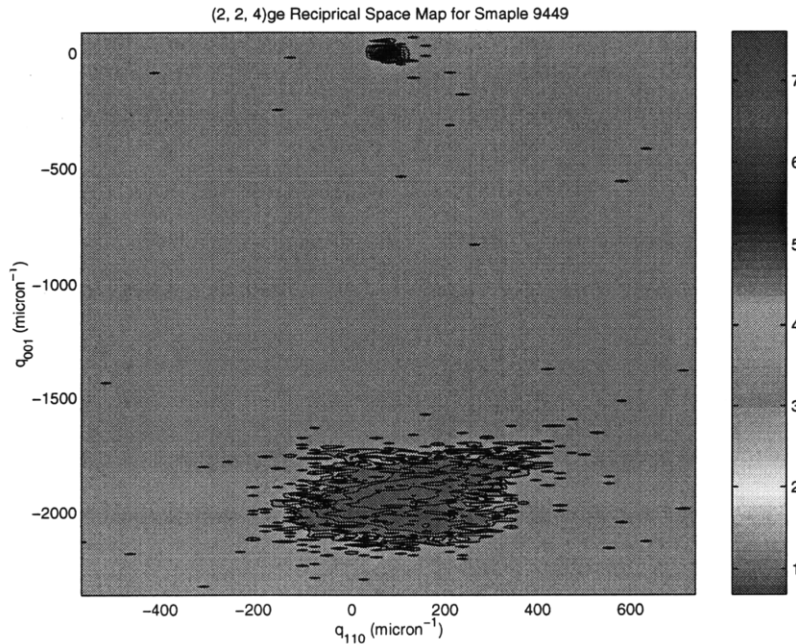

Figure 3.6: 224 glancing exit Reciprocal space map for Sample 9449. The color code bar on the right hand side is the diffraction intensity in logarithm scale.

which is usual in the MBE growth involved in this thesis work, the derived composition is $In_{0.55}Ga_{45}As$. However, a few rocking curves like these do not readily reveal the information about lattice tilt. For samples with critical importance, a thorough reciprocal space mapping is desired to reveal more complete information about the device structure.

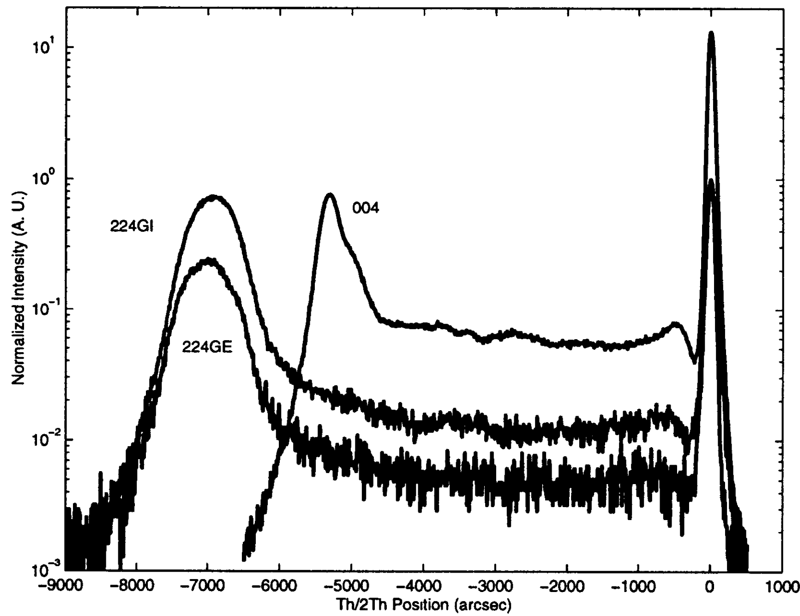

Figure 3.7: Multiple X-ray rocking curves for Sample 9614.

Once the material composition, thickness, and strain relaxation are satisfactory, cathodluminescence (CL) is used to evaluate the material quality. By injecting an electron beam with high enough energy into the material, electron-hole pairs are generated and recombine radiatively to produce band-gap radiation. The relative amount of radiative recombination is lower in the vicinity of a defect; therefore, the image of defects can be seen in the plot of luminescence as a function of electron-beam position [66]. By careful selection of the CL operating parameters such as the magnification, electron acceleration voltage, and electron current, the quality of the different relaxed buffers underneath the p-i-n structure with identical design can be

compared by the CL intensity obtained.

Transmission electron microscopy (TEM) was also used to study bulk defects. Elaborate substrate thinning using repeated mechanical polishing and ion milling prepared the samples into electron transparent thin films[3]. The cross-sectional TEM gives information to determine the threading dislocation density. For samples with high defect density, the estimation of the dislocation density through cross-sectional TEM is quite reliable. In addition, the diffraction contrast can also be used to identify the dislocation characteristics [66].

Scanning electron microscopy (SEM) and optical microscopy in the differential interference contrast (Nomarski) mode are also used routinely to monitor the surface morphology of the relaxed buffer growth. Finally, diode electrical measurements reveal the leakage current to ultimately assess the material quality in terms of device performance.

3.2.2 Relaxed Buffer Development

Two candidates of relaxed buffer structures were considered. One is the linearly graded buffer. Another is the Graded Short-period Superlattice (GSSL) buffer. The linearly graded buffer involves linearly increasing the indium content in the buffer until the desired $In_{0.53}Ga_{0.47}As$ is reached. The GSSL is displayed in Figure 3.8. The super lattice structure was originally used in a 1.55μm MSM photodetector structure grown on GaAs substrate by Yao et al., showing good response (0.3A/W) for a 0.25μm feature size MSM detector [77].

Two structures shown in Figure 3.9 and 3.10 were grown by MBE. The epitaxial layers are very much relaxed, which is evident in the reciprocal space maps displayed

[3]Dr. Mayank Bulsara prepared the cross-sectional samples and did the TEM microscopy for this thesis research.

Al As	10A
InAlAs	90A
AlAs	30A
InAlAs	70A
Al As	50A
InAlAs	50A
Al As	70A
InAlAs	30A
Al As	90A
InAlAs	10A

Figure 3.8: Structure of graded short-period superlattice buffer.

in Figure 3.5 and 3.6. The derived composition is $In_{52}Ga_{48}As$ and the degree of relaxation is 97%.

The morphology of these two samples was very different. Sample 9446 has a lot of misfit dislocations with cross-hatching pattern on the surface. On the other hand, Sample 9449 looks optically flat and little surface roughness is shown. The fact that Sample 9449 is highly relaxed suggests there is high density of threading dislocations in this sample. These threads provide huge numbers of misfit segments to get the lattice relaxed.

The threading dislocation densities were calibrated by TEM. The cross-sectional TEM shown in Figures 3.12 and 3.11 suggest the threading dislocation density in Sample 9446 were in high $10^7/cm^2$ while the Sample 9449 in low $10^9/\mathrm{cm}^2$. The additional image contrast presented in the device layer of Sample 9446 (Figure 3.12) is likely due to the surface roughness induced phase separation.[4] It may be removed

[4]Mayank Bulsara, private communications.

p+ In0.53Ga0.47As 1000A
p+ In0.52Al0.48As 2500A
UID In0.52Al0.48As 500A
UID In0.53Ga0.47As 11000 A
UID In0.52Al0.48As 500A
GSSL 500A
n+ GaAs Buffer 417A
n+ GaAs Substrate

Figure 3.9: Sample 9449: p-i-n grown on GSSL buffer.

p+ In0.53Ga0.47As 1000A
p+ In0.52Al0.48As 2500A
UID In0.52Al0.48As 500A
UID In0.53Ga0.47As 11000 A
UID In0.52Al0.48As 500A
n+ In0.52Al0.46Ga0.02As
30000A
n+ In0.02Al0.51Ga0.47As
n+ GaAs Buffer 417A
n+ GaAs Substrate

Figure 3.10: Sample 9446: p-i-n grown on the linearly graded buffer. The grading rate was 17 %In/μm.

by decreasing the growth temperature during the buffer growth [78].

The higher defect density of Sample 9449 basically deteriorates its optoelectronic performance. The cathodluminescence measurement shows that Sample 9449 did not have any luminescence for the given electron injection current and acceleration voltage(Figure 3.13).

Both samples were fabricated into photodetectors and the responsivity of the linearly graded buffer structure is two times higher than that of the GSSL-buffered structure, while the dark current of the GSSL-buffered structure is more than five times higher than that of the linearly graded buffer (Figure 3.14). The detectors are 100μm × 200μm mesas with 100μm × 100μm openings.

3.3 Evaluation of 1.55μm Photodetectors on GaAs

Based on the observation described in the last section, the linearly-graded buffer structure was chosen to continue further development. One way to improve the crystal quality is to use slower grading rate to lower the strain present in the epilayer and reduce the possibilities of threading dislocation nucleations. Ten percent indium composition increase per micron of buffer growth was used to grow Sample 9614. Sample 9610 with the same active layer structure was grown on an InP substrate lattice matched to serve as a performance benchmark.

The resulted structure in 9614 is well relaxed as shown in the reciprocal space mapping in Figures 3.15 and 3.16. This time the composition is $In_{55}Ga_{45}As$ with degree of relaxation of 98.64%. There is little strain and tilt in the sample.

The cathodluminescence was also improved. However, the luminescence in the lattice matched 9610 was still much stronger than that of the structure grown on GaAs, which means there are still a significant amount of threading dislocations present in the linearly graded buffer structure, even with the reduced grading rate.

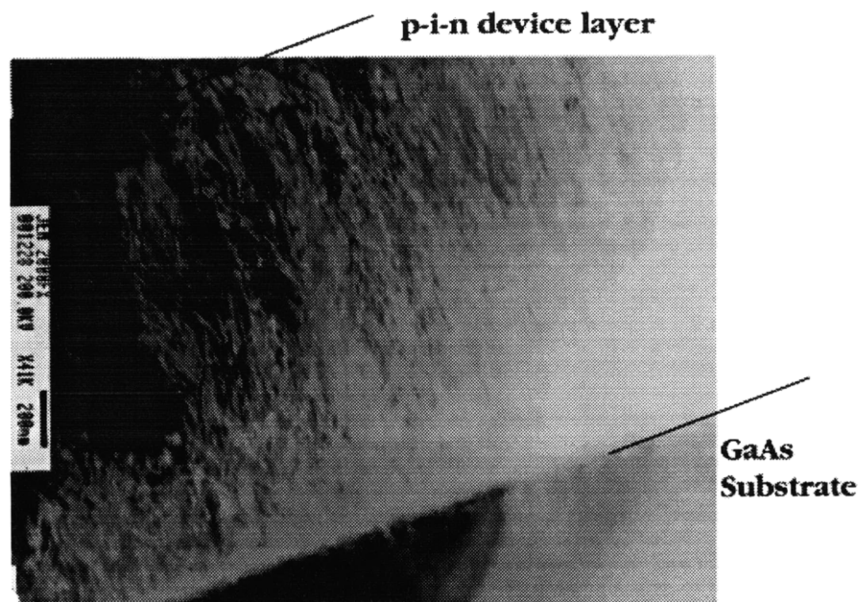

Figure 3.11: 41,000× cross sectional TEM image for Sample 9449 (GSSL buffer). The guide lines are parallel to the substrate surface (001). $\mathbf{g}$ = 220.

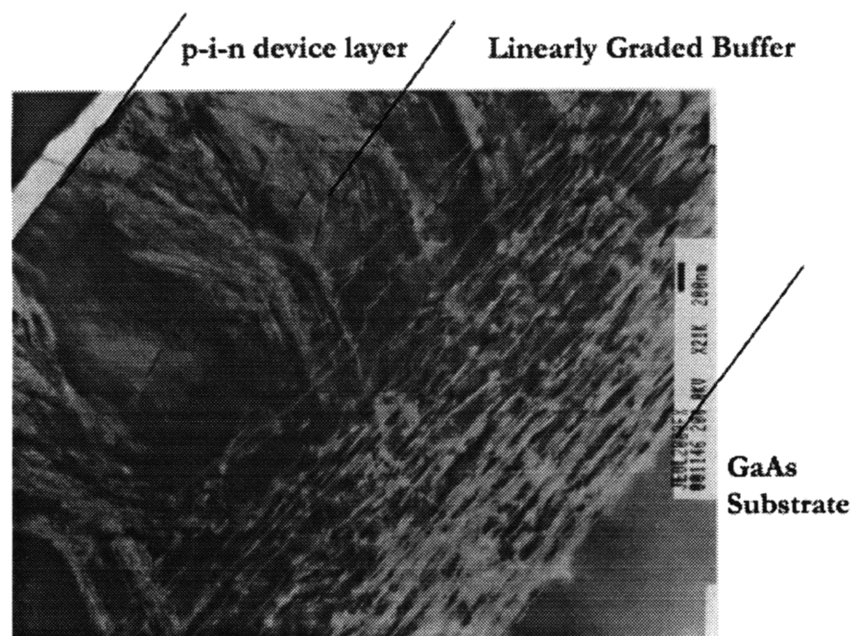

Figure 3.12: 21,000× cross sectional TEM image for Sample 9446 (linearly graded buffer). The guide lines are parallel to the substrate surface (001). $\mathbf{g}$ = 220.

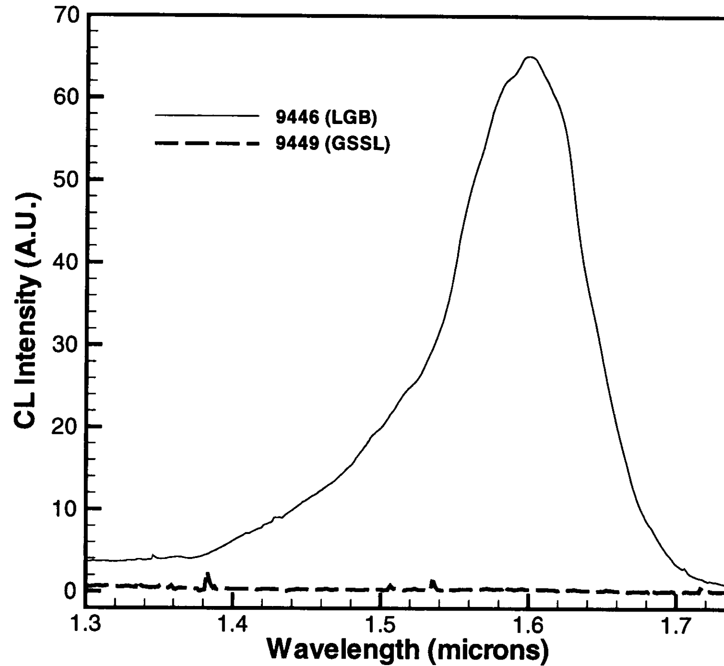

Figure 3.13: cathodluminescence for Sample 9446 and Sample 9449. The linearly graded buffer structure shows much better luminescence than the GSSL buffered structure does. This is consistent with the threading dislocation density present in these two samples.

3.3.1 Fabrication

Sample 9614 along with lattice-matched Sample 9610 were fabricated into photodetectors using the same techniques used for fabricating Sample 9446 and Sample 9449, described as the following:

First, Ti/Pt/Au Ohmic contact was made by e-beam evaporation and metal liftoff. The ring contact sizes range from 25μm square to 200μm square. Then the contact is rapid thermal annealed at 420°C for 30 second. The typical contact resistance were measured to be about $10^{-6}\Omega/\Box$ which is very good.

The detectors were then isolated from each other using a sulfuric acid based wet chemical etch. The depth of the mesa was well into the undoped InGaAs absorption

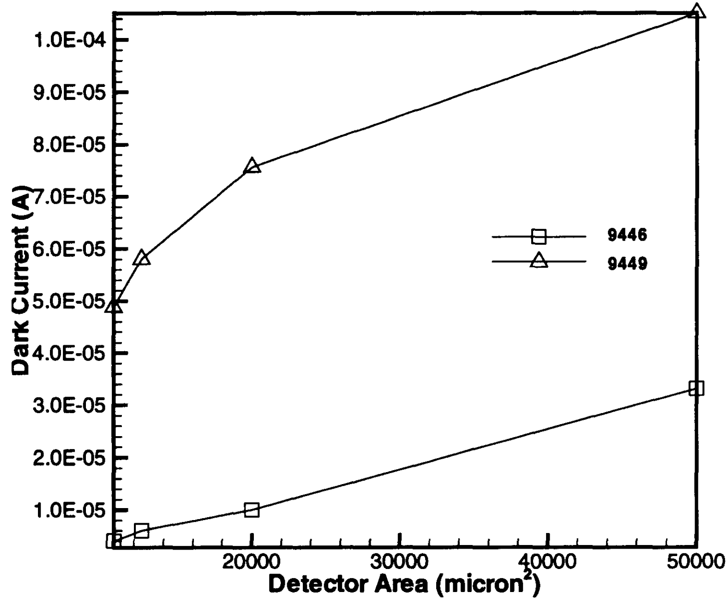

Figure 3.14: Dark current comparison for the linearly graded buffer and the GSSL buffer. The triangles (△) are for Sample 9449 with GSSL buffer; the squares (□) are for Sample 9446 with 17 %In/μm linearly graded buffer.

layer. Further etch does not improve the detector performance in terms of the leakage. The top InGaAs contact layer is also etched away to improve the responsivity.

The bottom contact was made by e-beam evaporation of AuGe on the back side of the wafer. The contact was rapid thermal annealed at 400°C for 30 seconds.

3.3.2 Detector Performance

The detector performance evaluation were made by mutual comparison among the linearly graded p-i-n structure previously grown at the faster indium grading rate (Sample 9446, 17% In/μm), the linearly graded structure grown at slower grading rate (Sample 9614, 10% In/μm), and the sample grown on n-type InP substrate lattice matched (Sample 9610).

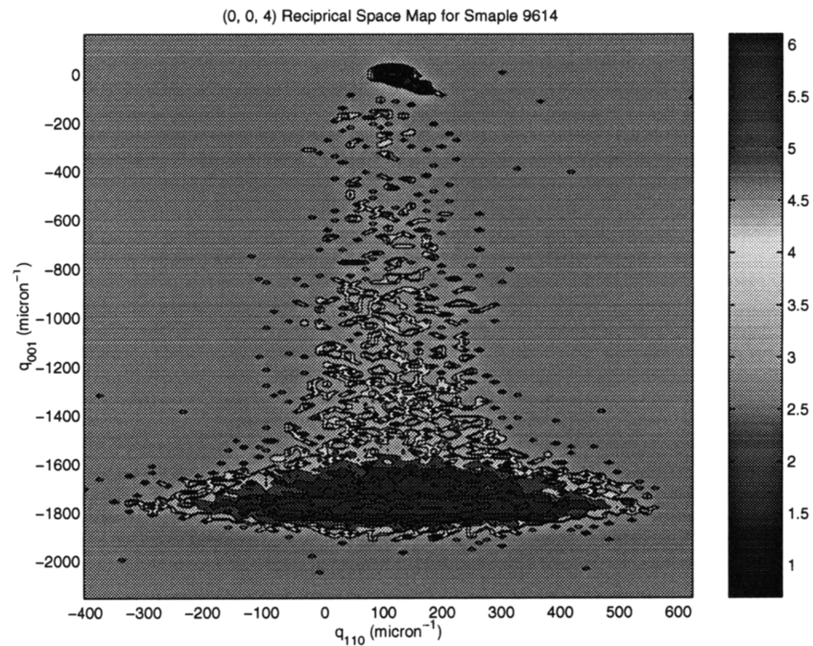

Figure 3.15: Reciprocal space mapping for Sample 9614 from 004 planes. Unlike the case presented in Figure 3.5, diffraction intensity appears between the substrate peak and the epi-layer peak due to the linearly graded buffer.

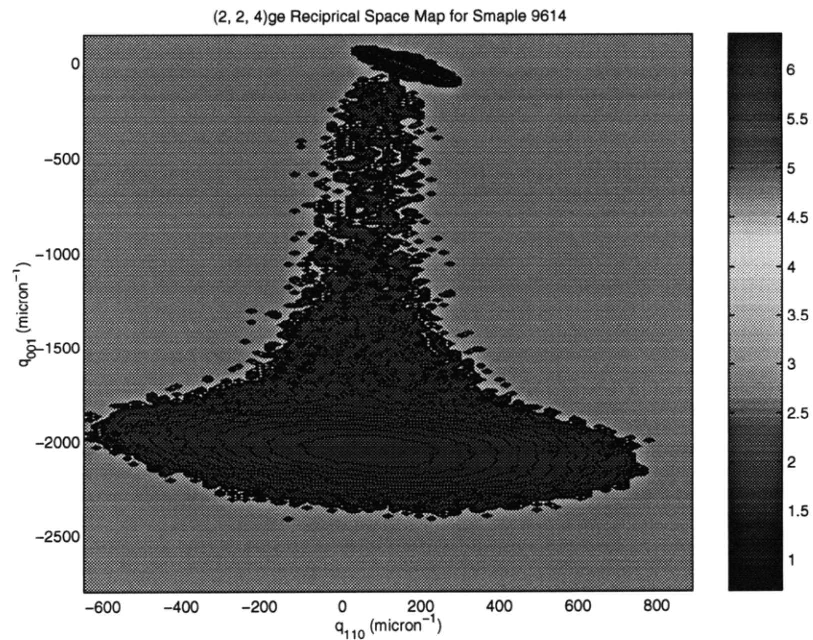

Figure 3.16: 224 glancing exit reciprocal space map for Sample 9614. Unlike the case presented in Figure 3.6, diffraction intensity appears between the substrate peak and the epi-layer peak due to the linearly graded buffer.

Sample 9614 is indeed improved from Sample 9446, which is evident in the dark current comparison in Figure 3.17.

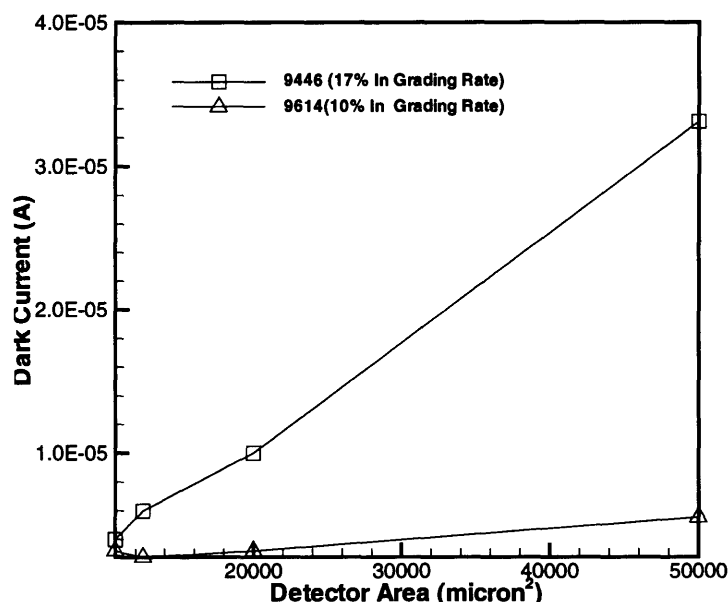

Figure 3.17: Dark current comparison for the linearly graded p-i-n photodetectors grown at different grading rates. The slower graded detectors clearly show smaller leakage currents which means less dislocation density in the junction region.

However, the performance difference between the lattice-matched structure on InP and the Sample 9614, Sample 9610, is still significant. The dark current in the lattice-matched sample is more than one order of magnitude smaller. Based on the measurement on more than 50 detectors on each wafer, the difference in term of the uniformity is also unveiled. The lattice matched structure shows superior performance in terms of much smaller leakage, more than 10 times higher responsivity, and much better uniformity. Figure 3.18 and Figure 3.19 show the comparison between 50 detectors grown on GaAs and 50 detectors grown on InP. Figure 3.21 and Figure 3.20 show the photoresponse under the same illumination conditions.

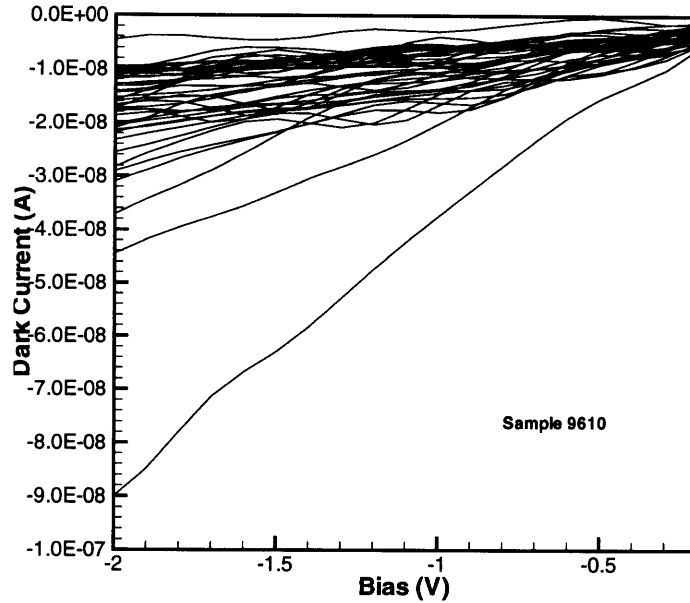

Figure 3.18: The dark current of 50 detectors grown on the lattice matche InP substrated.

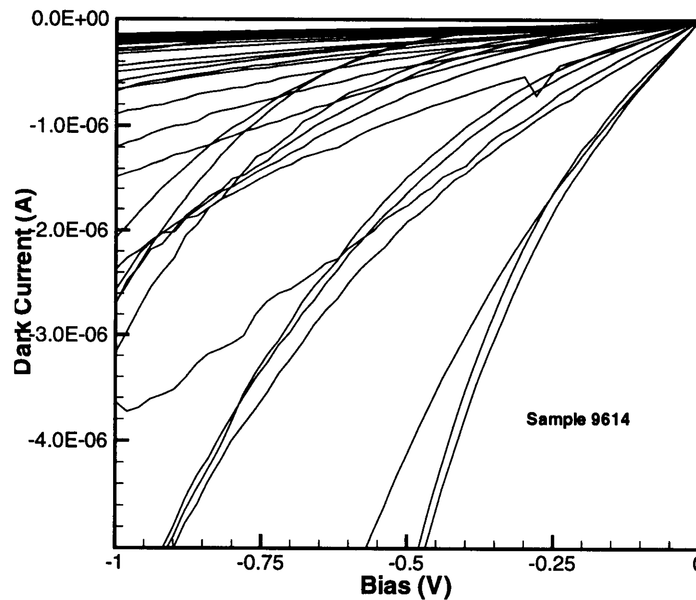

Figure 3.19: The dark current of 50 detectors grown on the lattice-mismatched GaAs substrate (Sample 9614). 10 %In/μm linearly graded buffer was used in the growth of this sample.

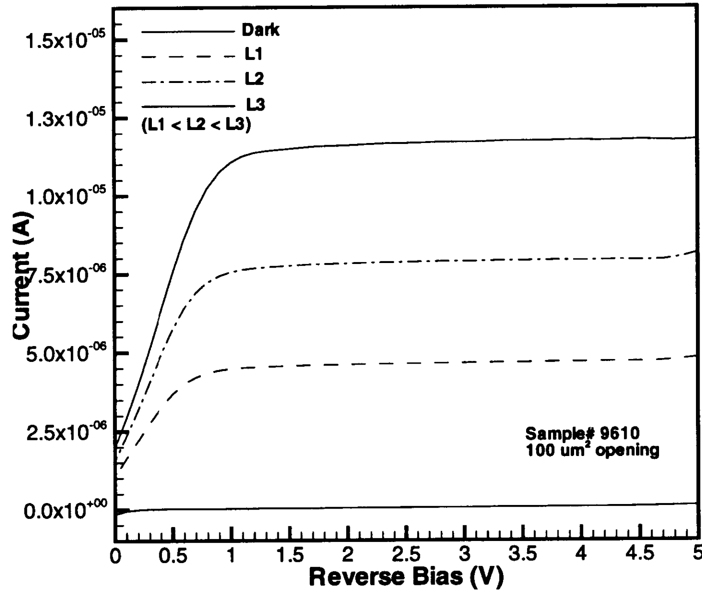

Figure 3.20: The photo currents for Sample 9610 grown on the lattice matched InP substrate.

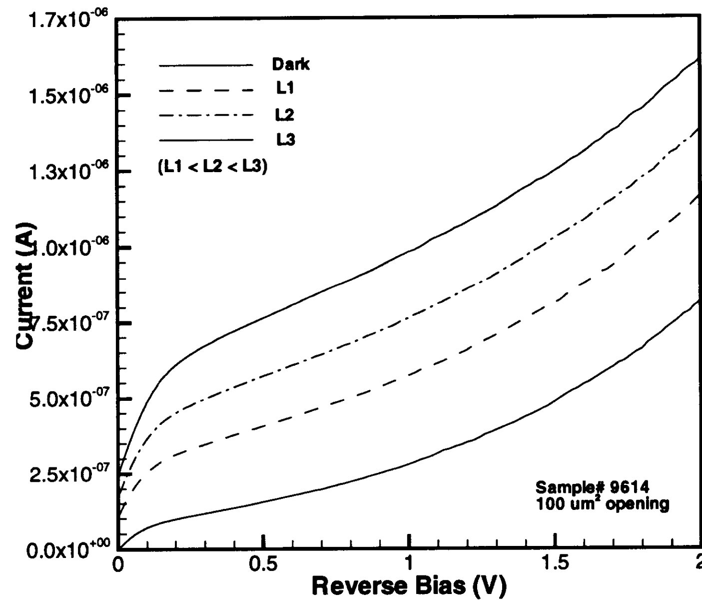

Figure 3.21: The photo currents for Sample 9614 grown on a lattice-mismatched GaAs substrate. 10 %In/μm linearly graded buffer was used in the growth of this sample.

3.4 Summary

Four kinds of p-i-n structures were grown by molecular beam epitaxy (MBE) and fabricated into photodetectors. These structures are: (1) Sample 9449: $In_{0.53}Ga_{0.47}As$ p-i-n grown on GaAs using 500 Å thin superlattice buffer as displayed in Figure 3.9; (2) Sample 9446: $In_{0.53}Ga_{0.47}As$ p-i-n grown on GaAs using linearly graded buffer with 17 %In/μm grading rate as displayed in Figure 3.10; (3) Sample 9614: $In_{0.53}Ga_{0.47}As$ p-i-n grown on GaAs using linearly graded buffer with 10 %In/μm grading rate; (4) Sample 9610: $In_{0.53}Ga_{0.47}As$ p-i-n grown on lattice matched InP substrate.

It is confirmed that the slower the grading rate is used, the better device performance it will achieve. Except the GSSL-buffered p-i-n detectors, all the other three samples exhibited a linear dependence of leakage current on the detector mesa area, which indicates the leakage currents therein were due to the bulk crystal quality rather than mesa sidewall surface. Assuming a zero grading rate for the p-i-n structure lattice matched to InP, the leakage current density from the latter three structures can be plotted as a function of the grading rate, as shown in Figure 3.22. If the grading rate is within the range from 0 %In/μm to 23 %In/μm, the leakage current density increases exponentially with the grading rate. It is usually assumed that the leakage current density is proportional to the threading dislocation density. Therefore, Figure 3.22 may suggest that the threading dislocation density increases exponentially with the grading rate. An empirical relationship between leakage current density and grading rate for $In_{0.53}Ga_{0.47}As$ grown on n-type GaAs using linearly graded buffer is given by:

$$\mathbf{J_D} = 0.15 \times \exp(0.96V) \times \exp(0.341x) \tag{3.1}$$

where J_D is the leakage current density in mA/cm^2, V is the reverse bias voltage in

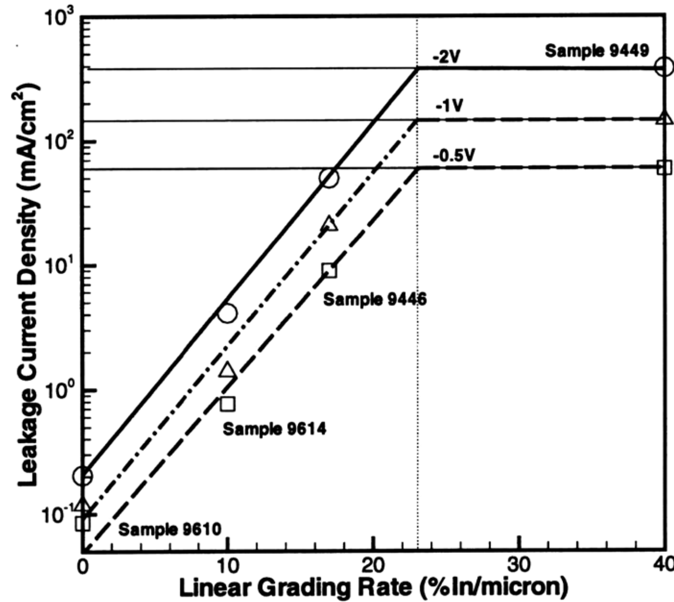

Figure 3.22: Leakage current density as a function of compositional grading rate. The leakage currents were measured at -2V, -1V, and -0.5V reverse biases. The horizontal lines are at the corresponding leakage levels of Sample 9449, which has a grading rate of 1040 %In/μm, way out of the displayed range.

volts, and x is the grading rate in %In/μm ($0 \leq x \leq 23$ %In/μm). Sample 9449 grown on the 500Å GSSL buffer can be approximated to be on a 500Å linearly graded buffer, with a very fast grading rate of 1040 %In/μm. If is found that the leakage current density is saturated at the level of Sample 9449. This suggests that it is only under certain saturation point (23 %In/μm in this case) that the grading rate be a useful growth parameter to control the threading dislocation density and thus the leakage current density. Above this saturation value, leakage current density is saturated and the material quality is no longer controllable by the grading rate. This saturation grading rate is independent of the reverse bias voltage used to measure the leakage currents, as shown in Figure 3.22.

The responsivity is also a strong function of the grading rate. The slower the

grading rate is, the higher the responsivity is. This was observed by the comparison between Sample 9446 and Sample 9449, as well as between Sample 9614 and Sample 9610. However, a plot like Figure 3.22 is not performed here for the responsivity at the present time since there were differences in both the absorption layer thickness and the material composition between Sample 9446/9449 and Sample 9614/9610. Also the relative responsivities were measured at different time under different illumination conditions. A complete study of the functional dependence of responsivity on the grading rate requires additional growth of multiple samples with the same active layers and the same fabrication and measurement sequences.

The integration of long wavelength photodetectors on GaAs substrates were sought by many groups in the past decades. Most of the early effort were made to integrate 1.3μm and 1.55μm MSM photodetectors on GaAs using MBE growth [77, 79, 80, 81]. For the only case of 1.55μm MSM photodiodes of 16 μm in diameter with 0.25μm finger width and spacing, the reported dark current was 1μA at -2 volts [77], which is comparable to that demonstrated in the present thesis research. Other cases involving 1.3μm wavelength using GaAs/InGaAs super-lattice grown on GaAs with the indium composition lower than 35% exhibited lower dark currents due to the strained structure and smaller degree of lattice mismatch [79, 80, 81].

Other efforts include the fabrication of planar, lateral InGaAs p-i-n structures on GaAs using $In_{0.53}Ga_{0.47}As$ [82]. The n-type InGaAs layers were grown by metalorganic vapor phase epitaxy. Selective area diffusion of Zn into the top layer of the n-type InGaAs turned the structure into lateral p-i-n photodiodes. The device performance for this planar p-i-n structure was very good. The exhibited dark current was as low as 30 $\sim$ 150 nA at 4V reverse bias for devices with 75μm-diameter opening. However, dark current larger than 1μA was observed when increased reverse bias depleted InP layer underneath where the dislocations at the hetero-interfaces started to affect the

I-V characteristics of the diode.[5]

The long-wavelength top-down p-i-n structures were also fabricated by several research groups [83, 84, 85] on GaAs, using either $In_{0.40}Ga_{0.60}As$ or $In_{0.53}Ga_{0.47}As$.

Ishimura et al. grew the p-i-n structure on 2° off-cut n^+-GaAs substrate by metalorganic chemical vapor deposition technique [84]. The dark current density reported there was quite low (0.38 mA/cm^2 at -10 V bias). However, the dark current was still three orders of magnitude higher than those detectors fabricated on InP substrates in their comparison study. It is believed that the off-cut substrate did reduce the threading dislocation density. InP cladding layer is also believed to be superior to InAlAs cladding layer.

InGaAs/InP p-i-n photodiodes were also fabricated on AlGaAs/GaAs waveguide films by Hsu et al. Using elaborated processing steps involving ultrahigh vacuum chemically assisted ion beam etching (CAIBE) and post etching polyimide surface passivation, Hsu brought the dark current down to 1.3 mA/cm^2. However, in their comparison study, InGaAs photodiodes grown on GaAs substrate with fairly thick InP buffer layer is still two orders of magnitude larger than that on InP.

In the present study, with the focused research goal on the material comparison among various buffer structures, neither mesa sidewall passivation nor AR-coating were utilized. InAlAs instead of InP was used as the cladding layer thus the inferior leakage characteristics was expected. Nevertheless, the self consistent result was obtained, the lower the grading rate is used in the buffer growth, the lower the leakage current density is. For a grading rate of 10 %In/μm, photodiodes exhibited leakage current density one order of magnitude higher than that on InP. To achieve less than 1 mA/cm^2 leakage current density, a grading rate slower than 5 %In/μm is needed, resulting in a buffer layer of more than 10 μm thick, according to Equation 3.22.

[5]The authors did not disclose the information about the spacing between p-contact and n-contact and whether the mesa was formed or not. Thus the dark current density is not clear.

While there is still room to improve the photodetectors grown on GaAs using even slower grading rate and higher growth temperature, the options for the Epitaxy-on-Electronics are rather limited. The finite depth of the growth well (6.5μm) sets the upper limit of 10 %In/μm to maintain planarization for post-growth processing. The preservation of electronics on the OEIC chips requires the growth temperature to be below 470°C which sets the upper limit of the growth temperature.

In conclusion, even though we can produce working detectors by direct growth of $In_{0.53}Ga_{0.47}As$ p-i-n structures on GaAs with the linearly graded buffer of 5.1μm and with a growth temperature below 470°C, clearly for the high performance high-speed receiver integration, direct epitaxial under limited conditions is not the best option. An alternative integration scheme is thus proposed and developed as described in Chapter 5.

Chapter 4

Integration via Epitaxy-on-Electronics

The original objective was to integrate the relaxed buffer 1.55μm photodetectors with GaAs transimpedance amplifiers using a novel optoelectronic integration technique, termed Epitaxy-on-Electronics (E-o-E), which has been demonstrated to be capable of producing good quality, high density OEICs for 850nm wavelength [86, 87, 88, 89]. E-o-E is intended to take advantage of the existing commercial VLSI GaAs MESFET electronics industry. To extend this technology to 1.55μm optoelectronic devices potentially could benefit the fiber optic communication OEICs from the considerable development of the very large scale integrated high speed electronics based on GaAs MESFETs, as discussed in Chapter 1.

This chapter presents the detailed description of the E-o-E integration technique and the work done towards integrating lattice mismatched InGaAs photodiodes onto GaAs OEIC chips. Section 4.1 introduces the E-o-E technology itself. The processing flow is displayed. The remaining sections address the design of the OEIC chip for the proposed integration (Section 4.2), chip preparation, reduced temperature MBE,

and finally the evaluation of the materials integrated on the chip (Section 4.3). The conclusion shows that the uniformity of material quality on the EoE chips is indeed an issue for growth with large amount of lattice mismatching.

4.1 Epitaxy on Electronics Integration Technology

The MIT Epitaxy-on-Electronics optoelectronic integration technology involves epitaxially growing optoelectronic device heterostructures directly on fully processed GaAs integrated circuits in special dielectric growth wells, and subsequently fabricating the heterostructures into optoelectronic devices monolithically integrated with the pre-existing electronic circuitry. In order to produce the OEICs via E-o-E technology, application-specific electronic circuits need to be designed with selected areas allocated for photonic devices. The designed circuits are then fabricated through a commercial foundry. After the chip fabrication, the areas reserved for photonic devices are cleaned and epitaxial growth of the optical devices is performed. Finally the optical device fabrication and interconnection with the electronics will generate the complete OEICs. This process is summarized in the flow chart depicted in Figure 4.1.

The epi-on-electronics technology offers an immediate path to complex, high performance OEICs and has already been demonstrated in a number of application-specific examples. The initial examples involve the integration of light emitting diodes and MSM photodetectors with neural network decision circuits and digital switches [86, 87, 88, 90]. Recently, this technique has been successfully extended to the monolithic integration of self electro-optic effect devices (SEEDs) with GaAs VLSI circuits [89]. Since the aluminum-based electrical interconnects degrade when exposed to temperatures in excess of 470°C, substantive effort is directed to develop the reduced temperature MBE. One important scheme towards the reduced growth temperature is the development of InGaAsP materials system integrated on GaAs chips. Thus,

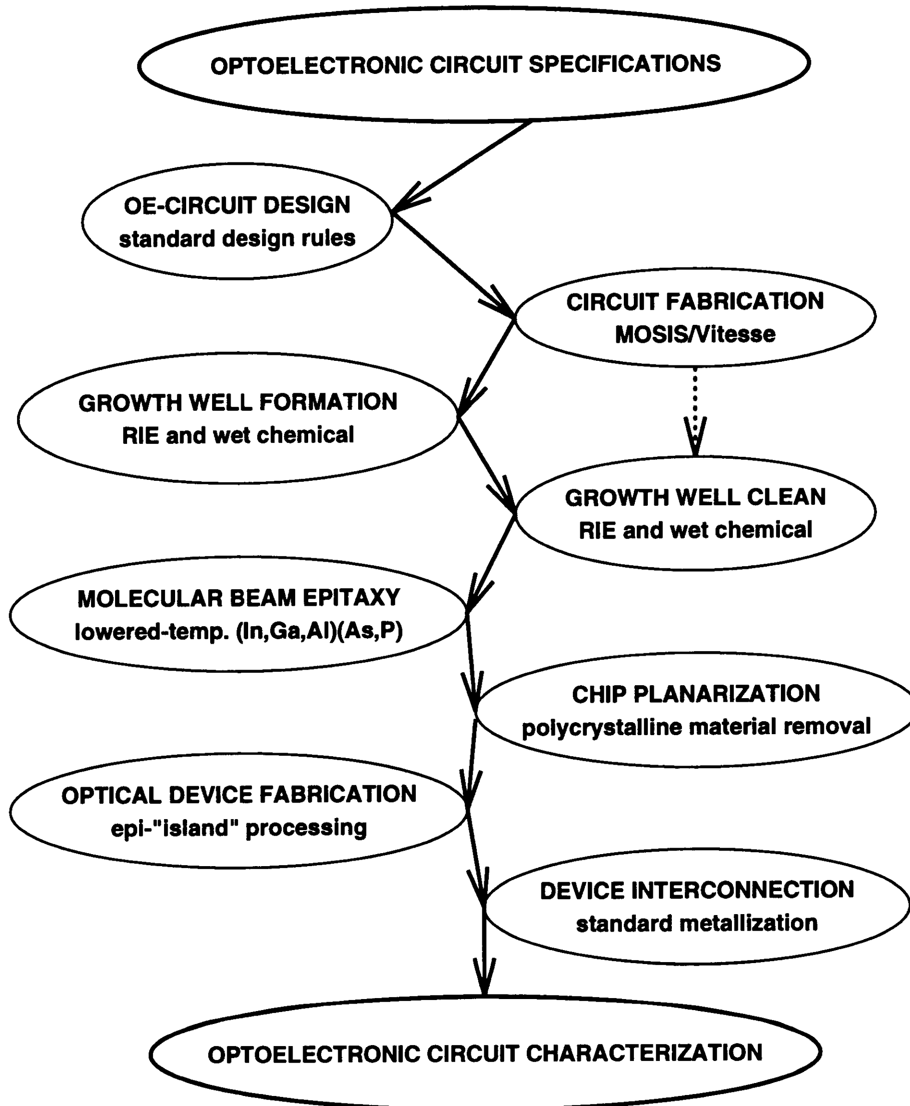

Figure 4.1: Optoelectronic circuit fabrication flow using the E-o-E integration technology [87].

InGaP-based LEDs have been demonstrated on chips recently [91]. The integration of 1.55μm photodetector naturally exploits InGaAs-based materials system and fits well in the continuous development of EoE.

4.2 MIT-OEIC5/LL-MORX1 Chip

4.2.1 Performance and Stability of GaAs Electronics

Vitesse has been taking advantage of GaAs's superior properties to create chips offering higher levels of performance than their silicon counterparts. The high electron mobility in GaAs translates into lower power dissipation. At any frequency range, Vitesse can come in with a part that consumes less power than Si bipolar or BiCMOS, which is a key cost consideration due to the expense of packaging. Even the drawback of the cost of starting materials is partially offset by the greater simplicity of the Vitesse GaAs process. For example, the standard MESFET process at Vitesse, which yields $f_T > 40$ GHz, is currently done with 0.4–0.5μm linewidths, and requires only 13 mask levels. In contrast, 16–18 mask levels are required in CMOS, and >20 levels for BiCMOS. In the end, the cost of the blank wafer is only a small fraction of the cost of the complete wafer.

Figure 4.2 shows the schematic of Vitesse's HGaAs IV MESFET structure, where four metal layers are constructed for signal routing, power distribution and ground return. The performance of the Vitesse HGaAs MESFETSs is displayed in Table 4.1. The smaller dimensions offer greater speed. In addition, better performance also results in excellent analog performance due to the technique in the newest HGaAs IV process of making contact to p-type surface implant eliminating the backgating. These improved performances make both Vitesse analog and digital VLSI circuits ideal for the construction of the cost-effective monolithic optical receivers using epitaxy-on-

electronic technology.

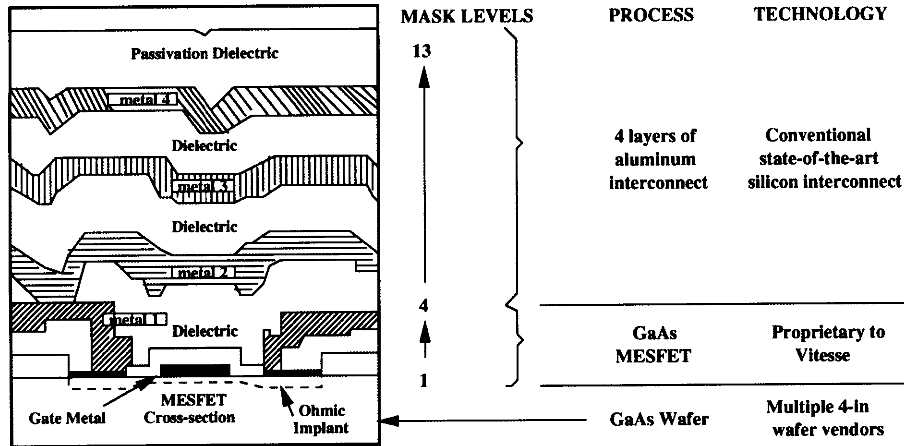

Figure 4.2: Schematic of Vitesse's HGaAs MESFET structure. Four layers of metal interconnects are implemented using the conventional state-of-the-art silicon interconnect technology (Jim Mikkelson, private communications).

Recent work by researchers at MIT has shown that Vitesse gallium arsenide MESFETs fabricated using commercial VLSI processes incorporating refractory metal ohmic contacts and gates, and standard silicon-IC-like multi-level metal interconnect technology, are not adversely affected by several hours at elevated temperatures [92]. This means that these devices will survive the molecular beam epitaxy growth sequence for many III-V optoelectronic device heterostructures. In fact, these MESFETs still function after being annealed at as high as 700°C, but as Figure 4.3 illustrates, the room temperature characteristics of the upper-level interconnects change after annealling above roughly 470°C. Thus if established design rules and simulation tools are to be used, the bulk of the epitaxial growth run must be conducted at 470°C, or less.

4.2.2 GaAs OEIC Chip Design

A customized OEIC chip has been designed and termed MIT OptoElectronic Integrated Circuits 5 (MIT OEIC5) and Lincoln Lab Monolithic Optical Receivers 1 (LL MORX1). The design of the circuits is based on the design tools developed for the Vitesse HGaAsIII process. A design layout for the OC12(622 Mbps) transimpedance amplifier from Robert Deming of Vitesse is incorporated along with the design of the dielectric growth wells (DGWs) developed at MIT. Six individual receivers cells including polarization diversity receivers, dual balanced receivers, single detector receivers, and other testing cells are included on the chip. Figure 4.4 shows the complete circuit layout of MIT OEIC5/LL MORX1 chip. The OEIC chip was fabricated by Vitesse via MOSIS.

4.2.3 Available OEIC Circuits

PDRx: Polarization Diversity Receivers.

Coherent receivers require matching of the state of polarization of the local oscillator to that of the received lightwave signal. In a practical situation, only the polarization of the local oscillator can be controlled. The polarization state of the received signal is

Parameter	*H-GaAs II*		*H-GaAs III*		*H-GaAs IV*	
	E-mode	D-mode	E-mode	D-mode	E-mode	D-more
$V_T(V)$	0.25	-0.7	0.24	-0.8	0.22	-0.5
$L(\mu m)$	0.80	0.80	0.60	0.60	0.50	0.50
$\beta(mA/V^2mm)$	174	155	280	220	380	340
$R_s(\Omega - mm)$	1.25	0.84	0.83	0.80	1.40	0.85
$g_m(mS/mm)$	207	223	250	280	310	340
$g_{ds}(mS/mm)$	4.0	13.0	14.5	27.0	6	13
$f_T(GHz)$	20.6	23.7	25	32	30	40

Table 4.1: Vitesse HGaAs process evolution: MESFET performance (Jim Mikkelson, private communications).

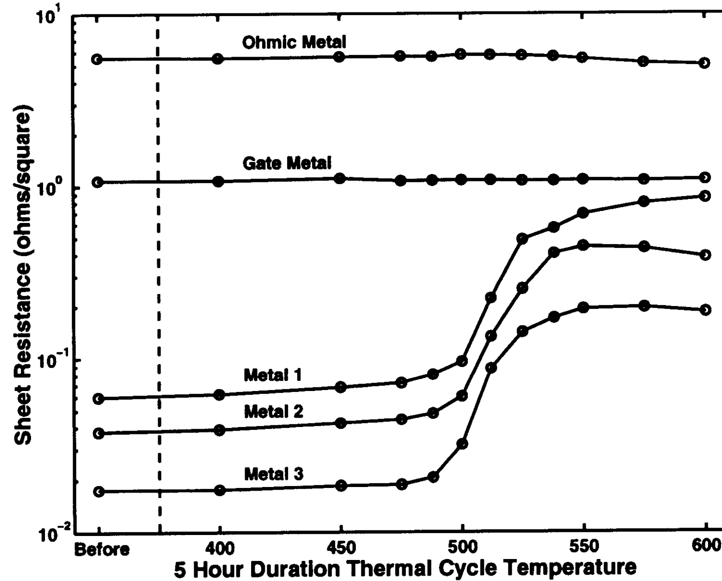

Figure 4.3: Metal-layer sheet resistance after 5-hour thermal cycles. The gate metal consists of 3500 Å WN_x deposited over the channel implant. The ohmic metal consists of 700 Å NiGe deposited over the source/drain (S/D) implant followed by a 100 Å WN_x barrier. The metal 1 through metal 3 layers are a WN_x/$AlCu_x$/WN_x sandwich with thickness ranges of (1000Å -1500Å)/(8000Å -17000Å)/(1000Å), respectively. The WN_x contains 10–20 atomic percent nitrogen and the $AlCu_x$ contains about 1% copper [92].

usually different from the one launched from the transmitter since it varies with time according to various environmental changes such as temperature and stress. When the polarization states of the local oscillator and the received signal are not well matched, the aligned component or so called heterodyned component only utilizes a fraction of the total power delivered by the received signal for the data detection. The system performance is thus degraded.

Several techniques have been conceived to minimize the effect of the polarization fluctuations. The proposed methods include (1) received signal polarization control, (2) polarization spreading, and (3) polarization diversity. Polarization diversity is the best candidate for obtaining polarization fluctuation insensitivity in coherent detec-

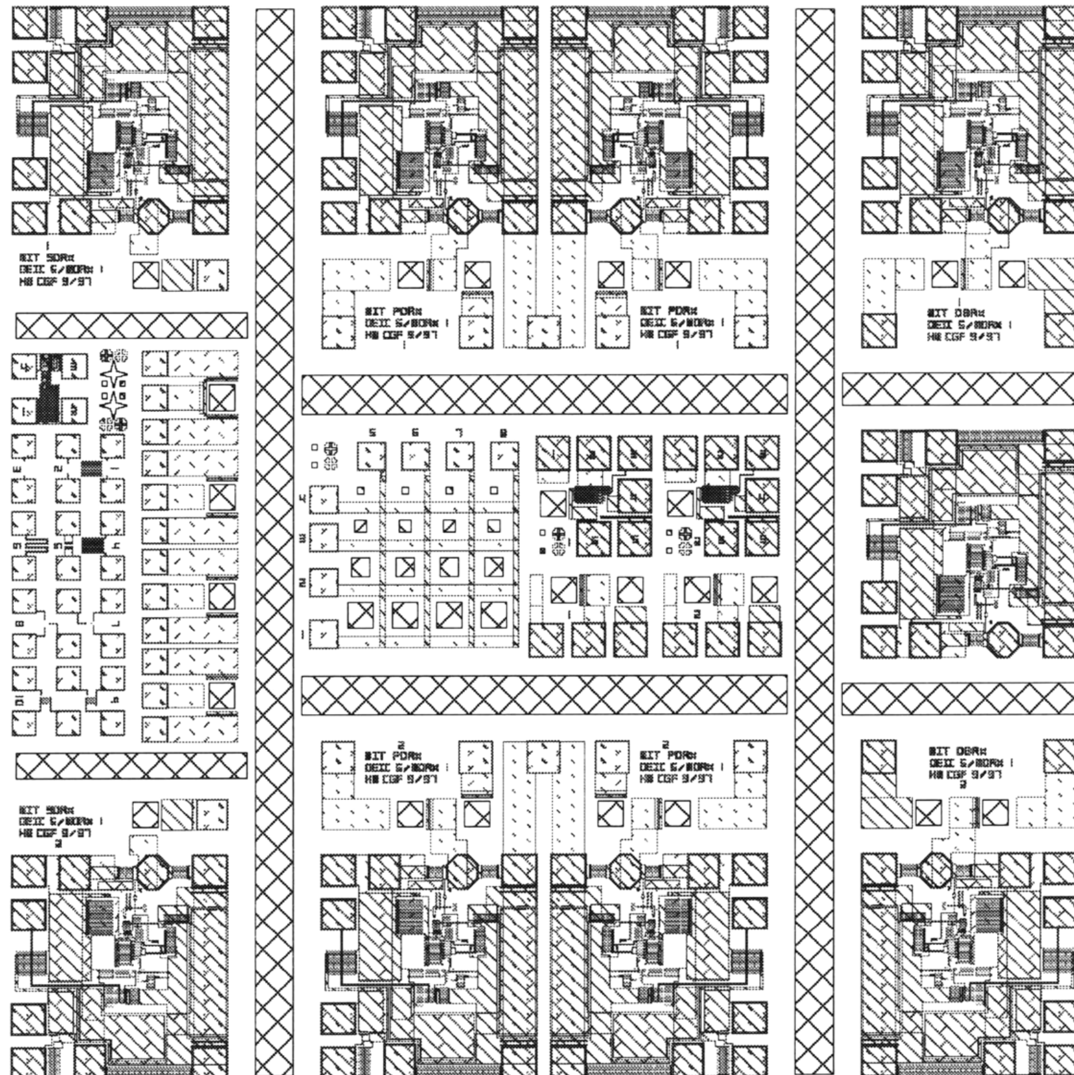

Figure 4.4: Circuit layout of MIT OEIC5/LL MORX1 chip (4mm × 4mm) showing different kinds of the receiver circuits and various diagnostic circuits. The rectangles and squares of various sizes with the cross lines are dielectric growth wells (DGWs).

tion [93, 94]. The insensitivity with respect to polarization fluctuations is achieved by deriving two demodulated signals stemming from two orthogonal polarizations of the received signal. The two signals are then combined so as to obtain a decision signal virtually independent of the polarization of the received signal.

Usually the hybrid polarization diversity receiver presents a complexity almost doubled with respect to a standard receiver. This makes the monolithic OEIC integration very attractive since the multiple photodetectors are made in close proximity simultaneously in the same process. Balanced wideband polarization diversity optical receiver circuits has been designed on MIT OEIC5/LL MORX1 chip as shown in Figure 4.5. Four photodetectors are 250μm apart from each other while aligned along the same line. Each polarization utilizes a balanced dual detector optical receiver for noise reduction. After the OEIC integration, a fiber ribbon will be used to simultaneously align the diversified signal beams into these four photodetectors.

DBRx: Dual Balanced Receivers.

The dual-detector balanced optical receivers have several advantages over other simpler receivers. The dual balanced receivers can cancel excess intensity noise generated by local oscillator so as to efficiently use the available signal and local oscillator power. This will improve the overall receiver sensitivity [48].

The Dual detector balanced receiver OEIC circuits are designed and fabricated on MIT OEIC5/LL MORX1 chip, as shown in Figure 4.6. Balanced coupling efficiency to both detectors can be obtained by a single alignment procedure. When the two photodetectors are fabricated in close proximity, the sensitivity as well as the optical and electrical path lengths can be well balanced between the two. The equalization of path length is important at high bit rates at which the time delay difference limits the performance.

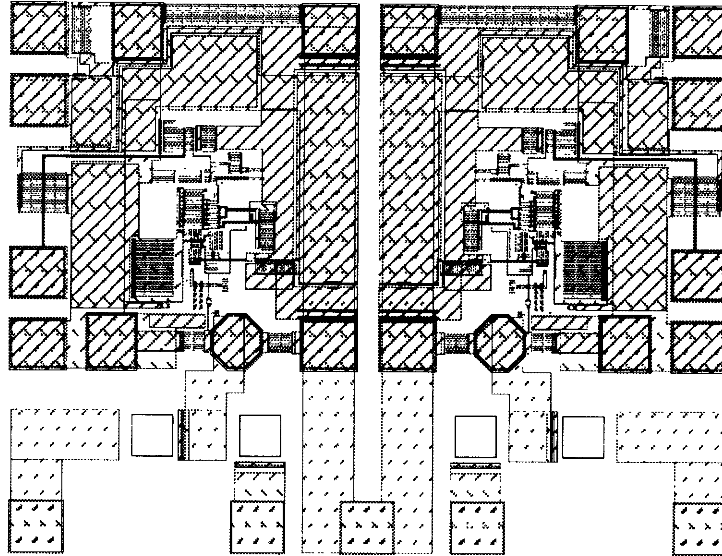

Figure 4.5: Circuit layout of the polarization diversity receivers on MIT OEIC5/LL MORX1 chip. The four blank squares 250μm apart from each other are dielectric growth wells (DGWs).

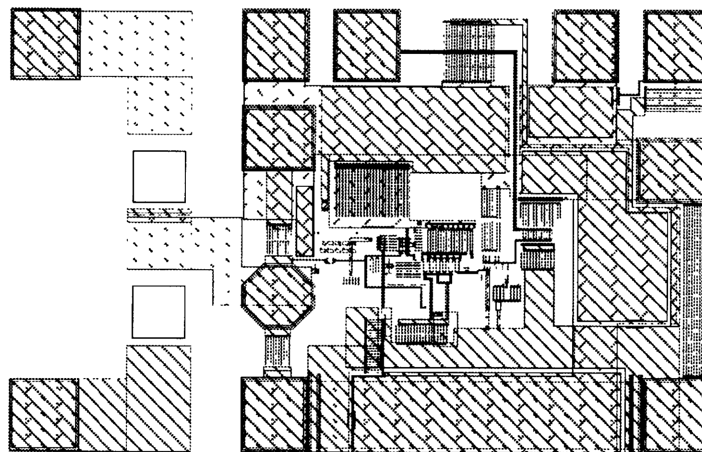

Figure 4.6: Circuit layout of the dual balanced receivers on MIT OEIC5/LL MORX1 chip. The two blank dielectric growth wells on the left side are 250μm apart in order to make the single alignment possible using the commercial fiber ribbon.

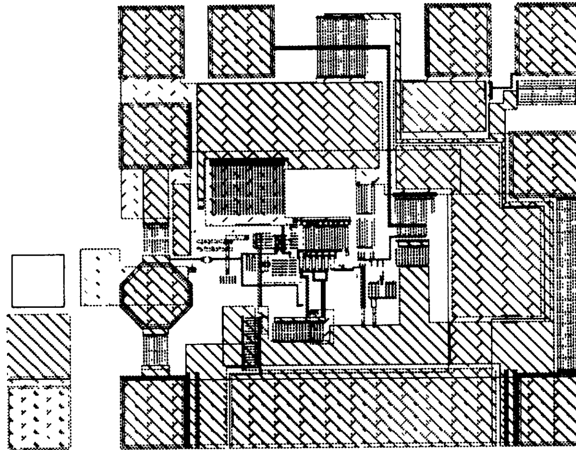

Figure 4.7: Circuit layout of the single detector receivers on MIT OEIC5/LL MORX1 chip.

SDRx: Single Detector Receivers.

The simplest optical receiver designed on MIT OEIC5/LL MORX1 chip only use one detector and one transimpedance amplifier. as shown in Figure 4.7. This cell is included mainly for process control purposes for the qualifications of discrete photodetector and the integration process.

PCM (Process Control Module) and Microwave Cell.

The process control module (Figure 4.8) includes the following components:

(1) Bottom row from right to left: two enhancement-mode field effect transistors (EFET) with both small and large gate length; two depletion-mode field effect transistors (DFET) with both small and large gate length; gate metal, metal 1, metal 2, metal 3 thin metal resistor snakes; one ring oscillator for gate delay measurement; and one alignment mark which could also be used as RIE etch monitor.

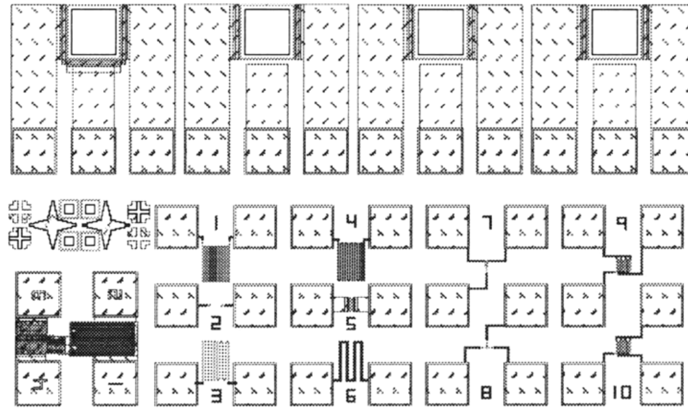

Figure 4.8: Circuit layout of the process control module and microwave testing cell on MIT OEIC5/LL MORX1 chip.

(2) Top row from right to left: two microwave probable photodetectors; one microwave open photodetector; and one microwave short. The triple ground-signal-ground bondpads are suited for the microwave probes with both 125μm pitch and 150μm pitch.

DGW Array; LED Driver; Dual Balanced Detectors.

An array of dielectric growth wells of various sizes are designed on the chip for discrete device characterization, as shown in the right hand side of Figure 4.9. Also in Figure 4.9, two LED drivers are included (top right corner in the figure) for potential expansion of the lattice-mismatched EoE integration to emitter integrations. On the bottom right corner, two dual detector modules are designed for the characterization of the performance matching.

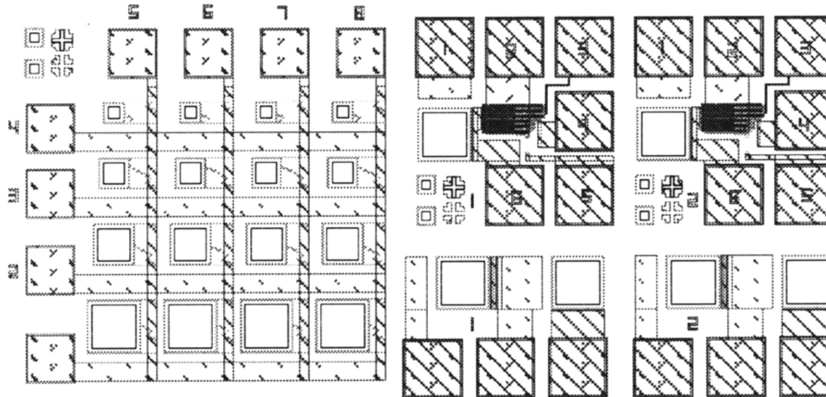

Figure 4.9: Circuit layout of DGW array, LED driver, and dual balanced detectors on MIT OEIC5/LL MORX1 chip.

4.2.4 Amplifier Performance

The transimpedance amplifier incorporated in the OEIC chip was originally designed by Robert Deming at Vitesse Semiconductor Corp. The specification of the original design was SDH/SONET 622Mb/s compatible with a modulation bandwidth of 600Mhz. It also had an integrated automatic gain control (AGC) circuit.

In the process of incorporating Deming's design onto MIT OEIC5/LL MORX1 chip, the AGC was turned off by Vitesse under mutual agreement. In addition, the MOSIS administrated Vitesse foundry lacks a few processing steps which were included for Vitesse commercial production. Several layers from Deming's orignal design were either removed or modified to satisfy the MOSIS specification.

The fabricated MIT OEIC5/LL MORX1 chip has been tested. Three chips were measured by Robert Deming at Vitesse, and the amplifiers on all three chips worked up to 500Mhz, as seen in Figure 4.10, which is consistent with the performance expected from the modified Vitesse design. The reduced bandwidth is still sufficient

for 622Mb/s data rate.

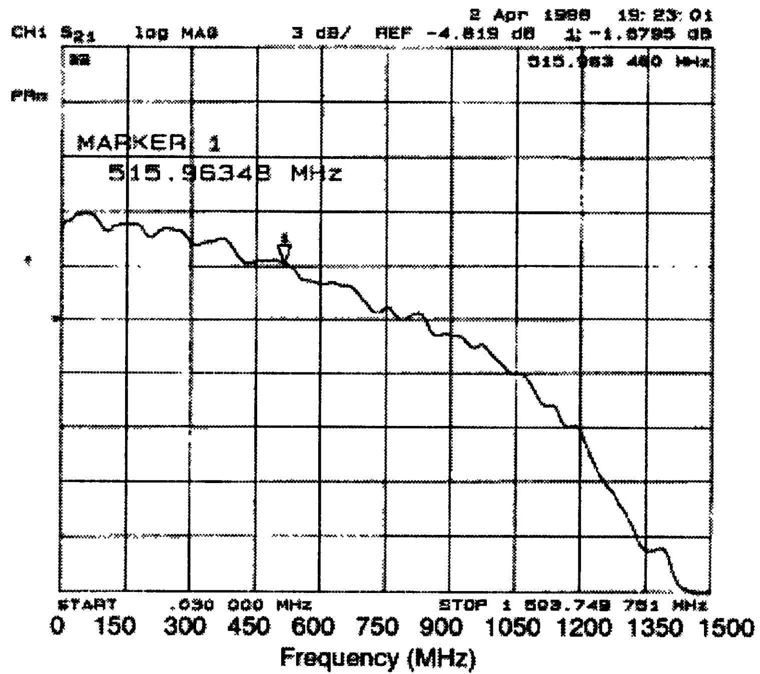

Figure 4.10: The bandwidth of a fabricated transimpedance amplifiers on MIT OEIC5/LL MORX1 chips. The bandwidth measurement was performed by Robert Deming at Vitesse Semiconductor Corp. after the chips were fabricated.

4.3 EoE Integration Process

After final metallization in the commercial foundry, MIT OEIC5/LL MORX1 GaAs IC wafers, which contain transimpedance amplifiers, have dielectric insulation and metal interconnection layers totaling approximately 6.5 microns in thickness covering their entire surface. In the epi-on-electronics process, this coating of dielectric and metal is removed in certain regions to expose the underlying GaAs wafer surface, as illustrated on the top in Figure 4.11. It is in these openings that the optoelectronic devices will be created. The wafer is then placed in a molecular beam epitaxy (MBE) and the desired heterostructures are deposited. Where GaAs wafer surface has been exposed, the deposition is epitaxial; elsewhere, polycrystalline material forms. The polycrystalline deposit is then removed, as shown in the middle illustration in Figure 4.11,

If the thickness of the heterostructure was designed to match that of the original dielectric and metal overcoating, then at this point the wafer surface is essentially planar. The epitaxial heterostructures are subsequently processed to create the intended optoelectronic devices and to monolithically interconnect them with the pre-existing electronics, which completes the process. The final structure is illustrated at the bottom in Figure 4.11.

4.3.1 Chip Cleaning

The chip cleaning is a rather tedious process. The major goal is to expose GaAs substrate covered originally by the dielectric stacks produced during the making of the electronic circuits. The dielectric stack is about 6.5μm thick and consists different material layers such as SiO_2, Si_3N_4, and WN/Al/WN metal sandwich. The optimized cleaning process should be such that the linewidth definition of dielectric growth wells should be preserved while the surface of the exposed GaAs is free of particulates,

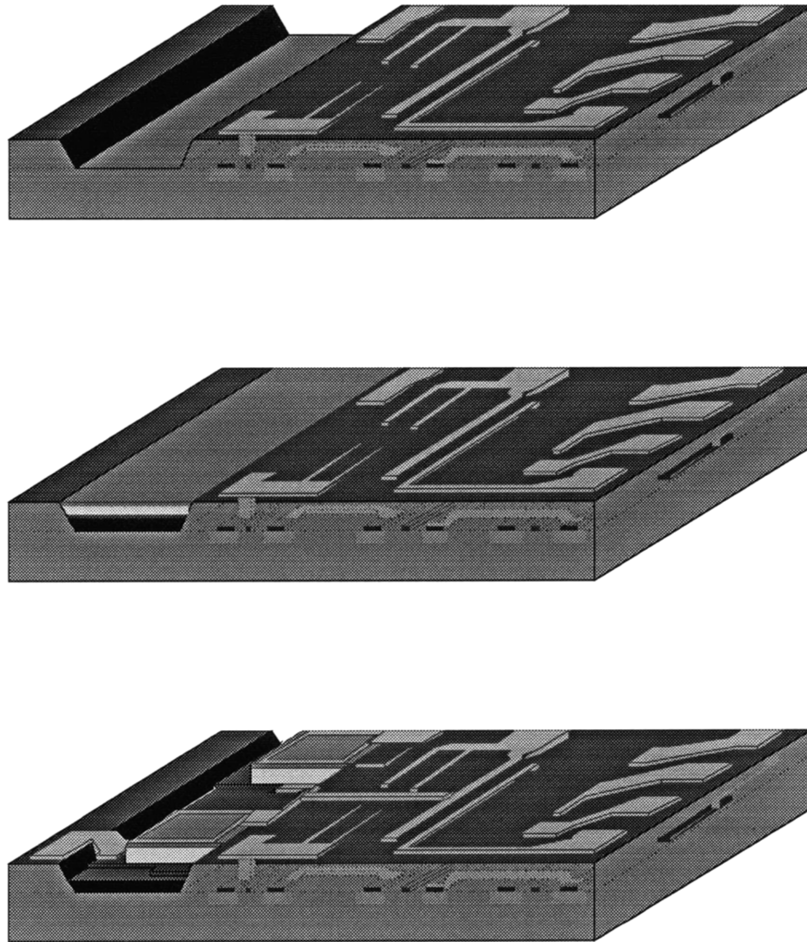

Figure 4.11: Illustration of epitaxy-on-electronics (EoE) integration of monolithic optical receivers. (a) High speed transimpedance amplifier (TIAs) have been fabricated on a semi-insulating GaAs substrate with growth wells left open. (b) After the growth well cleaning, a lattice-mismatched $In_{0.53}Ga_{0.47}As$ PIN structure has been grown in the well. Polycrystalline material on the TIA circuits has been removed. (c) Dual-balanced photodetector pairs are processed and integrated with the TIAs to form a high speed optical receiver working at 1.55μm telecommunication wavelength.

impurities, and mechanical damages.

The cleaning process is developed as shown in Figure 4.12: The OEIC5 chips came

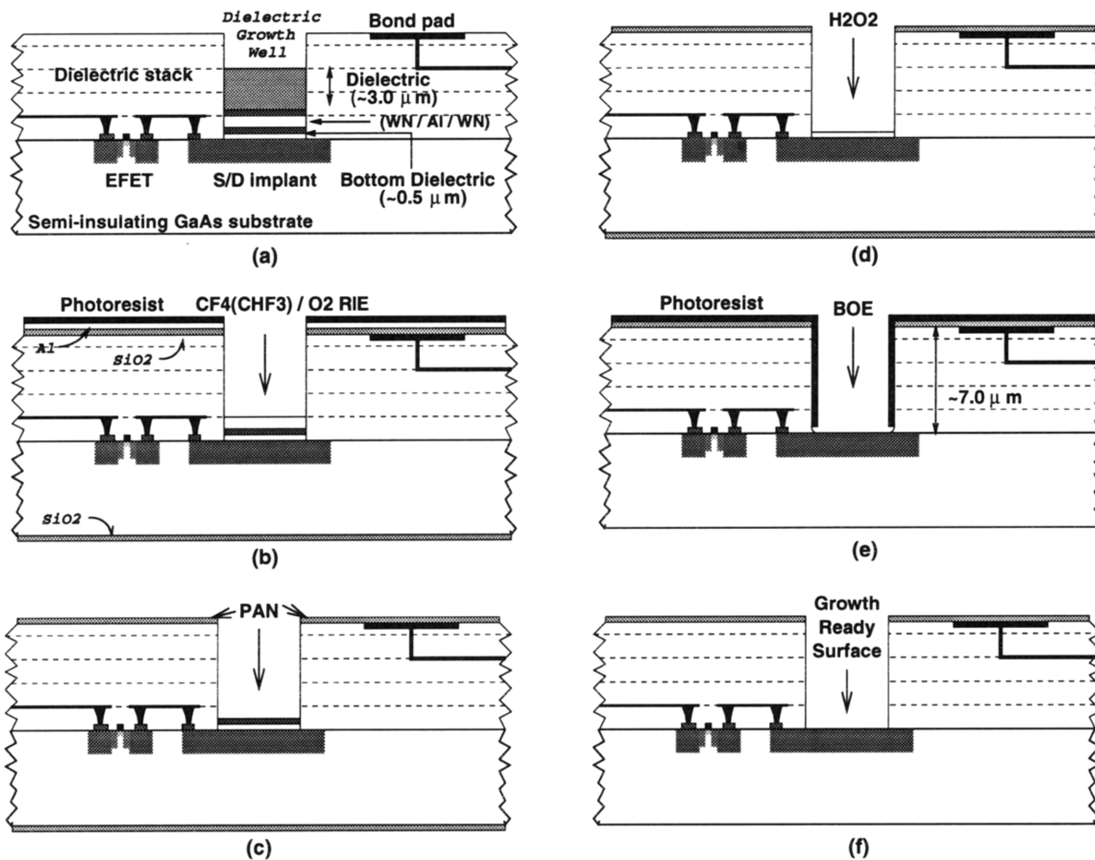

Figure 4.12: Dielectric Growth Well (DGW) cleaning process for MIT OEIC5/LL MORX1 chip.

with about 3μm thick dielectric above the metal one layer in the growth well. Since there is a metal layer underneath it, dry etching using CF_4/O_2 chemistry is the best solution because it maintains better linewidth control than wet buffered oxide etch does.

First, ~7000Å SiO_2 is deposited on both sides of the chips using PECVD to protect the bondpads and the chip backside from the subsequent multiple etching steps. This

leaves the total thickness of dielectric in the growth well up to 3.7μm. Then ~6000Å Al is thermally evaporated on the chip. The Al will act as the RIE etch mask for the oxide etch. PAN etch was used to pattern the Al mask so that the oxide is exposed in all the growth wells. While HCl attacks both positive and negative photoresists, PAN etch often gives cleaner, faster results. The SiO_2 deposited on the back side of the chip protects GaAs substrate from being etched by the PAN etch. After the PAN etch, the photoresist used to pattern Al was left on the chips during the following RIE etch to give the best etching result.

Then the thick 3.7μm oxide is etched away using the standard reactive ion etching. The gas mixture used is either CF_4/O_2 or CHF_3/O_2. The RIE etch is a fairly long process and takes more than 3.5 hours for a given etch rate of about 1μm/hr. The etching will eventually stop at the top surface of Al in the metal one layer. As described before, the metal one layer consists of sandwich layers of WN/Al/WN. The first WN_x layer seems to be etched away during the RIE etch.

The whole chip is dumped into PAN acid mixture again to etch away both the Al mask and the metal one Al layer. The following H_2O_2 dip removes the bottom WN_x layer and exposes the last layer of the dielectric layer at the bottom of the well.

Removal of the last dielectric layer is a rather delicate endeavor. Plasma etching is excluded due to the possible contamination of the substrate surface. Buffered oxide etch (BOE) is preferred but it will undercut the dielectric underneath the sidewall. To make the situation worse, due to the existence of silicon nitride in the final dielectric layer, etching using BOE takes longer than normally expected. The pace of the undercutting is fast so that leaving the chip in the BOE until the dielectric layer is gone will result in a lateral undercut of several tens or 100 of microns, posing the threat of destroying the isolation and metals in its pathway. Thus, the finally BOE etch is divided into multiple steps. Each step requires a new photoresist coating and

photolithography. The photoresist is used to cover the newly exposed sidewall to protect it from being eroded by BOE. Typically this takes about 2 to 4 steps before the substrate is fully exposed.[1] Finally, thorough degreasing using the elaborated solvent cleaning is conducted and the chip is ready to be mounted for the MBE growth.

4.3.2 Reduced Temperature MBE

Most epitaxy of GaAs-based heterostructures is performed at temperatures well above 500°C; MBE is typically done at 650 to 700°C. These temperatures are dictated, for the most part, by the use of AlGaAs wide bandgap layers and the fact that the quality (purity and morphology) of AlGaAs epilayers in general improves as the growth temperature is increased. In this thesis research, a narrower bandgap material, namely InGaAs, was used, leading to the subsequent reduction in the aluminum fraction in the active device region. Thus, high quality growth under 470°C could be achieved.

Another restriction of conventional molecular beam epitaxy is the initial surface preparation step which typically involves a brief cycle to 600°C or higher to desorb any oxide layer on the substrate surface. (A thin layer of oxide is often intentionally formed during substrate preparation to provide a protective, reproducible film on the substrate surface.) Recently, however, atomic hydrogen has been used to remove this oxide film at temperatures below 400°C [95, 96], and a high temperature oxide removal step is no longer essential.

The hydrogen atom can readily react with the native oxide on the GaAs substrate such that the oxide can be gradually reduced until it completely disappears. The hydrogen thermal cracker is installed in our MBE as described in Figure 4.13. The

[1]For the chip used specifically in the later EoE growth, 3 BOE steps were involved.

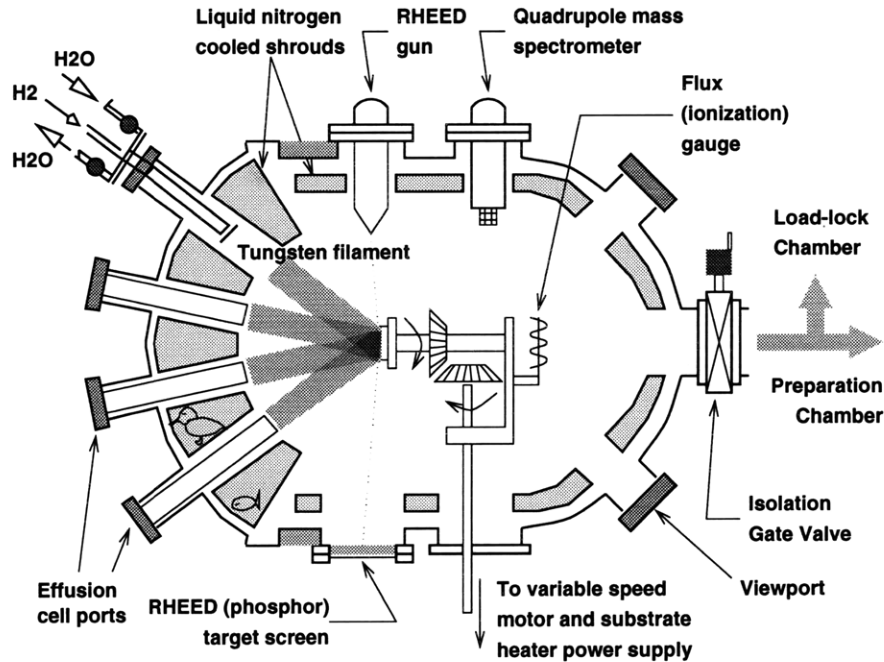

Figure 4.13: Installed Hydrogen cracker in MIT solid source MBE system.

installed hydrogen cracker has tungsten filament which is heated to over 2000°C when the hydrogen is passing thorough. The hydrogen molecules are thus thermally cracked and the atomic hydrogen impinging on the substrate surface reduces the native oxide on GaAs surface. The oxide is resolved in about half an hour at 450°C. The desorption could be faster and at even lower temperature if the thermal cracking efficiency is improved. This could be done by using dedicated higher current power supply to elevate the tungsten filament up to more than 2300°C where more than 15% cracking efficiency can be achieved.[2]

[2]private communication with the cracker manufacturer, Effusion Science.

4.3.3 EoE Material Evaluation

The MBE growth on the OEIC5 chip was done at a temperature about 475°C. A piece of the bulk n-type GaAs wafer was mounted at the side of the chip to help monitor the oxidation removal and the growth quality. The layer structure for this growth was similar to that in Figure 3.10 except the grading buffer is now 5.1μm thick using lower indium composition grading rate of 10%In/μm.

The yield of the growth in the dielectric growth wells was about 50%, i.e., half of the growth wells had single crystalline materials. The low yield may be due to either the incompleteness of the oxide removal prior to the MBE growth, or the wells were not sufficiently clean to start with.[3]

The X-ray analysis on the bulk monitoring wafer confirmed that the material consists $In_{0.55}Ga_{0.45}As$ which is suitable for the 1.55μm photodetection. The cathodluminescence shows that the material quality on the chips is comparable to that on the bulk substrate as given in Figure 4.14. One interesting observation is that the surface morphology looks strikingly different for the materials grown on a bulk GaAs substrate and on a chip(Figure 4.15 and Figure 4.16). The materials in the growth wells do not show the cross hatch that the bulk materials have. This might suggest that there is a different lattice relaxation process during the epitaxial growth in the confined small area of the well.

The cathodluminescence spectra for 4 growth wells in close proximity, shown in Figure 4.17, are given, along with that from the bulk monitoring wafer, as shown in Figure 4.18 and Figure 4.14. The result shows that even though the 4 growth wells are placed in close proximity, the cathodluminescence intensity varies quite significantly. The reason for this may very likely to be the non-uniformity of the

[3]Well cleaning has always been a rather labor intensive and time consuming for the Epitaxy-on-Electronics process. The cleaning procedure is also subject to modifications due to constant process changes of the manufacturing foundry. This may ultimately limit the manufacturability of EoE.

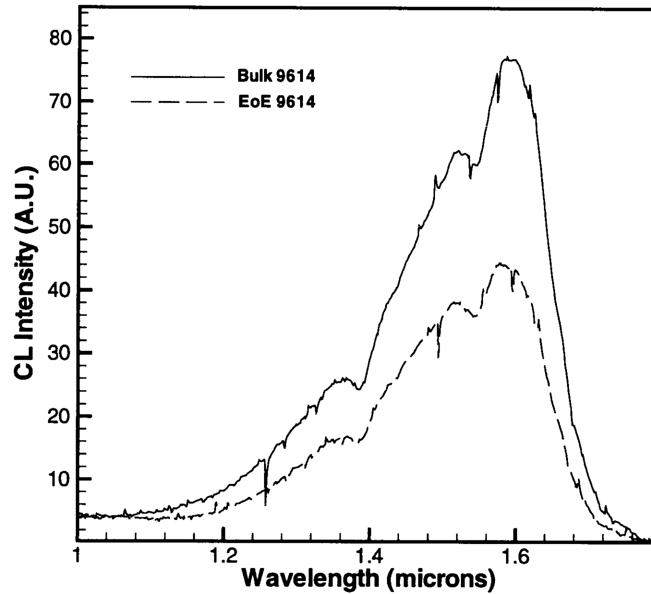

Figure 4.14: Comparison of the cathodluminescence from the bulk monitor Sample 9614 and the material grown in a big street well on the OEIC5 chip.

substrate surface cleanness from well to well. It may be also due to the random nature of the distribution of dislocations. Either way, the uniformity of the materials growth in the wells becomes an important issue, especially for the integration which requires sufficiently matched detector pairs. This possibility, which requires additional growth on chips to confirm, motivated the consideration of an alternative process termed aligned pillar bonding (APB) on electronics(Chapter 5), where the substrate surface cleanness becomes less critical and the materials can be bonded onto the chip free of dislocations.

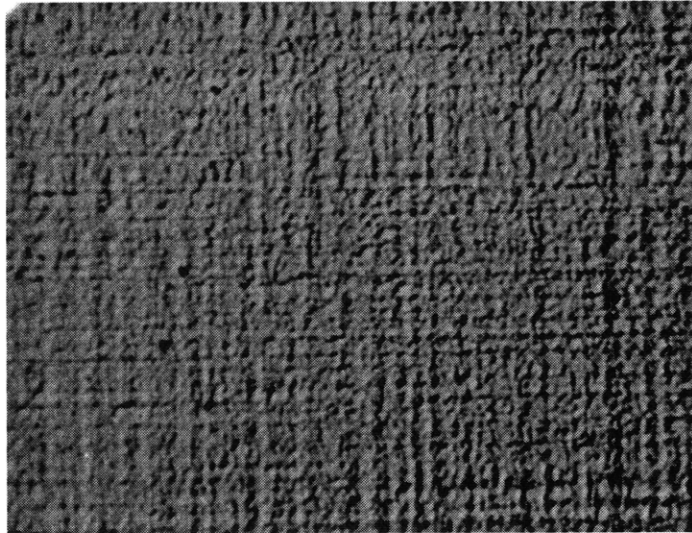

Figure 4.15: 1000× Nomarski photograph showing the surface morphology of bulk Sample 9614.

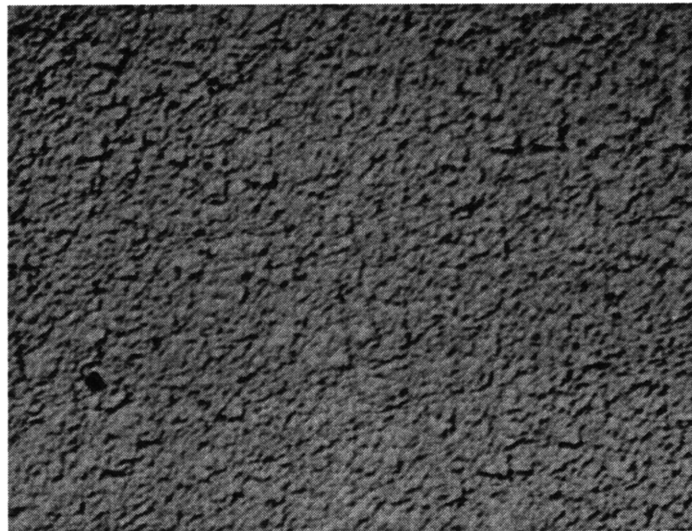

Figure 4.16: 1000× Nomarski photograph showing the surface morphology of materials in a 100×100μm Growth Wells on OEIC5 Chip.

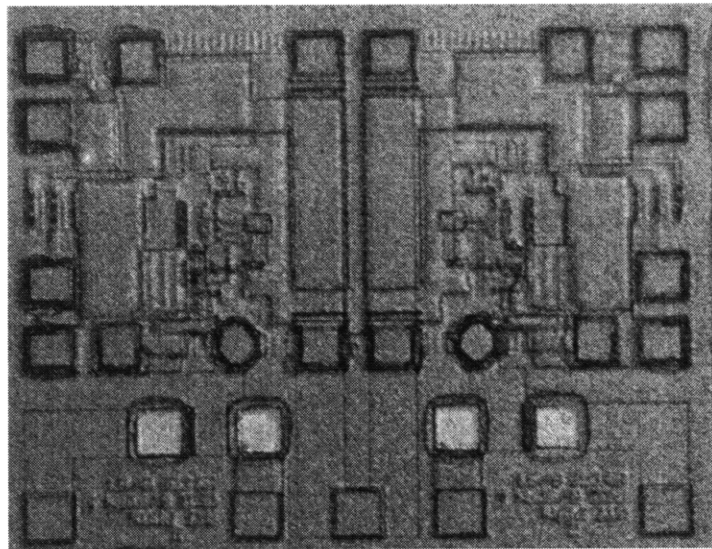

Figure 4.17: The Photograph of a PDRx cell after EoE growth on the OEIC chip. The wells are numbered 1 to 4 starting from the right to the left. The dimension of each growth well is 83μm $\times$ 83μm. The polycrystalline materials is still on the chip, covering the area other than those growth wells.

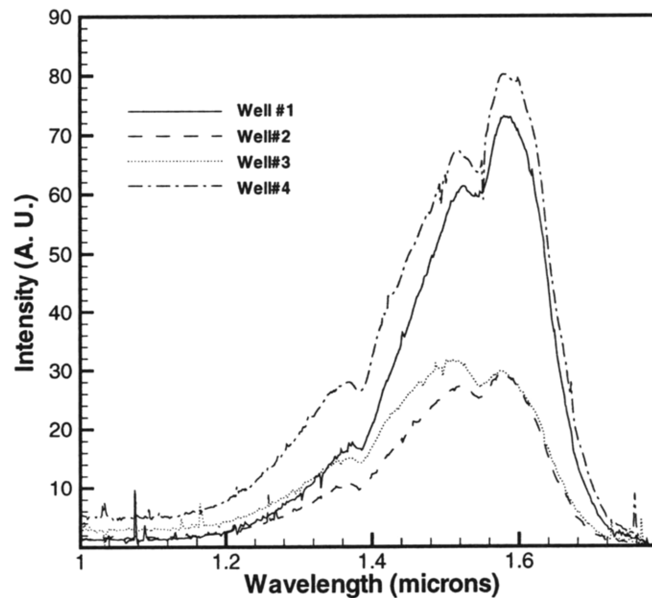

Figure 4.18: The cathodluminescence from four adjacent growth wells on the OEIC5 chips. Well numbers starts from the bottom right hand side corner to the left in Figure 4.17. For each well, the signal was collected from a 60μm $\times$ 40μm area.

Chapter 5

Aligned Pillar Bonding on Electronics

Despite the fact that the semiconductor epitaxial growth can offer a variety of precisely tailored high performance optoelectronic devices, the choice of materials is often limited by the requirement that the growth materials be lattice matched. In order to overcome the challenge posed by the lattice mismatching, in addition to the heteroepitaxial crystal growth, wafer bonding has emerged as another direct approach for the integration of dissimilar semiconductor and optoelectronic materials. While the wafer bonding has been studied intensively by many research groups in the past decade, application of this novel technology to high density optoelectronic integrated circuits is yet to be fully addressed and investigated.

This chapter briefly reviews the current status of the development of the wafer bonding technology (Section 5.1). In Section 5.2, the process requirement, set by the OEIC integration utilizing both existing commercial electronics fabrication foundry and the wafer bonding technology, is discussed. In order to meet the unique requirement for high density OEIC integration, a novel OEIC integration technology

termed Aligned Pillar Bonding (APB) is formalized. The APB process utilizes the reduced temperature wafer bonding, currently based on palladium solid phase reaction with III-V semiconductors, to bond patterned photonic device structures grown on their native, lattice-matched substrates into the designated integration wells in the electronic circuits on other host substrates, resulting in high-density, planarized optoelectronic circuits.

The APB process for the specific application of the integration of 1.55μm photodetectors grown on InP substrate with the commercially available high-speed GaAs MESFET VLSI density electronics is then being developed. The new process poses new challenges such as fast deep anisotropic etching for the making of the pillars of photonic device structure, and the wafer scale backside aligned pillar-to-well bonding with subsequent substrate removal. To overcome these challenges, electron cyclotron resonance (ECR) enhanced reactive ion etching of III-V compound semiconductors using Cl_2/He chemistry was developed which resulted in high aspect ratio, straight side wall pillars with smooth surface, as will be described in Section 5.3. The feasibility of the 1.55μm photodetectors bonded on GaAs substrates is then demonstrated using the Palladium assisted bonding described in Section 5.4. Finally etched pillar and the OEIC5 chips were aligned and the p-i-n diode heterostructures on InP were subsequently transferred into the bonding wells of an OEIC5 chip(see Section 5.4).

5.1 Wafer Bonding and Wafer Fusion

The interest in bonding of different crystalline and/or non-crystalline materials has been growing in the past decades, motivated by achieving the goal of realization of numerous novel devices and integration scheme exploiting various materials with different properties. The process is relatively simple, and thus this makes it very attractive.

The most widely studied bonding is between silicon and oxidized silicon, motivated by producing the silicon on insulator (SOI) substrates. The interest in bonding of silicon and a variety of other substrates is further motivated by numerous micromechanical applications. The techniques developed in silicon-related work is often subsequently transferred to bonding work involving III-V semiconductors.

The essence of the wafer bonding technology is that the misfit dislocations are strictly confined at the bonding interface for strain release. Therefore, there are no threading dislocations in the device layers, which is very essential for meeting the demands which device requirements place on the electrical and optical properties of the active materials.

The bonding of III-V compound semiconductor materials is primarily driven by the desire to realize various optoelectronic devices and integration schemes. Examples of bonding for integration include wafer bonding of InP to GaAs [97, 98], and InP to Si [99, 100].

Most recently, the technology referred to originally as wafer fusion and later as bonding by atomic rearrangement requires no foreign materials at the bonding interface [97, 98, 100]. Among the major features sought from wafer fusion techniques are optical transparency, good heat sinking, and high electrical and thermal conductivity. Wafer fusion can simultaneously offer these characteristics because of the absence of foreign materials at the bonded interface and hence the formation of a physical junction with properties similar to a heterojunction.

Although the detailed bonding process for III-V semiconductor wafer fusion may vary among different research groups, most of the bonding work has been done under pressure at an elevated temperature, and in a hydrogen ambient [100, 101]. III-V semiconductor fusion occurs between InP and GaAs compounds with a bonding temperature typically above 600°C. Although the process of the wafer fusion of GaAs

and InP is not fully understood, it is suggested that mass transport, or so called atomic rearrangement, occurs [101]. At the fusion temperature, P_2 dissociates from InP leaving behind mobile indium atoms at the interface. GaAs wafer in the close proximity prevents the P_2 from leaving the interface thus maintains the interface in the equilibrium state. The phosphorous fills the gaps in the junction while the indium diffuses laterally to fill any voids. Later on, indium reacts with phosphorous again to form an InGaAsP alloy and InP substrates thus conforms to GaAs.

Many important optoelectronics devices have been demonstrated using the wafer fusion process, including long wavelength vertical cavity surface emitting lasers (VCSELs) [102, 103, 104, 105], resonant cavity enhanced photodetectors [106], and high brightness light emitting diodes (LEDs) [107, 108]. All of the demonstrated optoelectronic devices were fabricated on bulk substrates and diced into discrete devices. The "integration" in these cases is mainly focused on integrating dissimilar materials with little emphasis on larger scale optoelectronics circuits. The bonding process is thus designed to enhance the discrete device performance only.

5.2 Aligned Pillar Bonding Process

5.2.1 Aligned Pillar Bonding on Electronics

As described in Chapter 1, a successful optoelectronic integration technique would take full advantage of the mature electronics industry in order to impact commercial systems, which require uniformity, reliability, and manufacturability. Bonding III-V photonic semiconductor structures directly onto GaAs or silicon integrated electronic circuits will fulfill this goal and provide the real fast track to commercialize decades' worth of the optoelectronic device development.

Aligned pillar bonding (APB) on electronics is thus proposed as a solution to this

need, illustrated in Figure 5.1. APB involves bonding of an epitaxially grown wafer with the desired optoelectronic device layer onto another wafer with VLSI density electronic circuits.

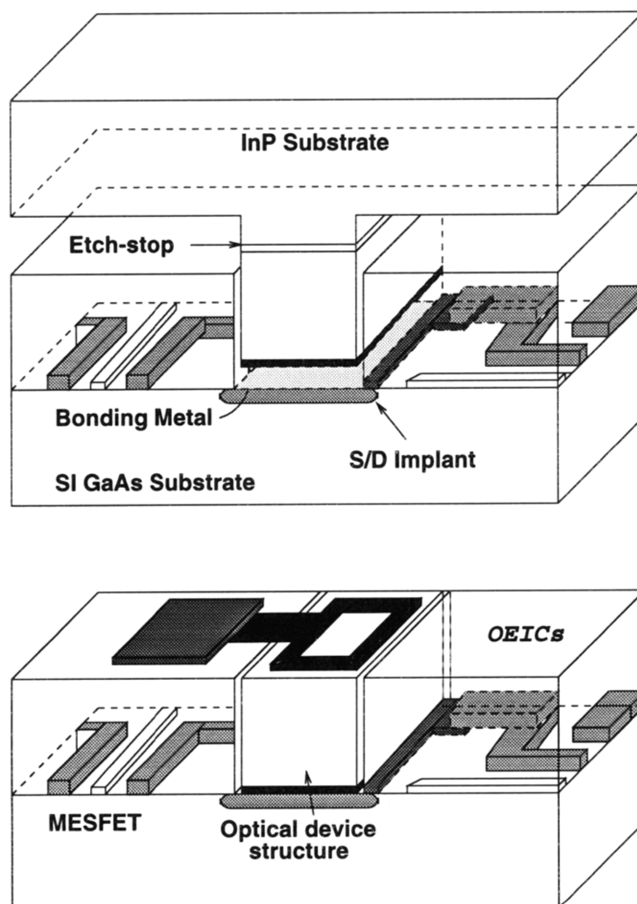

Figure 5.1: Aligned Pillar Bonding (APB) on electronics Process.

On the epitaxial wafer, the photonic device structure is grown on a lattice-matched substrate at the optimum growth temperature to maximize the crystal quality. Then the structure is patterned into small, tall mesas termed"pillars" using standard photolithography. The pattern of these pillars across the wafer is the mirror image of the small openings in the electronics circuits on the other wafer. The openings are termed "wells"; they are pre-designated during mask layout and created during the

commercial fabrication of the electronic circuits. After the IC fabrication process, these wells are covered with the a thick stack of multiple layers of dielectrics. The dielectric is removed partially or entirely during the foundry run. Any remaining dielectrics will be removed by the post electronic fabrication well cleaning process. The substrate hosting the electronics is thus exposed at the bottom of the wells. The pillar wafer and the electronics wafer are next brought together into contact face-to-face, and the pillar and well patterns are aligned using standard photolithographical infrared backside alignment. The mated pair of wafers are then secured and transferred into the bonding furnace, uniform uniaxial pressure is applied perpendicular to the wafer pairs as they are elevated to higher temperature, where the bonding between two wafers occurs. Subsequent substrate removal separates the optoelectronics device layers from the hosting substrate and leaves device structures in the wells of the electronics chips. These structures are then fabricated into devices using the standard micro-fabrication technology. Finally the devices are interconnected with the electronics to form completed OEICs.

The APB process addresses most of the important issues existing in today's integration technology development. It can remove many obstacles faced by other integration schemes. APB can simultaneously satisfy the desire to directly utilize the existing electronics industry, the desire of independent optimization of photonic and electronic components, the desire to maintain planarization and high device density, and the desire to reduce parasitics in the device interfacing. Last but not least, the simplicity of the APB process makes it highly compatible with large scale manufacturing.

5.2.2 Process Requirements for APB

Wafer fusion bonding as described in Section 5.1 is not ideally suited to the task of the aligned pillar bonding on electronics because of the high temperature involved. A reduced temperature bonding technology is required.

One of the most important aspects in the aligned pillar bonding is to preserve the electronics on the chips. As we described in section 4.3, GaAs electronic circuits using Al-based metal interconnection can not sustain any enlongated processing at temperatures above 470°C. For silicon-based electronics, the thermal cycle above 550°C is also detrimental. Thus, the wafer fusion process, which occurs above 600°C is not useful.[1]

Another reason to avoid using the higher temperature bonding process is the issue of thermal expansion coefficient mismatch. Except for some applications integrating devices based on the same substrate, for instance, integrating 850nm photonic devices such as vertical cavity surface emitting lasers (VCSELs) with the GaAs electronics, the majority of optoelectronics integration applications exploit dissimilar substrates. One specific application in this thesis research is to integrate InP-based photodetectors with GaAs-based MESFET VLSI electronics. The thermal expansion coefficient mismatch complicates the photolithographic processing as depicted in Figure 5.2. The resulting dimensional change due to the heterogeneous thermal expansion not only induces large stress on a microscopic scale, but also modifies the alignment achieved at room temperature. This limits the ultimate density of the possible OEICs.

The solution to the afore-mentioned problems is to develop a reduced temperature wafer bonding. The high bonding temperature in the wafer fusion results from the major needs to provide a transparent junction at the bonding interface. This demands the bonding of semiconductor directly to semiconductor without using any

[1] H. Wada, private communications.

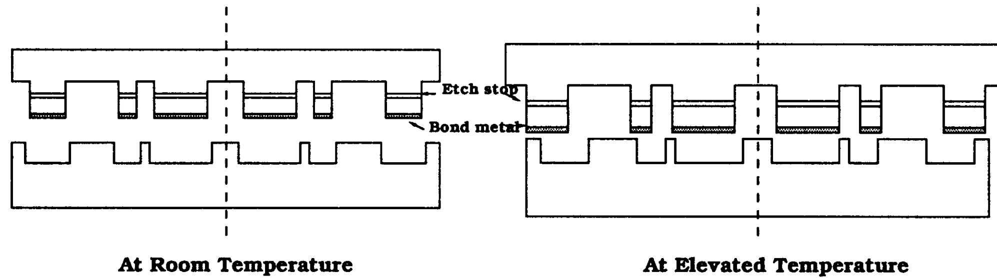

Figure 5.2: Photolithography misalignment caused by the thermal expansion coefficients mismatch. The dashed lines mark the center of the wafer. Top wafer is the pillar wafer with larger thermal expansion coefficient.

foreign materials such as dielectrics and metals. To form covalent bonding between two semiconductor surfaces directly not only requires a huge amount of thermal compression at a temperature higher than 600°C, but also limits the electrical characteristics at the interface. The resistance across the bonding interface is usually high because of the discontinuity in the energy band edge.

On the other hand, some reduced temperature bonding does not readily provide excellent electrical and mechanical strength at the interface for the large scale manufacturing of the OEICs. Such bonding techniques include epitaxial lift-off (ELO) and Van der Waals bonding. Thin film Van der Waals bonding directly onto semiconductors shows that the bonding layer consisted of 20–100Å of native oxides, which prevent the bonded interface from being superiorly conductive.

Since APB process does not require a transparent interface, utilizing foreign materials at the interface is permissible and in fact desired in terms of improving electrical and mechanical properties. Pd-assisted wafer bonding at a reduced temperature seems to be a good solution [109, 110]. Pd-assisted bonding is discussed in the following section.

There are additional requirements for the APB process to be practically achievable, including the fast deep etch of the III-V semiconductors, backside IR alignment, etc. These will be discussed in the following sections.

5.2.3 Palladium Assisted Bonding

In parallel with the vast development of the wafer fusion process, Yablonovitch [109] and Tan [110] developed Palladium(Pd)-assisted wafer bonding.

Pd is uniquely the only metal found so far which readily reacts with both elemental and compound semiconductors at low temperatures ($\sim 200°C$) [109]. The diffusion of Pd into both InP and GaAs is rather smooth and no spiking is observed. The mallability of the Pd layer is also versatile in terms of accommodating the thermal stress as well as the stress due to lattice mismatch between InP and GaAs.

In a typical Pd-assisted bonding, Pd will actually displace and disperse native oxide layers on the semiconductors, while resisting oxidation itself. The surface diffusivity of Pd on Pd is very high, allowing the required mass transport at temperatures as low as room temperature. The ability of palladium to penetrate native oxides on semiconductor surfaces at low temperatures is a remarkable attribute allowing to build highly conductive bonding interface at lower temperature. E-beam evaporated Pd is found to form good Ohmic contact to both GaAs and InP; the Pd bonded to heavily doped p+ and n+ GaAs is also found to have a contact resistance less than $10^{-4}\Omega/cm^2$ [109].

To verify the validity of the reduced temperature Pd-assisted bonding of InP onto GaAs, an experiment was designed following the process developed by Tan [110] [2]. One pair of n-type InP and n-type GaAs substrates are used to prepare 4 pairs of small pieces for bonding: (1) Bare InP bonded to the Pd coated GaAs (2) Pd-coated

[2]The initial experiment was done with the assistance of Donald Crankshaw.

InP bonded to the bare GaAs; (3) Pd-coated InP bonded to Pd coated GaAs; and (4) Bare InP bonded to bare GaAs. The backsides of all eight(8) pieces were e-beam evaporated with Ni/AuGe for the n-type Ohmic contact. The Pd was e-beam evaporated with a thickness of 1500Å.

The four pairs of bonding samples all had a similar size of approximately 6 by 6 mm. They were put into a specially designed graphite fixture which provides a uniform uniaxial pressure of about 84MPa. The graphite fixture is then put into a modified liquid phase epitaxy furnace. The furnace is heated up and stay at the elevated temperature for 90 minutes in the hydrogen ambient. The temperature used for three pairs involving Pd was at 350° while the temperature used for the pair of bare InP and GaAs is at 450°, taking into the consideration that the demonstrated InP directly bonded onto GaAs is performed at above 450°C, while the bonding should occur below 470°C limit set by the stability of the electronics. The backside Ni/AuGe Ohmic contact was annealed simultaneously during the bonding.

All four pairs were bonded. The current-voltage measurement shows Ohmic behavior for all samples, as displayed in the Figure 5.3

The resistance extracted by the I-V curves are only about 2Ω for all three pairs involving Pd. Surprisingly, InP directly bonded to GaAs at 450°C also shows good Ohmic behavior. This is in contrast to the observation made by Wada [111]. It is believed that the longer bonding time (90 minutes in this experiment vs. 30 minutes in Wada's experiment) and higher pressure (84 MPa vs 2.94kPa) may explain the difference. Even though InP directly bonded to GaAs fulfills the basic requirement of acting as Ohmic behavior across the interface, the Pd-assisted bonding is still preferred due to the 100°C lower bonding temperature and three times lower resistance.

While the electrical characteristics of the Pd-assistant bonding has been previ-

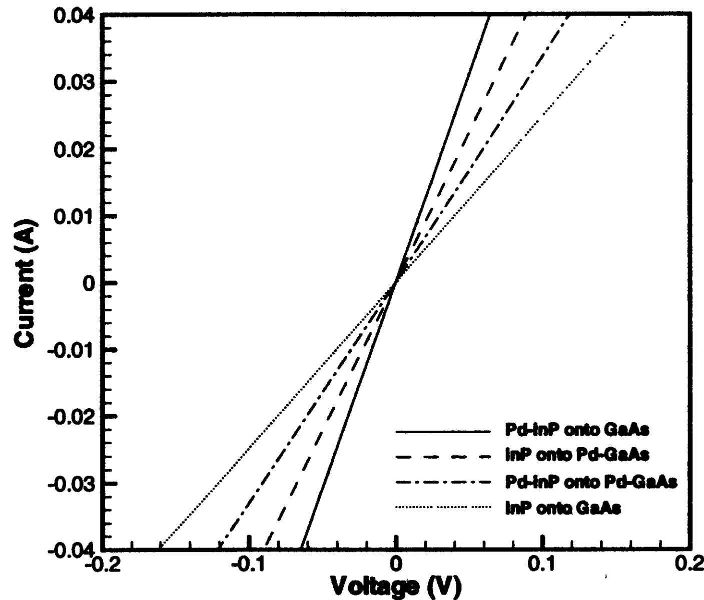

Figure 5.3: Conductivity comparison for Pd assisted wafer bonding.

ously studied for bonding Pd-coated InP to GaAs, and GaAs to Pd-coated glass, the metal to metal bonding between Pd-coated GaAs and Pd-coated InP has not been studied yet. The metal to metal reaction is expected to be harder than the metal to semiconductor reaction at the given low temperature. However the resulted good bonding between Pd surfaces suggests the ability of diffusion of Pd resulting in the required mass transport for the bonding. In addition, the resistance to oxidation makes the bonding interface less bothered with the native oxides. Thus, the Pd to Pd bonding is potentially the best of all.

The present experiment was designed with the on-going perspectives of future OEIC integration. Since bonding of photonic materials onto the electronic substrates may involve various materials different from InP and GaAs. A different substrate such as Si could possibly be used eventually. The electrical characteristics of Pd bonded to substrates like Si and $LiNbO_3$ might not be as good as Pd bonded to InP

and GaAs. The demonstration of the Pd to Pd bonding relaxes the requirement of a solid phase reaction to other substrates since the Ohmic contact can be pre-made underneath the Pd coating and the bonding can still result in good thermal and electrical conductivity through the reaction with the other substrates coated with Pd with good Ohmic contact underneath.

Moreover, even within the scope of bonding InP onto GaAs electronics, Pd to Pd bonding can be very helpful in terms of simplifying the manufacturing process. The cleaning of the bonding wells, which is similar to the growth well cleaning process described in Section 4.3, often requires elaborated effort. Putting the Ohmic contact down in the bottom of the well can be helpful in the subsequent well cleaning process since the bottom of the well can simply be Ohmic contact metal which acts as an etch stop for the dielectric RIE etching. The exposure of the semiconductor substrate is no longer an essential requirement.

5.3 Reactive Ion Etching of InP Based Materials

5.3.1 Needs of Deep Fast Isotropic Dry Etching

One of the challenges posed by the APB process is to etch the III-V semiconductors, InP in particular, into pillars of about $\sim 20\mu m$ in height. This is required for the planarization of the resulting OEICs and the simplicity, let alone the feasibility, of the post-bonding fabrication.

The electronic circuits produced by the commercial foundry, either Si-based or GaAs-based, consist of multiple level metal interconnects, which vary with the various extent of complication of the specific processes. The isolation between the multiple levels of metals employs dielectrics such as silicon dioxide and silicon nitride, which brings the total thickness of the overcoating on VLSI density circuits up to a thickness

of several microns or even more.

For the specific case of GaAs MESFET circuits produced by the Vitesse HGaAs III process as described in Section 4.2, the thinnest portion of the dielectric stack where the bonding wells are defined, is about ~6.5 μm thick. However, the via cuts through each dielectric isolation layer, along with any additional metal contacts and interconnections roughen the topology of the circuits such that the thickest portion of the dielectric stack is about 11μm thick. A 4μm thickness variation across the wafer on the top surface is typically the case. This requires that the pillar be at least 11μm tall.

In addition, the loading effect of typical dry etching process can not guarantee that the pillar height will be uniform across the whole wafer. The fail safe margin for this effect would demand that the pillar etch be about 20μm in depth.

For large packing density of the optoelectronics integration, small lateral pillar size is important. Typical optoelectronic sizes range from a few microns in diameter as in the case of the low threshold vertical cavity surface emitting lasers, up to a few tens to 100 microns in diameter as in the case of the photodetectors designed for multi-mode and/or single mode fiber applications. The etching for the pillar formation is thus required to be of high aspect ratio, and highly anisotropic.

For the specific application in this thesis work, the photodetectors are grown on an InP substrate. The etching process for 20μm deep pillars in InP needs to be developed in order to make the APB process feasible.

5.3.2 Difficulties with InP Dry Etching

The fast etch of III-V semiconductor has been studied intensively, motivated by the needs for deep features such as the via hole formation in substrates for microwave power devices. High aspect ratio features in InP have been demonstrated using laser-

assisted photochemical etching [112, 113]. However, in order to achieve high packing density in the OEIC integration through APB process, the desired etch profile is more anisotropic than what the wet chemical etching can accomplish.

The dry etching of GaAs and related compounds is successfully accomplished with chlorine-based reactive ion etching, with controllable etch rates possible between a few hundreds of angstroms per minute for transistor gate mesa formation to many microns per minutes for through-wafer via application. Smooth surface morphology are often obtained over a wide range of gas mixtures and process conditions because of the high volatility of the Ga and group V chlorides.

However, for the dry etching of InP and related materials, the processing window is much more restricted. Due to the low volatility of indium chlorides, chlorine-based RIE usually results in low etch rates and leads to rough surfaces when used at temperature $\leq$130°C. Productive etching using chlorine requires heating of the substrate to above 150°C to promote desorption of the indium chloride etch products [114]. The necessity to heat the sample limits the possible choice of mask materials to dielectrics or metals, since simple photoresists usually can not act as very defined mask upon baking at 150°C. Undercut also appears at elevated temperature. Even though the addition of CH_4 into the gas mixture [115] can regain the anisotropy with the CH_4 forming a sidewall protection polymer layer, the polymer redeposition is oftenly not desired for many device applications. Carbon-containing halogen gases such as CCl_4, CCl_3F, and CCl_2F_2 can also be used for InP RIE. However, such gases often caused surface roughening due to residual carbon-containing materials [116, 117].

Based on the inability of the room temperature RIE etching of InP using chlorine based gases, the CH_4/H_2chemistry has gained acceptance for dry etching InP [118, 119, 120]. While the mixture provides smooth, anisotropic etching, the rates are low ($\leq$ 600 Å/min) and the simultaneous polymer redepostion requires constant

oxygen plasma cleaning which makes the process even slower. Therefore, the CH_4/H_2 chemistry is particularly unsuitable for applications such as deep mesa (3-4μm) fabrications, let alone the 20μm deep pillar formation intended for mass production of large scale OEICs using the proposed APB process. A different, fast, deep, anisotropic dry etching process, ideally at room temperature is thus needed.

Various studies have demonstrated different etching schemes. Different gases such as Br_2, IBr, and ICl were studied and some etching results were obtained [121, 122, 123]. Even though the processes vary from one case to another, these studies often require elevated temperature and special gas installation and handling, while lacking confidence of control over the etch profile. Other etching technologies such as ion beam induced etching have also been introduced, but the mediocre etch rates are not suitable for the proposed fast deep etching.

The recent development of the high density plasma etching provides a possible solution. By discarding the conventional parallel plate RF generated reactive ion etching configuration, various schemes of plasma discharge configurations such as electron cyclotron resonance (ECR) enhanced plamsa, inductively coupled plasma (ICP) have demonstrated dramatic improvements in InP etching rates and the processing window. ECR etching of InP with over 1μm/min etch rates using Cl_2/Ar chemistry has been demonstrated [124]. The promising results demonstrated in the literature, plus the availability of the new ECR-RIE chamber on MIT campus [3], ECR enhanced reactive ion etching was studied and a new chlorine based chemistry using a Cl_2/He gas mixture has been developed.

[3]The ECR-RIE used in this study is the PlasmaQuest in Microsystems Technology Laboratory (MTL) at MIT.

5.3.3 Electron Cyclotron Resonance (ECR) Enhanced RIE

A plasma consists of positive ions and negative electrons along with a much larger quantity of neutral atoms. In the steady state, the plasma is stable and the electron and ion densities stay constant. Because there are various sources of energy loss inside the plasma and thus a stable system requires an external energy source.

In the conventional parallel plate configuration of the reactive ion etching chamber depicted in Figure 5.4, the energy source is an electric field which acts on the charged particles only. The action of the field is primarily to give energy to the electrons, and the work that the electrical field does on the charged particle is inversely proportional to the mass of the particle. Very little energy is transferred to heavy particles. Any

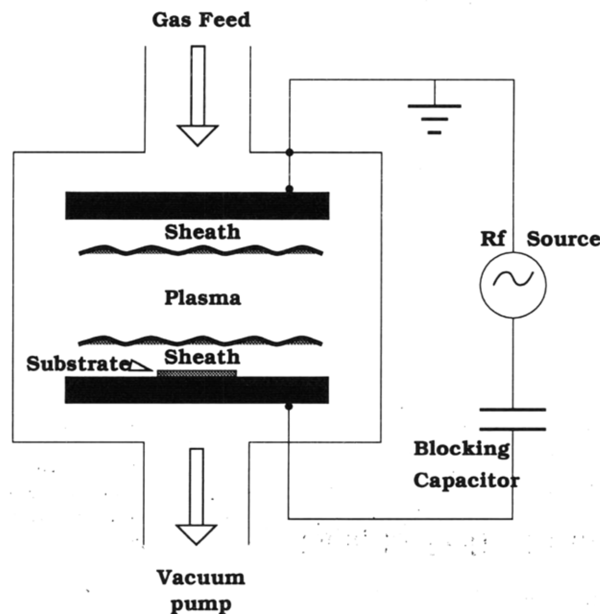

Figure 5.4: The conventional parallel plate reactive ion etching configuration.

stable plasma is spatially divided into the bulk plasma and the thin positive space charge regions called sheathes. The formation of the sheath is due to the fact that the electron flux towards the electrode is much larger than the ion flux for a given

plasma density. A thin positively charged space region must develop in the proximity of the electrode to repel the electrons back into the bulk plasma. While sheath keeps electrons in the bulk plasma region, it accelerates ions towards the electrodes once they enter the sheath. Thus one major energy loss in stable plasma systems is the energy loss for ions bombarding on the wall and the substrates across the sheath, which is determined by the sheath voltage. The higher the sheath voltage, the larger the energy loss. Neglecting other sources of loss, the overall discharge power balance can be written as:

$$P_{abs} = qn_s vAE. \tag{5.1}$$

where P_{abs} is the absorbed energy by the plasma, q is the electron charge, n_s is the ion density near the sheath which is related to the plasma density in the bulk region based on the given geometry of the chamber, v is the ion velocity which is often a constant, A is the chamber wall area, and E is the total energy loss per ion.

For the conventional RF powered RIE, the area A is usually the inner chamber surface area when it is grounded. The sheath voltage is several hundreds of volts and thus the energy loss E is large. For a given operating power, the plasma density is low.

Moreover, for the conventional parallel plate RIE configuration, ion flux and ion energy are coupled and can not be varied independently. The high sheath voltage causes substrate damage and loss of linewidth control. The low plasma densities ($10^9$to $10^{10}/\text{cm}^3$) result in low processing rates and low gas utilization.

Much of these limitations can be relaxed by using the plasma configuration displayed in Figure 5.5. The plasma is generated inside a dielectric vessel and flows out of the source into a material processing chamber. The microwave power is coupled to the plasma across a dielectric window, rather than by direct connection to an electrode immersed in the plasma [125]. The electrons are kept inside the chamber by

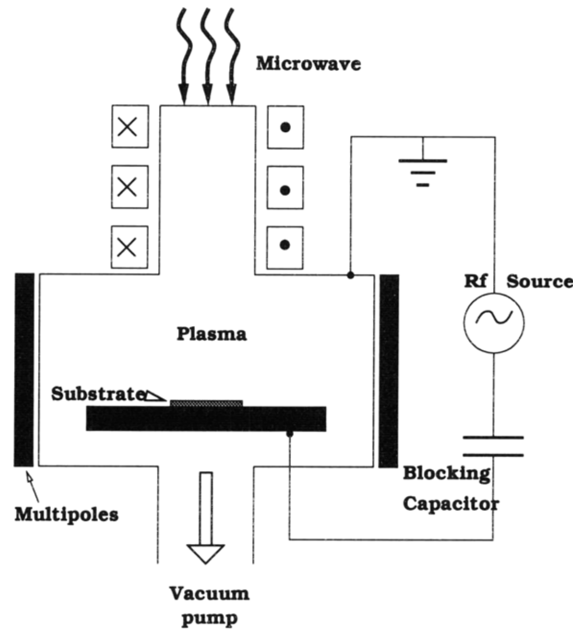

Figure 5.5: The Electron Cyclotron Resonance (ECR) enhanced Reactive ion Etching (RIE) Configuration.

the applied DC magnetic field B and the electron flux to the chamber wall is minimized. This in turn produces a much lower sheath voltage so that the energy loss due to ions bombarding onto the walls is much reduced. The reduced energy loss and somewhat reduced etching chamber area due to the confinement provided by the applied magnetic field results in higher ion density based on Equation 5.1.

By introducing the additional RF bias on the substrate, the ion flux and the ion energy onto the substrate can be varied independently. Furthermore, the ECR enhanced RIE can operate at lower pressure than the conventional parallel plate RIE. The improved anisotropy during the etching can be achieved from the reduced possibility of ion mutual collisions in the substrate sheath.

Finally, the typical ECR source offers a plasma density of $10^{11}$to $10^{12}/cm^3$ [126]. This implies faster processing rate. Most importantly, in the etching of InP, the higher ion density helps sputter the involatile indium chloride away from the surface so that

the fast steady etching can be achieved using chlorine chemistry without approaching higher temperature.

5.3.4 Fast Deep Etching of InP at Room Temperature

The Cl_2-based gas mixtures reported so far for etching InP are Cl_2/Ar, Cl_2/H_2, and Cl_2/N_2 [127, 124]. The Cl_2/Ar can provide fast etching but surface roughness is suspected to result from the high density energetic argon ions. Cl_2/H_2 and Cl_2/N_2 have reduced etch rate due to possible reaction between hydrogen/nitrigen atoms and chlorine, which reduces the available chlorine for the reaction with InP.

Cl_2/He is potentially the best gas mixture for this kind of etching. Helium is much lighter than argon and less energetic when bombarding onto the substrate surface in a down stream plasma configuration[4]; therefore, smoother surface morphology is expected. On the other hand, helium is very inert so that there is no possibility for helium to reduce the available chlorine density.

The availability of the helium gas in this thesis research was quite accidental.[5] Prior to the gas installation in the ECR-RIE system on campus, a user survey showed demand for helium rather than argon. The reason behind was mainly the wafer temperature control for dry etching of silicon-based material. By introducing helium from the backside of the wafers, the thermal conduction is enhanced and thus the surface of the wafer can be better cooled to sustain photoresist as the etch mask. Therefore, helium was chosen to be the only inert gas installed in the system without any concern about the fast etching of InP. It was only in this thesis work, the Cl_2/He chemistry was studied for InP dry etching for the first time.

The first batch of etch samples were first prepared using n-type InP substrate

[4]For conventional double plate plasma configuration, the lighter ions penetrates the substrates more and causes more damages [128].

[5]Joe Walsh, private communications.

coated with silicon dioxide. The silicon dioxide was then patterned into various size mesas to act as the etch mask. The etching is performed at 20~25°C, resulting 10μm deep pillar in five minutes with vertical sidewalls (Figure 5.6). The surface was rough because at that time the chlorine mass flow controller was having problems and the plasma was not as stable as expected. Even though the SiO_2 mask is strong

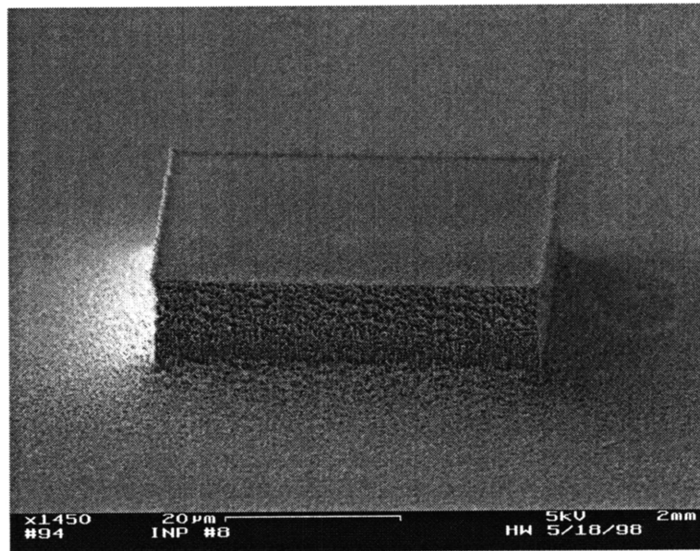

Figure 5.6: InP pillar etched in Cl_2/He chemistry with surface roughness.

enough for 20μm deep pillar etch, the ion bombardment left surface roughness on top of the pillar. This could be detrimental because good quality bonding requires well preserved smooth surface to prevent crevices and bumps which may hinder the bonding process.

A new mask was designed so that the photoresist used to etch the SiO_2 mask was left on during the deep etch. After the etching, the photoresist residual was liftoff by etching away the SiO_2 underneath, resulting mirror like top surface. Figure 5.7 shows the resulted 20 μm pillar with smooth surface on top of the mesa as well as at the bottom of the etched substrate.

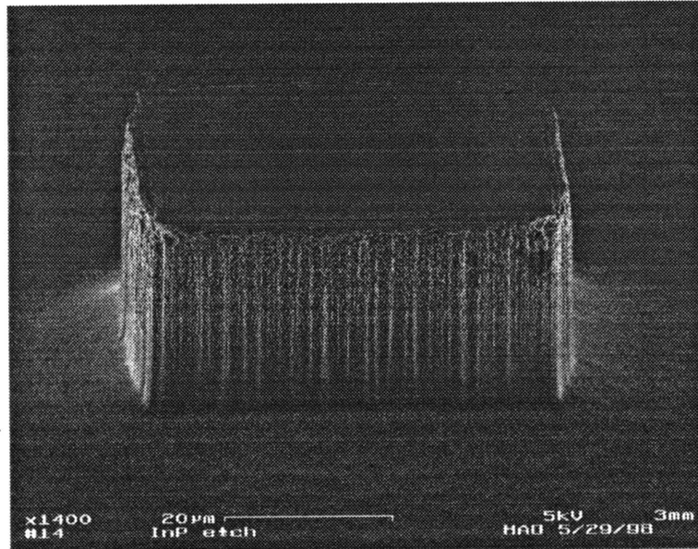

Figure 5.7: Deep InP pillar with smooth surface.

The etch rate was thoroughly calibrated versus the plasma parameters. Figure 5.8 shows the etch rate as a function of the ECR power. Increased ECR power generates a larger ion density; thus the processing rate is enhanced. Figure 5.9 displays the etch rate as a function of the independently tuned RF power. The RF power controls the energy of the ions. Higher energy plasma etchs InP at a faster rate. Figure 5.10 shows the etch rate as the function of the plasma pressure. Here the fastest etching occurs at low pressure because of the more sufficient removal of the etch products. Figure 5.11 displays the etch rate as a function of the percentage of chlorine in the gas mixture. The increase of the chlorine percentage in the gas mixture gives faster etching rate because more reaction agents are available.

The ECR RIE etching of InP was also demonstrated to be able to produce high aspect ratio features. Figure 5.12 shows the aspect ratio achieved of 10:1.

The etched surface roughness was calibrated using an atomic force microscopy (AFM) (Figure 5.13). The RMS roughness was estimated from 5 points on one

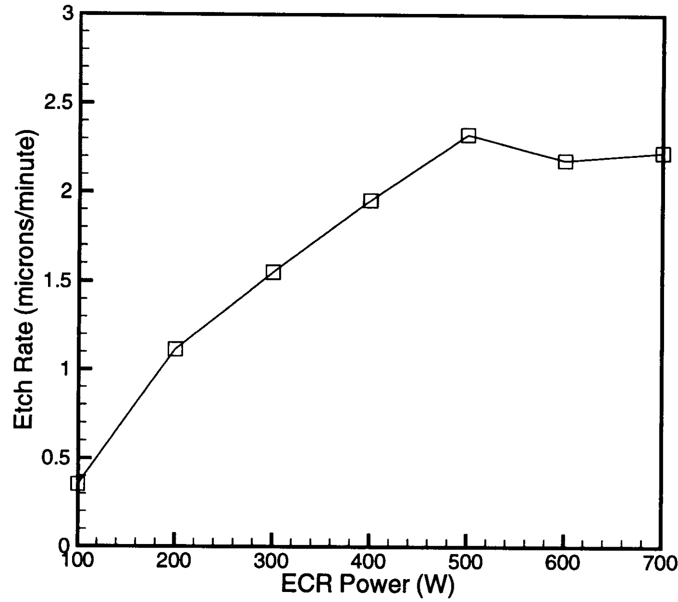

Figure 5.8: InP etch rate as a function of ECR Power. Etch parameters were: Cl_2 8sccm; He 12 sccm; pressure 5 mT; RF power 50W; etch duration 3 minutes.

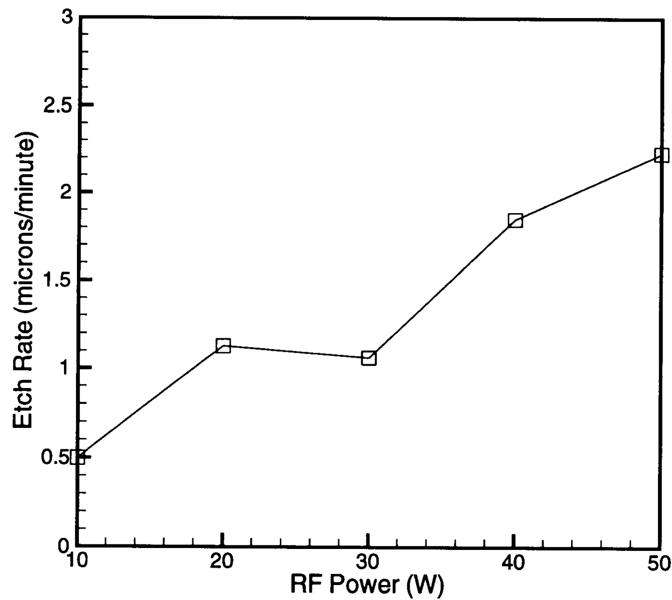

Figure 5.9: InP etch rate as a function of RF power. Etch parameters were: Cl_2 8sccm; He 12 sccm; pressure 5 mT; ECR power 700W; etch duration 3 minutes.

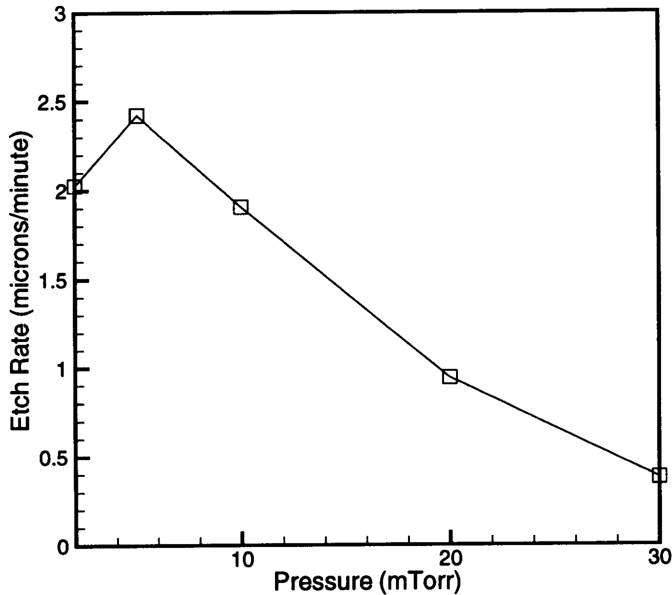

Figure 5.10: InP etch rate as a function of pressure. Etch parameters were: Cl_2 8sccm; He 12 sccm; RF power 50W; ECR power 700W; etch duration 3 minutes.

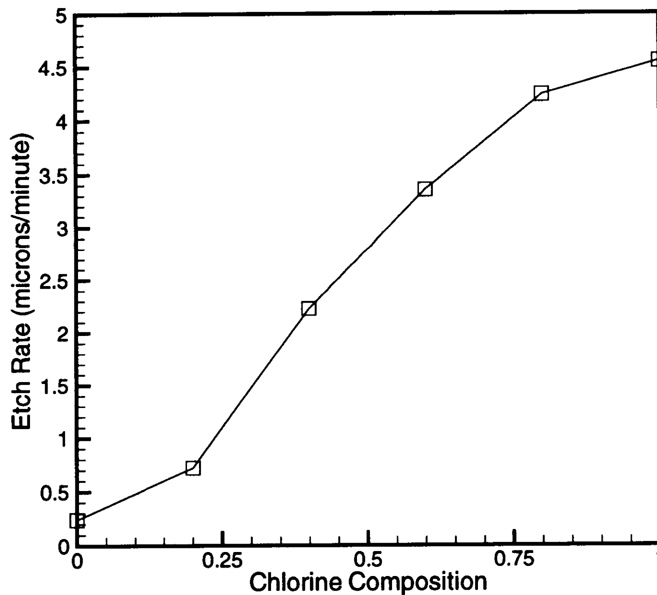

Figure 5.11: InP etch rate as a function of chlorine composition. Etch parameters were: total flow rate 20 sccm; pressure 5 mT; RF power 50W; ECR power 700W; etch duration 3 minutes.

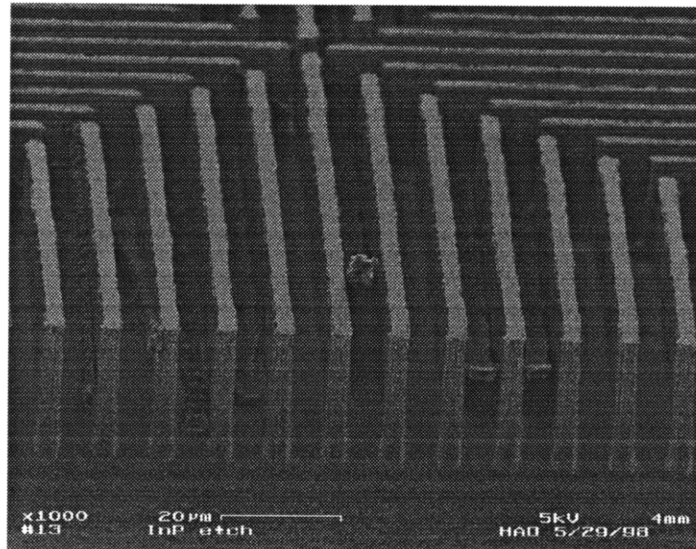

Figure 5.12: High aspect ratio InP dry etching demonstrated by Cl_2/He chemistry. Etch parameters are: Cl_2 8 sccm; He 12 sccm; pressure 5mT; ECR power 700W; and RF power 50W.

sample and shows the roughness is less than 2nm from all points.[6]

[6]The AFM work was performed by Minghao Qi of the Department of Electrical Engineering and Computer Science at MIT.

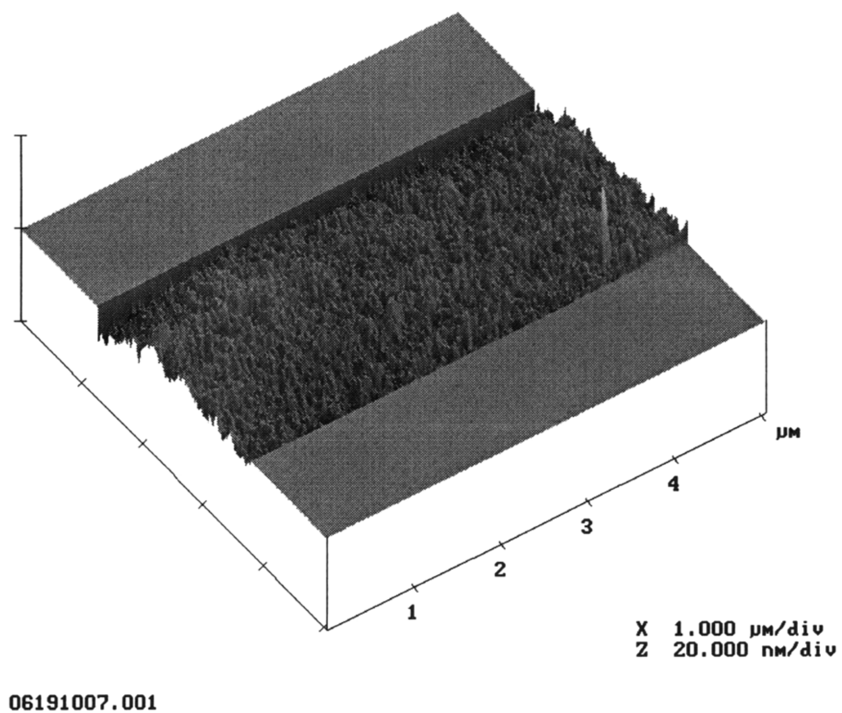

Figure 5.13: AFM image of the etched InP surface. The RMS roughness estimated from 5 points across the wafer were all under 2nm.

5.3.5 Fast Deep Etching of GaAs and Other III-V Semiconductors

Etch of GaAs is important for integrating optoelectronic devices grown on GaAs substrate, such as 850 vertical cavity surface emitting lasers (VCSELs). The detailed calibration of the etching characteristics is displayed in the following plots. The ECR enhanced RIE using the Cl_2/He chemistry is found to be capable of etching most common III-V semiconductors in a fast fashion. Palladium mask for the RIE was also investigated. The Pd mask is neither strong enough to sustain the 20μm etching nor smooth enough after the etching to be used as a bonding layer.

Additional Etching of GaP and InGaP has also been demonstrated, as shown in Figure 5.18 and Figure 5.19, with 2000Å Pd mask eroded after 5-minute etching.

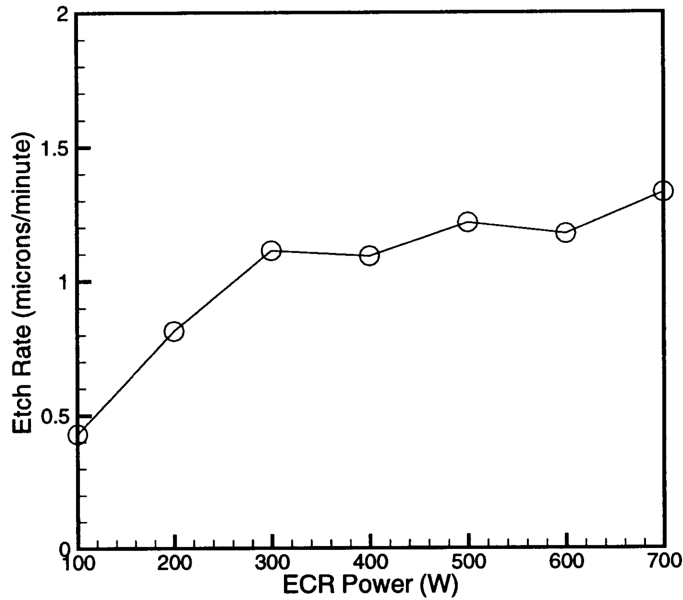

Figure 5.14: GaAs etch rate as a function of ECR Power. Etch parameters were: Cl_2 8sccm; He 12 sccm; pressure 5 mT; RF power 50W; etch duration 3 minutes.

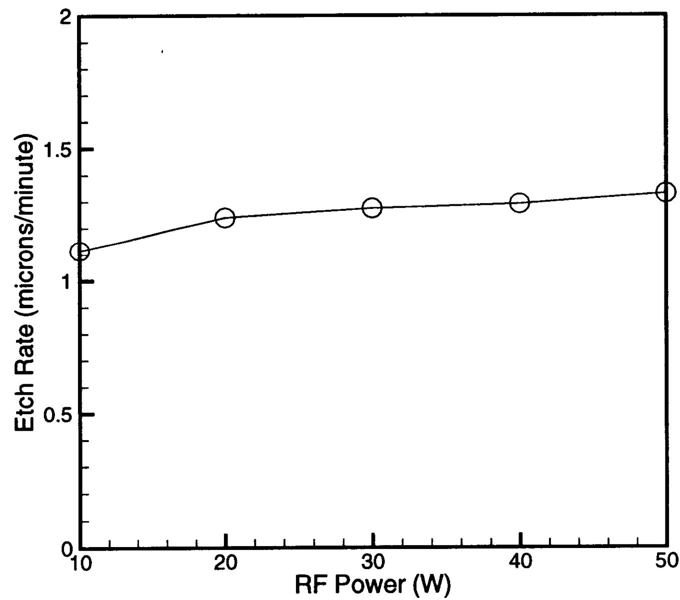

Figure 5.15: GaAs etch rate as a function of RF power. Etch parameters were: Cl_2 8sccm; He 12 sccm; pressure 5 mT; ECR power 700W; etch duration 3 minutes.

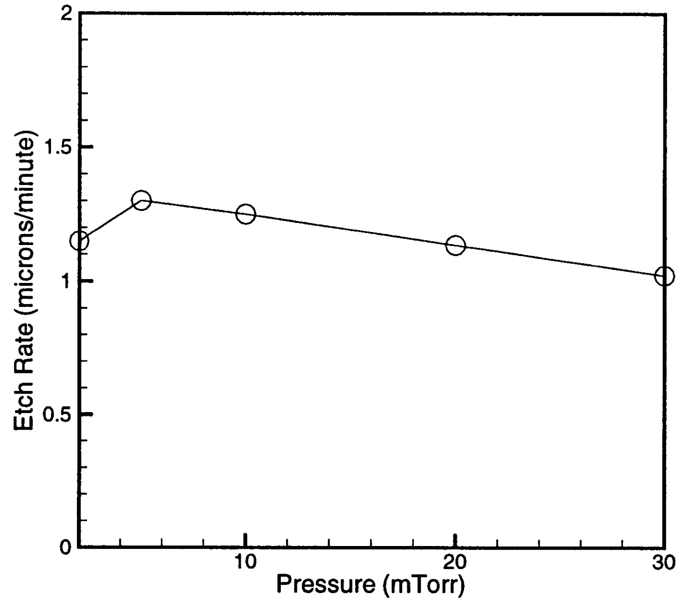

Figure 5.16: GaAs etch rate as a function of pressure. Etch parameters were: Cl_2 8sccm; He 12 sccm; ECR power 700W; RF power 50W; etch duration 3 minutes.

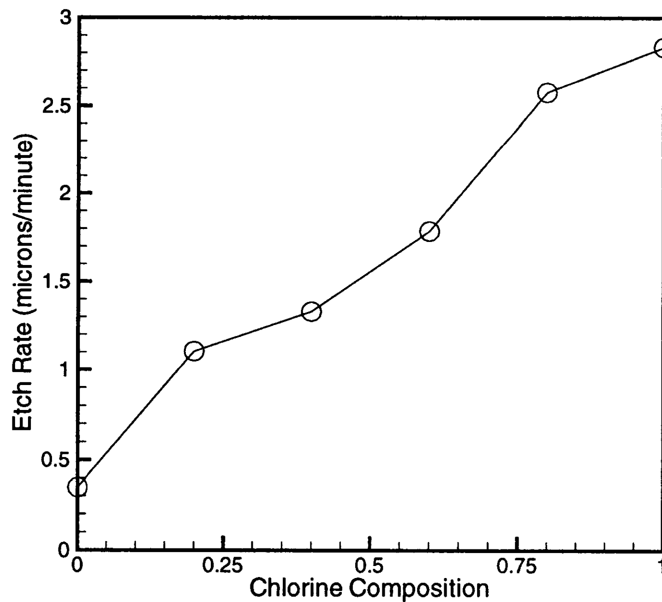

Figure 5.17: GaAs etch rate as a function of chlorine composition. Etch parameters were: total flow rate 20sccm; ECR power 700W; RF power 50W; etch duration 3 minutes.

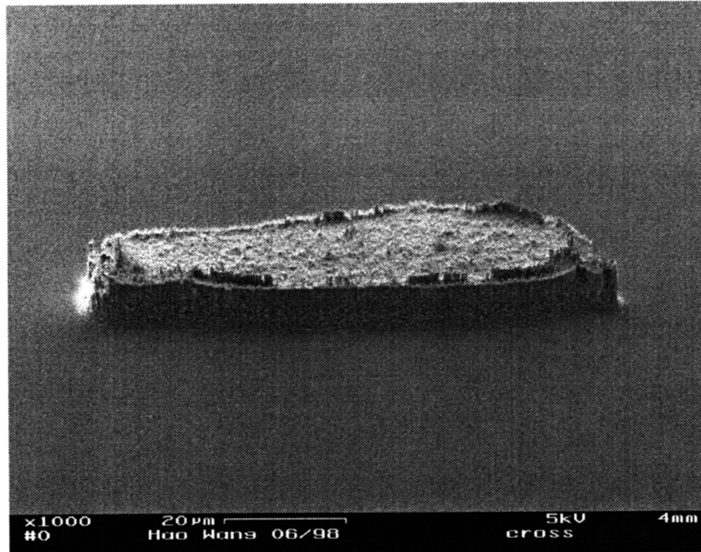

Figure 5.18: GaP etch by Cl_2/He chemistry. The palladium etch mask disappeared after 5 minutes etch under the conditions of: Cl_2 8sccm; He 12sccm; pressure 5mT; ECR 700W; RF 50W.

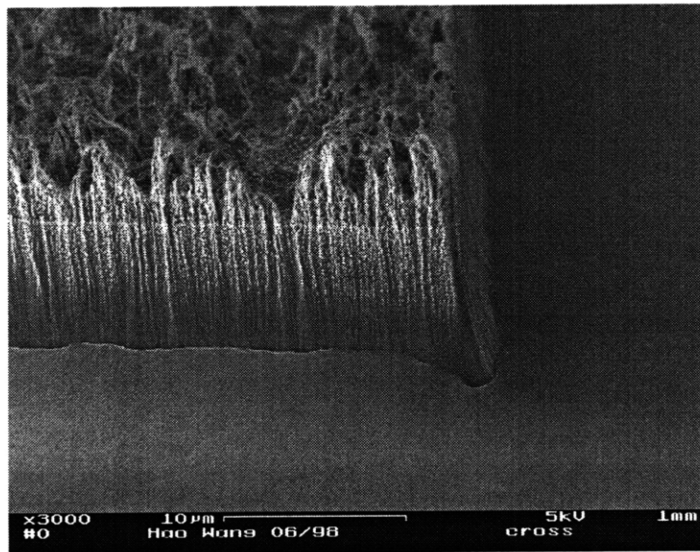

Figure 5.19: InGaP etch by Cl_2/He chemistry. The palladium etch mask disappeared after 5 minutes etch under the conditions of: Cl_2 8sccm; He 12sccm; pressure 5mT; ECR 700W; RF 50W.

5.4 1.55 μm Photodetectors Bonded on GaAs

The feasibility of the APB process also relies on the performance of InP-based photodetectors bonded on GaAs substrates. A inverted p-i-n structure was grown on the semi-insulating InP substrate with the n-side on the top as shown in Figure 5.20.[7] The sample was flipped over and bonded onto a PdGe-coated n-type GaAs substrate.

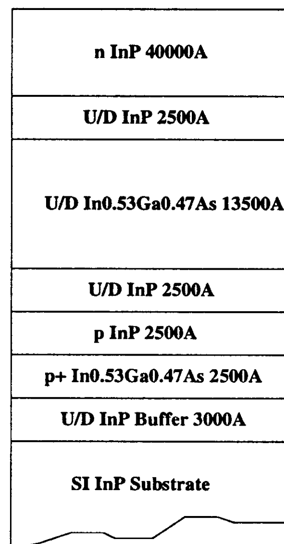

Figure 5.20: The structure of a p-i-n photodetector designed for bonding in the APB process.

The bonding was done in a hydrogen ambient at 350°C for 90 minutes. InP substrate was subsequently removed using wet etch which stops at the InGaAs etch stop layer. The resulted p-i-n structure of ~6.5μm thick is thus transferred onto GaAs substrate.

Standard fabrication procedure turns the bonded sample into photodetectors. ECR-RIE instead of the wet chemical etching was used for the mesa etch. The performance was evaluated in terms of the dark current and relative responsivity.

[7]This sample was grown by a commercial epitaxial wafer vendor.

As shown in Figure 5.21, the dark current is one order of magnitude lower than the best InGaAs detector grown on GaAs without utilizing sophisticated surface treatment. Using known wet chemical treatment [129, 130], the dark current of InP/InGaAs based p-i-n photodetectors can be significantly further reduced after the dry etching.

The responsivity (Figure 5.22) is more than 10 times higher than that of the direct grown detectors (Sample 9614) and it is about the same as that of the photodetector grown lattice-matched on the n-InP substrate(Sample 9610). The enhanced responsivity and the suppressed dark current promises better matched photodetectors for the OEIC integration.

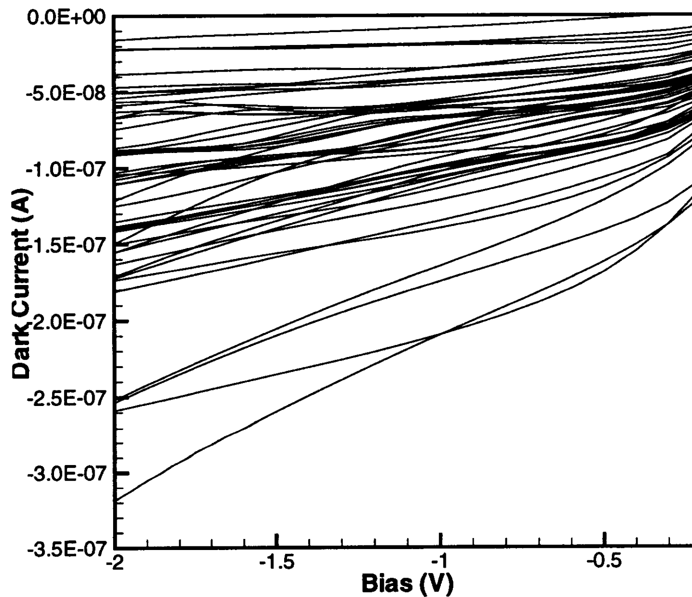

Figure 5.21: Dark current statistics for 1.55μm photodetector Sample EPIHao bonded onto GaAs, which is one order of magnitude lower than that of p-i-n photodiodes grown on GaAs. The dark current can be further reduced using known wet chemical treatment[129, 130].

The bonded photodetectors can also operate at reverse bias above 2 volts which

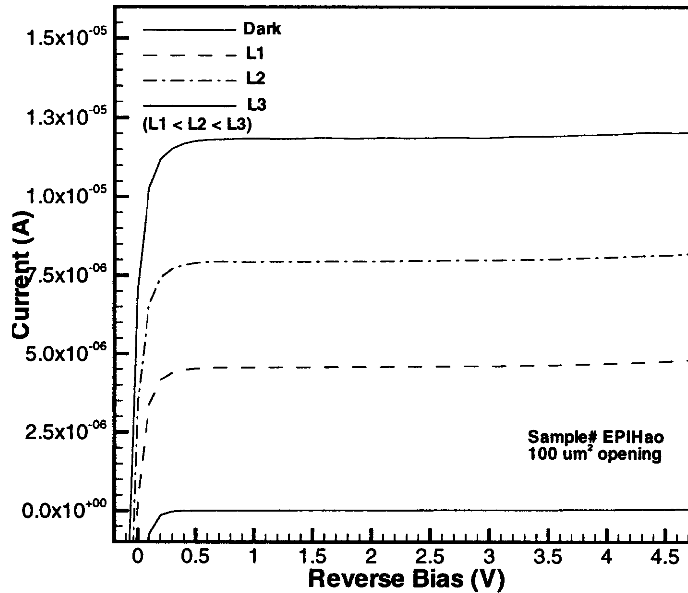

Figure 5.22: Photo response for the 1.55μm photodetector Sample EPIHao bonded onto GaAs, which is ten times higher than that of photodiodes grown on GaAs.

was not possible for the lattice-mismatched detectors grown on GaAs. Figure 5.23 shows that the breakdown voltages are 21V, 33V, and 37V for the detectors grown on GaAs, bonded on GaAs, and grown on InP, respectively. The details of the breakdown are shown in Figure 5.24, where the detectors grown on GaAs shows much softer breakdown due to the large leakage current density.

The Pd-bonded InP/InGaAs/InP p-i-n photodetectors shows devices characteristics superior to that of InAlAs/InGaAs/InAlAs p-i-n grown on the relaxed buffer on GaAs. The better uniformity for the bonded detectors shows promises for matched detector pairs needed for the OEIC integration.

As discussed in Chapter 3 and Chapter 4, it is still possible to improve the performance of directly grown devices by another order of magnitude if a slower grading rate is allowed. However, too thick a buffer layer not only requires lengthy growth, but also makes the post growth processing inconvenient. Furthermore, the detector

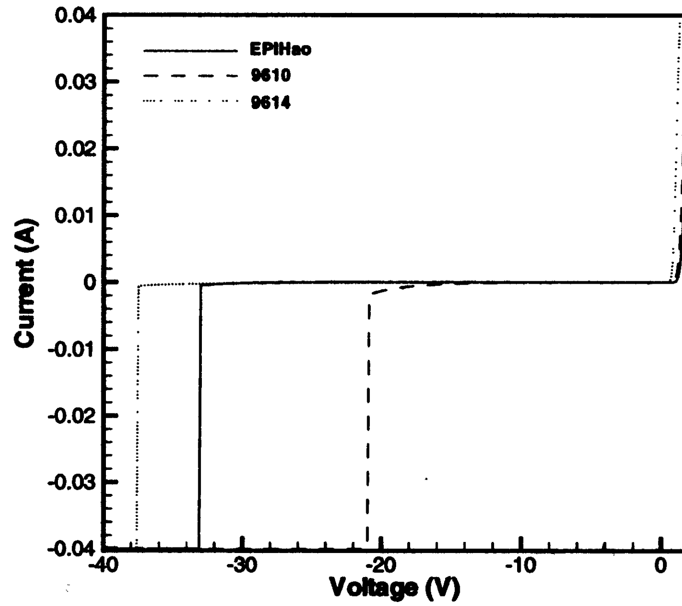

Figure 5.23: I-V characteristics showing the reverse breakdown voltage for three kinds of photodetectors.

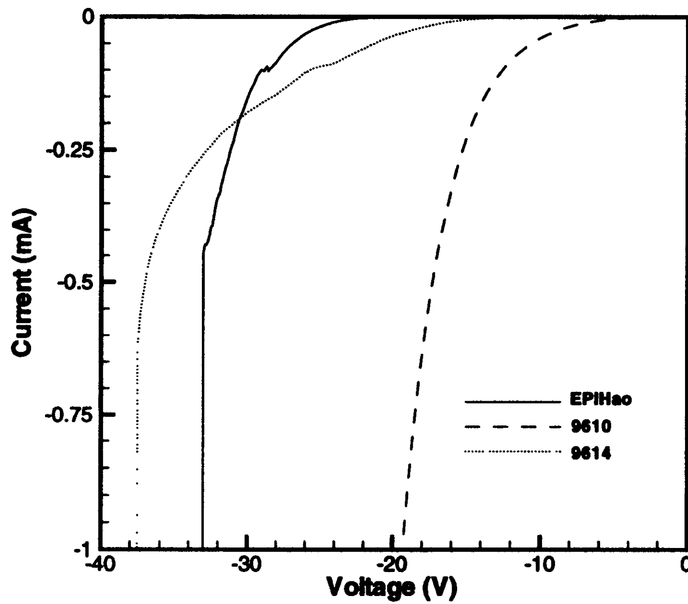

Figure 5.24: Comparison of the sharpness of the reverse breakdown.

performance on chip critically depends on the surface cleanness of the growth well, lacking confidence on the control over the material uniformity. With the improved detector performance and less stringent requirement of the surface cleaning, APB process seems to be a more attractive option for the OEIC integration.

5.5 Aligned Pillar Bonding on OEIC5 Chips

Finally, the feasibility of the aligned pillar bonding process depends heavily on the ability of transferring fabricated pillars into the wells on the chip.

The alignment is done using a IR aligner which can see through the substrate. Despite the fact that the IR optical resolution is more than a few microns, the pillar pattern and the bonding wells can be readily aligned within the design tolerance of $6\mu m$. This is shown in Figure 5.25 and the Figure 5.26 produced after a failed bonding. The impression of the top pillar surface is clearly seen at the bottom of the wells.

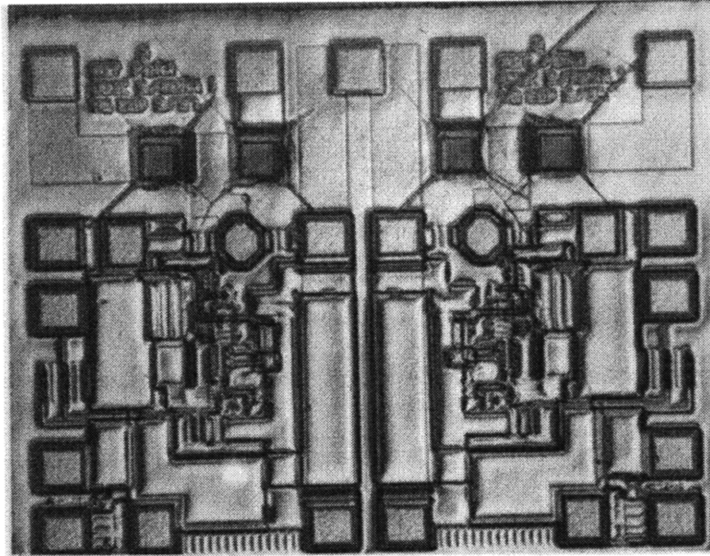

Figure 5.25: Proof of the alignment (1): the impression of the pillars at the bottom of the wells due to the mechanical and thermal compression.

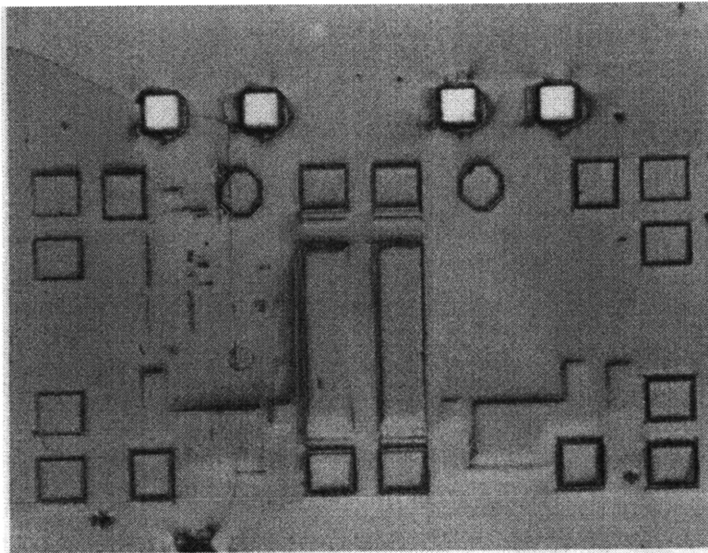

Figure 5.26: Proof of the alignment (2): the impression of the chip circuit onto the pillar wafer due to the mechanical and thermal compression.

In the current setup of the alignment-bonding equipment, the aligned samples have to be transferred into the graphite bonding fixture manually. Several screws have to be manually tightened afterwards to apply the pressure needed for bonding. These requires tremendous care to maintain the alignment of the samples. Nevertheless, a successful bonding was achieved. The bonding strength was high enough for the chip-pillar wafer pair to sustain several standard processing steps including two runs of photoresist spinning at 3000 rpm when applying the photoresist in the gap to protect the device structure from being attacked by the wet etching during the substrate removal.

After the substrate removal, the complete structure is transferred into the wells on the chip. The yield of the transfer is also high. Figure 5.27 shows a p-i-n structure transferred into the wells on the chip. The black surrounding area is the photoresist coverage obtained by the photoresist reflow in between the substrates and the pillar wafer. It is important to note also, the successful bonding/transferring of the smallest

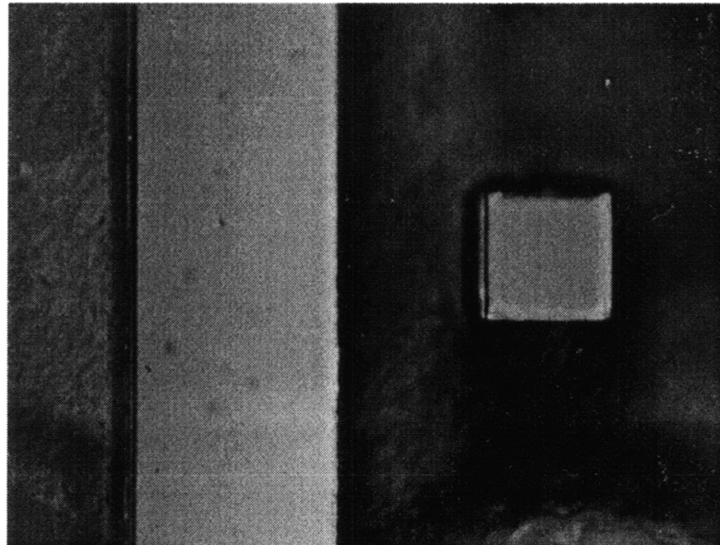

Figure 5.27: The materials bonded into the wells. After the substrate removal, surface preserved well.

pillar(13μm) into the smallest well(25μm) as shown in the Figure 5.28, indicates the

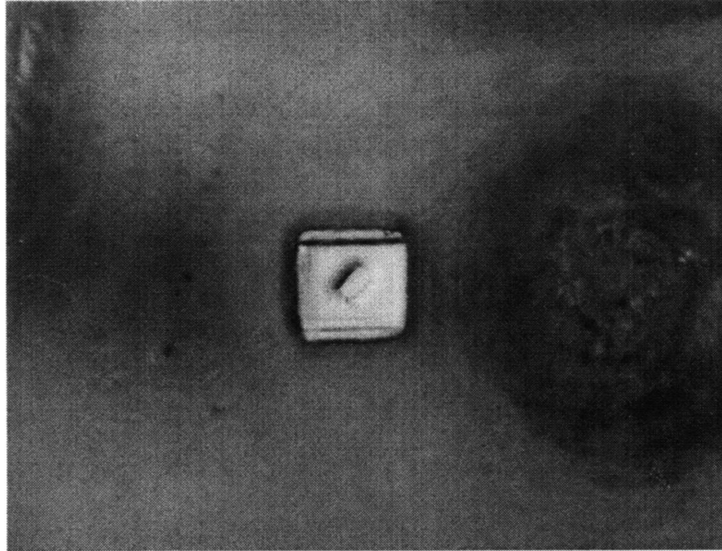

Figure 5.28: Smallest pillar (13μm square) has been bonded to the smallest well (25μm square).

aligned pillar bonding process is indeed suitable and feasible for high density OEIC integration.

The photoresist coverage for the protection of the device structure from the strong acid etching during substrate removal has already been shown in Figure 5.27. Additional proof in a larger scale is show in Figure 5.29.

Unfortunately, the transferred materials did not survive the later processing steps. The reason for this is most likely that the spinning process used in the photoresist reflow has loosen the bonding mechanically. The total area attached between two wafers is smaller than 2 mm^2. Spinning the substrate of more than 1 cm^2 size and more than 350μm thick generated large torque and shear stress on the tiny attached region, which is believed to destroy the bonding eventually.

In order to verify Pd-assisted pillar bonding across sufficient large wafer area, a separate experiment was conducted. InGaAs layer of more than 1 μm thick was

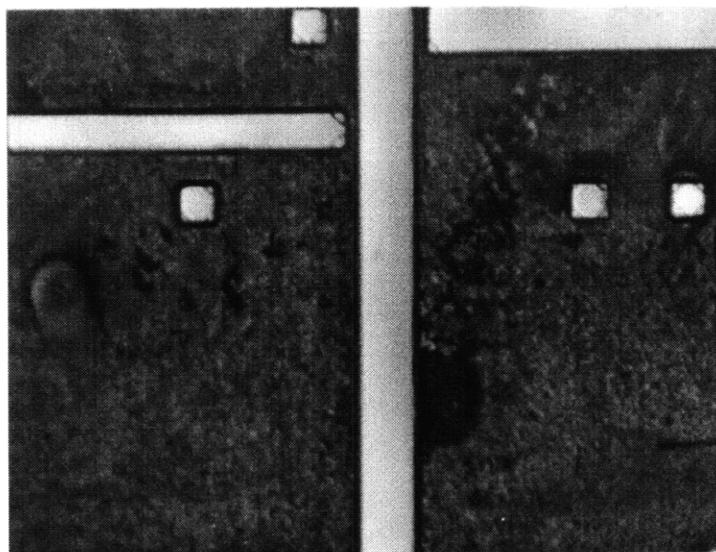

Figure 5.29: Proof of the pillar protection: the resist coverage on the chip after the resist reflow.

grown on lattice-matched InP substrate. Standard photolithography was used to pattern the InGaAs into various sizes of mesas and alignment marks. Sulfuric acid based wet etching turned the InGaAs layer into pillars of more than 1 μm in height. Then the photoresist was striped and thorough solvent cleaning was performed before the pillar wafer of 0.6 cm $\times$ 1.0 cm in size was put into contact with Pd-coated GaAs substrate. The bonding was completed at 350°C in hydrogen ambient for 90 minutes. The pressure used was several tens of MPa. After the bonding, the substrate was removed using HCl acid. The majority of hundreds of pillars were successfully bonded onto the GaAs substrate, including small alignment mark of 4μm linewidth and device mesa of 100 μm wide, as shown in Figure 5.30 and Figure 5.31.

The bonding integrity is also illustrated in Figure 5.32 where the SEM image shows the clean surface of the InGaAs layer and the well preserved mesa structure after the bonding and subsequent substrate removal.

In summary, the promises and feasibility of the aligned pillar bonding process

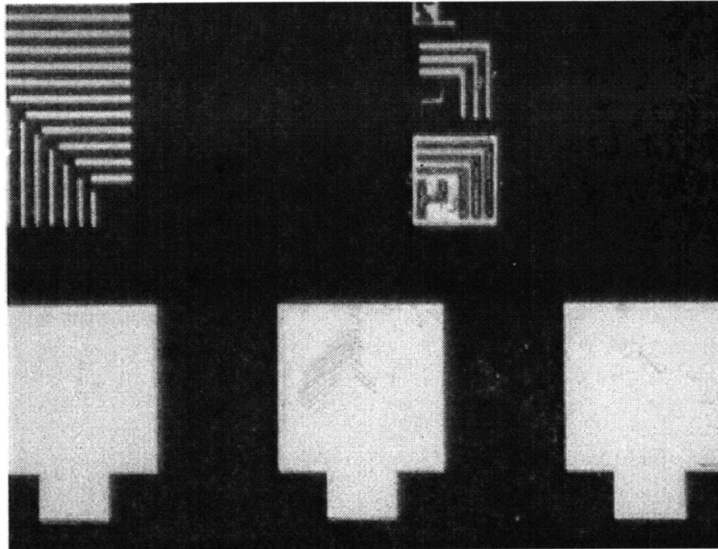

Figure 5.30: Proof of the Pd-assisted pillar bonding (1): InGaAs pillars of various sizes are bonded onto Pd-coated GaAs. The alignment marks are 2 $\sim$ 5 μm wide while the device mesas are 100 μm wide. The bright "white" regions are those pillars.

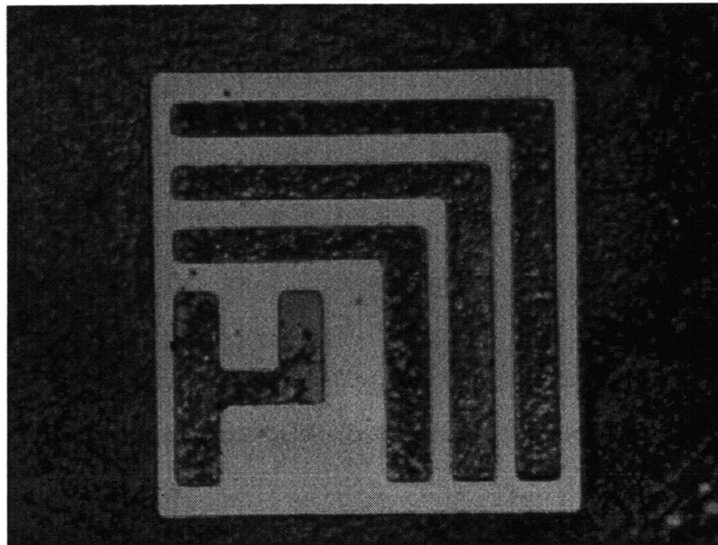

Figure 5.31: Proof of the Pd-assisted pillar bonding (2): The 4μm InGaAs alignment mark is transferred onto GaAs.

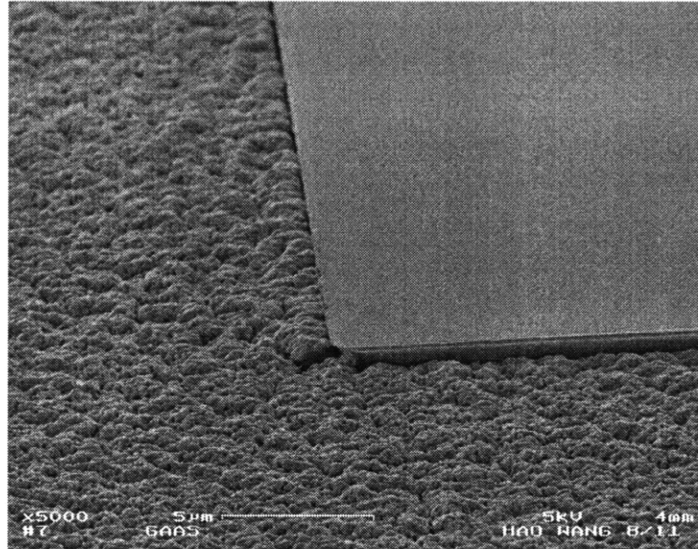

Figure 5.32: The SEM image of the InGaAs pillar bonded onto Pd-coated GaAs at 350°C. The surface roughness surrounding the pillar is due to the HCl eroding of Pd during the substrate removal.

have been illustrated from many aspects.

First, palladium-assisted reduced temperature bonding was studied. Palladium to palladium bonding at 350°C was demonstrated, which could potentially enable bonding of a variety of materials. For the first time, direct bonding of InP to GaAs at 450°C with high pressure (several tens of MPa) and long duration (90 minutes)achieved good Ohmic behavior .

A fast, deep, smooth, and highly anisotropic InP dry etching process at room temperature has been developed for the APB process. The Cl_2/He chemistry was systematically studied. The etching characteristics were calibrated for both InP and GaAs. Additional etching were also demonstrated for GaP, InGaP, AlAs, and InAlAs. The dry-etched surface was shown to be smooth, with an AFM RMS roughness of less than 2nm for InP etch.

High performance 1.55μm photodetectors were produced using palladium assisted reduced temperature bonding. The high responsivity, low dark current, and better uniformity enables better matched detector pairs needed for the OEIC integration.

While palladium was found not to be a durable etch mask, a multi-layer mask structure was developed using palladium, silicon dioxide, and standard photoresist, so as to preserve the top surface of the pillars for the subsequent wafer bonding. Using the dry etched, palladium coated pillar structures, initial pillar to well wafer bonding at the reduced temperature was studied. The backside alignment using long wavelength IR aligner was achieved within the 6μm design tolerance. Pillars as small as 13μm $\times$ 13μm was bonded and transferred into 25μm $\times$ 25μm wells.

Unfortunately, the materials transferred into the bonding wells on the OEIC chip did not survive the subsequent device processing due to possible damage by multiple runs of photoresist spinning. Additional study of the yield and integrity of the palladium assisted pillar bonding was conducted. Majority of hundreds of pillars across centimeter size wafer were bonded onto the palladium coated GaAs substrate. Smallest feature bonded and transferred was only a few microns wide. After the substrate removal, the pillars on their heterogeneous substrate show good integrity.

Though the final demonstration of the optoelectronic integration using APB process still awaits the more robust well-to-pillar bonding and successful device fabrication, the feasibility and promises of the APB have been revealed. The APB process can provide speedy path to integrate VLSI density optoelectronic devices with the inherited wealth of today's electronics development.

Chapter 6

Conclusions and Future Research

6.1 Accomplishments

The Epitaxy-on-Electronics (EoE) integration technique has been explored to integrate 1.55 μm photodetectors with GaAs VLSI electronics for high speed optical communication receivers. To overcome the shortcomings of the direct growth of the lattice-mismatched InGaAs detector structures on GaAs substrates, a novel process termed aligned pillar bonding (APB) has been proposed and partially developed. This thesis covered all phases of the development of the monolithic integration of the long-wavelength photodetectors with lattice mismatched GaAs substrates, including the design of photodetectors, the development of the lattice mismatched photodetectors grown on GaAs, the design and cleaning of MIT OEIC5/LL MORX1 chips, and the development of APB process.

The detector design phase of the work, Chapter 2, focused on three kinds of detector structures, namely, p-i-n photodetector, MSM photodetector, and uni-traveling carrier photodiode. Detailed design guidelines were presented for all three devices. By applying the bandgap engineering, a new design scheme called flatband uni-traveling

carrier photodetectors was derived with potential response faster than a few hundreds GHz.

The first experimental phase of the thesis, Chapter 3, concentrated on developing the MBE growth techniques for the 1.55μm p-i-n photodetectors on GaAs substrates. Graded short-period superlattice buffer and linearly graded buffer were compared, which led to the conclusion that the linearly graded buffer results in lower threading dislocation density, lower leakage current, and higher responsivity. A slower grading rate was found to be advantageous. The device leakage current density increases exponentially with the grading rate, revealing the possible exponential dependence of the threading dislocation density on the grading rate. Devices grown on lattice matched InP substrates were also fabricated, serving as the benchmark for the evaluation of the mismatched growth of long wavelength photodetectors. It was concluded that even though working 1.55μm photodetectors can be made via direct epitaxial growth on GaAs, the performance is limited and inferior to that on InP. The detectors were grown on GaAs under the restricted growth window set by the Epitaxy-on-Electronics technology, with growth temperature below 470°C and grading rate faster than 10 %In/μm, therefore, further improvement of the device performance is also restricted. Furthermore, the inferior device uniformity of the devices undermines the feasibility of integrate matched detector pairs for the balanced high bit rate optical communications.

The second experimental phase of the thesis, Chapter 4, was devoted to the design of the dedicated OEIC chip termed MIT OEIC5/LL MORX1. Utilizing the transimpedance amplifier design donated by Robert Deming of Vitesse Semiconductor, several high speed optical receiver modules were designed, consisting of the dual balanced optical receivers and the polarization diversity receivers. The OEIC chips were fabricated by a commercial foundry and the resulting modified transimpedance

amplifiers exhibited satisfactory performance. A new chip cleaning procedure was developed, targeting at the linewidth control of dielectric growth wells , minimal plasma damage and micro-contamination, and bondpad and substrate protection. MBE growth on chips was performed after the installation of a hydrogen thermal cracker allowing reduced temperature oxide removal. The material characterization shows the non-uniformity of the materials in adjacent growth wells.

The rather time-consuming and delicate surface cleaning process and the material uniformity issues existed for lattice-mismatched Epitaxial-on-Electronics integration technology may limit both of its performance and manufacturability for the long wavelength optical communication components utilizing GaAs electronics. An alternative process is thus introduced as aligned pillar bonding (APB) in the third experimental phase of the thesis, with its findings summarized in Chapter 5.

Instead of growing lattice mismatched materials directly onto the GaAs electronics with restricted growth window, in the APB process, the optoelectronic device structures are allowed to be optimized on their lattice matched substrates under the optimal growth conditions. The independently optimized electronics and optoelectronic devices are integrated via reduced temperature bonding. Palladium-assisted bonding was explored and demonstrated. Utilizing high pressure bonding techniques, the direct bonding of InP onto GaAs was also demonstrated at 450°C with good Ohmic behavior across the interface. Palladium to palladium metal bonding is also demonstrated in this thesis, with important implication for the applications of APB in a broader range.

During the development of the APB process, electron cyclotron resonance enhanced RIE using Cl_2/He chemistry was developed and calibrated for both InP and GaAs. The resulted fast, deep, anisotropic, smooth dry etching at room temperature makes the APB process feasible and manufacturable. High performance 1.55 μm pho-

todetectors have been produced on GaAs substrate using the Pd-assisted bonding, demonstrating good uniformity and two orders of magnitude higher signal-to-noise ratio than those grown directly on GaAs.

Aligned pillar bonding on the OEIC5/MORX1 chip was performed. Pillars with various sizes were transferred into the bonding wells on the OEIC chip. Separate pillar bonding experiment has shown the capability of bonding InGaAs features with sizes from 2μm to a few hundreds of microns onto GaAs substrates.

APB process builds upon the wealth of the electronics industry. It is compatible with the mainframe silicon electronics as well as high-speed GaAs electronics. APB allows independent optimization of both electronics and photonics. Furthermore, it presents potentially low parasitics, high performance, high complexity, and natural compatibility with the large scale manufacturing.

6.2 Possible Directions for Future Research

The immediate step in the continuing research is to fabricate the optoelectronics devices on chip using the APB process. The OEIC fabrication technology developed in the Epitaxial-on-Electronics can be easily modified and transferred to the APB.

Putting the Best of Everything Together

The APB process is developed for the integration of 1.55 μm photodetectors with GaAs electronics. However, it is compatible with a variety of optoelectronics devices and electronic fabrication processes.

The main attraction would be to integrate emitters onto the electronics using APB process. One of the most motivated devices is the vertical surface emitting laser (VCSEL) built on GaAs substrates. The discrete device fabrication is maturing for 850/980nm VCSELS while the smooth deep pillar etching has been steadily available

as shown in Figure 6.1. Since the electronics and photonics are sharing the same

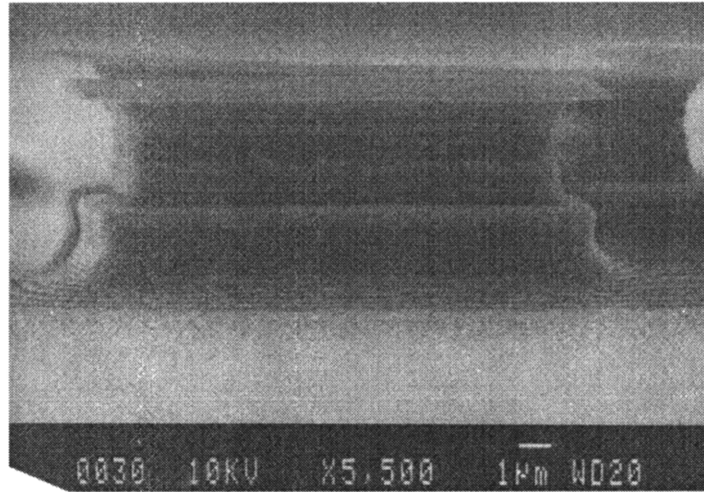

Figure 6.1: Chlorine based RIE etch of a vertical cavity surface emitting laser structure. The etching was performed by Hao Wang in 1994 at the University of Michigan.

GaAs substrate, the elevated bonding temperature would not degrade the alignment achieved at room temperature, thus high density OEICs are immediately feasible.

To impact the commercial market of the optoelectronics, integration of the photonics devices with silicon electronics is desired. With the demonstrated metal-to-metal bonding at the reduced temperature in this thesis, palladium assisted bonding can be simply applied to the silicon based optoelectronics for a variety of emitters, detectors, and modulators.

Materials Issues for Aligned Pillar Bonding

The optimization of APB process itself addresses several material issues.

(1) **Deeply Reduced Temperature Bonding**. The thermal expansion coefficient mismatch existed between many important materials requires the lowest possible temperature. Pursuit of the deeply reduced temperature bonding, ideally at room

temperature, is thus desired. Alloy rather than elemental metal can be used. Pd-Ag alloy can be tailored to lower both the bonding temperature and the manufacturing cost.[1]

In-Ga alloy is another candidate, which can be Ohmic contact to both n-type and p-type GaAs and Si. The low melting point of gallium also permits room temperature bonding.

(2) **Study of Bonding Pressure and the Induced Defects**. The bonding pressure used in this thesis is not fully studied yet, let alone optimized. It is believed that the bonding strength is a function of the pressure applied. How to achieve the sufficient high bonding strength and electrical conductivity at the lowest possible pressure to minimize the chances of introducing defects in the materials becomes an issue.

(3) **Study of the Electrical Contact by Bonding**. Although some estimation of the contact resistance is given in this thesis and in other literature, accurate measurement of the contact resistance is desired. To be specific, contact resistance as a function of the bonding temperature and applied pressure needs to be characterized. In order to improve the electrical conductivity, some palladium alloy such as palladium-gemanium may be beneficial since the PdGe has been demonstrated to be good Ohmic contact to both GaAs and InP.

To summarize, there is still a tremendous amount of further development to demonstrate that high quality OEICs for a variety of applications can be massively produced using APB process. While demonstrating devices including both the emitters and detectors has high priority, the fine tuning of the APB process needs to be investigated as well. Applying the APB technology to silicon-based optoelectronics is expected to ultimately endorse the APB as a large scale manufacturable technology.

[1]Professor Vander Sande, private communicaitons.

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