XI. PROCESSING AND TRANSMISSION OF INFORMATION

Prof. S. C. Caldwell	W. G. Breckenridge	A. J. Osborne
Prof. P. Elias	J. Capon	J. C. Stoddard
Prof. R. M. Fano	E. Ferretti	S. H. Unger
Prof. D. A. Huffman	E. J. McCluskey, Jr.	W. A. Youngblood

RESEARCH OBJECTIVES

In the Quarterly Progress Report of January 15, 1954, R. M. Fano gave an introductory discussion of the two kinds of problems that arise in applying information theory. The first is the determination of the amount of information generated by a message source, such as a speaker or a television camera. The second is the representation of a message in the best form for economical transmission over an imperfect channel.

In connection with problems of the first kind, work on speech and picture compression was discussed. These programs are nearing the end of the first phase of equipment construction. During the coming year descriptions of equipment, calibration procedures, and preliminary measurements will be reported as progress is made.

Work on problems of the second kind is also continuing. This work is centered on the simplest noisy channel: a binary channel that transmits zeros or ones and has the probability p_o of transmitting any digit incorrectly. The channel is so simple that it is possible to compute answers to a variety of detailed questions about error-correcting codes designed for it. It is also possible to build coders and decoders out of relays and trigger-pairs. This means that such codes can be tested, and some preliminary construction of apparatus for this purpose is under way.

Since information is a measurable quantity it can be considered somewhat analogous to energy (1). For example, certain switching circuits realized by means of delay lines and adders have this property: they may alternately store and give up the information supplied to them in the form of a sequence of binary digits in the same way that networks with inductive and capacitive elements store and give up the energy supplied to them in the form of time "sequences" of voltage and current. If certain restrictions are met, such information filters may be "lossless"; the analogous electrical-energy filters would be termed "reactive."

An intensive study of the properties and possible syntheses of information-filters was undertaken in the belief that proper internal feedback within such filters may stabilize them against the effects of component failure and external noise. From the viewpoint discussed above, the problem of obtaining error-free information from a noisy communication channel can be related to the problem of designing a feedback network which is lossless for the transmitted signal but lossy for external disturbances. Some details of the work mentioned above will soon appear as a technical report.

A practical realization of information filters might be in terms of sequential switching circuits. Switching theory is also developing useful techniques for the treatment of indefinitely extended sequences of binary variables. Therefore, steps have been taken to insure close cooperation among people with interests in both information theory and switching theory.

P. Elias, D. A. Huffman

A. THE SYNTHESIS OF ITERATIVE SWITCHING CIRCUITS

One of the properties of an iterative, or "positional," switching circuit is that its ability to transmit may, in general, depend upon a large number of binary switching variables. For example, the extended relay-contact network shown in Fig. XI-1 transmits a ground to the output terminal if and only if the number of operated relays in the

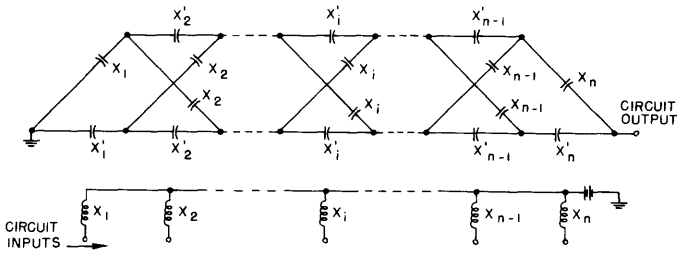

Fig. XI-1
An "even" circuit.

circuit is even. (Unprimed contacts are normally closed; primed contacts are normally open.) It is clear what the fundamental structure of a typical cell of this network is, and this structure (as in all iterative networks) remains the same throughout the network even if the number of variables is large.

In the synthesis of iterative switching networks (2) it has been difficult to be certain that the specification of terminal requirements is exact. One conceivable (and accurate) way to describe the transmission of a network with n binary variables would be to list an output of either one or zero (ground or no ground for a contact network) for each of the 2^n possible input states in a table of combinations (truth table). Clearly this table would become excessively large for relatively small values of n. (For example, $2^{10} = 1024$.)

What is needed is a method of specification that becomes complex only if the structure of a typical cell in the network is complex, and from which the typical cell itself may be synthesized directly.

The synthesis method proposed here satisfies these requirements and is based upon the fact that the variables in an iterative circuit are ordered from left to right, just as the input to a sequential switching circuit is a sequence of digits ordered from the past to the future. Therefore, an iterative circuit can be considered a sequential circuit with the variables ordered in space rather than in time. And we should be able to describe an iterative circuit by means of a flow table (3).

As an example we shall synthesize a contact network that transmits a ground if and only if at least two of the relay variables are equal to unity. A typical cell in such a network must "know," by means of the grounds on its input leads, how many variables to its left have the value unity and must transmit this knowledge – modified according to its own binary value – to the right (to the next cell).

Only three classifications of data need be distinguished by such a cell. Either

1. no variables to the left have the value one, or
2. one variable to the left has the value one, or
3. two or more variables to the left have the value one.

These three mutually exclusive states have been assigned the state-designators, "0," "1," and "2," respectively, and are associated with the three rows of the flow table in Fig. XI-2(a). The two columns of the table correspond to $X_i = 0$ and $X_i = 1$.

The six entries within the flow table itself specify the way in which the state of the circuit is modified when the value of the variable within a new typical cell is considered. For example, the entry "2" in the row associated with state "1" (the middle row) and with $X_i = 1$ (the right-hand column) is interpreted as follows: If to the left of a typical cell there is just one variable with the value unity, and if the value of the variable in the cell is also unity, then the data to be sent on to the next cell to the right are that two variables have the value one.

The output data in Fig. XI-2(a) tell whether or not the circuit should transmit a ground when the contact network is terminated just to the right of the typical cell under consideration.

The knowledge about the circuit state which is given to a typical cell is coded as a set of grounds on one or more input leads to the cell. The knowledge given to the next cell to the right is coded in exactly the same way. In our present example (and also in Fig. XI-1) two leads are sufficient. They correspond to states "1" and "2." That is, the state "0" is associated with no grounds on the cell leads; the state "1," with a ground on the first lead; the state "2," with a ground on the second lead.

Now the data in the flow table must be used to show how to connect the contacts within a typical cell (see Fig. XI-2(b)). The bottom pair of "2" entries in the flow table tells us that if the second input lead is grounded, the second output lead is to be grounded, regardless of whether $X_i = 0$ or $X_i = 1$. Thus the second input lead is tied directly to the second output lead.

The entry "2" in the middle row of the flow table instructs us to ground the second output terminal if the first input lead is grounded and if $X_i = 1$. The diagonal X_i contact in the typical cell accomplishes this.

The entry "1" in the top row tells us that when neither input lead is grounded and when $X_i = 1$, the first output lead should be grounded. The proper result is obtained by means of the X_i contact, which has one terminal connected to ground. The other entry "1" (in the $X_i = 0$ column) corresponds to the X_i' contact.

When an indefinite number of typical cells is connected in cascade (Fig. XI-3), it is found that two of the contacts in both the left-hand and right-hand cells are superfluous. All that we need do to complete the synthesis is to take the circuit output from the second output terminal of the last cell. The resultant contact network transmits a ground if and only if there are two or more operated relays in the circuit.

Because the flow table specification of an iterative circuit synthesis problem does not mention the physical nature of the binary variables, it holds, also, for example, for an electronic realization. A typical cell for one possible analogous vacuum-tube circuit

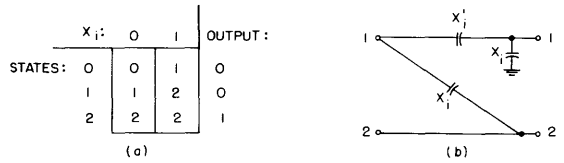

Fig. XI-2

The flow table and typical cell for an illustrative iterative circuit.

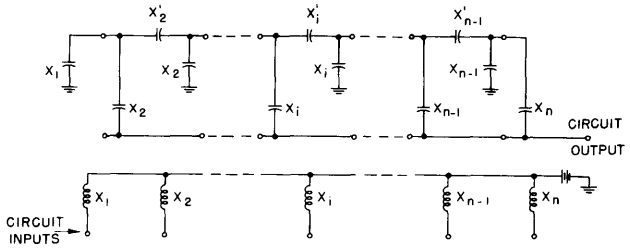

Fig. XI-3

The derived relay circuit.

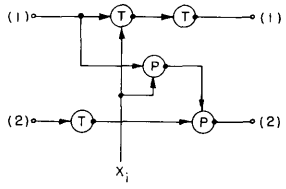

Fig. XI-4

The typical cell of an analogous vacuum-tube circuit.

is shown in Fig. XI-4. For this circuit, X_i has the value one or zero, depending on whether the input voltage X_i is high or low. The symbol T refers to a triode or to two triodes in parallel with a common plate-load resistor, and the symbol P to a pentode.

We indicated that the flow table is an implement in the synthesis of a wide variety of switching circuits; its use is valid whether the variables be ordered in space or in time. The complexity of the description for an iterative circuit does not depend upon the number of variables any more than the complexity of description for the synchronous sequential circuit depends upon the length of time it is allowed to operate. Finally, the methods that have already been developed for the simplification and manipulation of flow tables (3) have been shown to have a double usefulness.

D. A. Huffman

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2. W. Keister, A. Ritchie, and S. Washburn, The Design of Switching Circuits (D. Van Nostrand Company, Inc., New York, 1951), pp. 56-58.
3. D. A. Huffman, Technical Report 274, Research Laboratory of Electronics, M.I.T., Jan. 10, 1954.

B. SEQUENTIAL SWITCHING SYSTEMS WITH CLOSED MEMORY

1. Introduction

Before discussing this problem it is necessary to define some of the basic concepts of switching circuit theory.

Consider a switching system with several input and output terminals. Each terminal has associated with it a binary (two-valued) variable which may be physically represented by the presence or absence of a conduction path to ground, the presence or absence of a voltage pulse, one of two voltage levels, and so on. The possible states of these variables are generally designated as either 0 or 1.

The input state applied to a system is defined as the combination of values of the binary variables at the input terminals. The output state produced by the system is similarly related to the output terminals. (The terms system input or system output will occasionally be used.)

A switching circuit is referred to as "combinational" if the output state at any time is uniquely determined by the existing input state. (Ideally, no delay is involved.) Detailed studies of the principles of combinational switching circuits will be found in references 1 and 2.

A sequential switching circuit is characterized by the fact that its present output

state is, in general, a function of both the present input and the past inputs. This fact necessitates the use of a memory (usually composed of 2-state elements) whose function it is to provide information concerning previous input states. The memory state of a system is the condition of all its memory elements. (A memory composed of m binary elements can be in any one of 2^m states.)

For simplicity, the following discussion is restricted to synchronous, or clocked, systems where all inputs, outputs, and other actions occur in cadence with a sequence of reference pulses. This restriction is not of fundamental importance, since asynchronous systems can be treated in a similar manner.

Figure XI-5 depicts the signal flow in a synchronous sequential switching circuit. It is a functional diagram; the various parts do not correspond to physical entities.

The operation of the system described by the diagram is as follows. When a clock pulse arrives, the combinational circuit accepts at its input terminals the system input and the memory state. Some of its output terminals provide the system output; others lead to the memory input and specify the new memory state, which can be selected arbitrarily. Since there is a delay associated with the memory input, the memory state cannot change while the clock pulse is on.

A thorough general treatment of sequential switching circuits was presented by D. A. Huffman (3). One of the principal results of his paper is the flow table, a compact method of specifying, completely, any sequential problem. A companion result is a direct, though not unique, method for synthesizing a sequential circuit from any flow table.

2. Open and Closed Memories

The memories considered specifically by Huffman have the property that the states of all of their elements can be displayed simultaneously to a combinational circuit; furthermore, the states of any number of elements can be altered at one time. These characteristics make possible the two flow lines in Fig. XI-5 which connect the combinational circuit with the memory. Such memories will be designated as "open," since their states are at all times fully open to inspection and control by a combinational circuit. Open memories can be constructed with relays, vacuum tubes, transistors, or other devices.

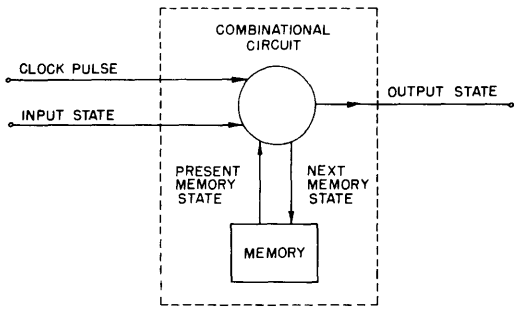

Fig. XI-5

Flow diagram of a synchronous sequential switching circuit.

There are also memories without the feature described above. That is, at any particular instant, the states of only a limited number of elements, or cells, can be made known to

the combinational circuit. In addition, the states of only a limited number of elements can be altered during any one time interval. Such memories, which include electrostatic storage tubes and magnetic core matrices, will be referred to as "closed," to indicate that at any particular time most of their elements are closed to inspection or control. This discussion will be limited to those memories in which, at each instant (excluding transient intervals) a single cell is being "scanned," and only the state of this cell can be determined or changed.

The terms "reading" and "writing" are used to indicate the operations of inspecting or changing, respectively, the contents of a cell.

There are at least two general ways in which closed memories can be, and are being, used. First, they may serve simply as data storage units. Binary coded sequences may be written into the cells, and then, at a later time, portions may be read out into smaller open memories so that they can serve as inputs to combinational circuits. Although this is a very important function, it is of little significance from the point of view of this study. The second, and more interesting, use of closed memories is in sequential switching circuits, where they can sometimes serve as replacements for open-memory elements.

It can be seen from the preceding definitions that closed memories are less flexible than open memories. However, considerations of such matters as size and cost militate against the exclusive use of open memories when a large memory (say thousands of elements) is required.

3. A Synchronous Sequential Switching System with Closed Memory

Consider the system described by Fig. XI-6. The number of states of the open memory is equal to the number of elements of the closed memory. The selector, which is controlled by the open memory, is a combinational circuit that selects the cell to be

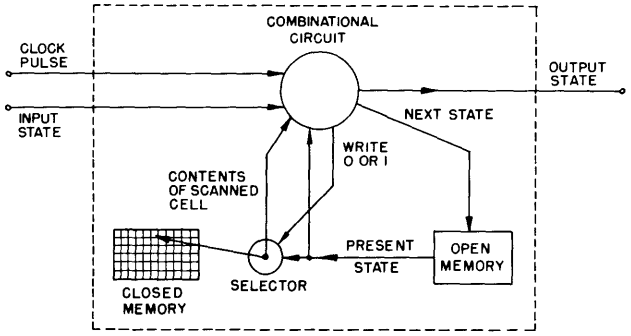

Fig. XI-6

Synchronous sequential switching system with closed memory.

scanned. For each state of the open memory there is one element of the closed memory.

When a clock pulse arrives, the combinational circuit inspects the system input state, the open memory state, and the state of the scanned cell. On the basis of this information, it fixes the system output, orders a one or a zero to be written in the scanned cell, and specifies the next open memory state (which is equivalent to choosing the next closed element to be scanned). A delay inherent in the open memory prevents its output from changing before the writing operation is over.

Note that the system has an over-all memory of $m2^m$ states, where m is the number of closed cells. (The closed memory has 2^m states, and at any time any one of the m cells may be scanned.)

Since the identity of the cell to be scanned during a time interval is dependent upon the output of the combinational circuit during the previous interval, a time translation is necessary, thus requiring the use of the open memory of Fig. XI-6. Because the size of this memory is logarithmically related to the size of the closed memory, it is much smaller than the latter for most cases where this type of system would be useful.

The mode of operation just described is certainly not the only one possible. Additional open elements might often be profitably added, or various other models requiring less open memory could be devised. An advantage of this model is that some practical closed memories have inherent in their access circuitry the open memory described here, and no additional open elements need be added.

4. Preliminary Results

For the sake of brevity, proofs of the following statements will be omitted.

1. Sequential circuits with closed memories can be analyzed in a straightforward manner by means of flow tables (3).

2. There exist sequential circuits with m closed elements and n open elements which require at least m + n open elements when no closed memory is used. In other words, in these cases, the closed memory is equivalent to an open memory of the same size.

3. There exist sequential circuits with n open elements which cannot be realized with fewer than n - 1 open elements, regardless of how much closed memory is used. In these cases closed memories are worthless.

Problems falling into the two preceding categories represent an extremely small fraction of the aggregate of all possible sequential problems; most cases will be of an intermediate kind. The classification of any particular flow table remains to be investigated, along with the problem of devising formal synthesis techniques.

4. The following interesting, though apparently inconsequential, fact has been proved concerning cycles in closed memory systems with no inputs: While it is always possible to design an open memory system that cycles through all of its memory states,

this can never be done with a closed memory system.

5. Several diagrammatic representations of possible memory state transitions in closed element systems have been devised. (One of these consists of a hypercube with clipped corners.)

S. H. Unger

References

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3. D. A. Huffman, Technical Report 274, Research Laboratory of Electronics, M.I.T., Jan. 10, 1954.