X. TRANSISTOR CIRCUITS

Prof. H. J. Zimmermann   Prof. S. J. Mason   J. Gross
Prof. R. B. Adler   C. R. Hurtig

A. CONSTANT-RESISTANCE AGC ATTENUATORS FOR TRANSISTOR AMPLIFIERS

Following the suggestion made in the Quarterly Progress Report of January 15, 1955, we have built a variable-gain bandpass amplifier, centered at 9.0 Mc/sec and having a nominal bandwidth of 1.7 Mc/sec, with tetrode transistors. The amplifier in Fig. X-1 consists of four synchronously-tuned stages, two of which are gain-controlled by means of constant-resistance agc attenuators. The pertinent data for three different designs are given in Table X-1.

Table X-1

Characteristics of Tetrode Amplifiers

	Design		
	I	II	III
Maximum power gain, db	29	17.5	25
Measured gain variation, db	-42	-42	-42
Center frequency (fc), Mc/sec	9.0	9.0	9.0
Percentage of change in fc	±1.7	±0.8	±1.4
Nominal bandwidth (BW), Mc/sec	1.0	1.4	1.7
Percentage of change in BW	±15	±3.9	±3.0
Second base current (I_{b_2}), ma	0.3	0.3	0.3
Maximum emitter bias current, ma	0.3	0.3	0.45
Load resistor (R_L), ohms	∞	4700	4700

The transformers are designed to provide an impedance match with a bandwidth of approximately 2.3 Mc/sec per stage. Because of the dissymmetrical characteristics of the external shunt diodes and the respective emitter diodes, and the diffusion capacitance of the shunt diodes, the center frequency and bandwidth do vary somewhat with changes in gain. The undesired variations may be reduced with a sacrifice in gain, as illustrated in case II. The tuned circuits, which are normally loaded by the variable attenuators, were shunted by additional 4700-ohm resistors. The bandwidth was increased, but the gain reduced by approximately 12 db. The variations in center frequency and bandwidth as functions of amplifier gain were correspondingly reduced. In case III the maximum emitter current was increased by 50 per cent without redesigning the transformers. For many critical applications the latter two amplifier designs may prove satisfactory.
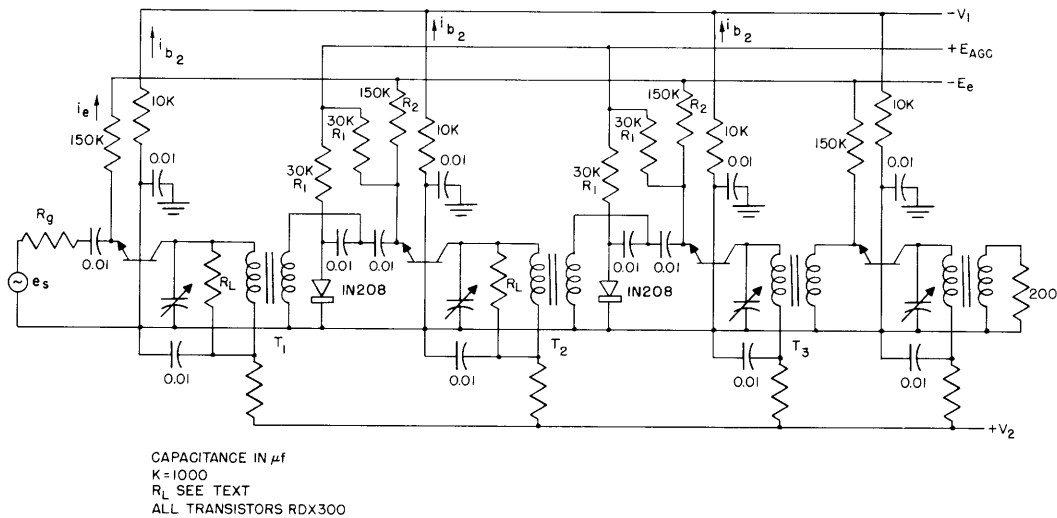
Fig. X-1

Variable-gain, constant-bandwidth tetrode amplifier.

Several low-capacitance, point-contact, silicon diodes were tested in the attenuator circuits in an attempt to minimize the effect of diffusion capacitance variations with the agc voltage. The change in the center frequency with agc voltage was indeed reduced, but the bandwidth variation was increased by the increased dissymmetry of the diodes.

It is probable that in all cases a significant portion of the variation in center frequency with agc voltage results from a corresponding variation in the transistor collector capacitance.

B. THE OPERATION OF MULTIPLICATION

As indicated in the Quarterly Progress Report of January 15, 1955, it is possible, by using a proper arrangement of the constant-resistance attenuator, to make the amplitude of a carrier signal a linear function of the control (agc) signal. By cascading two of these stages, and applying the same signal at both control inputs, a square-law device for either a positive- or a negative-polarity control signal (but not both) may be built. This type of circuit is shown in Fig. X-2. The amplitude of the output voltage at the carrier frequency of 1800 cps is shown as a function of a positive dc voltage at the input for two different pairs of transistors in Fig. X-3.

When the input signal is equal to or greater than the fixed bias signal in the constant-resistance attenuator, the amplitude of the carrier signal remains constant. At very low levels of input signal the carrier at the output becomes obscured in the transistor noise. The accuracy of the square-law action is better than ±10 per cent over at least a 50-db dynamic range.
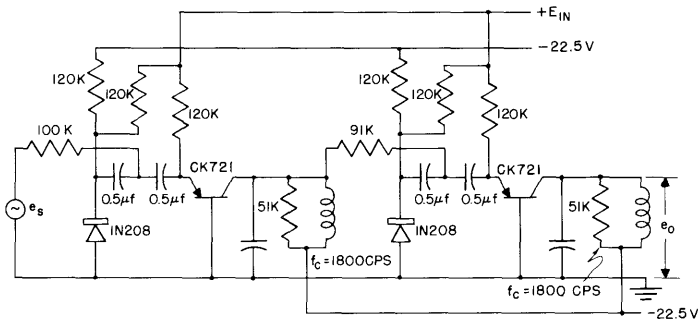
Fig. X-2
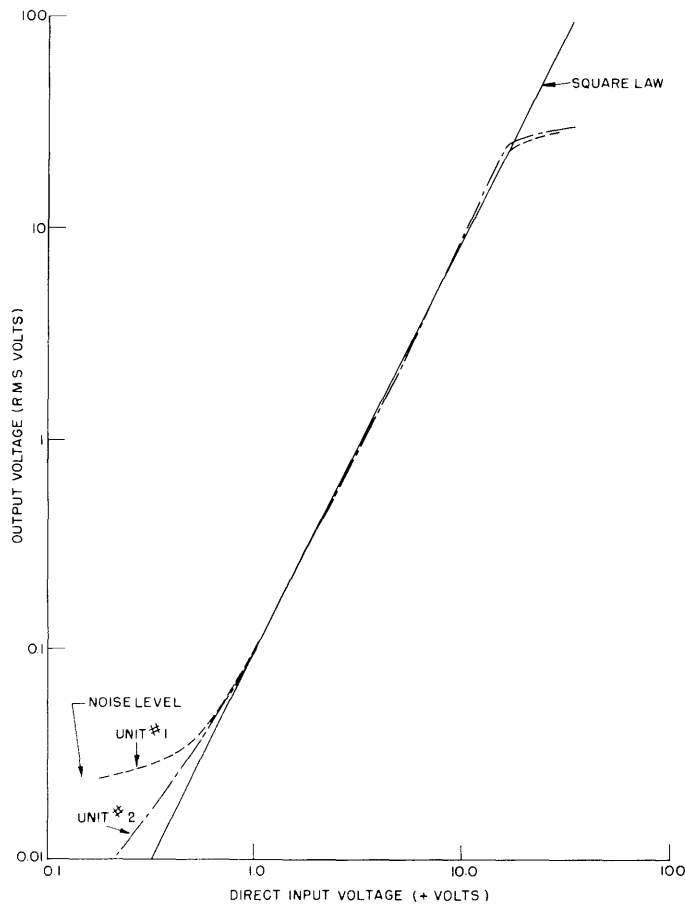
Square-law device for a positive polarity input voltage.

Fig. X-3

Transfer characteristics of a transistor square-law device.

There are two basic limitations to this type of square-law device: the input is restricted to a voltage of one polarity; the frequency response is severely limited. At either extreme of the dynamic range one of the diodes (either the shunt diode or the emitter diode of the transistor) is zero-biased, and the charge time constant is controlled by the large resistor used to simulate a current source. Thus, in the circuit shown in Fig. X-2 the charge time constant is approximately 0.1 sec. The value of the capacitance may be reduced only if the carrier frequency is increased, since the emitter and shunt diodes must be kept at the same ac potential.

Both of these limitations may be avoided by use of the circuit shown in Fig. X-4. In this circuit the quiescent operating point is set in the center of the linear region of the attenuator. The carrier signal at the output of the transistor at the quiescent point is balanced out by the use of the phase-shifting transformer and the resistance-adding network. The amplitude of the output voltage is a linear function of the modulating voltage, with a phase shift of 180° of the carrier signal occurring when the modulating voltage changes polarity. This circuit acts as a balanced modulator whose output is a linear function of both the modulating input and carrier input. Preliminary tests indicate that a dynamic range of 60 db may be obtained with an accuracy of better than ±10 per cent over this range. The frequency response of the modulator may be as high as 10 per cent of the carrier frequency. The stability of the balance of the modulator at the quiescent operating point has not been tested, but operation at room temperature has been very satisfactory.

To obtain the operation of multiplication, two such stages may be cascaded. Alternatively, this type of stage may be preceded by a conventional balanced modulator. To convert the output from carrier waveform to direct current, a sensed amplitude detector is required.

C. THE PROCESS OF TIME INTEGRATION

In many analog computers it is necessary to have a device capable of performing a time integration of a time-varying voltage. The term integration as commonly used implies a variety of desired objectives. Those of importance for our immediate purpose are realized by a device that has a gain approaching infinity at zero frequency and an ability to "remember" an integrated voltage after the input signal returns to zero. In applications where a memory accuracy of 0-10 per cent is desired for periods approaching one minute, the effective discharge time constant must be approximately 10 minutes.

The usual techniques for time integration require high-gain dc amplifiers. Unfortunately, our interest in transistor circuits for integration makes this method undesirable because simple transistor dc amplifiers are severely limited by the temperature dependence of the transistor parameters. Even though it is possible to minimize this
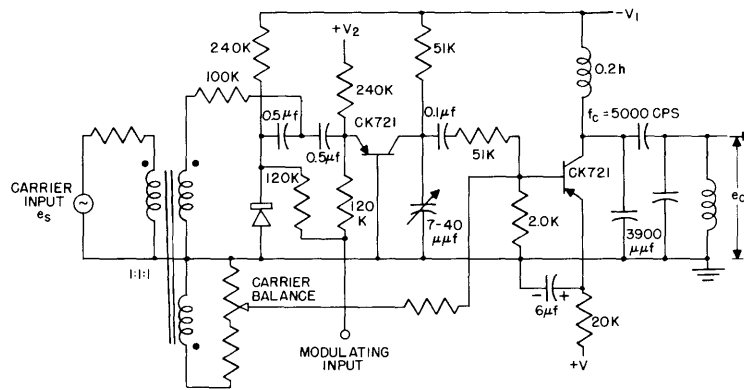
Fig. X-4

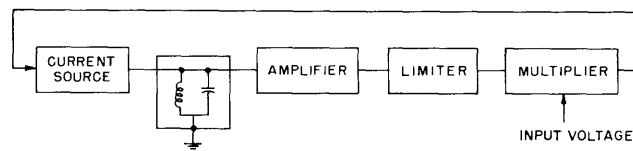Balanced modulator useful for the process of multiplication.

Fig. X-5

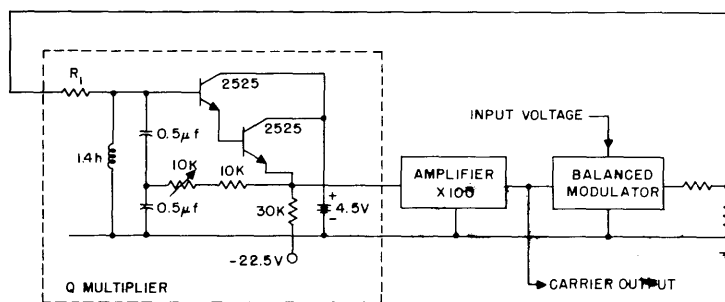Block diagram of an integrator employing a pole on the j-ω axis.

Fig. X-6

Transistor integrator employing a Q multiplier.

-69-

difficulty by using chopper stabilization or balanced-bridge techniques, the over-all amplifier performance is still limited by either time-varying parameters, excessive physical size, power supply requirements, or component lifetime. In view of these facts, it appears that the technique of time integration at a carrier frequency may prove advantageous for some applications.

It can be shown fairly simply that a high-Q timed circuit acts as a lowpass filter to sideband modulation signals. As the Q approaches infinity, the memory time of the tuned circuit approaches infinity. That is, in the simplest case, a circuit having poles on the $j\omega$ axis at values $\pm\omega_0$ will oscillate continuously at any prescribed amplitude. By a proper arrangement, it is possible to control the total energy stored in the tuned circuit as a function of an input signal. Since the Q of the tuned circuit is to approach infinity, an external oscillator used to drive the tuned circuit would have to oscillate at exactly the circuit resonance, a condition difficult to satisfy. If, however, the signal input is continuous, the energy stored in the tuned circuit may be used to drive the amplitude control circuit. One method of accomplishing this is shown in block diagram form in Fig. X-5. In this system the tuned circuit, composed of ideal components, is driven by a current source. The voltage across the tuned circuit drives a limiter and multiplier. The second input to the multiplier is the voltage to be integrated. The output from the multiplier is at carrier frequency (if the input is dc), but is either in phase or 180° out of phase with the carrier input. Thus, depending on the phase of the multiplier output, the total energy stored in the tuned circuit is either increased or decreased.

A preliminary transistor model is shown in Fig. X-6. The circuit consists of a transistor Q multiplier, an amplifier with a gain of 100, and a balanced modulator. By careful adjustment of the Q multiplier, the memory time may be made as long as 10 minutes for signals in the range of 0-20 mv rms across the tuned circuit. At the carrier frequency of 250 cps the equivalent Q of the tuned circuit is 10^6, representing a Q multiplication of approximately 10^5. Although this multiplication factor can be maintained satisfactorily at one temperature, it may change seriously with temperature.

A less temperature sensitive and generally more stable system may be realized by using a mechanically vibrating element to obtain a high initial Q. Bimorph quartz crystals have Q's greater than 10,000 at 1000 cps. However, the equivalent electric circuit contains a zero and pole in close proximity. By using a bridge circuit it is possible to obtain a transfer characteristic containing a simple pole, and then, by feedback, to increase the Q.

ERRATA: In the Quarterly Progress Report of January 15, 1955: Equation 3, page 72, should read: $G_1 = I_e/K$; line 2, page 74, should read: Thus the conductance G_2 must ...; Eq. 4, page 74, should read: $G_2 = G_{in} - G_1 = G_{in}$ ... .

C. R. Hurtig