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Effects of Ionizing Radiation on Digital Single Event Transients in a 180-nm Fully Depleted SOI Process

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Abstract—Effects of ionizing radiation on single event transients are reported for Fully Depleted SOI (FDSOI) technology using experiments and simulations. Logic circuits, i.e. CMOS inverter chains, were irradiated with cobalt-60 gamma radiation. When charge is induced in the n-channel FET with laser-probing techniques, laser-induced transients widen with increased total dose. This is because radiation causes charge to be trapped in the buried oxide, and reduces the p-channel FET drive current. When the p-channel FET drive current is reduced, the time required to restore the output of the laser-probed FET back to its original condition is increased, i.e. the upset transient width is increased. A widening of the transient pulse is also observed when a positive bias is applied to the wafer without any exposure to radiation. This is because a positive wafer bias reproduces the shifts in FET threshold voltages that occur during total dose irradiation. Results were also verified with heavy ion testing and mixed mode simulations.

Index Terms—Floating body, fully depleted silicon-on-insulator, gamma radiation, heavy ions, ionizing radiation, laser irradiation, single-event transients, total ionizing dose.

I. INTRODUCTION

RAPID scaling down in microelectronics circuit fabrication has made modern digital circuits more sensitive to single-event transients (SETs). Indeed, with the transistor gate capacitance getting smaller, particles found in space or at high altitudes are more likely to turn on transistors that were originally off [1]. These particles generate spurious analog signals that, if allowed to propagate through combinatorial logic gates, can corrupt data in storage elements including latches [2]. Data corruption is worse for higher-speed technologies [3], therefore characterizing and understanding transient generation and propagation through logic gates is needed to develop hardening

strategies that will not adversely limit circuit speed. Whether an SET signal propagates depends on the signal amplitude and width, and the circuit clocking speed. But one cannot assume that the SET will retain the same characteristics after propagation when arriving at the input of the first latch. Indeed, Ferlet-Cavrois *et al.* [4] were the first to show that transients can broaden as they propagate through a chain of inverters in both bulk and partially depleted SOI processes.

Further work presented last year [5]–[7] showed that SET broadening effects are quite complex and intractably dependent on the fabrication technology, transistor layout and engineering, and circuit operating conditions. Last year, we reported the first experimental data on SETs characterized in MITLL (MIT Lincoln Laboratory) 180-nm FDSOI CMOS process using an on-chip SET measurement circuit [7]. We showed that n-channel FETs (nFETs) and floating-body FETs are the most SET-sensitive devices. SET transients are twice wider for every 0.1-V decrease in the power supply voltage. Also, SETs are larger than 1 ns after propagating through 200 inverters, despite their initial width of less than 0.07 ns at the generation location. Using source-body-contacted FETs greatly reduced propagation broadening effects. While the probability for creating an SET is over one order of magnitude higher for bulk Si than in FDSOI [8], SETs can have comparable width in both technologies if SETs are propagating through a chain with at least two hundred inverters.

In this work, we show for the first time how ionizing radiation affects SETs in a 180-nm FDSOI CMOS process. We used a chain of inverters to study SET generation and propagation, and an on-chip SET characterization circuit for the SET pulse width measurement. SET test circuits were irradiated under bias with a Cobalt-60 gamma source. SET pulse widths were characterized before and after irradiation using a micron-size pulsed laser beam to generate charge in off-state n-channel FETs (nFETs). The laser technique allowed us to decouple ionizing from propagation-induced effects. We found that the accumulated ionizing radiation causes the SET pulse to get wider at the output node where it is initially generated. This initial widening is caused by radiation-induced positive charge trapped in the buried oxide layer (BOX), which shifts transistor threshold voltages. Furthermore, we show that, when an SET is generated due to charge collection in an nFET, the SET pulse width is wider after than before irradiation because ionizing radiation reduces the drive current of the p-channel FET (pFET). This is because the pFET is responsible for pulling up the driven node as the body charge in the struck nFET is dissipated. We found that ionizing radiation effects could be reproduced by applying a positive wafer

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bias without using any radiation at all. This is explained because, in FDSOI technology, a positive wafer bias mimics total dose radiation effects. Our results were also verified with mixed mode simulations and heavy ion testing.

II. EXPERIMENT DESCRIPTION

The SET characterization circuit was designed and fabricated in MITLL's Low-Power 1.5-V 180-nm FDSOI CMOS process [9] based on the circuit methodology developed by Narasimham [10]. This circuit was used previously to characterize SET pulses in advanced bulk Si and FDSOI processes [7], [10]. In this circuit, transients are generated in a chain of 200 inverters. The chain has a fixed input voltage. The nFET and pFET widths are 0.6 and 2.5 μm to balance the inverter; the etched gate length is 0.2 μm , or 0.02 μm larger than minimum length to reduce the effect of process-induced gate length variation in our analysis.

Any transient that propagates to the output of the inverter chain is captured within the pulse width measurement circuit composed of a series of 25 latches. The input of the latch circuit has a self-triggering delay sub-circuit that detects the arrival and the full capture of the SET event within the 25 latches. At that moment, the state of the 25 latches is held, transferred to a shift register, and clocked out serially to the output. If the leading edge of the SET pulse has traveled through a latch, the output state of that latch has flipped. If the trailing edge has passed through, then the latch has flipped back to its original state. Therefore, the width of the SET is measured in units of latch delays. A ring-oscillator test circuit with the same exact 25 latches and load as in the capture circuit was fabricated to measure the latch delay on chip. The capture circuit was designed to collect transients with widths between 1 and 25 times the latch delay within \pm one-half of the latch delay [10].

The laser experiments were performed at the pulsed-laser Single-Event Effects (SEE) facility at the Naval Research Laboratory in Washington, DC. The laser delivers 1-ps optical pulses centered at 590 nm (2.1 eV) with a full-width-at-half-maximum spot size of 1.2 μm . Packaged FDSOI SET chips are mounted on a xyz stage with 0.1- μm resolution and imaged with a TV monitor, which allows accurate placement of the laser spot within the SET-sensitive nFET region as shown in Fig. 1. For these experiments, the laser pulse energy was 3 or 4X larger than the minimum energy required to generate transients [7]. The transient width was calculated by multiplying the number of flipped latches by the measured latch delay. Circuits were irradiated with the Cobalt-60 gamma irradiator at the Naval Research Laboratory in two increments of 50 krad (SiO_2) each. During irradiation, the circuit was biased so that VDD was at 1.5 V, ground at 0 V and the input of the inverter chain was at 0 V. In this condition, every other CMOS inverter has an nFET and a pFET that is off state. Ionizing radiation effects are worst for this bias condition for this FDSOI technology [11].

MITLL 180-nm FDSOI CMOS process features a 4.2-nm thick gate oxide, a 40-nm-thick SOI and a 400-nm-thick buried oxide (BOX). MITLL uses a mesa process to isolate the transistor active SOI regions. The oxide thickness between the polysilicon gate and the SOI at the mesa edge is \sim 4.2-nm. In

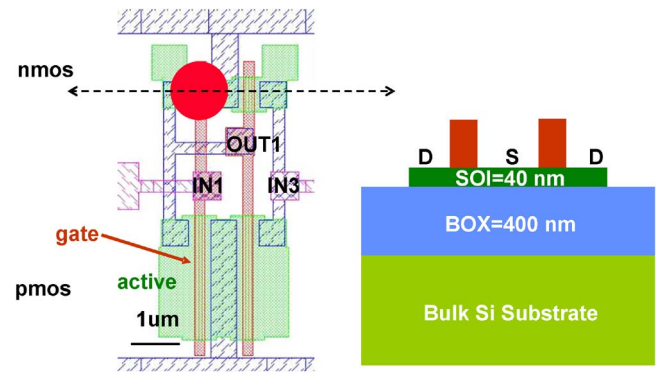


Fig. 1. (Left) Layout of adjacent inverters in the chain; the red circle is the laser beam half-maximum drawn to scale above an nFET gate region. (Right) Cartoon representation of the inverter cross-section in the region of the dotted line.

this process, charge accumulation in the oxide layer near the edge of the SOI and under the main gate region is negligible compared to that in the BOX, which is 400-nm thick. Circuits were characterized on the laser-pulse bench within less than 20 minutes of the irradiation.

III. RESULTS

As discussed earlier [7], an off-state nFET is the most sensitive transistor to SET generation. If a laser or ion hit an "off" transistor, it will generate charge in the transistor body, which turns on the device until the excess majority carriers either recombine or exit to the source. If the charge is large enough, it pulls down the output node of that inverter and causes the next inverter in the chain to change state, and the leading edge of a pulse propagates through all the downstream inverters. When the associated pFET transistor has passed enough current to bring the output voltage of the struck inverter back near its initial value, the following inverter switches back to its correct value and the pulse ends. Thus, the pulse width indicates the time required to dissipate the generated charge, and pull up the output.

Fig. 2 shows histograms of the SET count before and after irradiation up to 50 and 100 krad (SiO_2) for laser-induced charge in an off-state nFET. Results are shown for SET propagating through 20, 100 and 180 inverters. For these circuits, the latch delay is 80 ps with a pulse width resolution of \pm 40 ps. As discussed in the next section, the same latch delay value was used before and after irradiation. Results show that the SET pulse width increases with accumulated ionizing radiation. We observe that the increase in SET pulse width is larger between 0 and 50 krad than between 50 krad and 100 krad (SiO_2).

Fig. 3 shows a graph of the median SET width versus the SET propagation distance for the data shown in Fig. 2. The error bars represent \pm one standard deviation. We can clearly see on this graph that the SET width increases with increased total dose, but this increase is not linear with dose. A linear fit to the data shows that the SET width increases on average by 224 ps between 0 and 50 krad (SiO_2), while it increases only by 86 ps between 50 and 100 krad (SiO_2). Results also indicate that the propagation-induced pulse-width broadening does not appear to change with increased total dose (i.e., 4.6 ps/inv.) between 0 and 50 krad.

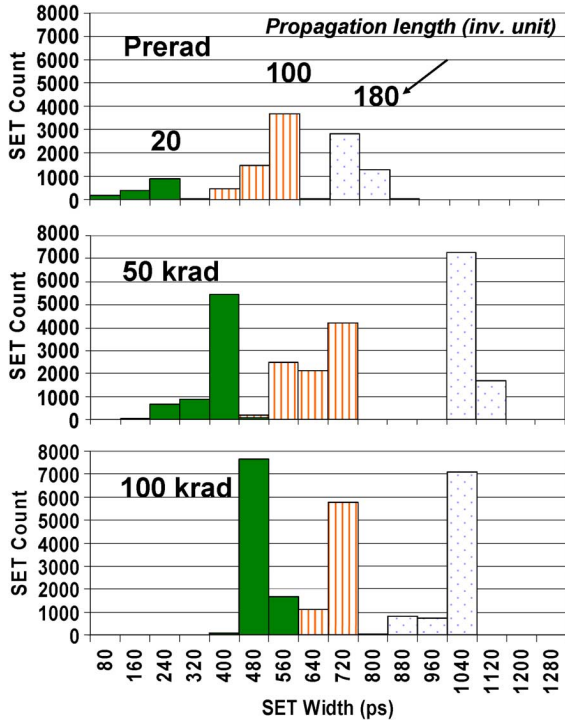


Fig. 2. Transient count versus SET pulse width before and after irradiation with Cobalt-60 for SETs generated with a pulsed-laser on an off-state floating body nFET; the transient propagates through 20, 100 and 180 inverters.

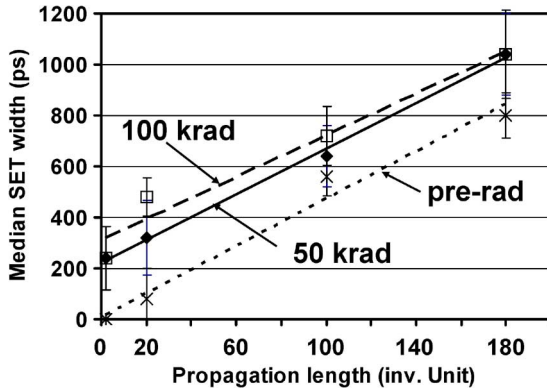


Fig. 3. Median SET pulse width versus the SET propagation distance in unit of inverters before and after Cobalt-60 irradiation. SETs were generated with a pulsed-laser in an off-state nFET.

We also found that the effects of ionizing radiation can be reproduced without using any radiation at all, simply by applying a positive voltage to the wafer. In FDSOI, the body of the transistor is fully depleted, therefore the front gate (formed by polysilicon gate/gate oxide/SOI layers) and the back gate (formed by the Si substrate/BOX/SOI layers) are capacitively coupled. Applying a voltage to the wafer shifts the threshold voltage (and drive current) of the nFET and pFET. The sign of the shift depends on whether the wafer voltage is positive ($-\Delta V_{th}$) or negative ($+\Delta V_{th}$). Fig. 4 shows histograms of the transient count versus the SET pulse width for V_{wafer} of 0, +3 V and +6 V for SET propagating through 20, 100 and 180 inverters.

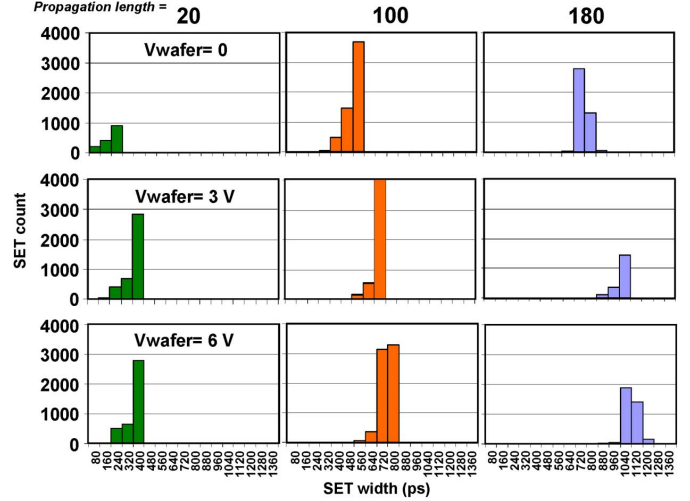


Fig. 4. Histograms of the transient count versus SET pulse width for $V_{wafer} = 0, +3$ and $+6$ V and SETs propagating through 20, 100 and 180 inverters. SETs were generated with a pulsed-laser in an off-state nFET.

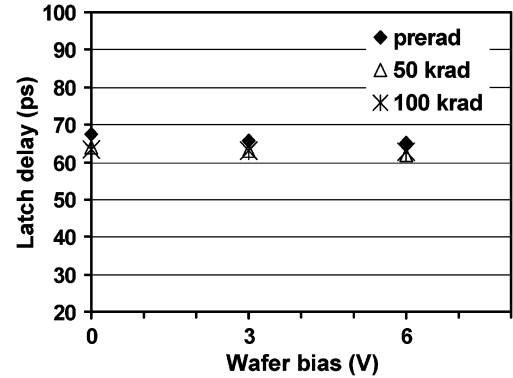


Fig. 5. Latch delay versus wafer bias, V_{wafer} , normalized to $V_{wafer} = 0$ before and after total ionizing doses (10-keV X-ray) of 50 and 100 krad (SiO_2).

IV. DISCUSSION

First, we show why we used the same latch delay before and after irradiation. Then, we explain why the SET pulse-width widens with increased accumulated radiation, and why the increase in SET pulse width is larger between 0 and 50 krad than between 50 and 100 krad (SiO_2).

The latch delay was measured on a ring-oscillator sub-circuit fabricated next to the SET circuit. The ring-oscillator has a chain of CMOS inverters with $L = 0.2 - \mu\text{m}$, $W = 0.5 - \mu\text{m}$ nFET and $L = 0.2 - \mu\text{m}$, $W = 1.7 - \mu\text{m}$ pFET that is matching the size and load of the 25 latches in the SET measurement circuit. Fig. 5 shows the latch delay versus the wafer bias voltage, V_{wafer} , and the total ionizing dose for these circuits. Testing was done with 10-keV X-rays in an Aracor 4100. Results for Cobalt-60 irradiation are expected to be similar to that of X-rays for this particular test. For V_{wafer} between 0 and 6 V, the latch delay changes by less than 5% up to 100 krad (SiO_2). 5% of the latch delay is comparable to the resolution of our measurement circuit (i.e., = half a latch). In comparison, the increase in SET pulse width measured at 100 krad, and shown in Fig. 3, is equivalent to 3 latches. Using a constant latch delay was appropriate.

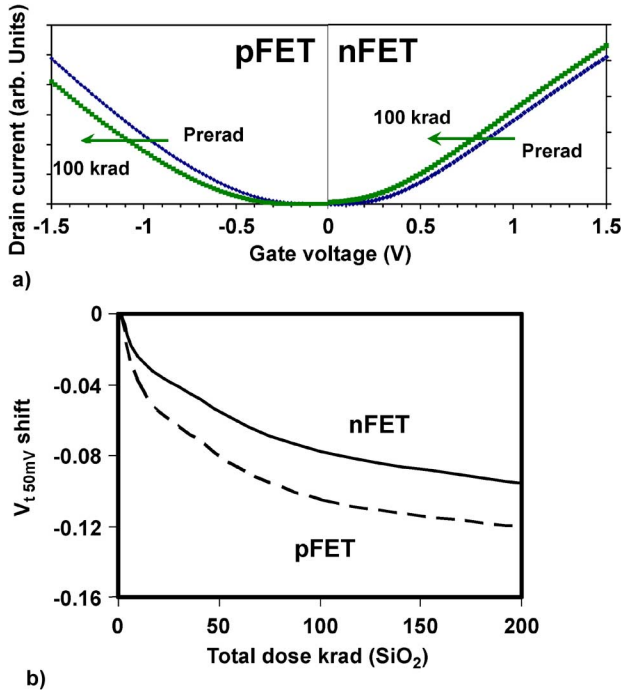


Fig. 6. a) Drain current versus gate voltage, $I_D(V_G)$, curves for minimum geometry pFET and nFET at a drain voltage of 1.5 V. b) Threshold voltage shift for pFET and nFET versus total dose (10-keV X-ray data).

The latch delay does not change significantly with total dose, but the drive strengths of the nFET and pFET do. Fig. 6(a) shows the drain current versus gate voltage, $I_D(V_G)$, curves, for the nFET and pFET at a drain voltage of 1.5 V. After irradiation, the nFET threshold voltage decreases, and the pFET threshold voltage increases. This is because the radiation-induced charge trapped in the BOX is positive, therefore the threshold voltage shift for nFET and pFET is negative. Ionizing radiation increases the latch output rising time (pFET dominated), and decreases the latch output falling time (nFET dominated). The latch delay remains roughly constant with total dose indicating that the increase in rising time is roughly compensated by the decrease in falling time.

Fig. 6(b) shows that the change in threshold voltage is not linear with dose. Indeed, the change in threshold voltage between 0 and 50 krad is $\sim 4\times$ larger than between 50 and 100 krad. The increase in SET pulse width with increased TID seems to be consistent with the change in the FET threshold voltage with TID.

Fig. 7 shows the normalized drain current at $|V_G| = |V_D| = 1.5$ V of FDSOI nFET and pFET (i.e., the FET drive strength) as a function of the substrate bias voltage (positive). The nFET drive strength increases while the pFET drive strength decreases with an increase in wafer bias. This is because the BOX/SOI interface is capacitively coupled to the front thin-oxide/SOI interface [11]. The change in transistor drive current observed at positive substrate bias voltages is analogous to the effect of the positive charge induced by ionizing radiation and trapped in the BOX [12].

Fig. 8 shows that the median SET pulse width for $V_{\text{wafer}} = +6$ V before irradiation and for $V_{\text{wafer}} = 0$ after a 50-krad ir-

radiation. Both sets of data are similar indicating that, indeed, applying a positive wafer bias without exposure to radiation can mimic the effects of ionizing radiation. Conversely, for chain irradiated at 50 krad, applying a negative bias of -6 V to the wafer shifts the SET width to its pre-radiation values. In previous work [11], P. Gouker *et al.* have shown that the density of fixed charge in the BOX is $\sim +3.2 \times 10^{11} \text{ cm}^{-2}$ for a total dose of 50 krad (SiO₂). This density corresponds to a SOI/BOX (back gate) threshold voltage shift of $+6$ V, which is consistent with the value of wafer bias voltage applied to reproduce the TID effects.

Wafer bias effects were also verified with heavy ion testing. Fig. 9 shows an histogram of the SET count versus the SET width for an SET testchip exposed to Xe heavy ions (LET = 68.84 MEV-cm²/mg) at Berkeley National Laboratory. The total fluence was $1 \times 10^8 \text{ cm}^{-2}$. Experimental results are shown for $V_{\text{wafer}} = 0$ and $V_{\text{wafer}} = +6$ V. The pulse widths are larger with heavy ions than with the laser. This is because the micron-size laser spot generates SET events in a very specific location within the inverter chain, while the 3-inch diameter heavy ion beam generates SET events in the entire chain of 200 inverters. The results in Fig. 9 are consistent with the pulsed-laser experiments, and show that the SET pulse width increases with an increase in the wafer bias voltage.

Fig. 3 shows that the SET pulse widths are larger after irradiation than before irradiation regardless of how long the SETs propagate through the chain of inverters (i.e., propagation length). These results also suggest that the propagation-induced broadening has remained unchanged after irradiation (i.e., same slope for the linear fit to the data before and after irradiation). Therefore it appears that, for charge injected in an off-state nFET, the accumulation of ionizing radiation causes the SET pulse to get wider at the output node where it is initially generated.

To verify this, mixed mode simulations were performed using TCAD and SPICE models calibrated to measurements made on transistors fabricated in MIT-LL 180-nm FDSOI technology. Fig. 10 shows that in the simulations, the off-state nFET of the second inverter was modeled using 3D-TCAD [13]. The other transistors were modeled in SPICE. Simulations show that, as long as the ion strikes the transistor body, the SET pulse width is approximately independent of the exact location. Fig. 11 shows the simulated transient pulse width with a Full Width Half Maximum (= SET width) value of ~ 80 ps for an equivalent LET of 60 MeV-cm²/mg. This value is consistent with previous work [7]. Simulations were repeated with modified nFET and pFET SPICE models to match the effects of ionizing radiation. The BSIMSOI threshold voltage parameter, V_{TH0} , [14] was changed with V_{TH0} (after irradiation) = V_{TH0} (before irradiation) + ΔV_{TH0} , where $\Delta V_{\text{TH0}} < 0$ (i.e., both n and pFET thresholds shifted negatively). Fig. 9 shows that the SET pulse-width increases from 80 to 110 ps for $\Delta V_{\text{TH0}} = -0.25$ V.

Fig. 12 shows simulations again for $\Delta V_{\text{TH0}} < 0$, but this time only the pFET models were modified, not the nFETs. Results show that the SET pulse-width increases by the same amount even though only the pFET models were modified to simulate TID effects. These results confirm that the increase in

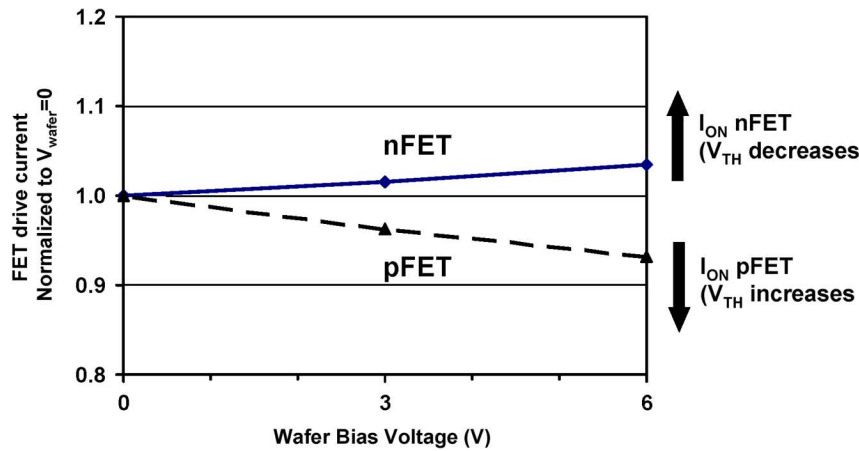


Fig. 7. nFET and pFET drive currents at $|V_G| = |V_D| = 1.5$ V for $L = 0.2\text{-}\mu\text{m}$, $W = 0.5\text{-}\mu\text{m}$ nFET and $L = 0.2\text{-}\mu\text{m}$, $W = 1.7\text{-}\mu\text{m}$ pFET (as in the latch circuit) versus V_{wafer} .

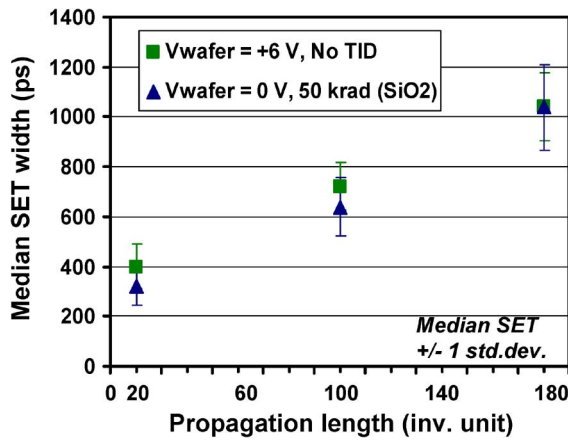


Fig. 8. Median SET pulse width versus the SET propagation distance in unit of inverters before irradiation for $V_{\text{wafer}} = 6$ V and after Cobalt-60 irradiation for $V_{\text{wafer}} = 0$. SETs were generated with a pulsed-laser in an off-state nFET.

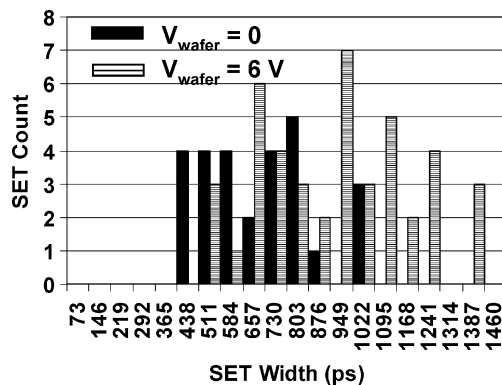


Fig. 9. Histogram of the SET count versus SET pulse width for an inverter chain exposed to Xe heavy ions ($\text{LET} = 68.84 \text{ MEV-cm}^2/\text{mg}$) up to a total fluence of $1 \times 10^8 \text{ cm}^{-2}$. Data are shown for $V_{\text{wafer}} = 0$ and $V_{\text{wafer}} = +6$ V.

SET pulse-width with increased ionizing radiation is directly correlated to the decrease in drive strength of the pFET. Indeed, for SET induced in nFET (most sensitive case), the pFET is responsible for restoring the inverter output to its original state after the nFETs was turned on. A lower pFET drive means

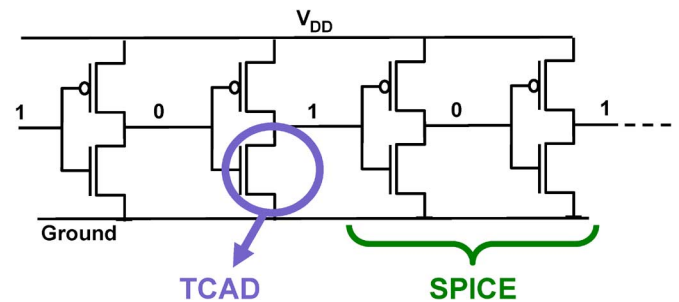


Fig. 10. Illustration of the mixed mode approach used to simulate the SET pulse width. The chain has 4 inverters. Charge is deposited in the body of the second nFET that is modeled in 3D TCAD. The other transistors are modeled in SPICE.

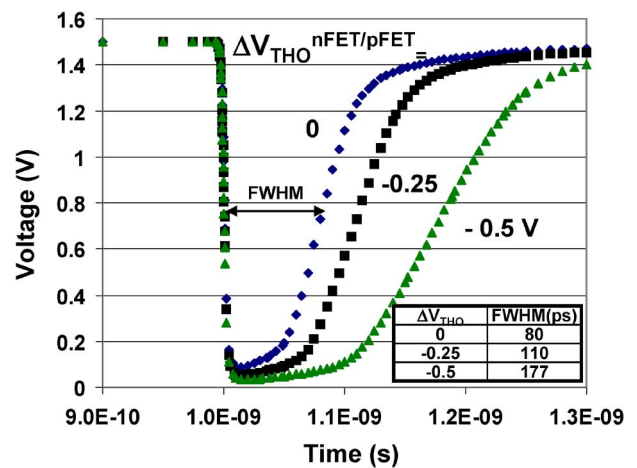


Fig. 11. Simulated SET pulse width for nominal n/pFETs ($\Delta V_{\text{TH0}} = 0$), for $\Delta V_{\text{TH0}} = -0.25$ V and for $\Delta V_{\text{TH0}} = -0.5$ V for both n/pFETs; $\Delta V_{\text{TH0}} < 0$ to simulate ionizing dose effects.

that more time is required to restore the output to its original state; therefore, a broader transient signal is generated. Note that the ΔV_{TH0} values used in the simulations are larger than that extracted from experimental data [Fig. 6(b)]. This could be explained in part because we are not simulating the entire circuit. Further work will be required to fully understand this discrepancy.

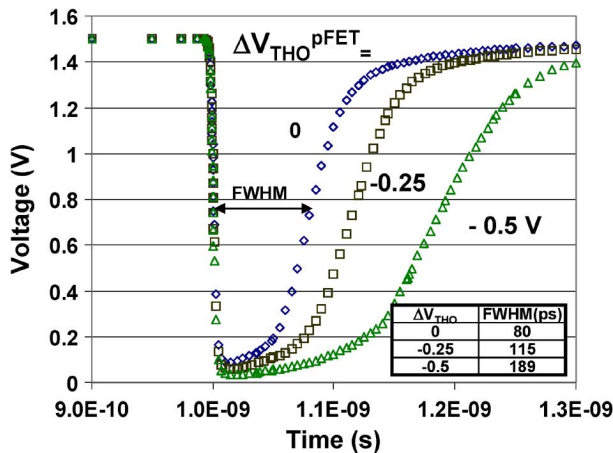


Fig. 12. Simulated SET pulse width for nominal n/pFETs ($\Delta V_{TH0} = 0$), for $\Delta V_{TH0} = -0.25$ V and for $\Delta V_{TH0} = -0.5$ V **only for pFET**; $\Delta V_{TH0} = 0$ for all nFET.

V. CONCLUSION

We have shown for the first time how ionizing radiation affects single event transients in a 180-nm FDSOI CMOS process. SETs were generated in an inverter chain, and SET pulse widths were measured with an on-chip characterization circuit. SETs were characterized before and after irradiation with a Cobalt-60 gamma source using a pulsed laser beam. Laser-induced charge was generated in an off-state nFET, the most sensitive FET to both SET and ionizing radiation. The accumulated ionizing radiation causes the SET pulse to get wider at the output node where it is initially generated. Radiation-induced positive charge is trapped in the BOX layer, and shifts the FET threshold voltages. Most importantly, ionizing radiation reduces the drive current of the pFET, which is responsible for restoring the transistor struck by the laser to its original state. Ionizing dose effects were reproduced by using a positive wafer bias without any radiation at all. Results were also verified using mixed mode 3D TCAD simulations and heavy ion testing.

The effects reported in this paper are applicable to any technology sensitive to oxide charging when exposed to ionizing radiation. This include the buried oxide in SOI, and possibly the isolation oxide in both bulk and SOI technologies. Our FDSOI process uses a mesa isolation, in which the thin sidewall oxide has minimal sensitivity to oxide charging compared to that in the BOX.

These results show also the importance of testing for the combined effects of total dose and single event phenomena, which is more accurately representing the natural space radiation environment. For hardness assurance of FDSOI parts, we recommend repeating the single event (SE) testing after exposure to a TID value corresponding to the total accumulated dose during the space mission. Alternatively, applying

a wafer bias during SE testing may provide some insights on TID effects. The specific wafer bias value is a function of the FDSOI process (BOX thickness, VDD value, etc.) and the total dose value. This work also highlights the benefit of using the pulsed-laser characterization technique to understand the basic radiation effect mechanisms.

REFERENCES

- [1] R. Baumann, "Single event effects in advanced CMOS technology," in *Proc. IEEE NSREC Short-Course*, Seattle, WA, Jul. 11, 2005.
- [2] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger, "Comparison of error rates in combinational and sequential logic," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 2209, 1997.
- [3] P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, and J. R. Schwank, "Production and propagation of single-event transients in high-speed digital logic ICs," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, p. 3278, Dec. 2004.
- [4] V. Ferlet-Cavrois, P. Paillet, D. McMorrow, N. Fel, J. Baggio, S. Girard, O. Duhamel, J. S. Melinger, M. Gaillardin, J. R. Schwank, P. E. Dodd, M. R. Shaneyfelt, and J. A. Felix, "New insights into single event transient propagation in chains of inverters-evidence for propagation-induced pulse broadening," *IEEE Trans. Nucl. Sci.*, vol. 54, p. 2338, 2007.
- [5] V. Ferlet-Cavrois, V. Pouget, D. McMorrow, J. R. Schwank, N. Fel, F. Essely, R. S. Flores, P. Paillet, M. Gaillardin, D. Kobayashi, J. S. Melinger, O. Duhamel, P. E. Dodd, and M. R. Shaneyfelt, "Investigation of the Propagation Induced Pulse Broadening (PIPB) effect on single event transients in SOI and bulk inverter chains," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, p. 2842, Dec. 2008.
- [6] L. W. Massengill, "Single-event transient pulse propagation in digital CMOS," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, p. 2861, Dec. 2008.
- [7] P. Gouker, J. Brandt, P. Wyatt, B. Tyrrell, A. Soares, J. Knecht, C. Keast, D. McMorrow, B. Narasimham, M. Gadlage, and B. Bhuvu, "Generation and propagation of single event transients in 0.18- μ m fully depleted SOI," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, p. 2854, Dec. 2008.
- [8] M. Gadlage, J. R. Ahlbin, V. Ramachandran, P. Gouker, C. A. Dinkins, B. L. Bhuvu, B. Narasimham, M. W. McCurdy, R. D. Schrimpf, R. L. Shuler, and D. McMorrow, "Temperature characterization of digital single event transients in bulk and fully depleted SOI technologies," presented at the Nuclear and Space Radiation Effect Conf., Quebec City, QC, Canada, 2009.
- [9] MITLL Low-Power FDSOI CMOS Process Design Guide Revision 2007:2 [Online]. Available: <http://www.ll.mit.edu/AST>
- [10] B. Narasimham, V. Ramachandran, B. L. Bhuvu, R. D. Schrimpf, A. F. Witulski, W. T. Holman, L. W. Massengill, J. D. Black, W. H. Robinson, and D. McMorrow, "On-chip characterization of single event transient pulse widths," *IEEE Trans. Dev. Mater. Rel.*, vol. 6, p. 542, 2006.
- [11] P. Gouker, J. Burns, P. Wyatt, K. Warner, E. Austin, and R. Milanowski, "Substrate removal and BOX thinning effects on total dose response of FDSOI NMOSFET," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, p. 1776, Dec. 2003.
- [12] S. Cristoloveanu and S. Li, *Electrical Characterization of Silicon-on-Insulator Materials and Devices*. Norwell, MA: Kluwer, 1995, ch. 8 and 10.
- [13] M. Gadlage, P. Gouker, B. L. Bhuvu, B. Narasimham, and R. D. Schrimpf, "Heavy ion induced digital single event transients in a 180 nm fully depleted SOI process," presented at the Nuclear and Space Radiation Effect Conference, Quebec City, QC, Canada, 2009.
- [14] BSIMSOI [Online]. Available: <http://www-device.eecs.berkeley.edu/~bsimsoi/>