An Energy-Efficient Wireless Data Link for Implantable Electronics

by

Daniel Prashanth Kumar

B.S., Electrical Engineering, Stanford University (2007)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2009

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Abstract

Low-power wireless links are important for the development of long-term implantable neural prostheses. Furthermore, in implanted systems with many neural recording electrodes, the data rate of the wireless link will need to be quite high since each recording electrode can produce about 120 kbps of data. For low-power operation, inductively-coupled near-field wireless links have shown great promise and were used to develop a power-efficient data link for biomedical implants.

A prototype bi-directional, half-duplex wireless link based on inductive coupling was designed in a 0.18 μm process. The uplink (i.e. data transmission from the internal transceiver) was designed to use an impedance modulation strategy. Since this technique only requires a single local oscillator (LO) in the external transceiver, the energy expenditure of the implanted transceiver is minimized. Simulated uplink data transfer rates of up to 10 Mbps has been shown. A PWM based ASK coding strategy was used for the downlink (i.e. data transmission to the implanted device). The downlink is able to achieve a data transfer rate of up to 1.5 Mbps. A technique to reduce BER of inductive coupling links due to pulse-width distortion effects by pre-distorting the transmitted data is also presented. A calibration technique to reduce the resonant frequency mismatch between the two magnetically coupled resonators is also shown.

Thesis Supervisor: Rahul Sarpeshkar
Title: Associate Professor

Acknowledgments

First of all, I would like to thank my thesis advisor, Professor Rahul Sarpeshkar for his guidance and support during this project. His strong physical intuition of circuits and systems continues to amaze me.

I would also like to thank Professor John Wyatt at MIT and Dr. Joseph Rizzo at the Massachusetts Eye and Ear Infirmary for funding this project. Many thanks also to my academic advisor, Professor John Kassakian, especially for making sure I was aware that there was a lot more to Boston than just MIT.

I would like to thank the past and present members of the Analog VLSI & Biological Systems Group at MIT. In particular, I would like to thank Scott Arfin, Bruno Do Valle, Soumyajit Mandal, Benjamin Rapoport, Lorenzo Turicchia, and Woradorn Wattanapanitch, who have served as valuable points of reference for all things technical and otherwise.

I am also grateful to MOSIS, through which the prototype chips were fabricated. Many thanks to Wes Hansford at MOSIS for all his help. Also, my thanks to Gamuda Inc., Malaysia for the financial support I received during my undergraduate studies.

Next, a word of thanks for all my friends near and far. To Omair Saadat, roommate-extrodinaire, many thanks. To the MIT crew, namely Mohamed Abutaleb, Siddharth Bhardwaj, Eddie Eltoukhy, Shirin Farrahi, and Wei Li, thanks for making the last couple of years memorable. Many thanks to Edward Boenig, Margo Lipstin, June Park, and Edward Tay for all your support. And to Johann John, many, many thanks.

Finally, I would like to acknowledge my family. I owe my deepest gratitude to my parents, Iruthia Kumar and Suganyah Ganesan. Thank you both for everything. To the two of my biggest supporters, Nicholas P. Kumar and Monica P. Kumar, your love and support mean a lot to me.

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Chapter 1

Introduction

> Steve Austin, astronaut. A man barely alive. Gentlemen, we can rebuild him. We have the technology. We have the capability to build the world's first bionic man. Steve Austin will be that man. Better than he was before. Better, stronger, faster.
>
> ---
>
> *The Six Million Dollar Man*

The goal of re-engineering the human body to make it better, stronger, and faster has been a recurring theme in the realm of science fiction for many decades now. In recent years, however, a similar theme of re-engineering the human body, not so much as to provide superhuman powers but to improve the quality of life of patients with significant physical or mental impediments, has become increasingly popular within the mainstream scientific community. To this end, brain machine interfaces (BMIs), or more generally, systems that interface with neural systems in biology, have been the subject of significant research of late [13].

BMIs can be largely divided into two groups, stimulation and recording systems. Stimulation based systems, in particular, have been the focus of much research over the last two decades, and some have even moved beyond the research phase and into the mainstream of rehabilitative medicine. One BMI in particular, the Cochlear implant, has enjoyed significant success in restoring hearing to deaf patients for nearly

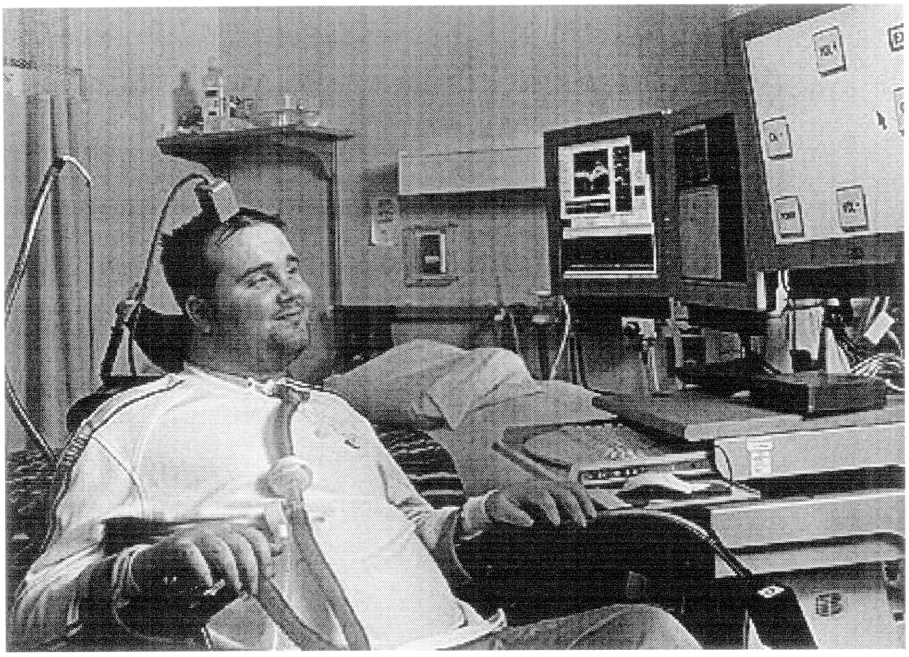

Figure 1-1: The first published human trial of a recording BMI. The patient in the photograph suffer from severe spinal cord injury. The patient is able to control a computer cursor (top right) using thought alone. Neural firing data recorded using an implanted electrode array is relayed to the external processing units via a transcranial, transdermal cable attached to the top of the patient's head. The need for a transdermal device opens a pathway for infection, which prevents long-term use of such devices in rehabilitative medicine [2, 14].

three decades now [17, 19, 26] and has been implanted in over 150,000 patients worldwide. Besides Cochlear implants, other BMIs such as pacemakers [37], which are used to regulate heartbeats, and more recently, deep brain stimulation systems (DBS) [34], which are used to alleviate the symptoms of Parkinsons disease have shown considerable promise in improving the survival rates and quality of life of patients with arrhythmia or Parkinsons disease.

All of the systems mentioned above are examples of stimulation based BMIs. More recently however, recording based BMIs have begun to garner significant interest. In the field of rehabilitative medicine, for example, recording based BMIs hold promise to help improve the quality of life for patients with spinal cord injury [23]. The key concept behind the motivation to use recording BMIs to improve the quality of life of patients suffering from paralysis lies in the results obtained from basic neuroscience research, which indicate that regions of the brain known as the primary motor cortex

and pre-motor cortex play an important role in planning and control of deliberate motion [30] [9]. Thus, by recording neural activity of a population of neurons in the pre-motor or motor cortex, and decoding the neuron firing rates [25], the thoughts of the patient can be decoded and used to control an external device such as keyboard, a robotic arm, or even to re-stimulate motor neurons in the peripheral nervous system in order to cause muscular motion. Beyond medicine, BMIs are also of significant interest to neuroscientists who are conducting basic neuroscience research in order to further uncover the mysteries of the brain. Being able to record action potentials from a population of neurons opens new doors for exploration.

A series of recent experiments using behaving animal models have shown, quite extraordinarily, the viability of a recording BMI to help patients with severe neurological injuries [22,25,29,31]. In these experiments, neuronal recording from primate models was used to predict, with a high level of accuracy, the intended direction of motion in real time. Preliminary human trials indicate that patients using such systems are able to move a cursor, 'type' on a virtual keyboard, and perform simple movements using a robotic arm [14]. While these experiments serve to illustrate the immense potential of BMIs, to ensure long term viability of recording BMIs, numerous engineering challenges will need to be overcome. Issues such as the coating of electrodes with glial cells that results in the loss of the electrical signal sensed by the recording electrodes over time, and preventing the electrode arrays from drifting due to the motion of the brain will need to be addressed before recording BMIs can be used as a neuroprosthetic in the mainstream of rehabilitative medicine.

One significant challenge to chronic implantation of BMIs is the fact that most experimental recording systems in use today require a transdermal pathway for a cable to provide power to the implanted device and telemeter data from the recording neural amplifiers to external processing units [14,28]. Such open wounds need close monitoring as they provide an infection route directly to the brain, which severely limits the use of such systems in chronic implants. Furthermore, even in basic neuroscience research, long term experiments using freely-moving animal models make the use of a BMI with a physical connection between the implanted unit and the exte-

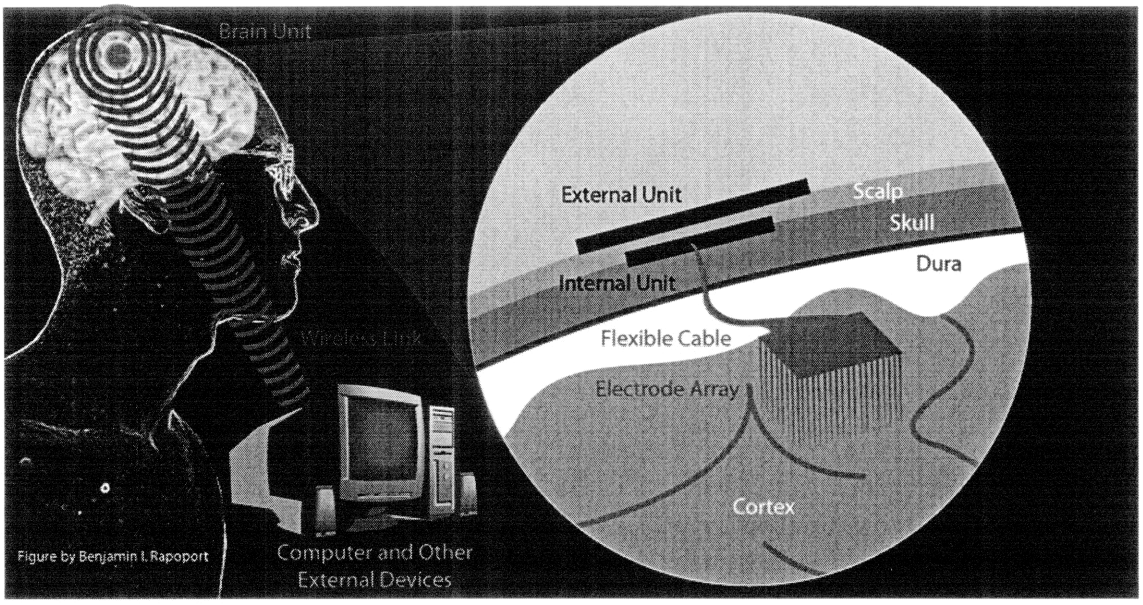

Figure 1-2: A proposed configuration of a completely wireless BMI. The implanted recording devices is completely wireless. Power is delivered remotely to the device using an inductive power link, and data is wirelessly transmitted from the implanted device. An external processing unit then relays the decoded data to an external actuator. Such a setup obviates the need for a direct opening through the skin.

rior cubersome. As such, novel methods to deliver power wirelessly to the implanted BMI and to wirelessly receive recorded neuronal waveforms from the implanted BMI will need to be developed. In this thesis, we explore an energy efficient, wireless communication link that is optimized for use in implantable biomedical devices.

1.1 Thesis Organization

This chapter serves to motivate the need for an energy efficient, wireless data link for biomedical implants. A wireless data link is necessary to move the use of BMIs from research labs to the surgical room, where BMIs can be used in therapeutic applications. In chapter 2, we evaluate the requirements of a wireless link that is to be used in implantable BMIs. We begin by surveying the different types of BMIs under development today, and the various communication requirements of each system, and some of the challenges that need to be overcome when communication with implantable devices.

Chapter 3 discusses the basics of impedance modulation. We explore two methods that have been used to analyze coupled resonator systems - a more traditional two-port analysis technique, and a more recent feedback view of magnetically coupled resonator systems. In Chapter 4, the design of the prototype primary transceiver is described. In particular, close attention is paid to shifting the burden of complexity and power consumption as much as is feasible from the implanted secondary transceiver to the external primary. Chapter 5 describes the design of the implantable secondary transceiver.

In chapter 6, we discuss the experimental setup and strategies employed to test the various subsystems in both t the primary and secondary transceivers. Measured performance data is also presented. Chapter 7 serves to summarize the work presented in this thesis. Possible future research directions for the work in this thesis are also presented here.

Chapter 2

System Design

2.1 Introduction

In this chapter, we begin by defining, in general terms, the architecture of an implantable BMI. We then examine the high-level requirements of an implantable wireless telemetry link for such a system. We will explore challenges that will need to be overcome in an implantable wireless telemetry link. Some of the challenges of developing a wireless link for an implantable device may not always be present in conventional, over-the-air wireless communication links. We end by considering possible wireless telemetry architectures that have been previously used for implantable devices. The insights obtained in this chapter will motivate our choice to use an impedance modulation scheme for wireless communication with an implanted device.

2.2 A Generalized BMI Architecture

In general, there are two large classes of BMIs, stimulation based BMIs and recording based BMIs. More recently, however, a new class of BMIs have started to emerge in the literature. These new BMI systems combine stimulation and recording BMIs into a single system to form a 'closed-loop' BMI, which is particularly useful in basic neuroscience research. We term these new class of BMIs as hybrid BMIs.

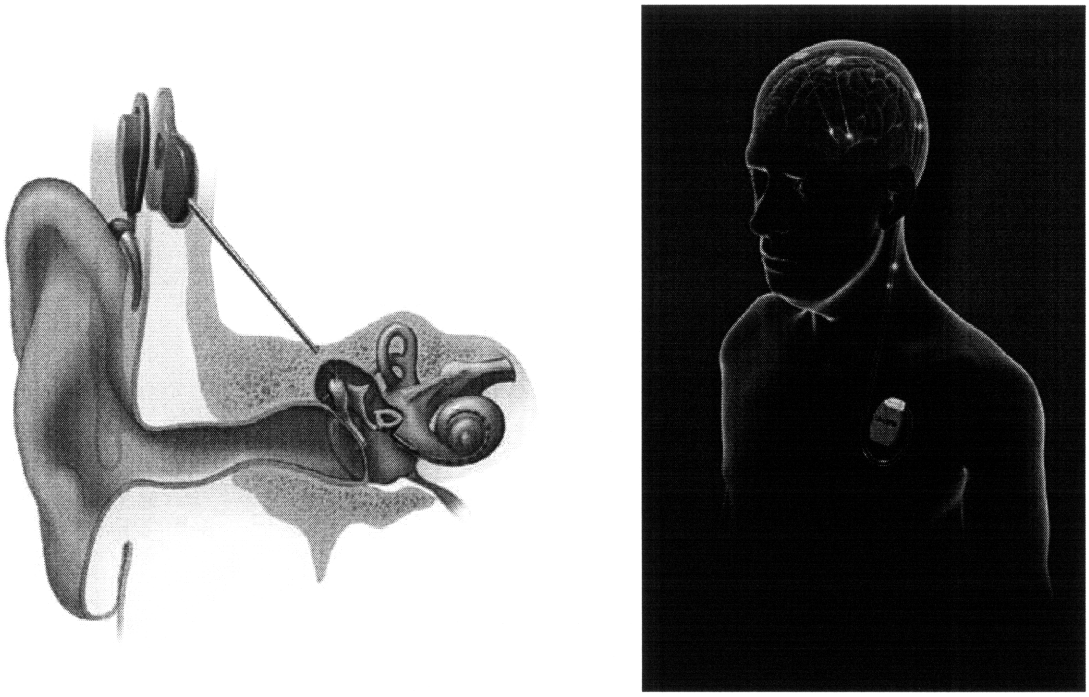

Figure 2-1: Stimulation based BMI systems. (a) A cochlear implant which converts electrical outputs from a external microphone into a train of stimulation impulses that are then wirelessly transmitted to the internal stimulation electrodes placed within the cochlear [24], and (b) a deep brain stimulation system (DBS), which has shown great promise in alleviating the debilitating symptoms of Parkinson's disease.

2.2.1 Stimulation BMIs

Stimulation BMIs are often used to compensate for loss of sensory ability of the nervous system by stimulating, electrically or otherwise, the neurons in the nervous system such as to simulate a particular sensation. In such systems, an external sensor such as a video camera or a microphone is used to record data from the environment. The information is conditioned, processed, digitized and relayed to an implanted unit connected to a set of electrodes. Based on the received data, the implanted unit then delivers a controlled amount of charge to the electrodes based on a pre-determined algorithm to stimulate neurons in close proximity to each electrode. Stimulation of neurons along the auditory or visual pathways have been shown to cause a sensation of hearing or vision in deaf or blind patients. Besides

electrical stimulation, chemical and photonic stimulation of neurons have also been demonstrated in the literature [4, 21]. Fig 2-1 illustrates two different examples of stimulations BMIs, namely Cochlear implants for the deaf and deep-brain stimulation (DBS) systems for Parkinson's disease.

2.2.2 Recording BMIs

Another class of BMIs are recording BMIs which are mainly used to record electrical neural activity of a population of neurons. For example, in BMIs being designed to aid patients with paralysis, recording BMIs are used to record neural activity from the motor or pre-motor cortex, where much of planning of voluntary motion has been shown to occur. Current recording systems are able to monitor anywhere from four to more than a 100 electrodes [14]. After amplification, signal conditioning, digitization, and in some cases pre-processing, the neural data will need to be telemetered out to an external unit. The external unit can then use the neuronal data to decode the intention of the patient, which can then be used to control an external device such as a computer or a robotic arm.

2.2.3 Hybrid BMIs

Recently, a number of implantable BMIs being developed are hybrid in nature, in that stimulation and recording are done simultaneously, often at close proximity to each other. This ability for implantable units to stimulate and record simultaneously are proving to be exceedingly useful in basic neuroscience and medical research. For example, experiments in the field of optogenetics where light is used to excite or inhibit genetically modified neurons have shown great promise in exploring various neural circuit within the brain [4, 36]. In such experiments recording BMIs are used simultaneously to record the activity of a population of neurons (Fig 2-2).

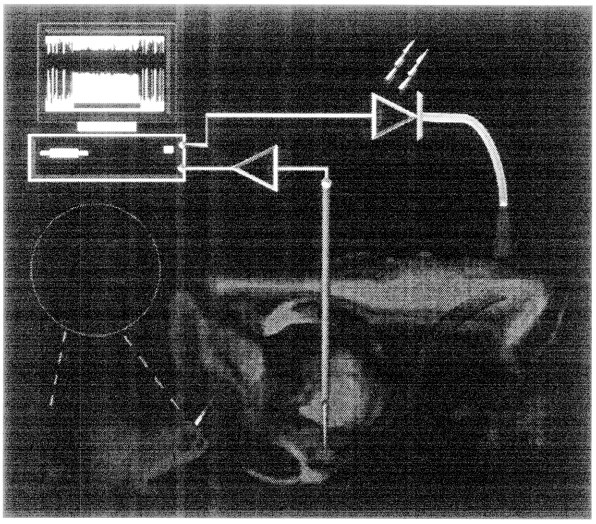

Figure 2-2: A hybrid BMI where stimulation and recording are performed simultaneously. In the area of research known as optogenetics, light is used to excite or inhibit populations of genetically modified neurons. The firing activity of these neurons are recorded using recording BMIs [36].

2.3 System Requirements

Initial experiments to explore the efficacy of BMIs for use in decoding neural data from the motor or pre-motor cortex used a trancutaneous connection through which a cable is used to deliver both power to the implanted unit and to relay raw recorded neural activity from implanted unit. BMI systems that require a transdermal and transcranial port, while may be used in short term experiments, cannot be used in long term implanted system. The high risk of infection is unacceptable and requires an alternate solution. As such, systems geared for long term implantation necessarily require a the elimination of all physical connection to the implanted device.

An implanted battery can be used to power the internal device. Recent advancement in the development of low power front-end analog amplified [33] and energy-efficient ADCs [10, 27], coupled with wireless recharging units that can achieve up to 75% efficiency [3] have made it possible for the implanted unit to be remain powered remotely for substantial periods of time. For data communication to and from the implanted device, an energy-efficient wireless link will need to be used in place of the wired link.

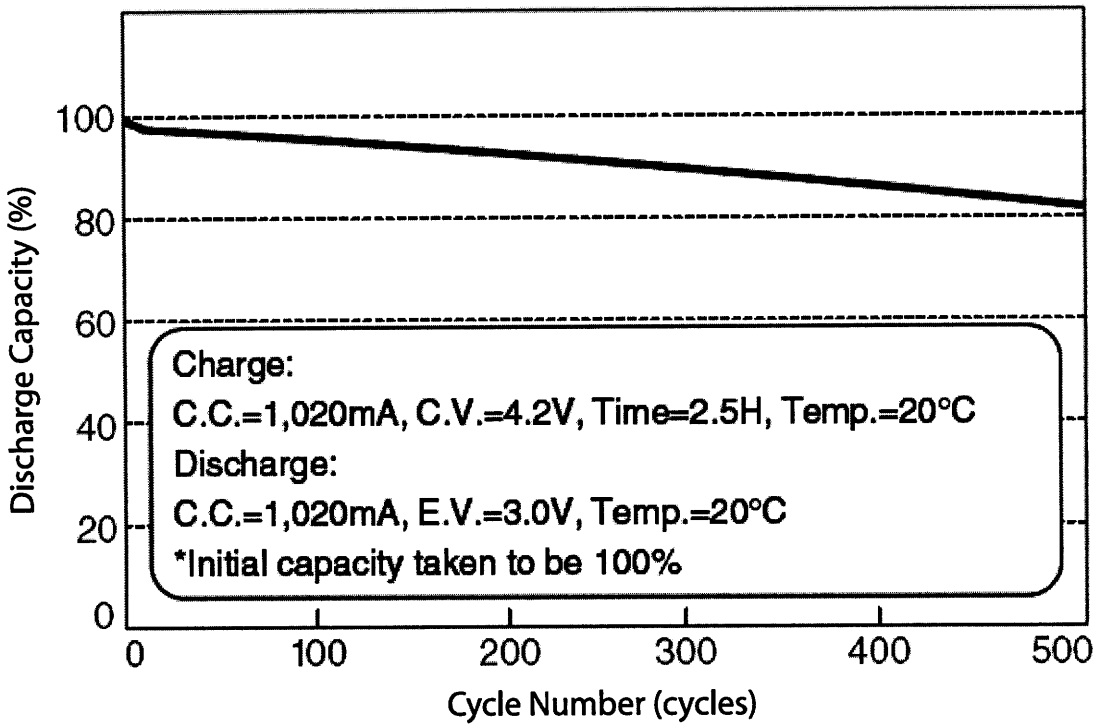

Figure 2-3: Charge storage capacity of an Lithium-ion battery vs. number of recharge cycles [1].

For the remainder of this work, we will assume that the wireless telemetry link will be used in a recording BMI. As will become apparent in the following sections, the requirements of wireless telemetry link for a recording BMI, for example with respect to power and bandwidth, is significantly more stringent for a recording BMI than for stimulation based BMIs.

2.3.1 Energy-efficient Operation

Energy-efficient operation of the wireless telemetry link is the single biggest criteria for a completely implantable unit. The implanted battery has a limited amount of power, which will need to be spent wisely, to ensure long-term operation. There are two main reasons why low-power operation is vital:

- **Limited Space for an Implanted Battery:** Most BMIs are implanted in

locations with very limited space. For example, a BMI implanted in the brain will need to be placed in the intracranial cavity, right below the skull or between the skull and the skin flap, while a retinal implant will need to be implanted on the retina, and often will need to follow the curvature of the eye. Given the limited energy density of current batteries, size constraints can severely limit the total available energy of the implanted power source. Thus any transceiver used in the implanted unit will need to be very energy-efficient.

- **Limited Number of Recharge Cycles for Batteries:** In order to ensure long-term operation, a wireless recharging system will be able to recharge the implanted battery. However, batteries have a limited number of recharge cycles before its performance degrades significantly. A Lithium-ion battery has approximately 10,000 recharge cycles, before its capacity falls below a 10%, rendering it unusable. From Fig 2-3 shows the maximum capacity of a battery under repeated charge-discharge-recharge cycles. Even after a few hundred cycles, the maximum capacity of the battery has been reduced by 20%. Given that replacing a battery on an implanted device will involve complex surgical procedures, the implanted unit will need to be able to operate for many years (or even decades) before needing a replacement battery.

Given the power constraints above, it is important to appreciate the fundamental difference between an implantable wireless telemetry system, and other over-the-air wireless communication schemes. In most other wireless communication schemes, the general optimization strategy is to optimize the total link power. This results in a trade-off between the power consumption of the transmitter and receiver. Often, the ratio of the power consumed in the transmitter to the power consumed in the receiver is close to unity. In implantable telemetry systems, however, the power optimization requirement is highly asymmetrical. Minimizing the power consumption of the implantable secondary, which has a highly limited energy supply, is paramount. The power consumption of the implanted secondary should be minimized even if it results in an increase in the power consumption of the external primary. This is the

fundamental driver in almost all architectural and circuit design choices made in this work.

2.3.2 Bandwidth

Initial experiments of BMIs have shown that reliable neural decoding can be performed with recording from about a hundred neurons. Increasing the number neurons that can be recorded from, however, is vital in improving the efficacy of BMIs used in neural prosthesis. On the other end of the spectrum, BMIs that are intended for use in basic neuroscience studies, will always benefit from recording of a larger neuron population. The need for data from a larger population of neurons translates directly to a larger bandwidth requirement for the communication link.

The required bandwidth for a recording BMI is given by,

$$BW = (1 + k) \cdot N f_s B_{ADC},$$

where N corresponds to the number of electrodes in the system, f_s is the sampling frequency, and B_{ADC} is the resolution of the on-chip ADC that digitizes the recorded neural signal. The constant k is an excess factor that models the overhead incurred by the communication channel such as the extra bits necessary to encode the header data or for error correction bits. In a 100-electrode recording BMI with $f_s = 15kHz$ and 8 bit resolution of the ADC, a BW of over 12 Mbps is required. Since the bandwidth requirement is linearly related to N, increasing the number of recording channels results in a proportional increase in the required bandwidth. As such, the wireless link will need have high-bandwidth to cope with the data output of recording BMIs.

2.3.3 Penetration Through Biological Matter

Another important distinction between an over-the-air communication system as opposed to a wireless link used to communicate with an implanted device is the requirement that a wireless link for implantable bio-electronics must be able to penetrate tissue. Biological tissue such as skin, muscle, cerebrospinal fluid, and muscle all have

finite conductivity and permittivity that increase and decrease with frequency respectively. The conductivity and relative permittivity of a number of different biological tissue over various frequencies is plotted in Fig 2-4 and Fig 2-5 respectively [6]. From this data, the penetration depth of signals at different frequencies can be calculated. The penetration depth, δ, is given by [15],

$$\delta = \frac{1}{\omega\sqrt{\mu\varepsilon}\left[\frac{1}{2}\left(\sqrt{1+\frac{\sigma^2}{\varepsilon^2\omega^2}}-1\right)\right]^{\frac{1}{2}}}.$$

The penetration depth, is plotted against frequency in Fig 2-6. From the plot in Fig 2-6, we can see that the penetration depth falls off sharply at high frequencies, particularly above a frequency of 1 GHz. As such, to maximize the penetration depth, while allowing for higher data bandwidths, the carrier frequency used by the wireless telemetry link should ideally be below 100 MHz.

In general, it is more efficient to transmit power and data using two seperate wireless links. To achieve efficient power transfer through the skin, very low frequencies that maximize the penetration depth of the signal (2-6), and a highly tuned link is beneficial to increase power transfer efficiency. On the other hand, for a data link, a high bandwidth is required, needing the use of higher frequencies. To satisfy these two competing requirements, having two wireless links, one for power and another for data is desirable.

2.3.4 Directionality

For recording BMIs, data will need to be transmitted to and received from the internal primary. The data transmitted to the implanted device will mostly constitute of programming data, which is used to configure the implanted device. As such, we can expect that the bandwidth requirement for the reverse telemetry is significantly lower than the bandwidth required to transmit out recorded neural data. Furthermore, since it can be expected that programming information will most likely be transmitted at infrequent intervals, a bandwidth of 1 Mbps for the downlink will be more than

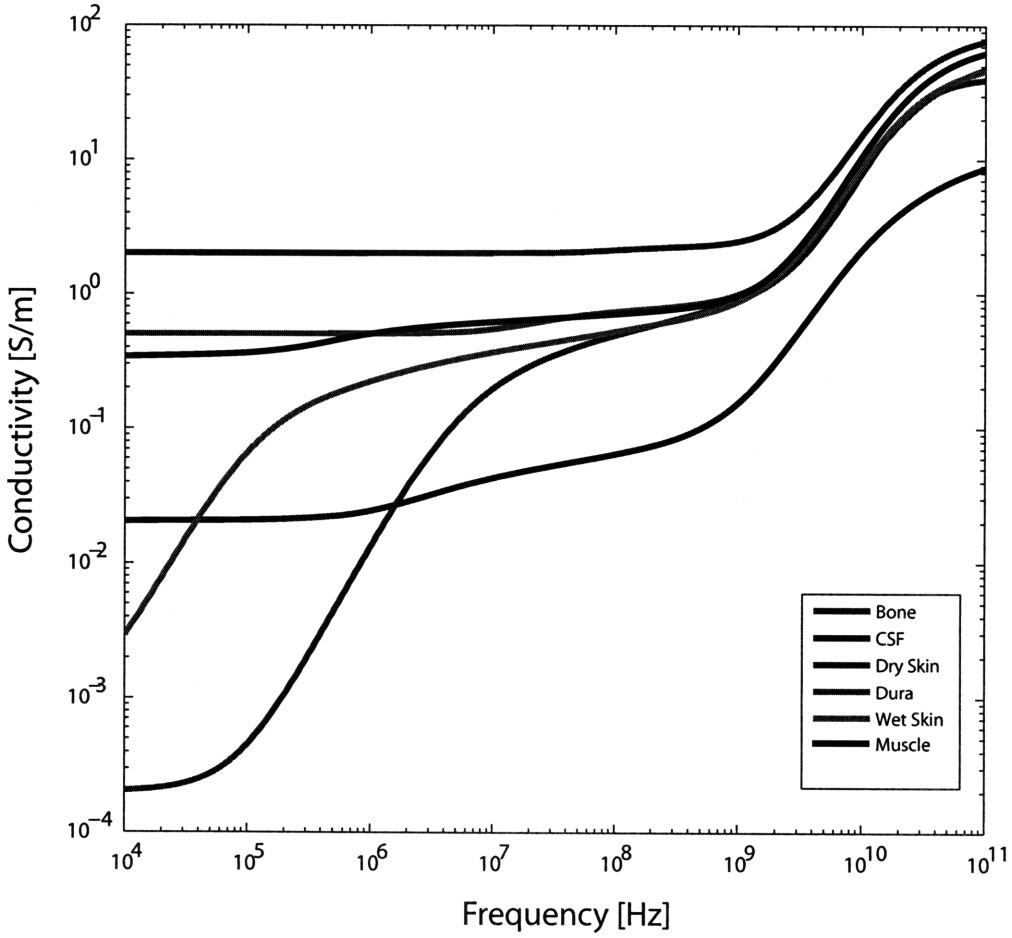

Figure 2-4: Conductivity of various biological tissue versus frequency

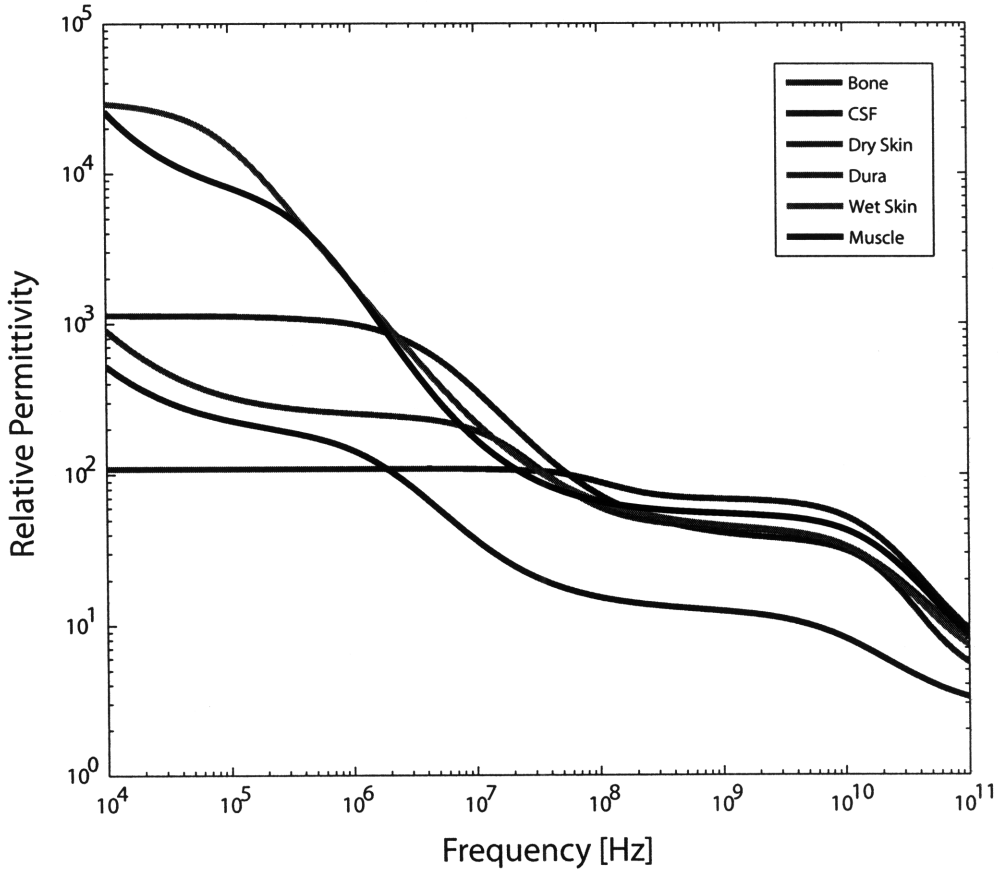

Figure 2-5: Relative permittivity of various biological tissue versus frequency

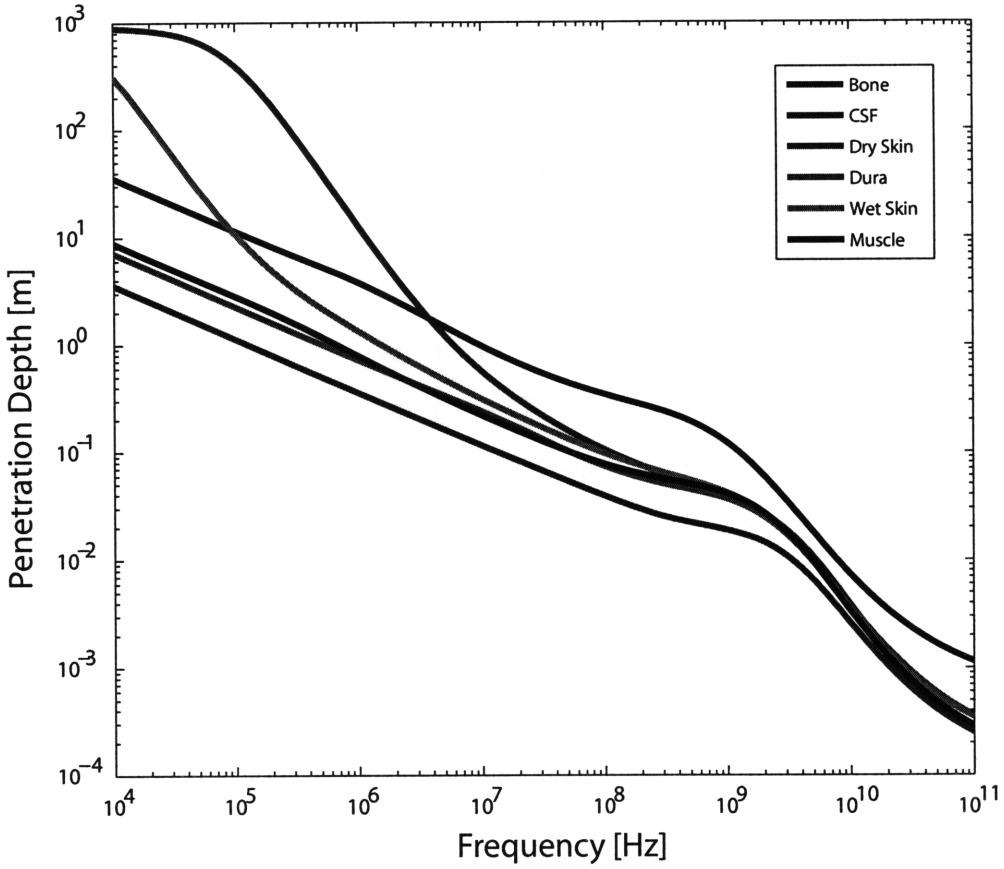

Figure 2-6: Penetration depth, δ, of various biological tissue versus frequency

Table 2.1: Implantable wireless telemetry link requirements

Parameter	Requirement
Power	Minimized (Particularly on the implanted transceiver)
Carrier Frequency	< 100 MHz
BW (Uplink)	> 8 Mbps
BW (Downlink)	0.5 - 1 Mbps

sufficient. This asymmetric bandwidth requirement is yet another difference between a link for implanted devices and a regular wireless communication link, where the bandwidth requirement in both communication directions are often assumed to be very similar.

2.4 Conclusion

In this chapter we have considered the requirements of a wireless link suited for communication with an implanted device. The requirements of such as link is often very different from that of a regular over-the-air communication link. The requirements of the wireless link for implantable devices is summarized in Table 2.1.

In the rest of this work, the term *uplink* will be used to denote the data transmitted from the implantable secondary to the external primary. The term *downlink* will then be used to denote the data being transmitted from the external primary to the implantable secondary.

Chapter 3

Theoretical Link Analysis

3.1 Introduction

In this section we develop and analyze theoretical models for the proposed bi-directional wireless data link. We begin by analyzing the impedance modulation based uplink. We first develop a model for the link and analyze it in two different ways: (i) using standard reciprocal two-port models, and (ii) by using a more intuitive, feedback-based block-diagram method. We close the chapter by briefly analyzing the ASK modulation based downlink.

3.2 Coupled Resonator Link

The wireless telemetry link will be used to transmit data across the skin-flap, over a short distance of about 1-2 cm. A model of a magnetically coupled resonator pair is illustrated in Fig 3-1. The primary resonator is driven by a time varying current source. The secondary resonator is magnetically coupled to the primary via the flux linkage through the two coils.

In the following analysis, we assume that most of the magnetic flux produced in the primary is directly coupled to the secondary. In transformers, this assumption is valid as the iron core couples the flux between the two coils very efficiently. However, in a magnetically coupled resonator system with an air core, this assumption is only

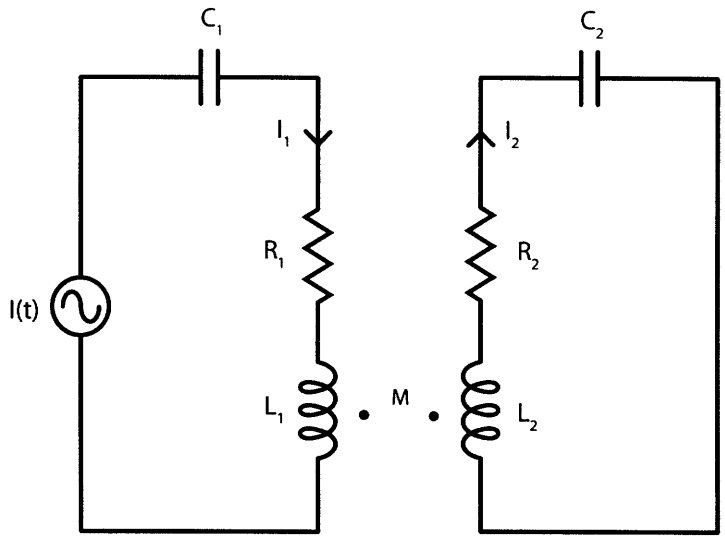

Figure 3-1: Schematic of an electrical model of a pair of magnetically coupled resonators.

valid if $A_1 >> A_2$, where A_1 and $A2$ are the cross-sectional areas of primary and secondary coils respectively.

3.2.1 Mutual Inductance, M

As shown in Fig 3-1, when the secondary coil is placed in close proximity to the primary, the two circuits become coupled by the flux that is generated by the current, I_1 flowing through the primary resonator. If I_1 is time varying, then the changing flux through the secondary coil will induce an electromotive force (EMF) in the secondary coil.

The magnetic field at the center of the secondary coil due to a time varying current, I_1 in the primary when both coils are separated by a distance, x, can be expressed as [12],

$$B(x) = \mu_0 N_1 I_1 \frac{r_1^2}{2\sqrt{(x^2 + r_1^2)^3}}, \tag{3.1}$$

where r_1 and r_2 are the radii of the primary and secondary coils respectively. The magnetic flux that passes through the secondary coil can then be expressed as,

$$\Phi(x) = B(x) \cdot A_2 \tag{3.2}$$

$$= \mu_0 N_1 I_1 \frac{\pi r_1^2 r_2^2}{2\sqrt{(x^2 + r_1^2)^3}}, \tag{3.3}$$

Therefore, the rate of change of the magnetic flux through the secondary coil, Φ, is proportional to the rate of change of the current in the primary coil. This proportionality constant is defined as the mutual inductance, M [20].

$$N_2 \frac{d\Phi}{dt} = M \frac{dI_1}{dt} \tag{3.4}$$

$$M = \frac{N_2 \Phi}{I_1} \tag{3.5}$$

$$= \mu_0 N_1 N_2 \frac{\pi r_1^2 r_2^2}{2\sqrt{(x^2 + r_1^2)^3}} \tag{3.6}$$

To be precise, the mutual inductance, M, is the mutual inductance due to the current I_1 and should be expressed as M_{21}. The induced voltage in the secondary can cause a current to flow, which will in turn induce a voltage in the primary, due to the mutual inductance M_{12}. However, using the reciprocity theorem derived from Ampere's and Biot-Savart's laws, one can show that [12],

$$M_{12} = M_{21} = M. \tag{3.7}$$

3.2.2 Coupling Coefficient, k

A convenient method of quantitatively describing the magnitude of coupling between two resonators is to use the coupling coefficient, k, which is given by [7],

$$k = \frac{M}{\sqrt{L_1 L_2}}, \tag{3.8}$$

where $0 \leq k \leq 1$ and the inductances L_1 and L_2 are the inductances of the primary and secondary coils and are given by,

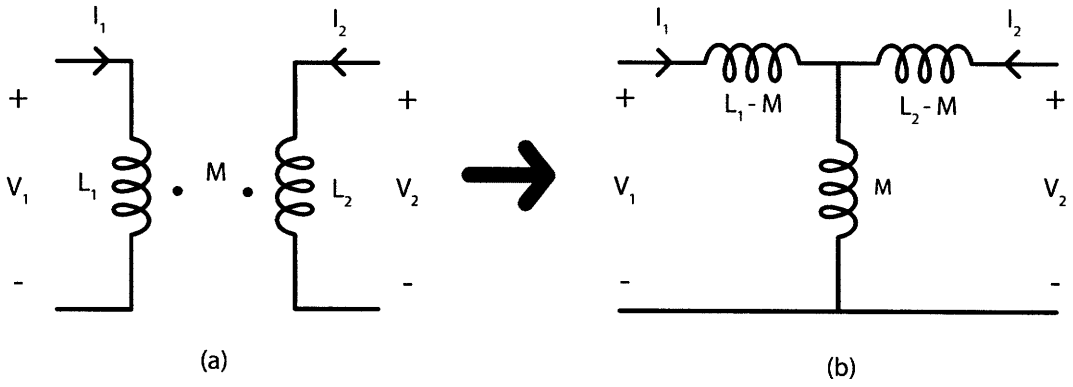

Figure 3-2: Magnetically coupled coils a) circuit schematic, and b) reciprocal two-port circuit model of the coupled coils

$$L_1 = N_1^2 \cdot \mu_0 \cdot \ln\left(\frac{2r_1}{d_1}\right) \tag{3.9}$$

$$L_2 = N_2^2 \cdot \mu_0 \cdot \ln\left(\frac{2r_2}{d_2}\right), \tag{3.10}$$

and d_1 and d_2 are the the thickness of the wire used in the primary and secondary coils respectively. When k is equal to one, both the coils are directly beside each other, such that all the magnetic flux generated by the primary is flow through the secondary and indicated perfect coupling. When k is zero, this indicates very weak coupling between the coils due to a large separation or magnetic shielding between the coils.

3.3 Two Port Model of Coupled Resonators

In order to simplify the analysis of a coupled resonator system, a two-port model can of the magnetically coupled resonator system can be developed. For simplicity, let us first focus on the coils that magnetically couple the two circuits and ignore the rest of the network on both the primary and secondary circuits. Fig 3-2(a) illustrates the circuit schematic of the magnetically coupled coils. From Equation (3.4), we see that

a time varying current in one coil creates a voltage in the other resonant circuit via the mutual inductance, M. Hence, for a set of ideal coils, the voltages V_1 and V_2 are given by the following differential equations [5],

$$V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \tag{3.11}$$

$$V_2 = L_2 \frac{di_1}{dt} + M \frac{di_1}{dt}. \tag{3.12}$$

The equations show that the voltages V_1 and V_2 is related to the current in the complementary circuit via the mutual inductance, M. Using these two equations, a reciprocal two-port model of the coupled coils in terms of the self inductances of both coils and M can be developed in order to describe electrically the magnetic coupling between the coils. Fig 3-2(b) shows the two-port representation of the coupled coils, which is also often referred to as the T-model of magnetically coupled coils. Given the T-model of the coupled coils, we can now use standard reciprocal two port circuit analysis methods to analyze the complete coupled resonators. A reciprocal-two port model of both the primary and secondary networks are illustrated in Fig. 3-3 [18]. Mapping the circuit variables obtained from the coupled resonators to the two port network, we obtain the following,

$$Z_{11} = sL_1 + R_1 \tag{3.13}$$

$$Z_{12} = sM \tag{3.14}$$

$$Z_{22} = sL_2 + R_2, \tag{3.15}$$

where R_1 and R_2 denote the series parasitic resistances of each coil. The source and load impedances are given by,

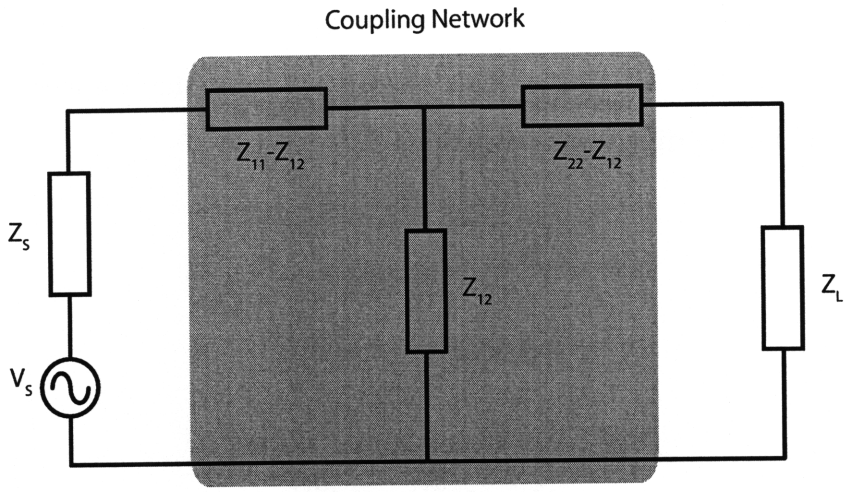

Figure 3-3: Reciprocal two-port model used in the analysis of two magnetically coupled resonators

$$Z_S = \frac{1}{sC_1} \tag{3.16}$$

$$Z_L = \frac{1}{sC_2} \tag{3.17}$$

If we then proceed to solve for the port impedances Z_T and Z_R which denote the impedances seen at the transmitter and receiver respectively as shown in Fig 3-3, we have,

$$Z_T = Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_L} \tag{3.18}$$

$$Z_R = Z_{22} - \frac{Z_{12}^2}{Z_{11} + Z_S}, \tag{3.19}$$

where Z_S and Z_L denote the source and load impedances respectively.

3.3.1 Impedance Modulation - High-Q State

If we drive the primary with a sinusoidal current source, i_{in}, while the secondary resonator is the high-Q state with the switch S open, as shown in Fig 3-4, the impedance

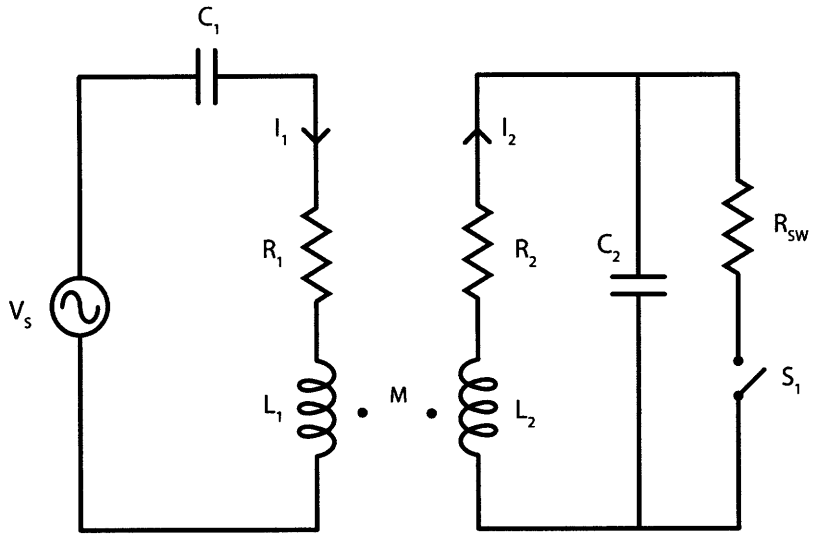

Figure 3-4: Circuit schematic of the coupled resonator system with the secondary resonator in the high-Q state. In the high-Q state, switch S_1 is turned off.

observed by the current source can is given by,

$$Z_{in} = Z_G + Z_T \tag{3.20}$$

$$= \left(\frac{1}{sC_1} + sL_1 + R_1\right) + \left(\frac{\omega^2 M^2}{\frac{1}{sC_2} + sL_2 + R_2}\right) \tag{3.21}$$

With the switch S open, and assuming that both resonators are operating at their resonant frequencies, ω_0, where

$$\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}, \tag{3.22}$$

and by observing that the quality of the primary and secondary resonators can given by,

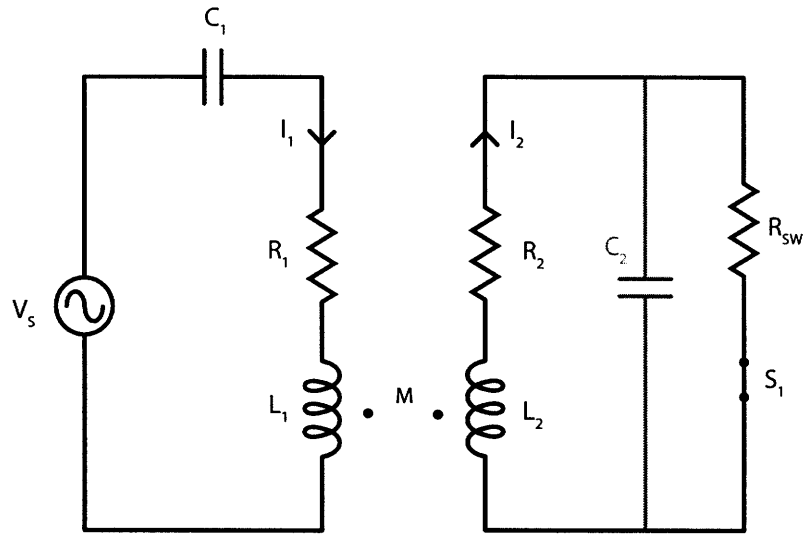

Figure 3-5: Circuit schematic of the coupled resonator system with the secondary resonator in the low-Q state. In the low-Q state, switch S_1 is turned on, which then shorts out capacitor C_2. R_{SW} denotes the finite resistance of the switch S_1

$$Q_1 = \frac{\sqrt{\frac{L_1}{C_1}}}{R_1} \tag{3.23}$$

$$Q_2 = \frac{\sqrt{\frac{L_2}{C_2}}}{R_2}, \tag{3.24}$$

and using equation (3.8), we can rewrite the impedance Z_{in} as,

$$Z_{in,hiQ} = R_1(1 + k^2 Q_1 Q_2). \tag{3.25}$$

3.3.2 Impedance Modulation - Low-Q State

When the switch S is closed, the capacitor C_2 is shorted out. The impedance seen by the driving current source I_{in} is then given by,

$$Z_{in,hiQ} = \left(\frac{1}{sC_1} + sL_1 + R_1\right) + \left(\frac{\omega^2 M^2}{sL_2 + R_2}\right). \tag{3.26}$$

Now, using equation (3.23), we can rewrite equation (3.26) in the following form,

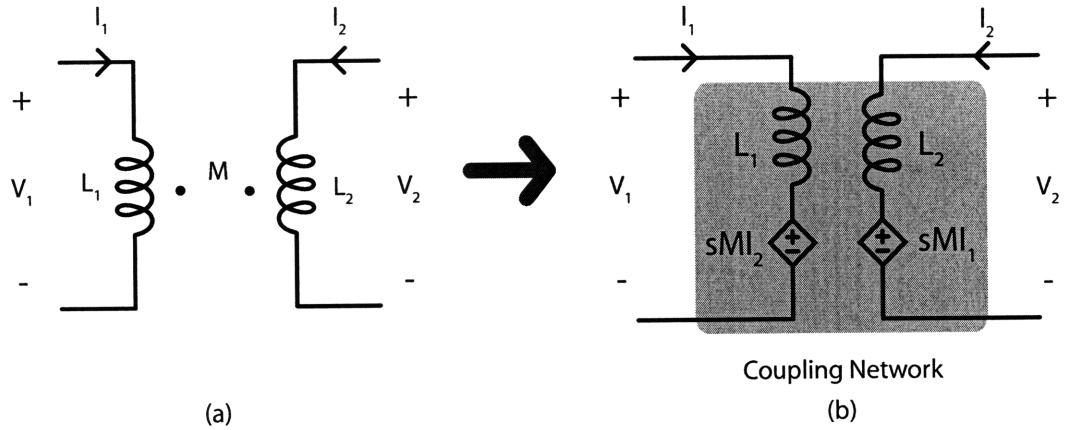

Figure 3-6: Schematic of a two-port model of magnetically coupled coils using a current-controlled voltage sources (CCVSs) to model the mutual inductance between the coils.

$$Z_{in,lowQ} = R_1 \left(1 + \frac{k^2 Q_1 \cdot \omega_0 L_2}{j\omega_0 L_2 + R_2 + R_{SW}}\right)$$

$$Z_{in,lowQ} = -sk^2 L_1 + R_1 \left(1 + k^2 Q_1\right). \tag{3.27}$$

There are two important observations that one can make from the result above:

- The imaginary part of the impedance, $sk^2 L_1$ can be absorbed into the inductance L_1. This serves to reduce the resonant frequency. However, since k^2 is in the order of 10^{-3} in most conditions, this frequency drift is negligible.
- The effective value of Q_2 is one. Since the capacitor has been shorted out, during each cycle, all the energy stored in the inductor L_2 is dissipated in the resistor R_2. Thus the real impedance seen by the input source remains R_1.

3.4 Feedback Coupled Resonator Model

The previous section illustrated a two port analysis method of coupled resonator circuit. While the results are valid, a more elegant method is the use of feedback to

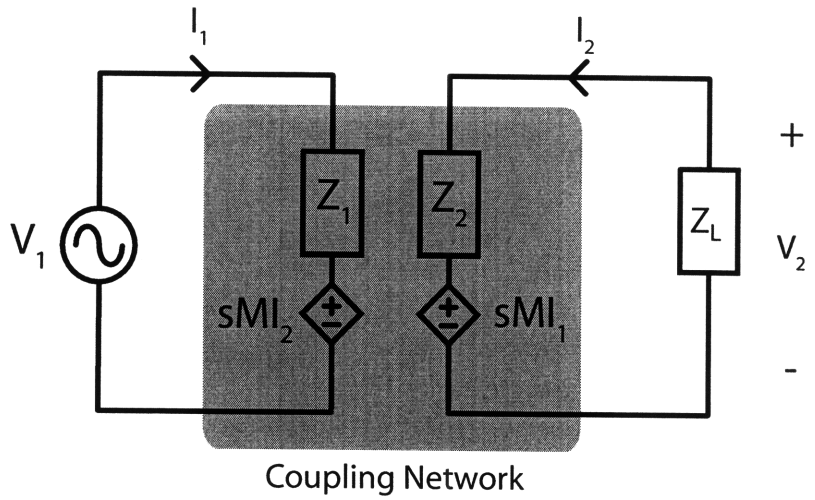

Figure 3-7: Two-port model of a magnetically coupled resonator pair.

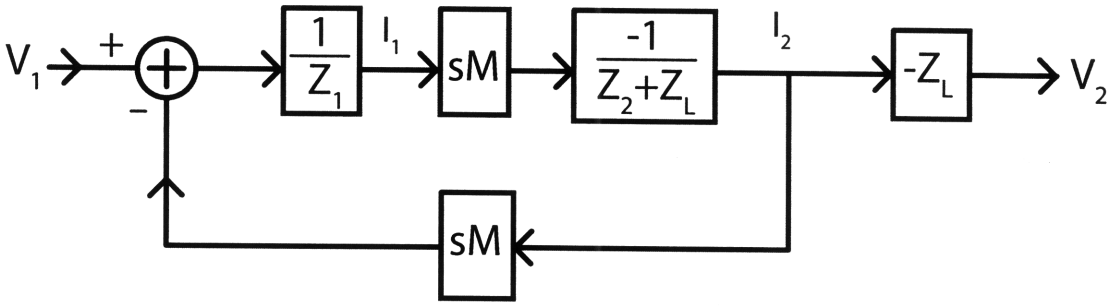

Figure 3-8: Two-port model of a magnetically coupled resonator pair.

analyze the magnetically coupled resonator system. A similar feedback model of a magnetically coupled resonators system was used to analyze optimal power transmission conditions in an inductive power links in [3] . This model can also be used to analyze an impedance modulation link. We begin by developing a equivalent two-port electrical model of the magnetically coupled coils that will lend itself to easy manipulation using block diagrams commonly used to analyze systems with feedback.

From Equations (3.12) and (3.12), we see that the current in one half circuit induces a voltage in the other half circuit. Thus the mutual inductance can be modeled as a current-controlled voltage source (CCVS). This allows us to redraw the coupled coils as two individual circuits with dependent voltage sources as shown in Fig. 3-6. Using this model, we can redraw the magnetically coupled resonator system as illustrated in Fig 3-7.

Again, assuming that the primary resonator is driven by a time varying sinusoidal current source, i_{in}, we can draw the block diagram to obtain Z_in as shown in Fig 3-8. From this diagram, we can immediately write the input impedance as follows,

$$\begin{aligned} v_1 &= \left(R_1 + sL_1 + \frac{1}{sC_1}\right) i_1 + Mi_2 \\ &= i_1 \left(R_1 + sL_1 + \frac{1}{sC_1}\right) + \left(\frac{M^2}{R_2 + sL_2 + \frac{1}{sC_2}}\right). \end{aligned} \tag{3.28}$$

As before, assuming that both circuits are nominally operating near resonance and the resonant frequencies, ω_0 of both resonators are equal, we can write the impedance see by the input current source as,

$$Z_{in} = \frac{v_1}{i_1} = R_1 + \frac{M^2}{R_2 + sL_2 + \frac{1}{sC_2}}. \tag{3.29}$$

This expression is the same as the one obtained using the two-port model in the last section. However, the ease with which this can be obtained by using the feedback model makes this a worthwhile exercise.

3.5 Modulation Index

From the analysis in section (two-port analysis) above, we can observe that,

$$\begin{aligned} Tx_{bit=1} &: Z_{in} = R_1(1 + k^2 Q_1 Q_2) \\ Tx_{bit=0} &: Z_{in} = R_1. \end{aligned} \tag{3.30}$$

The modulation index, m, of this modulation scheme is given by,

$$m = k^2 Q_1 Q_2 \tag{3.31}$$

As described in [18], since the series resistances, R_1 and R_2 are small, as they are

merely the parasitic resistances of the coil, we can transform the primary resonator into a parallel configuration, then assuming that $w_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2}$, we can rewrite Z_in as,

$$Z_{in} \approx R_1(1+m)\left(\frac{Q_1}{1+m}\right)^2 = \frac{R_1Q_1^2}{1+m}. \tag{3.32}$$

Thus, the input impedance for the case where the transmitted bit is either one or zero is given by,

$$\begin{aligned} Tx_{bit=1} &: Z_{in} = R_1Q_1^2 \\ Tx_{bit=0} &: Z_{in} = \frac{R_1Q_1^2}{1+m} \end{aligned} \tag{3.33}$$

Therefore, the modulation index of the parallel resonator case is now,

$$m_{eff} = \frac{m}{1+m} \tag{3.34}$$

3.6 Downlink

In the case when data is being transmitted from the external primary to the internal secondary, the oscillation amplitude of the primary oscillator is modulated to encode the data to be transmitted. In this configuration, the switch S is kept open, so that the secondary resonator is also in the high-Q state. If the resonator is turned off to indicate a '0' bit and turned on to indicate a '1' bit, the voltage amplitude observed on the secondary is given by,

$$\begin{aligned} Tx_{bit=1} &: \frac{v_2}{v_1} = kQ_2\frac{L_2}{L_1} \\ Tx_{bit=0} &: \frac{v_2}{v_1} = 0 \end{aligned} \tag{3.35}$$

3.7 Data Coding

For uplink communication, the data is encoded using the non return to zero (NRZ) format. This allows us to use less bandwidth to transmit the same amount of information as in a return to zero (RZ) scheme. This is important as high bandwidth is required in the uplink.

For the downlink however, a RZ scheme is used. The donwlink data is Manchester coded. Since Manchester coding results in a transition during each bit, which can be used to clock the downlink data. This is crucial in reducing the power consumption of the secondary as a Phase Locked Loop (PLL), which usually consumes significant power, is not required for clock recovery. Since the downlink data will mainly be used for transmitting low bandwidth data such as programming information, the resulting drop in bandwidth due to the use of a RZ coding scheme is unimportant.

Chapter 4

External Primary Transceiver Design

4.1 Introduction

In the last chapter, the theoretical operation of a implantable, impedance modulation wireless data link was analyzed. In this section, one implementation of the external primary transceiver for such a wireless link is explored. SPICE simulation results of each of the blocks in the external transceiver is also presented.

4.2 System Block Diagram

The block diagram of the primary is shown in Fig 4-1. A Colpitts oscillator is used as the primary oscillator for this system. The inductor used in the Collpits oscillator is implemented using an off-chip coil on a printed circuit board (PCB), which is used to magnetically couple the RF energy to the secondary coil.

During uplink data transmission (from the secondary to the primary), the output of the Colpitts oscillator is fed into a differential envelope detector. The differential envelope detector tracks the positive and negative envelope of the output of the Colpitts oscillator. The envelope of the oscillator output is modulated by the time varying effective resistance of the Colpitts' RLC tank due to the varying Q_2 of the

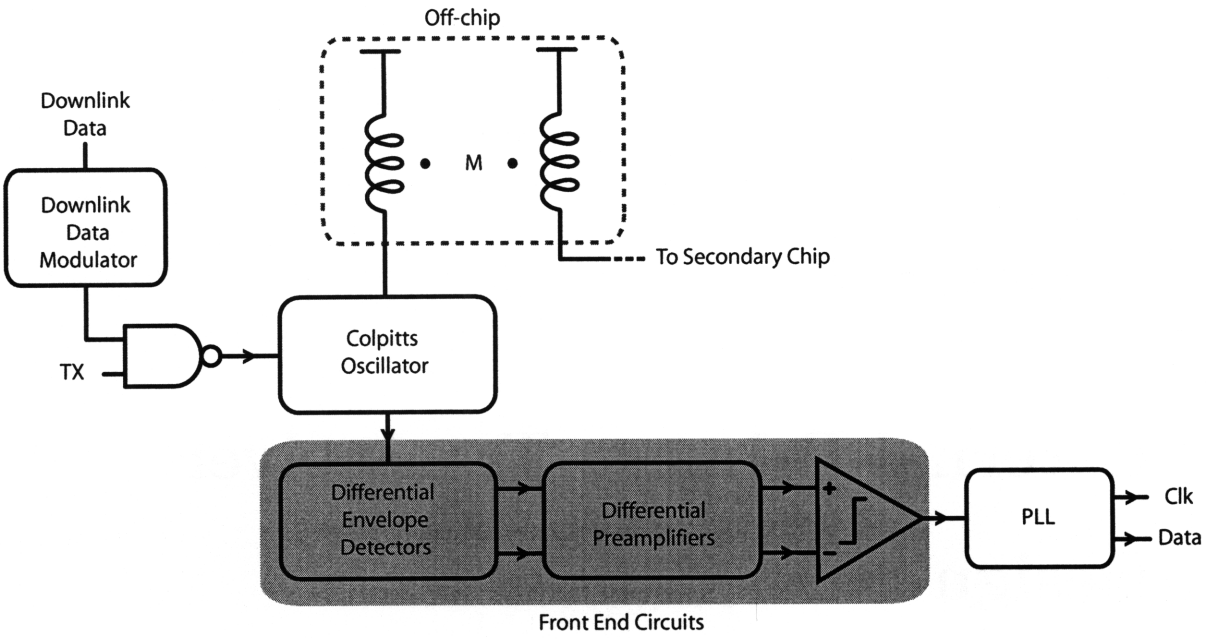

Figure 4-1: Block Diagram of the Primary Transceiver Chip

secondary resonator as analyzed in the previous chapter.

Under nominal operating conditions (i.e. with a link distance of a few centimeters), the coupling coefficient, k, can be expected to be very small and in the order of 5^{-2}. This will result in the modulated envelope of the oscillator output to be very small (in the order of 10s of millivolts). Thus, the evelope detector outputs are first amplified using a differential preamplifier.

The amplified version of the positive and negative envelopes are then passed into a comparator. The comparator flips whenever the positive and negative envelopes intersect. The output of the comparator is essentially the transmitted data, however, since NRZ modulation is used for the uplink to minimize bandwidth, the clock will need to be recovered from the data using a a PLL. The PLL then outputs the retimed data stream including the recovered clock.

During downlink data transmission (from the primary to the secondary), the data to be trasmitted is Manchester coded. The oscillation amplitude of the Colpitts oscillator is modulated according to the Manchesterd coded data essentially by turning it on and off. This varying oscillation amplitude is then coupled to the primary, where it can then be decoded.

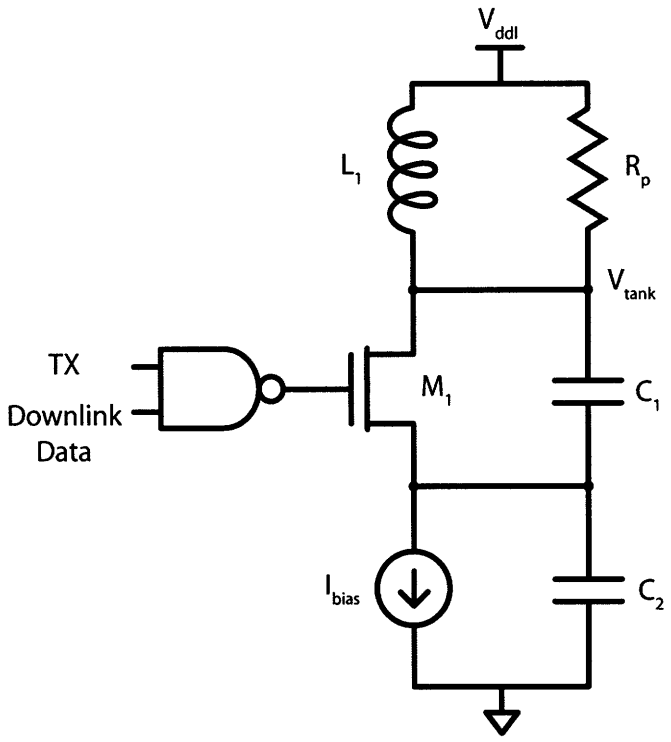

Figure 4-2: Canonical Circuit Schematic of a Colpitts Oscillator

4.3 The Colpitts Oscillator

A variety of LC oscillator topologies can be used to implement the oscillator in the primary. However, a Colpitts oscillator is ideally suited for this application because the oscillation amplitude of a Colpitts oscillator can easily be controlled by varying the bias current through the oscillator. This is desirable in cases where the coupling coefficient k between the primary and secondary coils is large such that the modulation index m is larger than necessary to achieve a particular bit error rate (BER) of the communication link. The oscillation amplitude can then be decreased to save power i.e. the power consumption of the Colpitts oscillator can be modulated based on the BER of the received data such that only minimum required amount of power is consumed in the the oscillator. This is particularly pertinent since a significant percentage (up to 75% in some cases) of the total power consumption of the primary is consumed by the Colpitts oscillator.

In order to see how the bias current can be used for amplitude control, we will need to first analyze the Colpitts oscillator. However, since oscillations are large signal

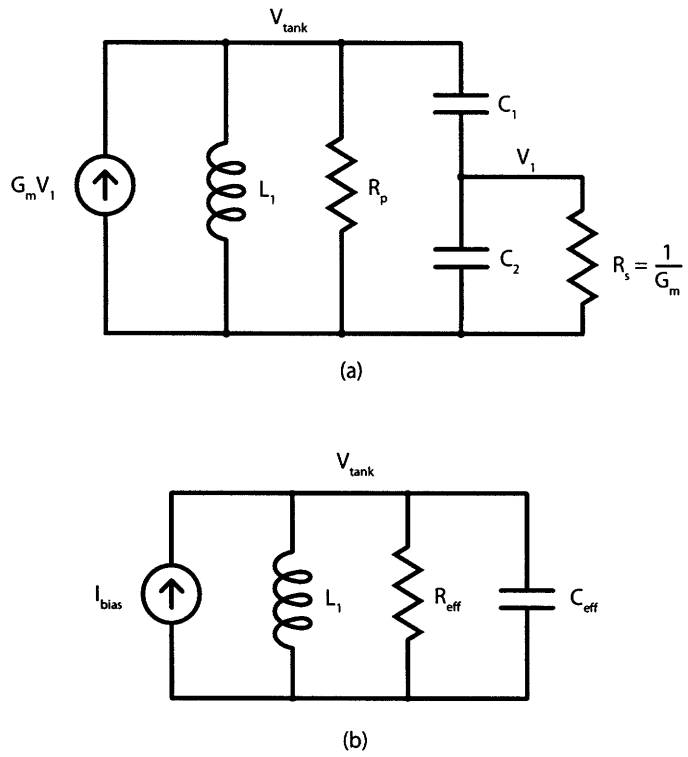

Figure 4-3: (a)Describing Function Model of the Colpitts Oscillator, and (b)a Simplified Model of the Colpitts Oscillator

phenomena, small signal analysis cannot be directly applied and describing function methods will need to be used [8]. The canonical circuit schematic of a CMOS variety of the Colpitts oscillator is shown in Fig 4-2. The resistance R_p is the series parasitic resistance of the inductor. Close to the resonant frequency, R_p is given by,

$$R_p \approx R_s(Q^2 + 1). \tag{4.1}$$

For inductors with a reasonable Q, R_p is usually very large and is in the order of $k\Omega s$.

A describing function model of the Colpitts oscillator is illustrated in Fig 4-3(a). Assuming that the gate of M_1 is ac ground, the transistor can then be represented by a resistor R_s and a transconductance generator, modeled using a VCCS in Fig 4-3(a). However, the transistor also loads the tapped capacitor circuit, and this loading due to the impedance observed at the source of M_1 is modeled using the resistor $1/G_m$ connected to the node V_1. This representation is essentially equal to the small signal model of the Colpitts oscillator with one important difference. The transconductance

of M_1 is denoted by G_m, the large signal transconductance of the transistor obtained from describing function analysis, and not g_m, the small-signal transconductance commonly used in circuit analysis. From describing function analysis, G_m is given by,

$$G_m = \frac{2I_{bias}}{V_1}. \tag{4.2}$$

The describing function model can be simplified further by combining R_s with R_p of the resonant tank. This can be done by observing that the tapped capacitor operates much like an impedance transformer. Similar to an analysis of regular transformers while assuming that C_1 and C_2 are purely reactive, the equivalent resistance across both C_1 and C_2 due to R_s can be obtained using energy conservation arguments. This transformed resistance, $R_{s,tran}$ is given by,

$$R_{s,tran} = \frac{R_s}{n^2}, \tag{4.3}$$

where n, the capacitor voltage divider is defined to be,

$$n \equiv \frac{C_1}{C_1 + C_2}. \tag{4.4}$$

If we assume that the tapped capacitors merely serve to divide V_{tank} down to V_1, where $V_{tank} \approx V_1/n$ the circuit in Fig 4-3(a) can be simplified further as none of the variables are dependent on V_1, the circuit can be simplified further to a regular driven RLC circuit as shown in Fig 4-3(b), where the effective device parameters and resonant frequency are given by,

$$\begin{aligned} R_{eq} &\approx R_p \| \frac{1}{n^2 G_m} \\ C_{eq} &= nC_2 \\ w_0 &= \frac{1}{\sqrt{LC}} \end{aligned} \tag{4.5}$$

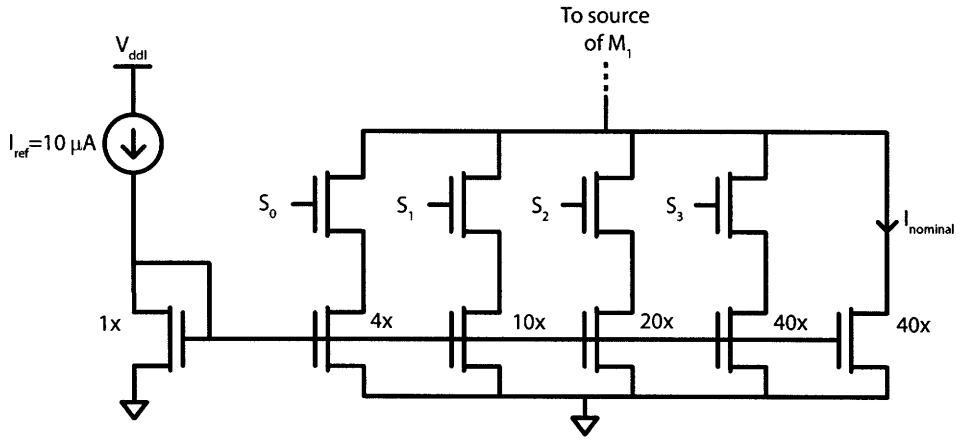

Figure 4-4: Four-bit, binary-weighted current DAC used to implement I_{bias}. The last branch is used to supply the minimum current required to ensure that the Colpitts oscillator starts-up.

After some algebra, V_{tank} at the resonant frequency w_0 can be written as [16],

$$V_{tank} = 2I_{bias}R(1-n) \tag{4.6}$$

From equation (4.6), we see that V_{tank} is directly proportional to I_{bias}. Thus, the amplitude of oscillation can be directly controlled by changing I_{bias}. In our implementation, the current source I_{bias} is controlled using a four-bit, binary-weighted current DAC as shown in Fig 4-4. However, in order to ensure that the oscillator starts-up, the loop transmission of the oscillator will need to be greater than unity. This imposes a minimum small-signal transconductance, g_m, for the oscillator which can be written as,

$$g_m > \frac{1}{R_p(n-n^2)}. \tag{4.7}$$

To ensure that steady state oscillations can be achieved, a minimum bias current of 400 μA is used, which is implemented with the current mirror without the control switch as illustrated in Fig. 4-4. This minimum bias current can be increased up to 1.1 mA using the four-bit binary-weighted current DAC. The parameters used in our Colpitts oscillator is listed in Table 4.1 and SPICE simulation outputs at the lowest and highest current levels are shown in Fig 4-5.

Furthermore, as indicated in Table 4.1, the supply voltage, V_{ddl} used for the os-

Table 4.1: Colpitss Oscillator Parameters

Parameter	Value
f_{osc}	40 MHz
L_1	200 nH
C_1	98.9 pF
C_2	396 pF
n	0.2
V_{ddl}	0.9 V
Nominal I_{bias}	300 μA
I_{bias} DAC	4-bit binary weighted
I_{bias} Range	400 μA - 1.1 mA
V_{tank} Range	0.53 V - 1.17 V (V_{pp})

cillator is 0.9 V, which is half of the the system supply voltage, V_{ddh}, which is 1.8 V. This is done to further reduce the power consumption of the system, and the amplitude of oscillation does not depend significantly on the supply voltage, as long as all transistors are in saturation.

4.3.1 Inductor Design

In order to allow for magnetic coupling between the external and implanted chips, the inductor used in the Colpitts Oscillator in Fig 4-2 is implemented using a microstrip on a PCB. However, in order to be implantable, the coils used will need to be less than 2 cm on a side. This limits the size of inductance that can be used in the design of the Colpitts oscillator, which requires the use of larger on chip capacitors to achieve the necessary resonant frequency of the LC tank. The exact calculation of inductance of a square coil implemented using rectangular wire is algebraically complicated and can be found in [35]. However, in the case when the width of the microstrip trace is significantly smaller than the length of each side of the square coil (which is the case for microstrip coils), the inductance can be approximated by [32],

$$L \approx n^2 \cdot \frac{2\mu_0 D}{\pi}\left(sinh^{-1}\frac{D}{w} - 1\right), \tag{4.8}$$

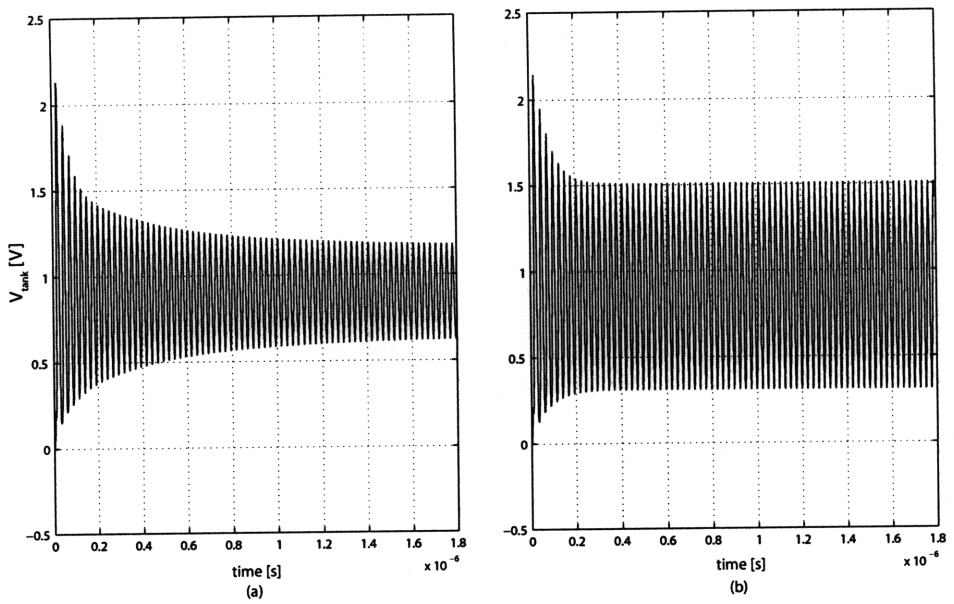

Figure 4-5: SPICE simulation output of the Colpitts Oscillator (a) at the minimum current level of 0.4 mA, and (b) at the maximum current level of 1.1 mA for I_{bias}.

where D is the length of the side of the square coil, w is the width of each trace, and n is the number of turns. For a coil with two turns, and a square of 2 cm on a side, and a trace thickness of 15 mils, this formula predicts an inductance of $L \approx 240$ nH.

A square coil with an inductance of 195 nH was designed and simulated using a method of moments technique in Agilent Advanced Design System (ADS). The layout of the coil is illustrated in Fig 4-6. The coil has two turns, with a microstrip trace thickness of 15 mils spaced 7 mils apart, and 730 mils on a side. The ADS simulation results are illustrated in Fig 4-7. Simulations indicate that the microstrip coil implemented on a FR-4 substrate is able to achieve a Q of approximately 60 at 40 MHz.

4.3.2 Positive Feedback in Colpitts Oscillators

In general, oscillators need one of two qualities to maintain steady-state oscillations, some flavor of non-linearity and a way to overcome the parasitic resistive losses that exist in all physical LC tanks. The resistive losses can be overcome either by using a negative resistance or a positive feedback scheme. The Colpitts oscillator is an example of a positive feedback based oscillator. This ensures that the poles of the

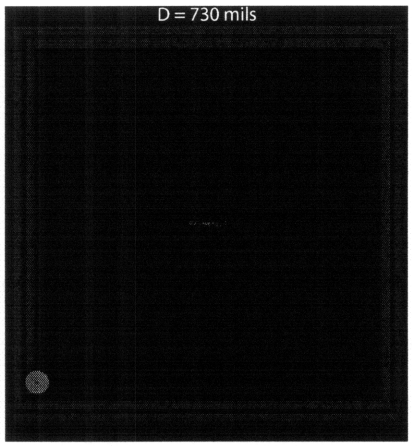

Figure 4-6: Layout of the microstrip inductor (L = 200 nH) used in the Colpitts Oscillator

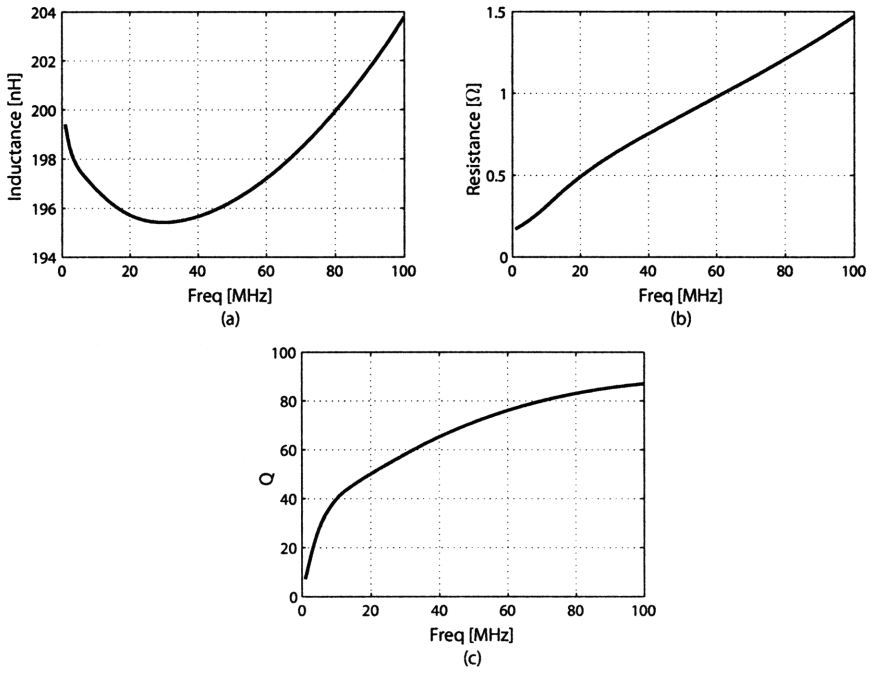

Figure 4-7: EM simulation results of the microstrip coil. Simulations were performed using Agilent ADS

loop transmission root-locus are pinned on the $j\omega$ axis, which results in sustained oscillations.

In the Colpitts oscillator, the non-linearity is provided by the non-linear large signal transconductance, G_m, of the MOS transistor. The positive feedback, however, is setup quite elegantly by the tapped capacitor. The tapped capacitor performs two functions simultaneously: 1) it transforms the the source impedance of M_1, and ii) it samples a fraction of V_{tank} to be fed back into the voltage control current source (VCCS) of M_1. From energy conservation arguments, since $P = \frac{V^2}{R}$, when the voltage across a resistor is halved, the resistance will need to fall by four times for energy to be conserved, as is conserved in a tapped capacitor circuit. Thus, while V_1 is a fraction n of V_{tank}, the impedance of the tank has increased by a factor of $\frac{1}{n^2}$, assuming that the resistance in the tank is dominated by the transformed source impedance of M_1, which is a good assumption for relatively high Q values of L_1. Therefore, the loop transmission is $L(s) \approx n \cdot 1/n^2 = 1/n$.

4.4 Front-end Circuits

4.4.1 The Differential Envelope Detector

By opening and shorting the switch in the secondary, the oscillation amplitude of the primary is modulated, according to the theoretical analysis presented in Section 3.3.1. An envelope detector can be used to track the amplitude variations, from which the transmitted bit can be determined using a comparator. However, the amplitude variation under weak coupling is expected to be very small due to the strong dependence of m_{eff} on k, a more robust method is required. Since both the positive and negative envelopes of the carrier is modulated, a differential envelope detector can be used to effectively double the envelope signal amplitude and aid the discrimination of a '1' bit from a '0' bit.

The envelope detector used is illustrated in Fig 4-8. Two CMOS diodes, M_1 and M_2 are used, but in different directions to allow for each branch to track either the

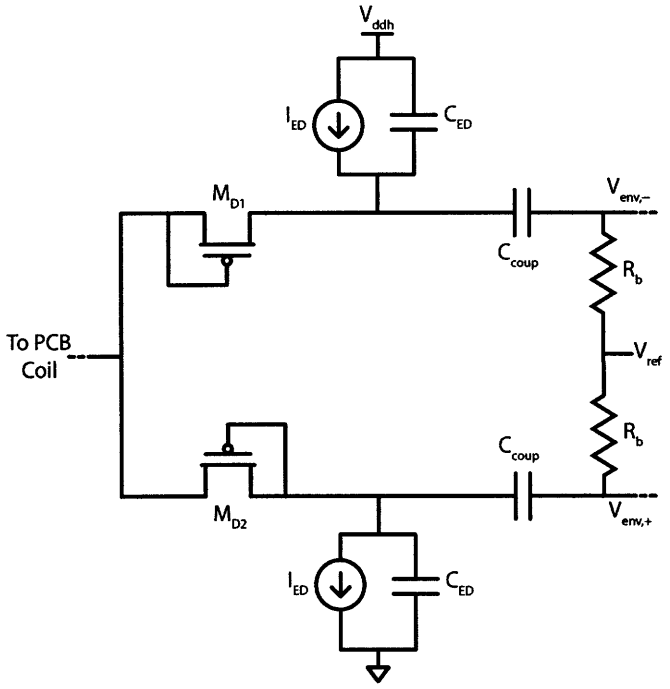

Figure 4-8: Differential envelope detectors to track the positive and negative envelope of the modulated oscillator output.

positive or negative envelope. A parallel RC low-pass filter is used to filter out the high-frequency RF components of the carrier. The RC time constant is implemented with a capacitor C_{ED} and leak current I_{ED} implemented using a MOS device. The effective corner frequency of the low-pass filter is given by,

$$f_{c,ED} = \frac{g_{m,ED}}{2\pi C_{ED}}$$

$$= \frac{I_{ED}}{2\pi C_{ED}\phi_t}, \tag{4.9}$$

where $\phi_t = kT/q$, the thermal voltage. The carrier frequency used in this design is 40 MHz, while the maximum data rates that the system is designed to handle is ≈10 MHz. This close proximity of the maximum modulation frequency from the center frequency causes a predicament in choosing appropriate values for C_{ED} and I_{ED}. If the cutoff frequency is close to the carrier frequency, not all of the signal components at the carrier frequency will be filtered out causing a high frequency ripple on top of

the envelope. The high frequency ripple is particularly detrimental as it can cause erroneous crossings between the differential envelopes, which translates into jitter in the data transition edge. On the other hand, having the cutoff frequency too close to the data modulation frequency will result in the filtering of the modulated envelope, resulting in lower signal amplitudes. Given these constraints, C_{ED} is chosen to be $1pf$, and I_{ED} is chosen to be 4 μA. This results in $f_{c,ED} = 25$ MHz.

Before the outputs of the differential envelope detectors can be used to determine the transmitted bit, the DC level of both signals will need to be equalized. This is done by using the high pass network implemented using C_{coup}, used to ac couple the signal from the envelope detectors, and R_b shown in Fig 4-8. The value of C_{coup} and R_b used is 10 pF and 900 kΩ respectively. Given these device values, the corner frequency of this network is 17 kHz. This relatively low cut-off frequency is chosen to ensure that for long runs of zero's or one's the envelope signal is not significantly attenuated by this RC network.

4.4.2 Differential Pre-amplifier

For nominal values of the coupling coefficient, the signal amplitude of the output of the two envelope detectors are in the order of 20-30 mVs. This small signal will need to be amplified before they can be fed into a comparator to determine the transmitted bit. The output of the envelope detectors are amplified using a resistively loaded, differential pair. A differential pair is used to reject any disturbance that is common to both envelopes such as the high frequency ripple of the RF carrier. Another benefit of using a differential amplifier here is that it consumes significantly less power than using an operational amplifier with resistive feedback for amplification [18].

The resistively loaded, differential amplifier is illustrated in Fig 4-9. The gain of the amplifier is simply given by $A_v = g_{m,diff}R_d$. The value of R_d used is 200 kΩ. However, since more or less gain may be needed depending on the coupling strength between the coils, the tail current source is implemented using a two-bit current DAC. The current through the pre-amplifier can be varied from $15 - 30\mu$A in three equally-weighted steps. Therefore, the effective gain of the pre-amplifier can be varied from

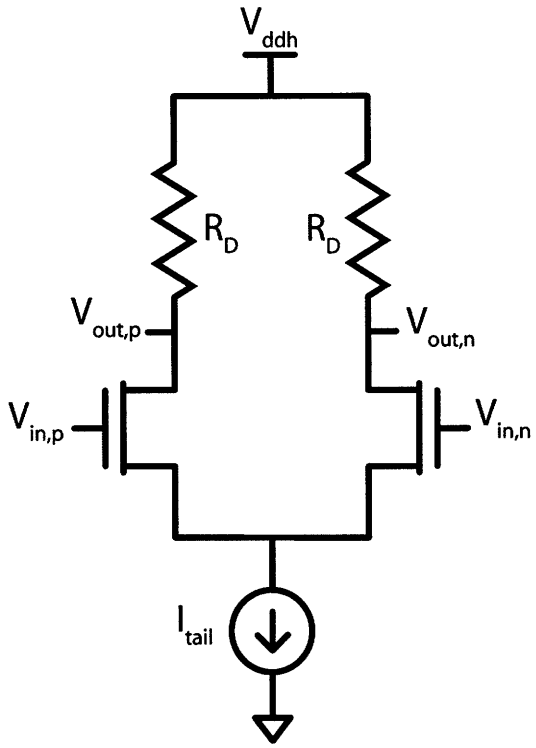

Figure 4-9: Schematic of the pre-amplifier implemented using a resistively loaded, differential pair.

$5 - 20$.

As illustrated in Fig 4-1, the output of the differential pre-amplifier is fed into a comparator which determines if a bit '1' or bit '0' was transmitted. A simple five transistor op-amp was used to implement the comparator. As we discussed earlier, since the RF carrier is spectrally close to the maximum modulation frequency, it is possible to have erroneous transitions in the output of the comparator. Hence, a hold timer is used to remove pulses that are significantly shorter than one bit period at the maximum expected uplink data rate of 10 Mbps. The hold timer works in conjunction with the comparator to produce a hysteric comparator which has a built in delay between successive transitions. The schematic of the hold timer is shown in Fig 4-10. This hold timer uses two current-starved inverters, instead of just one as in [18]. The second inverter is used to speed up the output of the first inverter loaded with capacitor C_L. This is done to save power because slowly varying inputs when fed into a Schmitt trigger results in large currents through the Schmitt trigger during time when the input signal is between the low and high trip points of the Schmitt

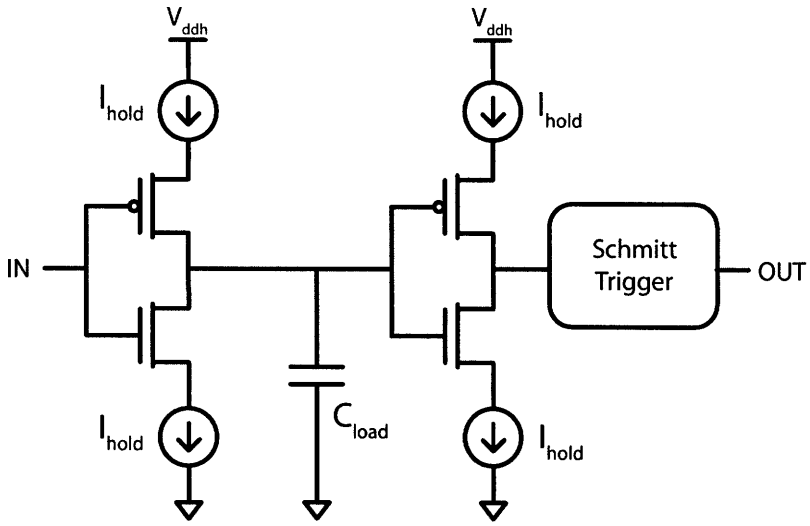

Figure 4-10: Schematic of the hold timer used to remove erroneous pulses that are significantly shorter that one bit period at the maximum expected data rate of 10 Mbps. With a $C_{load} = 10\text{pF}$ and $I_{hold} = 6\mu\text{A}$, pulses shorter than 15 ns are rejected.

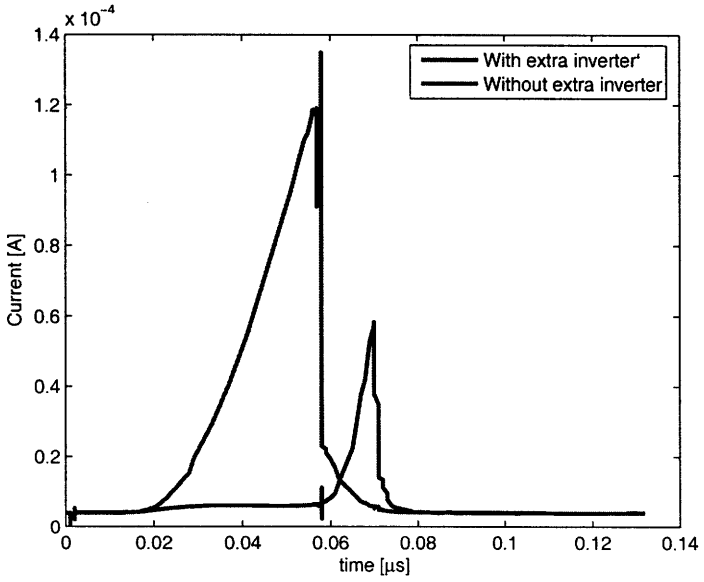

Figure 4-11: Simulations results of both flavors of hold timers, with and without the extra inverter stage right before the Schmitt Trigger. The red curve shows that the hold timer without the extra inverter draws significantly more current than the hold timer with the extra inverter stage.

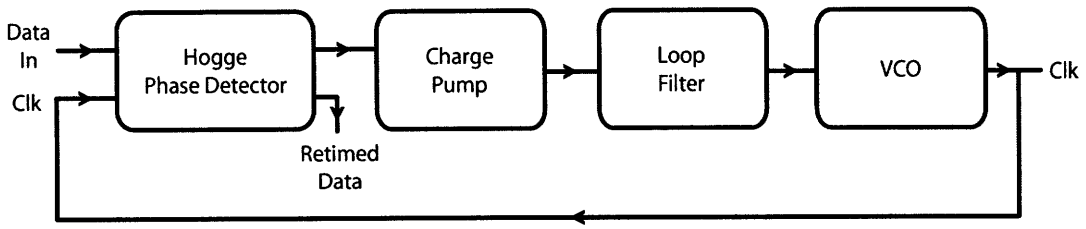

Figure 4-12: Block Diagram of the PLL used to recover the clock from the uplink data stream.

trigger. Simulation results of both flavors of hold timers, with and without the extra inverter stage is shown in Fig 4-11. The dead zone for each transition is then given by,

$$t_{trip} = \frac{C_L V_M}{I_{INV}}, \tag{4.10}$$

where V_M is the switching threshold of the inverted and is assumed to be close to the mid-rail of the power supply. $C_L = 0.1\text{pF}$ and $I_{INV} = 6\mu\text{A}$ was chosen such that the dead zone was 15 ns, which results in any pulse shorter than 15 ns being suppressed.

4.5 The Phase-Locked Loop

The uplink data is encoded in NRZ form to allow for higher data rates for a given link bandwidth than that would be possible when using a purely RZ encoding strategy. This is because an RZ encoding scheme will result in the transmitted data stream having shorter pulses for any particular data rate in order accommodate the extra clock transition edge within each bit, thus requiring a larger link bandwidth. However, when NRZ encoding is used, a PLL is needed to recover the clock from the transmitted data stream. A block diagram of the PLL is shown in Fig 4-12.

4.5.1 Hogge Phase Detector

The schematic of a Hogge phase detector is illustrated in Fig 4-13. Given that NRZ encoding is used, when successive runs of the same bit is being transmitted, there will not be any edges in the incoming data stream. If a sequential phase detector is used, missing edges will be interpreted as a change in frequency and the PLL will

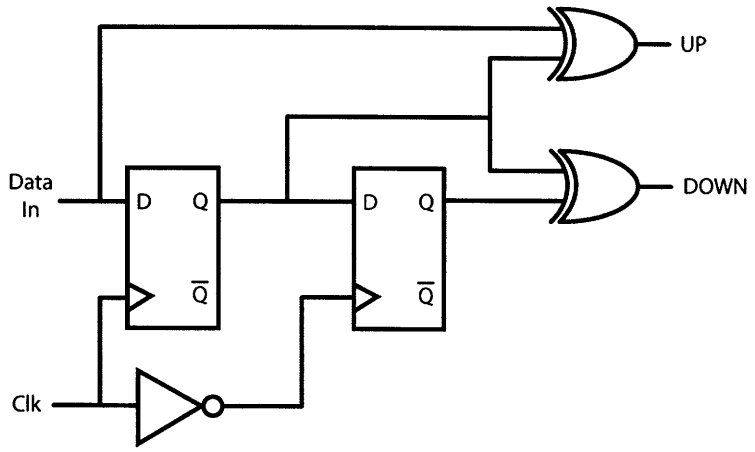

Figure 4-13: Schematic of the Hogge Phase Detector.

attempt to 'correct' and lock to a lower frequency, thus resulting in bit errors. The output Hogge phase detector, however, goes high then low for half the clock cycle each when a missing edge on the data stream in detected. If the clock is assumed to have a 50% duty cycle, then the high and low times of the Hogge phase detector is equal resulting in the same amount of charge being injected and removed from the loop filter. Thus, the loop will still remain in lock. A more detailed discussion of the Hogge phase detector can be found in [16].

4.5.2 Charge Pump and Loop Filter

The schematic of the charge pump and loop filter is shown in Fig 4-14(a). The charge pump uses a differential topology that helps mitigate differential switching errors. Cascoding is also used to improve the output impedance of the charge pump. V_{ref} is nominally set to the middle of the supply voltage.

The loop filter is implemented using passive components as shown in Fig 4-14(b). The R_1C_1 pair is used to set the dominant pole of the loop filter and a high frequency zero near the crossover frequency such that the loop has a reasonably large phase margin (PM) at the crossover frequency to ensure loop stability. R_2, C_2 and C_3 are used to set two higher order poles beyond the crossover frequency. These poles are used to further suppress high-frequency spurs and produce a smoother output to drive the VCO, which will result in higher frequency stability when the PLL is in lock. The

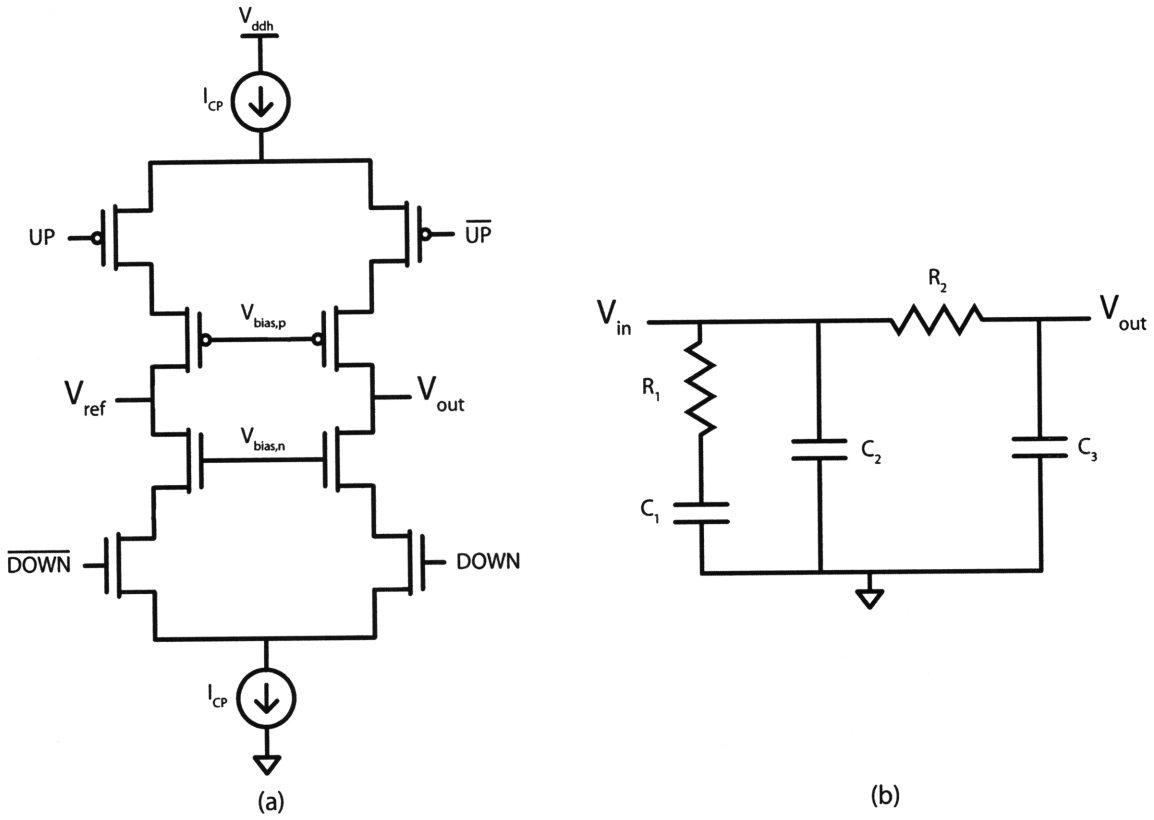

Figure 4-14: (a)Schematic of the charge pump used in the PLL. V_{ref} is nominally set to the mid-rail supply voltage, and (b)Schematic of the third order loop filter.

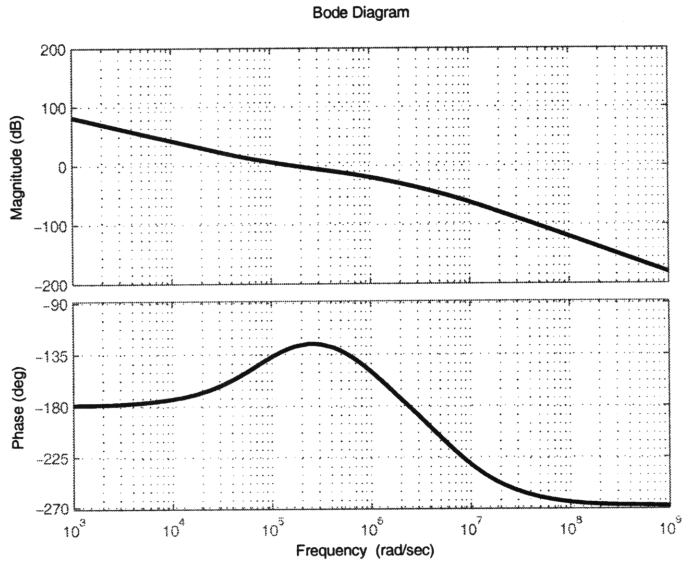

Figure 4-15: The magnitude and phase bode plot of the PLL

Table 4.2: Loop Filter Parameters

Parameter	Value
R_1	$140k\Omega$
R_2	$500k\Omega$
C_1	$216pF$
C_2	$2pF$
C_3	$2pF$

loop filter is designed to set the loop crossover frequency of the complete PLL at $27kHz$ with a phase margin of 53°. The low PLL loop crossover frequency is chosen to minimize frequency drift when the PLL is in lock while trading off speed of lock acquisition. The slower resulting lock acquisition is tolerable since the data rate is preset and can be expected to be relatively fixed over time. The Bode magnitude and phase plot of the loop transmission for the PLL, including the VCO which will be discussed in the following section is illustrated in Fig 4-15 showing loop stability at the crossover frequency. The values of the passive components used in the loop filter are given in Table 4.2. During reset, the voltage of C_1 can be set to V_{ref}, which is nominally set to the mid-rail voltage. However, this voltage can be varied to aid acquisition by setting it closer to the expected output voltage required for lock at a particular input data frequency.

4.5.3 Voltage Controlled Oscillator

The VCO used in the PLL consists of two circuit blocks, namely a $V \rightarrow I$ converter and a current controlled oscillator (CCO). The schematic of the $V \rightarrow I$ converter is shown in Fig 4-16. The CCO consists of a three stage, current-starved ring oscillator as shown in Fig 4-17. The CCO was chosen to implement the oscillator for two reasons: 1) the oscillation frequency of a CCO is easily controllable by simply changing I_{cco} and ii) the CCO gain constant, $K_{O,i} = df/dI_{starve}$, is very linear of over large frequency ranges. However, one challenge in using a CCO as the oscillator is that the output of the loop filter is a voltage. Hence, a $V \rightarrow I$ stage is needed before the output of the loop filter can be used to drive the CCO. This $V \rightarrow I$ conversion is implemented

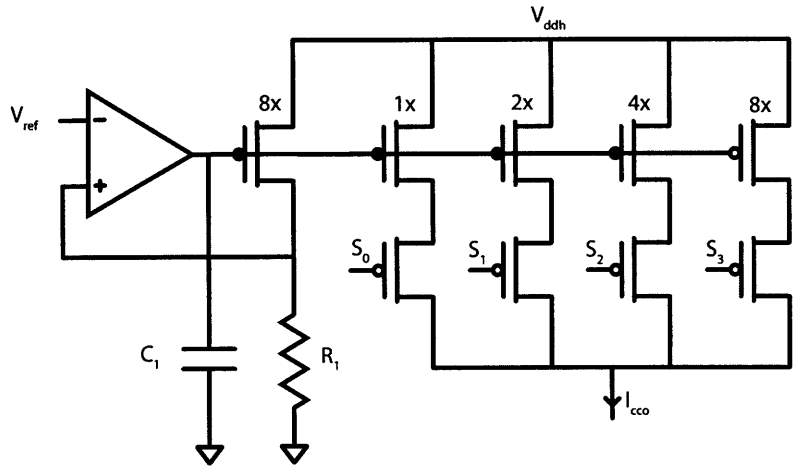

Figure 4-16: Schematic of the V→I converter used in the VCO, which is used to convert the voltage output of the loop filter into a proportional current to drive the current controlled ring oscillator

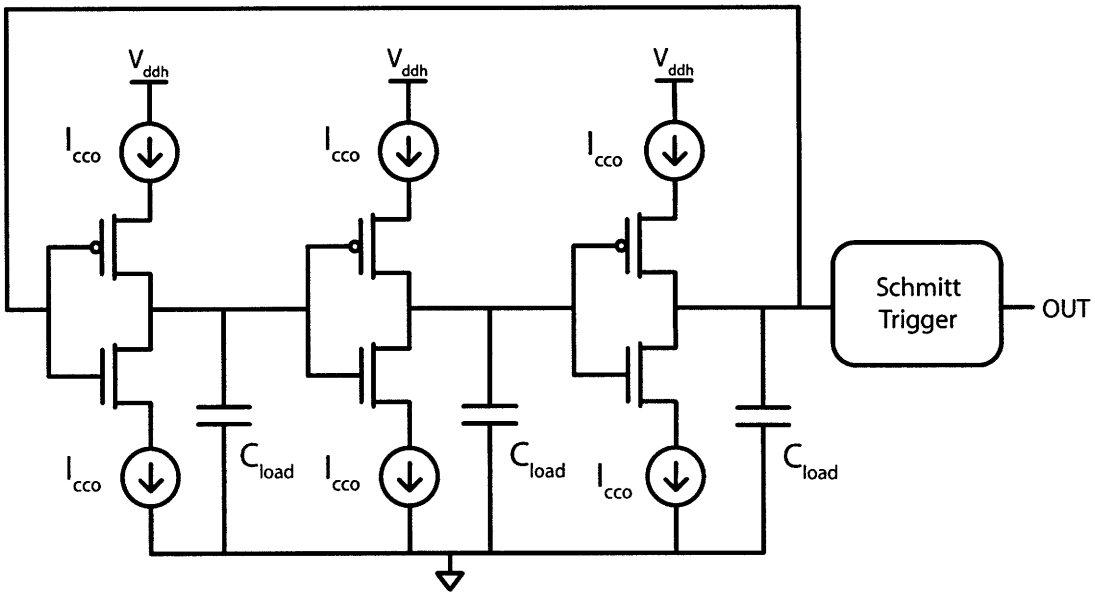

Figure 4-17: The current controlled oscillator used in the VCO. I_{CCO} is generated by the V→I converter. The value of C_{load} used here is 120fF

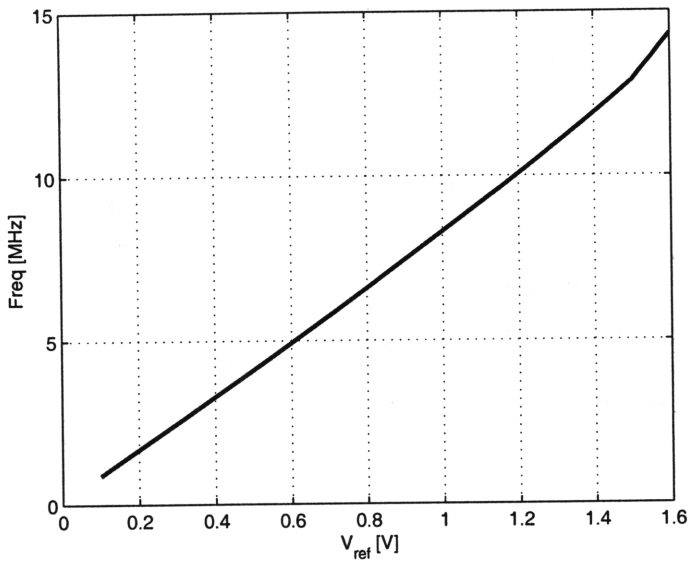

Figure 4-18: Output frequency vs. input voltage of the VCO showing linear behavior over large input voltages

using an op-amp, transistor M_1, and a resistor R_1 as shown in Fig 4-16 [11]. The op-amp is used to control the current flowing through M_1 such that the voltage drop across R_1 due to the current through M_1 is equal to the input voltage, V_{ref}. As long as the input voltage to the op-amp does not exceed the linear range of the op-amp, the V to I conversion is quite linear, and will result in a linear VCO behavior over large frequency ranges. Fig 4-18 illustrates the linearity of this VCO over a large input voltage range. The capacitor C_1 is needed to provide a low-pass cutoff to filter out ripple in the output of the op-amp, which ensures stability at high frequencies. R_1 is chosen to be equal to $125k\Omega$ such that the nominal current through M_1 when V_{ref} is mid-rail is equal to the desired center frequency of the CCO output, which is equal to about 5 MHz in our case. However, to provide more flexibility, the current to the CCO is mirrored through a 4-bit binary-weighted DAC. This effectively allows one to change the center frequency of the CCO (i.e. the frequency of oscillation when V_{ref} is at the middle of the supply voltage) without changing the K_0 of the VCO. This is important in ensuring that the loop dynamics is preserved when the nominal current through the CCO is altered.

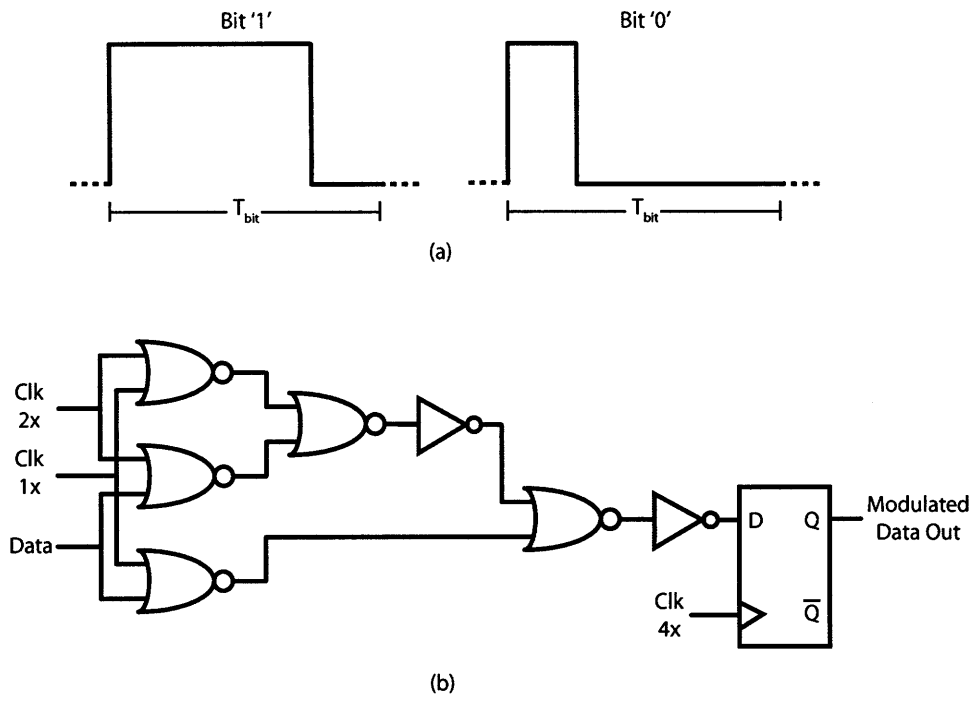

Figure 4-19: (a) Waveform for the RZ scheme used in the downlink. A square pulse with either 75% or 25% duty cycle is used to represent a bit '1' or bit '0' respectively. (b) Schematic of the on-chip RZ data modulator.

4.6 Downlink

As discussed earlier, the downlink data bandwidth will be considerable lower than the required uplink data bandwidth because the downlink will mainly be used to transmit programming and control data. Hence, a RZ coding scheme is used for the downlink in order to significantly simplify the data and clock recovery circuits required in the implantable secondary. Since in a RZ coding strategy, the clock edge is always present in each bit, a PLL is not required in the secondary, which significantly reduces the power consumption and complexity of the implanted secondary.

4.6.1 Downlink Data Modulator

The downlink data is modulated using the following method: for a bit '1', a 75% duty cycle square wave pulse is used, while for a bit '0', a 25% square wave pulse is used. The waveform for each bit is illustrated in Fig 4-19(a). An on-chip modulator generated the RZ modulated waveform from the input data stream, and a clock

running at 4 times the input data rate and generates the corresponding RZ output data stream. The schematic of the onboard data modulator is shown in Fig 4-19(b).

4.7 Power Reduction During Downlink

When data is being transmitted to the implantable secondary, all receiver circuits are turned off. This is done by turning off the current mirrors to all devices that consume static power such as the envelope detectors, differential pre-amplifiers, comparator, and the PLL.

Chapter 5

Implantable Secondary Transceiver Design

In the last chapter, the design of the external primary transceiver was explored. In this section we explore the design of the implantable secondary transceiver. Since the secondary transceiver will be implanted, minimizing power consumption and reducing the overall complexity of the system design will be paramount.

5.1 System Block Diagram

The block diagram of the implantable secondary transceiver is illustrated in Fig 5-1. An external coil (implemented on a PCB using microstrip traces) is used in the resonant LC tank to magnetically couple with the primary coil.

During uplink data transmission, TX is set high and the data is used to turn on or off a switch that shorts out the coil, to effectively modulate the Q of the secondary resonant tank between the nominal loaded value of Q_2 and unity.

During downlink data transmission from the external primary to the internal secondary, the resonant tank is left in the high-Q state. An envelope detector is used to track the envelope of the OOK modulated RF signal coupled into the secondary coil from the primary oscillator. Since the downlink data is encoded in RZ, PWM format, the envelope is detector output is then fed into a pulse-width demodulator

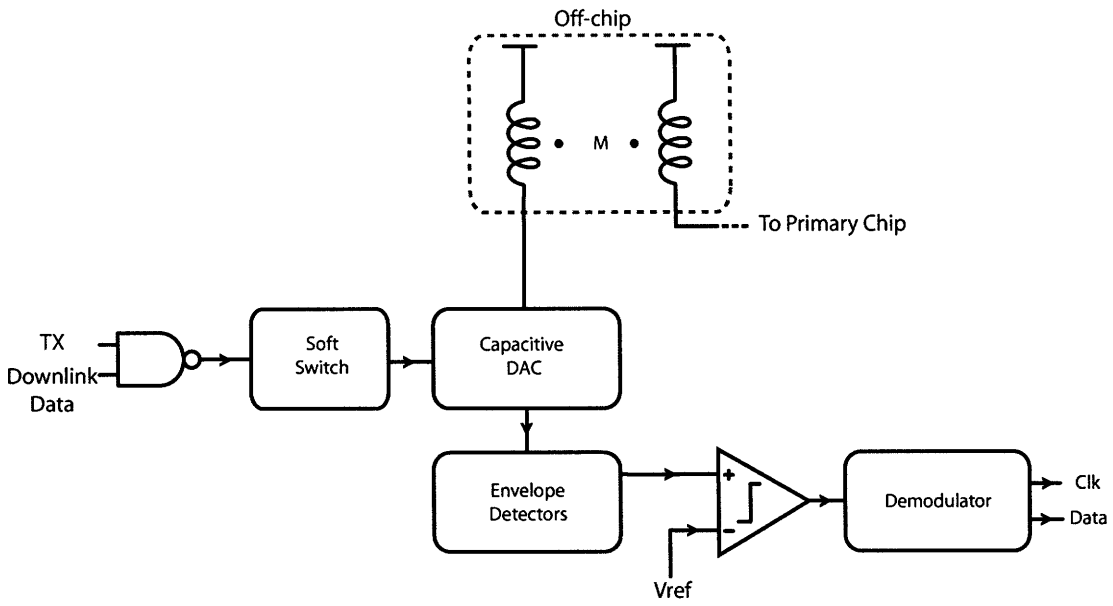

Figure 5-1: Block diagram of the secondary transceiver chip.

circuit to recover the transmitted bit and the corresponding clock stream.

5.2 Resonant LC Tank

The resonant LC tank is the core of the secondary transceiver and is illustrated in Fig 5-2. During uplink data transmission, TX is set high, and the data is used to turn the MOS switch M_1 on and off. This then modulates the Q of the secondary between the high-Q value, which is essentially the loaded Q of the inductor when the switch is turned off, and unity when the switch is turned on. This modulation then appears as a reflected impedance in the primary, leading to a modulation of the carrier amplitude as described in Section 3.3.1.

During downlink data transmission, TX is held low, which turns off the switch M_1. This sets the secondary resonant tank in the high-Q state, and the RF signal from the magnetically coupled to the secondary coil will appear as a voltage signal at the node V_{out}. This received RF signal can the be fed into an envelope detector and the pulse-width demodulator circuit to recover the transmitted data and associated clock edge.

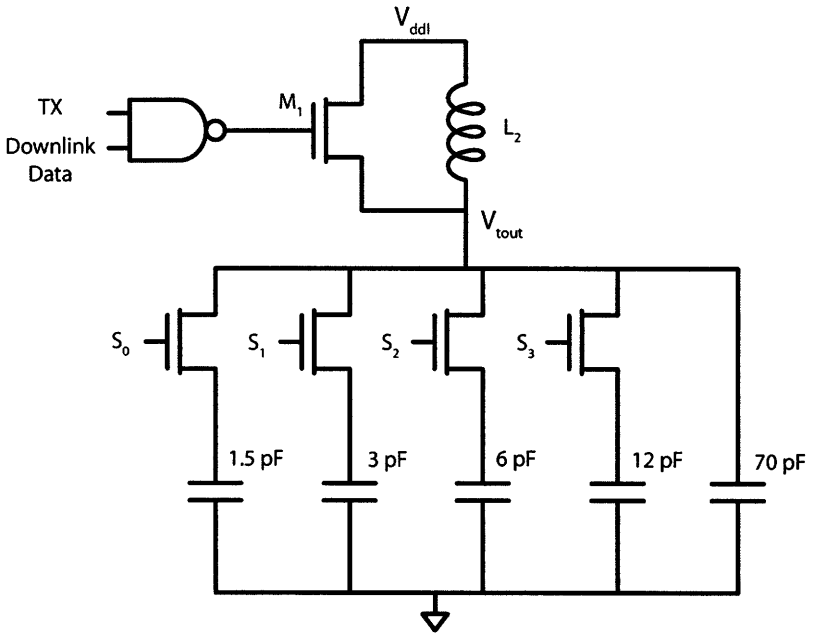

Figure 5-2: Schematic of the secondary resonant LC tank.

5.2.1 Resonant LC Tank Design

In order to simplify the design, the LC tank used in the secondary and illustrated in Fig 5-2 is electrically similar to the resonant tank of the Colpitts Oscillators as described in Section 4.3. Hence, the inductance of the coil is 200nH while the capacitance used to resonate out the coil inductance at the resonant frequency is the series combination of capacitors C_1 and C_2 of the Colpitts Oscillator. This effective capacitance is given by,

$$C_{eff} = \frac{C_1 C_2}{C_1 + C_2}.$$

For the values of C_1 and C_2 used in the primary, $C_{eff} \approx 76pF$.

However, as can be seen in Fig 5-2, a capacitive DAC is used to implement the capacitor in the secondary. This is done to essentially provide the secondary with a tuning range (i.e. the capacitive DAC allows the resonant frequency of the secondary to be varied over a set range of frequencies around the nominal operation frequency of 40 Mhz). While SPICE simulations allow the designer to approximate the oscillation frequency of the external oscillator, various factors can contribute to the deviation of the actual oscillation frequency from that predicted by SPICE. Some major factors

that may contribute to this frequency deviation are as follow:

- Variation of on the on-chip capacitors that are used in conjunction with the external coil to set the oscillation frequency of the Colpitts oscillator. For the process used, there can be up to 15% error in the on-chip capcitor values.
- Variation of the external coil inductances. While ADS EM simulations are used to design the PCB coils, deviations of up to 20 % have been observed between the simulated and measured coil inductance values.
- Effects of operating conditions. All simulations assume ideal operating conditions similar to that of free space. However, when the coils are used close to skin, extra parasitic reactances can cause the actual oscillation frequency of the external oscillator to deviate from the expected nominal value.

The reasons above illustrate the need for tunability in the resonant frequency of the secondary coil, in order to ensure maximize the magnetic coupling between the coils in the primary and secondary resonant tanks. With the values of capacitors used in the capacitive DAC as shown in Fig 5-2, the resonant frequency of the secondary resonant tank can be varied from 37 MHz to 42.5 MHz in 16 steps.

5.3 Soft Switch

5.3.1 Pulse-width Distortion

While all that is required for uplink data modulation is that the switch M_1 is turned on and off, in Fig 5-1, we see that the data first passes through a block called the soft switch. The soft switch is used to reduce the BER of the uplink data transmission.

One source of bit errors is due to the pulse width distortion of the amplitude of the RF carrier. When the internal resonant tank switches from a low-Q state to a high-Q state indicating that the bit '1' is being transmitted (with the previous bit transmitted being '0'), we see that the envelope detector output waveform in the primary has an exponential rise time behavior. as shown in Fig 5-3(a).

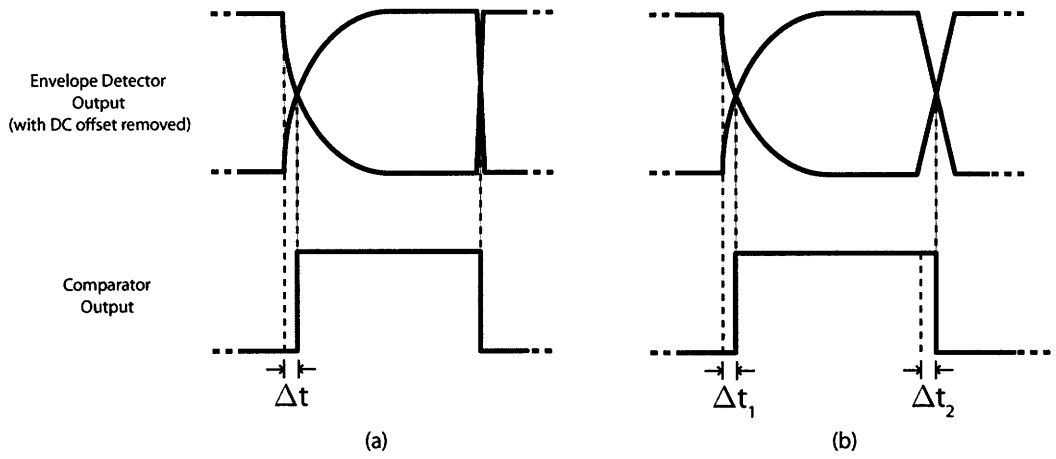

Figure 5-3: Representative waveforms illustrating the effects of PWM distortion due to the exponential rise time of envelope amplitude when the secondary switches from a low-Q state to a high-Q state in two different configurations: a) without the soft switch and b) with the use of the soft switch. If $\Delta t_2 \approx \Delta t_1$, then the effect of the pulse-width distortion can be nullified.

Conversely, when a bit '0' is transmitted right after a bit '1', Q_2 switches almost immediately between the high-Q state to the low-Q state. The envelope detector output waveform in the primary also falls quickly. Thus, the fall time of the envelope detector output is significantly shorter than the rise time due to the absence of an exponential decay of the envelope detector output as illustrated in Fig 5-3(a).

The phenomena described above produces asymmetric rise and fall edges, which result in the comparator output for a bit '1' having slightly shorter pulse widths everytime a $0 \rightarrow 1$ transition occurs [18]. One way in which this pulse-width distortion problem can be solved is to artificially introduce a slower edge on the $1 \rightarrow 0$ transition such that an equal amount of delay is added to the falling edge of the comparator output as shown in Fig 5-3(b). If $\Delta t_2 \approx \Delta t_1$, then the effect of the pulse-width distortion is effectively nullified.

5.3.2 Soft Switch Architecture Using a Resistive DAC

The soft-switch circuit schematic is shown in Fig 5-4. The soft-switch is essentially an asymmetric current-starved inverter. On the output rising edge of the inverter, the charging current is not limited, and the output will rise as fast as possible with the

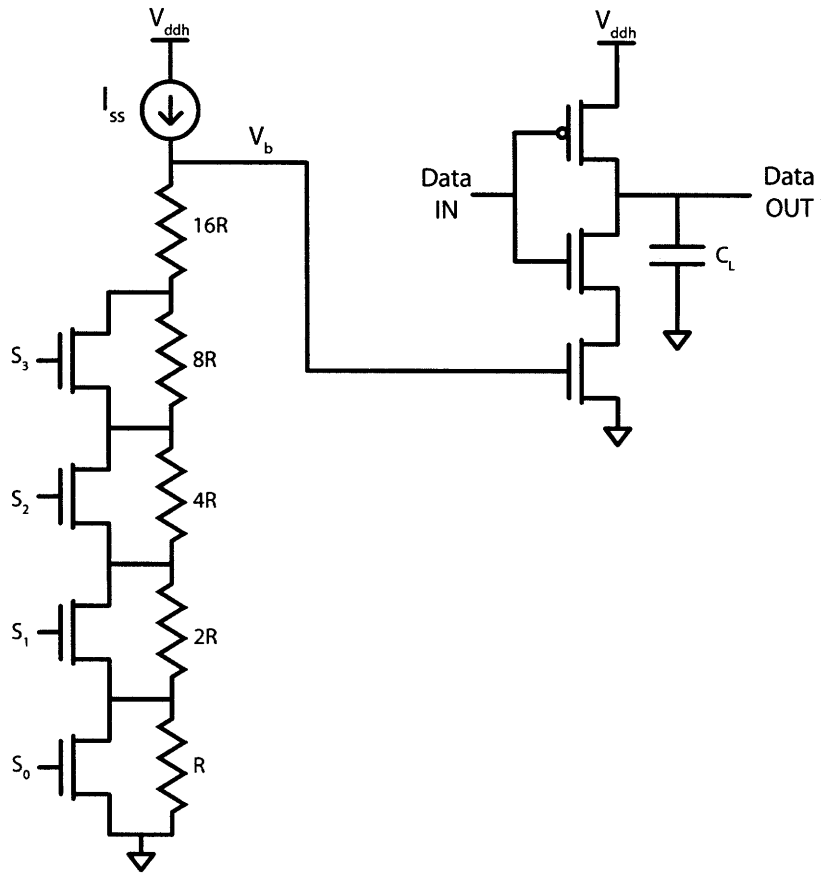

Figure 5-4: Schematic of the soft-switch showing the resistive DAC used to generate the gate voltage of the NMOS-only-current-starved inverter

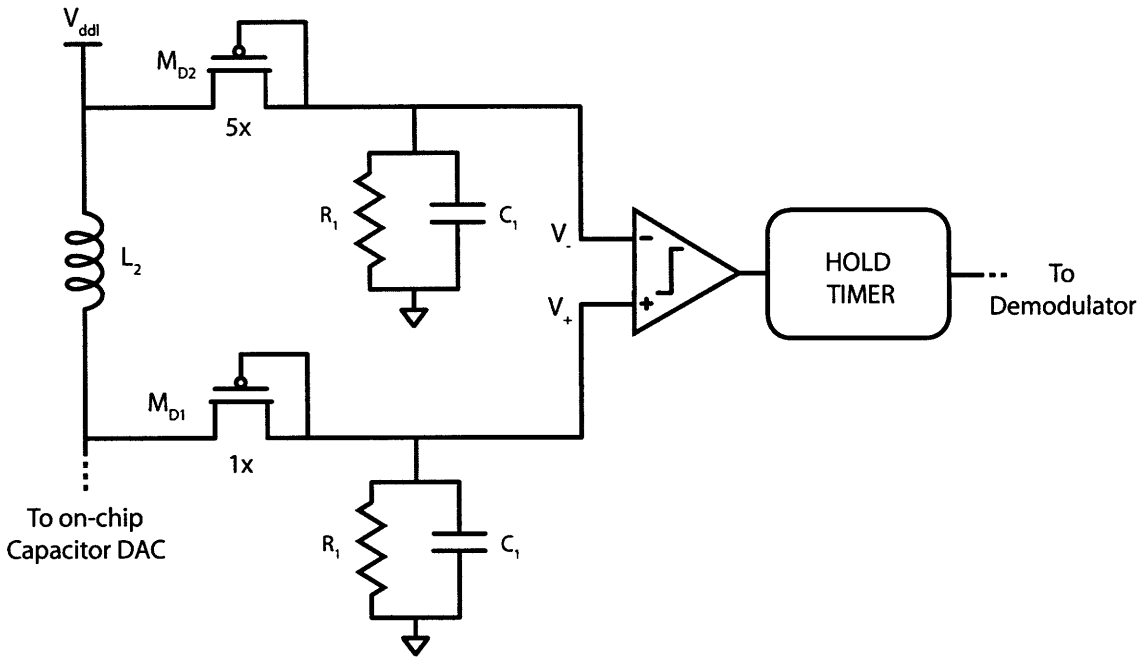

Figure 5-5: Schematic of the envelope detector used in the secondary transceiver

delay being approximated by $R_{on,PMOS}C_L$. However, when the output is transitioning from $1 \rightarrow 0$, the current is limited by maximum on current of M_3. The maximum on current of M_3 can be varied by varying the gate voltage of M_3 using the resistive DAC as illustrated in Fig 5-4. The resistive DAC is nominally biased with a current of 0.2μA. The output voltage of the resistive DAC can be varied from 300 mV to 580 mV in 16 discrete steps.

5.4 Envelope Detector

When data is being transmitted to the implantable secondary, TX is held low. The magnetic flux from the primary that is coupled to the secondary induces a voltage across the load inductance. This induced RF voltage is sensed using an envelope detector. The schematic of the envelope detector used is illustrated in Fig 5-5.

The time constant of the envelope detector is set using R_1 and C_1, and is given by,

$$\tau_{ed} = R_1 C_1.$$

The value of R_1 and C_1 used is 100 kΩ and 1 pF respectively such that the low pass cutoff frequency is set at $f_c = 1.5$ MHz.

The output of the envelope detector is then fed into the positive input of the comparator. Ideally, the negative input can be connected to the supply voltage, V_{ddl} since the nominal DC value of the RF signal will be at the supply voltage. However, this strategy does not provide any noise immunity as any noise picked up by the coil or even comparator input offsets can potentially cause the comparator to flip. To provide better immunity against noise, an internal reference voltage V_{ref} is generated, such that V_{ref} is about 10-20 mV above the DC voltage of the resonant tank output.

V_{ref} is generated by connecting another envelope detector to the supply voltage, V_{ddl} as illustrated in Fig 5-5. However, the PMOS as the diode in this second arm is designed to be a factor M times larger than that of the diode connected to the output of the resonant tank as shown in Fig 5-5. At DC, the coil is just a short. As such, the DC voltage at the inputs of both envelope detectors are equal, and given that both diodes carry the same current, the comparator input differential voltage is given by,

$$\begin{aligned} V_{id} &= V_+ - V_- \\ &= -\frac{\phi_t}{\kappa} \ln(M), \end{aligned} \tag{5.1}$$

where M is the W/L ratio between M_{D1} and M_{D2}, ϕ_t is the thermal voltage, and κ is the subthreshold constant (approximated to be 0.7). Given that in this design $M = 5$, $V_{id} \approx 58$ mV nominally. This negative V_{id} ensures that the output of the comparator is nominally low, even in the presence of a comparator input referred offset of ~ 10 mV. Furthermore, any noise picked up by the coil will not be able to cause the comparator output to go high as long as the noise voltage does not exceed $-V_{id}$. However, when sufficient signal is coupled from the primary to the secondary such that the peak output of the envelope detector exceeds $-V_{id} \approx 59$ mV, the output of the comparator will go high. Similar to the primary, the output of the comparator is passed through a hold timer to remove spurious transitions that are shorter than

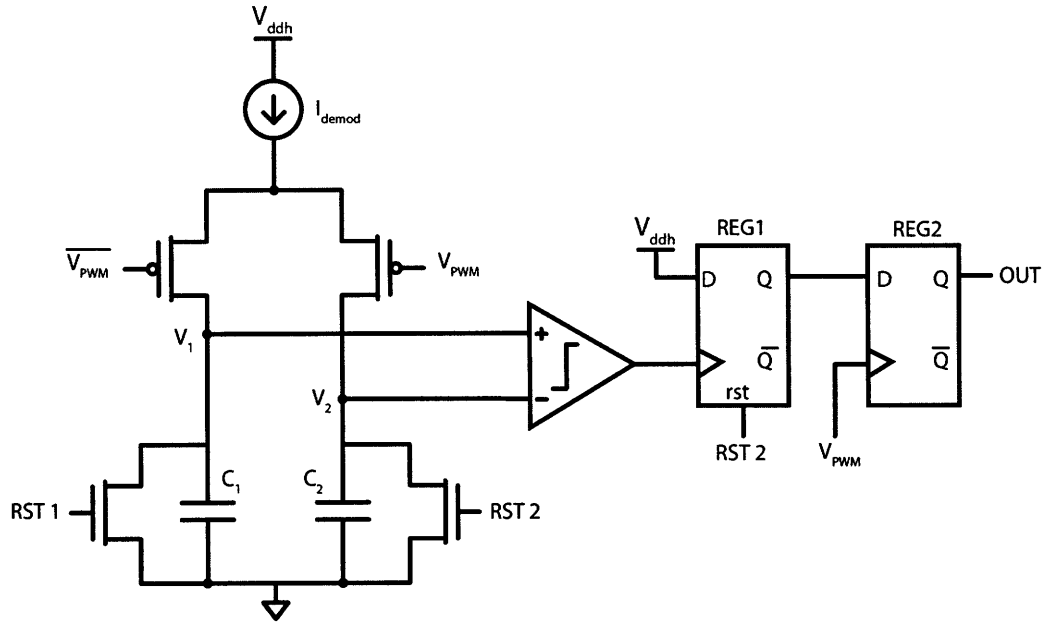

Figure 5-6: Schematic of the pulse-width demodulator circuit used in the secondary transceiver. $C_1 = C_2$ in the demodulator implemented on chip.

200 ns.

5.5 Demodulator

The schematic in Fig 5-6 illustrates the demodulator that is used in the implanted secondary to demodulate the RZ modulated downlink data. The RZ coding strategy employed for downlink data transmission is a square wave with either a 75% or 25% duty cycle to denote either a bit '1' or bit '0' respectively. The envelope detected PWM data is used gate a current, I_{demod}. The current source is used to charge the two capacitors C_1 and C_2 during the high and low phase of the input PWM signal. Therefore, at the end of the bit period, T, the voltage on both capacitors is given by,

$$\text{Bit } 0 \ : V_1 = \frac{I_{demod}T}{4C_1} \tag{5.2}$$

$$V_2 = \frac{3I_{demod}T}{4C_2} \tag{5.3}$$

$$\text{Bit } 1 \ : V_1 = \frac{3I_{demod}T}{4C_1} \tag{5.4}$$

$$V_2 = \frac{I_{demod}T}{4C_2} \tag{5.5}$$

To minimize the BER given this coding scheme and assuming that the distribution of ones and zeros in the data stream occur with equal probability, the threshold should be set at the 50% modulation point. Hence, for an input PWM signal with a 50% duty cycle, at the end of the bit period, $V_1 = V_2$. This is easily achieved by setting $C_1 = C_2$, since the charging current is the same for both capacitors.

The operation of the demodulator relies primarily on two narrow timing pulses RST1 and RST2, which are generated from the rising and falling edges of the input PWM signal. During the start of the bit, the signal RST1 discharges C_1 and sets V_1 to ground. I_{demod} then charges C_1 for the duration of the high phase of the input PWM signal. When the PWM input falls, RST2 resets C_2 and sets the node V_2 to ground. The demodulator current is then switched and charges C_2 for the remaining duration of the bit. The output of the comparator flips in the positive direction only in the case when a bit '1' is received, which then causes the output of Register 1 to go high. The second register is used to ensure that the each bit is stretched out for the entire bit period and is clocked on the rising edge of the PWM input signal. Since there is a falling edge in the middle of every bit period, this edge can be used to clock the output data.

The capacitor charging waveforms are shown in Fig 5-7. By using two individual reset pulses to reset the charging capacitors as opposed to a single global reset at the beginning of the bit period, the offset introduced by the width of the reset pulse can be mitigated. With individual reset phases for both capacitors, a similar offset as seen in the charging waveform of C_1 is introduced in the charging waveform of C_2.

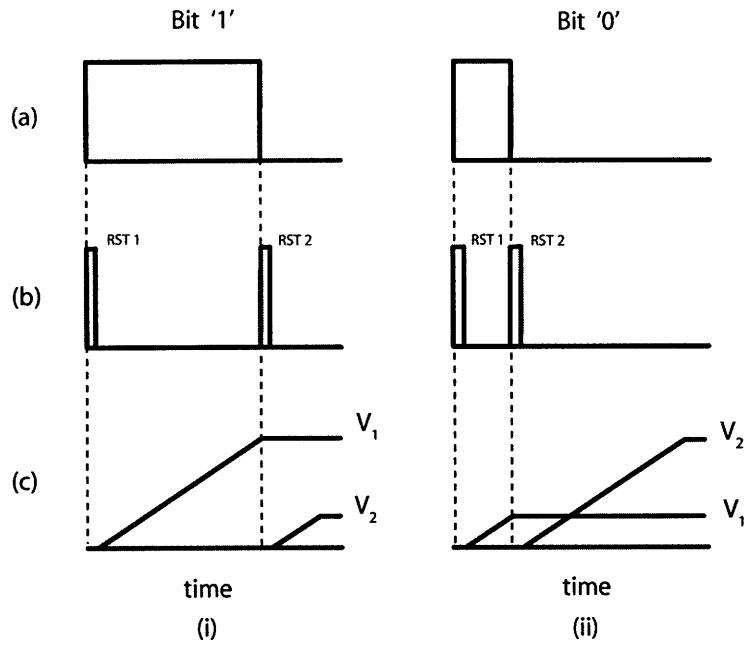

Figure 5-7: Relevant waveforms associated with the demodulator circuit. Column (i) illustrates the waveforms with a bit '1', while column (ii) illustrates the waveforms associated with a bit '0'. The PWM input waveforms are shown in row (a), while the reset signals generated from the rising and falling edges of the PWM input are shown in row (b). The charging profiles of capacitors C_1 and C_2 are shown in row (c)

This ensures that the differential offset voltage between the two capacitors at the end of the bit period is essentially zero.

Another limitation of this demodulator illustrated in Fig 5-6 is that this modulator requires that the data rate is higher than some minimum operation frequency. If the data frequency is too low, the voltage across both C_1 and C_2 will be at V_{DD} at the end of the bit period, making it impossible to discriminate between a bit '1' or bit '0' This minimum frequency is given by,

$$V_{DD} = \frac{I_{demod}T}{4C} \tag{5.6}$$

$$f_{min} = \frac{I_{demod}}{4CV_{DD}}, \tag{5.7}$$

where $C = C_1 = C_2$. To mitigate this problem, I_{demod} is replaced with a 2-bit current DAC that can be programmed by the user for the given downlink data rate so as to

minimize the downlink BER.

5.5.1 Power Reduction During Uplink

Similar to the power saving strategy applied in the primary transceiver, when data is being transmitted to the external primary, all receiver circuits in the implantable secondary are turned off. This is done by turning off the current mirrors to all devices that consume static power such as the envelope detectors, comparator, hold timer, and the demodulator circuits.

Chapter 6

Testing and Characterization

The previous three two chapters presented the design of a prototype impedance modulation based wireless data link for implantable applications. In this chapter we discuss the experimental methods used to test the various subsystems included in this wireless link. Measured performance data is also presented.

6.1 Prototype Chip

A prototype impedance modulation based wireless data link was fabricated using a 0.18 *mu*m standard CMOS process with six layers of metalization. The overall chip measures 3.1mm x 3.1mm. Due to logistical reasons, both the primary and secondary transceivers were implemented on the same die. However, two different chips that were mounted on separate PCBs were used during testing. The primary transceiver consumed a total active area of $0.5mm^2$, while the implantable secondary transceiver utilized a total active area of $0.35mm^2$. The layout of the prototype chip is shown in Fig 6-1. The primary and secondary transceivers are highlighted in green.

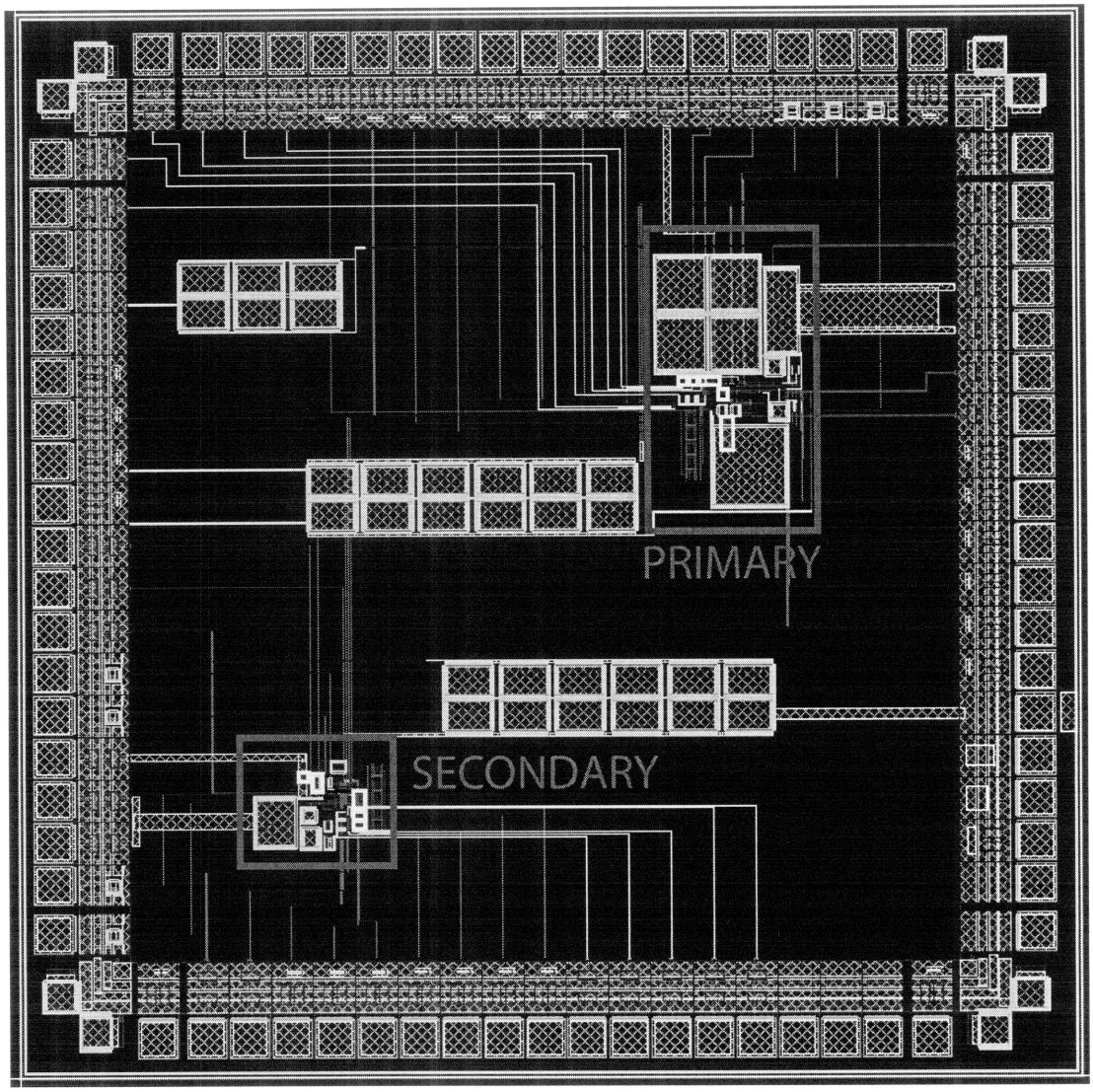

Figure 6-1: Layout of the prototype chip. The primary and secondary transceivers are highlighted in green outlines.

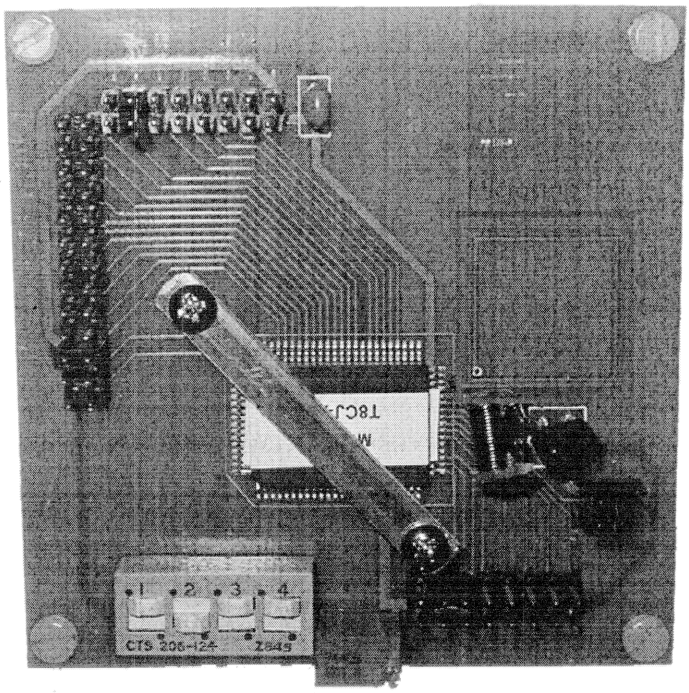

Figure 6-2: Test board used to characterize the primary transceiver. The microstrip coil is outlined in red.

6.2 Primary Transceiver Subsystems Characterization

6.2.1 Testing Strategy

The block diagram of the primary transceiver is illustrated in Fig 4-1. As can be seen from the block diagram, the primary transceiver consists of three major subsystems, namely the local oscillator and the corresponding front-end analog circuitry, the PLL that is used to recover the clock from the uplink data, and an on-chip PWM modulator used to modulate downlink data. In order to facilitate testing of each subsystem, two muxes were used. By setting the setting the appropriate muxes, external data can be directly input into either the PLL or the on-chip demodulator. The output of each subsystem can then be examined independently to ensure functionality independent of all other circuitry on board.

The primary transceiver chip was mounted on a PCB. The test board included the microstrip coil that is used as the inductive load in the local oscillator used in the

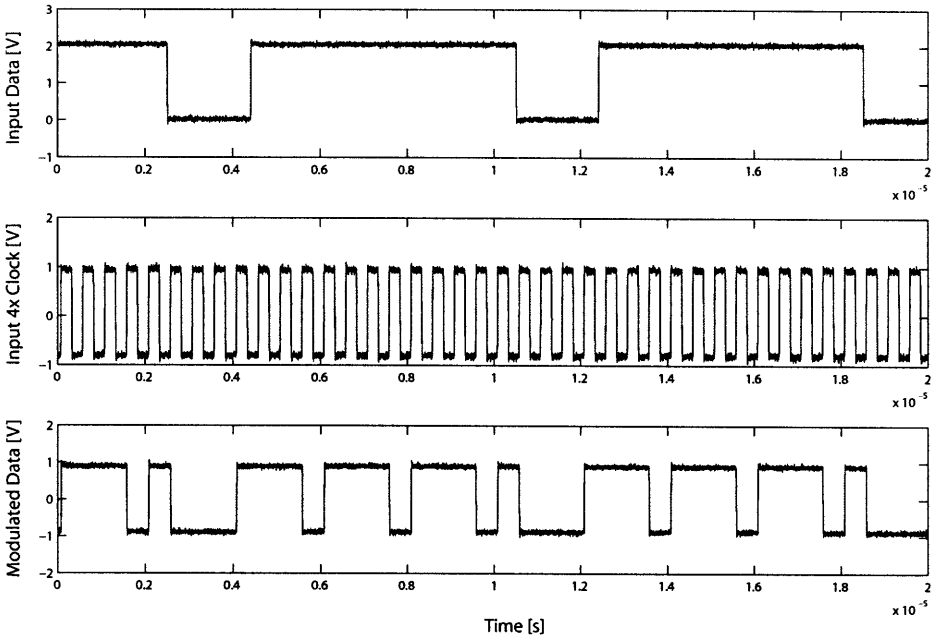

Figure 6-3: Measured data of the on-chip PWM data modulator. The top curve shows the input data, the middle curve shows the 4x clock used by the on-chip modulator while the bottom curve illustrates the modulator output.

primary. A photograph of the primary test board is shown in Fig 6-2.

6.2.2 On-Chip Current Reference

An on-chip PTAT current reference was used to bias all on-chip circuitry. The current reference was designed to provide a nominal current of 1μA. A two-bit calibration circuit allowed the value of the current reference be varied $\pm 50\%$ in four steps. The test-chips showed close agreement between simulation and measured results. The mismatch of the on-chip current reference varied between 5-15% below the simulated value.

6.2.3 PWM Modulator

The downlink data is modulated using a 75%-25% modulation scheme to denote a bit '1' and bit '0' respectively as described in Section 4.6.1. Fig 6-3 shows measured data of the dowlink data modulator. The measured data show that there is a one

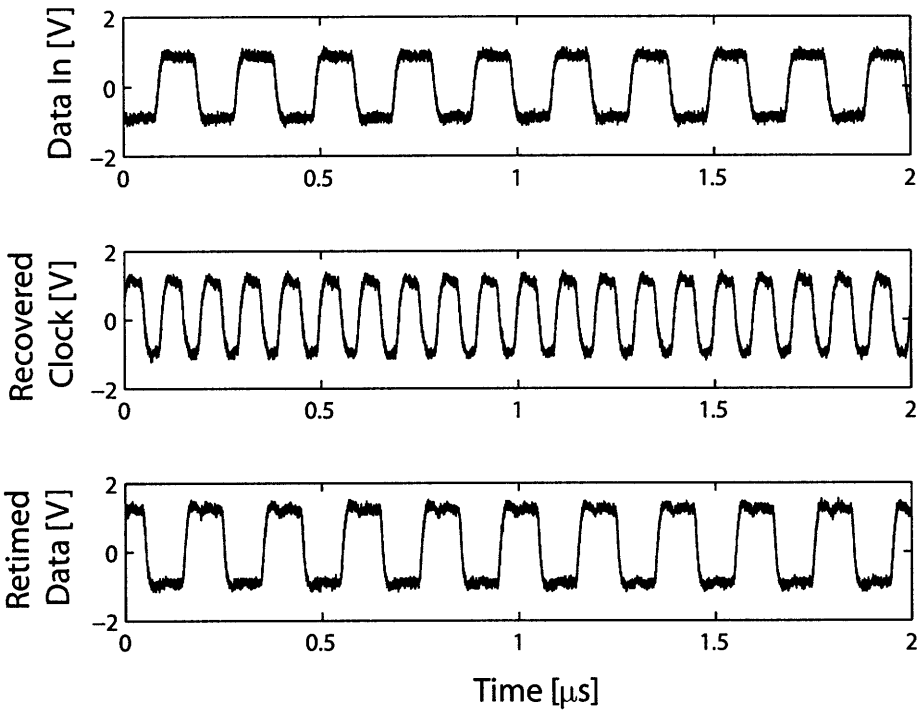

Figure 6-4: Measured data of the PLL during lock. The input data has a frequency of 10MHz (top). The middle row shows the recovered clock. The bottom row shows the retimed data, which is aligned to the rising edge of the clock.

cycle delay between the input data and the modulated output.

6.2.4 PLL

As described in Section 4.5, the on-board PLL is used to recover the clock from the uplink data. To ensure functionality, both muxes in Fig. 1 was set 'LOW' in order to allow an external digital signal to be directly input to the PLL. As shown in Fig 6-4, a train of '101010...' bits was used as the input data for the PLL. The input data stream has a frequency of 10 MHz. Fig. 5 shows the PLL in lock, with the recovered clock being 2x the frequency of the input data stream. The rising edge of the recovered clock stream can be seen to align correctly with the retimed-data output (i.e. in the middle of each bit).

One benefit of using a Hogge detector as the phase detector in the PLL is the ability of the Hogge to not consider missing edges as a error in the frequency, and thus lose lock with the input signal. To measure the lock stability of the PLL, the

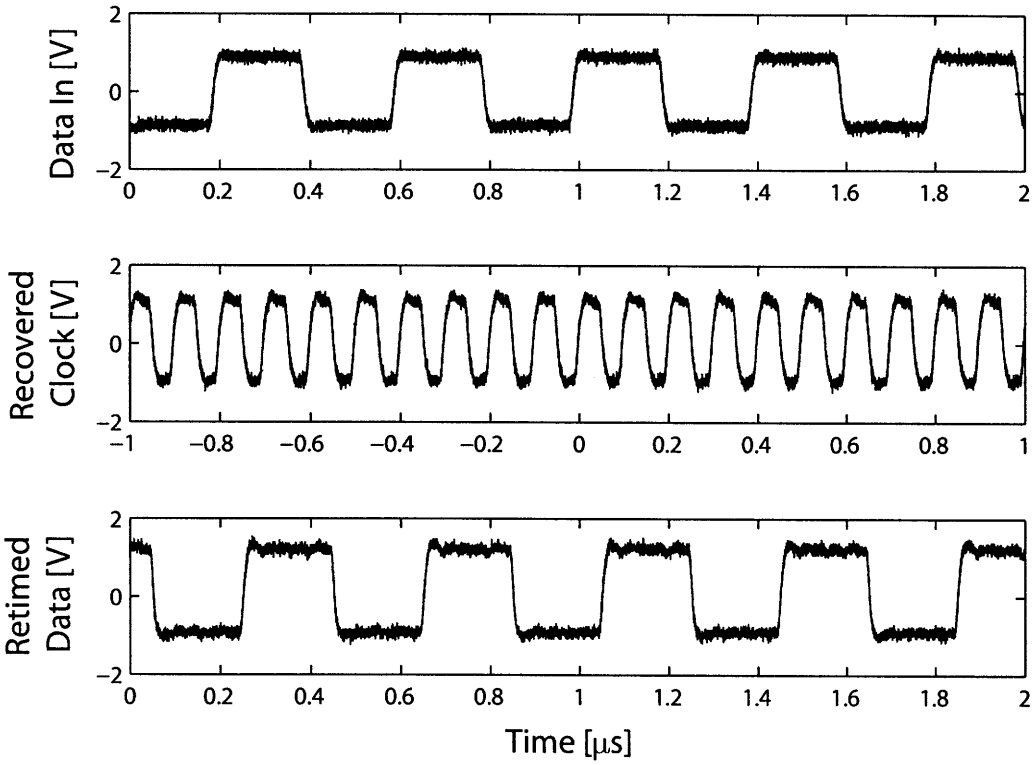

Figure 6-5: Measured data of the PLL during lock. The input data has a frequency of 10MHz (top), with two successive bits of the same value being transmitted to simulate missing edges in the input data stream. The middle row shows the recovered clock. The bottom row shows the retimed data, which is aligned to the rising edge of the clock.

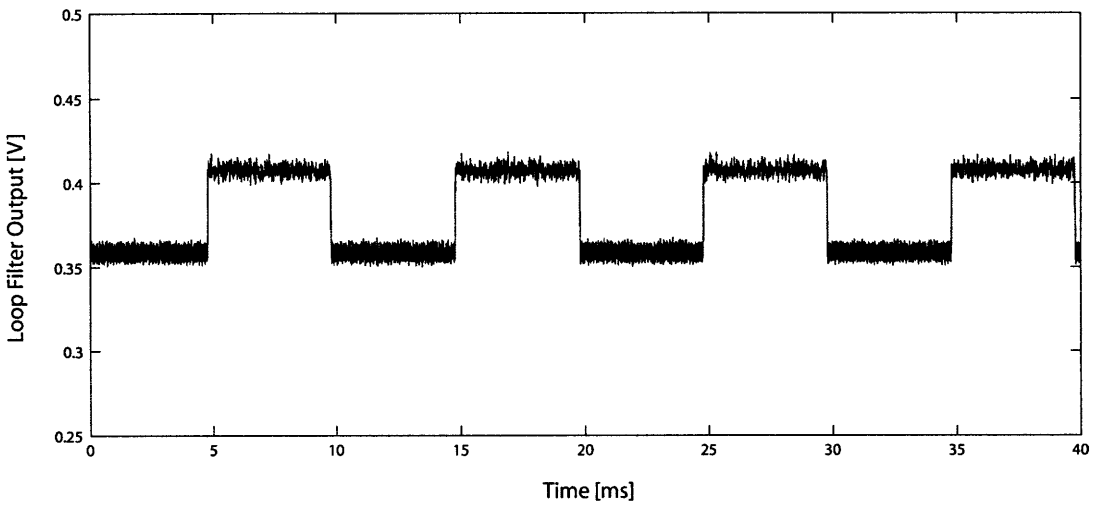

Figure 6-6: Measured data of the loop filter output of the PLL. The input data modulated using a FSK modulation scheme between 9MHz and 10MHz. The LF output has a square wave output indicating that the PLL can indeed track frequency variations in the input data stream.

input data stream was switched between a '101010...' data stream to a '11001100...' data stream. This essentially introduces a 'missing' edge in the data between two bits of the same value. Fig 6-5 shows the measured data of the PLL with missing edges in the input data. The PLL still remains in lock, and the recovered clock frequency remains constant at 10 MHz. This implies that the PLL has good lock stability and does not lose lock in the presence of missing edges, as can be expected in a normal data stream.

While missing edges should be ignored, when there is an actual shift in the frequency of the input data, the PLL should ideally react to this shift and lock to the new input frequency. Fig 6-6 shows the output of the loop filter when the input data frequency is shifted between 9 MHz and 10 MHz respectively. The square wave of the LF output indicates that the PLL reacts well to actual frequency changes and locks to the new input frequency. This plot is a nice pictorial example of basic FM demodulation property of all PLLs.

The lock range of the PLL is programmable by varying the current multiplier in the VCO's V→I circuit as described in Section 4.5.3. The PLL has a lock range of 3.1 - 14.6 MHz. As is the case with almost all PLLs used as clock and data recovery

Table 6.1: Measured electrical characteristics of the microstrip coil at 40 MHz.

Parameter	Value
Reactance @ 40 MHz	67 Ω
Resistance @ 40 MHz	0.92 Ω
Q	73

circuits (CDRs), the lock acquisition range is smaller and spans from 7 - 11 MHz of the input data rate.

6.2.5 Colpitts Oscillator Performance

Microstrip Coil Measurements

The microstrip coil properties was measured and characterized using a network analyzer. While the coil was designed to provide 200nH of inductance, the fabricated coil had a total inductance of 267nH. This will result in a shift in the Colpitts' oscillation frequency. Other electrical characteristics of the microstrip coil is listed in Table 6.1.

Colpitts Oscillator Start-Up Issues

In Section 4.3, the design of the Colpitts Oscillator used as the LO in the primary was described. Simulation results indicated that the amplitude of oscillation of the Colpitts Oscillator can be controlled by varying I_{bias}. Simulations results indicated that the oscillation amplitude can be varied between 0.5V - 1.2V, and start-up was guaranteed even with the minimum current setting of 400μA.

In practice however, the total current required for start-up is larger than expected. A minimum current of 1mA is required before startup is achieved. Furthermore, the amplitude of oscillation during start-up is lower than expected. The frequency of oscillations was measured to be 35.1MHz, which matches well with calculations after taking into account the extra inductance of the microstrip coil.

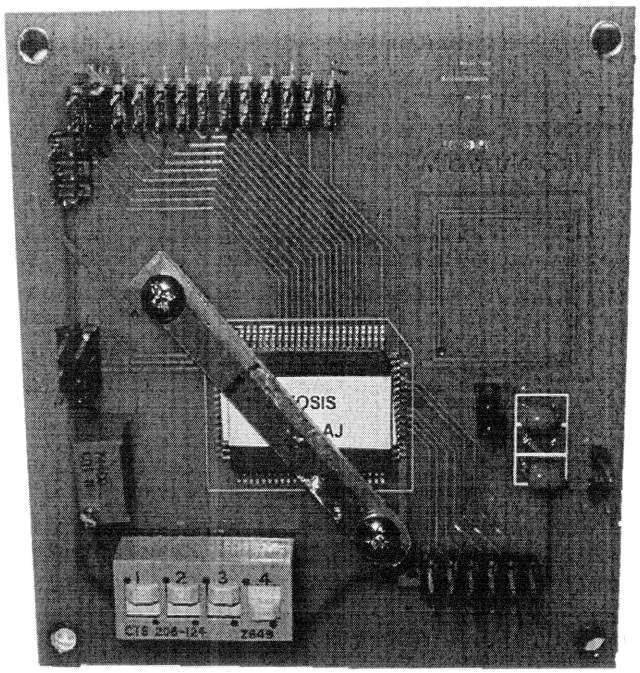

Figure 6-7: Test board used to characterize the secondary transceiver. The microstrip coil is outlined in red.

6.3 Secondary Transceiver Subsystems Characterization

6.3.1 Testing Strategy

The block diagram of the secondary transceiver is illustrated in Fig 5-1. The main subsystem of the secondary is the demodulator circuitry that is used to demodulate the downlink data. In order to allow for independent of testing of the downlink demodulator, a mux was used to allow an externally input PWM signal to be input directly into the demodulator.

The secondary transceiver chip was mounted on a PCB test board. The test board included the microstrip coil that is used as the inductive load in secondary resonator circuit. A photograph of the primary test board is shown in Fig 6-7.

Table 6.2: Demodulator operation frequencies at various current levels.

Demodulator currnet (nA)	Demodulation Frequency Range
45	160 kHz - 1.2 MHz
90	245 kHz - 1.14 MHz
125	360 kHz - 2.4 MHz

6.3.2 On-Chip Current Reference

An on-chip PTAT current reference was used to bias all on-chip circuitry in the secondary transceiver. The current reference was designed to provide a nominal current of 100 nA. A two-bit calibration circuit allowed the value of the current reference be varied ±50% in four steps. The test-chips showed close agreement between simulation and measured results. The mismatch of the on-chip current reference varied between 5-10% below the simulated value.

6.3.3 Demodulator

The demodulator circuit used to recover the data and clock from the PWM modulated downlink data is described in Section 5.5. One issue with the flavor of PWM demodulator circuits described in Section 5.5 is that for slow data rates, the voltages on both capacitors can rail resulting in it being impossible to distinguish if a bit '1' or '0' was transmitted. A current DAC was used to make the demodulator charging current programmable such that lower data rates can be used, which also reduces the power consumption of the demodulator circuitry. The demodulator circuit was measured to require a minimum frequency of 160 kHz at the lowest charging current setting. The demodulator performance is summarized in Table 6.2.

6.4 Downlink Data Transmission

The test setup for downlink data transmission measurement is shown in Fig 6-8. The coils were separated by a distance of 1 cm. Measure results of the transmitted and received data is illustrated in Fig 6-9. Downlink data transmission rates of up to

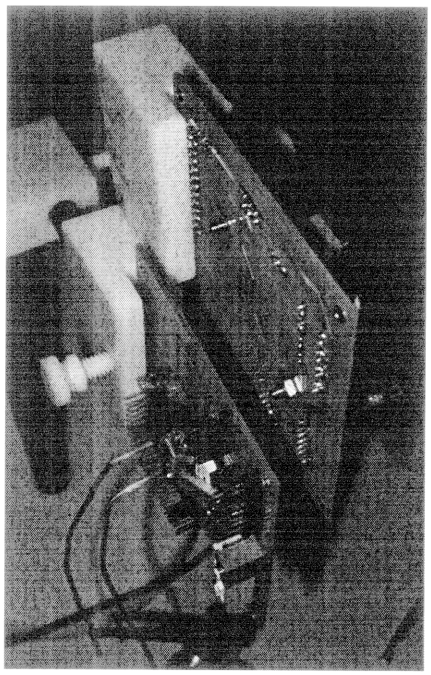

Figure 6-8: The test setup used to measure the downlink data transmission. The boards are mounted on stands and separated by 1 cm. The coils are aligned on axis.

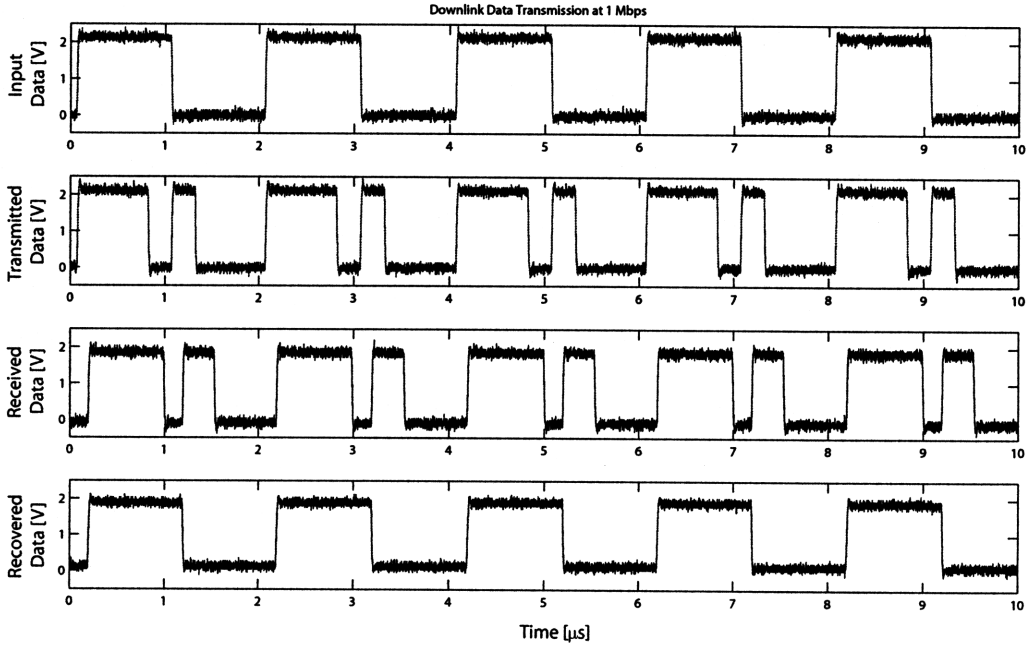

Figure 6-9: Measured data of the downlink transmission at a data rate of 1 Mbps. The primary and secondary coils are 1 cm apart. The top row shows the transmitted data, while the second row shows the modulated data that is actually transmitted. The third row illustrates the received data, while the last row shows the demodulated data.

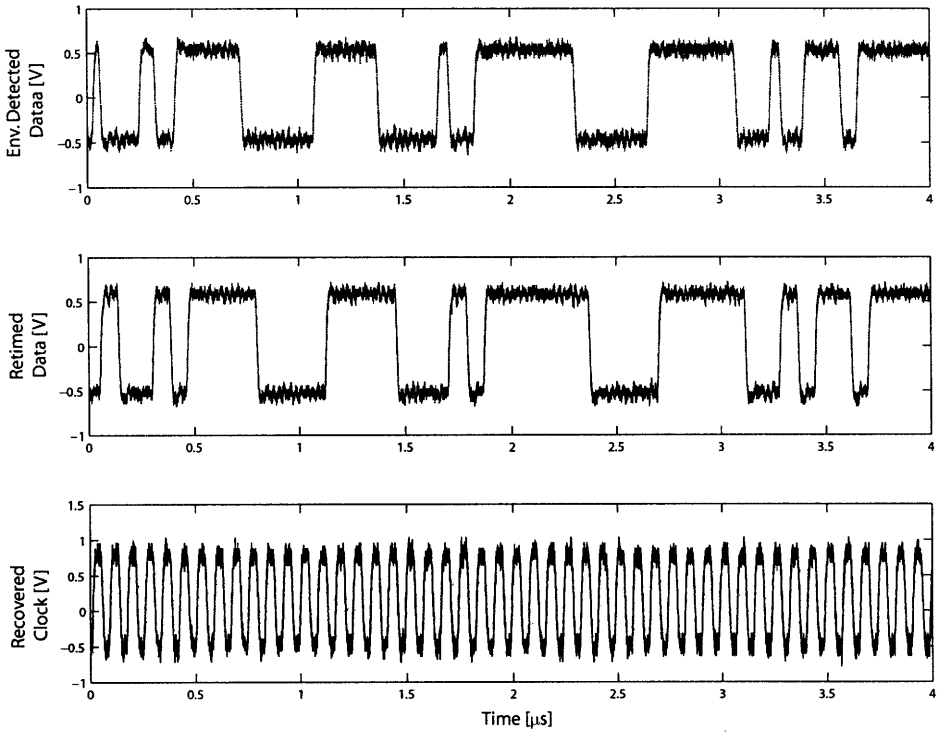

Figure 6-10: Measured data of the simulated uplink transmission at a data rate of 10 Mbps. The top plot shows the output of the envelope detectors and comparator. The center plot shows the retimed data output of the PLL, while the last curve shows the clock stream recovered from the input data.

1.5 MHz can be achieved. The BER of downlink data transmission was measured to be 6 x 10^{-7}. In this prototype, the downlink transmission distance was limited to 1cm due to the reduced oscillation amplitude of the primary oscillator, which in turn resulted in a significantly lower received signal amplitude on the secondary resonator.

6.5 Uplink Data Transmission

Due to the reduced oscillation amplitude of the Colpitts Oscillator, it was difficult to set up the uplink data transmission experiment. While in the downlink case, the received signal is attenuated by k, where k is the coupling coefficient and is usually in the order of 10^{-3}, for the uplink case, the received signal is proportional to k^2. This results in the received signal being significantly smaller than simulated, which severely impedes the impedance modulation based uplink.

However, in order to measure the performance of the front-end circuitry, a simu-

lated uplink transmission experiment was performed. The microstrip coil was cut and an external AM modulated signal produced by a Wavetek Arbitrary Waveform Generator (AWG) was directly input into the receiver circuitry of the primary transceiver. Fig6-10 illustrates the signal recovered by the on-board envelope detectors, and the corresponding PLL output for a simulated 10 MHz data rate.

Chapter 7

Conclusions

7.1 Summary

In this thesis, we have presented the design of an impedance-modulation based wireless link. The wireless link presented here is half-duplex, with a high bandwidth uplink and a low bandwidth downlink. This wireless link is optimized for communication with an implanted device, where the main goal is to minimize the power consumption of the implanted device that needs to operate on a highly limited energy supply.

In this design, a method to control the LO oscillation amplitude by varying the bias current of a Colpitts Oscillator is discussed. Hence, only the minimum required current needed to achieve a pre-determined BER rate for the link is used, to further reduce the power consumption of the external transceiver. This is important since the Colpits Oscillator consumes up to 75% of the total power consumption of the entire system.

One issue present in all impedance based wireless links is the effect of pulse-width distortion phenomena as discussed in Section (5.3.1). A soft-switch mechanism to pre-distort the transmitted data using an asymmetrically current-starved inverter is presented.

Given that both the implanted and external transceivers will be in close contact to the skin, we can expect a shift in the resonant frequency of the magnetically coupled resonators. To ensure that post-implantation both the primary and secondary

resonator center frequencies are matched, a tuning circuit is used in the secondary resonator.

7.2 Future Work

There are a number of ways in which the ideas presented in this thesis can be further explored. Some of ideas worth pursuing are:

- One issue with the Colpitts Oscillator used in this prototype is that the coil is connected in series to the power supply. As such, the peak currents in the inductor can be very high ($Q \cdot I_{DC}$). Hence, the power supply will need to source and sink these large transient currents, which is undesirable. Supply filtering (e.g. using a LC filter between the coil and the power supply) can be used to reduce the large transient currents. An alternative method would be to use a differential Colpitts topology with a center-tapped inductor.

- In the current prototype, the capacitor DAC that is used to adjust the center frequency of the secondary resonator such that both the primary and secondary transceivers are tuned is implemented in a feed-forward fashion. An alternative would be to develop an automatic feedback loop that is able to periodically adjust the center frequency of the secondary resonator to ensure that both resonators are in tune. This circuit can be implemented by a circuit that runs through all the possible capacitor configurations and chooses the capacitor DAC setting that maximizes the amplitude of the received signal.

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