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Abstract—**Graphene transistors are made by transferring a thin graphene film grown on Ni onto an insulating SiO$_2$ substrate. The properties and integration of these graphene-on-insulator transistors are presented and compared to the characteristics of devices made from graphitized SiC and exfoliated graphene flakes.**

Index Terms—**Carbon CVD, carbon transistors, chemical-vapor deposition (CVD), epitaxial graphene, graphene, graphene transistors.**

I. Introduction

GRAPHENE, a thin sheet of graphitic carbon, is a promising candidate as a material for future electronics [1]. The major advantages of graphene are its high intrinsic mobility and its 2-D structure. The 2-D structure makes extremely thin sheets of graphene, less than 1 nm, highly conductive, and it makes it possible to fabricate extended active areas of arbitrary length and width. Graphene is also unique in that it is a semimetal with a zero band gap and in that the electrons have a zero effective mass (m_e). While the zero m_e is advantageous for graphene transistors, the lack of a band gap is problematic, because it prevents the devices from turning off below a fairly high threshold conduction of approximately e^2/h per square. Recently, significant progress has been made in developing various methods of producing a band gap in graphene [2], [3].

Another problem with graphene is that a well-controlled method of preparing a graphene substrate suitable for device fabrication has not yet been demonstrated. The two established methods for preparing thin graphene films, SiC sublimation [4], [5] and highly oriented pyrolytic graphite (HOPG) exfoliation [1], [6], have significant limitations. SiC sublimation leads to polycrystalline graphene layers even when the SiC is single crystal, and the HOPG exfoliation produces small graphene flakes of various shape and thickness.

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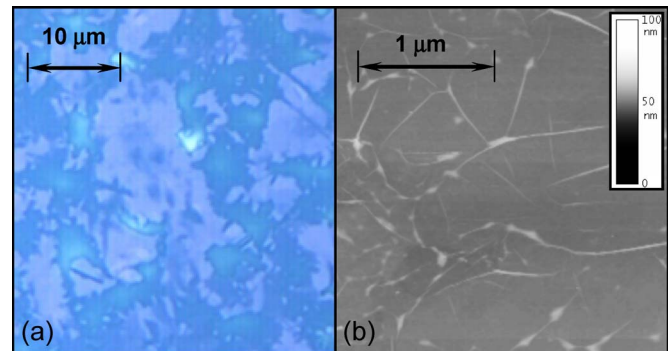
Fig. 1. (a) Optical micrograph and (b) AFM scan of the GOI substrate after transfer and prior to transistor fabrication. Light-blue areas in (a) indicate thinner graphene. The causes of the graphene thickness variation are still under investigation.

Recently, Reina *et al.* [7] have developed a promising alternative technique for preparing graphene films for use as electronic substrates. This technique involves growing an epitaxial graphene film on a nickel layer by chemical vapor deposition [8] and, then, transferring the graphene onto an insulating substrate. In this letter, the resulting graphene-on-insulator (GOI) substrate was used to make transistors. The GOI transistors show similar characteristics to the ones made on graphitized SiC [5], with $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratios of about 10 and mobilities up to 2200 cm^2/V $\cdot$ s.

II. Fabrication

The method for the preparation of GOI material is described in more detail elsewhere [7]. In brief, graphene is grown epitaxially on a polycrystalline Ni film at 1000 °C for 5 min with 99 : 1 H$_2$: CH$_4$ (760 torr). A protective PMMA layer is then spun on top of the graphene. Next, the graphene–PMMA film stack is selectively lifted-off from the substrate by etching the Ni in HCl. The graphene–PMMA film is then placed, with graphene facing down, on a suitable insulator, which, for this letter, was a 150-mm silicon wafer with 500 nm of SiO$_2$. Next, the PMMA is dissolved selectively to the graphene in acetone, and the wafer is annealed. The anneals, an initial one at 400 °C for 20 min in 50% H$_2$ 50% N$_2$ and a second one at 1000 °C for 10 s in N$_2$, are preformed to remove PMMA residue and to promote graphene adhesion. In principle, this method can be used to produce GOI substrates of any size, but in this experiment, 12 mm × 10 mm squares of graphene were transferred onto a 150-mm wafer.

Fig. 1 shows the optical and atomic force microscope (AFM) micrographs of the GOI material after transfer and before transistor fabrication. The graphene film is continuous across
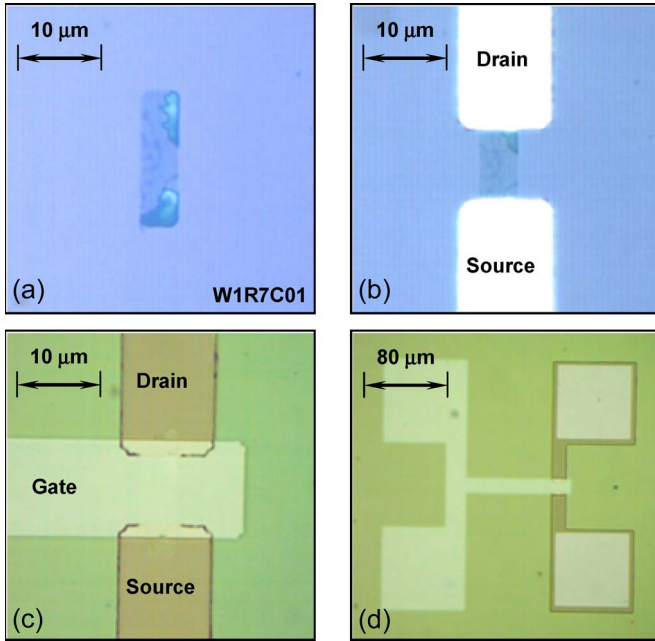
Fig. 2.   Transistor-fabrication optical micrographs. (a) Device region after graphene etch and resist strip. (b) After 2-nm/20-nm Ti/Pt source–drain lift-off. (c) After 40-nm HfO_2 dielectric deposition and 20-nm Pt gate lift-off. (d) Entire device after pad etch. The thickness of the graphene in the region between the source and drain is ∼1.5 nm as measured by AFM, which represents ∼4 monolayers of graphene.

the whole region but with thickness variations from location to location. The dark-blue regions of the graphene are thicker, on the order of 10 nm, while the light-blue regions are thinner, on the order of 2 nm. The AFM shows that folds in the graphene layer exist after the transfer onto the oxide.

The transistor-fabrication sequence is shown in Fig. 2. First, the graphene areas were patterned and etched with an oxygen plasma. The resist was then stripped using an 80 °C sulfuric acid etch for 10 min. Next, a lift-off process was used to pattern the metal source/drain regions. The source–drain area consisted of 2-nm Ti topped with 20-nm Pt. Next, a HfO_2 dielectric was evaporated onto the wafer with the wafer held at 150 °C. Following dielectric deposition, a 20-nm Pt gate was patterned using lift-off. Finally, the HfO_2 was etched over the source/drain pads using a 4-min SILOX HF wet etch.

III. ELECTRICAL RESULTS

Transistors were tested at room temperature and normal laboratory atmosphere. Fig. 3 shows the I_d–V_g behavior of the graphene transistor shown in Fig. 2. The V-shaped I_d characteristic is typical of semimetal graphene devices, with electrons conducting for positive gate voltages and holes conducting for negative gate voltages. At $V_d = 0.1$ V, the I_{on}/I_{off} is more than ten. This is an excellent result for top-gated graphene devices with no band gap. The low field mobility for this device is 800 $cm^2/V \cdot s$ for electrons and 1600 $cm^2/V \cdot s$ for holes, somewhat smaller than the best results achieved on graphitized SiC and exfoliated HOPG [1], [5]. This is particularly encouraging, since the evaporated HfO_2 dielectric is not optimized and is expected to significantly reduce the carrier mobility.
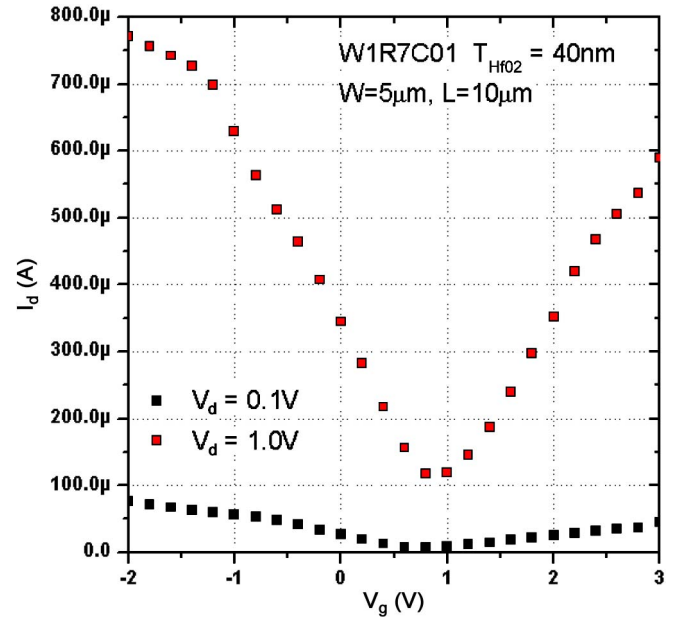

Fig. 3. I_d–V_g characteristic of the device shown in Fig. 2. Drain–current increases in both directions, for negative gate voltages because of hole conduction and for positive gate voltages because of electron conduction. This V-shaped characteristic is typical of zero-band-gap graphene.
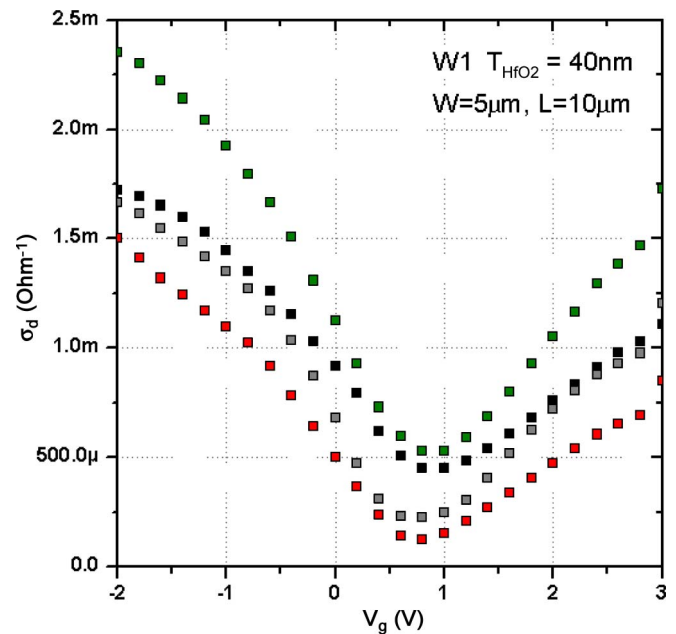

Fig. 4.   Low-voltage source-to-drain conduction characteristics for a set of "identical" devices. The device from Figs. 2 and 3 is the one with the lowest conduction. The V_d used for conductance measurement is 0.1 V.

The conduction behavior of a series of transistors with identical dimensions and process conditions is shown in Fig. 4. It is important to note that slightly more than half of the devices measured had cracks in the gate dielectric, causing the gate to short with the graphene layer. These devices are not shown in the ensemble. Since the cracks happened predominantly in the thicker graphene regions, the ensemble of the devices shown in Fig. 4. is skewed toward the thinner end of the graphene-thickness distribution. For this set of devices, the minimum conduction varies from 120 to 530 μS per square, the hole
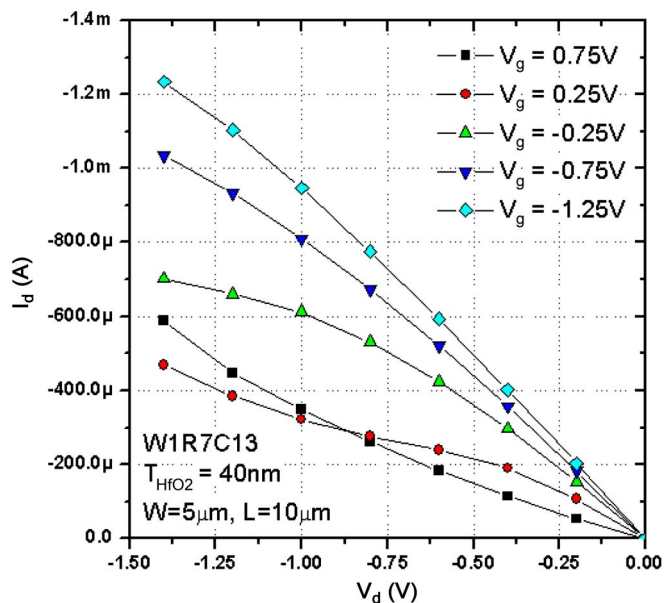
Fig. 5. I_d–V_d characteristics of a typical graphene device, for the hole-conduction branch ($V_g < 0.75$ V). This device has a smaller $I_{\text{on}}/I_{\text{off}}$ than the one shown in Fig. 3.
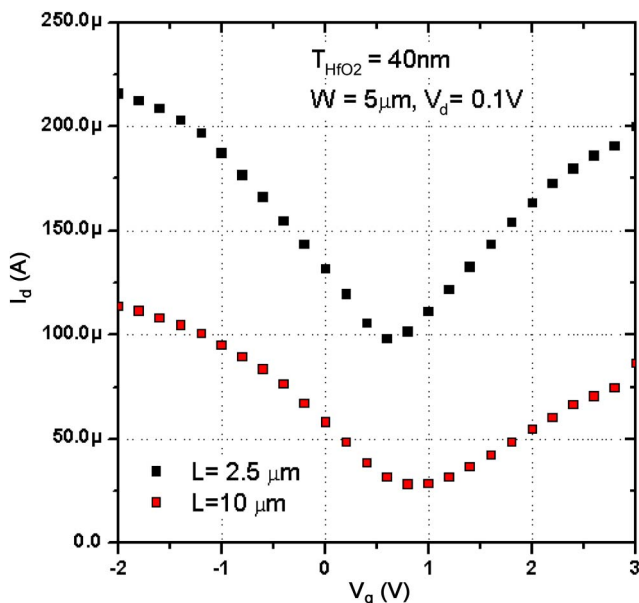

Fig. 6. Current characteristics of two graphene devices with different gate lengths. The shorter device has higher current and transconductance.

mobility varies from 1600 to 2200 cm^2/V $\cdot$ s, and the electron mobility varies from 800 to 1400 cm^2/V $\cdot$ s.

Fig. 5 shows the I_d–V_d of a typical device; this one has $I_{\text{on}}/I_{\text{off}}$ that is lower than the best device shown in Fig. 3. The gate is biased below 0.75 V, displaying pFET holelike conduction. Even at these gate biases, the electronlike conduction does turn on at the larger $|V_d|$ voltages, for V_g of 0.75–0.25 V, since the drain for holes is the source for electrons.

All the devices shown so far have the same gate length and channel width: 10 and 5 μm, respectively. Fig. 6 shows the conduction characteristics of two devices with different gate lengths: 10 and 2.5 μm. As expected, the shorter channel device shows higher current and transconductance. The trends, however, are not linear in gate length. It is likely that the contact resistance between the graphene and the metal is at least in part responsible for this discrepancy.

IV. CONCLUSION

The graphene transistors fabricated from GOI described in this letter show characteristics similar to graphene devices made by more established methods such as SiC graphitization and HOPG exfoliation. When compared to devices built on graphitized SiC, GOI devices exhibit higher $I_{\text{on}}/I_{\text{off}}$ ratios and mobilities that are typical of the higher mobility C-face graphene [5].

The advantage of the GOI preparation is that, unlike in HOPG exfoliation, arbitrarily large graphene regions are possible and, unlike SiC graphitization, a lattice match to the (111) Ni seed layer can be achieved. This match may open a path in producing single-crystal GOI of high thickness uniformity. An additional advantage of GOI is that processing graphene on a standard silicon wafer reduces fabrication complexity. In this initial experiment, the GOI was polycrystalline and showed large thickness variation. Future improvements to both the substrate-preparation methods and to the device-fabrication process are required to advance graphene-transistor technology.

ACKNOWLEDGMENT

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