Chapter 7. High-Frequency InAlAs/InGaAs Metal-Insulator-Doped Semiconductor Field-Effect Transistors (MIDFETs) for Telecommunications

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7.1 Introduction

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The goal of this project is to design, fabricate, test, and model submicron InAlAs/InGaAs Heterostructure Field-Effect Transistors (HFETs) on InP. These devices are of great interest for applications in long-wavelength optical communications and ultra-high frequency microwave telecommunications. We expect that extraordinary device performance will result from the unique combination of: (1) the large conduction bandgap discontinuity between InAlAs and InGaAs, (2) the large $\Gamma - L$ separation in InGaAs, and (3) the high velocity of electrons in InGaAs.

We have recently pioneered HFETs in which the InGaAs channel is heavily doped but the InAlAs insulator is undoped (MIDFETs for Metal-Insulator-Doped semiconductor FET).[1] We have found that these devices display a performance comparable to InAlAs/InGaAs Modulation-Doped FETs (MODFETs) of similar gate length. In addition, these devices offer a number of unique benefits not found in other device structures: reduced transconductance[1] and f_T collapse,[2] higher breakdown voltage,[1] and freedom to optimize gate insulator parameters.[3] A new *modulation-doped channel* MIDFET also displays unprecedented microwave characteristics.[4]

During 1989, we obtained the first working InAlAs/InGaAs MIDFETs on InP fabricated

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[1] J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+In_{0.53}Ga_{0.47}As$ MISFET with a Heavily-Doped Channel," *IEEE Electron Device Lett.* EDL-8 (11): 534-536 (1987).

[2] J.A. del Alamo and T. Mizutani, "Bias Dependence of f_T and f_{max} in an $In_{0.52}Al_{0.48}As/n^+-In_{0.53}Ga_{0.47}As$ MISFET," *IEEE Electron Device Lett.* EDL-9 (12): 654-656 (1988).

[3] J.A. del Alamo and T. Mizutani, "A Recessed-Gate $In_{0.52}Al_{0.48}As/n^+-In_{0.53}Ga_{0.47}As$ MIS-type FET," *IEEE Trans. Electron Devices* ED-36 (4): 646-650 (1989).

[4] J.A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+-In_{0.53}Ga_{0.47}As$ MISFET with a Modulation-Doped Channel," *IEEE Electron Device Lett.* EDL-10 (8):394-396 (1989).

at MIT.[5] The performance and properties of these MIDFETs are similar to those fabricated elsewhere.[3] More relevant to the problem, we fabricated, for the first time, strained-insulator InAlAs/InGaAs MIDFETs. This report gives a detailed description of our research on these devices.

We have exploited the inherent flexibility of gate insulator design of a MIDFET by increasing the AlAs content in the InAlAs insulator from the lattice-matching composition to InP ($In_{0.52}Al_{0.48}As$), straining it towards larger bandgaps. This rapidly effects an enhancement in the conduction band discontinuity (ΔE_c) between the InAlAs and the InGaAs channel (figure 1). We expect, in this manner, to obtain the following benefits:

- reduced gate leakage
- improved gate breakdown voltage
- reduced real-space transfer of hot electrons from the channel to the gate.

We have demonstrated all of these benefits experimentally while largely unaffecting the rest of the device parameters (threshold voltage, transconductance, etc.).

7.2 Experiments

We grew four wafers by molecular-beam epitaxy in MIT's Riber 2300 system. Following standard procedures, we prepared the surface of the InP wafer. Figure 2 shows the cross section of the grown heterostructures. The layer structure is similar to those utilized previously,[1] except for:

1. The channel design is more aggressive: doping is higher, 4×10^{18} cm^{-3}, and thickness is lower, 100 Å. This channel is expected to result in superior performance.
2. The Al composition in three of the wafers is increased over lattice matching conditions, i.e., wafers were grown in which x in the $In_{(1-x)}Al_xAs$ layer is 0.48, 0.52, 0.60, and 0.70 (all insulator layers are 300 Å thick). This is the main purpose of the present experiment.

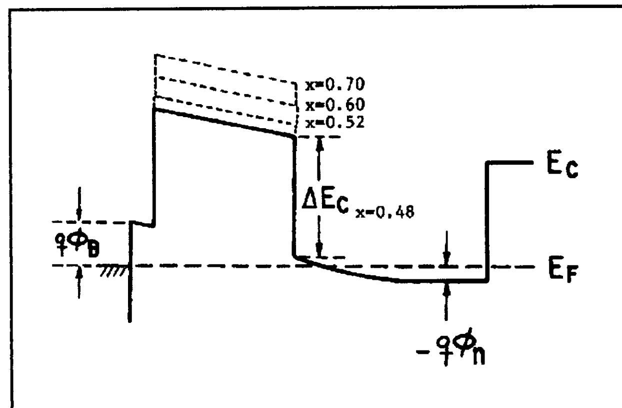

Figure 1. Cross-sectional equilibrium band diagram of device structure indicating the increase in ΔE_g with increase in Al composition.

We continued fabrication after growth with mesa isolation utilizing a selective chemical etchant, AuGeNi ohmic contact formation, TiAu interconnect, and TiAu gate layer formation. Figure 2 shows the resulting device cross section.

We have integrated a number of devices of varying dimensions and a large set of test structures into a 2.9×2.7 mm^2 chip. We present here DC I-V measurements on MIDFETs with a nominal gate length of 1.5 μm and a gate width of 30 μm.

7.3 Device Results

Figure 3 shows a plot of the transconductance versus gate to source voltage for four representative devices with varying $In_{(1-x)}Al_xAs$ insulator compositions. As expected from simple theory, the threshold voltage is, to the first order, unaffected by the introduction of strain in the insulator. The lattice-matched device has a maximum transconductance of 220 mS/mm. This value is higher than for any of the InAlAs/InGaAs MIDFETs previously reported in the literature with a similar gate length and overall epitaxial structure (the best was 160

[5] S. Bahl, W.J. Azzam, and J.A. del Alamo, "Fabrication of an InAlAs/n$^+$-InGaAs MIDFET," unpublished paper presented at the Fourth New England MBE Workshop, Cambridge, Massachusetts, May 4, 1989.

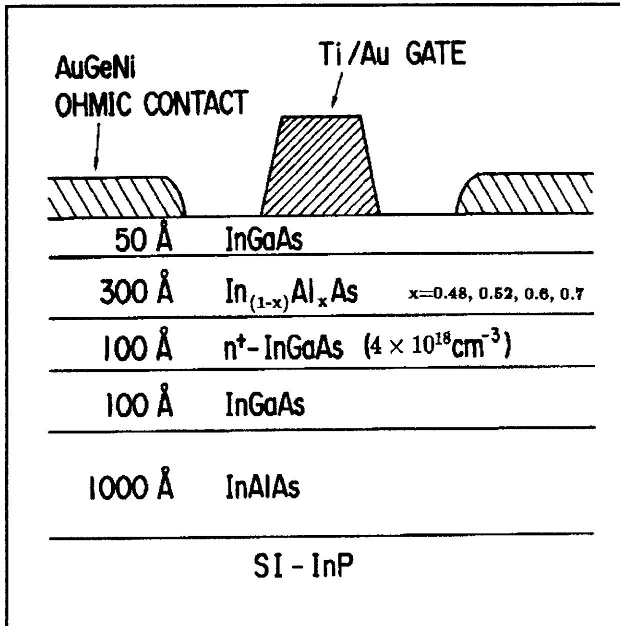

Figure 2. Cross section of device structure.

mS/mm).[3] We believe that is due to the enhanced channel doping in this new device structure.

An increase of AlAs composition in the $In_{(1-x)}Al_xAs$ gate insulator from the lattice-matched condition x = 0.48 to x = 0.6 brings about a slight reduction of peak g_m due to an enhanced contact resistance. First order theory predicts this result. A further increase of x to 0.7 results in a catastrophic reduction in g_m that cannot be explained by a larger source resistance. It appears that, from an electrical point of view, the critical layer thickness for the 300 Å $In_{(1-x)}Al_xAs$ insulator has been exceeded in going from x = 0.6 to x = 0.7.

While there is a small reduction of g_m with AlAs composition, the g_m curve broadens in V_{gs}, as figure 3 indicates, because gate current is being suppressed due to the enhanced conduction band discontinuity (discussed below). Thus, the maximum current driving capability of the devices is not degraded. In fact, this capability improves with AlAs composition up to 0.6. The maximum drain current obtained is 300 mA/mm for the x = 0.6 device. This is better than that which had been reported previously in similar devices and is a very competitive value for any 1.5 μm gate length HFET.

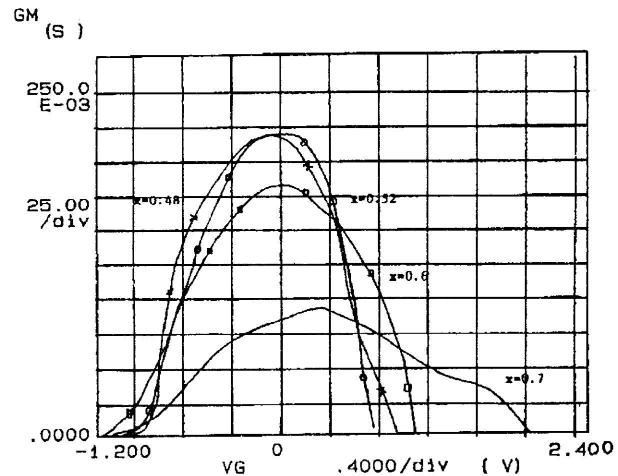

Figure 3. Transconductance versus gate to source voltage for V_{ds} = 4 V.

Increasing the AlAs composition results in a drastic reduction of forward gate current. Figure 4 illustrates gate current as a function of drain-source voltage for V_{gs} = 1.2 V. As the AlAs composition increases, gate current at all values of V_{ds} is drastically suppressed. This results in broader g_m versus V_{gs} characteristics (shown in figure 3) and higher $I_{D\,max}$, as mentioned above.

A more significant result, shown in figure 5, is the impact of AlAs composition on the real-space transfer of hot electrons from the channel to the gate. Such a phenomenon is very clearly observed in the devices with AlAs composition of 0.48 and 0.52. Its unique signature is an increase in the gate current as V_{ds} increases for a given V_{gs}. This increase is due to electrons that are heated by the high electric field prevalent inside the channel and then acquire sufficient energy to overcome the conduction band discontinuity between the channel and the gate insulator. The drain current saturates when the device itself enters saturation. An AlAs composition of 0.6 results in a sufficient conduction band discontinuity to completely suppress this phenomenon. This may be a major advantage of submicron strained-insulator MIDFETs in which the electric field in the channel can reach a very high value.

Figure 5 shows that real-space transfer of hot electrons to the gate causes a small negative differential output resistance. Because elec-

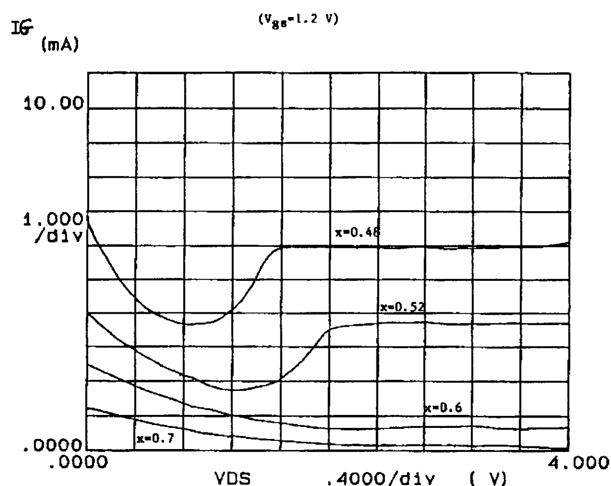

Figure 4. Gate current versus V_{ds} at $V_{gs} = 1.2$ V, as a function of AlAs composition.

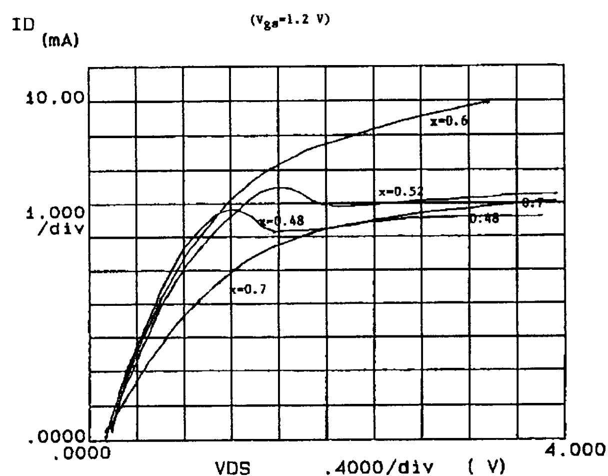

Figure 5. Drain current versus V_{ds} at $V_{gs} = 1.2$ V, as a function of AlAs composition.

trons are lost to the gate, this phenomenon results in drain current reduction. In addition, it may produce device instabilities and oscillations. For the x = 0.6 device, real-space transfer is completely suppressed and the drain current reaches higher values, as figure 5 indicates. Overall, the x = 0.6 device has ten times less gate current than the x = 0.48 device at practical operating points.

A final advantage of the strained-insulator MIDFETs is the enhanced reverse-bias gate breakdown voltage. Figure 6 shows the gate I-V characteristics measured with drain and source shorted. We obtain a rather hard breakdown for all devices. If we define breakdown at a reverse current of 1 mA, the breakdown voltage for the lattice matched device is 17 V. As the AlAs composition is increased in the insulator, the breakdown voltage increases very quickly, up to 28 V for x = 0.7.

The combination of the unique features investigated above makes strained-insulator InAlAs/n^+-InGaAs MIDFETs very suitable candidates for high-power microwave applications. Figure 7, for example, shows that $In_{0.40}Al_{0.60}As/n^+-In_{0.53}Ga_{0.47}As$ MIDFETs displayed excellent I-V characteristics up to $V_{ds} = 10$ V.

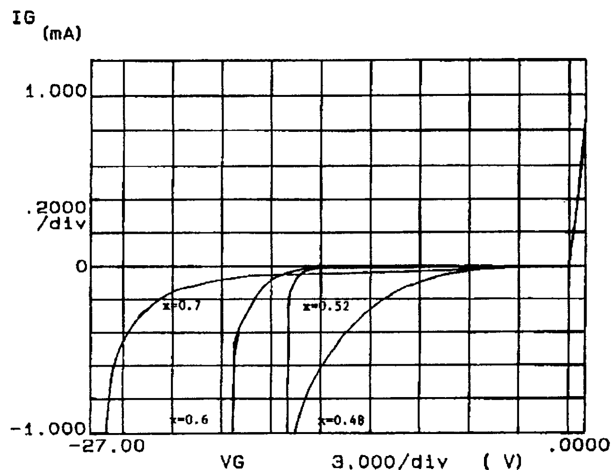

Figure 6. Reverse gate current characteristics of FETs as a function of AlAs composition $V_{ds} = 0$ V.

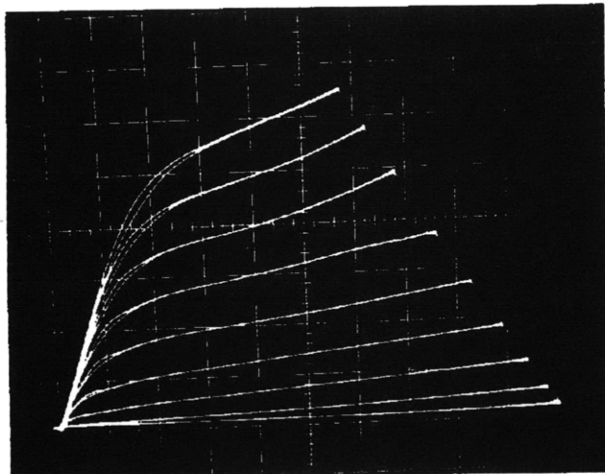

Figure 7. I-V characteristics of fabricated $In_{0.40}Al_{0.60}As/n^+-In_{0.53}Ga_{0.47}As$ MIDFET. Scales: I_D: 1mA/div,V_{ds}:1V-div,V_{gs}:0.2V/step, V_{gs}(max) = 0 V.

7.4 Publications

Bennett, B.R., and del Alamo, J.A. "Index of Refraction Anysotropy in Mismatched InGaAs/InP Heterostructures Measured by Ellipsometry." Paper presented at the Symposium on Layered Heterostructures - Heteroepitaxy, Superlattices, Strain and Metastability of the 1989 Fall Meeting Materials Research Society, Boston, Massachusetts, November 27-December 2, 1989. Symposium *Proceedings*. Forthcoming.

del Alamo, J.A., and Azzam, W.J. "A Floating-Gate Transmission-Line Model (FGTLM) Technique for Accurate Measurement of Source Resistance in HFETs." Paper presented at 1989 Workshop on Compound Semiconductor Materials and Devices, Hilton Head, South Carolina, February 20-22, 1989.

del Alamo, J. A. and Mizutani, T. "A Recessed-Gate $In_{0.52}Al_{0.48}As/n^+-In_{0.53}Ga_{0.47}As$ MIS-type FET." *IEEE Trans. Electron Devices* ED-36 (4): 646-650 (1989).

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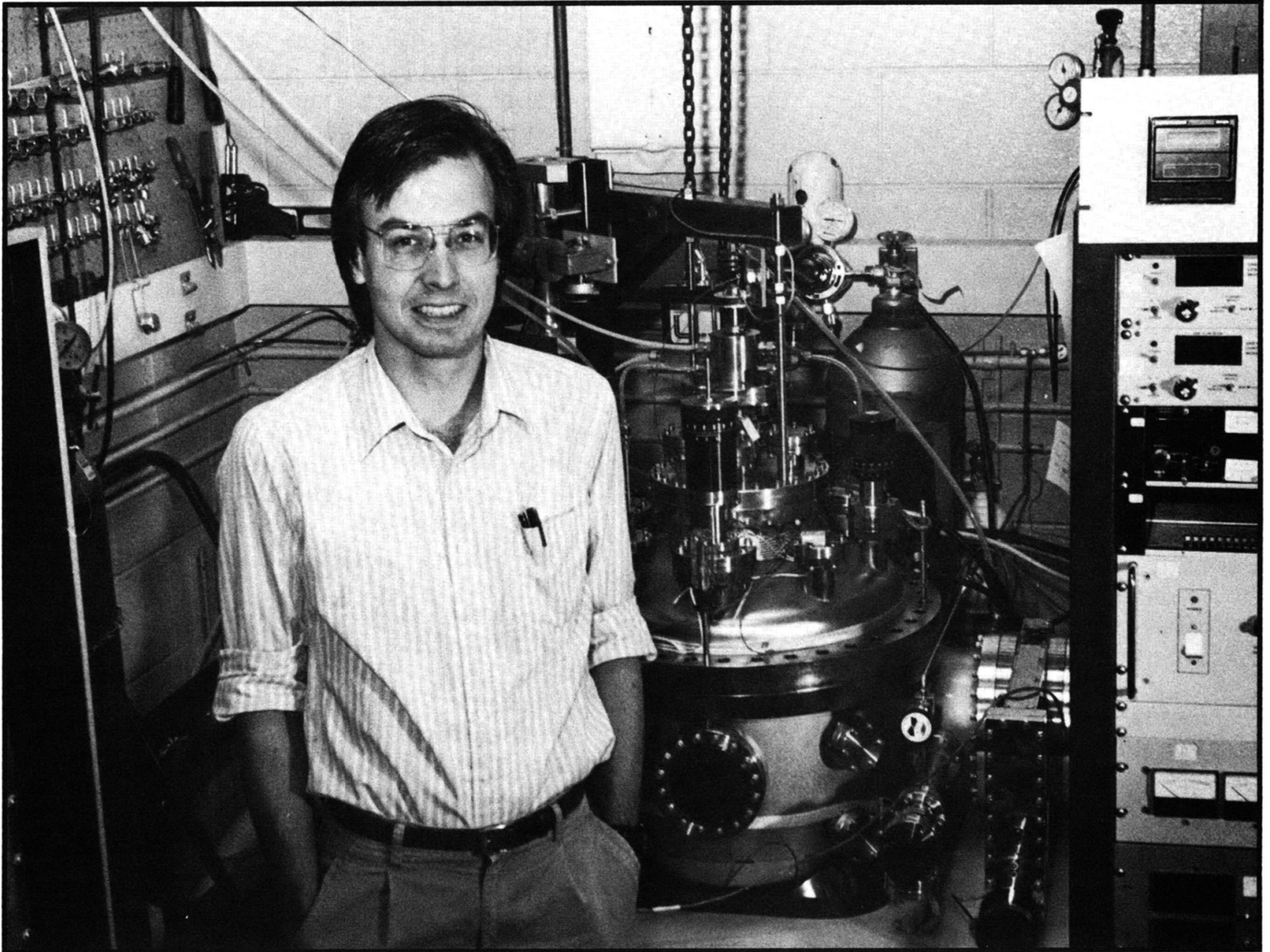
del Alamo, J.A., and Azzam, W.J. "A Floating-Gate Transmission-Line Model (FGTLM) Technique for Measuring Source Resistance in Heterostructure Field-Effect Transistors." *IEEE Trans. Electron Devices* 36 (11): 2386-2393 (1989).



Professor John M. Graybeal in his laboratory.