Chapter 2. Computer-Integrated Design and Manufacture of Integrated Circuits

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2.1 Introduction

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Computer-Aided Fabrication Environment (CAFE) is a software system being developed at MIT for use in the fabrication of integrated circuits (IC) and microstructures. The distinguishing feature of CAFE is that it can be used in all phases of process design, development, planning, and manufacturing of integrated circuit wafers. CAFE presently provides day-to-day support to research and production facilities at MIT with both flexible and standard product capabilities. This manufacturing software system is unique because a process flow representation (PFR) has been developed and integrated into actual fabrication operations. CAFE provides a platform for work in several active research areas including "technology" (process and device) computer-aided design (TCAD), process modeling, manufacturing quality control, and scheduling.

2.1.1 Architecture

The CAFE architecture is a computer-integrated manufacturing (CIM) framework for the deployment and integration of integrated circuit and process design and manufacturing software. CAFE uses an object-oriented database model which is implemented in a layered manner on top of a relational database. Our database schema is based on GESTALT, an object-oriented, extensible data model. GESTALT is a layer of abstraction which maps user defined objects onto existing database systems (e.g., a relational database management system) while shielding application programs from the details of the underlying database. The integration architecture includes conceptual schema and models used to represent the integrated circuits manufacturing domain in CAFE and user and programmatic interfaces to the various applications. Two important CAFE applications relate process simulation and actual wafer fabrication to the same PFR.

2.1.2 CAFE Applications

The fabrication of wafers with a process represented as a PFR involves several steps. A suitable PFR for the specific process must be created and installed. Then wafer lots must be created and associated with this specific PFR. These lots must then be "started" to create a task data structure which is isomorphic to the hierarchical structure of the PFR.

At this point, actual machine operations can be scheduled and reservations made for both machines and operators. Finally, machine operations can be performed, instructions given to the operator and machines, and data collected from the operator or machine and entered into the database.

Current work involves implementing hierarchical scheduling and using PFR for real time process control and integration of a mechanical TCAD system.

2.2 Principal Objectives

The primary objectives for 1992 were (1) evaluation of the results of the initial experiments with fabrication via PFR, (2) development of applications and improvements responsive to the initial users' comments and suggestions, (3) integration of these improvements into CAFE, and (4) continued use of PFR fabrication for lots using the CMOS baseline process. A fifth objective was to develop an application to serve as the initial integration of the Run-by-Run (RbR) control project into the CAFE software system.

2.3 Principal Accomplishments

2.3.1 Implementation of PFR-based Fabrication

The fabrication of wafers with a process represented as a PFR involves several steps. A suitable PFR must be created and installed to create persistent flow objects. The tree structure of these flow objects reflects the hierarchical decomposition of PFR encoding. Wafer lots must then be created and associated with this PFR. These lots are then "started" to create a task data structure which is isomorphic to the flow data structure. The tasks point to flow objects, and these tasks are used to record lot specific information because multiple lots are usually fabricated from a single flow. At this point, actual machine operations can be scheduled and reservations made for both machines and operators. Finally, the actual machine operations can be performed, instructions given to operator and machines, and data collected from operator or machine and entered into the database.

2.3.2 Processing of All CMOS Baseline Defect Array Lots via PFR

Several lots have been processed via PFR for the MIT CMOS baseline process. All future fabrication runs of the MIT CMOS baseline process used to process test lots known as defect array (DA) lots will be processed with the aid of our PFR-based fabrication. All operations are driven by the CAFE system using a PFR-based representation of the process. Settings and operator instructions are displayed (some are downloaded automatically), and specified readings and data are collected via operator entry or, in some cases, automatically. Both types of information are stored in the GESTALT database. The report generators access the database to retrieve the data and present it in a form suitable for the user.

2.3.3 Development of PFR-based Split Lot Processing Capabilities

We have augmented the MIT PFR to include a mechanism for user specified split lot processing. Users can now specify which wafers in a lot are to be processed by a subflow. With this mechanism, users can specify different parameters or, indeed, completely different processing for individual wafers or groups of wafers.

2.3.4 Traveler and "Op-set" Report Generators In Use

We have completed projects to produce report generators to replace the traveler and "Op-set" reports now in use in our Integrated Circuits Laboratory (ICL) and Technology Research Laboratory (TRL). The traveler reports provide a succinct summary of the current state of processing for a lot augmented with details concerning past and planned special activities. These include (1) when the lot was put on hold, (2) reasons for putting the lot on hold, and (3) what was done to remove the hold status. The Op-set reports are more expansive, including details of processing, recipes used, operator instructions gleaned from PFR, and measurements and other data that were collected in accordance with the PFR used for processing the lot.

2.3.5 Initial Integration of Run-by-Run Control into CAFE

Applications implementing a first integration of RbR process control into the MIT Computer Integrated Manufacturing (CIM) system (CAFE) have been developed. Object oriented data structures have been designed and implemented to support the setup of the RbR control project and ongoing control calculations. The actual processing of wafers is conducted via PFR-based fabrication applications.

This initial control experiment uses a simple process consisting of a pre-process measurement, an oxide etching step, and a post-process measurement. A Nanospec is used for both measurements, and data sent via the RS 232 interface for the Nanospec are automatically collected and stored in the database in accordance with information specified in a PFR. A LAM Model 590 plasma etcher is interfaced to a PC via a SECS II RS 232 link. Etch recipes are uploaded and downloaded to a disk on the computer running CAFE via PCNFS. The soft-

ware which dynamically modifies the etch recipes runs under the CAFE CIM system.

The CAFE system was intended to be used in all phases of process design, development, planning, and manufacturing of integrated circuits. CAFE was to provide a platform for work in TCAD, process modeling, and manufacturing quality control. A requirement for the CAFE architectural framework was to support a wide variety of software modules, including both development tools and on-line applications. The key components of the CAFE architecture are the data model and database schema, user interface, process flow and wafer representations, and application programming and database interfaces.

Particular emphasis was placed on the use of a single PFR to drive both simulation and fabrication and the actual use of PFR-based fabrication in our ICL.

2.3.6 CAFE Installed and Operational at Case Western Reserve University

The CAFE software system has been successfully installed at Case Western Reserve University in Cleveland, Ohio. The hardware configuration consists of a Sun Sparc 2 Workstation with 48 megabytes of memory and a 1 gigabyte disk. This installation required purchase of an INGRES license. Installation was accomplished via network. Several days of familiarization and system manager training were provided at MIT for Case personnel.

2.3.7 PFR-driven Simulation Manager

We have developed a rather remarkable system for the simulation of IC processing from our PFR. Users can enter and/or edit their process flow representation and then run SUPREM III simulations without knowing it specifically. A key feature of this software is the "validator" which checks the validity of previous simulation computations and retains any valid computations after the PFR has been modified. Thus computation time is minimized while maintaining correctness of the final simulations. This software also allows the user to conveniently generate reports, such as plots of impurity concentrations and calculations of sheet resistance, etc.

2.3.8 Dynamic Modification of PFR-based Fabrication Provided

Initial experience with PFR-based fabrication resulted in user requests for applications to enable dynamic modification of fabrication plans. Users wanted to be able to skip planned operations, as well as to insert new operations (or sequences of operations) at arbitrary points in the processing plan. In addition, users wanted to revise their processing plan (and its associated PFR) and fabricate according to this new plan as if it had been in effect from the start. A restart lot mechanism has been provided which permits a user to initiate processing with the best estimate of all future processing. If, in the course of fabrication processing, the user realizes that some modifications are required for future processing of this lot, then the user can edit the PFR and initiate the restart lot operation. The restart lot function will verify that the new PFR calls for precisely the same fabrication operations as the former PFR for all processing that has already been accomplished. This check ensures that actual, completed processing history is not changed. If it is, then this restart lot operation fails; and the program informs the user. If the new PFR passes this test, then the former task structure is deleted and replaced by a new task structure corresponding to the new PFR.

2.3.9 X-based PFR Flow and Task Browser Enables Global View of Hierarchical Structure

An X-based application enables users to browse through the tree structures of either installed PFR flows or the tasks associated with a lot being processed with a PFR-based flow. In addition to providing the user with a more global perspective than provided by individual machine operations, this browser enables detailed examination of task or flow attributes at any point in the hierarchy. It also enables users to easily specify tasks to be skipped and places in the task hierarchy for insertion of additional flows.

2.3.10 User Friendly Hold Application Developed

A fabform-based application has been developed to facilitate the creation of a PFR appropriate to the specification of a hold status for a lot. This application queries the user and collects the reason for placing the lot on hold as well as the necessary conditions for removing the lot from the hold status. A new PFR is then automatically generated, installed, and the corresponding task tree is gener-

ated and installed in the task structure associated with the lot. In a subsequent operation, an operator will be presented with this information and, when the hold status is removed, the operator will enter the appropriate information as specified in this new PFR subflow.

2.3.11 GESTALT Extended to Support Inheritance and CLOS

The current version of GESTALT now supports inheritance and provides transparent access to persistent objects, which are described and manipulated solely via CLOS constructs. This transparency simplifies applications programming, as it frees the programmer from the task of translating between programming language structures and database structures, which is required in many systems. Applications programmers may utilize the rich object modeling, generic functions, interactive debuggers, interpreters, etc., present in the CLOS environment to further simplify programming.

2.4 Process Flow Representatation

Project Staff

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The objective of this project is the development of a Process Flow Representation (PFR) for the integration of technology (process and device) CAD (TCAD) into integrated circuits semiconductor computer-integrated manufacturing (CIM). The effort has proceeded on three major fronts: fundamental modeling, application to process design and fabrication at MIT, and cooperative work with industry to define and test a process representation standard.

For high performance computing systems and other advanced technology, concurrence in the design of the product, manufacturing process, and factory is crucial. The goal is to achieve fully integrated design and manufacture in which the boundary between design and manufacturing domains is eliminated. In particular, information from the manufacturing floor is continuously available from the earliest stages of process and device design onward, while the manufacturing process, developed concurrently with the product, continues to undergo design improvement and modification while in production. Computer-integrated design and manufacture (CIDM), therefore, requires a coherent manufacturing process representation capable of storing information from a variety of different knowledge domains and disciplines, and supporting access to this information in a consistent manner. We believe that our general semiconductor process modeling framework organizes the complexity of this interrelated information and puts our PFR on a sound footing by giving it clear semantics.

A high-level conceptual model for describing and understanding semiconductor manufacturing processing is a crucial element of both the CIDM research program and software frameworks for TCAD and CIM, including the MIT Computer Aided Fabrication Environment (CAFE). Initially a "two-stage" generic process step model was used. This described processing steps in terms of two independent components: (1) an equipment-dependent, wafer-independent stage, which maps equipment settings to physical processing environments, and (2) an equipment-independent, wafer-dependent stage, which relates physical environments to changes in the input wafers. Driven by the needs of process control and optimization research, including sophisticated modeling, design, and experimental model verification, our fundamental conceptual process model has evolved from the two-stage generic process model into one which is part of a more general process modeling framework, in which the earlier two-stage model is a special case. Our approach to process representation for both TCAD and CIM is based on this general modeling framework for semiconductor processing. In this framework, state information (e.g., wafer, environment, and equipment state), and models, or transformations, that describe relationships between state descriptions, are formally identified and described. The purpose of this comprehensive framework is to enable an effective representation that can be used throughout the IC semiconductor process life-cycle, from early conception and design phases through fabrication and maintenance.

In the MIT CAFE system, the PFR is expressed in a textual (ASCII) format and then converted into GESTALT objects and loaded into the CAFE database. The textual language of the PFR is extensible, so that it can flexibly accommodate changes and extensions to both the underlying modeling methodology and the needs of specific applications. The object-oriented nature of the GESTALT database interface enables the convenient evolutionary development of CAFE software applications built around the PFR. The PFR allows process step descriptions to be "underdetermined," for example, by expressing only the wafer-state change, making it possible to develop a process incrementally with increasing degrees of detail. In addition to expressing the fundamental concepts of wafer transformation within individual process steps, the PFR supports both hierarchical and parameter abstraction and embedded computation, thereby

providing support for modular process design and development. Processes expressed in the PFR can be simulated using a variety of technology CAD tools; PFR extensibility allows the incorporation of both simulator-dependent and simulator-independent information. A simulation manager application uses the appropriate information in the PFR along with knowledge of specific simulators to invoke simulation tools and maintain simulation state.

Extensions to the textual PFR and corresponding database schema support specification of individual wafers or wafersets (sublots or splits) within a lot for processing, and specification of engineering holds at a particular step in the process sequence. An engineering hold might be planned, for example, as part of the fabrication specification for a process which is currently under experimental development. In conjunction with developments in CAFE that support dynamic modificaton of processes in the fabrication line, the "hold" capability in the PFR can also be used in response to unexpected events that occur during fabrication. With these manufacturing extensions, the PFR is used in the CAFE system at the MIT ICL for the fabrication processes supported by the ICL technical staff, with all processing operations driven by CAFE from the PFR stored in the database.

Work has also proceeded on the definition of a standard semiconductor process representation (SPR) for use in both industry and research fabrications, in association with the industry CAD Framework Initiative (CFI) Technical Subcommittee on Technology CAD in defining broadly applicable TCAD framework standards. Mr. McIlrath is currently the chair of the working group on SPR. Based largely on the conceptual process model described above, a high-level information model of semiconductor processes is being developed in conjunction with Motorola, IBM, Texas Instruments, and other industry and university representatives. A prototype SPR implementation and a programming interface have been developed and employed in an experimental TCAD framework, which included an implementation of the semiconductor wafer representation (SWR), and tools developed by industry and other university researchers. An industry survey of specific itemized requirements for SPR has been completed and published as part of a formal CFI Request for Technology, which identifies mandatory requirements and evaluation criteria for complete SPR proposals now under consideration by the working group.

2.5 Technology CAD Framework

Project Staff

Michael B. McIlrath

Contemporary large-scale software system engineering emphasizes frameworks, wherein common structure and interface specifications enable both current and future software components to be integrated in a flexible and modular way. Software may be roughly divided into tools, such as a simulator, which perform some part of an application task, and services, such as a database, which provide some necessary support capability used by various tools. With framework standards, reusable, interchangeable software components from various suppliers may be deployed in systems which comply with the standard. In the broad sense, a framework standard specifies:

- data representations for the objects of discourse in the application domain and their semantics, and programmatic interfaces to those representations, and
- architecture; that is, interactions among software components (tools and services), and how tools fit together to perform tasks for the user.

Frameworks have been particularly successful in development of electronic circuit CAD systems. Standards for CAD frameworks are currently being established by the CFI, a broad organization of vendor and user companies which has now expanded its scope to include technology (process and device) CAD. A TCAD framework standard includes programming representations for the fundamental objects of process and device CAD: physical structures on the wafer, manufacturing process, and structure and behavior of the resulting devices. A TCAD framework standard also specifies how application software is structured to use these representations and the underlying software services in process and device design and simulation activities.

At present, development of TCAD framework architectural standards is limited to (1) specifications of implementation and interfaces for the wafer and process representations, (2) use of domain-independent framework standards, such as intertool communication (ITC), user interface (UI), and (3) extension language specifications. We are beginning to look at higher level architectural issues, such as the interrelationships between the framework data representations and the connection of compliant tools to achieve end-user design objectives. We are also investigating the larger

questions of the relationship between frameworks for different related domains (e.g., circuit CAD and TCAD), and the integration of design frameworks into frameworks for CIM.

We are currently active as members of the TCAD Technical Subcommittee (TSC) of the CFI, contributing to fundamental modeling, implementation (language and database technology), programmatic interfaces, prototyping development, and relation to overall CIM and TCAD architectural frameworks.

2.6 Publications

Journal Articles

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