Chapter 2. Computer-Integrated Design and Manufacture of Integrated Circuits

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2.1 Introduction

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Computer-Aided Fabrication Environment (CAFE) is a software system being developed at MIT for use in the fabrication of integrated circuits and microstructures. The distinguishing feature of CAFE is that it can be used in all phases of process design, development, planning, and manufacturing of integrated circuit wafers. CAFE presently provides day to day support to research and production facilities at MIT with both flexible and standard product capabilities. This manufacturing software system is unique in its development of a process flow representation which is integrated into actual fabrication operations. CAFE provides a platform for work in several active research areas, including "technology" (process and device) computer-aided design (TCAD), process modeling, manufacturing quality control, and scheduling.

2.1.1 Architecture

The CAFE architecture is a computer integrated manufacturing (CIM) framework for the deployment and integration of integrated circuits (IC) circuit and process design and manufacturing software. CAFE uses an object-oriented database model which is implemented in a layered manner on top of a relational database. Our database schema is based on GESTALT, an object-oriented, extensible data model. GESTALT is a layer of abstraction which maps user defined objects onto existing database systems (e.g., a relational DBMS) and shields application programs from the details of the underlying

database. The integration architecture includes the conceptual schema and models used to represent the IC manufacturing domain in CAFE and the user and programmatic interfaces to the various applications. Two important CAFE applications relate process simulation and actual wafer fabrication to the same process flow representation.

2.1.2 CAFE Applications

The fabrication of wafers with a process represented as a process flow representation (PFR) involves several steps. A suitable PFR for the specific process must be created and installed. Wafer lots must be created and associated with this specific PFR. These lots must then be "started" to create a task data structure which is isomorphic to the hierarchical structure of the PFR.

At this point, actual machine operations can be scheduled and reservations made for both machines and operators. Finally, the machine operations can be performed, instructions given to the operator and machines, and data collected from the operator or machine and entered into the database.

Current work involves the implementation of hierarchical scheduling, development of factory design tools, real time process control using the PFR, and integration of a TCAD system using the PFR.

2.2 Principal Objectives

There were two principal objectives: (1) installation of CAFE at MIT Lincoln Laboratory and (2) development of a microsystems factory representation (MFR).

2.2.1 MIT Lincoln Laboratory Installation

MIT Lincoln Laboratory has selected CAFE as the CIM system for use in a new IC processing facility. CAFE is now in operation at Lincoln Laboratory, and multiple lots are being processed daily via PFR-based fabrication. Lincoln Laboratory is committed to having all the wafers processed in this facility with PFR-based fabrication.

2.2.2 Microsystems Factory Representation

We have embarked on a new research initiative to develop a microsystems factory representation (MFR). The goal of the MFR is to be a powerful, common language with which semiconductor factories can be described unambiguously. MFR will be used to organize static data pertaining to resources of production systems. That is, it will describe all attributes of the factory that do not change very often. The MFR, the state (and its evolution), the PFR, the demand, and the scheduler will provide all data necessary for simulations, analytical calculations of performance measures, and for the implementation of factory controllers. A system created from these items can represent either a real factory or a simulation of a factory. The only difference is in the state and its dynamics. In a real factory, events occur either as a result of decisions made by the scheduler (controllable events such as loading lots) or at random (uncontrollable events such as machine failures). In a simulation, the random events are synthesized by means of a random number generator.

2.3 Principal Accomplishments

2.3.1 CAFE Installation at MIT Lincoln Laboratory and Expanded PFR-Based IC Fabrication

The CAFE architectural framework at Lincoln Laboratory supports a wide variety of software modules including both development tools and on-line applications. The key components of the CAFE architecture are the data model and database schema, process flow representation, user interface, and application programming and database interfaces. The approach of the MIT PFR is to use the same representation for multiple purposes including simulation, scheduling, process control, and fabrication. The PFR provides an extensible framework for process steps including knowledge about instructions to operators and equipment, scheduling requirements, changes effected to the wafer product, and physical process model parameters.

A primary reason for this selection is that CAFE supports PFR-based fabrication and has demonstrated process simulation driven by the same PFR. Other reasons include CAFE's use of a robust commercial database, provision of an ASCII process definition, flexible process descriptions, handling of splits and joins, and satisfactory user interface support. In conjunction with this selection, there have been substantial improvements in CAFE. The speed of operation has been dramatically increased, and a number of significant new applications have been developed. An important enhancement was the ability to execute applications in the background and at slack times in the evening or early morning. An important, new application developed displays the queue of lots available for processing at a machine or set of machines.

A major task was to write a large number of unit processes into the PFR. A new application was developed to enable production of detailed reports from a PFR-based encoding without actually installing the process. Changes and enhancements to the PFR and utility functions which facilitated the expression of the required processing will be described. In addition, a scheme for sharing of installed process flows has been provided.

2.3.2 Microsystems Factory Representation

The microsystems factory representation (MFR) is conceived to be a powerful, common language with which semiconductor factories can be described unambiguously. The MFR will specify the organization of static data pertaining to resources of production systems; that is, it will describe all attributes of the factory that do not change very often. The MFR will also specify the static data itself and the organization of the dynamic data.

The MFR is designed to be used in conjunction with a set of representations of other semiconductor factory data. They include:

- 1. The state of the factory, a list of all relevant dynamic information. The evolution of the state provides a history of the factory's activities.
- The process flow representation (PFR), a representation of the process that is used to produce a given product.
- The demand, all information available about future requirements including known specific orders, long range forecasts, and any statistical measures of uncertainty.
- The scheduler and the set of rules by which the factory is run. The scheduler takes infor-

mation from the current state, MFR, PFR, and demand, and makes a decision about which operation to do next, where to move lots, etc. This decision, when implemented, determines the next value of the state.

The MFR, state (and its evolution), PFR, demand, and scheduler will provide all necessary data for simulations, analytical calculations of performance measures, and implementation of factory controllers. When a system is created from these items, the state evolves; reports are generated that summarize the behavior of the state over time. These reports include such performance measures as average in-process inventory, mean cycle time, machine utilization, etc.

The system created in this manner can represent either a real factory or a simulation of a factory. The only difference is in the state and its dynamics. In a real factory, events occur either as a result of decisions made by the scheduler (controllable events such as loading lots) or at random (uncontrollable events such as machine failures). In a simulation, the random events are synthesized by means of a random number generator.

One important goal of our approach to scheduling and simulation is that the MFR and PFR, and their use, are designed to be the same, whether they are part of a real-time factory management system, or a simulation of a factory. Future demand information can also be used in the same way, whereas current orders may have to be synthesized in a simulation.

2.4 Process Flow Representation

Project Staff

Professor Donald E. Troxel, Michael B. McIlrath

The objective of this project is the development of a process flow representation (PFR) for the integration of technology (process and device) CAD (TCAD) into IC semiconductor computer integrated manufacturing (CIM). The effort has proceeded on three major fronts: fundamental modeling, application to process design and fabrication at MIT, and cooperative work with industry to define and test a process representation standard.

For high performance computing systems and other advanced technology, concurrence in the design of the product, manufacturing process, and factory is crucial. The goal is to achieve fully integrated design and manufacture, in which the boundary between design and manufacturing domains is eliminated. In particular, information from the manufacturing floor is continuously available from the

earliest stages of process and device design onward. Conversely, the manufacturing process, developed concurrently with the product, continues to undergo design via improvement and modification while in production. Computer integrated design and manufacture (CIDM), therefore, requires a coherent manufacturing process representation which is capable of storing information from a variety of different knowledge domains and disciplines as well as supporting access to this information in a consistent manner. We believe that our general semiconductor process modeling framework organizes the complexity of this interrelated information and puts our PFR on a sound footing by giving it clear semantics.

A high level conceptual model for describing and understanding semiconductor manufacturing processing is a crucial element of both the CIDM research program, and of software frameworks for TCAD and CIM, including the MIT Computer Aided Fabrication Environment (CAFE). Initially a "twostage" generic process step model was used, which described processing steps in terms of two independent components: (1) an equipment-dependent, wafer-independent stage, which maps equipment settings to physical processing environments, and (2) an equipment-independent, wafer-dependent stage, which relates physical environments to changes in the input wafers. Driven by the needs of process control and optimization research, including sophisticated modeling, design, and experimental model verification, our fundamental conceptual process model has evolved from the two-stage generic process model into one which is part of a more general process modeling framework, in which the earlier two-stage model is a special case. Our approach to process representation for both TCAD and CIM is based on this general modeling framework for semiconductor processing. In this framework, state information (e.g., wafer, environment, and equipment state), and models, or transformations, that describe relationships between state descriptions, are formally identified and described. The purpose of this comprehensive framework is to enable an effective representation that can be used throughout the IC semiconductor process life-cycle, from early conception and design phases through fabrication and maintenance.

In the MIT CAFE system, the PFR is expressed in a textual (ASCII) format and then converted into Gestalt objects and loaded into the CAFE database. The textual language of the PFR is extensible, so that it can flexibly accommodate changes and extensions to both the underlying modeling methodology and the requirements of specific applications. The object-oriented nature of

the Gestalt database interface enables the convenient evolutionary development of CAFE software applications built around the PFR. The PFR allows process step descriptions to be "underdetermined"; for example, by expressing only the wafer-state change, making it possible to develop a process incrementally with increasing degrees of detail. In addition to expressing the fundamental concepts of wafer transformation within individual process steps, the PFR supports both hierarchical and parameter abstraction and embedded computation, thereby providing support for modular process design and development. Processes expressed in the PFR can be simulated using a variety of technology CAD tools; PFR extensibility allows the incorporation of simulator-dependent and A simulation manager independent information. application uses the appropriate information in the PFR along with knowledge of specific simulators to invoke simulation tools and maintain a simulation state.

Extensions to the textual PFR and to the corresponding database schema support specification of individual wafers or wafersets (sublots, or splits) within a lot for processing, and specification of engineering holds at a particular step in the process sequence. An engineering hold might be planned, for example, as part of the fabrication specification for a process which is currently under experimental development. In conjunction with developments in CAFE that support dynamic modification of processes in the fabrication line, the "hold" capability in the PFR can also be used in response to unexpected events that occur during fabrication. With these manufacturing extensions, the PFR is used in the CAFE system at the MIT Integrated Circuits Laboratory (ICL) for the fabrication processes supported by the ICL technical staff, with all processing operations driven by CAFE from the PFR stored in the database.

Work has also proceeded on the definition of a standard semiconductor process representation (SPR) for use in both industry and research fabs, in association with the industry CAD Framework Initiative (CFI) Technical Subcommittee on Technology CAD in defining broadly applicable TCAD framework standards. Michael McIlrath is currently the chair of the working group on SPR. Based largely on the conceptual process model described above, a high level information model of semiconductor processes is being developed in conjunction with Motorola, IBM, and Texas Instruments, and other industry and university representatives. A prototype SPR implementation and programming interface has been developed and employed in an experimental TCAD framework, which included an impleof mentation the semiconductor wafer representation (SWR) and tools developed by industry and other university researchers.

2.5 Technology CAD Framework

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Michael B. McIlrath

Contemporary large-scale software system engineering emphasizes frameworks, wherein common structure and interface specifications enable both current and future software components to be integrated in a flexible and modular way. Software may be roughly divided into tools, such as a simulator, which perform some part of an application task, and services, such as a database, which provide some necessary support capability used by various tools. With framework standards, reusable, interchangeable software components from various suppliers may be deployed in systems which comply with the standard. In the broad sense, a framework standard specifies:

- data representations for the objects of discourse in the application domain and their semantics, and programmatic interfaces to those representations, and
- architecture; that is, interactions among software components (tools and services), and how tools fit together to perform application tasks for the user.

Frameworks have been particularly successful in the development of electronic circuit CAD systems. Standards for CAD frameworks are currently being established by the CAD Framework Initiative (CFI), a broad organization of vendor and user companies which has now expanded its scope to include technology (process and device) CAD. A technology CAD (TCAD) framework standard includes programming representations for the fundamental objects of process and device CAD: the physical structures on the wafer, the manufacturing process, and the structure and behavior of the resulting devices. A TCAD framework standard also specifies how application software is structured to use these representations and the underlying software services in process and device design and simulation activities.

At present, development of TCAD framework architectural standards has been limited to (1) specifications of implementation and interfaces for the wafer and process representations and (2) use of domain-independent framework standards, such as intertool communication (ITC), user interface (UI), and extension language specifications. We are investi-

gating higher-level architectural issues, such as the interrelationships between the framework data representations and the connection of compliant tools to achieve end-user design objectives. We are also looking at the larger questions of the relationship between frameworks for different related domains (e.g., circuit CAD and TCAD) and integration of design frameworks into frameworks for CIM.

2.6 Publications

Internal Publications

- Ahn, S., S. Gershwin, M. Stamatopoulos, and D.E. Troxel. *MFR Textual Representation*. CIDM Memo 93-11. MIT, 1993.
- Boning, D.S., and M.B. McIlrath. *Guide to the Process Flow Representation, Vers. 3.1.* CIDM Memo 93-17. MIT, 1993.
- Fischer, G. *The CAFE Accounting Package On FAB.* CIDM Memo 93-9. MIT, 1993.
- Fischer, G.T., and D.E. Troxel. Writing PFRs for Use in Fabrication. CIDM Memo 93-18. MIT, 1993.
- Gershwin, S., D.E. Troxel, S. Ahn, A. Bonvik, N. Srivatsan, and M. Stamatopolous. *Efficient Capital Utilization in Semiconductor Fabrication*. CIDM Memo 93-20. MIT, 1993.
- Lohman, T.J. *The CAFE Lab Terminal Management System.* CIDM Memo 93-10. MIT, 1993.
- Lohman, T.J. *CAFE Ingres Requirements.* CIDM Memo 93-19. MIT, 1993.
- Lohman, T.J. *The Gestalt Database System—An Overview.* CIDM Memo 93-21. MIT, 1993.
- McIlrath, M.B. *Shared Process Flows.* CIDM Memo 93-8. MIT, 1993.
- Stamatopolous, M., D.E. Troxel, and S. Gershwin. Microsystems Factory Representation. CIDM Memo 93-2. MIT, 1993.

- Stamatopolous, M., D.E. Troxel, S. Ahn, and S. Gershwin. *Microsystems Factory Representation*. CIDM Memo 93-6. MIT, 1993.
- Troxel, D.E. Release 5.0 of CAFE. CIDM Memo 93-3. MIT, 1993.
- Troxel, D.E. *Release 5.1 of CAFE*. CIDM Memo 93-7. MIT, 1993.

Meetings and Presentations

- McIlrath, M.B. Chair, SPR Working Group Meeting, Waltham, Massachusetts, April 1993.
- McIlrath, M.B. "Process Flow Representation for TCAD Frameworks," SEMATECH, Dallas, Texas, April 22, 1993.
- McIlrath, M.B. "Process Flow Representation in Computer Integrated Design and Manufacturing Research." SEMATECH, Dallas, Texas, April 22, 1993.
- McIlrath, M.B. Session Chair at the SRC/ARPA CIM-IC Workshop, Carnegie Mellon University, Pittsburgh, Pennsylvania, August 24-26, 1993.
- Stamatopolous, M., D.E. Troxel, S. Ahn, and S. Gershwin, "Microsystems Factory Representation." (Abstract) Presentation at the Eighth Annual SRC/ARPA CIM-IC Workshop, Carnegie Mellon University, Pittsburgh, Pennsylvania, August 24-26, 1993.
- Troxel, D.E., J.M. Knecht, T.M. Murguia, G.R. Young, and T.J. Lohman. "CAFE Installation at the Lincoln Laboratory and Expanded PFR Based IC Fabrication." (Abstract) Presentation at the Eighth Annual SRC/ARPA CIM-IC Workshop, Carnegie Mellon University, Pittsburgh, Pennsylvania, August 24-26, 1993.
- Troxel, D.E. "CAFE Installation at Lincoln Laboratory," Presentation at the MIT MTL Research Review, September 21-22, 1993. (CIDM Memo 93-16)

Thesis

Woo, A.R. *A Generic Graphical Tree Editor for Wafer Processing.* S.M. thesis, Dept. of Electr. Eng. and Comput. Sci., MIT, 1993.