Chapter 4. Nanostructures Technology, Research, and Applications

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4.1 NanoStructures Laboratory

The NanoStructures Laboratory (NSL) at MIT develops techniques for fabricating surface structures with feature sizes in the range from nanometers to micrometers and uses these structures in a variety of research projects. The NSL includes facilities for lithography (photo, interferometric, electron beam, and x-ray), etching (chemical, plasma and reactive-ion), liftoff, electroplating, sputter deposition, and e-beam evaporation. Much of the equipment and nearly all the methods utilized at the NSL are developed in-house. This is because commercial processing equipment, designed for the semiconductor industry, generally cannot achieve the resolution needed for nanofabrication, is inordinately expensive, and lacks the required flexibility.

Research projects within the NSL fall into three major categories: (1) development of submicron and nanometer fabrication technology, (2) short-channel semiconductor devices, quantum-effect electronics, and microphotonics, and (3) periodic structures for x-ray optics, spectroscopy, atomic interferometry and nanometer metrology.

4.2 Scanning-Electron-Beam Lithography

Sponsor

Joint Services Electronics Program
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Project Staff

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Figure 1 is a photograph of the scanning-electron-beam lithography (SEBL) system (VS-PL) located in Room 38-185. This instrument was obtained as a donation from IBM in November 1993. The digital pattern generator is based on a commercial high-performance array processor, which utilizes dual RISC processors. The system is capable of creating large-area patterns composed of multiple stitched fields. Conversion software has been developed which allows a CAD data file to be fractured and translated prior to exposure by the electron-beam tool.

The VS-PL system is the cornerstone of a facility for high-performance, large area (up to eight-inch wafers) electron-beam lithography at linewidth down to ~70 nm. The goals of the facility are to (1) provide the MIT research community with an in-house SEBL capability for writing directly on experimental device substrates; (2) advance the state-of-the-art in SEBL, particularly with regard to pattern placement accuracy and long-range spatial-phase coherence; and (3) pattern x-ray nanolithography masks for in-house use. In order to enable writing concentric circular patterns such as Freznel zone plates, software was developed to generate arbitrary arcs of an annulus with user specified start and finish radii and angles.

Figure 1. Photograph of the VS-PL scanning-electron-beam lithography system. The operator is Research Specialist Mark K. Mondol.

In 1997, the VS-PL was used in the direct-write mode to create patterns on substrates for a variety of projects including: 1D photonic bandgap structures, 3D photonic bandgap structures, 100 nm-period magnetic pillars, and zone plates on SiNx membranes. X-ray masks were written for: short channel MOSFETs, 1D photonic bandgap waveguides, T-gate MESFETs and mask-alignment experiments. VS-PL was also used extensively in experiments on spatial-phase-locked e-beam lithography.

4.3 Spatial-Phase-Locked Electron-Beam Lithography

Sponsors

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Semiconductor Research Corporation
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Grant DAAH04-95-1-0564

Project Staff

Dr. James G. Goodberlet, Alex Bernshteyn, Juan Ferrera, Mark K. Mondol, Professor Henry I. Smith

Electron-beam lithography (EBL) is the most effective method of creating patterns of arbitrary geometry on photomasks and x-ray masks. In conventional EBL systems, the precision with which patterns can be placed on a substrate (3σ = 30 nm to 100 nm) is significantly poorer than required for future deep-sub-micron and sub-100 nm IC lithography. Our research in spatial-phase-locked electron-beam lithography (SPLEBL) will improve the writing precision of the EBL system to $\sim 3\sigma < 2$ nm, about an order of magnitude better than conventional systems.

In contrast to conventional EBL systems, which employ indirect referencing, i.e., inferring the position of the e-beam from information about the substrate-holding stage's position, SPLEBL employs direct referencing to a fiducial grid placed directly on the substrate, as shown in Figure 2. In SPLEBL, the interaction of the e-beam with the fiducial grid creates a periodic signal which provides information about the position of the e-beam. One mode of SPLEBL, the segmented-grid mode, was used in 1994 to pattern spatially-coherent gratings for integrated-optical devices that spanned many EBL fields. In essence, the stitching error was eliminated. Another version of SPLEBL, the global-fiducial-grid (GFG) mode, is presently under development as a general two-dimensional scheme for precision mask-writing.

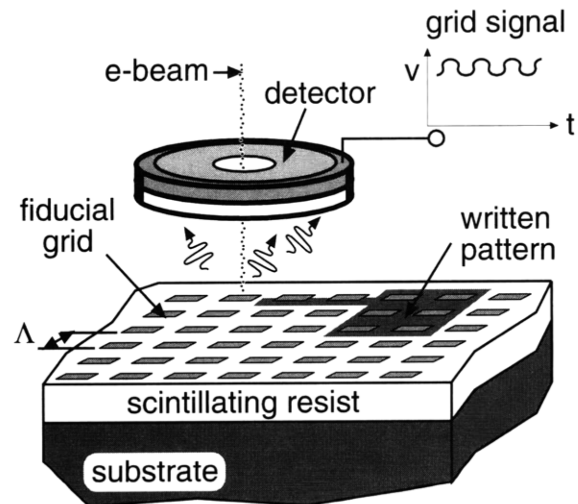

Figure 2. In spatial-phase-locked electron-beam litho-graphy (SPLEBL), the position of the e-beam is referenced directly to a fiducial grid on the substrate. A periodic signal (grid signal), created by the interaction of the e-beam with the grid, is used to track the position of the e-beam, so that written patterns are located in reference to the grid. The spatial period of the grid, p, can be 200 nm or finer.

This year, we demonstrated the efficacy of the GFG mode of SPLEBL in 1D, by patterning gratings on a substrate with their location referenced to a global-fiducial grating. In this experiment, one grating section was patterned. Then, the substrate was moved a small distance (100 μm) and a second grating section written beside the first with a small separation, as

shown in Figure 3. The goal was to align the teeth of the grating sections. Many gratings were written so that statistics about the writing precision could be obtained. A measurement algorithm which analyzed the alignment of the two grating sections revealed that the writing precision of the SPLEBL system was 8.3 nm, mean-plus-sigma. Without the use of the fiducial grid (conventional EBL mode), the writing precision was measured to be 49 nm, mean-plus-sigma. This was the first demonstration of the GFG mode of SPLEBL and represents the highest precision achieved in an EBL system.

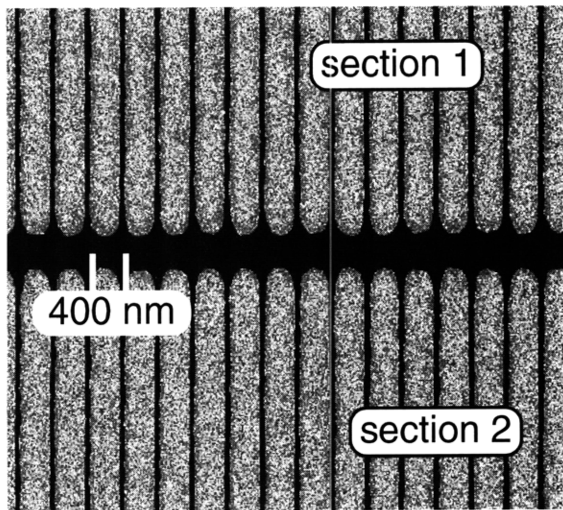

Figure 3. To test SPLEBL, separate grating sections were written aligned to one another. First, a 400 nm-period grating was written. Then the substrate was moved to a new location, and a second section written. An analysis of the aligned grating sections indicates that the writing precision had improved from 49 nm to 8.3 nm, mean-plus-sigma. The grid-signal contrast for this experiment was 1.2, a non-ideal condition.

The writing precision in SPLEBL depends upon the fidelity of the grid, the grid's period, and the quality of the periodic signal from the grid. We have developed a model of SPLEBL which evaluates the relative importance of these parameters. One prediction of the model, shown in Figure 4, indicates the importance of the grid-signal contrast (maximum signal/minimum signal).

To improve signal contrast, we are developing a scintillating fiducial grid, comprised of organic scintillating components that can be patterned on top of the substrate, or added to the e-beam resist (indicated in Figure 2) and optically quenched with UV radiation. We have measured a signal contrast greater than 4 from a patterned scintillator and have identified UV-quenchable scintillating components that can be added to PMMA, an e-beam resist. The signal contrast achieved with the scintillating grid is much higher than values obtained from secondary-electron or backscattered-electron signals, which are typically used in conventional EBL systems.

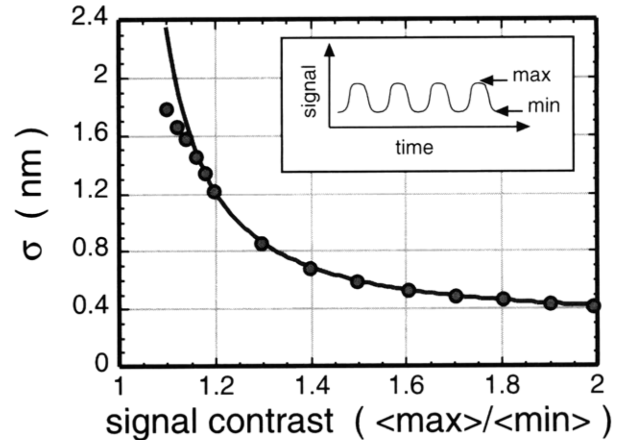

Figure 4. A Monte-Carlo model of SPLEBL shows how the pattern-placement precision improves with increasing signal contrast. A grid period of 200 nm is assumed. With a scintillating fiducial grid, we have measured signal contrast greater than 4. This should yield sub-nm writing precision.

4.4 X-Ray Nanolithography

Sponsors

Defense Advanced Research Projects Agency/U.S. Navy - Naval Air Systems Command
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Project Staff

David J. Carter, Mark R. Schweizer, James M. Daley, Michael H. Lim, Euclid E. Moon, Professor Henry I. Smith

For several years, we have been developing the tools and methods of x-ray nanolithography. We have explored the theoretical and practical limitations, and endeavored to make its various components (e.g., mask making, resists, electroplating, sources, alignment, etc.) reliable and "user friendly." Because of the critical importance of the x-ray mask technology, we discuss this in a separate section.

Our sources for x-ray nanolithography are simple, low-cost electron-bombardment targets, typically Cu_L (λ = 1.32 nm), separated by a 1.4 µm-thick SiN_x vacuum windows from helium-filled exposure chambers. In the future, we hope to replace the Cu_L sources with higher flux sources.

For applications such as CMOS and T-gate GaAs devices, which require alignment of two or more levels of lithography, we have developed a high-precision mask alignment and gapping system (see Section 7). For most other applications, including quantum-effect devices, alignment is not critical, and a single level of exposure is all that is required.

In earlier research, we showed that for wavelengths longer than 0.8 nm, the important limitation on resolution is diffraction in the gap between mask and substrate. Figure 5 summarizes this, which is the result of extensive simulations of the diffraction field, taking into account the vectorial nature of the electromagnetic radiation, the dielectric properties of the absorber, and the spatial incoherence of the source. At α = 1, the process latitude is very wide and all feature types print within 10 percent of the dimensions on the mask. At α = 1.5, latitude is smaller and features print well, but some require biasing on the mask. At α > 2, significant diffraction occurs, requiring modeling of the aerial image to determine the mask structure necessary to achieve a desired image.

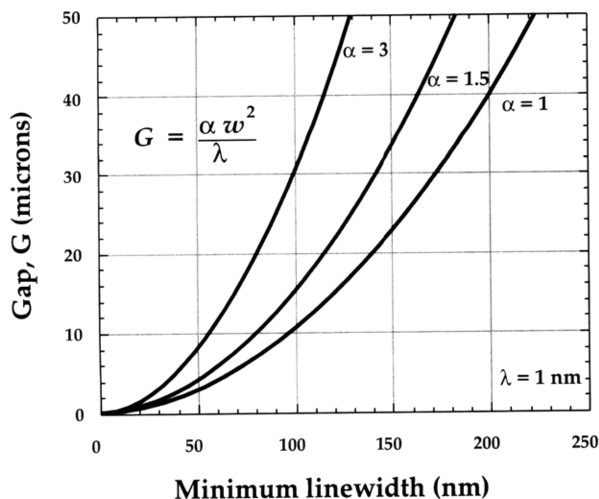

Figure 5. Plot of the minimum feature size versus mask-sample gap, G, at λ =1 nm, for three values of the parameter α.

As indicated in Figure 5, for replicating features below about 70 nm, the mask-sample gap must be below 5 µm. For such high resolution work we generally use soft contact. That is, since the mask is a compliant membrane, only 1 µm thick, one can bring the mask into soft contact with the substrate, via electrostatic means or partial vacuum, without concern that this will cause any damage.

A scanning-electron-beam lithography system is used to write x-ray masks, as illustrated in Figure 6.

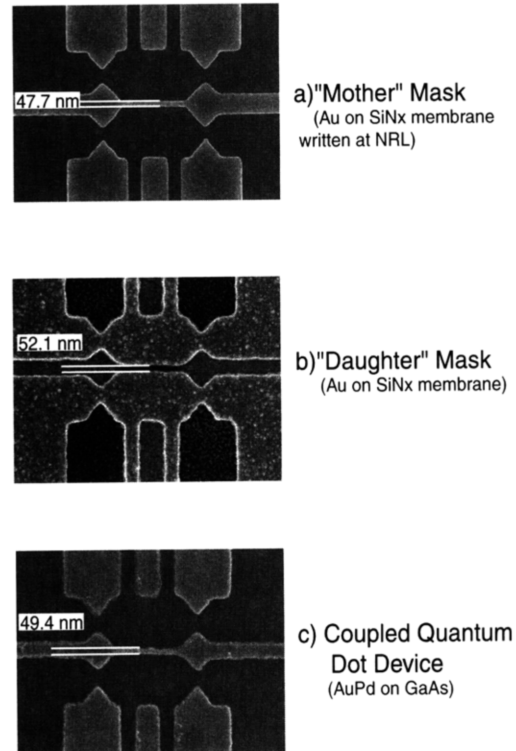

Figure 6. Scanning-electron micrograph illustrating three stages of soft-contact x-ray nanolithography. (a) The "mother" x-ray mask, a pattern in electroplated gold on a 1-micron-thick SiNx membrane formed subsequent to exposure with scanning-electron-beam lithography (at the Naval Research Laboratory). (b) Replication using 1.3 nm x-rays, of the mother mask onto another x-ray mask, the "daughter," and electroplating in gold. This step reverses the "polarity." (c) Replication, of the daughter x-ray mask onto a GaAs substrate; the device is a coupled pair of quantum-dot single-electron transistors.

Features as fine as 25 nm are achieved in this step using the e-beam system at the Naval Research Laboratory (our in-house system cannot achieve features below about 70 nm). This pattern is plated up in gold and then a replica, or "daughter mask," is cre-

ated using soft-contact x-ray nanolithography and electroplating. Finally, this daughter mask is exposed on a device substrate and the pattern transferred.

Recent work has focused on improving our understanding of the practical limits to x-ray nanolithography in the sub-50 nm regime and developing the process technology for improved fabrication of devices at such ultra-small dimensions. Photo-and Auger electrons which emanate from the substrate during an x-ray exposure can have a detrimental effect on the integrity of the resist. Figure 7 shows a plot of resist dissolution rate as a function of height above the substrate for two substrate materials. These experimental plots match very well with simulations, which are omitted here for clarity. A dramatic increase in development rate near the substrate can be seen for the “thick” gold-film substrate. This effect was interfering with faithful replication of very fine (sub-50 nm) features in our mask “daughtering” process by undercutting fine resist lines. By decreasing the thickness of the gold thin film to below the effective absorption depth for x-rays, labelled as the “thin” gold thin-film substrate in Figure 7, the effect is minimized and resist adhesion is dramatically improved. Understanding and correcting for this effect has allowed us to pursue device fabrication in previously-inaccessible regimes.

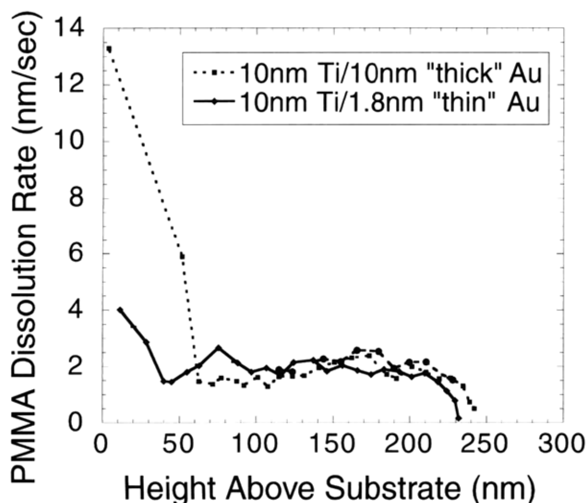

Figure 7. Plot of the dissolution rate of PMMA x-ray resist as a function of height above a gold-film substrate, for two thicknesses of the gold, illustrating the enhanced exposure due to photoelectrons emanating from the thicker gold film.

Figure 8 illustrates that 25 nm features are achievable with 1.3 nm soft-contact x-ray nanolithography and electroplating pattern transfer.

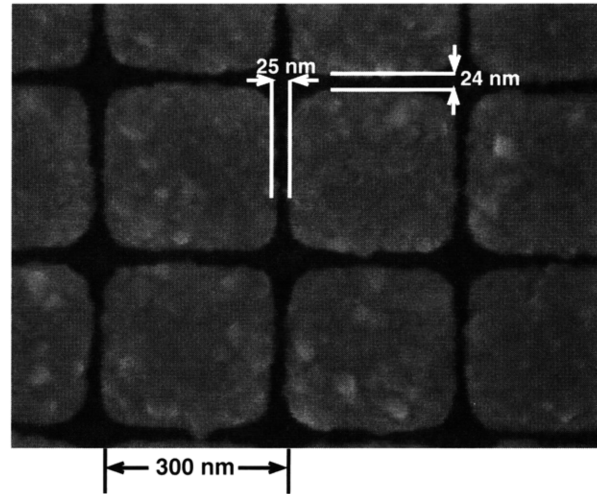

Figure 8. Scanning-electron micrograph illustrating that 25 nm features are achievable using 1.3 nm soft-contact x-ray nanolithography followed by gold electroplating. The mother x-ray mask was written at NRL and contains the patterns for a family of lateral-surface-superlattice devices.

4.5 Zone-Plate Based X-Ray and Deep-UV Projection Lithography

Sponsors

Defense Advanced Research Projects Agency/
Semiconductor Research Corporation
SA1645-25508PG

Project Staff

Ihsan Djohmehri, Timothy A. Savas, Professor Henry I. Smith

Soft-contact x-ray nanolithography is unique to MIT and although suitable for research it is considered incompatible with manufacturing. Accordingly we have sought an alternative approach that would preserve the desirable features of x-ray lithography with 1.3 or 4.5 nm photons while circumventing the need to bring the mask into intimate contact with the substrate. Our proposed solution is illustrated in Figure 9, a maskless projection lithography system that employs an array of Fresnel zone plates. As illustrated, an array of Fresnel zone plates focuses an incident beam of 4.5 nm x-rays from a microundulator, forming an array of diffraction-limited spots on a

substrate. Writing is done via a dot-matrix-printing strategy, with the individual beams multiplexed by an array of grazing-incidence micromechanical mirrors located upstream of the zone-plate array. Registration of the writing will be done continuously under laser interferometer control. If made from spent uranium, Fresnel zone plates can focus 4.5 nm x rays with 31 percent efficiency. The resolution or spot size is approximately equal to the width of the outermost zone. Hence, the resolution of the system is determined by one's ability to make the zone plates by e-beam lithography and dry etching.

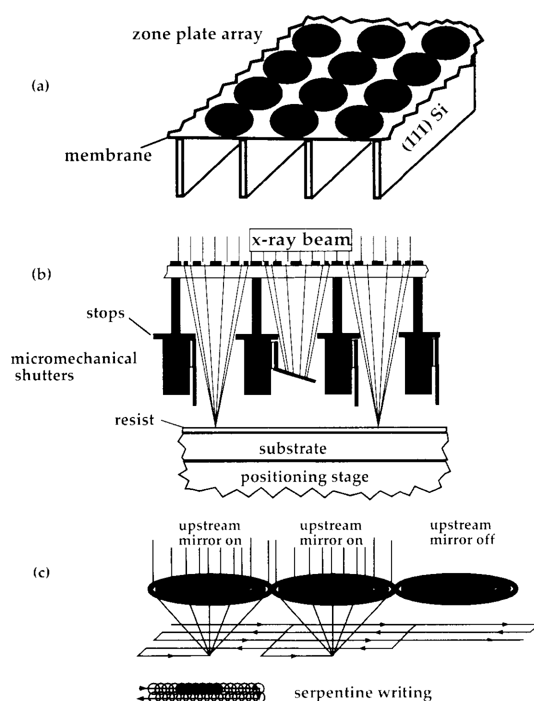

Figure 9. Schematic of a maskless projection lithography scheme that employs 4.5 nm x-rays and hence should be capable of sub-25 nm lithography. Zone plates can focus 4.5 nm x-rays with 31 percent efficiency. Writing is done via a dot-matrix strategy using laser interferometry to ensure precise registration. Although (b) depicts multiplexing of individual beamlets by micromechanical shutters, in practice this will most likely be done by upstream grazing-incidence micromechanical mirrors (c).

The maskless projection system, shown in Figure 9, would circumvent the problems associated with masks, such as distortion, defects, and slow turnaround. Moreover, because of the low energy of the 4.5 nm photon (280 eV) there will be negligible substrate damage and no deleterious backscattering, photoelectrons or proximity effects. The only currently available source of 4.5 nm photons that has the necessary temporal and spatial coherence is an undulator attached to a synchrotron. Because such a system is unavailable to us, we have begun our investigation of zone-plate-based projection lithography using a deep-UV source, the ArF laser. We have fabricated phase-shifting zone plates in quartz plates and built an apparatus that ensures the substrate is in the correct focal plane of the zone plate array. Implementing an array of micromechanical reflecting mirrors for multiplexed writing represents our major current hurdle.

4.6 Improved Mask Technology for X-Ray Lithography

Sponsors

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Project Staff

James M. Carter, James M. Daley, Michael H. Lim, Mark K. Mondol, Edward R. Murphy, Professor Henry I. Smith.

At feature sizes of 100 nm and below the mask-to-substrate gap, G, must be less than ~10 μm (see Figure 5). Thus, for nanolithography the mask membrane should be considerably flatter than 1 μm, preferably ~100 nm. Our mask technology is based on low-stress, Si-rich silicon nitride, SiNx. This material is produced in the IC Laboratory at MIT in a vertical LPCVD reactor. Membranes of SiNx can be cleaned and processed in conventional stations. Radiation hardness remains a problem at dose levels corresponding to production (i.e., millions of exposures). For research purposes, however, the material is acceptable.

For absorber patterns, we use gold which is electroplated onto the membrane after resist exposure and development using a specially designed apparatus. A Ti/Au plating base is deposited on the membrane prior to resist coating.

For patterning of x-ray masks with periodic structures, interferometric lithography (IL) is used, while for patterns of arbitrary geometry, e-beam lithography is used, either at the MIT SEBL facility or in col-

laboration with NRL. Our Digital Instruments STM/AFM was found to be highly effective in inspecting x-ray masks, providing information on defects not apparent by other means.

Figure 10 illustrates a new approach to fabricating x-ray masks that should be especially valuable for gaps less than 10 μm. In brief, after creation of the absorber pattern on the membrane, the latter is bonded anodically to the mesa rim of a Pyrex frame. In this way, the critical absorber pattern can be protected within a He-filled enclosure from the accumulation of dust, as depicted in Figure 11. Dust and contamination that might accumulate on the 1 μm-thick mask membrane can be removed by aggressive methods, including brushing. The x-ray-transparent pellicle on the back side of the glass frame could be made of, for example, 250 nm thick SiN_x. It would not need to be cleaned aggressively since dust particles on it would not be imaged on the substrate due to diffraction and penumbral blurring. Figure 12 illustrates that the membranes bonded according to Figure 10 are extremely flat, ~100 nm. The Figure 11 mask configuration also includes an edge reinforcement which provides a transition from the rigid mesa to the membrane, and a fiducial grid on the side of the membrane opposite the absorber. This grid would be created via interferometric lithography on a Si substrate prior to CVD deposition of the SiNx membrane material. The purpose of this grid is to enable measurement of in-plane distortion using the FSS interferometer described in Section 9. In principle, if the distortion is known, it should be possible to correct it by stress compensation.

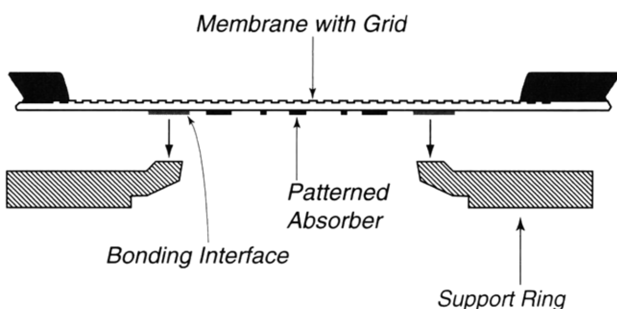

Figure 10. To achieve the protection of the absorber pattern depicted in Figure 11, the mask's membrane is anodically bonded to the rim of the Pyrex support ring after formation of the absorber pattern.

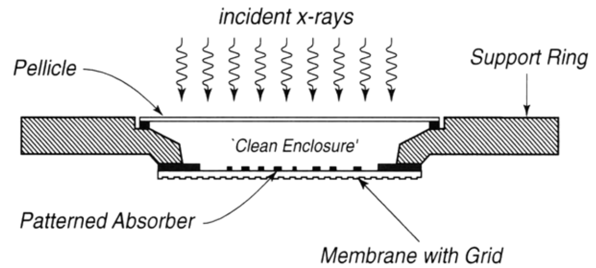

Figure 11. Schematic showing how the absorber pattern on an x-ray mask can be protected from the accumulation of dust and other contamination by enclosing it between the membrane and a pellicle. Dust accumulated on the membrane can be removed by aggressive techniques. The grid is to enable measurement of in-plane distortion via the FSS interferometer (Figure 20).

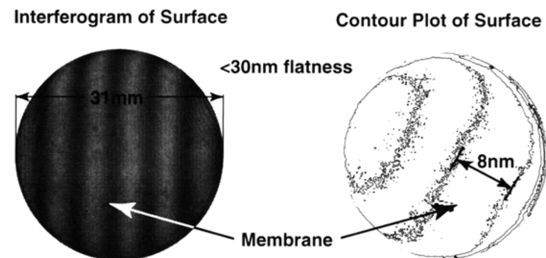

Figure 12. Interferogram of the top surface of an x-ray mask membrane bonded to a Pyrex support ring as in Figure 10, indicating a flatness better than ~30 nm over most of the membrane area.

4.7 Robust, High-Precision Mask Alignment and X-ray Exposure System

Sponsors

Defense Advanced Research Projects Agency/
Semiconductor Research Corporation
SA1645-25508PG
Suss Advanced Lithography
P. O. 51668

Project Staff

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A high-precision mask alignment and x-ray exposure system was constructed that incorporates our novel interferometric broad-band imaging (IBBI) alignment technique. The scheme employs grating and check-

erboard type alignment marks on mask and substrate, respectively, which are viewed through the mask from outside the x-ray beam at a Littrow angle of 15 degrees with f/10 optics and a 110 mm working distance (Figure 13). Each mark consists of two gratings (or checkerboards) of similar periods, arranged so that only dissimilar periods are superimposed during alignment. Using a CCD camera, misalignment is measured from two identical sets of moiré fringes (~10 μm period) that move in opposite directions as the mask is moved relative to the substrate. Alignment corresponds to a specific spatial-phase relation of the two sets of fringes. We have found that checkerboard type alignment marks on the substrate eliminate gap-dependent effects on the image, thereby yielding a more robust moiré alignment signal. Strong fringes are observed for mask-substrate gaps between 0 and 200 microns.

Although two sets of fringes are capable of yielding high-precision alignment on the order of 1 nm, their useful range of detection is limited. Displacing the mask by half the grating period results in an identical phase relation of the moiré fringe sets. Typically, this acquisition range is less than 1 μm. A second set of coarse gratings and the corresponding moire fringes (Figure 14) is used to remove that ambiguity. With this mask configuration, all coarse and fine fringes are in alignment at only one position over a range of several microns. The remaining ambiguity can be removed completely by a conventional set of "bar" alignment marks.

We devised a "coarse" gapping scheme based on reflection from the substrate of a beam diffracted from a special mark on the mask. This scheme allows detection of large gaps (several hundred microns) necessary for the safe approach and leveling of the mask and the wafer. The mark consists of a narrow stripe (7 μm wide) of 1-μm-period grating. One of the diffracted orders reflects off the wafer, and back towards the microscope at the same angle as the incident illumination. As shown in Figure 15, the image is composed of one stripe diffracting back from the mask and another stripe reflecting off the wafer. The distance between the stripes in the image varies linearly with gap. Detectivity of coarse gapping is on the order of 1 μm. Gapping marks are required only on the mask.

We have verified the robustness of IBBI by demonstrating that the system performance is not deteriorated when the illuminating and viewing beams traverse paths consisting of 25 mm of air, a 13 mm-thick glass optical flat, and 72 mm of helium (Figure 13). Specifically, we compared the displacement as measured by IBBI and a closed-loop piezoelectric drive with calibrated capacitive sensor. Figure 16 shows the results, corrected for thermal drift. It is significant that these measurements were made external to the helium enclosure through the above optical paths, indicating the feasibility of continuous monitoring of alignment during x-ray exposure. The unique capabilities of IBBI alignment are being employed in the fabrication of a variety of electronic and optical devices.

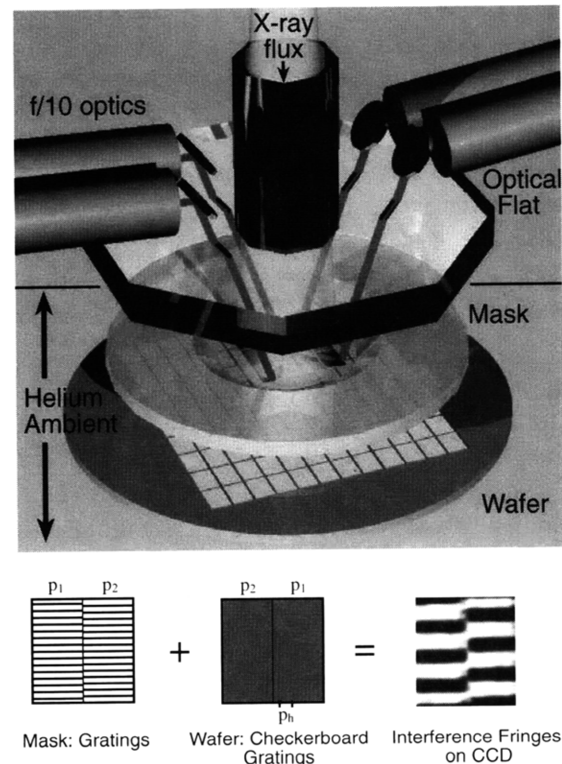

Figure 13. Interferometric broad-band imaging alignment scheme. Alignment is signified by the relative spatial phase of counter-moving interference fringes displayed on CCDs attached to each of the f/10 optics.

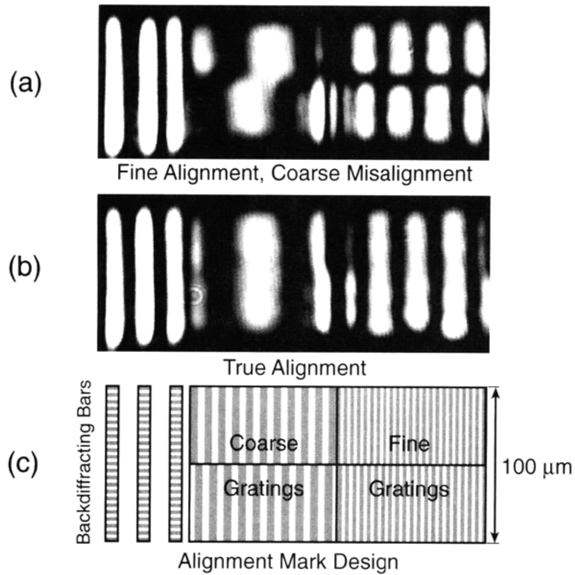

Figure 14. Illustration of the fringe pattern displayed on the CCD for (a) alignment of the spatial phase of fringes from fine gratings, but misalignment of fringes from coarse gratings; (b) alignment of all three types of marks; (c) layout of coarse and fine alignment marks on the mask, and the back diffracting bars. The middle of the three bars depicted is located on the substrate.

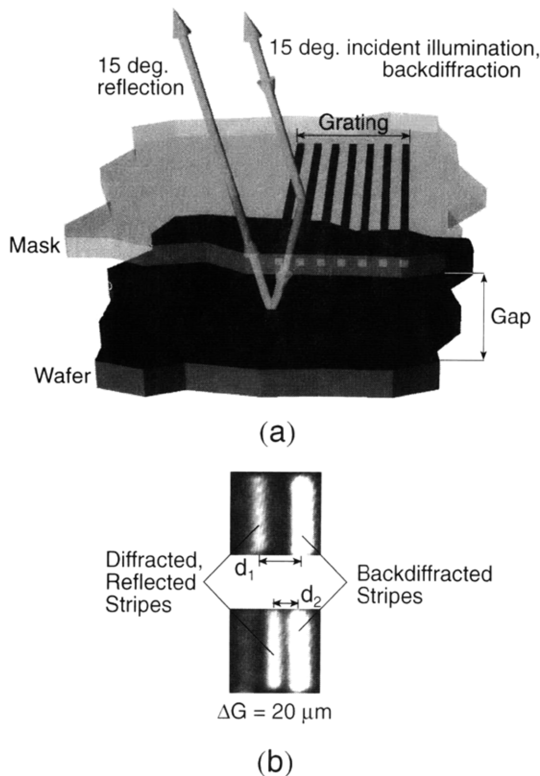

Figure 15. Two images of the marks used for coarse gapping for two gaps that differ by 20 μm.

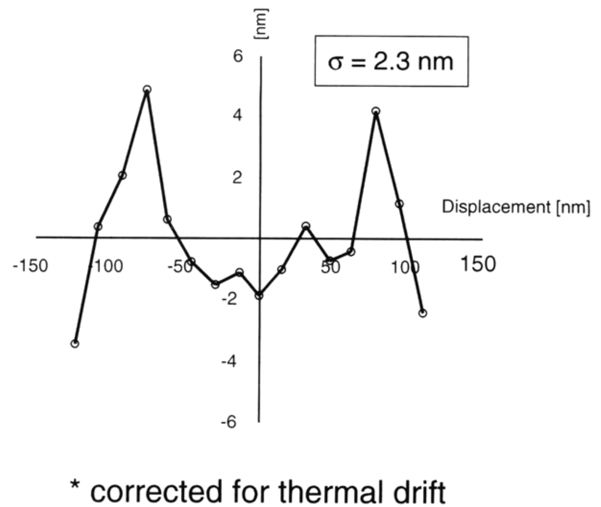

Figure 16. Plot of the difference in mask displacement as measured by a remotely located capacitive sensor and the IBBI system, after data has been corrected for thermal drift between the mask and the remote sensor.

4.8 Interferometric Lithography

Sponsors

Joint Services Electronics Program
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National Aeronautics and Space Administration
Contract NAS8-38249
Grant NAGW-2003

Project Staff

James M. Carter, Maya Farhoud, Juan Ferrera, Robert C. Fleming, Timothy A. Savas, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Interferometric lithography is preferred for the fabrication of periodic and quasi-periodic patterns that must be spatially coherent over large areas. For spatial periods down to 200 nm, an argon ion laser is used in a Mach-Zehnder configuration, with a fringe-locking feedback system, as illustrated in Figure 17. This scheme produces large area (10-cm diameter) gratings with long-range, spatial-phase coherence. Fringe locking ensures reproducibility of exposure.

The gratings and grids produced are used as fiducials in spatial-phase-locked electron-beam lithography and in a new approach to metrology for the sub-100 nm domain. In addition, a wide variety of applications, from ultra-high-density magnetic information storage to atom-beam interferometry, depend on

interferometrically produced gratings and grids. These applications are separately described in this report.

For spatial periods below 200 nm, a source wavelength below 200 nm, must be used. Since such sources have limited temporal coherence, one is forced to employ an achromatic scheme, as shown in Figure 18. The source is an ArF laser (193 nm wavelength). A collimating lens, polarizer and scanning system are interposed between the source and the interferometer in order to achieve reasonable depth-of-focus and large exposure areas. We also use a white light interference principle to ensure equal path lengths in the two interferometer arms. Using this system, gratings and grids of 100 nm period (nominally 50 nm lines or posts) are obtained in PMMA on top of an antireflection coating. Figure 19 shows a 100 nm-period grid etched into Si following achromatic interferometric lithography.

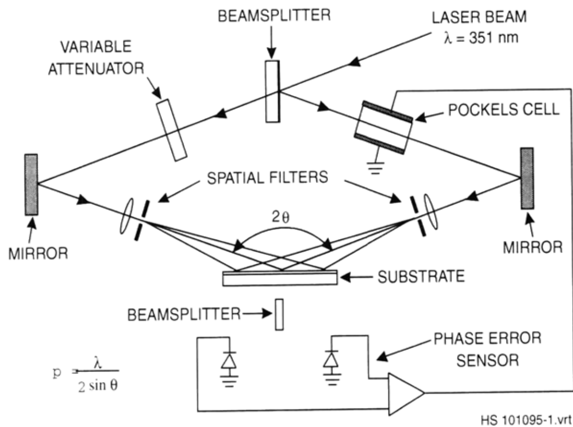


Figure 17. Schematic of the MIT interferometric lith-ography system. The system occupies a 2X3m optical bench in a class 100 clean environment. The beamsplitter directs portions of the two interfering spherical beams to photodiodes. A feedback locking is achieved by differ-entally amplifying the photodiode signals and applying a correction to the Pockels cell which phase shifts one of the beams.

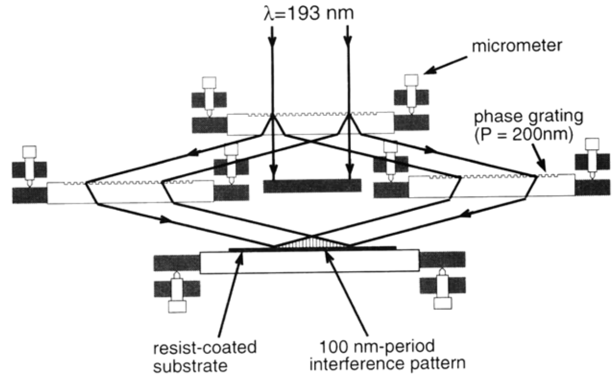


Figure 18. Achromatic interferometric lithography (AIL) configuration.

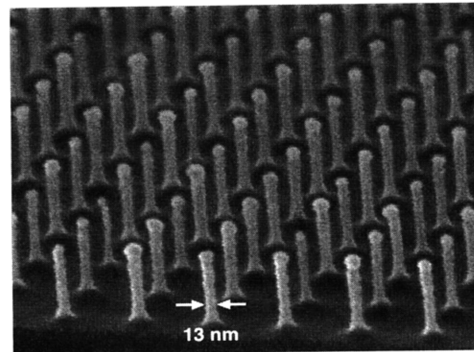


Figure 19. Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating, and transferred into Si by reactive ion etching.

4.9 Sub-100 nm Metrology Using Interferometrically Produced Fiducial Grids

Sponsors

Defense Advanced Research Projects Agency/
U.S. Army Research Office
Grant DAAH04-951-0564

Project Staff

Dr. Mark L. Schattenburg, Juan Ferrera, Professor Henry I. Smith

The ability to see and measure the results of a process is critical to advancing fabrication technology. Historically, the development of improved microscopy techniques led to rapid progress in microfabrication. Thus, the scanning-electron microscope was essen-

tial to the microelectronics revolution. Similarly, the scanning-tunnelling microscope is creating a revolution in the study of interfaces and nanostructures.

In the past, metrology of microstructures and the measurement of workpiece distortion (e.g., a photolithographic reticle or an x-ray mask) has been based on point-by-point measurement through an optical microscope using an X-Y table monitored by a laser interferometer. Although this approach enables relative distances in a plane to be measured with 1 nm-level detectivity, it is expensive, tedious, and subject to a number of shortcomings, including the necessity of placing rather perturbative marks on a workpiece. We have initiated a new approach to metrology for the sub-100 nm domain that is based on large-area fiducial grids produced by interferometric lithography. This new approach is complementary to the point-by-point approach in much the same way that aerial photogrammetry is complementary to ground-based land surveying for the mapping of terrain.

A key element in this new initiative is the FSS interferometer, illustrated in Figure 20. This system, once fully developed, will enable us to measure in a global manner the in-plane distortion of a workpiece provided one of its surfaces contains a shallow fiducial grid. Ideally the grid on the workpiece will be created by interferometric lithography or a derivative, such as near-field holography.

As part of this new initiative in sub-100 nm metrology, we are pursuing a variety of approaches to eliminating the distortion in interferometrically produced grids, decreasing the coefficient of the hyperbolic phase progression (a consequence of creating a grid by interfering spherical wavefronts), and increasing the useful area of fiducial grids. By means of a scanning beam interferometric lithography, we hope to achieve spatially coherent grids hundreds of millimeters in diameter.

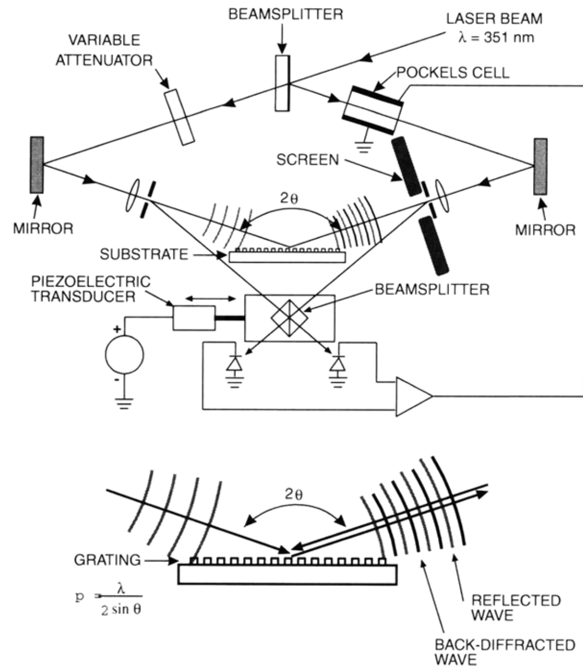


Figure 20. Schematic of the FSS interferometer. A spherical wave back-diffracted from a shallow substrate grid, and a second wave specularly reflected, interfere on a fluorescent screen at the spatial filter. The fringes are imaged onto a CCD. By shifting the beam splitter with a piezo, a computer generates an X-Y map of phase error.

4.10 Arrays of Nanomagnets for High-Density Information Storage

Sponsor

3M Corporation

Project Staff

Maya Farhoud, James M. Carter, Professor Caroline A. Ross, Professor Henry I. Smith, Professor Kamal Youcef-Toumi, Jungmok M. Bae, M. Hwang

For several years, the aerial density of information storage in thin-film hard disks has been increasing rapidly through improvements in magnetic materials, head design, signal processing, and mechanical design; while prices have fallen with equal rapidity. This trend clearly cannot continue forever, and, in fact, will soon slow down unless a new paradigm for magnetic information storage is invoked. Following earlier work by S.Y. Chou, R.L. White, and others, we have initiated a program to develop fabrication technologies for ultra-high-density information storage based on discrete pillars of ferromagnetic materials,

as illustrated in Figure 21. In order to exceed the extrapolated information density of conventional hard discs, the pillars must have diameters less than 100 nm and a spatial period less than 200 nm (aerial density of 2.5 x $10^9/cm^2$). In fact, our goal is to achieve aerial densities of $4x10^{10}/cm^2$, corresponding to a spatial period of 50 nm in the array of magnetic pillars. An important focus of our research is to realize such densities via techniques that are compatible with low-cost manufacturing. The lithography candidates are therefore restricted to interferometric lithography, x-ray lithography, achromatic-interferometric lithography, and nanoimprint lithography. At present our work is confined to the first, using a process illustrated in Figure 22. Interferometric lithography is described in detail in Section 7. The magnetic materials of choice at present are nickel and cobalt, both of which are electroplated into the holes produced in an antireflection coating (ARC) by the process illustrated in Figure 22. Figure 23 shows some results of electroplating cobalt.

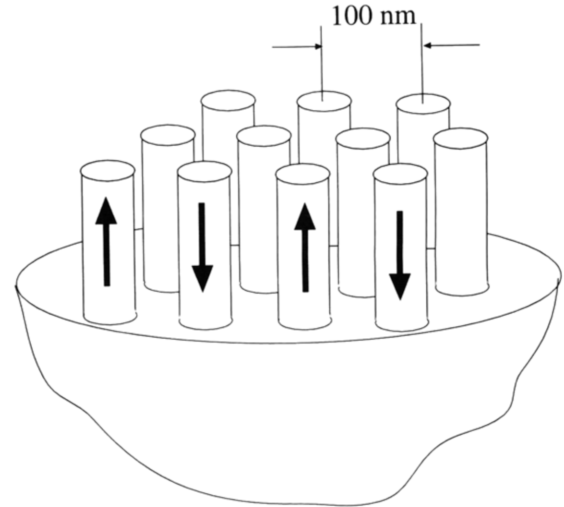


Figure 21. Schematic of high density magnetic information storage based on discrete sub-100nm sized magnetic pillars.

Reading and writing of the information stored in the magnetic pillars appears to be the most formidable problem of the proposed new paradigm. Because the magnetization is vertical, a scheme akin to the magnetic-force microscope with multiple reading heads will presumably be required. Interferometric lithography cannot produce nanopillar arrays in a cylindrically-symmetric configuration compatible with rotating disc reading and writing; it can provide only a Cartesian geometrical arrangement. Accordingly, if interferometric is the lithography of choice, entirely new apparatus for reading and writing must be developed, presumably utilizing micromechanical schemes, such as electrostatic motors that move exclusively in X and Y. If, on the other hand, a rotating scheme is desired, x-ray nanolithography or nanoimprint lithography will be used to produce the nanomagnet arrays. Both of these schemes are compatible with 25-50 nm pillar dimensions. Both the x-ray mask and the nanoimprint master would have to be made by scanning-electron-beam lithography.

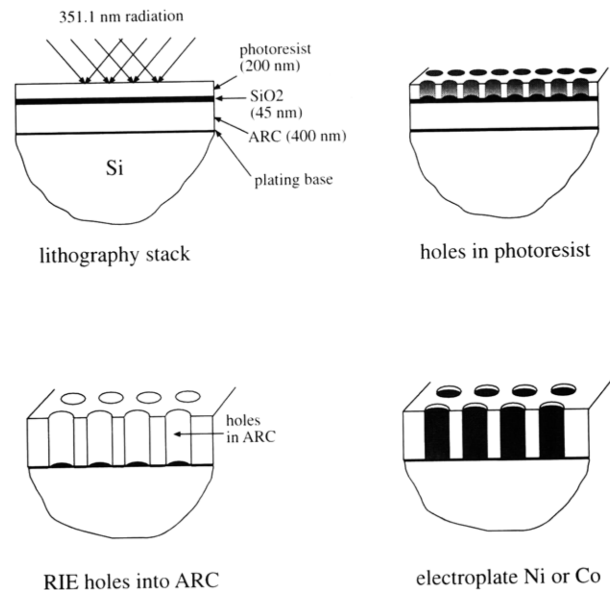


Figure 22. Schematic of the process currently used to fabricate 100 nm-scale magnetic pillars. Photoresist exposure is by interferometric lithography using the 351 nm line of the Ar ion laser. The antireflection coating (ARC) prevents backreflection from the substrate from interfering with the lithography. Circular holes in the SiO_2 and ARC are created by reactive-ion etching in CHF_3 and O_2, respec-tively.

An important focus of our research will be the basic study of how discrete nanoscale magnets switch direction of magnetization. It has been predicted theoretically that below a certain size, which depends on the magnetic properties of the material, the magnetization will switch coherently. This as well as other mechanisms of switching will be studied.

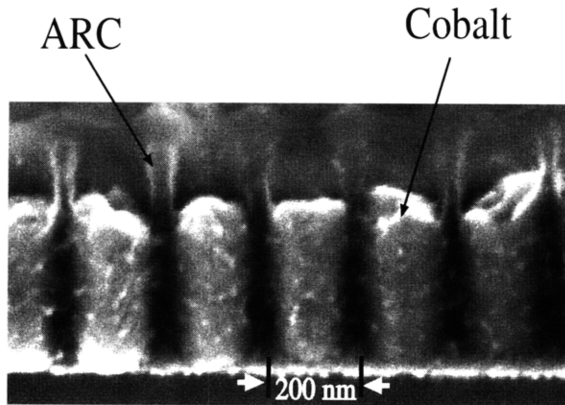


Figure 23. Scanning-electron micrograph of cobalt pillars electroplated to a height of 200 nm still embedded in ARC. The spatial period is 200 nm.

4.11 Design and Fabrication of Single-Mask 50 nm MOSFETs

Sponsors

Defense Advanced Research Projects Agency/U.S. Navy - Office of Naval Research
Contract N66001-97-1-8909
National Science Foundation
Graduate Fellowship

Project Staff

Keith M. Jackson, Zachary Lee, Professor Dimitri A. Antoniadis, Professor Henry I. Smith

As MOSFET dimensions are scaled to lengths below 100 nm, significant challenges arise in controlling fabrication processes. Rapid turnaround between process changes and device results, and an ability to extract the exact structure and doping of the fabricated device are tools critical to the development. The first requires a short-flow process that focuses only on the fabrication steps that critically define device performance in a minimum number of steps. The second tool, known as inverse modeling, couples a device simulator with an optimizing routine that shifts the doping in the simulated device until the current-voltage and capacitance characteristics of the simulated device match those of the real device. This project focuses on creating a short-flow process for 50 nm channel-length MOSFETs and coupling it with currently existing inverse modeling capabilities.

The short-flow process we have conceived will allow working MOSFETs to be fabricated in one mask step. It is shortened from a normal full-length MOSFET process by eliminating the need for oxide isolation around the devices and by eliminating the need for the passivation and metal layers at the end of the process. Two types of structures will allow devices to be operational MOSFETs without field-oxide isolation. The first structure is an annular device where the source is completely enclosed inside of a gate and the drain is outside of the annular gate. The second structure is a figure-eight configuration (Figure 24) where the parasitic out-of-channel (i.e., field region) source-to-drain current is less than 0.02 times the in-channel current under the gate in the center of the structure. By using a self-aligned cobalt-silicide process (salicide), the source and drain will be low enough in resistivity that they can be contacted directly by probes. Even though two significant steps of the conventional fabrication process are left out, the steps that define the device operation—the gate stack, implantation, and critical high temperature steps—are all contained in the short-flow process.

The gate-level lithography (the only lithography step) for the short-flow process will be done using X-ray lithography, easily allowing linewidths down to 50 nm. The mask will be fabricated with a mix of optical steps for the large features and e-beam writing for the fine gates. Using optically placed e-beam registration marks, the e-beam tool can match the in-plane scale and distortion of the optical projection tool to achieve good pattern placement.

The key elements in the fabrication of sub-100 nm devices are the placement of dopants and the use of very thin gate oxides. A process to grow 20 Å oxides in N_2O has been developed. With such thin oxides, etching the poly-silicon gate and stopping on the gate oxide will be the major challenge. The placement of the dopants calls for a combination of implantation and diffusion. We are investigating very-low-energy implants for the source and drain of these devices. Dopant diffusion will be carefully controlled by a few high-temperature, rapid-thermal anneals. Building on our previous successes in fabricating robust 100 nm NMOS, we will explore the optimization of source and drain design.

After devices are fabricated using the short-flow process, their doping and structural components can be evaluated via inverse-modeling, using current-voltage and capacitance measurements. Understanding

what doping profiles were achieved versus the original design then will allow us to go back and adjust the process and to see how changes affect the doping profiles in the device. This approach should facilitate the optimization of device fabrication for deep-sub-100nm MOSFETs.

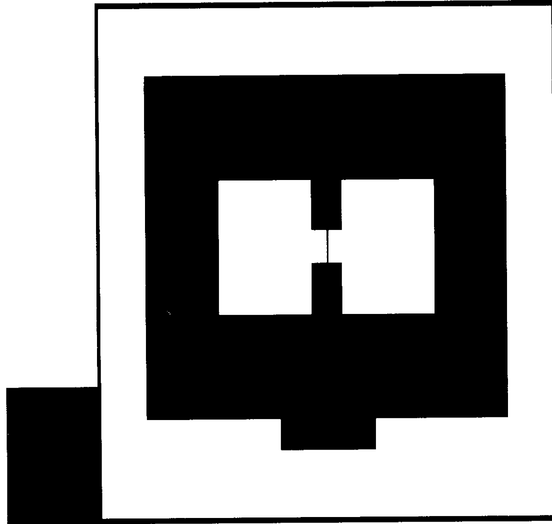


Figure 24. Gate mask layout of a figure-eight geometry MOSFET. The inner two white square areas are the source and drain probe pads that will be salicided. The dark wide ring is the gate pad with the active gate being the fine line in the center. The outer ring is a guard ring.

4.12 CMOS Technology for 25 nm Channel Length

Sponsors

Defense Advanced Research Projects Agency/U.S. Navy - Office of Naval Research
Grant N66001-97-1-8909

Project Staff

Anthony Lochtefeld, Ilia Sokolinski, Professor Dimitri A. Antoniadis, Professor James Chung, Professor Henry I. Smith

The scaling of CMOS transistors into the sub-100 nm region is extremely challenging because of short-channel effects. We are pursuing two distinct approaches that should permit scaling to 25 nm channel lengths. Both can be considered three-dimensional-gate CMOS (3DG-CMOS) technologies. One is a planar twin-gate configuration, with either joint or independent control of the two gates per MOSFET; the other features a gate that surrounds a pillar-like vertical channel.

Monte-Carlo modeling predicts that twin-gated devices scaled to L_{eff} = 25 nm will have transconductances G_m in excess of 2000 mS/μm, while maintaining almost perfect sub-threshold slope. However, models also predict that the tolerance in aligning front and back gates has to be within Lg/4 in order to avoid performance deterioration due to overlap capacitance. The Lg/4 requirement translates into 6 nm alignment tolerance for a 25 nm channel. In order to meet this alignment challenge we will use the IBBI alignment technique which achieves sub-nanometer misalignment detectivity. The planar twin-gate devices will be fabricated starting with a SIMOX wafer. First, the gate stack for the back-gate will be deposited and patterned by x-ray lithography. The structure will then be covered by a layer of CVD oxide, planarized, and bonded to a "handle wafer." The bulk of the SIMOX wafer will then be chemically etched using the back-oxide of the SIMOX wafer as the etch-stop. The fabrication will then follow a conventional SOI process, with front gate precisely aligned to back-gate layer using the IBBI alignment scheme. The final structure is depicted in Figure 25.

The second approach to 3DG-CMOS utilizes epitaxially grown vertical pillars of Si. Such a structure addresses two major problems in ultra-short-channel MOS fabrication. First, a surround-gate has maximum possible control of the channel potential, improving sub-threshold slope and reducing short-channel effects to allow scaling of the effective channel length (L_{eff}) down to 25 nm for pillar MOS device 40-50 nm in diameter. Second, epitaxial definition of a vertical channel allows almost arbitrarily short L_{eff} with tighter control than is possible with current lithography technologies. In planar MOS devices, gate length is limited by lithography; the inherent variability in the lithography and etch processes can lead to unacceptable variation in L_{eff} from device to device and wafer to wafer. This is especially critical in ultra-short-channel devices, where the threshold voltage is extremely sensitive to gate length.

Previously demonstrated processes for epitaxially-defined vertical MOS structures generally start with the etching of a pillar from the epi wafer, and suffer from severe difficulties in the subsequent contact and isolation of gate and source/drain regions. These problems are avoided in our proposed vertical-MOS process, illustrated in Figure 26 where the gate elec-

trode material and dielectrics for source/drain isolation are deposited prior to hole-definition and epitaxial growth.

We are currently experimenting with selective epitaxial growth in features down to 100 nm in diameter in oxide on silicon, a key technology for our novel vertical-MOS process.

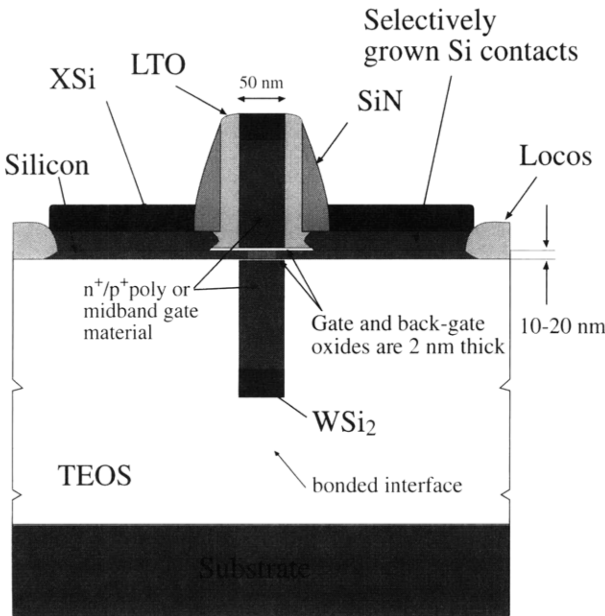


Figure 25. Dual gate n-MOS transistor with 25 nm effective channel length.

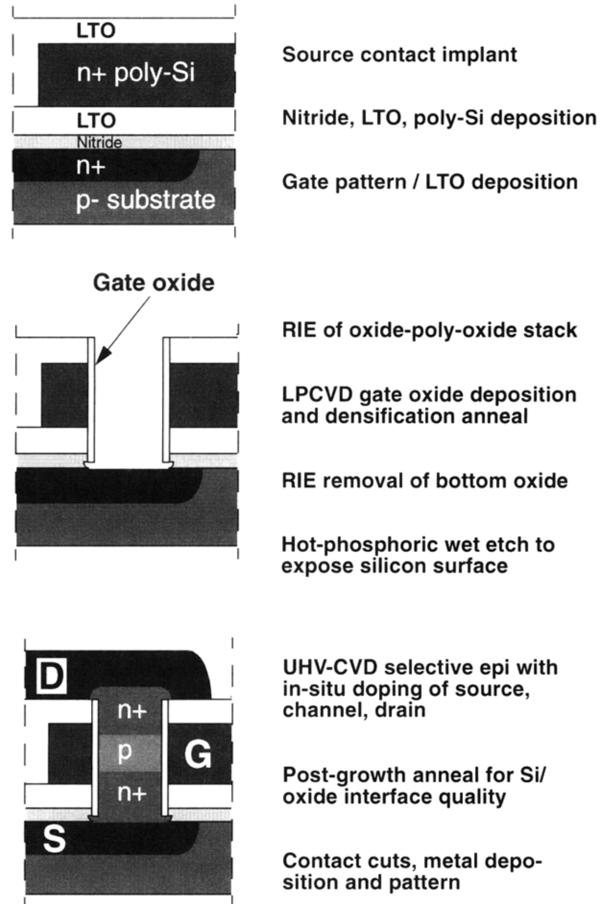


Figure 26. Process for fabricating surround-gate vertical MOS devices.

4.13 Fabrication of T-gate Devices Using X-ray Lithography

Sponsor

U.S. Army Research Office
Contract DAAH04-94-G-0377

Project Staff

Mitchell W. Meinhold, Professor Henry I. Smith

Monolithic microwave integrated circuits (MMICs) have applications in wireless communications as well as other signal processing applications which require high speed and/or low noise. The high-speed MODFET devices of such circuits simultaneously require very short gate lengths and low resistance. Low resistance (satisfied by long gate lengths) is required for high current drive. To meet these conflicting demands, so-called "T-gate" processes are used in

which the base or stem of the gate is very short (80-150 nm), while the upper portion is a large fraction of 1 μm. Although such structures can be achieved using direct-write, electron-beam lithography in double-layer resists, the technology is expensive, slow, and unlikely to meet future production needs. For these reasons, we are developing a process for fabricating T-gates using x-ray lithography.

The fabrication sequence is shown in Figure 27. The first layer defines the stem of the gate, a critical parameter for a field-effect device. After aligning, exposing and developing the first layer, a second layer of resist is deposited. The pattern corresponding to the upper part of the gate is aligned, exposed and developed. At this point, a metal lift-off is performed to create the T-gate. Several challenges present themselves. First, it must be possible to align the x-ray mask to place the gate stems within 100 nm of the source. This requires both a precision mask-alignment system and placement of patterns on the x-ray mask by the electron-beam system so that the various patterns will properly overlay one another. Finally, pattern magnification, intrinsic in point-source x-ray systems at a finite gap between mask and substrate, must be taken into account when writing the mask. We anticipate no difficulty in aligning mask marks to substrate marks with our improved IBBI mask alignment system to well below 100 nm.

To ensure pattern overlay, idential registration marks are put down on all of the x-ray masks using optical lithography. The e-beam system then registers its writing relative to these marks, ensuring that the position of patterns on all the x-ray masks will properly overlay one another.

Our current focus is on dynamically controlling the mask-sample gap during x-ray exposure. This is necessary because an error in gap will cause a failure of overlayer due to the point-source magnification effect. The IBBI alignment system and its protocols are being modified to enable continuous control of both alignment and gap during exposure.

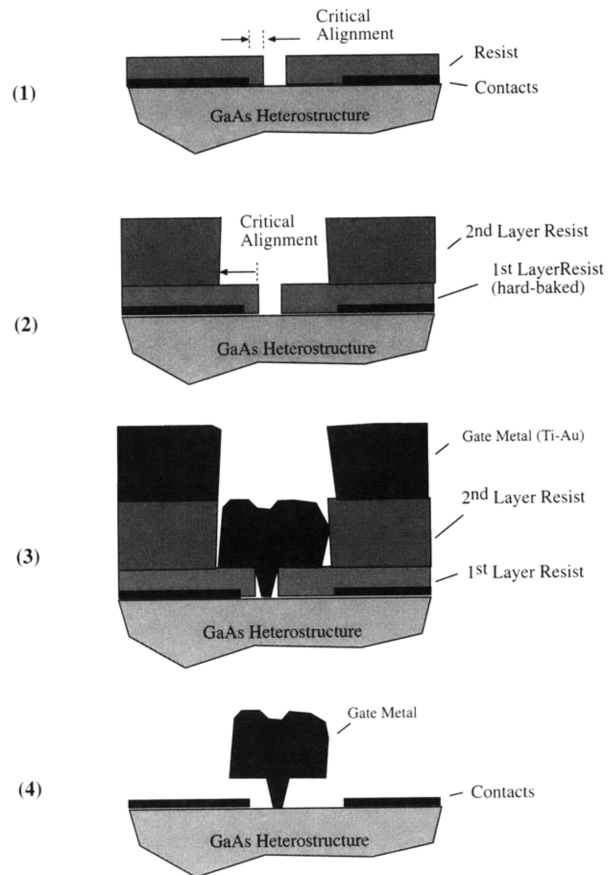


Figure 27. Depiction of the T-gate process steps: (1) Resist is deposited over existing contact metal. Alignment and exposure takes place. (2) After hardening the first layer, a second layer is deposited. The second pattern alignment and exposure takes place. (3) Gate metal is deposited. (4) Liftoff (resist removal).

4.14 Single-Electron Transistor Research

Sponsor

Joint Services Electronics Program
Grant DAAH04-95-1-0038

Project Staff

David B. Berman, Professor Raymond C. Ashoori, Professor Henry I. Smith

The single-electron transistor (SET) has the highest charge sensitivity of any man-made device. In many respects, it is the electric analog of the SQUID, which is the most sensitive detector of magnetic field. It is very well suited for applications where one needs to

measure small fluctuations of charge without disturbing the system under study. An example of such a system is a quantum dot.

Figure 28 shows a scanning-electron micrograph of one of our devices. The SET consists of a metal island connected to the source and drain electrodes by two small tunnel junctions. Fabrication of the tunnel junctions is performeed using a shadow evaporation method.

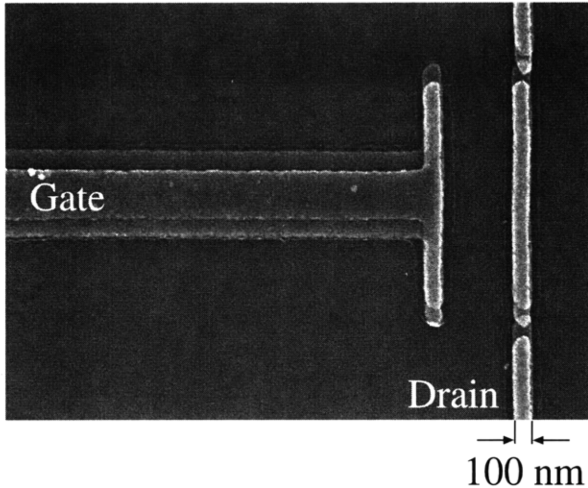


Figure 28. Scanning electron micrograph of a single-electron transistor, made of Al, in which the two tunnel barriers are produced by a two-angle shadow evaporation process.

The operation of the single-electron transistor depends on the fact that the central island has a very small capacitance and the energy that it takes for electrons to charge this island is quite large. For example, if the device is cooled to temperatures below 1 K, the electron thermal energy becomes less than the charging energy. This means that without a significant source-drain voltage bias, the electrons cannot travel through the central island. This effect is known as the Coulomb blockade. The Coulomb Blockade is manifested as a zero current region in the current-voltage dependence of the SET. This effect is shown in Figure 29. The addition of gate voltage can alter the size of the Coulomb Blockade region, thus we can use this device as a transistor.

We have incorporated our technique of fabricating SETs into experiments with quantum dots in GaAs. Figure 30 is a micrograph of the device. The quantum dot is created in the 2DEG below the surface by applying a negative voltage to the metal leads on the surface, thereby depleting the electrons below. The SET is integrated into the lead pattern defining the quantum dot and is used to detect any electrostatic changes in the dot. In one of the experiments performed we tested the effect of point contact resistance on the Coulomb blockade in the quantum dot. Figure 31 shows a sample of the data from this experiment. One of the point contacts to the quantum dot is completely pinched off so there is no conduction through it. The other point contact is slowly closed as one of the gates is scanned. The onset of Coulomb Blockade occurs when the point contact resistance is approximately 15 kohms.

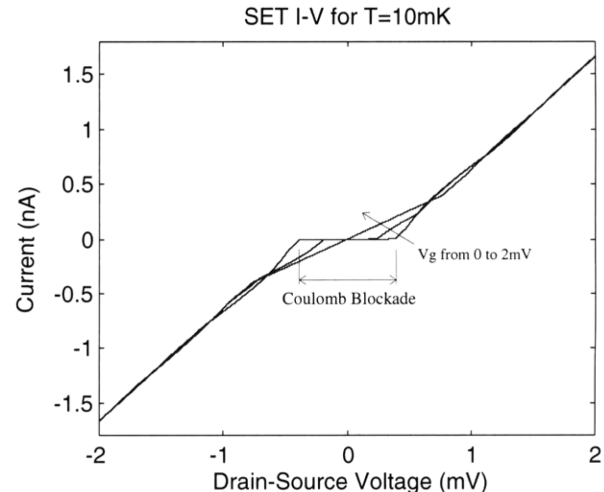


Figure 29. Current-voltage characteristic of a single-electron transistor taken at 10 mK, for three values of gate voltage. The Coulomb blockade is maximum at zero gate bias.

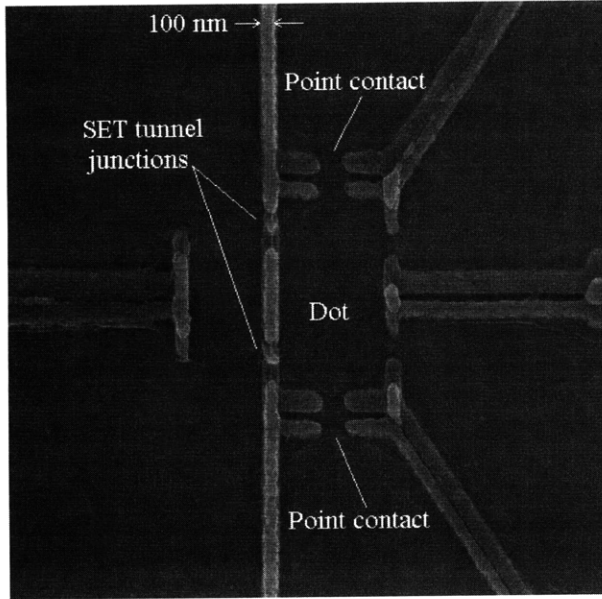


Figure 30. Scanning-electron micrograph of a lateral quantum dot experiment. The quantum dot is defined electrostatically in the two-dimensional electron gas below the surface by applying negative voltage to the metal leads on top. The single-electron transistor is fabricated in the lead pattern, such that the central island is located next to the quantum dot for good electrostatic coupling.

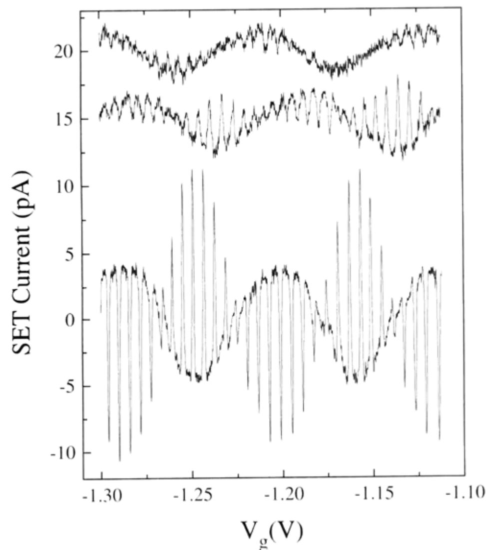


Figure 31. The signal from the single-electron transistor as the gate of the quantum dot is varied. One of the point contacts is completely pinched off, and the resistance of the other is slowly increased from the top trace to the bottom one. The point contact resistance is increased from about 12 kohms (top trace) to 100 kohms (bottom trace). The quantization of charge, or the appearance of single-electron peaks in the signal, appears for a point contact resistance of about 15 kohms.

4.15 One-Dimensional Photonic-Band-Gap Devices in SOI Waveguides

Sponsors

Joint Services Electronics Program
Grant DAAH 0495-1-0038
National Science Foundation
Contract DMR-940034

Project Staff

Shanhui Fan, Juan Ferrera, James S. Foresi, Günter Steinmeyer, Erik R. Thoen, Dr. Pierre R. Villeneuve, Professor Erich P. Ippen, Professor John D. Joannopoulos, Professor Lionel C. Kimerling, Professor Henry I. Smith

Photonic band gap (PBG) structures are optical analogs of semiconductors. A light wave traveling through a PBG structure encounters a large, periodic change in the dielectric constant. The periodicity causes bands of frequencies to be disallowed from propagating through the structure. These bands can be as large as 30 percent of the mid-gap frequency. PBGs can be designed in one-, two-, and three-dimensions. 1D PBGs are similar to distributed Bragg reflectors (DBRs), but have much larger gaps; band gaps for DBRs are typically less than 1 percent. In this project we have developed 1D PBGs that are directly integrated into silicon waveguides. Their band gaps are centered at λ = 1.54 μm. This wavelength is compatible with commercial fiber optic communication systems.

We have fabricated and measured a 1D PBG microcavity with a resonance at λ = 1.56 μm, a quality factor (Q) of 265 and a modal volume (V) of 0.055 μm^3, which makes it the most tightly confined photon mode ever achieved. Its applications range from the control of spontaneous emission in light emitting materials, to channel dropping filters for wavelength division multiplexing.

The 1D PBG device consists of a single-mode strip waveguide fabricated from SOI material with a periodic series of holes etched through the Si (Figure 32). The large dielectric contrast between the Si and the holes (12:1) results in a band gap of 27 percent of the mid-gap frequency. The waveguide width is approximately 0.47 μm, with holes of 0.20 μm diameter, separated by 0.42 μm, center to center. The minimum dimension, 0.13 μm, occurs between the edges of the waveguide and the edges of the holes. Because of the small feature size, we use a combi-

nation of e-beam and x-ray lithography for patterning. To minimize possible alignment errors, we fabricated an x-ray mask that contained both the waveguide and hole structures. The holes were etched into long waveguides (typically around 2 mm) which required stringent control of e-beam field stitching.

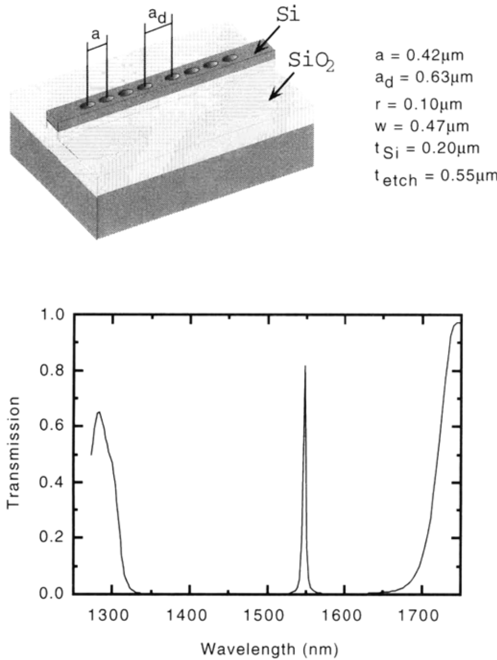


Figure 32. Dimensions and basic properties of a PBG microcavity. (a) Schematic of a PBG waveguide microcavity with dimensions for operation at λ= 1.54 μm: a is the hole period, a_d is the defect length, r is the hole radius, w is the waveguide width, t_{Si} is the silicon thickness and t_{etch} is the total etch depth through both the Si and the oxide. (b) Computation of the transmission through the structure. The transmission spectrum corresponds to the device dimensions listed. The resonance is centered at 1.547 μm and has a Q of 280.

The device, which consists of two sections of four holes separated by a gap, behaves as a microcavity. Light gets localized in the region between the two sets of holes. The holes act as mirrors, forming a resonant cavity within the waveguide. The transmission spectrum of this structure was computed using a three-dimensional, finite-difference time-domain method which is shown in Figure 32b.

The devices were fabricated from a Unibond silicon-on-insulator substrate with a 0.2 μm single-crystal silicon layer on a 1.0 μm oxide layer. The relatively thick oxide is required to keep the optical mode of the waveguide from leaking into the substrate. The wafer was then coated with PMMA and the pattern transferred to the PMMA via x-ray lithography. The PMMA was developed and a 50 nm Cr layer evaporated onto the sample. The PMMA was then dissolved in acetone, leaving intact the Cr which was in direct contact with the Si. The Si layer was then etched in a CF_4 plasma with 15 percent O_2. An additional etch into the oxide was performed using CHF_3. The oxide etch was shown theoretically to improve the performance of the PBG device.

A scanning electron micrograph of a completed PBG waveguide device is shown in Figure 33.

The transmission through the device was measured by coupling light from a tunable color-center laser, with a wavelength range from 1.500 μm to 1.625 μm. The ratio of transmitted to incident intensity was then measured as a function of wavelength. Figure 34 shows the measured (solid) and calculated (dotted) transmission spectra for this microcavity. A resonance is seen at λ = 1.560 μm, which is within 1% of the calculated resonant wavelength of 1.547 μm. The measured Q is 265, while the calculated Q is 280. The measured values are in remarkable agreement with theory.

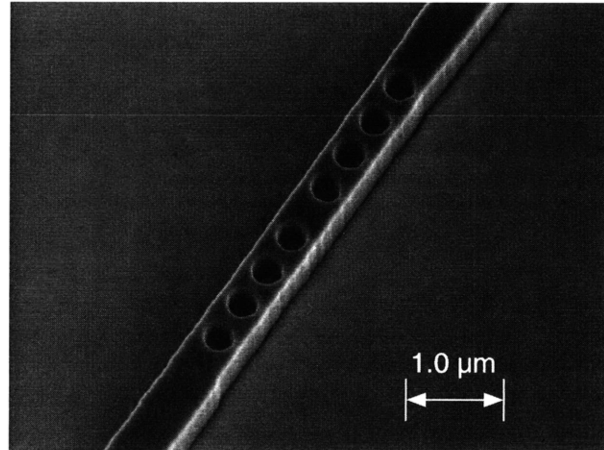


Figure 33. Scanning electron micrograph of a 1D photonic-bandgap microcavity in Si on SiO_2, fabricated using e-beam and x-ray lithographies, Cr liftoff, and reactive ion etching.

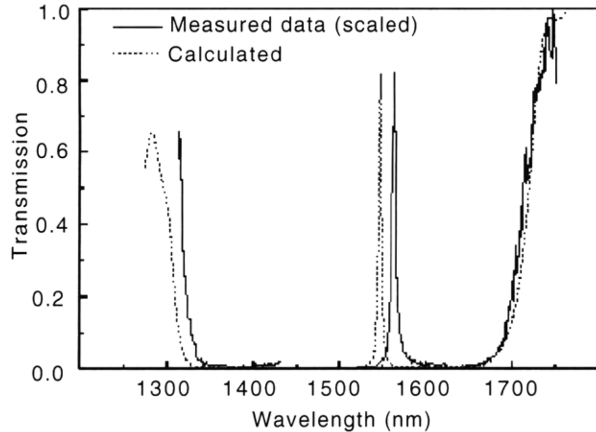


Figure 34. Comparison of measured transmission (solid lines) to calculated transmission (dotted line) for a PBG microcavity with four holes on each side of the microcavity.

4.16 Three-dimensional Photonic Bandgap Structures

Sponsor

National Science Foundation
Grant DMR 94-00334

Project Staff

Minghao Qi, Professor John D. Joannopoulos, Professor Henry I. Smith

In order to achieve a photonic bandgap in three dimensions, the structure must present a periodic modulation of the refractive index in three dimensions. Moreover, that modulation must be of a specific form. To date, two specific types of periodic modulation have been found that theoretically enable a true bandgap for all possible directions of propogation. One of them, illustrated in Figure 35, is designed to enable the use of planar fabrication techniques.

The objective of this project is to fabricate the structure illustrated in Figure 35 by means of a multistep process consisting of: amorphous-Si deposition; lithography and etching of the Si; depostion and planarization of thick SiO_2; reactive-ion etch back of the SiO_2 to the level of the Si; and then a repeat of this sequence until about seven layers are achieved. In between successive layers, a critical alignment step is required, as can be seen from Figure 35. Theoretical anaysis has shown that seven layers are sufficient to achieve a 3D bandgap.

Our approach to date has been to use scanning-electron-beam lithography (SEBL) because of its flexibility, the ease with which design changes can be made, and its ability to perform the precision alignment. SEBL restricts us to relatively small areas because of the slow writing time and problems of drift of the beam location. However, for an initial demonstration small areas are sufficient. If larger areas are required in the future, x-ray lithography could be employed.

Figure 36 illustrates an etched amorphous Si layer, the first step in the process for fabricating seven-layer, 3D photonic-bandgap structures. The lithography is done in NSL's scanning-electron-beam lithography system, and the etching is done by reactive-ion etching in CF_4/O_2.

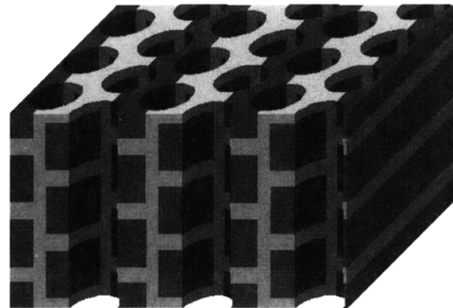


Figure 35. Depiction of a 3D photonic-bandgap crystal to be fabricated at a 790 nm period. The dark gray and light gray regions correspond to Si, with a high refractive index (3.4) and SiO_2, with low index (1.4), respectively.

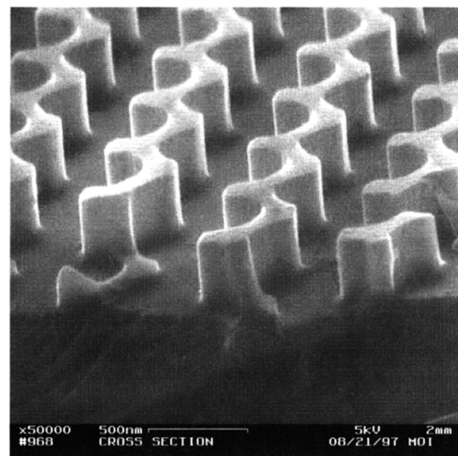


Figure 36. Scanning electron micrograph of a patterned layer of amorphous Si, the first step in the process for fabricating the 3D photonic bandgap structure illustrated in Figure 35.

4.17 Design and Fabrication of an Integrated Channel-Dropping Filter in InP

Sponsors

Defense Advanced Research Projects Agency/
U.S. Air Force - Office of Scientific Research
Contract F49620-96-1-0126

Project Staff

Dr. Jay N. Damask, Michael H. Lim, Juan Ferrera, Mohammed Jalal Khan, Elisabeth M. Koontz, Thomas E. Murphy, Professor Leslie A. Kolodziejski, Professor Hermann A. Haus, Professor Henry I. Smith

In order to meet the ever-growing demand for telecommunications, it will be necessary to exploit the enormous capacity offered by optical communications. Wavelength-division-multiplexing (WDM) is one way to utilize more of the available bandwidth in optical communications by transmitting several distinct communications channels on one optical fiber, each channel at a different wavelength within the communications band (analogous to AM/FM radio transmission.) This technology relies on optical filters to distinguish between the various channels. The channel dropping filter which we are building at MIT is one such device. Its function is to selectively add or drop a single communication channel from an optical communication stream without affecting the remaining channels.

Figure 37 is a sketch of our most recent design of the channel-dropping filter. The bus waveguide carries many communication channels, each centered at a different wavelength. The filtering operation is performed by the quarter-wave-shifted resonators, located on either side of the bus waveguide. The Bragg grating structure, containing an abrupt quarter-wave phase shift in the center, acts as an optical resonator which is excited only by a specific wavelength. The resonant wavelength is tapped off into the upper waveguide of the device, while all other wavelength channels continue along the bus undisturbed. Figure 37 also illustrates the calculated spectral response of the device. Note that the device may also be used in the reverse manner, i.e., to inject or add a specific wavelength channel.

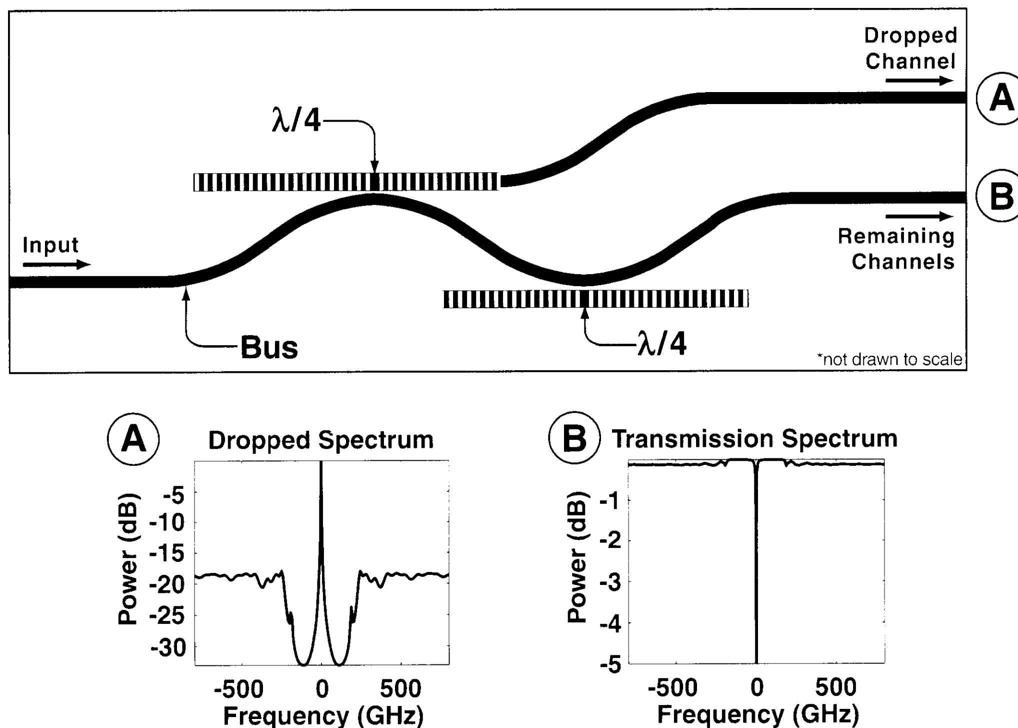


Figure 37. Diagram of the channel-dropping filter design. Several wavelength channels propagate along the bus waveguide, and one particular channel is tapped off into the upper waveguide.

Figure 38 illustrates the waveguide structure of the channel-dropping filter. The device is built on an InP substrate, with a quaternary InGaAsP core material. After the waveguide core and Bragg gratings are patterned lithographically, a final layer of InP cladding (not depicted in Figure 38) is deposited over the top of the structure, thereby creating a channel waveguide. In order for the device to operate within the 1.55 μm communications band, the Bragg-grating period must be approximately 240 nm. Constructing the device in InP offers the potential for integration with other optoelectronic components of the communications system, such as detectors or DFB lasers. Moreover, although the channel dropping filter described here is a passive device, the properties of InP could be later exploited to build related active devices.

The curved-bus design depicted in Figure 37 represents a significant improvement in the channel dropping filter design. Previous designs called for a straight bus waveguide, but we have found that by curving the bus towards and away from the resonators, it is possible to reduce the crosstalk level outside of the grating stop-band. It is important that those channels located far from the center-wavelength of the filter not be transmitted into the upper waveguide along with the dropped channel. Previous straight-bus designs were found to transmit a large fraction of power outside of the grating stop-band into the upper waveguide. Thus, for the straight-bus devices, the number of usable wavelength channels was limited by how many could fit within the grating stopband. The improved curved-bus design helps to ease this constraint by reducing the out-of-band transmission. Moreover, the curved-bus design is predicted to be more tolerant of fabrication errors.

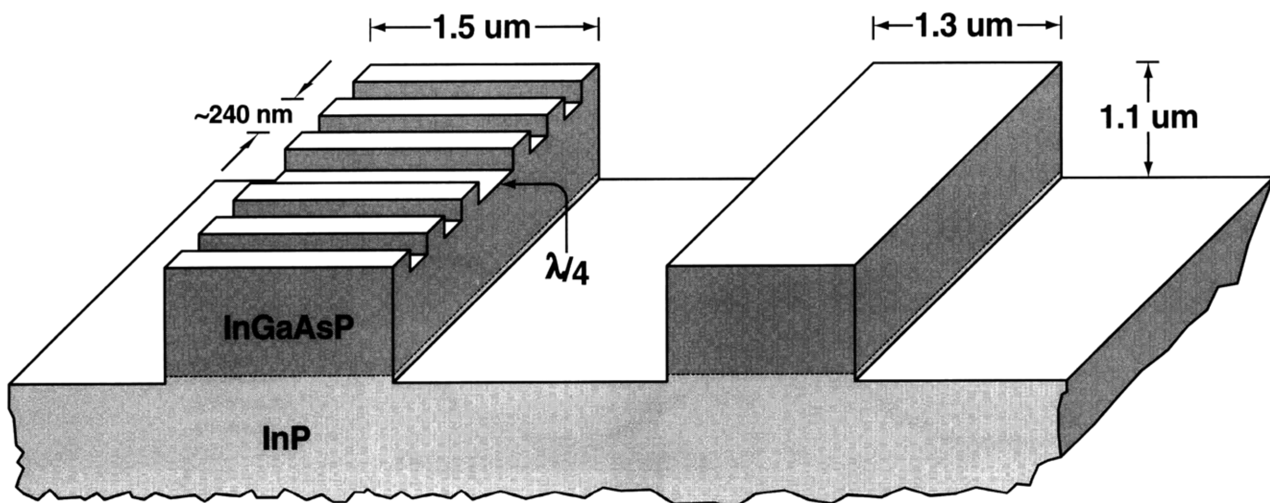


Figure 38. Waveguide structure of the channel-dropping filter. A grating of ~240 nm period is etched into the top surface of the resonator waveguide. After all lithography steps are performed, a final layer of InP cladding (not depicted) is deposited over the structure.

Because the grating period required for the channel dropping filter is ~240 nm, high-resolution nanolithography techniques are required to pattern the Bragg gratings. A further requirement is that the grating patterns be spatially coherent over lengths of several hundred microns. This means that there cannot be any phase errors or stitching errors in the written gratings, something which cannot be achieved with conventional e-beam lithography. We use a technique called spatial-phase-locked e-beam lithography to write the grating patterns onto an x-ray mask. X-ray nanolithography is then used to transfer the fine-period patterns repeatably onto the InP substrates. Spatial-phase-locked e-beam lithography (SPLEBL) uses an interferometrically generated fiducial reference grating on the x-ray mask to ensure that there are no phase errors (or stitching errors) when writing the grating resonators. One significant challenge to building the channel dropping filter is to precisely fabricate a specified grating frequency. The center-frequency of a filter is determined by the period of the grating and the material index of refrac-

tion. If the fabricated grating period is uncertain to 1 nm, the center frequency of the filter could be off by as much as 800 Ghz, which would make the filter completely miss the desired channel. We have developed a novel interferometric lithography system which allows us to repeatably control grating periods to well within 1 nm.

It is crucial to the operation of the channel-dropping filter that the bus waveguide and resonators be synchronous. This means that at the center-frequency of the filter the propagation constants of the two waveguides depicted in Figure 38 must be equal. This translates into tight tolerances on the waveguide and grating geometry. It is therefore important that all lithography steps be carefully characterized and controlled. Additionally, when the final cladding layer of InP is deposited over the top of the device, it is important that the waveguide and grating structures not be disturbed. To this end, we have developed and demonstrated III-V deposition techniques that can be used to deposit material over fine-period gratings without appreciably effecting the shape of the underlying grating structure. The design of the channel-dropping filter has been completed and most of the fabrication steps have been developed and characterized. We are presently in the process of integrating all of the process steps.

4.18 Fabrication of an Integrated Optical Grating-Based Matched Filter for Fiberoptic Communications

Sponsors

Defense Advanced Research Projects Agency/U.S. Air Force - Office of Scientific Research
Contract F49620-96-1-0126

Project Staff

Dr. Jay N. Damask, Thomas E. Murphy, Michael H. Lim, Juan Ferrera, Professor Henry I. Smith.

For future all-optical communication systems, filters are needed for a wide variety of network functions including dispersion compensation, wavelength multiplexing, gain flattening, and noise suppression. This project seeks to develop the technology for building such filters using integrated Bragg gratings. Integrated gratings provide a convenient way to perform filtering operations in a package that can be integrated on a chip with other electronic and optical components of the communications system. As a vehicle for demonstrating this technology, we are in the process of fabricating an integrated matched filter. The matched filter is a grating-based device designed to filter out unwanted noise from an optical communication signal.

The dominant source of noise in most modern communications systems is the broad-band noise generated by amplified spontaneous emission in optical amplifiers. A filter is needed in order to separate the communication signal of interest from this unwanted background noise. Because the broadband noise typically overlaps with the signal of interest, the most suitable filter is one that has a spectral response similar in shape to the signal. The goal of our project is to build a matched-filter, i.e., a filter with a spectral response that is matched to the communications signal. Such a filter is predicted to yield better performance than currently-used Lorentzian filters. Moreover, because the filtering is performed with an integrated Bragg grating, the device has the potential of being integrated with other components of the optical receiver.

One of the most common methods of encoding binary information on an optical signal is to modulate the amplitude or phase to represent a sequence of ones and zeros. Usually, the modulation takes the form of a square wave pattern, where each bit of information occupies one available time-slot. For such square-wave modulation the corresponding signal spectrum has the characteristic sinc shape, centered at the optical carrier wavelength. The integrated Bragg-grating is an ideal filter for such a communications signal. If the length and shape of the grating are properly selected, the reflection spectral response can be made to also have a characteristic sinc shape, matched to the binary communications signal.

Figure 39 illustrates the structure of the integrated matched-filter. The grating is formed by etching a relatively shallow corrugation onto the top surface of the waveguide structure. The length and shape of the grating are selected so that the reflection spectral response is precisely matched to a 10 Gb/s optical signal. In order to separate the reflected filtered signal from the incident noisy input signal, a Mach-Zehnder interferometer configuration is used. A noisy communication signal is launched into the upper port of the device and a codirectional coupler splits the input signal between the upper and lower arms of the interferometer. A portion of the incident light is reflected by identical Bragg gratings in the two arms

of the interferometer. The reflected signals are recombined in the coupling region and emerge in the lower port of the device.

The device depicted in Figure 39 can be extended to perform other filtering functions needed in the optical communications. By merely changing the properties of the Bragg grating such as the shape, period, and length, the spectral response can be tailored to suit alternative needs.

The fabrication of integrated grating devices presents many fabrication challenges. We have developed a flexible and robust method of constructing integrated Bragg-grating-based devices which solves some of the critical problems of alignment, period selection and grating fidelity.

While conventional photolithography is used to pattern the waveguide features of the device, patterning the fine-period grating structures requires high-resolution nanolithography techniques. We employ interferometric lithography to generate uniform, spatially-coherent gratings on x-ray masks. X-ray nanolithography is then used to transfer the grating patterns onto the substrate. We have devised an interferometric lithography system that enables us to control the grating period to within 1 nm. This is essential in order to achieve a desired center-frequency of the filter.

The integrated-matched filter requires that the sub-micron-period gratings are etched into the top surface of relatively tall (~7 μm) waveguides. To perform nanolithography over such extreme topography, we have developed a novel scheme, depicted in Figure 39 which allows all of the lithography steps to be performed over essentially planar surfaces. In this procedure, separate "hard mask" materials are used for the waveguide etch and the grating etch. The "grating" hard-mask is patterned first; then the "waveguide" hard-mask is deposited and patterned as illustrated in Figure 40. The two can be distinguished in a subsequent process step by selective chemical etching.

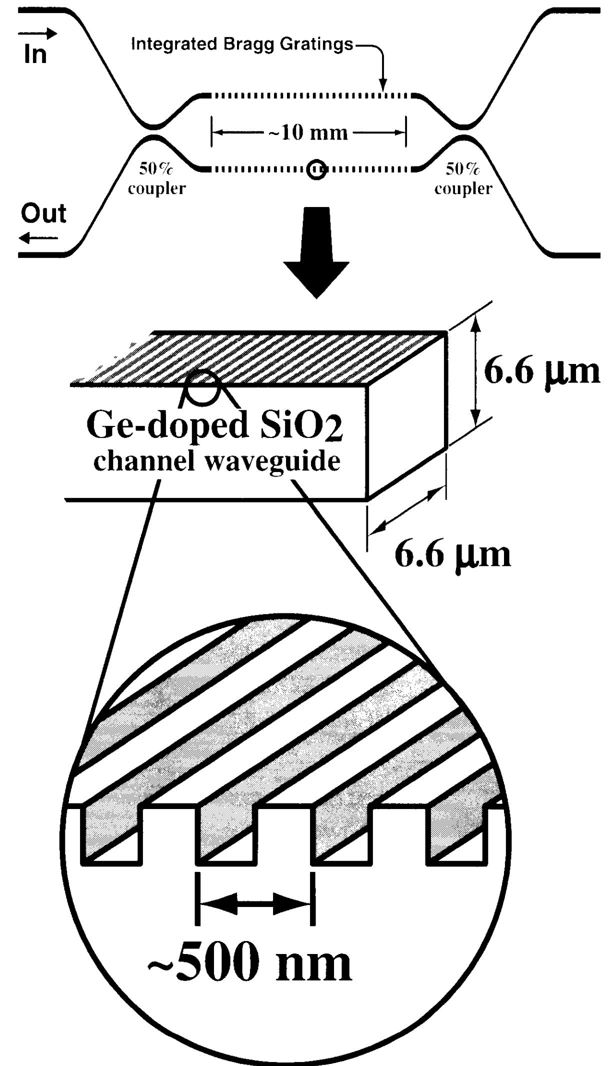


Figure 39. Schematic of an integrated optical matched-filter. The waveguide consists of a germanium-doped SiO_2 core, 6.6 μm wide and tall, surrounded by SiO_2 cladding. The 10 mm-long Bragg grating is formed by etching a shallow, 535 nm-period grating onto the top of the waveguide before the upper cladding layer is deposited. The waveguide interferometer is designed to redirect the reflected filtered signal to a separate output port.

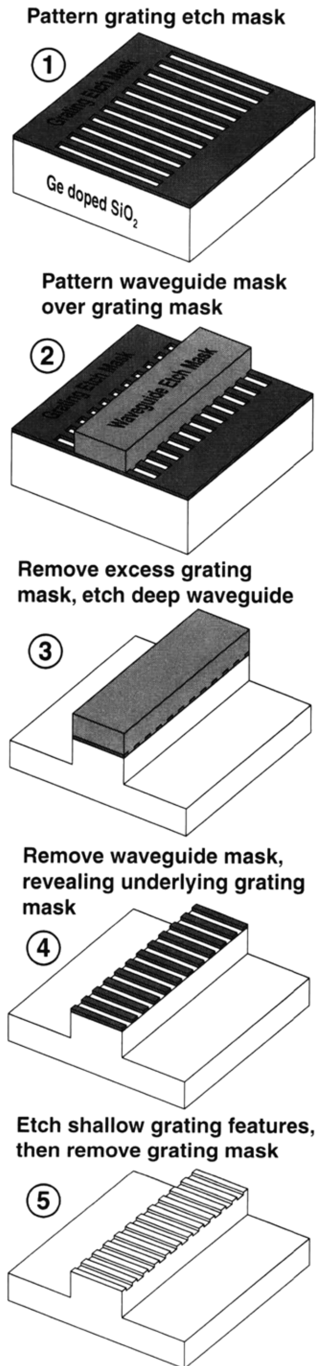


Figure 40. Fabrication sequence used to etch gratings into tall waveguides. This sequence enables both high-resolution and low-resolution lithography steps to be performed over essentially planar surfaces. The only requirement is to find two compatible etch-mask materials that can be selectively removed in subsequent steps.

It is crucial to the operation of the matched filter that the arms of the interferometer be equal in optical path length. Accordingly, the Bragg grating k-vectors must be accurately aligned to the waveguide axes, e.g., within 0.2 mrad. To achieve this, we have used e-beam lithography to add alignment marks, 20 mm apart, to an interferometrically-patterned x-ray mask. A special procedure enables the e-beam system to ensure k-vector alignment. Complementary marks are included on the waveguide mask, thereby enabling angular alignment better than 0.2 mrad.

With this device, we hope to demonstrate an integrated optical grating-based noise filter that improves the performance of an optical receiver. Moreover, we believe the fabrication technology developed for this device can be applied to many other related active and passive grating-based devices.

4.19 High-Dispersion, High-Efficiency Transmission Gratings for Astrophysical X-ray Spectroscopy

Sponsor

National Aeronautics and Space Administration
Contract NAS8-38249

Project Staff

Dr. Joost van Beek, Robert C. Fleming, P. Hindle, Jeannie M. Porter, Jane D. Prentiss, Robert D. Sisson, Professor Claude R. Canizares, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Through a collaboration of the Center for Space Research (CSR), the NanoStructures Laboratory (NSL), and the Microsystems Technology Laboratory (MTL), x-ray transmission gratings are fabricated for the NASA Advanced X-ray Astrophysics Facility (AXAF) x-ray telescope, scheduled for launch on the Space Shuttle in 1998. This major national facility will provide high-resolution imaging and spectroscopy of x-ray-emitting astrophysical objects, with unprecedented power and clarity, promising to significantly widen our view of the Universe.

Many hundreds of large-area, gold transmission gratings with 200 nm and 400 nm periods are required for the high-energy transmission grating spectrometer (HETGS) on AXAF, which will provide high-resolution x-ray spectroscopy in the 100 eV to 10 keV band. In order to achieve spectrometer performance

goals, the gratings need to have very low distortion (< 200 ppm), and high-aspect-ratio structures, significantly pushing the state-of-the-art of nanofabrication.

The need for high grating quality, and an aggressive production schedule, demanded the development of a robust, high-yield manufacturing process. We adopted a scheme that uses interferometric lithography with tri-level resist, followed by cryogenic reactive-ion etching and gold electroplating (see Figure 41). A chemical etching step then yields membrane-supported gratings suitable for space use. The gratings undergo extensive testing before being assembled in the spectrometer.

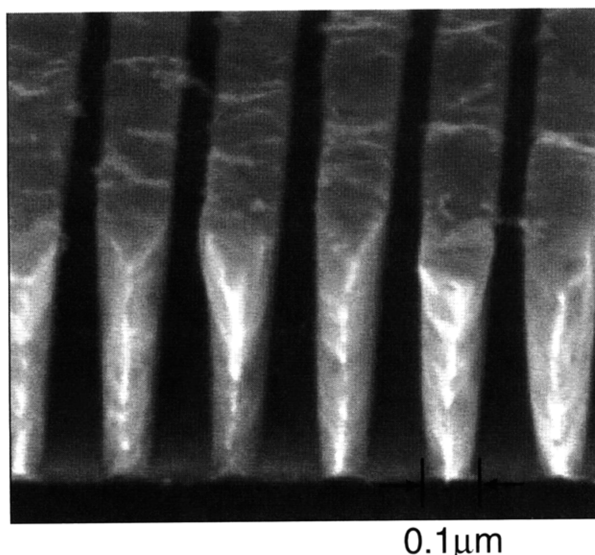


Figure 41. Scanning-electron micrograph of a 200 nm-period gold x-ray transmission grating, cleaved to show the 100 nm-wide lines.

A new cleanroom fabrication facility was built (the Space Microstructures Laboratory on the fourth floor of Building 37 adjacent to the Gordon Stanley Brown Building), in order to fabricate the AXAF gratings. The proximity of the new lab to the NSL and MTL allows the sharing of many services such as DI and process water, nitrogen, process vacuum, and waste drains. The SML space includes 1700 square-feet of Class 100 clean room and associated support areas, and a large complement of state-of-the-art equipment. Production of flight gratings has now been completed and flight spares production is underway. In October 1996, NASA took delivery of the completed HETGS flight instrument (Figure 42), which is now undergoing calibration and integration.

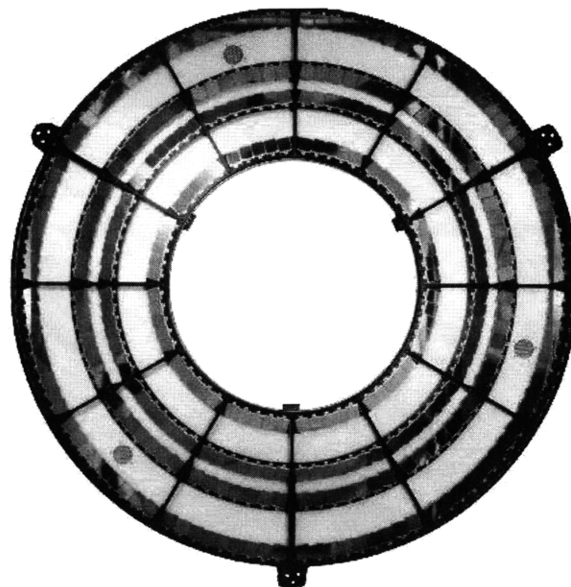


Figure 42. Photograph of the HETGS flight instrument, which consists a 1.0 meter-diameter aluminum wheel populated with hundreds of 200 nm and 400 nm-period gold x-ray transmission gratings (340 total).

4.20 Super-smooth X-ray Reflection Gratings

Sponsors

Harvard-Smithsonian Astrophysical Observatory
Contract SV630304
National Aeronautics and Space Administration
Grant NAG5-5105

Project Staff

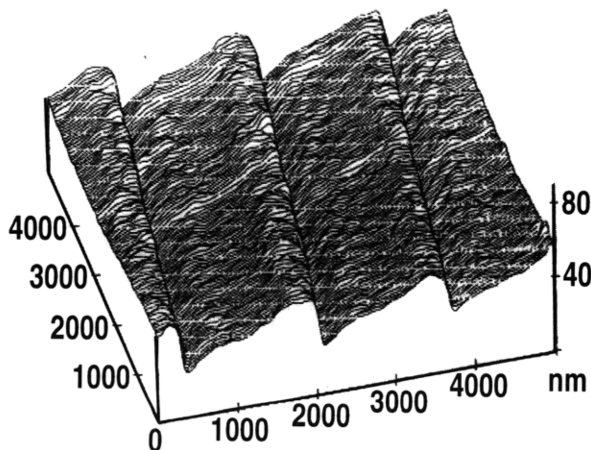
Dr. Joost van Beek, Robert C. Fleming, Andrea E. Franke, Jeannie M. Porter, Jane D. Prentiss, Robert D. Sisson, Dr. Mark L. Schattenburg, Professor Claude R. Canizares, Professor Henry I. Smith

Grazing-incidence x-ray reflection gratings are an important component of modern high-resolution spectrometers and related x-ray optics. These have traditionally been fabricated by diamond scribing with a ruling engine or, more recently, by interferometric lithography followed by ion etching. These methods result in gratings which suffer from a number of deficiencies, including high surface roughness and poor groove profile control, leading to poor diffraction efficiency and large amounts of scattered light.

We are developing improved methods for fabricating blazed x-ray reflection gratings which utilize special (111) silicon wafers that are cut 0.7 degrees off the (111) plane. Silicon anisotropic etching solutions such as potassium hydroxide (KOH) etch (111) planes extremely slowly compared to other crystallographic planes, resulting in the desired super-smooth blaze surface. Previous work used similar off-cut (111) silicon substrates to fabricate blazed diffraction gratings. However, that method utilized a second KOH etch step which compromised the grating facet flatness and is unsuitable for small grazing angle x-ray diffraction.

Our gratings are patterned using interferometric lithography with the 351.1 nm wavelength, and transferred into the substrate using tri-level resist processing, reactive-ion etching (RIE), and silicon nitride masking during the KOH etch. The narrow (~100 nm) ridge of silicon which supports the nitride mask is removed using a novel chromium lift-off step followed by a CF4 RIE trench etch. The result is an extremely-smooth sawtooth pattern, which is suitable for x-ray reflection after applying a thin evaporated coating of Cr/Au (Figure 43). Gratings have been tested with special x-ray spectrometers in the laboratories of our collaborators at Columbia University and the Lawrence Berkeley National Laboratory. Peak gratings efficiencies achieved are ~35% greater than those of the best available ruled masters of comparable design (see Figure 44).

Potential applications of these improved gratings are for laboratory and satellite-based high-resolution x-ray spectroscopy. The next phase of the work will continue more in-depth x-ray testing and attempt to produce gratings on lightweight substrates suitable for astrophysical use.



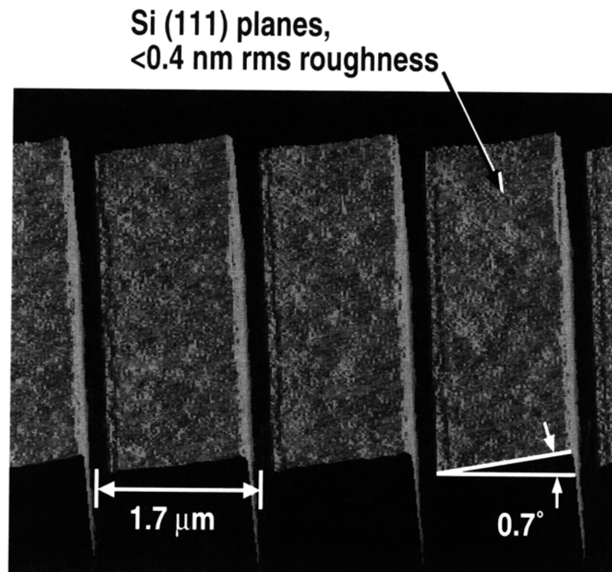


Figure 43. (a) An AFM image of a traditional mechanically-ruled and replicated x-ray reflection grating.[1] Note the rough, wavy grating surfaces which lead to poor diffraction performance. (b) An AFM image of a blazed x-ray reflection grating fabri-cated by anisotropic etching of special off-cut (111) silicon wafers. Note the improvement of grating surface flatness and smoothness, leading to significantly improved performance.

1 Bixler et al., *Proc. SPIE* 1549: 420-8 (1991).

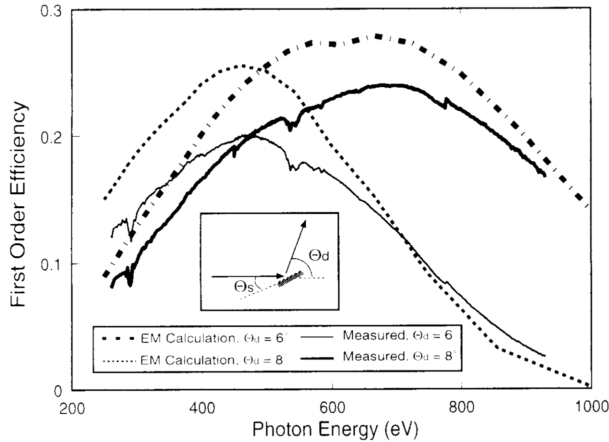


Figure 44. Comparison of x-ray diffraction efficiency measured at Lawrence Berkeley Laboratory and electromagnetic finite element calculations performed at Columbia University. Peak gratings efficiencies achieved are ~35% greater than those of the best available ruled masters of comparable design.

4.21 Transmission Gratings as UV-blocking Filters for Neutral Atom Imaging

Sponsors

Los Alamos National Laboratory
Contract E57800017-9G
Southwest Research Institute
Contract 83832

Project Staff

Dr. Joost van Beek, Robert C. Fleming, P. Hindle, Jeannie M. Porter, Jane D. Prentiss, Robert D. Sisson, Professor Claude R. Canizares, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Neutral-atom-beam imaging detectors are used to study dilute plasmas in laboratory systems such as tokamaks, and in astrophysical environments such as the magnetospheric region of the Earth. Neutral atom emission can be a particularly useful probe of plasmas since neutrals travel in straight lines of sight, unperturbed by electromagnetic fields.

Charge-exchange interactions between solar-wind particles and atoms in the Earth's tenuous outer atmosphere are predicted to form strong currents of neutral atoms (mostly oxygen and helium) emanating from the Earth, which, if they could be imaged, would provide unprecedented real-time mapping of this complicated magnetohydrodynamic environment. This information would be valuable in safeguarding the health of orbiting satellites and ensuring the stability of our nation's electric power grid.

Unfortunately, sensitive orbiting neutral-beam detectors are easily overwhelmed by the bright flux of UV photons typically emitted from astrophysical plasmas (mostly the 121.6 nm emission from hydrogen and the 58.4 nm emission from helium). Filters which allow the passage of low-energy neutral atoms but block UV light are essential for the performance of this instrumentation. Through several years of collaboration with the Los Alamos National Laboratory (LANL), the University of West Virginia, and the University of Southern California, we have developed neutral-beam filters which consist of mesh-supported 200 nm-period gold transmission gratings with 30-60 nm wide slots (Figure 45). The tall, narrow slots in the gratings behave as lossy waveguides at or below cutoff, providing discrimination on the order of millions between UV and atoms.

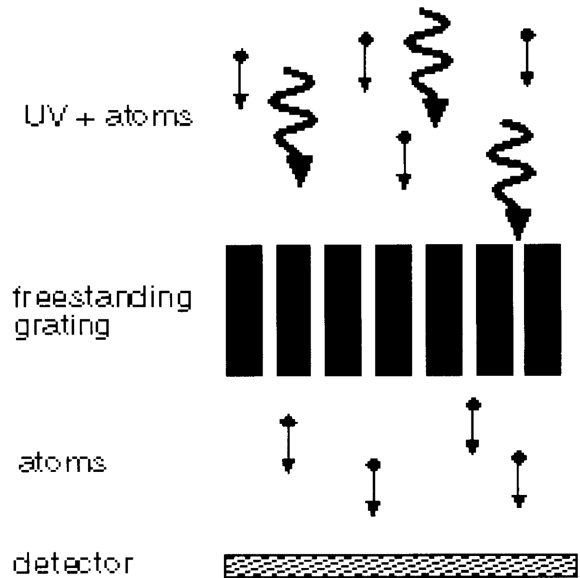


Figure 45. Concept of UV filtering by means of a metal freestanding grating. As a result of polarization and waveguide effects UV is blocked while allowing the passage of atoms. In this way, UV background counts on the atom detector are avoided.

We are fabricating flight grating filters for the Medium Energy Neutral Atom (MENA) instrument on the NASA Magnetospheric Imaging Medium-Class Explorer (IMAGE) mission, scheduled for launch in January 2000. The gratings are fabricated by interferometric lithography with tri-level resist, followed by

cryogenic reactive-ion etching and gold electroplating. An additional masking step followed by nickel plating fabricates the mesh support structure, and a final chemical etching step yields mesh-supported gratings suitable for space use (Figure 46).

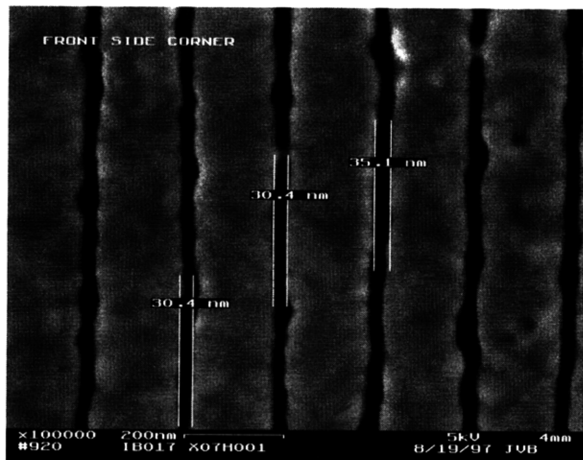


Figure 46. A scanning-electron micrograph image showing a close up of the UV blocking grating. Due to the narrow slot width of 30-35 nm, and the large slot depth (~500 nm), the UV transmission of the grating is extremely low (10^{-5} to 10^{-6} at 121.6 nm), while decreasing the transmitted atomic flux only by a factor of ten.

4.22 Submicrometer-Period Transmission Gratings for X-ray and Atom-Beam Spectroscopy and Interferometry

Sponsors

Joint Services Electronics Program
Grant DAAH04-95-1-0038
National Aeronautics and Space Administration
Contract NAS8-38249
Grant NAGW-2003

Project Staff

Jeannie M. Porter, Timothy A. Savas, Dr. Mark L. Schattenburg, Professor Henry I. Smith

Transmission gratings with periods of 100-1000 nm are finding increasing utility in applications such as x-ray, vacuum-ultraviolet, and atom-beam spectroscopy and interferometry. Over 25 laboratories around the world depend on MIT-supplied gratings in their work. For x-ray and VUV spectroscopy, gratings are made of gold and have periods of 100-1000 nm and thicknesses ranging from 100-1000 nm. The gratings are most commonly used for spectroscopy of the x-ray emission from high-temperature plasmas. Transmission gratings are supported on thin (1 μm) polyimide membranes or made self supporting ("free standing") by the addition of crossing struts (mesh). (For short x-ray wavelengths, membrane support is desired, while for the long wavelengths, a mesh support is preferred in order to increase efficiency.) Fabrication is performed by interferometric lithography combined with reactive-ion etching and electroplating. Progress in this area tends to focus on improving the yield and flexibility of the fabrication procedures.

Another application is the diffraction of neutral-atom and molecular beams by mesh supported gratings. Lithographic and etching procedures have been developed for fabricating free-standing gratings and grids in thin silicon nitride (SiN_x) supported in a Si frame. Figure 47 shows a free-standing 100 nm period grating in 100 nm-thick silicon nitride. Figure 48 shows a 100 nm-period free-standing grid in 100 nm thick SiN_x membrane. Such a grid is used in experiments as a "molecular sieve."

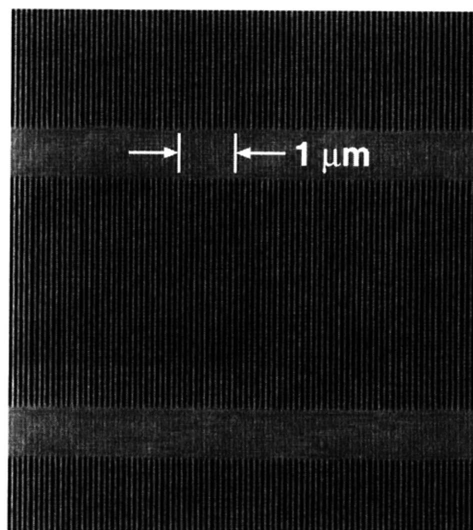


Figure 47. Scanning electron micrograph of a free-standing 100 nm-period grating in a silicon nitride membrane of area 500 μm by 5 mm.

We have established a collaboration with the Max-Planck Institute in Göttingen, Germany, in which they utilize our gratings and grids of 100 nm period in diffraction experiments using He atom beams. Figure 49 shows a spectrum obtained by diffracting a He beam through a 100 nm-period transmission grating. In addition, we have established a collaboration with

Professor David E. Pritchard at MIT. His group uses our 100 nm-period gratings in diffraction and interferometer experiments with neutral sodium atom beams.

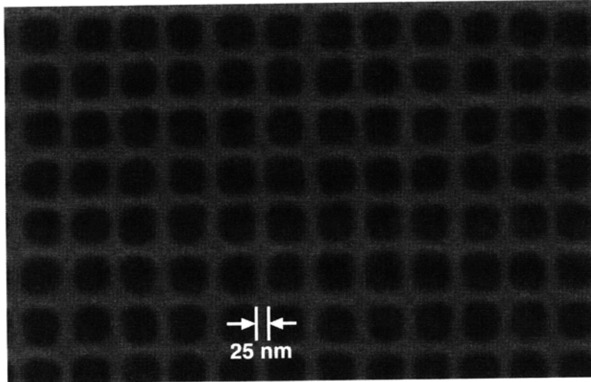


Figure 48. Scanning electron micrograph of a free-standing 100 nm period grid in a silicon nitride membrane of area 500 μm by 5 mm. Such grids are used in experiments to separate out Helium trimers from other clusters.

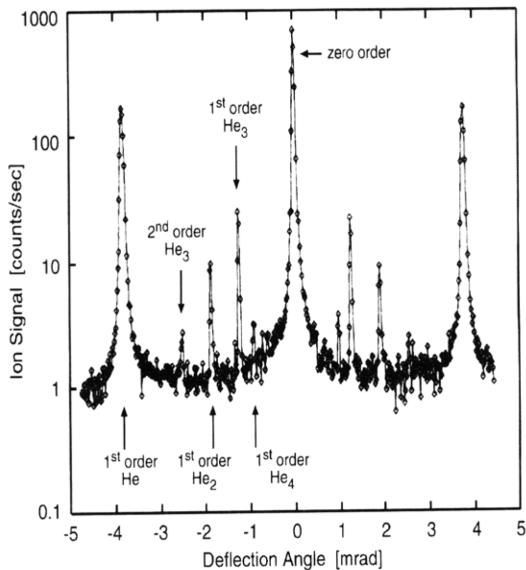


Figure 49. Helium beam diffraction spectrum. These results were obtained by Wieland Schoellkopf and Peter Toennies at the Max-Planck Institute in Göttingen, Germany, using a grating such as in Figure 47.

4.23 Field-Emitter-Array Flat-Panel Displays for Head-Mounted Applications

Sponsor

MIT Lincoln Laboratory
Advanced Concepts Program

Project Staff

David Pflug, Professor Akintunde I. Akinwande, Professor Henry I. Smith, Dr. Carl Bozler

Advances in nanostructure technology have made feasible small, high-resolution, high-brightness and high-luminous-efficiency field-emitter-array image sources for head-mounted displays (HMDs). HMDs are expected to have a variety of applications in military, medical, commercial and entertainment fields. The technology most commonly used in deployed HMD systems is the CRT which is bulky because of the use of a single-electron gun to generate images on a cathodoluminescent screen, but has the most desirable attributes of high luminous efficiency, high brightness and easy image rendition. The relay optics required for see-through HMDs become complicated because of the bulky nature of the CRT. For other applications such as entertainment virtual reality, the most commonly used image source is the backlit active matrix liquid crystal display (AMLCD). It is thin, has high resolution, and the addressing electronics are integrated on the same substrate as the image source. However, the backlit AMLCD image source does not have sufficient brightness or luminous efficiency for application to see-through HMDs.

Our approach to demonstrating a small, high-resolution, high-luminous-efficiency and high-brightness display is the field-emitter array flat-panel display (FED) which incorporates a high-density, high-performance array of low-voltage field emitters, as shown in Figure 50. CMOS-controlled electron emission from the tips impinge on a cathodoluminescent screen. It is thus possible to integrate the addressing and signal conditioning electronics on the same substrate as the field-emitter arrays (FEAs). The main advantage of this approach is the reduction in the number of wires and p bond pads from about 2,000 to about 50. For example, it will be difficult to attach greater than 2,000 wires to bond pads in a 1.5 inch x 1.5 inch area and obtain ultra-high vacuum in the display envelope. High-resolution (>1000 dpi) FEDs are

only possible if the addressing/driver and other signal conditioning electronics are integrated on the same substrate as the field emitter arrays.

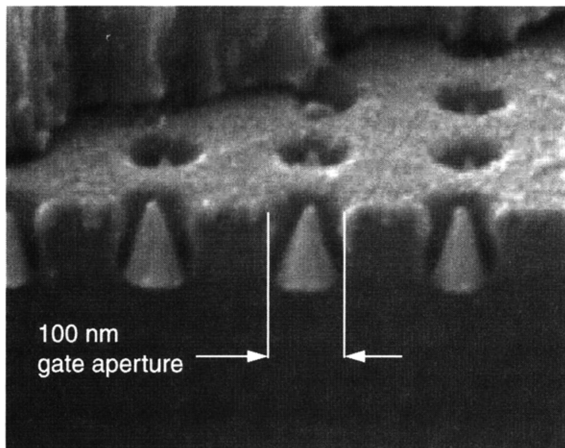


Figure 50. 100 nm gate aperture molybdenum field emitter cones with chromium gate, formed using a vertical evaporation.

Our initial objective is to demonstrate the integration of Si CMOS technology with low voltage field-emitter arrays fabricated using interferometric lithography. This project requires the fabrication of Si CMOS wafers with one or two levels of metal interconnect followed by surface planarization using CMP technology. Interferometric lithography is then used to define Molybdenum-cone field emitter arrays that are 200 nm tip-to-tip and have less than 50 nm gate-to-emitter separation. Fabricated field-emitter cone arrays with a 320 nm period have demonstrated emission currents of 1 mA at gate voltage of 20V from 900 cones in a 10 μm x 10 μm area. This current is more than adequate for a brightness of 1000 fL at a screen voltage of 500V.

Our initial efforts have focused on modeling the scaling behavior of FEA devices. Numerical simulation and computer models to predict FEA performance have been developed and continue to be refined. These models allow us to obtain a correlation between different device geometries (cone tip radius or curvature, gate aperture etc.) and the emitter's output characteristics. The results of this study have directed our fabrication efforts toward devices whose performance will not only be better, but more dependent on geometries that can be well controlled in the manufacturing process. Preliminary results indicate that we will be able to increase the current density and reduce the operating voltage by decreasing the tip-to-tip separation to 200 nm.

FEAs of 200 nm period have been fabricated using the interferometric lithography and are being integrated with additional metallization layers and conventional lithography to create discrete arrays for electrical characterization. The fabricated cones have similar size and structure to those simulated. After electical characterization, the process will be expanded to include the fabrication on substrates containing standard CMOS driver and control circuitry.

A semiautomated ultra-high vacuum (UHV) probe chamber has been developed for the electrical characterization of FEAs. This test bed allows the performance of the arrays to be evaluated without the lengthy overhead of vacuum packaging. Device performance has been shown to be not only dependent on the devices physical structure, but also on surface contamination that may have resulted during fabrication and MEMS processing. The UHV probe chamber has the capability to do device conditioning including ECR plasma cleans and wafer bake-out. The system is designed to allow future expansion to include surface analysis chambers including a Kelvin Probe, Scanning Maxwell Microscope, and Auger. We plan to demonstrate the use of a load transistor to limit the current in the field-emitter array. Previous approaches have used high valued resistors in series with the field-emitter arrays to control the current density and its uniformity. This is critical to the control of brightness across the display because Fowler-Nordheim emission depends exponentially on the ratio of the gate voltage to the tip radius of curvature (Vg/r). It is therefore very sensitive to small changes in the radius of curvature. It should be possible to control the emitted current density using the gate voltage of the transistor load and demonstrate the feasibility of analog voltage gray scale or temporal gray scale.

The above demonstrations will go a long way to showing the feasibility of high-brightness, high-resolution FEA image sources for head-mounted displays.

4.24 Development of High-Speed Distributed Feedback (DFB) and Distributed-Bragg Semiconductor Lasers

Sponsor

MIT Lincoln Laboratory
Contract BX-6558

Project Staff

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High-speed semiconductor lasers are becoming increasingly important for high-speed optical communication links. With the advent of wavelength-division multiplexing (WDM) technology, single-mode high speed distributed-feedback (DFB) and distributed-Bragg-reflector (DBR) lasers are receiving increased attention. These lasers can be directly modulated at frequencies reaching 30 to 40 GHz. Presently, external electro-optic modulators provide the highest modulation bandwidth. However, direct modulation schemes are usually much simpler to implement and integrate. Therefore, any progress made in improving the high frequency performance of semiconductor lasers will have immediate applications in optical communications. The goal of this project is to develop DFB and DBR lasers capable of being modulated at high speeds with low distortion and chirp.

High-performance DFB and DBR lasers demand careful attention to the design of the grating which provides the optical feedback. Spatial hole burning, side mode suppression, radiation loss, laser linewidth, spontaneous emission in non-lasing modes, lasing wavelength selection and tunability, laser relaxation oscillation frequency are all features that are very sensitive to the grating design. Improved grating design can significantly enhance laser performance, especially at high frequencies. In the last few years, various techniques have been developed in the NanoStructures Laboratory that allow fabrication of gratings with spatially varying characteristics and with long-range spatial-phase coherence. Chirped optical gratings with spatially varying coupling parameter can be made using a combination of interferometric lithography, spatially phase-locked electron-beam lithography, and x-ray lithography. This provides a unique opportunity for exploring a wide variety of grating designs for semiconductor DFB and DBR lasers. We plan to explore laser devices suited for high-speed as well as low-noise operation.

We have developed techniques for fabricating high speed polyimide-planarized ridge-waveguide laser structures that have low capacitance and are therefore ideally suited for high frequency operation. A cross section of an InP based DFB laser is shown in Figure 51. The active layers consist of multiple InGaAsP quantum well layers. The grating is etched in InP, and InGaAsP is regrown on top. The ridge is etched and then planarized using polyimide. Ohmic contact to the ridge is made by liftoff on top of the polyimide layer. RC rolloff is one of the most important factors that limit the high-frequency performance of lasers. The thick layer of polyimide reduces significantly the capacitance between the top metal electrode and the substrate. In addition to this structure, we are also exploring laser structures with co-planar microwave striplines for the ridge and substrate ohmic contacts. This is illustrated in Figure 52. This design offers improved high-frequency performance and low series resistance.

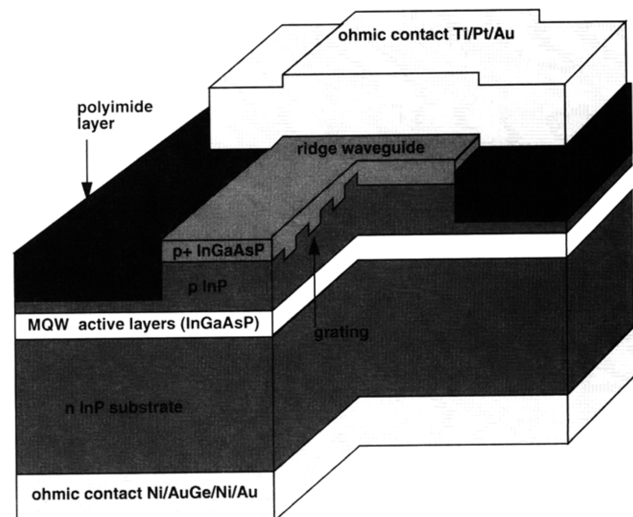

Figure 51. Polyimide-planarized InP-based DFB ridge-waveguide laser for 1.55 um operation.

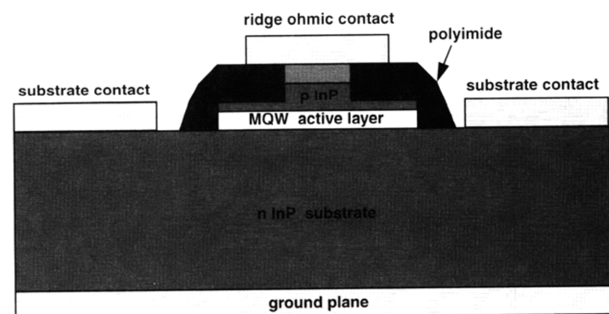

Figure 52. High-speed laser structure with top substrate contact.

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