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An Oscilloscope Array for High-Impedance Device Characterization

Fred Chen, Anantha Chandrakasan, Vladimir Stojanović

Department of Electrical Engineering
Massachusetts Institute of Technology
Cambridge, MA 02139
{fredchen,anantha,vlada}@mit.edu

Abstract— An equivalent time oscilloscope array is implemented in a 90nm CMOS technology. A combination of adjustable termination, calibration circuitry and capacitance compensation enables driver bandwidths between 0.4 to 2GHz for termination impedances of 20k Ω to 2k Ω for extraction of S-parameters and delay characteristics of high impedance devices such as carbon nanotubes (CNTs) and graphene. Measurement results show that the capacitance compensation technique enhances the bandwidth by 3X for impedances between 2k Ω and 20k Ω .

I. INTRODUCTION

Characterizing both DC and high-frequency characteristics of nanoscale devices such as CNTs, graphene and nanowires is a critical step in determining their viability for semiconductor applications [1]. Previous efforts to measure high frequency characteristics of CNTs have been limited by a handful of common problems. First, the traditional approach of using a network analyzer (VNA) to capture the frequency response is limited by the poor power transfer between the high impedance (>10k Ω) of the device and the 50 Ω test equipment termination. This impedance mismatch offsets the selective bandwidth of the VNA used to reduce the noise floor, resulting in a large variance of measured data due to signals being at or near the noise floor. Second, measurement parasitics from test probes and pads often dominate the reactance of the CNTs being measured both limiting the accuracy of the results and the bandwidth of the measurement. Third, given the dimensions of CNTs, test setups are difficult to reproduce, limiting the range of lengths and number of CNTs that can be measured.

To address these issues, we have developed an on-chip test platform consisting of an array of 256 transceivers. Fig. 1 shows a SEM image of the test-chip which is divided into two regions—a

higher termination impedance region (right) for long CNT/device measurements and a lower termination impedance region (left) for multi-wall CNT via or bundled CNT/device measurements. A transceiver, whose layout is shown in the inset of Fig. 1, occupies a 100 μm x 100 μm area beneath each pad, and is independent of all other transceivers allowing for measurements between any two pads in the array. A capacitance compensation technique is used to allow full sized 52 μm square bond pads for device characterization at the chip interface while maintaining input drive bandwidths up to 2GHz for a 2k Ω termination. Each transceiver has an adjustable termination, nominally between 2k Ω and 20k Ω , enabling better power transfer by providing flexibility to match varying device impedances. The adjustable termination used in conjunction with several calibration circuits also enables direct measurement of resistance and capacitance seen at the pad. Combined with several on-chip test coupon transceivers that contain varying pad components, these various measurement approaches aid in de-embedding test setup parasitic from device measurements.

II. TRANSCEIVER ARCHITECTURE

A. System Architecture

Fig. 2 shows the top level block diagram of two transceivers linked by a CNT ‘channel’. Similar to the technique used in [2] but implemented with mostly on-chip components, the step response of the channel is captured by changing the threshold voltage of the sampler ($VREF$) and the relative phase of the receiver clock ($RxCik$) with respect to the transmit clock ($TxCik$). Each transceiver is capable of capturing the waveform at its input so both the launched and received waveforms in a link can be captured simultaneously.

Fig. 3 highlights the measurement infrastructure and test setup for the system. The sampler reference voltage ($VREF$) is provided by a 16-bit off-chip DAC which provides sub-mV voltage resolution. The DAC also provides the sampler calibration voltage and drives the reference currents for the chip. To get both good frequency resolution and range, fine phase control over a long period is required. To achieve this dynamic range, an external PLL with 6.5ps delay steps feeds a 16-bit programmable clock divider to generate the receive clock while the reference for the PLL feeds a similar clock divider to drive the transmit clock. As shown in Fig. 3, rotating the

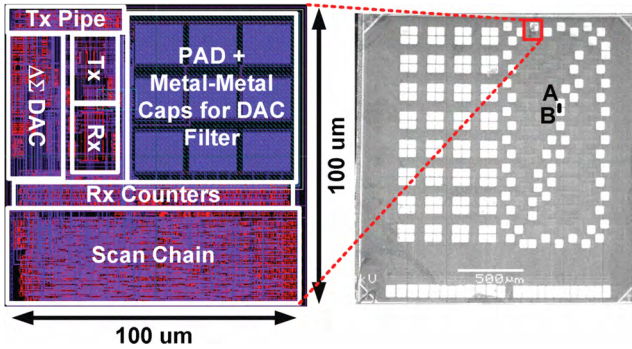


Fig. 1. SEM of the test chip (right) and a transceiver layout (left). Points A and B indicate the link shown in the CNT measurement in section III

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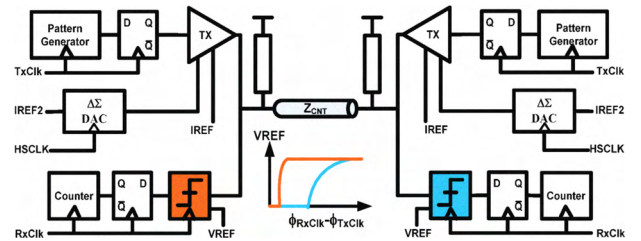


Fig. 2. Block diagram of 2 transceivers linked by a CNT and conceptual waveforms captured by shifting $VREF$ and $RxCik$

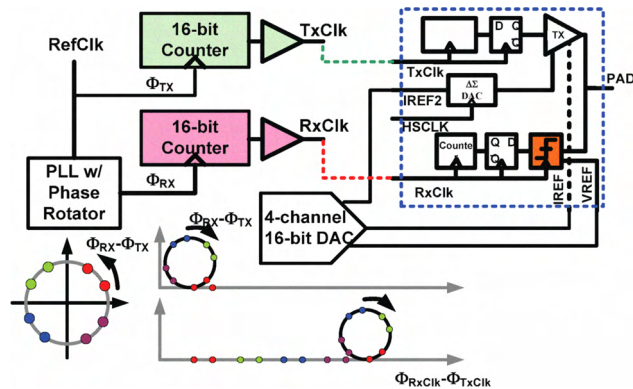


Fig. 3. Measurement infrastructure enabling both voltage and timing resolution and range

phase difference between the input clocks of the dividers will cause the divider output phase difference to accumulate thereby realizing a large time step range while maintaining fine time step resolution.

B. Receiver Design

The power transfer of the sub-sampling approach is better than that of a VNA measurement, but being a wideband measurement its noise floor is higher. To improve the noise floor of this sub-sampling approach, a pair of 20-bit counters is used to accumulate a million samples per test point to average out timing noise due to jitter and any dynamic voltage offsets in the sampler.

Fig. 4 shows the sampler circuit (left) which is derived from [3] and modified to allow for rail-to-rail operation by adding PMOS devices at the input. Since the termination impedances being used are large, it is critical to minimize any capacitances at the pad interface. This topology is chosen for its high bandwidth per unit input device size and because power is not a constraint for the system. Also, because the sampler input devices are nearly minimal, it is expected that there will be large offsets due to device mismatch and varying input common mode. To calibrate out this offset, the offset for each sampler can be measured using an external reference voltage (V_{CAL}) through a muxed input to the V_{IN} port and subsequently calibrated out of any measured step responses.

C. Transmitter Design

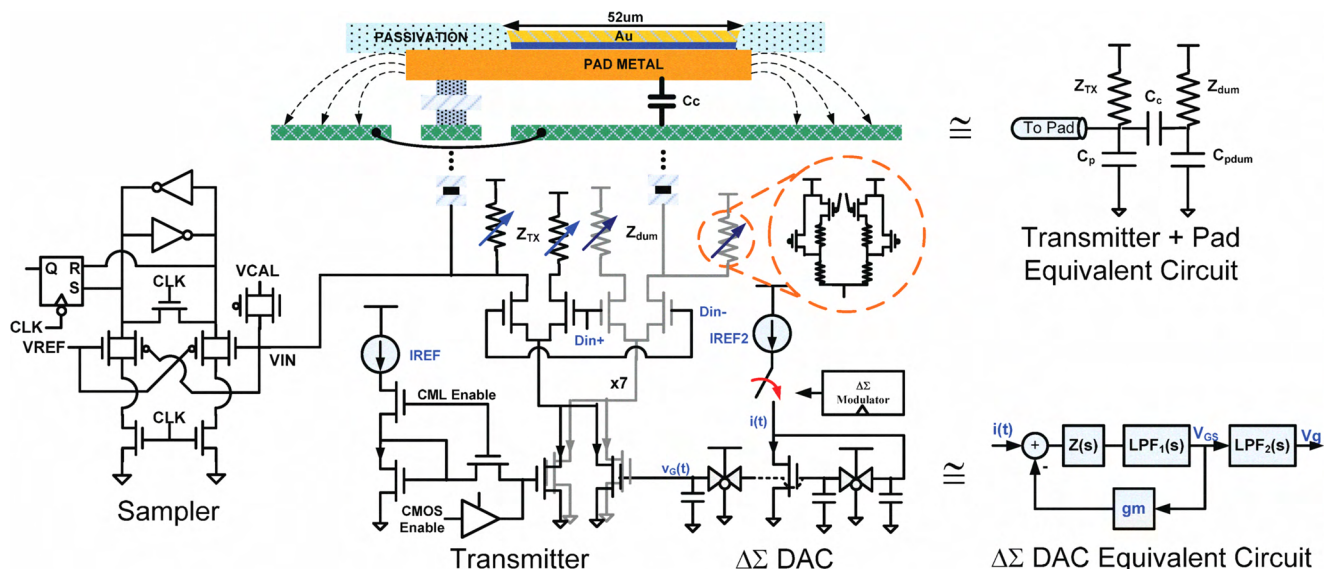
Similar to the receiver, it is critical that the parasitic capacitance of the transmitter be minimized to enable as high an output bandwidth as possible. Since the goal is also to enable a large pad interface, the parasitic capacitance of the pad needs to be mitigated. Fig. 4 shows the transmitter and pad structure that is used to accomplish this. The transmitter differential pair is segmented into two parts; the active driver portion, connected to the pad, and a dummy portion connected to a ‘shield’ located under the pad. The ‘shield’ acts as an intermediate node to which most of the pad parasitic capacitances are coupled to. The termination, driver transistor sizes, and drive currents for the main driver and dummy driver are sized proportionally such that they have equivalent bandwidths and range (i.e. $Z_{\text{dummy}}I_{\text{dummy}}=Z_{\text{TX}}I_{\text{TX}}$). Thus, during operation, the dummy driver and main driver will drive their respective nodes to equivalent voltages eliminating most of the pad parasitic capacitance, C_C , seen at the pad.

Also shown in Fig. 4 is a delta-sigma current DAC that biases the output current via a parallel current path. The DAC provides linear control of the bias current at low reference currents and is used for calibration and measurement of the termination resistances. A delta-sigma modulator, implemented using a digital accumulator, modulates the reference current into the current mirror. Despite the non-linearity of the current mirror's transconductance, the mirror perfectly extracts the desired bias for the average input current provided by the delta-sigma modulator thus realizing a linear *current* DAC when mirrored back. The low-pass filter to reconstruct the desired bias voltage is implemented by adding a 2nd-order voltage-mode filter in the local feedback loop of the current mirror. An additional filter on the resulting bias voltage results in a 3-pole transfer function that is described in Fig. 4. The filters are implemented using thick oxide transmission gates for the resistance and metal-metal capacitors. By implementing the current filter in voltage-mode and placing it in the mirror, the size of the capacitors are reduced to 340fF each for a nominal 1MHz cut-off frequency, and fit beneath the 52 μ m x 52 μ m area occupied by the pad.

III. EXPERIMENTAL RESULTS

A. Receiver

As discussed in section II, the concern with parasitic capacitance



at the pad leads to other sources of measurement uncertainty due to variation and noise susceptibility. To counteract these effects in the receiver we employ statistical averaging to combat noise and enable sampler characterization to remove offset via post-processing. Fig. 5 shows the CDF and PDF of a sampled voltage at a given phase step that is used to acquire the mean voltage at a fixed time sample. The voltage distribution is acquired by taking one million samples at each voltage point. From Fig. 5, it can be seen that the accumulated effect of timing noise, dynamic voltage noise, and any dynamic sampler response results in roughly $30\text{mV}_{\text{p-p}}$ voltage noise. Conservatively assuming this voltage noise spans a 3σ range, the effect of the million averages is to reduce the noise σ from 10mV to at best $10\mu\text{V}$ or equivalently to improve the dynamic range from 40dB up to 100dB for a 1V signal depending on the spectral properties of the noise.

Fig. 6 shows the characterized offset for all of the samplers on one chip over the entire input range. The static sampler offset across the chip varies between -370mV and $+320\text{mV}$ and Fig. 6 clearly shows the systematic offset of the sampler topology as the input common mode changes. The large offsets near 300mV inputs are due to the NMOS and PMOS input transistors both being weakly turned on. The offsets at the higher common modes are due to increasing common mode to differential mode current which reduces the time for the sampler to resolve. The inset of Fig. 6 shows the spatial distribution of the largest magnitude sampler offsets across the chip. The distribution of offset magnitudes appears random while the sign of the offsets show a slight increasing gradient from the lower left hand corner to the upper right hand corner. This could be due in part to the location of the analog supply and input reference voltages which originate near the lower left hand corner.

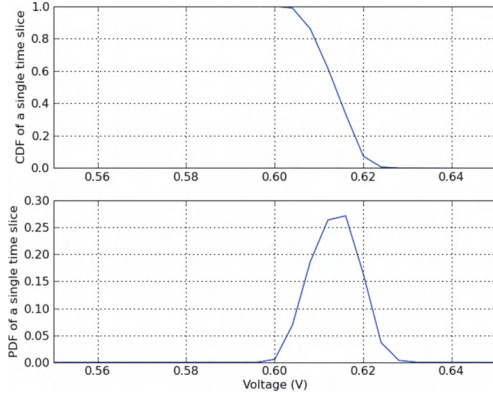


Fig. 5. Measured CDF of a voltage sample in time (top) and its corresponding PDF used to determine mean voltage and sampling noise.

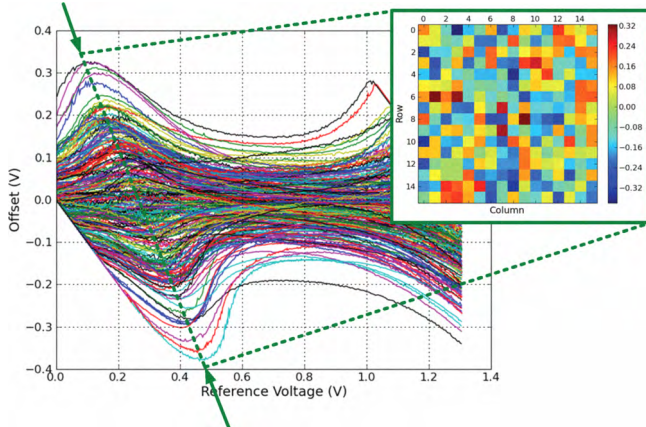


Fig. 6. Measured offset voltage for all 256 samplers on the chip across the entire input range and the corresponding spatial distribution (inset) of the largest magnitude offset for each sampler.

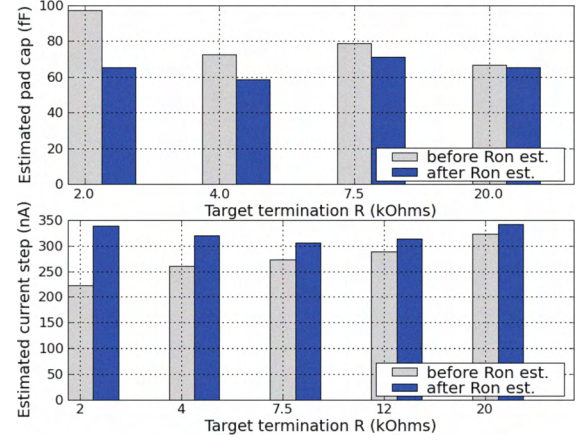


Fig. 7. Estimated pad capacitance calculated before and after estimating the series termination resistance.

B. Transmitter

As shown in Fig. 4, allowing for adjustable termination means that part of the termination impedance is determined by the transistor on-resistance, R_{on} . We need to find this value to reliably interpret measurements and can determine it by assuming that the local variation in the passive component of the termination is small and then fit measured results across several termination settings to determine the transistor contribution to the resistance.

This approach is employed to calculate the actual effective R_{on} of the termination for both step responses and DC inputs so that the circuit parameters we actually want, device resistance and capacitance, can be determined. Uncompensated step responses are captured for several different terminations. Knowing that the capacitance seen at the pad is fixed, the bandwidth of each resulting response is then used to fit the data to find the effective R_{on} , which was found to be $\sim 1\text{k}\Omega$. The result can then be used to estimate the capacitance at the pad ($\sim 65\text{fF}$) as shown in Fig. 7 (top). Similarly, for the DC case, we use the delta-sigma modulator to provide a set of linear current inputs and take voltage samples across this range for different termination values. Knowing that, on average, the current step size is fixed, a similar data fit approach to the previous case can be used to find R_{on} again. Once R_{on} is determined, the actual current step size ($\sim 330\text{nA}$ in this case) can then be calculated as shown in Fig. 7 (bottom). Knowing the current step size then enables the direct measurement of the resistance of a device under test.

For the purpose of calibrating the termination resistance, the current DAC does not need a lot of resolution, just enough linearity to provide sufficient data to extract the slope corresponding to the resistance. For the results shown in Fig. 7, each termination setting is swept through the full range of current inputs for when the DAC is in 6-bit resolution mode. However, the DAC is designed to provide anywhere between 3 and 10 bits of resolution depending on what modulation frequency is used. For DC inputs, the residual error in delta-sigma modulators is maximal at the extreme inputs [4]. To keep the residual error less than 1 LSB, the modulation frequency needed can be described by (1).

$$f_M \geq 2f_C \cdot 2^B \quad (1)$$

Here, f_M is the modulation frequency, f_C is the cutoff frequency of the analog low-pass filter and B is the bits of resolution desired for the DAC. Fig. 8 shows the INL and DNL performance of the delta-sigma current DAC in 6-bit resolution mode with a modulation frequency of 500MHz . The effective number of bits (ENOB) of the DAC is approximately 4.6 for this modulation frequency which

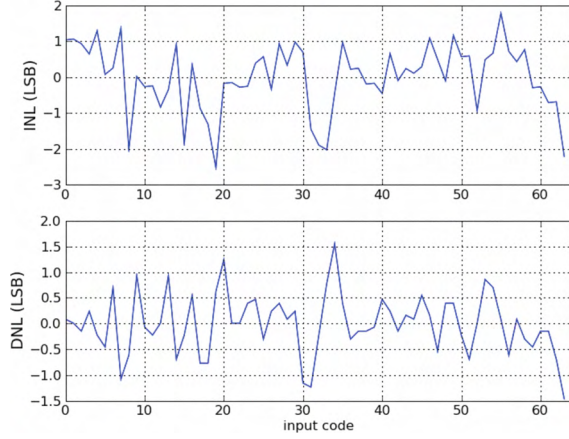


Fig. 8. Measured INL and DNL for the $\Delta\Sigma$ current DAC in 6-bit resolution mode using a modulation frequency of 500MHz. Output INL & DNL include resistor non-linearity and show an ENOB of 4.6 bits.

implies a filter cutoff frequency of 10.3MHz and is reasonable given that the nominal corner frequency of the filter was designed to be about 1MHz. If needed, additional resolution can be achieved by running the modulator at a higher frequency.

C. Pad Parasitic Compensation

The effect of the parasitic compensation on the injected step waveform is captured in Fig. 9. Fig. 9 shows a measured step response at the transmitter for a 7.5k Ω termination both with and without the compensation enabled and also shows the corresponding frequency response for the two steps. This same measurement was repeated for 2, 4, and 20k Ω terminations. The resulting 3dB bandwidths both with and without the compensation consistently indicate that the effective bandwidth of the launched input step waveform is nearly 3X better with the compensation enabled, allowing for simultaneously high impedance and high bandwidth outputs in the presence of a standard wirebond sized pad interface. The effective pad parasitic associated with the pad and the devices can be extracted from these measurements and is calculated to be ~ 22 fF. This falls in line with simulated results predicting 15fF of device and 5fF of residual pad capacitance.

D. Preliminary CNT Measurements

Given the uncertainty in transferring novel devices, another advantage to moving the test system to silicon is that the process of finding connections can be automated. For this measurement, CNT connections were automatically detected by systematically

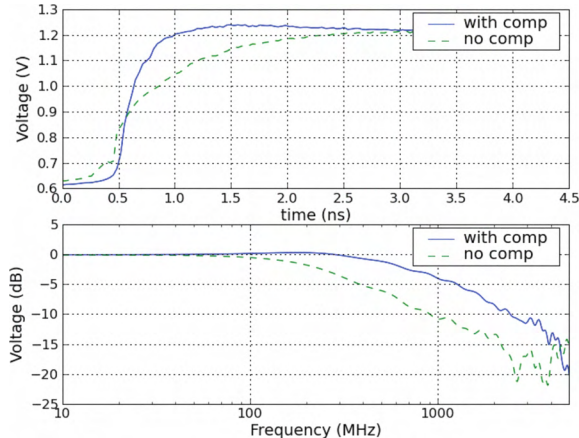


Fig. 9. Step response (top) and corresponding frequency response (bottom) for an empty pad with and without the parasitic cap compensation.

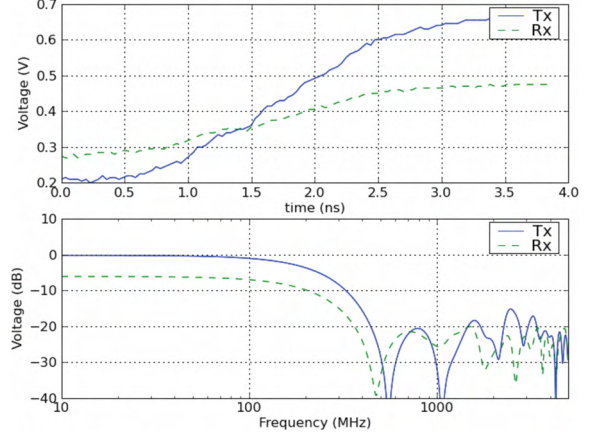


Fig. 10. Measured CNT step response at the transmitter and receiver (top) and the corresponding frequency response (bottom) for each.

transmitting known patterns from one transceiver and polling the other transceivers to see if the pattern was received. Fig. 10 shows a measured step response with a 7.5k Ω termination at both the transmitter and receiver through a sheet of CNTs, each between 30-50 μ m long, spanning a distance greater than 10 μ m between two pads (points A and B in Fig. 1) on top of the test chip. The estimated capacitance seen at the transmitter and receiver are 59fF and 65fF respectively. Most of this capacitance is likely due to the pad capacitance at the receiver. The similar bandwidths between the Tx and Rx waveforms also suggest a relatively low resistance path between the two transceivers.

IV. CONCLUSIONS

A flexible on-chip test infrastructure to address the need to characterize novel devices and materials, many of which are high-impedance, has been presented. In order to enable high frequency characterization at high impedances, care is taken to minimize device parasitics at the interface. To enable this, circuit techniques have been presented to reduce the noise and uncertainty associated with measurement circuits using small device sizes. Also, a pad interface and driver have been shown to enable both large pad interfaces while maintaining good signal bandwidth and novel supporting circuitry and methodologies have been presented to directly extract resistances and capacitances at the pad while maintaining a small area footprint. This full suite of tools enables flexible AC and DC device testing as well as support for de-embedding device measurements.

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REFERENCES

- [1] P.J. Burke, et al., "Nanotube Technology for Microwave Applications," Microwave Symp. Digest, 2005 IEEE MTT-S Intl., pp12-17, June 2005
- [2] K. Soumyanath, et al., "Accurate On-Chip Interconnect Evaluation: A Time-Domain Technique," JSSC, Vol 34, No. 5, pp 623-631, May 1999.
- [3] M. Takamiya, Mizuno, M., "A Sampling Oscilloscope Macro Toward Feedback Physical Design Methodology," Symp. on VLSI Circuits, 2004.
- [4] R.M. Gray, "Spectral Analysis of Quantization Noise in a Single-Loop Sigma-Delta Modulator with dc Input", IEEE Trans. on Comm., June 1989.