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**Citation:** Jungwoo Joh, and J.A. del Alamo. "Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors." *Electron Device Letters*, IEEE 29.4 (2008): 287-289. © 2008 IEEE

**As Published:** <http://dx.doi.org/10.1109/LED.2008.917815>

**Publisher:** Institute of Electrical and Electronics Engineers

**Persistent URL:** <http://hdl.handle.net/1721.1/59403>

**Version:** Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

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# Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors

Jungwoo Joh and Jesús A. del Alamo

**Abstract**—We have found that there is a critical drain-to-gate voltage beyond which GaN high-electron mobility transistors start to degrade in electrical-stress experiments. The critical voltage depends on the detailed voltage biasing of the device during electrical stress. It is higher in the OFF state and high-power state than at  $V_{DS} = 0$ . In addition, as  $|V_{GS}|$  increases, the critical voltage decreases. We have also found that the stress current does not affect the critical voltage although soft degradation at low voltages takes place at high stress currents. All of our findings are consistent with a degradation mechanism based on crystallographic-defect formation due to the inverse piezoelectric effect. Hot-electron-based mechanisms seem to be in contradiction with our experimental results.

**Index Terms**—DC stress, degradation, GaN, high-electron mobility transistor (HEMT), reliability.

## I. INTRODUCTION

ONE OF THE MOST promising devices for RF power amplifier and high-voltage switching applications is the GaN high-electron mobility transistor (HEMT). Due to the extraordinary material properties of GaN, GaN HEMTs have already shown an output power density over 30 W/mm at 8 GHz [1]. Recently, GaN-based HEMTs have also expanded their frequency range. A power density of 2.1 W/mm has been demonstrated in W-band [2]. However, in spite of this impressive performance, a wide-scale deployment of GaN HEMTs has yet to take place. The main impediment is the limited electrical reliability that these devices exhibit.

Although a few studies have been conducted attempting to provide understanding of the physics behind the electrical degradation of GaN HEMTs [3]–[7], detailed failure mechanisms have yet to be identified. The prevailing hypothesis in the literature is hot-electron-induced trap generation [3], [4]. Recently, we have presented experimental evidence that is in contradiction with this hypothesis [7]. We have also proposed a degradation mechanism based on crystallographic-defect formation through the inverse piezoelectric effect [7]. In this letter, we study in detail one of our most significant findings in [7]: the observation of a critical voltage for electrical degradation. We show that the critical voltage depends on the bias configuration

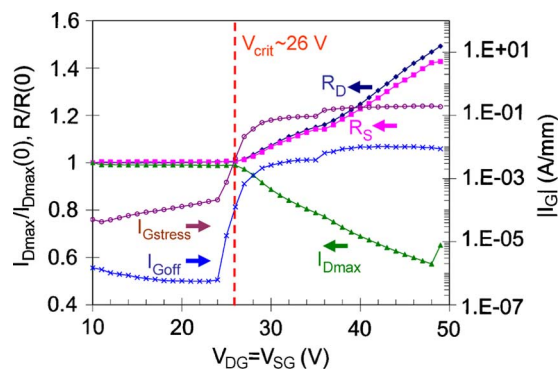


Fig. 1. Change in normalized  $I_{D\max}$ ,  $R_D$ ,  $R_S$ ,  $I_{G\text{stress}}$ , and  $I_{G\text{off}}$  as a function of stress voltage in a step-stress experiment in the  $V_{DS} = 0$  state ( $V_{DG} = 10\text{--}50$  V in 1-V steps).

during stress and on the device geometry in ways that are inconsistent with a hot-electron hypothesis.

## II. EXPERIMENTAL RESULT

The devices that we have studied are millimeter-wave industrial GaN HEMTs of  $L_G = 0.25\ \mu\text{m}$  with a field plate. Both source-to-gate gap and gate-to-drain gap distances were  $2\ \mu\text{m}$ . A typical device shows  $I_{D\max}$  of 1.2 A/mm,  $V_T$  of  $-3$  V, and  $f_T$  of 40 GHz. We have electrically stressed these devices in dc at room temperature and in  $N_2$  under various conditions. During stress, we have measured several device parameters by a benign characterization suite [8].

First, we carried out step-stress experiments in the  $V_{DS} = 0$  state. This condition is interesting in that no current flows through the channel of the device, and both sides of the device can be stressed simultaneously. In a typical experiment,  $V_{GS}$  is stepped from  $-10$  to  $-50$  V in 1-V steps while keeping  $V_{DS} = 0$ . The device is stressed for 1 min in each voltage step. Fig. 1 shows the change in  $I_{D\max}$  (drain current at  $V_{DS} = 5$  V and  $V_{GS} = 2$  V),  $R_S$ ,  $R_D$ , stress gate current, and  $I_{G\text{off}}$  (gate current at  $V_{DS} = 0.1$  V and  $V_{GS} = -5$  V) as the stress experiment proceeds. There is a negligible degradation up to around  $V_{DG} = V_{SG} = 26$  V. At this critical voltage, degradation in all figures of merit starts sharply and increases as the stress experiment proceeds.

Our finding of a critical voltage for electrical degradation is surprising in itself. More surprising is realizing that this critical voltage is quite low since, separately, we have verified that these devices operate normally at 30 V with minor degradation [9]. In order to study this, we have carried out similar experiments under other bias conditions: high-power state and OFF state.

Manuscript received November 12, 2007; revised January 16, 2008. This work was supported by the Army Research Laboratory (ARL) under Contract W911QX-05-C-0087. The review of this letter was arranged by Editor G. Meneghesso.

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Digital Object Identifier 10.1109/LED.2008.917815

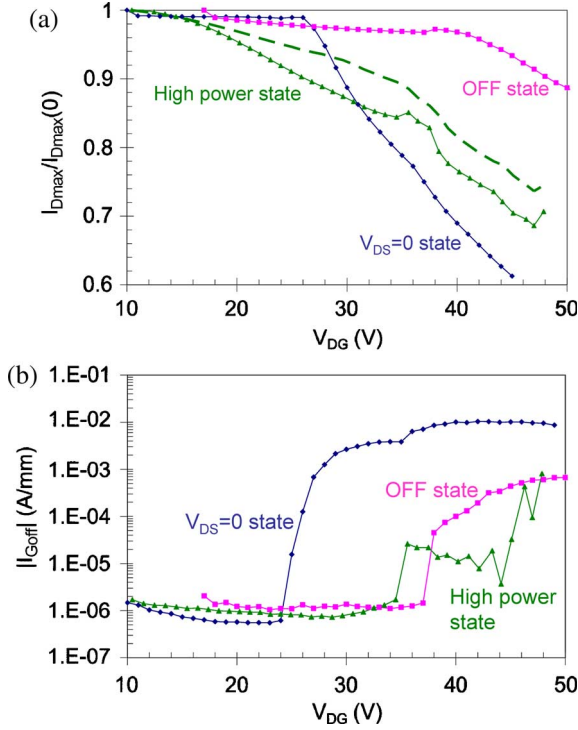


Fig. 2. (a) Change in normalized  $I_{Dmax}$  in step-stress experiments for three different stress conditions. Dashed line represents the estimated change in  $I_{Dmax}$  in the high-power state removing the effect of  $V_T$  change. (b) Change in the gate leakage current  $I_{Gooff}$  (gate current at  $V_{DS} = 0.1$  V and  $V_{GS} = -5$  V) in the same experiment.

Fig. 2(a) shows the  $I_{Dmax}$  degradation in three different step-stress experiments. In the OFF state, the stress bias conditions were  $V_{GS} = -7$  V and  $V_{DS} = 10$ –50 V. In the high-power state, we applied  $V_{DS} = 10$ –50 V with  $I_D = 0.8$  A/mm. For reference, we replot the data for  $V_{DS} = 0$  from Fig. 1. In all these experiments, the devices have been stressed for 1 min in each step, and the voltage step size was 1 V. In all three experiments, we observe again a mirror image behavior in the degradation of  $I_{Dmax}$  and  $R_D$  (not shown).

In the OFF state, we observe a well-defined critical voltage of about 38 V. In the high-power state, we observe a gentle degradation at low  $V_{DS}$  followed by an increase in the slope of degradation at around 35 V. The low-level degradation in  $I_{Dmax}$  at low  $V_{DG}$  in the high-power state is partly due to a significant positive shift of threshold voltage (about +0.5 V for the entire experiment). The  $I_{Dmax}$  change that would have taken place if there had been no  $V_T$  change is shown through the dashed line in Fig. 2(a). As it can be seen, for  $V_{DG} > 30$  V, the overall degradation in the high-power state is lower than in the  $V_{DS} = 0$  state in spite of the high current. This is inconsistent with a hot-electron hypothesis [3], [4].

Fig. 2(b) shows the time evolution of  $I_{Gooff}$  for these experiments. In all cases,  $I_{Gooff}$  exhibits a sharp rise at around the same critical voltage of Figs. 1 and 2(a), which implies that the  $I_D$  and  $I_G$  degradations have the same origin [10]. This behavior in  $I_G$  again confirms that the critical voltages in the high-power state and in the OFF state are about 10 and 15 V higher, respectively, than that in the  $V_{DS} = 0$  state.

In principle, this difference in critical voltage could result from different values of  $V_{GS}$  or different levels of stress current.

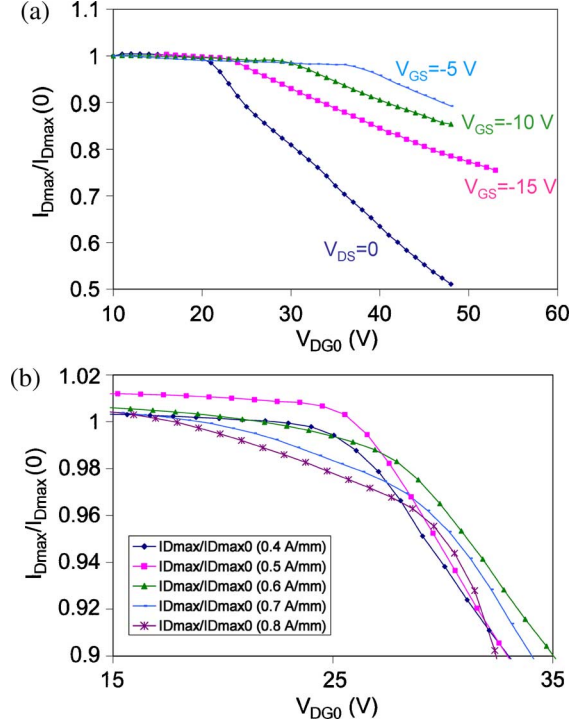


Fig. 3. Change in  $I_{Dmax}$  in two different sets of step-stress experiments. (a) Impact of  $V_{GS}$  on the critical voltage  $V_{DGcrit}$ .  $V_{GS} = -5$ ,  $-10$ , and  $-15$  V were investigated. For the  $V_{DS} = 0$  state,  $V_{GS} = -V_{DG}$ .  $V_{DGcrit}$  increases as  $|V_{GS}|$  decreases. (b) Impact of stress current (0.4–0.8 A/mm). No clear impact of the stress current is observed.

We have studied both possibilities. We investigated the impact of  $V_{GS}$  by step stressing  $V_{DS}$  with  $V_{GS}$  fixed at different values. The results are shown in Fig. 3(a) with the data for the  $V_{DS} = 0$  state as reference (in this case,  $V_{GS} = -V_{DG}$ ). As one can see,  $V_{DGcrit}$  increases as  $|V_{GS}|$  decreases. This change in  $V_{DGcrit}$  does not come from a change in current. For  $V_{GS} = -10$  and  $-15$  V, the stress current was less than 1 mA/mm up to  $V_{DGcrit}$ . Even for  $V_{GS} = -5$  V, the stress current was 115 mA/mm at  $V_{DGcrit}$ . Further confirmation of the relatively unimportant role of current comes from the step-stress experiments with current as a parameter. In Fig. 3(b), we can see that the stress current has a little impact on  $V_{DGcrit}$  except for a softening of the corner at high current, just as in the high-power state.

The results that we show in this letter have been observed with great reproducibility in many different devices fabricated through different processes on different heterostructures.

### III. DISCUSSION

In [7], we proposed a degradation mechanism for GaN HEMT that is based on crystallographic-defect formation through the inverse piezoelectric effect due to high vertical electric field at the drain edge of the gate. In this hypothesis, the mechanical strain produced by this electric field adds on top of the tensile strain due to lattice mismatch between AlGaIn barrier and GaN layer and increases the elastic energy in the AlGaIn barrier. If this elastic energy exceeds a critical value, crystallographic defects are formed which become trapping sites for electrons. The elastic energy in the AlGaIn barrier layer is proportional to strain squared, and strain is linearly

proportional to the vertical electric field which is a function of voltage. The existence of a critical voltage for electrical degradation is consistent with the notion that lattice damage does not occur until the elastic energy reaches its critical value [11].

A higher  $V_{\text{DGcrit}}$  in the OFF state and in the high-power state when compared with the  $V_{\text{DS}} = 0$  state as well as the  $V_{\text{GS}}$  dependence of  $V_{\text{DGcrit}}$  can be explained by the impact of strain field produced from the source side of the device. As  $V_{\text{SG}}$  increases, the strain field at the source side of the gate edge increases, and the total elastic-energy density under the gate increases, resulting in lower  $V_{\text{DGcrit}}$ .

This hypothesis also explains the gate-length dependence of  $V_{\text{DGcrit}}$  in the  $V_{\text{DS}} = 0$  state that we reported in [7]. There, we found that  $V_{\text{DGcrit}}$  decreases as  $L_G$  decreases with stress in the  $V_{\text{DS}} = 0$  state. This result is also inconsistent with a hot-electron-related hypothesis [3], [4] in that to the first order, the electrostatics in the extrinsic portion of the device must be the same regardless of the value of  $L_G$  if the gate-drain gap length does not change, as is the case in these devices. Therefore, at a given bias point, the hot-electron production should be about the same in all these devices. In contrast with this, we have not seen any clear dependence of degradation on  $L_G$  in the OFF state and the high-power state. In our hypothesis, in the  $V_{\text{DS}} = 0$  state, longer gate-length devices bring the two high-field points at both ends of the gate further apart, presumably resulting in an overall lower strain in the AlGaIn layer under the gate. In the OFF state or in the high-power state, the gate length should have less impact on the critical voltage as the mechanical stress from the source side is smaller. Along with these results, the small impact of current on  $V_{\text{DGcrit}}$  that we observe confirms that the role of hot electrons is minor since hot-electron effects should depend on current and  $V_{\text{DG}}$ .

On top of the strain-related mechanism, some other degradation mechanism seems to be involved for high currents for which we observe a soft degradation below the critical voltage [Fig. 3(b)]. This may be due to an increased channel temperature or some hot-electron effect. In fact, we also observe that in the high-power state, the source resistance degrades to some extent. This needs to be investigated further in the future.

#### IV. CONCLUSION

We have found a critical voltage for electrical degradation beyond which a GaN HEMT starts to degrade abruptly. We have found that  $V_{\text{DGcrit}}$  is higher in the OFF state and the high-power state than in the  $V_{\text{DS}} = 0$  state. This is due to the fact that high  $V_{\text{SG}}$  decreases  $V_{\text{DGcrit}}$ . We have also found

that the stress current does not change  $V_{\text{DGcrit}}$ . These results are consistent with earlier observations of higher  $V_{\text{DGcrit}}$  in longer devices in the  $V_{\text{DS}} = 0$  condition, but being gate length independent in the other bias conditions. Our experimental results are consistent with a defect formation mechanism due to the inverse piezoelectric effect [7].

#### ACKNOWLEDGMENT

This research took place at the Microsystems Technology Laboratories, MIT. The authors would like to thank TriQuint Semiconductor and BAE Systems for their collaborative efforts.

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