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# Scalability of sub-100 nm thin-channel InAs PHEMTs

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## ABSTRACT

We have experimentally investigated the role of thinning down the channel thickness and using high InAs composition as a channel material, which aims to improve the electrostatic integrity of the device as well as high frequency characteristics of the device. To do so, we have fabricated InAs PHEMTs with  $t_{ch} = 10$  nm, together with reference  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs with  $t_{ch} = 13$  nm. In comparison with reference  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  ones, InAs PHEMTs with  $t_{ch} = 10$  nm exhibit excellent electrostatic integrity of the device down to  $L_g = 30$  nm regime, such as subthreshold swing ( $S = 75$  mV/dec), DIBL = 84 mV/V and  $g_{m,max} = 1.9$  mS/mm at  $V_{DS} = 0.5$  V. Besides, InAs PHEMTs with  $L_g = 30$  nm show outstanding  $f_r = 600$  GHz and  $f_{max} = 490$  GHz at  $V_{DS} = 0.5$  V. More importantly, InAs PHEMTs exhibit a far better scaling behaviors, down to  $L_g = 30$  nm regimes. Indeed, InAs is a promising choice of the channel material for future THz and logic applications.

## Introduction

InP-based High-Electron-Mobility-Transistors (HEMTs) have shown outstanding promise for future Tera-Hz (THz) electronics as well as post-Si CMOS logic applications. This is mainly as a result of the excellent carrier transport properties of high-InAs composition InGaAs which is used as channel material [1-3]. In FETs, the path for high-frequency and high-speed performance is gate-length ( $L_g$ ) scaling. However, this requires harmonious scaling of all device dimensions. Without this, in the sub-100 nm regime, gate length scaling alone often results in at best modest performance improvements [4]. In particular, maintaining electrostatic integrity in the sub-100 nm regime requires the use of a very thin channel, together with a thin barrier. Thin channels suffer from enhanced carrier scattering and result in decreased performance. We have recently been investigating the combination of a very thin channel with enhanced InAs composition as a way to remedy this problem. Our results have shown outstanding high frequency performance as well as logic operation that compares favorably to that of Si in the 30 nm gate length range [5-6].

In order to understand in detail advantages of this device design, in this work, we report on sub-100 nm

InAs PHEMTs and reference  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs that have been fabricated simultaneously following an identical process. This study reveals the relative roles of channel composition and channel thickness in device performance.

## Process Technology

**Fig. 1** shows a cross-sectional view of the devices fabricated in this work. Our devices are built in an InP substrate. The heterostructures and the device fabrication process have been reported before [5-6]. The only difference in both families of devices is the channel design. The InAs PHEMTs feature a 10 nm thick channel containing a 5 nm pure InAs layer inside, whereas  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs features a 13 nm thick channel containing an 8 nm  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  layer. In Hall epi wafers but using a simpler 10 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  cap with  $1 \times 10^{18}$  /cm<sup>3</sup>, the Hall mobility ( $\mu_{n,Hall}$ ) of InAs PHEMTs was 13,200 cm<sup>2</sup>/V-s, which is about 20% better than that of reference  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs.

The fabricated devices here bring together novel design features to reduce parasitic capacitance and resistance, to improve short-channel effects, to speed up electron transport. Among them, a three-step gate recess process was used to scale down the  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$

barrier layer to  $t_{\text{ins}} = \sim 4$  nm. A Ti/Pt/Au metal stack was utilized in a T-gate with a stem height of about 150 nm. The side-recess spacing ( $L_{\text{side}}$ ) was about 80 nm. We have made devices with  $L_g$  in the range of 30 nm to 130 nm.

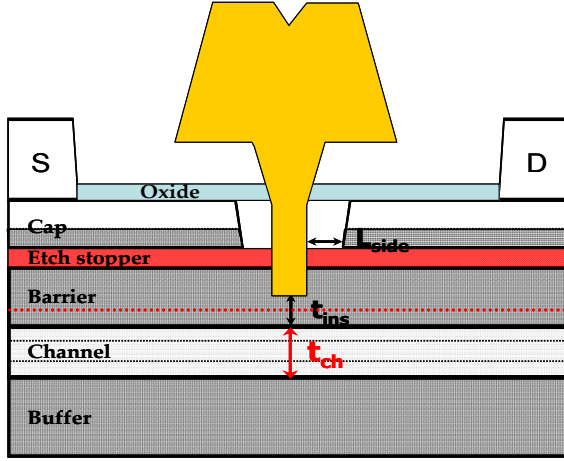


Fig. 1 Schematic of InAs and  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs.

## Results & Discussions

Fig. 2 (a) and (b) show output characteristics of both classes of devices for various  $L_g$ . InAs PHEMTs exhibit better current driving capability than  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  ones. In addition, as  $L_g$  decreases, InAs devices show better ID scalability than  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  ones. A trade-off with InAs subchannel is an increased output conductance ( $g_o$ ) or kink effect. These are related with the used InAs subchannel with narrow bandgap ( $E_g$ ), which presumably induces more impact-ionization rate in the channel [7]. As shown below, however, this does not result in degraded RF gain characteristics for InAs PHEMTs.

Fig. 3 shows subthreshold and gate leakage current ( $I_G$ ) characteristics of both families of devices with  $L_g = 30$  nm at  $V_{\text{DS}} = 0.05$  and 0.5 V. The benefits of thinning down the channel are now evident. The InAs PHEMTs exhibit better subthreshold swing (75 mV/dec) and DIBL (84 mV/V) than the InGaAs devices ( $S = 95$  mV/dec and DIBL = 120 mV/V). It is also to be noted that in both types of devices the off-state current ( $I_{\text{OFF}}$ ) is dominated by Schottky gate current, not by band-to-band-tunneling (BTBT). The lack of significant BTBT in InAs PHEMTs might be due to electron quantization in the thin channel.

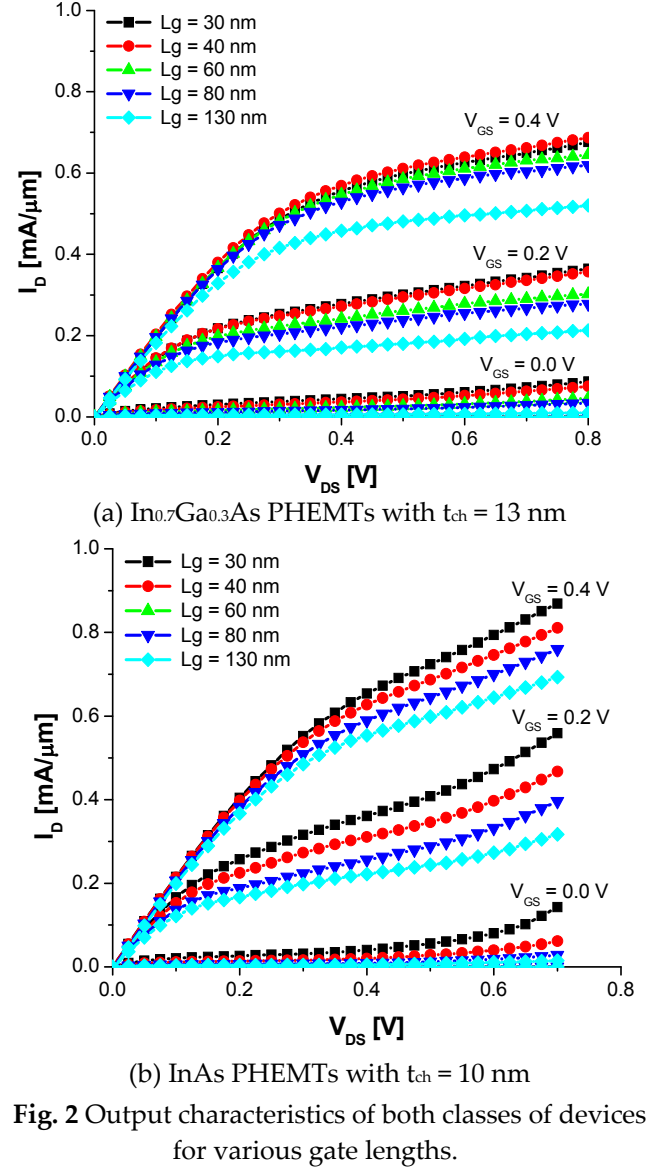


Fig. 2 Output characteristics of both classes of devices for various gate lengths.

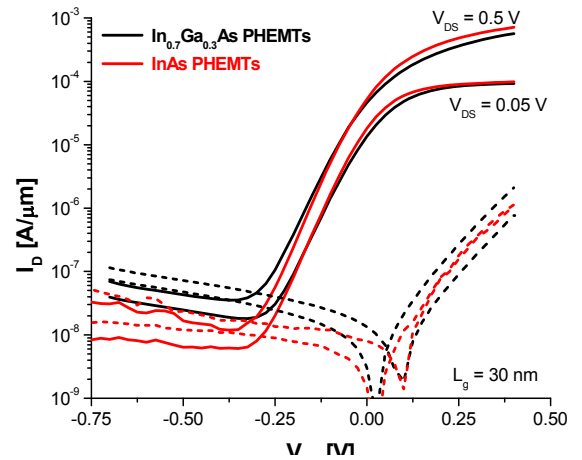
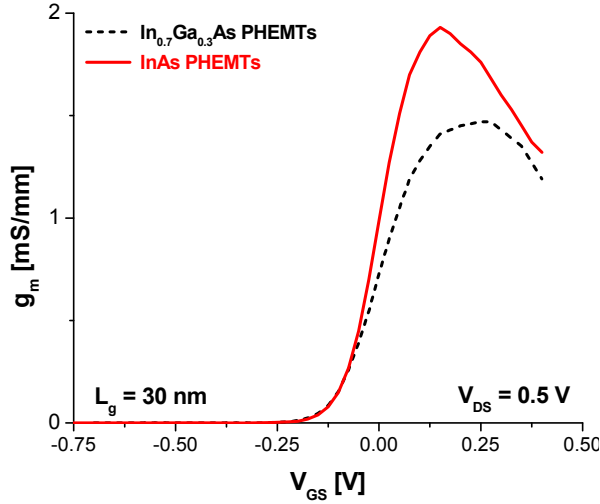
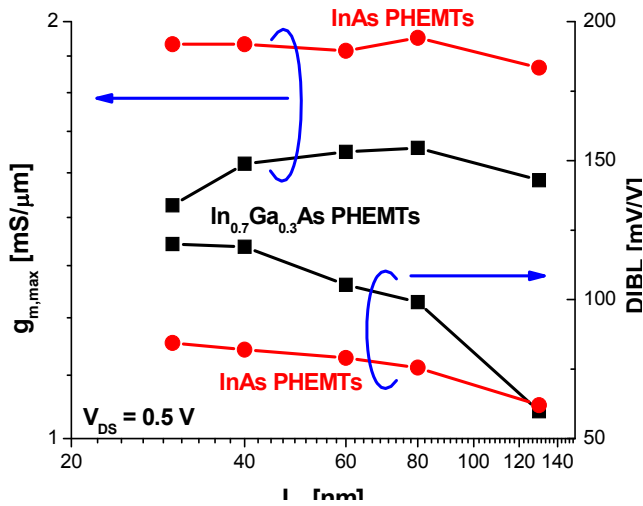


Fig. 3 Subthreshold and  $I_G$  characteristics of  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs and InAs PHEMTs with  $L_g = 30$  nm.

Improvements in the carrier transport properties can be more clearly observed in the transconductance ( $g_m$ ) characteristics. **Fig. 4** shows the measured  $g_m$  as a function of  $V_{GS}$  for both types of 30 nm devices at  $V_{DS} = 0.5$  V. We can see how InAs PHEMTs outperform against  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  ones, especially in the sense of much higher peak  $g_m$ . **Fig. 5** shows the scaling behavior of  $g_{m\_max}$  (on the left axis) and DIBL (on the right axis) as a function of  $L_g$ , at  $V_{DS} = 0.5$  V. The InAs PHEMTs exhibit much higher values of  $g_{m\_max}$  and, more importantly, better  $g_{m\_max}$  scalability than InGaAs PHEMTs. In fact, the InAs devices show outstanding  $g_{m\_max}$  of 1.9 mS/ $\mu\text{m}$ , at  $V_{DS} = 0.5$  V. At the same time, the InAs devices show much better DIBL scalability down to  $L_g = 30$  nm.

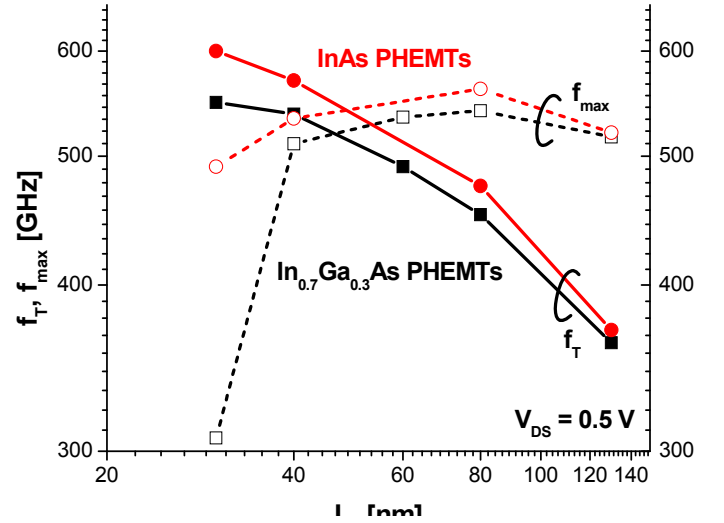


**Fig. 4**  $g_m$  characteristics of 30 nm  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  and InAs PHEMTs at  $V_{DS} = 0.5$  V.

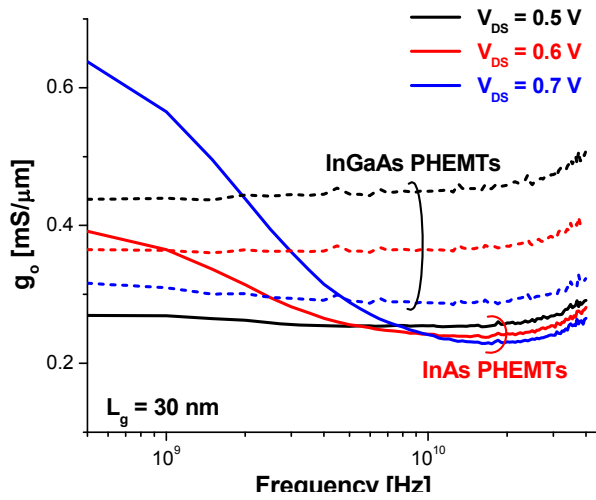


**Fig. 5**  $g_{m\_max}$  and DIBL as a function of  $L_g$ .

Microwave performance was characterized from 0.5 to 40 GHz using an HP 8510C network analyzer with an LRM calibration standard. **Fig. 6** shows the extracted cut-off frequency ( $f_T$ ) and maximum oscillation frequency ( $f_{max}$ ) as a function of  $L_g$  for both families of devices. Here, we used on-wafer open/short de-embedding method to subtract pad capacitances and inductances. Similar to DC characteristics above, InAs PHEMTs exhibit not only higher values of  $f_T$  and  $f_{max}$ , but also much better  $f_T$  and  $f_{max}$  scalability down to  $L_g = 30$  nm. In particular, 30 nm InAs devices show an excellent  $f_T$  of above 600 GHz at  $V_{DS} = 0.5$  V. Looking at  $f_{max}$  characteristics in both families of devices, we find an interesting contradiction of the higher  $f_{max}$  of the InAs devices even with their worse DC output conductance ( $g_o$ ) caused by the kink effect. In trying to understand this behavior, **Fig. 7** plots small-signal extracted  $g_o$  against frequency for both devices with  $L_g = 30$  nm for different values of  $V_{DS}$ . InAs devices exhibit more frequency dispersion in  $g_o$  in the lower frequency range as a consequence of the kink effect. However, as the frequency increases beyond the key time constant for the kink effect [8], InAs devices eventually show lower values of  $g_o$  than InGaAs ones. This improvement in  $g_o$  arises from the use of a thin channel, and eventually results in an improved  $f_{max}$  for the InAs devices.



**Fig. 6**  $f_T$  and  $f_{max}$  scaling behavior for both families of devices. The bias point is the one corresponding to peak  $f_T$  at  $V_{DS} = 0.5$  V



**Fig. 7** Small-signal modeled output conductance ( $g_o$ ) as a function of frequency for both families of devices with  $L_g = 30$  nm (The gate bias is the one corresponding to peak  $f_T$ ).

## Conclusions

In summary, we have experimentally identified the benefit of thin channel and high InAs composition, aiming to improve the electrostatic integrity of the device as well as carrier transport properties. In comparison with reference  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  PHEMTs with  $t_{ch} = 13$  nm, InAs PHEMTs with  $t_{ch} = 10$  nm exhibit excellent electrostatic integrity of the device, such as better subthreshold swing, DIBL and  $g_m$  scalability down to 30 nm  $L_g$  regime. Besides, InAs PHEMTs with  $L_g = 30$  nm show outstanding  $g_{m\_max} = 1.9$  S/mm,  $f_T = 600$  GHz and  $f_{max} = 490$  GHz at  $V_{DS} = 0.5$  V. Indeed, InAs is a promising choice of the channel material for future THz and logic applications.

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