

## MIT Open Access Articles

*High-speed graphene interconnects monolithically integrated with CMOS ring oscillators operating at 1.3GHz*

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

**Citation:** Xiangyu Chen et al. "High-speed Graphene Interconnects Monolithically Integrated with CMOS Ring Oscillators Operating at 1.3GHz." IEEE, 2009. 1–4. © Copyright 2009 IEEE

**As Published:** <http://dx.doi.org/10.1109/IEDM.2009.5424293>

**Publisher:** Institute of Electrical and Electronics Engineers (IEEE)

**Persistent URL:** <http://hdl.handle.net/1721.1/71870>

**Version:** Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

**Terms of Use:** Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.



# High-Speed Graphene Interconnects Monolithically Integrated with CMOS Ring Oscillators Operating at 1.3GHz

<sup>1</sup>Xiangyu Chen, <sup>2</sup>Kyeong-Jae Lee, <sup>1</sup>Deji Akinwande, <sup>1\*</sup>Gael F. Close, <sup>3</sup>Shinichi Yasuda,  
<sup>4</sup>Bipul Paul, <sup>3</sup>Shinobu Fujita, <sup>2</sup>Jing Kong, <sup>1</sup>H.-S. Philip Wong

<sup>1</sup>Center for Integrated Systems, Stanford University, Stanford, CA94305, USA E-mail:xiangyuc@stanford.edu

<sup>2</sup>Dept. of Electrical Engineering and Computer Science, MIT, Cambridge, MA 02139, USA

<sup>3</sup>Advanced LSI Technology Laboratory, Toshiba Corporation, Kawasaki, Japan;

<sup>4</sup>Toshiba America Research, San Jose, CA, USA

## Abstract

We have successfully experimentally integrated graphene interconnects with commercial 0.25 $\mu$ m technology CMOS ring oscillator circuit using conventional fabrication techniques, and demonstrated high speed on-chip graphene interconnects that operates above 1GHz.

## Introduction

Graphene has been considered as one of the most promising materials for future interconnects technology [1]. Theoretical studies have shown that graphene has lower resistivity, higher maximum current density, and lower capacitance compared to copper in nanoscale dimensions [2]. Graphene also potentially offers advantages such as simpler fabrication processes and better material control and reproducibility, compared with multi-walled carbon nanotubes (MWCNT). Despite the exciting theoretical predictions and measurements performed at DC [2,3], experimental demonstration of high speed signaling in graphene interconnects has not been made. There is no report yet on the integration of graphene with CMOS technology either. This paper presents **1) the first monolithic integration of graphene with commercial CMOS technology, and 2) the first experimental demonstration of high-speed signaling of on-chip graphene interconnects.** Characterization results showed operation frequency up to 1.3 GHz.

## Device Fabrication

### (1) Graphene synthesis and transfer

Large area graphene films are grown by chemical vapor deposition (CVD), and then transferred to a 5mm $\times$ 5mm CMOS chip following the procedure developed by Reina et al. [4]. The graphene synthesis and transfer is described below in brief. A 500nm Ni film is evaporated on a SiO<sub>2</sub>/Si substrate and thermally annealed. The growth is carried out for 5 minutes at 1000°C, with 5 sccm and 1300 sccm flow of CH<sub>4</sub> and H<sub>2</sub>, respectively. After the growth process, poly(methyl methacrylate) (PMMA) is spin-coated on the graphene/Ni film. The substrate is subsequently placed in a 10% HCl aqueous solution, which etches away the underlying Ni film and releases the graphene film. Once the PMMA/graphene film is placed on the target substrate, the PMMA layer is removed by acetone [4]. The described process flow of material synthesis and transfer is shown in Fig. 1. An average sheet resistance of  $\sim$ 700ohms/sq was extracted for graphene before post-transfer process by transferring graphene films onto SiO<sub>2</sub>/Si test substrates.

### (2) Integration with CMOS circuit

The CMOS chip was fabricated using a 0.25 $\mu$ m CMOS technology. Each of the arrays of 256 ring oscillators was designed with a missing interconnect wire onto which a graphene interconnect wire was subsequently integrated. Fig. 2 illustrates the process flow for post-transfer processing. The

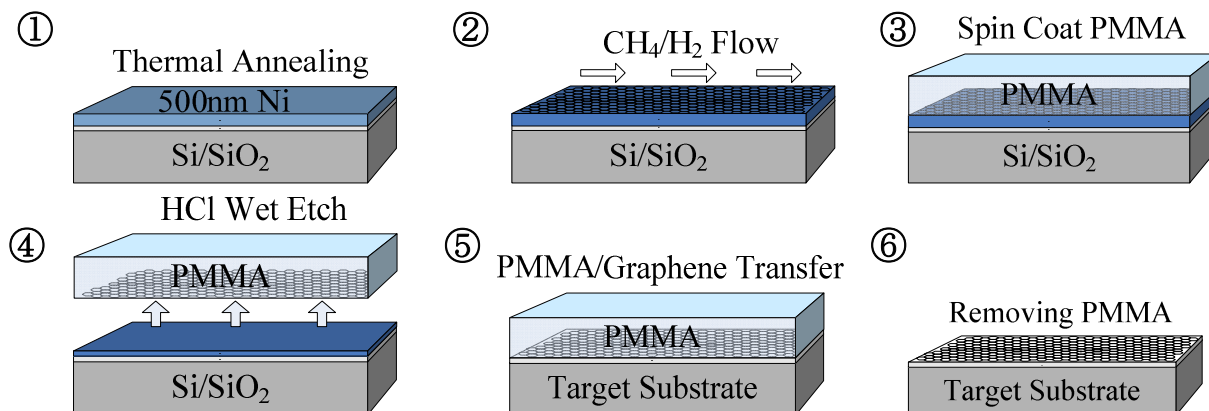


Fig.1 Process flow for graphene CVD growth and transfer to target substrate.

\*: Gael F. Close was with Stanford University. He is now affiliated with IBM Research, Zurich Research Laboratory, Switzerland.

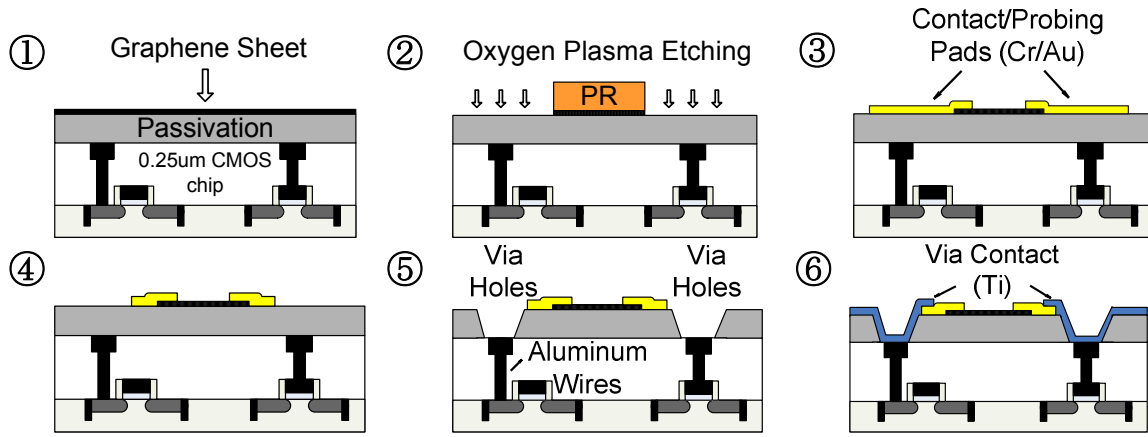


Fig.2 Process flow for post-transfer processing to integrate graphene interconnects with underlying CMOS ring oscillator circuit.

graphene sheet is first patterned into stripes using optical lithography and oxygen plasma dry etching. Gold electrodes are then deposited as contacts. Then via holes are formed by etching through the CMOS passivation layer, reaching down to the topmost aluminum metal layer (M3) of the chip. Finally via contacts are formed by filling the via holes with 100nm of titanium (Fig.3). MWCNT interconnects are integrated in a similar approach [5] for comparison.

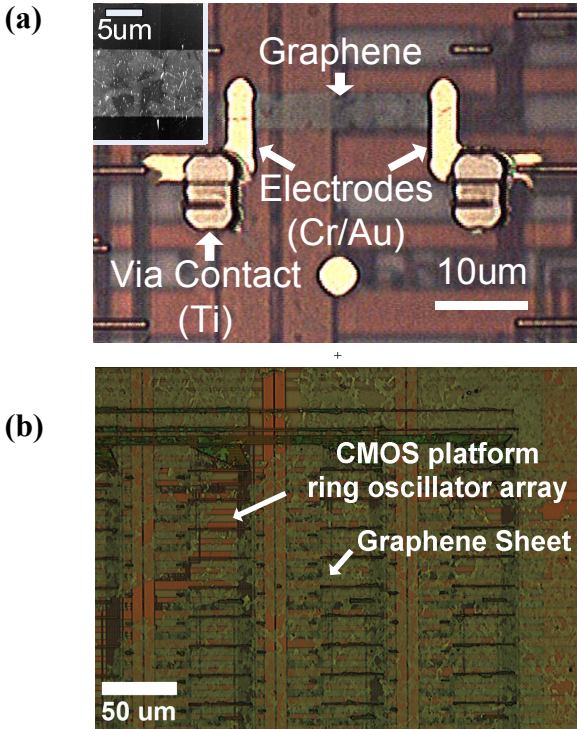


Fig.3 Optical images of graphene on top of CMOS chip. (a) Graphene film after being transferred onto a CMOS chip. (b) One fabricated graphene interconnect on top of CMOS ring oscillator array. The lines that appear black in the middle of Ti via contacts are M3 Al lines . Inset: AFM image of graphene stripe on SiO<sub>2</sub>/Si test substrate.

## Electrical Testing

The oscillator circuit on chip was implemented as a 5-stage ring oscillator with 4 inverters and one differential amplifier [6] at the receiving end of the interconnect line, as shown in Fig.4c.

### (1) DC characterization

The statistics of DC resistivity in Fig. 5(a) shows that the average sheet resistivity remains about 700Ω/sq after post-transfer processing, indicating that the quality of the

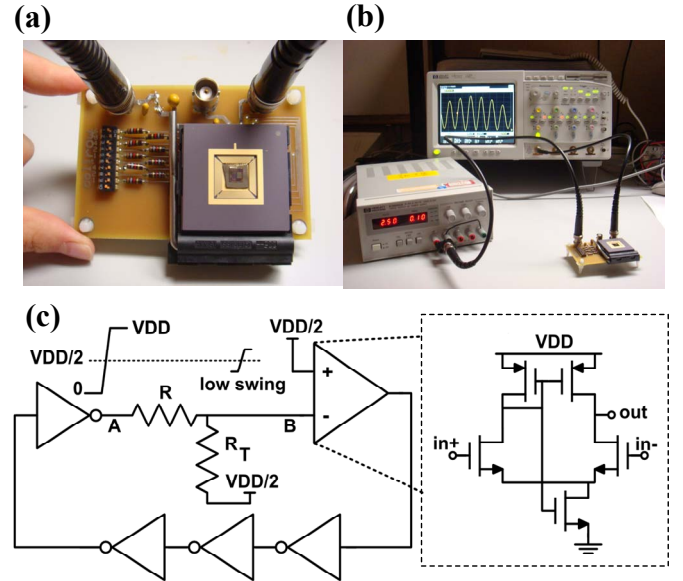


Fig.4 (a) Printed circuit board for RF characterization; (b) RF measurement setup; (c) Schematic of ring oscillator circuit implemented on the chip. The differential amplifier at the receiver end offers a higher sensitivity compared to an inverter. It allowed us to trade off a reduction in the signal swing for a commensurate speed improvement. The line is terminated by a termination resistor ( $R_T=20k\Omega$ ) to a mid supply voltage, hence the signal swing at the receiver end (node B) is reduced to  $V_{DD} \times R / R_T$  while the speed is increased by a factor  $R/R_T$ .

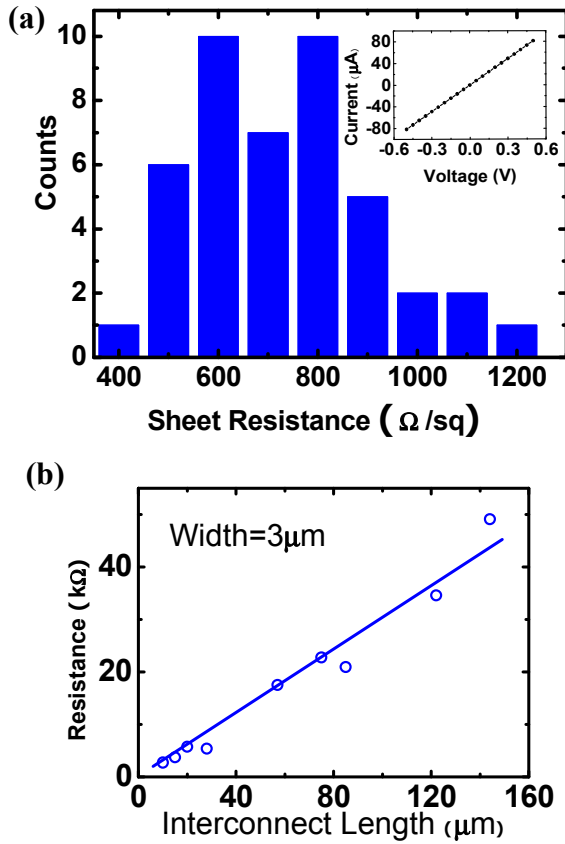


Fig.5 (a) Sheet resistance distribution for graphene interconnects. Average sheet resistance is  $R_s \sim 711 \Omega/\text{sq}$ . The wide distribution was due to variation in the number of layers and surface defects. Inset: I-V curve of a graphene interconnect showing an Ohmic contact ( $L/W=28\mu\text{m}/3\mu\text{m}$ ,  $R=6.15\text{k}\Omega$ ); (b) Interconnect resistance as a function of length, indicating diffusive transport.

graphene film is preserved after transfer and post processing. Sheet resistances data of graphene prepared by a variety of

synthesis techniques are extracted from previous literature, and compared in Table 1. We can see that a few to several layers of graphene is generally more favorable for obtaining low sheet resistance for high-speed interconnects. Contact resistance extracted from Fig. 5b was negligible compared to interconnect resistance. Along with the linear I-V curves shown in Fig. 5b, it is clear to see that we have obtained near-ideal ohmic contacts, a key requirement for interconnect technology. The distribution of resistivity is probably due to material nonuniformity.

#### (2) RF characterization

Oscillation frequency  $f$  of the ring oscillator circuit is determined by RC delay expressed by Eq. (1). If capacitance associated with graphene,  $C_g$  dominates the total capacitance  $C_{\text{tot}}$ ,  $f$  is then expressed by Eq. (2):

$$f \propto \frac{1}{RC} \propto \frac{W}{L \cdot C} \quad (1) \quad f \propto \frac{1}{RC} \propto \frac{1}{L^2} \quad (2)$$

where  $L$  is the interconnect length, and  $W$  is the width. Experimental results (Fig.6) show that frequency is directly correlated with  $W$ , and inversely correlated with  $L/W$  ratio as it is in Eq.(1), which means  $C_{\text{tot}}$  is not dominated by  $C_g$ .

Comparison of RF performances between graphene and MWCNT is shown in Fig.7. For the same ring oscillator circuit design, graphene interconnects have lower resistance and thus offered a higher oscillation frequency. However at the same resistance value, MWCNT tends to have better performance. This is probably due to the larger capacitance associated with wide graphene stripes. Therefore narrower, multi-layered graphene with smaller RC delay should be more desirable for RF applications. Currently, RF performance of MWCNT is mainly limited by the difficulty in achieving Ohmic contacts to all the shells for maximum conductance.

Table 1: Comparison of the room temperature sheet resistance of graphene synthesized from different techniques, demonstrating that a few to several layers of graphene is more attractive for obtaining low sheet resistance for high-speed interconnects.

$R_{\text{sheet}}$ (KΩ/sq)	# of layers	Synthesis	Reference
~0.28	~6-10	CVD growth on Ni	[7]K. S. Kim et. al., <i>Nature</i> , 457, 2009
~1.6	~1-2 layers	Epitaxial growth on SiC	[8]Y. Q. Wu et. al., <i>Appl. Phys. Letters</i> , 92, 2008
~10	~1 layer	Exfoliation	[9]X. Li et. al., <i>Nature Nanotech.</i> , 3, 2008
~1.8	~10.1nm*	Graphene oxide reduction	[10]X. Wang et. al., <i>Nanoletters</i> , 8, 2008
~0.7	~10nm*	CVD growth on Ni	*this work

\*The film thickness is reported in lieu of the number of layers

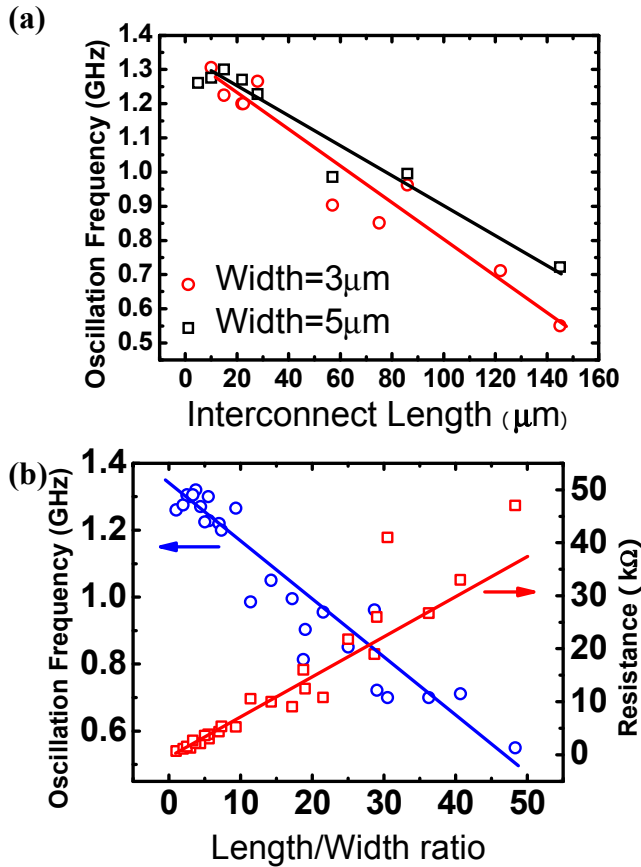


Fig.6 (a) Oscillation frequency for various interconnect lengths and widths. GHz range operation frequency is observed for interconnects up to ~80μm long; (b) Oscillation frequency and resistance as functions of L/W ratio indicative of the # of squares. Symbols are experimental data, bold lines are a visual guides.

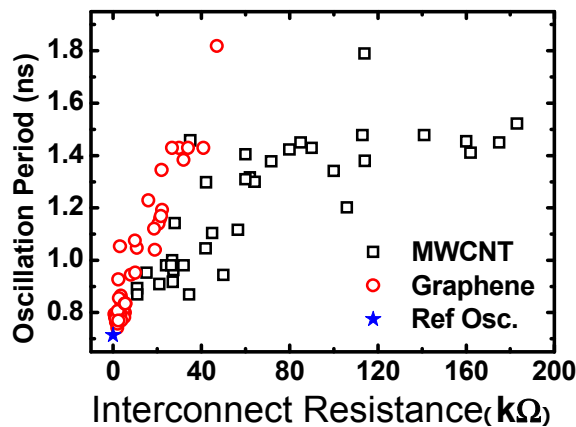


Fig.7 Oscillation period as a function of interconnect resistance for CMOS reference interconnect (aluminum), MWCNT, and graphene. For the same ring oscillator circuit, graphene offers higher speed operation compared to MWCNT. However, at the same resistance value MWCNT interconnects are faster most likely due to their smaller capacitance.

## Conclusions

The demonstration of monolithic integration of graphene with CMOS using conventional fabrication processes represents an important step forward for potential VLSI application of graphene for nanoelectronics that is scalable to any CMOS technology and arbitrary wafer sizes. Additionally, the observation of GHz operation in graphene stripes with length as long as 80μm indicates the promising future of graphene for local and semi-global high-speed interconnects.

## Acknowledgements

X. Chen, G. F. Close, K.J. Lee, J Kong, and H.-S. P. Wong, acknowledge the support of Interconnect Focus Center, one of the Semiconductor Research Corporation/DARPA Focus Centers. This work was also supported in part by the Toshiba Corporation. Part of the work of this paper was performed at the Stanford Nanofabrication Facility. The work of D. Akinwande was supported by the Stanford DARE fellowship, the Ford Foundation and Alfred P. Sloan Foundation graduate fellowships.

## Reference

- [1] A. Naeemi, J.D. Meindl., "Performance Benchmarking for Graphene Nanoribbon, Carbon Nanotube, and Cu Interconnects", *IITC 2008*, pp. 183-185.
- [2] A. Naeemi, J.D. Meindl, "Conductance Modeling for Graphene Nanoribbon Interconnects", *IEEE EDL*, Vol. 28, Issue 5, 428-431, 2007.
- [3] R.Murali, K. Brenner, Y. Yang, T. Beck, J. D. Meindl, "Reisistivity of Graphene Nanoribbon Interconnects", *IEEE EDL*, Vol. 30, Issue 6, pp. 611-613, 2009.
- [4] A.Reina et.al, "Large Area Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition", *Nano Letters*, Vol. 9, No. 1, pp. 31-35, 2009.
- [5] G. Close et.al, "A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors", *Nano Letters*, Vol. 8, No. 2, 706-709, 2008.
- [6] B. Chappell et al., "Fast CMOS ECL Receivers With 100-mV Worst-Case Sensitivity", *IEEE J. Solid-State Circuits*, Vol. 23, Issue 1, pp. 59-67, 1988.
- [7] K. S. Kim et. al., "Large-scale pattern growth of graphene films for stretchable transparent electrodes", *Nature*, Vol. 457, pp. 706-710, 2009.
- [8] Y. Q. Wu et. al., "Top-gated graphene field-effect-transistors formed by decomposition of SiC", *Appl. Phys. Letters*, Vol. 92, p. 092192, 2008.
- [9] X. Li et. al., "Highly conducting graphene sheets and langmuir-Blodgett films", *Nature Nanotech.*, Vol. 3, pp. 538-542, 2008.
- [10] X. Wang, L. Zhi, K. Kullen, "Transparent Conductive Graphene Electrodes for Dye-Sensitized Solar Cells", *Nano Letters*, Vol. 8, No.1, pp. 323-327, 2008.