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Evolution of structural defects associated with electrical degradation in AlGaN/GaN high electron mobility transistors

Prashanth Makaram,[1,2] Jungwoo Joh,[2] Jesús A. del Alamo,[2] Tomás Palacios,[2] and Carl V. Thompson[1,2,a)]
[1]*Material Processing Center, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*
[2]*Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*

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We have investigated the surface morphology of electrically stressed AlGaN/GaN high electron mobility transistors using atomic force microscopy and scanning electron microscopy after removing the gate metallization by chemical etching. Changes in surface morphology were correlated with degradation in electrical characteristics. Linear grooves formed along the gate edges in the GaN cap layer for all electrically stressed devices. Beyond a critical voltage that corresponds to a sharp increase in the gate leakage current, pits formed on the surface at the gate edges. The density and size of the pits increase with stress voltage and time and correlate with degradation in the drain current and current collapse. We believe that high mechanical stress in the AlGaN layer due to high-voltage stressing is relieved by the formation of these defects which act as paths for gate leakage current and result in electron trapping and degradation in the transport properties of the channel underneath. © *2010 American Institute of Physics*. [doi:10.1063/1.3446869]

AlGaN/GaN high electron mobility transistors (HEMTs) are very attractive for high-power and high-frequency applications.[1] Even though excellent performance has been demonstrated,[2] wide deployment of these devices has been hampered by their uncertain reliability.[3–5]

In previous studies, electrical reliability characterization of GaN HEMTs has revealed that degradation, especially in drain current and current collapse,[6] is driven by the vertical electric field across the AlGaN barrier.[3] Due to the high voltages involved and the piezoelectric nature of GaN, we hypothesized that degradation is related to structural damage of the AlGaN layer.[7] This was later confirmed using cross-sectional transmission electron microscopy (TEM)[8,9] which showed that pits and cracks formed in the film. In order to develop a reliability model, it is important to study material damage under different stress conditions.

Although TEM is of great value, it is an extremely localized technique and sample preparation is costly. Thus the early stages of degradation are difficult to observe and local observations cannot be generalized to behavior along the length of the gate region. Hence, in order to better understand the structural degradation of AlGaN/GaN HEMTs under electrical stress, a planar view of defect formation is required.

In this work, by removing the SiN passivation layer and all the metals on the sample, we have carried out plan-view studies of structural degradation of electrically stressed AlGaN/GaN HEMTs using atomic force microscopy (AFM) and scanning electron microscopy (SEM). Using this method, we have been able to correlate the evolution of surface damage with electrical degradation.

Experimental HEMT devices[2,8] with a GaN cap layer and AlGaN/GaN grown on SiC using metal organic chemical vapor deposition were studied [Figs. 1(a) and 1(b)]. Nominally identical devices that were located side by side were stressed in the OFF-state (low drain current I_D and high source-drain voltage V_{DS}), and at intervals, the stress bias was removed and electrical figures of merit were measured.[3] These include the maximum drain current $I_{D\,max}$, source resistance R_s, drain resistance R_D, and threshold voltage V_T. Before and after the stress, full I-V characteristics and current collapse measurements were also carried out following the protocol in Ref. 10.

Following stress tests, the SiN passivation layer was removed using an HF etch (1:10 $HF:H_2O$) and the contact and gate metals were removed using aqua regia (3:1 $HCl:HNO_3$) at 80 °C for 20 min. The surface was then cleaned using piranha solution ($H_2SO_4:H_2O_2$) for 5 min at 115 °C. The removal of the gate metal enabled the study of the surface of the material underneath and around the gate. We verified on unstressed devices that aside from dislocations and pits that

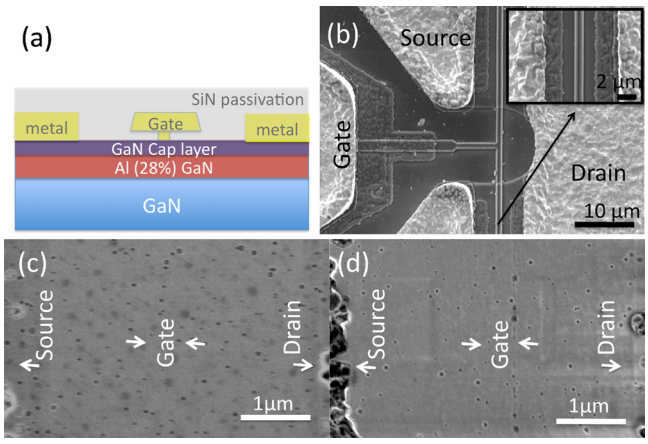

FIG. 1. (Color online) SEM micrographs and schematic of the device. (a) Cross section of the device showing the different layers. (b) Top view of the device before etching. [(c) and (d)] Micrographs of the gate area of unstressed and stressed devices (V_{DG}=20 V), respectively, after metal removal.

a)Electronic mail: cthomp@mit.edu.

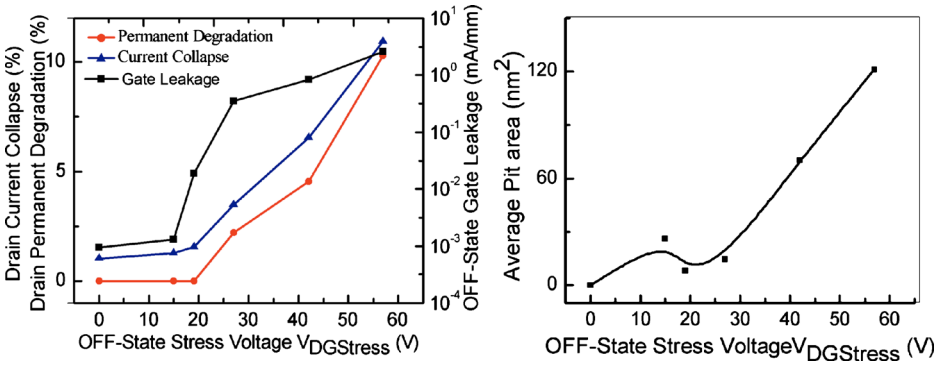

FIG. 2. (Color online) (a) Electrical figures of merit as a function of $V_{DGstress}$: percent decrease in uncollapsed $I_{D\,max}$ (drain current permanent degradation) and percent increase in current collapse (left scale) and absolute value of off-state gate leakage current (right scale). (b) Average pit area vs stress voltage $V_{DGstress}$ in the same experiment. $V_{DGstress}=0$ indicates the unstressed device.

are expected in the virgin material, this material removal process did not introduce any damage to the surface of the device [Fig. 1(c)]. The footprint of the gate wasn't visible either. In contrast, heavily stressed devices, as in Fig. 1(d), show a clear row of pits along the gate edge on its drain side.

Identical devices from the same chip were step-stressed at $V_{GS}=-7$ V with increasing values of V_{DG} from 8 to 50 V, with a step size of 1 V (stressed for 1 min at each step) at a base-plate temperature of 150 °C. We determined that, under these conditions, the critical voltage V_{crit} at which a sharp increase in the gate current occurred[7] was around 20 V [Fig. 2(a)]. Beyond V_{crit} there was significant permanent decrease in $I_{D\,max}$, of up to 10%, as well as a large increase in current collapse [Fig. 2(a)].

AFM scans (Fig. 3) showed that below V_{crit} a groove developed in the GaN cap layer at the drain side of the gate extending the entire length of the device [Fig. 3(b)]. A very faint and discontinuous groove is also detectable on the source side. In unstressed devices [Fig. 3(a)], other than as-grown pits, the surface is smooth under the gate and no groove was observed. For devices stressed at higher voltages, the groove on the source side becomes more apparent [Figs. 3(d) and 3(e)]. For stress voltages beyond V_{crit}, localized pits formed along the groove line, and their density and size increased with an increase in $V_{DGstress}$ [Figs. 3(d) and 3(e)]. For the most heavily degraded devices, these pits penetrate into the AlGaN layer and are as deep as 8 nm, as seen from AFM scans averaged over a gate width of 2 μm [Fig. 3(f)]. The actual depth might be much higher due to the small planar dimensions of the pits compared to the AFM tip radius. Similar groove and pit formation was observed across many devices from different wafers.

Devices were also stressed at $V_{DG}=50$ V for different time periods. As the stress time increases, we observe an increase in the number of pits and a merging of the pits with each other to form a continuous defective region along the gate (Fig. 4). This is consistent with a larger electrical degradation in the device stressed for longer time. The current collapse and permanent drain current degradation increased from 5.1% and 5.6% at 10 min to 17.8% and 26.6% at 1000 min, respectively. The pattern of the defective region and its correlation with electrical degradation are consistent with the electroluminescence results of Ref. 11.

The GaN cap protects the AlGaN surface.[5] Previous TEM studies on similar samples show the existence of a thin oxide layer between the gate and the GaN cap layer.[5,8,9] This layer is seen to be consumed on the drain side with electrical stressing.[5] High temperature storage experiments of our devices (150 °C for over 1000 min) without applied bias showed no electrical degradation or physical degradation of the GaN cap layer. On the other hand, room temperature stress produced the same kind of grooves and pits although with lower density. This suggests an electric field-induced diffusion process. One possibility is that oxygen diffuses to

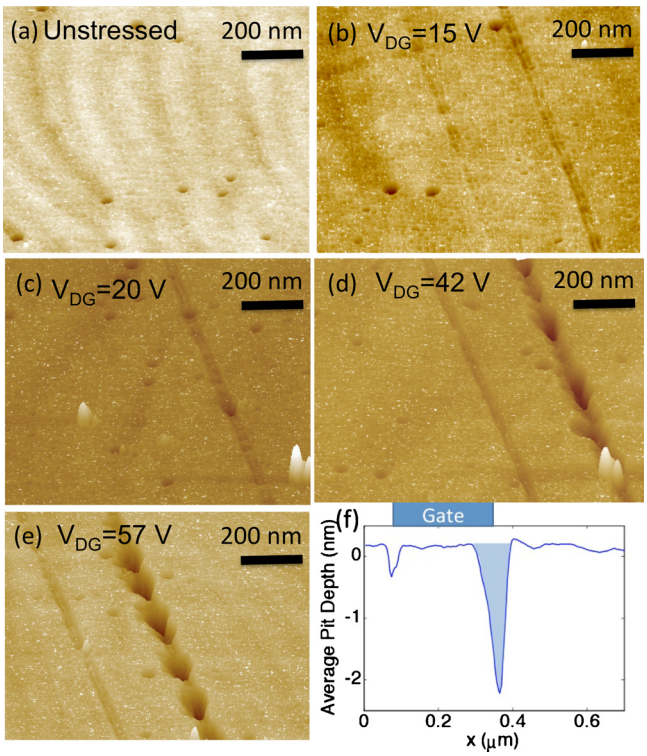

FIG. 3. (Color online) Progressive structural damage with voltage stress (a) unstressed device, (b) $V_{DGstress}=15$ V $<V_{crit}$, (c)$V_{DGstress}=20$ V $\cong V_{crit}$, (d) $V_{DGstress}=42$ V, and (e) $V_{DGstess}=57$ V. (f) Averaged AFM depth profile over a gate width of 2 μm for the most degraded device ($V_{DGstress}=57$ V).

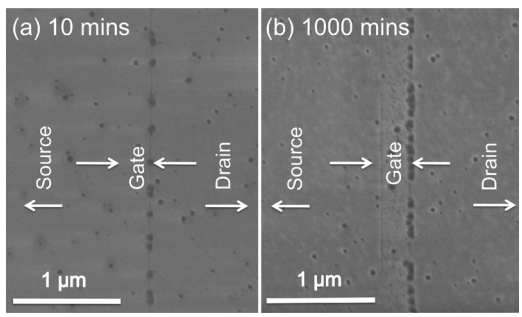

FIG. 4. SEM images of the pits after stressing at $V_{DGstress}=50$ V for (a) 10 min and (b) 1000 min.

cause localized oxidation of the GaN cap under the gate edge, and that this oxide is removed when the sample is exposed to HF, creating the observed grooves.[9,12] However, very shallow indentations were observed in devices stressed below V_{crit} through TEM where no etching process is involved.[13] These grooves are therefore not likely to be a by-product of etching. Electrochemical etching[14,15] and gate metal diffusion to form a product that is subsequently etched might be other possible mechanisms for the groove formation. Since the groove is visible at voltages below the critical voltage, it seems that the inverse piezoelectric effect is not involved in this process.

At the critical voltage, AFM images [Fig. 3(c)] indicate that the groove in the GaN cap layer becomes deep and pits[16] on the AlGaN layer appear on the drain side. Some of these pits may form at nanopipes[17] or v-defects[18] that nucleate on pre-existing threading dislocations which have been established as paths for leakage current.[19–21] However, the pits eventually appear at a density that exceeds the initial defect density, suggesting that new pits form without pre-existing defects. The simultaneous emergence of pits and the increase in gate leakage current at the critical voltage in our electrical measurements are consistent with the electrical characteristics of pits reported in the literature.[17–19]

In the as-grown heterostructure, the top AlGaN layer is under tensile stress due to lattice mismatch with the GaN buffer. The application of a high negative voltage to the gate increases the stress near the gate edge because of the inverse piezoelectric effect.[22] The local stress can be relieved by an increase in the pit density and size.[23] The stress around these pits is generally high enough to generate cracking,[24] likely toward a nearby pit. The appearance of pits and cracks reduces the maximum drain current and introduces trapping centers that contribute to current collapse. In fact, the average cross-sectional pit area computed along the gate width [defined as the shaded area in Fig. 3(f)] correlates well with the degradation in drain current and current collapse [Fig. 2(b)].

In conclusion, we have developed a wet etching process for removal of the metallization stack in AlGaN/GaN HEMTs that allows us to characterize the exposed surface using AFM and SEM. Using this technique, we have studied the evolution of structural damage at the surface of experimental devices after stressing them in the OFF state condition at different voltages and lengths of time. The electrical degradation is closely related to structural damage at the gate edge of the device. We postulate that degradation is a three-step process; first a groove forms in the GaN cap layer due to field-induced oxidation or electrochemical etching. This is followed by pit formation and subsequent growth and eventually the formation of cracks along the edge of the gate in the AlGaN layer. Though thermally enhanced, the diffusive processes that are required for groove formation and pit growth only occur in the presence of an electric field. As a consequence, both field and thermal enhancement must be accounted for in reliability models for the associated degradation processes.

This work represents the first plan-view, large-area characterization of the evolution of defects associated with GaN HEMT electrical degradation. The methodology described here will enable further studies focused on development of a better mechanistic understanding of the evolution of defects under various electrical stress conditions, and ultimately, modeling and improvement of the reliability of these devices.

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