GaN power electronics

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Bin Lu, Daniel Piedra and Tomás Palacios

Department of Electrical Engineering and Computer Science,
Massachusetts Institute of Technology,
77 Massachusetts Ave., Bldg. 39-567B, Cambridge, MA 02139, USA
e-mail: tpalacios@mit.edu

Between 5 and 10% of the world's electricity is wasted as dissipated heat in the power electronic circuits needed, for example, in computer power supplies, motor drives or the power inverters of photovoltaic systems. This paper describes how the unique properties of GaN enables a new generation of power transistors has the potential to reduce by at least an order of magnitude the cost, volume and losses of power electronic systems. We will describe three key technologies: Schottky drain contacts and substrate removal to increase the breakdown voltage, and a dual-gate device with superior enhancement-mode characteristics.

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are excellent candidates for the next generation of power electronics, due to their combination of high electron mobility (μ_e) and high critical electric field (E_c)[1], [2]. As shown in Figure 1, for a given breakdown voltage V_{bk}, normally set by the application, the theoretical specific on-resistance, R_{ON}, of GaN transistors is nearly three orders of magnitude smaller than that of Si transistors and it also surpasses the limit of SiC. These excellent performance enables the use of GaN high voltage transistor in a new generation of power electronic circuits, characterized by at least 10-fold reduction in power losses, volume and cost.

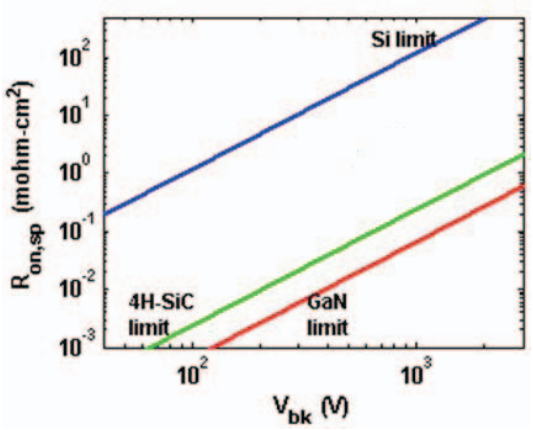

Figure 1: Specific on-resistance as a function of operating voltage for different semiconductor materials.

Most of the reported high-breakdown AlGaN/GaN HEMTs are grown on SiC substrates. However, the limited diameter (up to 4 inch) and high cost of SiC severely hinders the commercialization of GaN-based power electronics in SiC. Intense effort is currently under way to demonstrate the performance GaN transistors on Si substrate, where the low cost and large diameters of the wafers are very attractive from a commercialization point of view.

2. Challenges for GaN-on-Si Power Electronics

In spite of the great potential of GaN on Si high voltage transistors, its application to power electronics is currently limited by three important challenges. On one hand, the breakdown voltage of GaN transistors on Si substrates is lower than when SiC is used as a substrate. To mitigate the effect of the Si substrate, very thick layers of GaN buffer are

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typically used, which increases the wafer cost and, more importantly, the wafer bow[3]. Wafers with more than 50 μm of bow are very difficult to process using commercial fabrication technologies. In addition, the great majority of GaN transistors are normally-on or depletion mode due to the large charge densities induced by the polarization at the AlGaN/GaN interface. Finally, the leakage current of GaN transistors is still higher that what is required in power electronics (<0.1 μA/mm). In this paper we present three novel technologies to overcome the challenges described above:

1. Schottky-drain metallization
2. Substrate removal
3. Dual gate transisors

3. Schottky-Drain Technology

To maximize the breakdown voltage of GaN power transistors for a given thickness of the buffer region, it is important to engineer the electric field in the drain access region in a way that it is as uniform as possible. Our group has recently developed a new drain contact technology based on a Schottky metallization that significantly increases the device breakdown voltage[4].

To demonstrate our Schottky drain technology, we used commercially-available GaN/$Al_{0.26}Ga_{0.74}N$/AlN/GaN transistor structures grown by metal organic chemical vapor deposition on Si (111) substrates by Nitronex. The heterostructure has a 20 Å GaN cap layer, a 175 Å $Al_{0.26}Ga_{0.74}N$ barrier and a 10 Å AlN interlayer on a 2 μm undoped GaN buffer and transition layer. Standard ohmic contacts were formed by Ti/Al/Ni/Au alloyed for 30 s at 870C in N_2 atmosphere. Unannealed Ti/Au was used as Schottky metallization in the Schottky drain devices. Prior to the Ti/Au deposition, 10 nm recess on the GaN/$Al_{0.26}Ga_{0.74}N$ barrier was performed by BCl_3 and Cl_2 plasma with an etch rate of 13~14 Å/min to reduce the series resistance in the Schottky contact. Then 150 nm mesa isolation was achieved by BCl_3 and Cl_2 plasma etching. Finally, Ni/Au/Ni Schottky gates were formed by E-beam evaporation. Both the ohmic drain and Schottky drain devices were fabricated at the same time on the same wafer. All the breakdown voltages were measured with a Tektronix Curve Tracer 576 system. The breakdown voltage is defined as the voltage at which the leakage current reaches 1 mA/mm. The devices were immersed in Fluorinert™ FC-770 to prevent surface flash breakdown during measurements.

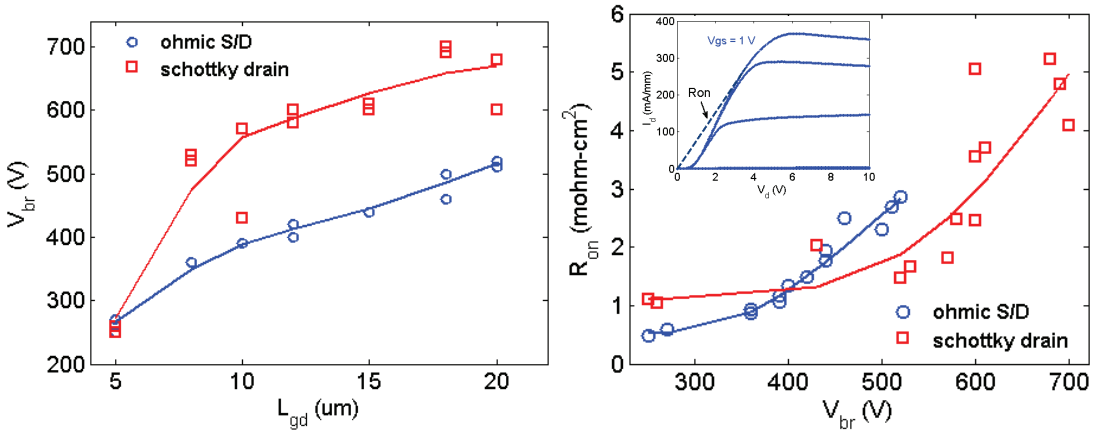

Figure 2: Three terminal breakdown measurement for alloyed ohmic contact and Schottky drain contact.

At least two different mechanisms limit the breakdown voltage in power transistors: buffer/substrate breakdown and gate breakdown. The new Schottky drain devices help improving both of them. We measured the buffer/substrate breakdown voltages of the standard and the Schottky drain devices. In these measurements, a 150 nm deep recess was performed between the contacts to eliminate the 2DEG. The buffer/substrate breakdown of the conventional ohmic drain devices is about 550V. By using Schottky drain contact, the buffer/substrate breakdown voltage is increased above 700 V. This improvement has been associated to the much smoother morphology of the Schottky drain contacts. In conventional ohmic contacts, the high temperature annealing causes metal spikes which we believe increase the electric field, reducing the breakdown voltage.

Three terminal breakdown voltages were also measured on both Schottky drain and ohmic drain HEMTs as shown in Figure 2. Again, the Schottky drain devices had almost 200 V higher breakdown voltage than the standard transistors. This higher performance is obtained without degrading the specific on-resistance, R_{on}. The specific R_{on} resistance was calculated from the I-V curves of the devices when V_{ds}/I_{ds} reaches the lowest value divided by the active area defined as the area between source and drain. The Schottky drain devices have higher breakdown voltage and better V_{br}/R_{on} characteristic at high voltage level.

4. Substrate Removal Technology

For large enough source-to-drain distances, the ultimate breakdown voltage of a GaN power transistor on Si is determined by the distance between the GaN channel and the Si substrate [3]. The Si substrate is typically p-type doped during the grown of the GaN buffer and acts as a highly conductive layer underneath the GaN transistor and the critical breakdown field in the device then becomes vertical instead of horizontal.

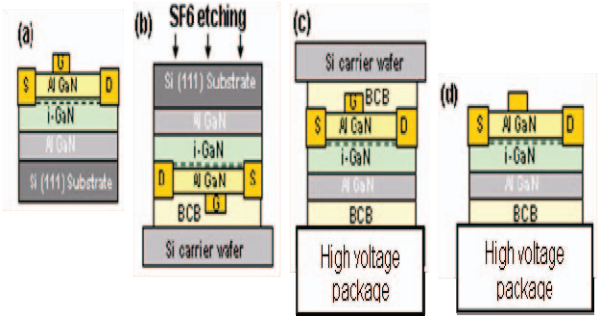

Figure 3. Simplified process flow for the removal of the original substrate in GaN power transistors.

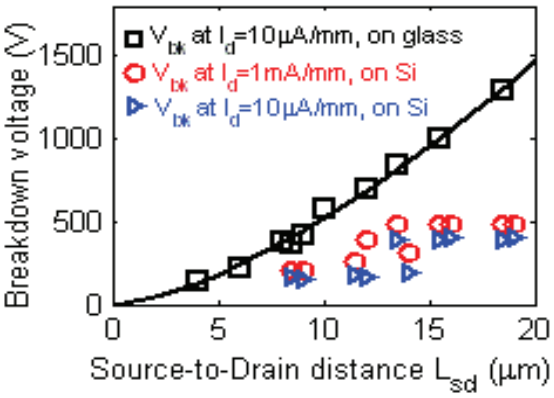

Figure 4. Typical breakdown voltage as a function of source-to-drain distance for AlGaN/GaN structures with and without Si substrate removal technology.

To eliminate the vertical breakdown of the AlGaN/GaN HEMTs on Si, our group has recently demonstrated a new technology based on chemically removing the Si substrate and transferring the AlGaN/GaN HEMTs to a high voltage insulating substrate (glass in our first demonstration) through wafer bonding (Figure 3) [5]. This new device shows a x3-4 fold increase in the maximum breakdown voltage for a given gate-to-drain spacing. For example, device with L_{gd} = 18 μm shows breakdown of 1370 V and on-resistance of 4.3 mΩ•cm^2 with very low leakage current (< 10 μA/mm), much higher than the ~500 V of breakdown obtained in the same device before removing the Si substrate. Figure 4 shows the two terminal buffer breakdown voltage as a function of source-to-drain spacing (L_{sd}). More than 1450 V breakdown and an on-resistance of 5.3 mΩ•cm^2 is achieved on devices with L_{gd} = 20 μm, which is beyond our power supply maximum output voltage.

5. Dual Gate Technology

In spite of the great potential of AlGaN/GaN HEMTs for power electronics applications, its use is severely limited by most of the devices being depletion-mode (D-mode). Enhancement-mode (E-mode) AlGaN/GaN HEMTs are highly desirable for power electronics as they can greatly simplify circuit designs and improve system reliability. Several approaches have been reported in the past to fabricate normally-off GaN HEMTs, including gate recess, AlGaN/GaN/AlN/GaN heterojunctions, fluorine plasma treatment, and p-type AlGaN gate, among others. Many of these methods, although successful in achieving E-mode operation, compromise the on-current, specific-on resistance and the threshold voltage. We have recently developed a new dual-gate AlGaN/GaN E-mode HEMT with a threshold voltage of 2.5 V, maximum drain current of 430 mA/mm, and breakdown voltage of 643 V at zero gate-to-source voltage [6].

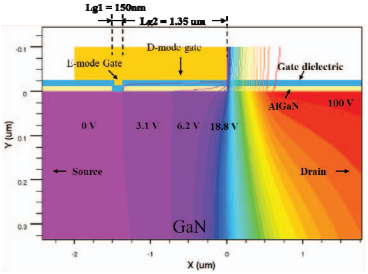

Figure 5: Simulation of the electrostatic potential in AlGaN/GaN HEMTs fabricated with a dual gate technology.

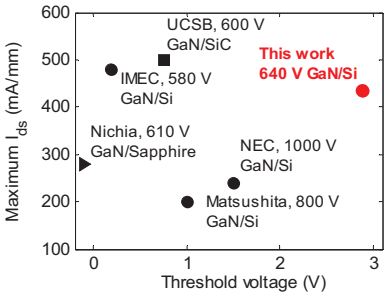

Figure 6: Trade-off between maximum ON current and threshold voltage in different devices reported in the literature.

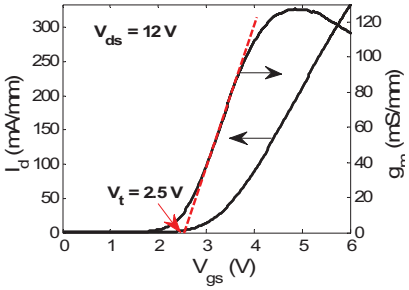

Figure 7: Transfer characteristic and threshold voltage of a dual-gate GaN power transistor.

The device reported in this paper has the same wafer structure and fabrication technology that it was reported in section 3 of this paper. The only difference is the use of a new dual gate structure, where a very short gate controls the E-mode behavior while a longer gate (D-mode) supports most of the electric field in pinch-off as shown in Figure 5. The first ~ 150-nm-long gate was patterned with electron beam lithography and the AlGaN barrier was then fully recessed with low damage BCl_3/Cl_2 plasma etching. 14 nm Al_2O_3 gate dielectric was then deposited by atomic layer deposition. Finally, a 2-µm-long Ni/Au/Ni gate was deposited overlapping with the first gate-recess region. The 2 µm gate was shifted ~ 1 µm towards the drain side to support the drain voltage. The transistor has a gate-to-source spacing (L_{gs}) of 1.5 µm and a gate-to-drain spacing (L_{gd}) of 18 µm.

The new dual gate device shows a maximum drain current of 430 mA/mm (Figure 6), with a specific on-resistance of 4.1 mΩ.cm2. The double gate structure allows this device to combine a low on-resistance with a large threshold voltage of 2.5 V, extrapolated from the g_m-V_{gs} transfer characteristic curve (Figure 7). The breakdown voltage, measured at V_{gs} = 0 V, was 643 V with gate leakage less than our equipment sensitivity of 100 nA/mm. The combination of large threshold and breakdown voltage, with the low on-resistance and leakage current makes this new E-mode device a very attractive option for the next generation of power electronics circuits.

6. Conclusion

In conclusion, GaN-on-Silicon HEMTs offer the potential to revolutionize power electronics by enabling important energy savings and new flexibility for advanced power circuits. In this paper, we have presented three new technologies to overcome some of the main challenges of these devices. First, by using a Schottky drain contact the buffer breakdown can be significantly increased. Second, the removal of the Si substrate allows the fabrication of GaN HEMTs with only 2 µm of GaN buffer thickness and more than 1500 V breakdown. And third, a dual-gate technology enables the combination of low on-resistance and normally-off behavior in the same device. By using these technologies and others currently under development, GaN power electronics will quickly become one of the main markets for GaN devices.

Acknowledgement

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