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**Citation:** Wang, Han et al. "Gigahertz Ambipolar Frequency Multiplier Based on CVD Graphene." Proceedings of the IEEE International Electron Devices Meeting (IEDM), 2010. 23.6.1–23.6.4. © Copyright 2010 IEEE

**As Published:** <http://dx.doi.org/10.1109/IEDM.2010.5703423>

**Publisher:** Institute of Electrical and Electronics Engineers (IEEE)

**Persistent URL:** <http://hdl.handle.net/1721.1/72955>

**Version:** Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

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# Gigahertz Ambipolar Frequency Multiplier based on CVD Graphene

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## Abstract

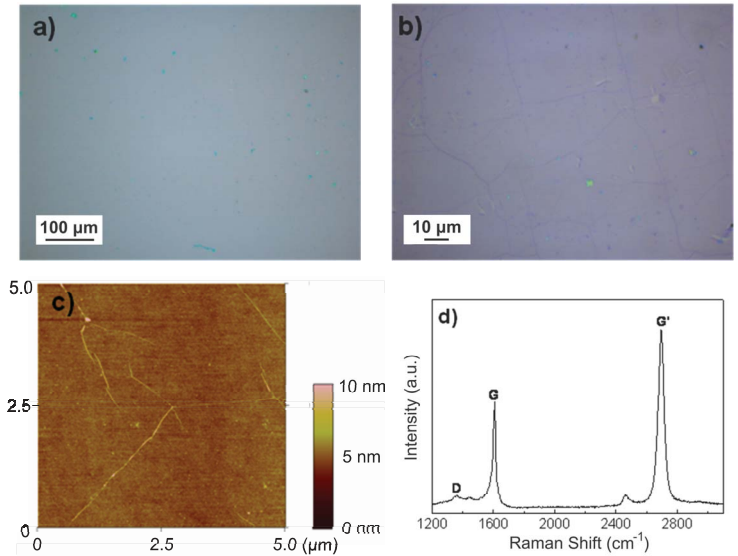
Ambipolar transport in graphene offers great opportunities for novel device and circuit applications. This paper discusses the RF performance of CVD grown graphene transistors for the first time. Then, a new graphene ambipolar frequency multiplier that can operate at 1.4 GHz with extremely high output spectral purity ( $> 90\%$ ) is demonstrated. These GHz graphene frequency multipliers, made from wafer-scale graphene synthesis and fabrication processes, demonstrate the great potential of graphene-based ambipolar devices for RF and mixed-signal applications.

## Introduction

The unique ambipolar transport properties of graphene, combined with its high mobility ( $>100,000 \text{ cm}^2/\text{Vs}$  in suspended graphene, and  $>10,000 \text{ cm}^2/\text{Vs}$  in graphene on a substrate at room temperature) [1, 2], enable the development of a new form of non-linear electronics for radio frequency (RF) and mixed-signal applications [3, 4, 5]. This paper presents a new graphene ambipolar frequency multiplier that can operate at gigahertz frequencies. The contributions of this paper are three-fold. First, RF performance of graphene field effect transistors (GFET) grown by chemical vapor deposition (CVD) is presented for the first time. Second, this device demonstrates ambipolar frequency multiplication at 1.4 GHz. This improves frequency performance of graphene frequency multipliers by more than 4 orders of magnitude from previous work [3, 4, 6], making it suitable for a much wider range of applications in communication systems. Finally, these devices show a very high spectral purity at the output without any filtering, where more than 90% of the RF power is at the useful frequency. This excellent spectral purity is highly desirable for high frequency mixed-signal circuits.

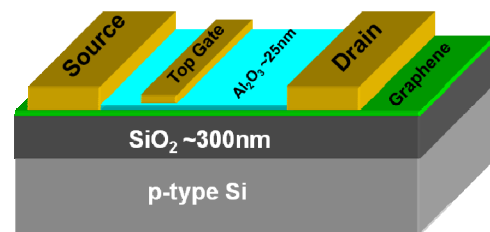
## CVD Growth and Device Fabrication

Single-layer graphene films were grown by CVD on copper substrates [7]. Firstly, copper foils are annealed at  $1000^\circ\text{C}$  in  $\text{H}_2$  (350 mTorr for 30 minutes) to increase the grain size of copper. Then, they are exposed to  $\text{CH}_4$  under low-pressure condition (1.6 Torr) to initiate graphene growth. After the growth, polymethyl methacrylate (PMMA) is coated on the graphene film and the copper substrate is etched away in copper etchant and diluted HCl. Films are then transferred



**Fig.1** (a) and (b) optical micrograph of CVD-grown graphene. Using Cu substrate, single-layer graphene with uniformity greater than 95% is obtained. (c) AFM image of the graphene obtained with a Veeco Dimension 3100 system showing excellent uniformity. (d) Raman spectrum confirms the presence of single-layer graphene.

onto polished Si wafers with a 300 nm thermally-grown  $\text{SiO}_2$  on top (Fig. 1). As shown in Fig. 1, Raman spectroscopy confirms that single-layer graphene with uniformity greater than 95% can be grown. Carrier mobilities in the 1800 to 2500  $\text{cm}^2/\text{Vs}$  range were measured through Hall effects. The ohmic contacts of the GFETs are formed by depositing a 2.5 nm Ti/ 45 nm Pd/ 15 nm Au metal stack by e-beam evaporation. Device isolation is achieved by  $\text{O}_2$  plasma etching. The gate dielectric consists of 5 nm of e-beam evaporated  $\text{SiO}_2$  as a seed layer; followed by 15 nm  $\text{Al}_2\text{O}_3$  deposited using Atomic Layer Deposition (ALD). The top gate is formed with a 30 nm

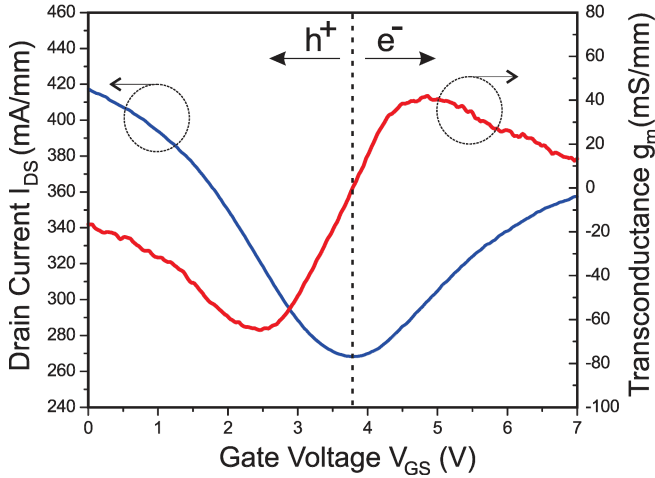


**Fig.2** Structure of the fabricated devices. Ohmic metal: 2.5 nm Ti/ 45 nm Pd/ 15 nm Au; Gate dielectric: 5 nm  $\text{SiO}_2$  (e-beam)+15 nm  $\text{Al}_2\text{O}_3$  (ALD); Gate Metal: 30 nm Ni/ 200 nm Au/ 50 nm Ni; Source to Drain Distance  $L_{\text{DS}} = 1.7 \mu\text{m}$ ; Gate Length  $L_{\text{G}} = 1.6 \mu\text{m}$ ; Channel Width  $W = 25 \mu\text{m}$ .

Ni/ 200 nm Au/ 50 nm Ni metal stack (Fig. 2). DC and RF characterization of the devices was performed using an Agilent 4155C Parameter Analyzer and an Agilent N5230 Vector Network Analyzer respectively. The devices were measured at room temperature under vacuum ( $1.4 \times 10^{-4}$  Torr) to reduce hysteresis.

### DC and RF characteristics

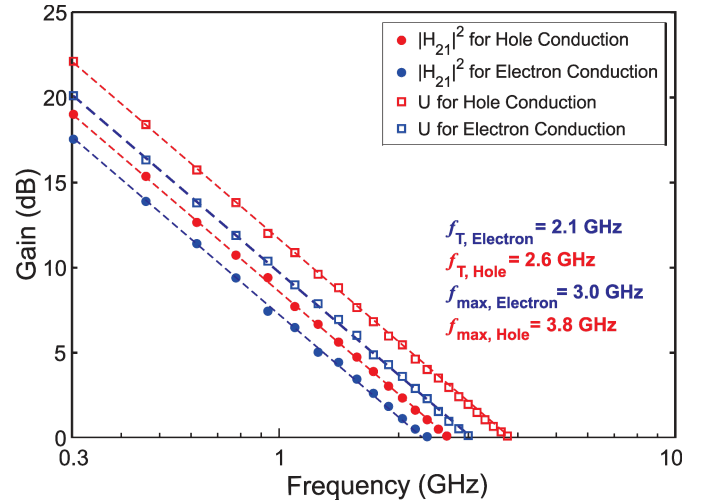
Fig. 3 shows the DC characteristics of the fabricated GFETs. The minimum conduction point is at 3.7 V. The peak transconductance for hole and electron conduction is -68 mS/mm and 40 mS/mm respectively. Fig. 4 shows the RF characteristics of the GFETs. The extrinsic current-gain cut-off frequency,  $f_T$ , and the extrinsic maximum oscillation frequency,  $f_{max}$ , for hole conduction are  $f_{T,Hole}=2.6$  GHz and  $f_{max,Hole}=3.8$  GHz and for electron conduction are  $f_{T,Electron}=2.1$  GHz and  $f_{max,Electron}=3.0$  GHz. Both hole and electron transports are important for frequency doubling since, as it is described in the next section, the conduction in these devices happens by alternating half cycles of holes and electrons. The frequency performance will be limited by the lower of the two conduction modes.



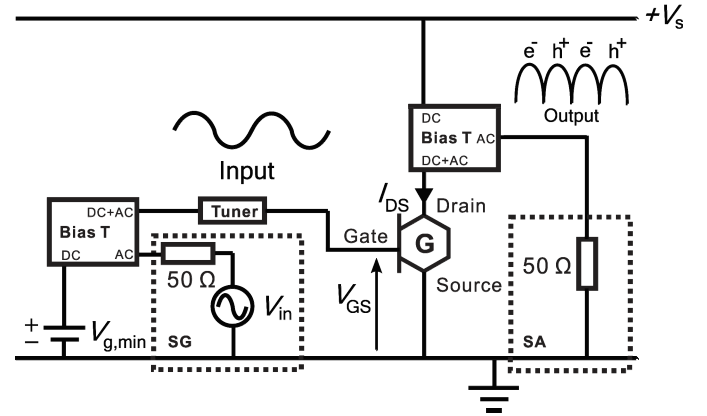
**Fig.3** DC characteristics of GFET at  $V_{DS}=4.5$  V. Device dimensions are given in Fig. 2. The hole conduction mode has slightly higher transconductance than the electron conduction mode.

### Frequency Doubling at Gigahertz Frequencies

Fig. 5 shows the test circuit for frequency doubling. Low loss bias tees are used both at the input and the output to combine DC and RF signals, and provide isolation between them. Tuners are used at the input to provide adequate impedance matching. Under the test conditions, the gate of the GFET is biased at its minimum conduction point. As a sinusoidal RF signal is superimposed to the gate DC bias, the GFET will operate in alternating half cycles of electron and hole conduction due to the V-shape transfer characteristics of the



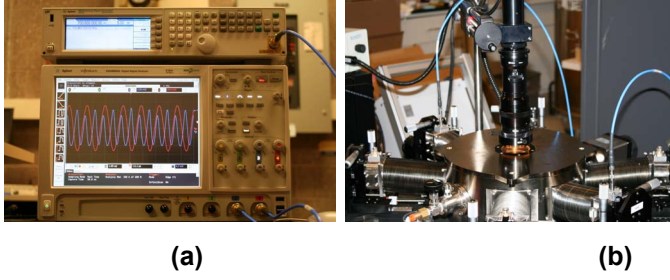
**Fig.4** RF characteristics of the GFETs.  $f_T$  and  $f_{max}$  are higher for hole conduction than for electron conduction, in correspondence to similar discrepancies in the DC transconductances shown in Fig. 3. The device dimensions are shown in Fig. 2. DC bias:  $V_{DS}=3$  V and  $V_{GS}=1.5$  V for the hole side and 5 V for the electron side.



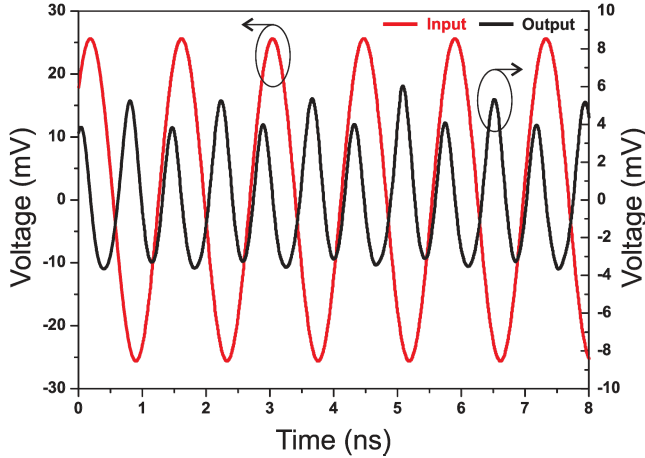
**Fig.5** Application and test circuit for frequency doublers. Low loss bias tees are used to decouple DC and RF signals, and to provide isolation between them. A tuner is used at the input to match the impedance. SG: Signal Generator. SA: Spectrum Analyzer.

GFET. The sinusoidal input signal is, hence, full-wave rectified by the GFET, giving an output signal that has a fundamental frequency twice of the input frequency.

Fig. 6 shows the measurement setup. Clear frequency multiplication is observed between the input signal and the output signal, both measured by an Agilent DSA90604A oscilloscope. Fig. 7 plots both the input signal at 700 MHz and the output signal, which has a fundamental frequency of 1.4 GHz. Frequency doubling is clearly demonstrated. This frequency doubler device shows high spectral purity in the output RF signal, where more than 90% of the output RF energy is at the useful frequency (1.4 GHz). Frequency doubling at 1.4 GHz is also confirmed by the output signal spectrum measured by an Agilent N9010A spectrum analyzer. In the output signal, the signal power at  $f_{out}=2f_{in}=1.4$  GHz is



**Fig.6** Measurement setup for demonstrating frequency doubling. (a) Signal generator and Agilent DSA90604A oscilloscope showing frequency doubling. (b) Lakeshore Cryogenic Probe Station for RF and frequency doubling measurements in vacuum.

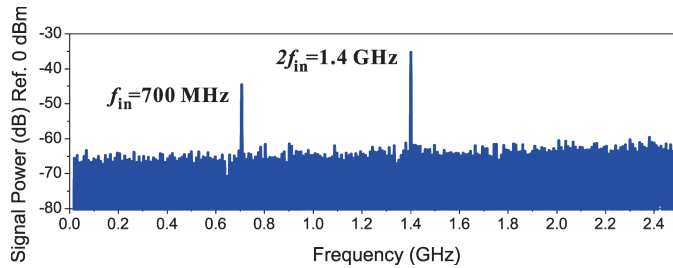


**Fig.7** Experimental demonstration of frequency doubling measured by an Agilent DSA90604A oscilloscope. The input is at 700 MHz. The output fundamental frequency is 1.4 GHz. DC bias:  $V_{DS}=1$  V. The gate is biased at  $V_{GS}=3.61$  V, slightly below the minimum conduction point (3.7 V), to compensate for the small asymmetry in the transfer characteristics and, hence, to improve symmetry of electron and hole conduction at the output.

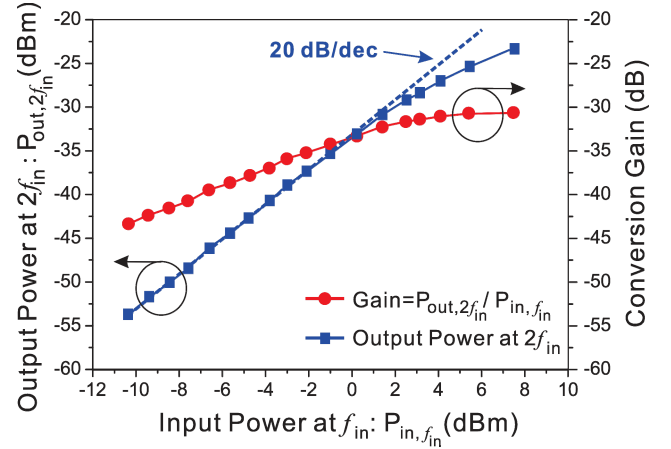
about 10 dB higher than the signal power at  $f_{out}=f_{in}=700$  MHz (Fig. 8). This is the first time frequency doubling has been achieved with a single transistor at gigahertz frequencies without any filtering elements.

### Conversion Gain

Fig. 9 shows the output power at  $f_{out}=2f_{in}$ ,  $P_{out,2f_{in}}$  (blue square),

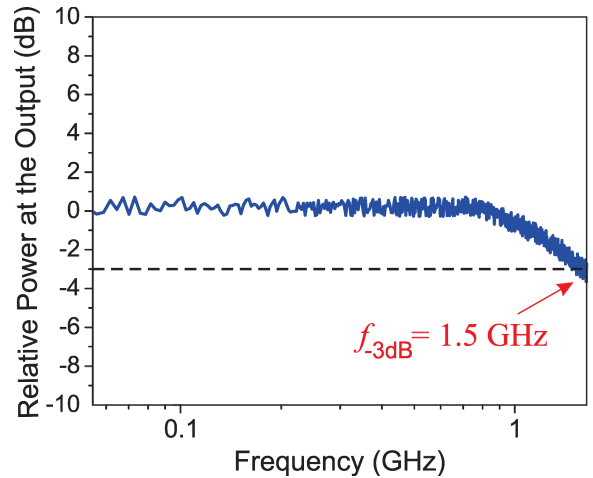


**Fig.8** Power spectrum of the output signal from the graphene frequency doublers. The input is at 700 MHz. Frequency doubling is clearly visible. The signal power at  $f_{out}=2f_{in}=1.4$  GHz is about 10 dB higher than signal power at  $f_{out}=f_{in}=700$  MHz without filtering. More than 90% of the total RF power in the output signal is at 1.4 GHz. DC bias:  $V_{DS}=1$  V and  $V_{GS}=3.61$  V.



**Fig.9** Output power at  $f_{out}=2f_{in}$  is plotted against the input power at  $f_{in}$ . The output power at  $2f_{in}$  increases with the input power with a slope of 20 dB/dec. Conversion Gain =  $P_{out,2f_{in}}/P_{in,f_{in}}$  increases with input power up to 2 dBm.

against input power at  $f_{in}$ ,  $P_{in,f_{in}}$ . The output power increases with the input power at a slope of 20 dB/dec. This agrees with the fact that the signal at  $f_{out}=2f_{in}$  is generated by the quadratic component in the transfer characteristics of the GFET and its power increases with a slope of 2 with respect to input power when plotted in logarithmic scale. The conversion gain (red dot), defined as:  $gain=P_{out,2f_{in}}/P_{in,f_{in}}$ , increases with input power up to  $P_{in,f_{in}}=2$  dBm where saturation starts to occur. The gain, while still low, has improved by two orders of magnitude from previous work [3].



**Fig.10** Frequency dependence of gain. The -3dB cut-off point is at 1.5 GHz. Bandwidth is not limited by the carrier transit time, but mainly by the RC constant of the device.

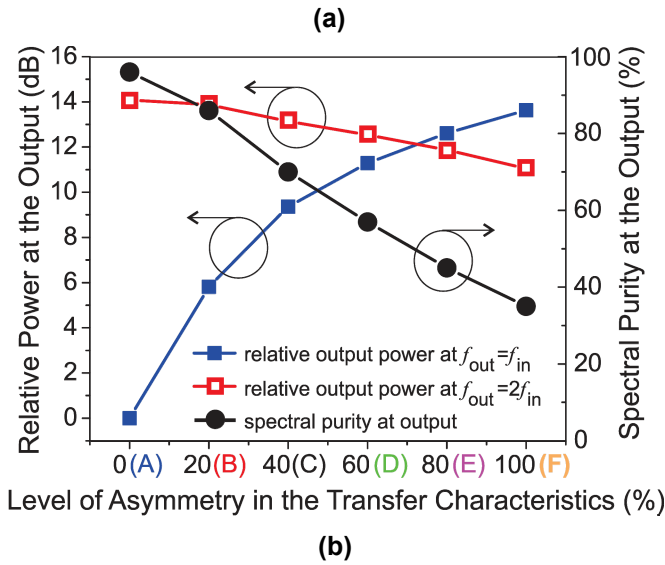
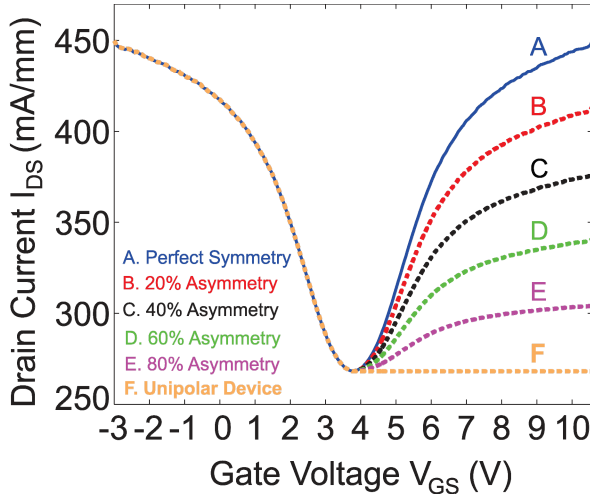
### -3dB Cut-off Frequency

The frequency dependence of the gain is characterized and shown in Fig. 10. The -3dB cut-off point is 1.5 GHz, at about 70% of  $f_{T,Electron}=2.1$  GHz. Owing to the high carrier mobility and high saturation velocity, the bandwidth is not limited by

the carrier transit time, but mainly by the RC time constant of the device.

### Effects of Asymmetry in Device Characteristics

By simulating the input and output signals from GFETs using MATLAB, we study the effects of asymmetry in GFET transfer characteristics on the spectral purity at the output. As shown in Fig. 11(a), devices with transfer characteristics ranging from perfect symmetry to unipolar are simulated. The hole conduction branch of these devices' transfer



**Fig. 11** Effects of asymmetry in the transfer characteristics on relative output power at  $f_{out}=f_{in}$  and  $f_{out}=2f_{in}$ . (a) Simulated transfer characteristics: the left half of the transfer curve is identical to that in Fig. 3. The right half is simulated from (A) perfect symmetry, to (F) unipolar (similar to conventional FET). (b) Relative output power at  $f_{out}=f_{in}$  (blue squares) and  $2f_{in}$  (red squares) for devices from 0% asymmetry (perfect symmetry) to 100% asymmetry (unipolar device), corresponding to simulated devices A to F in Fig. 11(a). The device is assumed to be biased at the minimum conduction point. The output spectral purity (black dots) decreases as the GFET transfer characteristics becomes more asymmetrical.

characteristics is assumed to be identical to the device in Fig. 3. The device is assumed to be biased at the minimum conduction point. Fig. 11(b) shows the simulated relative output power at  $f_{out}=f_{in}$  and  $f_{out}=2f_{in}$ . As the device transfer characteristics changes from perfect symmetry to unipolar, the relative power at  $f_{out}=f_{in}$  increases from 0 dB to 13.5 dB while the power at  $f_{out}=2f_{in}$  decreases from 14 dB to 11 dB. This result shows that, for a given input power, as the device transfer characteristics becomes more asymmetric, the quadratic term in the transfer characteristics decreases while the linear term increases, leading to a reduction in the output power at  $f_{out}=2f_{in}$  (and other even order harmonics) and an increase in the output power at  $f_{out}=f_{in}$  (and other odd order harmonics). Hence, the output spectral purity for frequency doubling decreases as a result. As shown in Fig. 11(b), perfectly symmetric GFETs can achieve a spectral purity that is well above 90% (vs. 35% for unipolar device similar to conventional FET). This highlights the great advantage of ambipolar frequency multipliers in terms of output spectral purity as compared to the conventional frequency multipliers based on unipolar devices.

### Conclusion

In conclusion, this paper presents a new ambipolar frequency multiplier based on CVD graphene with operation up to 1.4 GHz. These new ambipolar frequency multipliers can achieve extremely high spectral purity in the output signal ( $> 90\%$ ), which is confirmed by both experimental results and numerical simulations. With the graphene used in the devices grown by wafer-scale CVD synthesis and the device fabrication processes compatible with traditional technologies in semiconductor industry, these gigahertz graphene frequency multipliers demonstrate the great potential of graphene-based ambipolar devices for RF and mixed-signal applications, and possible integration with Si electronics in the near future.

### Acknowledgements

This work has been partially supported by the ONR GATE MURI program (Dr. Chagaan Baatar) and by the MSD Focus Center.

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