Strained silicon on silicon by wafer bonding and layer transfer from relaxed SiGe buffer

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***Abstract* — We report the creation of strained silicon on silicon (SSOS) substrate technology. The method uses a relaxed SiGe buffer as a template for inducing tensile strain in a Si layer, which is then bonded to another Si handle wafer. The original Si wafer and the relaxed SiGe buffer are subsequently removed, thereby transferring a strained-Si layer directly to Si substrate without intermediate SiGe or oxide layers. Complete removal of Ge from the structure was confirmed by cross-sectional transmission electron microscopy as well as secondary ion mass spectrometry. A plan-view transmission electron microscopy study of the strained-Si/Si interface reveals that the lattice-mismatch between the layers is accommodated by an orthogonal array of edge dislocations. This misfit dislocation array, which forms upon bonding, is geometrically necessary and has an average spacing of approximately 40nm, in excellent agreement with established dislocation theory. To our knowledge, this is the first study of a chemically homogeneous, yet lattice-mismatched, interface.**

Index Terms — layer transfer, SiGe graded buffer, strained silicon, wafer bonding

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I. Introduction

The relaxed graded SiGe buffer has allowed for the development of a multitude of new heterostructures with enhanced properties relative to bulk Si. Early work focused on using these relaxed buffers as templates for inducing tensile strain in silicon channels, and metal-oxide-semiconductor field-effect transistor (MOSFET) devices utilizing these strained-Si channels have long been recognized to provide significantly enhanced performance over their bulk silicon counterparts (1-3, 4-5). A logical extension of using SiGe buffers to engineer strained heterostructures involved the use of compressively strained Ge-rich SiGe layers that served as enhanced conduction pathways for holes, making them ideal for PMOS applications (6). By selectively utilizing the band alignments of strained-Si, strained-SiGe, and strained-Ge for optimal carrier confinement, the relaxed SiGe buffer has recently been used to fabricate dual-channel heterostructures that exploit the enhanced electron mobility of strained-Si as well as the enhanced hole mobility of strained Ge-rich layers (7-8). Dual-channel devices utilizing relaxed SiGe buffers graded to $Si_{0.5}Ge_{0.5}$ have even exhibited nearly symmetric electron and hole mobilities (9).

Recently, however, the utility of the relaxed SiGe buffer has been further extended to allow for the transfer of various scaleable, lattice-mismatched layers to Si handle wafers. Successful demonstrations of layer transfer using relaxed SiGe buffers include strained-Si on insulator (SSOI), silicon-germanium on insulator (SGOI), and most recently germanium on insulator (GOI) (10, 11-15, 16). As the crosshatch surface roughness inherent to efficient relaxation during the grading process in SiGe buffer growth precludes the possibility of successful bonding, a chemical-mechanical planarization (CMP) step is required to reduce to the RMS surface roughness to a level suitable for bonding. For the case of Ge and Ge-rich $Si_{1-x}Ge_x$ (i.e. $x>0.6$) layers transferred to Si, where the Ge-rich surface cannot be easily planarized using standard Si CMP

techniques, an intermediary low-temperature oxide (LTO) layer can be deposited and subsequently planarized, thereby allowing successful bonding to take place using relatively well-established hydrophilic bonding techniques (16).

A significant drawback to the SSOI, SGOI, GOI, and strained-Si on relaxed SiGe platforms mentioned above for high-power devices is their dramatically reduced thermal conductivity values near the active device regions relative to bulk silicon substrate. Though its presence drastically reduces parasitic capacitances, an intermediate oxide layer has a thermal conductivity value of 0.014 W cm^{-1} K^{-1} at 300 K, nearly 2 orders of magnitude lower than bulk Si, which serves to significantly reduce heat extraction from the device channel (17). Attributable mainly to increased scattering due to alloying effects, even relaxed silicon germanium layers with Ge fractions of about 0.25 have significantly reduced thermal conductivities relative to silicon, with values on the order of 0.1 W cm^{-1} K^{-1} at 300 K (18). Local temperature increases near the device channel can lead to loss of mobility and a reduced drain current (19). Temperatures in SOI devices, for example, have reportedly increased as much as 100 K under static conditions (20).

For high-power applications, it would be highly beneficial to couple the performance gain of strained-Si technology with the high thermal conductivity of bulk Si near the active device regions. This strained-Si on silicon (SSOS) substrate technology, in which a strained-Si layer would be transferred directly to bulk Si without intermediary oxide or SiGe layers, would make SSOS a direct substitution for silicon substrate. Furthermore, the SSOS substrate would be the first system studied in which a chemically homogeneous, single-phase system exhibits lattice-mismatch.

II. Experiment

SSOS substrates without an intermediate SiGe or SiO_2 layer were fabricated by wafer bonding and layer transfer, as shown in the process flow diagram in Figure 1. The process involved growth of relaxed SiGe virtual substrate at 900°C via ultra-high vacuum chemical vapor deposition (UHVCVD) to fabricate relaxed $Si_{0.76}Ge_{0.24}$ layer which was compositionally-graded at 10% Ge μm^{-1} with a 3 µm $Si_{0.76}Ge_{0.24}$ cap layer. The combination of a low grading rate and a high growth temperature results in complete relaxation with threading dislocation densities of ~10^5 cm^{-2} (21). The structure was then chemical-mechanical polished to reduce the RMS surface roughness to a level suitable for bonding. Following the regrowth of 20 nm of $Si_{0.76}Ge_{0.24}$ at 550 °C, an 18 nm strained-Si transfer layer was deposited. A lower growth temperature was chosen for these layers in order to preserve planarity at the surface.

The strained-Si on graded SiGe buffer and another Si wafer were then treated with a modified RCA clean consisting of 10 min in $3H_2SO_4$:$1H_2O_2$, 15 sec in $50H_2O$:1HF, and 15 min in $6H_2O$:1HCl:$1H_2O_2$ (SC-2) at 80°C. As this step left the bonding surfaces hydrophilic, a 1 minute immersion in $10H_2O$:1HF was employed to remove surface oxide and leave the surface H-passivated and strongly hydrophobic. The wafer pairs were then bonded at room-temperature and annealed in N_2 at 800 °C for 2 hours to strengthen the bond. Layer transfer was accomplished via mechanical grinding and subsequent etching in a 20wt% KOH solution to remove the backside of the seed wafer and the low-Ge content portion of the graded buffer. Previous work has shown that the narrowing of the SiGe band gap and the SiGe/electrolyte band alignment leads to a natural etch stop for relaxed $Si_{1-x}Ge_x$ at x~0.20 (22). The remaining SiGe layers were subsequently removed using a SiGe-selective dHF:HNO_3:CH_3COOH-based etch, where dHF is a dilute HF solution (100 H_2O:1 HF) thus generating the final SSOS structure. Such solutions have been shown to have a selectivity of greater than 100 over Si (23).

Plan-view and cross-section transmission electron microscopy (PVTEM and XTEM, respectively) were performed in JEOL 2000FX and 2010FX microscopes to inspect the structural quality of the strained-Si/Si interface. Secondary ion mass spectrometry was used to measure the Ge concentration in the transferred Si layer and tapping-mode atomic force microscopy (TM-AFM) was used to measure the surface roughness of the structure. Asymmetric {224} triple-axis x-ray diffraction was used to determine composition and misorientation within the structure.

III. Results and Discussion

Shown in Figure 2 are cross-sectional transmission electron microscopy images of the SSOS structure (a) before and (b) after SiGe removal. The arrows shown in Figure 2(a) indicate the location of misfit dislocations with line directions normal to the image plane. Note the average dislocation spacing of these dislocations is approximately 40 nm. The RMS surface roughness of the structure after mechanically grinding and KOH etching was determined via TM-AFM to be approximately 30nm over a 25µm×25µm area, with the crosshatch pattern that is characteristic of relaxed SiGe buffer layers reappearing due to the anisotropic nature of the KOH etch. Shown in Figure 2(b) is the final strained-Si on Si (SSOS) structure, demonstrating the complete removal of the SiGe layer after grinding and etching. At the inset of Figure 2(b) is a high-resolution TEM image of the bond interface, which indicates the lack of an intermediary oxide layer. The RMS surface roughness of the strained-Si after SiGe removal was approximately 1.9 nm for a 10µm×10µm TM-AFM scan, signifying excellent surface quality. We note here that although we have achieved creating SSOS, several regions of the strained-Si were breached during the removal of the SiGe layer, and therefore complete coverage of the strained-Si layer on Si was not obtained. With further process improvements, we believe full-wafer coverage is possible.

Shown in Figure 3 is a bright field PVTEM image of the strained-Si/Si interface. We observe a pattern of mostly orthogonal lines running in <011>-type directions under the given diffraction condition. Because the interface between strained-Si and Si is formed through bonding, we expect that an edge dislocation array will be present at the interface, with an interdislocation spacing corresponding to the difference in the lattice spacing between the strained-Si layer and the Si substrate. As the in-plane lattice spacing of the strained-Si layer should be equivalent to that of relaxed $Si_{0.76}Ge_{0.24}$, the edge dislocation array is expected to have a spacing of $S=b_{SiGe}/\delta=0.3877nm/.0094=41.2nm$. Shown in Figure 4 are images of the interface under the two <022>-type reflections for the plan view image. It is clear from Figures 3 and 4 that the dislocation spacing is ~40nm, close to the expected spacing considering that the interface will invariably contain a slight twist and tilt due to the variability in wafer miscut and the alignment of <011> directions during bonding.

Recent work has shown that misfit dislocations at the strained-Si/SiGe interface can create large off-state leakage currents by greatly enhancing source drain dopant diffusion (24). The interface array in SSOS differs greatly from the typical interface dislocations at the strained-Si/SiGe interface; however, their effect on transistor devices is unclear. A future area of research in SSOS will be to determine the properties of the interface dislocations in order to either minimize any deleterious enhanced diffusion or exploit such diffusion in a controlled fashion.

An important consideration for any device utilizing the SSOS heterostructure is the internal band alignment of the structure due to the bond interface. Previous reports of similar strained-Si structures grown on relaxed SiGe buffers with similar levels of strain have shown that the strained-Si channel behaves as an electron well with a depth of approximately 130-200 meV (25). The bandgap of such strained-Si layers has also been determined to be approximately 1 eV. Based on these previous determinations of the band alignment of strained-Si relative to bulk Si, one can speculate on the likely internal band alignment of the SSOS heterostructure. The schematic shown in Figure 6 is our suggested representation of the SSOS band alignment.

The internal band alignment predicted in Figure 6 is unique. Historically, abrupt changes in bandstructure at interfaces have always been accomplished by employing different materials, perhaps the most classical example being the GaAs/AlAs system. However, with SSOS we are likely to see abrupt changes in bandstructure in a chemically homogeneous system, which does not exist in nature and has been created here for the first time.

IV. Conclusion

Strained silicon on silicon (SSOS) substrate technology has been presented, and the method described allows for the fabrication of a well controlled, epitaxially-defined, strained-Si layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. PVTEM reveals a network of misfit dislocations with an average spacing of approximately 40 nm, a value consistent with an abrupt interface between bulk Si and strained-Si transferred from a relaxed $Si_{0.76}Ge_{0.24}$ template. The expected bandstructure of the SSOS structure, coupled to its superior thermal conductivity near the active device region, should make SSOS a useful platform for high-power MOS applications.

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References

[1] E. A. Fitzgerald, Y.-H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y.-J. Mii, and B. E. Weir, *Appl. Phys. Lett.* **59**, 811 (1991).

[2] Y.-J. Mii, Y.-H. Xie, E. A. Fitzgerald, D. Monroe, F. A. Thiel, B. E. Weir, and L. C. Feldman, *Appl. Phys. Lett*. **59**, 1611 (1991).

[3] E. A. Fitzgerald, Y.-H. Xie, D. Monroe, P. J. Silverman, J. M. Kuo, A. R. Kortan, F. A. Thiel, and B. E. Weir, *J. Vac. Sci. Technol. B* **10**, 1807 (1992).

[4] J. Welser, J. Hoyt, S.-I. Takagi, and J. F. Gibbons, Tech. Dig. - Int. Electron Devices Meet. 1994, 373 (1994).

[5] M. T. Currie, C. W. Leitz, T. A. Langdo, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, *J. Vac. Sci. Technol. B* **19**, 2268 (2001).

[6] Y.-H. Xie, D. Monroe, E. A. Fitzgerald, P. J. Silverman, F. A. Thiel, and. G. P. Watson, *Appl. Phys. Lett*. **63**, 2263 (1993).

[7] G. Hock, E. Kohn, C. Rosenblad, H. von Kanel, H.-J. Herzog, and U. Konig, *Appl. Phys. Lett.* **76**, 3920 (2000).

[8] C. W. Leitz, M. T. Currie, M. L. Lee, Z.-Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald, *Appl. Phys. Lett.* **79**, 4246 (2001).

[9] M.L. Lee and E. A. Fitzgerald, *Appl. Phys. Lett.* **83** (20), 4202 (2003).

[10] T. A. Langdo, M. T. Currie, A. Lochtefeld, R. Hammond, V. K. Yang, J. A. Carlin, C. J. Vineis, G. Braithwaite, H. Badawi, M. T. Bulsara, and E. A. Fitzgerald, IEEE International SOI Conference Proceedings, 2002, p. 211.

[11] S. Fukatsu, Y. Ishikawa, T. Saito, and N. Shibata, *Appl. Phys. Lett.* **72**, 3485 (1998).

[12] G. Taraschi, T. A. Langdo, M. T. Currie, E. A. Fitzgerald, and D. A. Antoniadis, *J. Vac. Sci. Technol. B* **20**, 725 (2002).

[13] L. J. Huang, J. O. Chu, D. F. Canaperi, C. P. D'Emic, R. M. Anderson, S. J. Koester, and H.-S.-P. Wong, *Appl. Phys. Lett.* **78**, 1267 (2001).

[14] Z. Cheng, G. Taraschi, M. T. Currie, C. W. Leitz, M. L. Lee, A. Pitera, T. A. Langdo, J. L. Hoyt, D. A. Antoniadis, and E. A. Fitzgerald, *J. Electron. Mater.* **30**, L37 (2001).

[15] T. Tezuka, N. Sugiyama, and S. Takagi, *Appl. Phys. Lett.* **79**, 1798 (2001).

[16] Arthur J. Pitera, G. Taraschi, M. L. Lee, C. W. Leitz, Z. -Y. Cheng, E. A. Fitzgerald, *Jour. of the Elec. Soc.,* **151** 7 (accepted for publication).

[17] D. A. Dallmann, K. Shenai, IEEE Transactions on Electron Devices, **42**, 489 (1995).

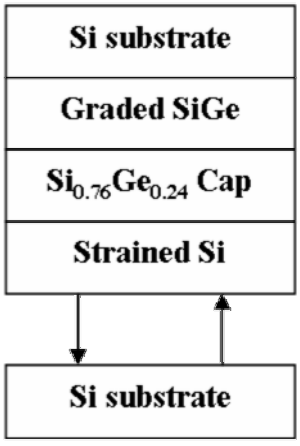
[18] E. Kasper, *Properties of Strained and Relaxed Silicon Germanium*, (INSPEC, London, 1995), p. 70.

[19] A. L. Caviglia, A. A. Iliadis, *IEEE Elec. Dev. Lett.* **14**, 133 (1993)

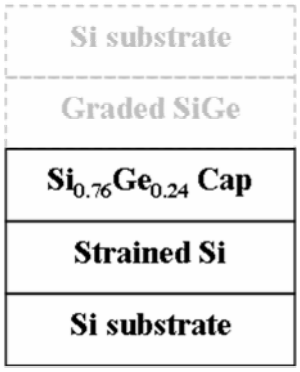
[20] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, M. I. Flik, *IEEE Transactions on Electron Devices,* **41**, 69 (1994).

[21] C. W. Leitz, M. T. Currie, A. Y. Kim, J. Lai, E. Robbins, E. A. Fitzgerald, and M. T. Bulsara, Journal of Applied Physics, **90** (6), 2730-2736 (2001).

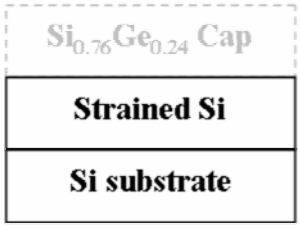
[22] K.C. Wu, P. Shay, J.T. Borenstein, MRS Symposium Proceedings, 197 (1996).
[23] G. Taraschi, A. J. Pitera, L. M. McGill, Z. Y. Cheng, M. L. Lee, T. A. Langdo, and E. A. Fitzgerald, Mater. Res. Soc. Symp. Proc. 745, N4.7.1 (2002).
[24] J. G. Fiorenza, G. Braithwaite, C. W. Leitz, M. T. Currie, J. Yap, F. Singaporewala, V. K.Yang, T. A. Langdo, J. Carlin, M. Somerville, A. Lochtefeld, H. Badawi, M. T. Bulsara, Semi. Sci. Tech 19, L4 (2004).
[25] R. People and J. C. Bean, Appl. Phys. Lett. **48,** 538 (1986).



(a) Wafer bond and anneal

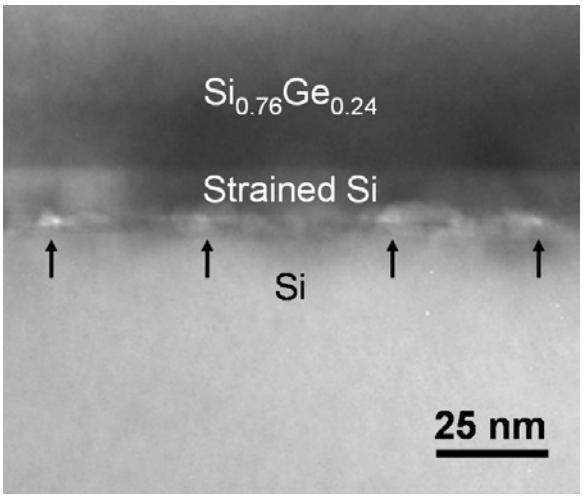


(b) Substrate/buffer removal



(c) $Si_{0.76}Ge_{0.24}$ cap removal

Figure 1: SSOS fabrication process showing (a) wafer bond and anneal, (b) structure after Si substrate and SiGe graded buffer removal, and (c) structure after removal of the $Si_{0.76}Ge_{0.24}$ cap.



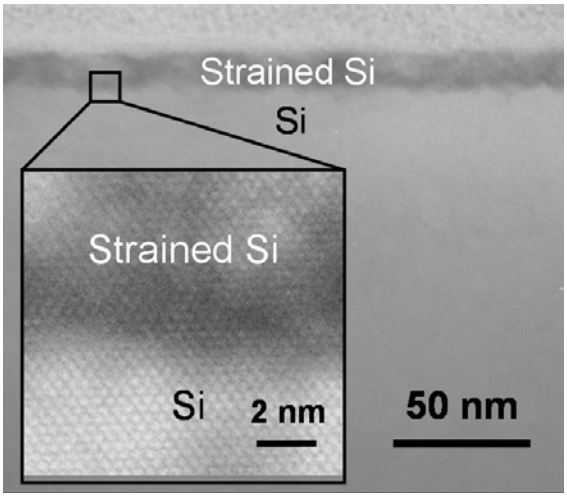


Figure 2: Cross-sectional TEM images (a) before and (b) after SiGe layer removal. Arrows in (a) indicate the location of misfit dislocations at the interface

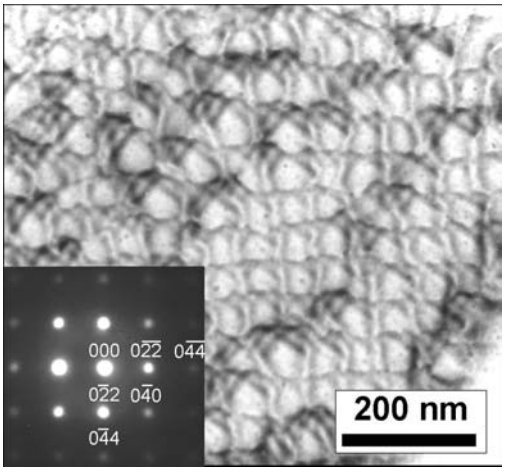
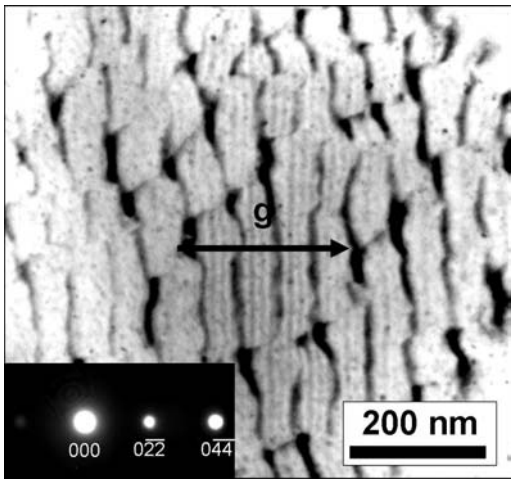


Figure 3: Plan-view transmission electron microscopy image of the strained-Si/Si interface under bright field conditions.



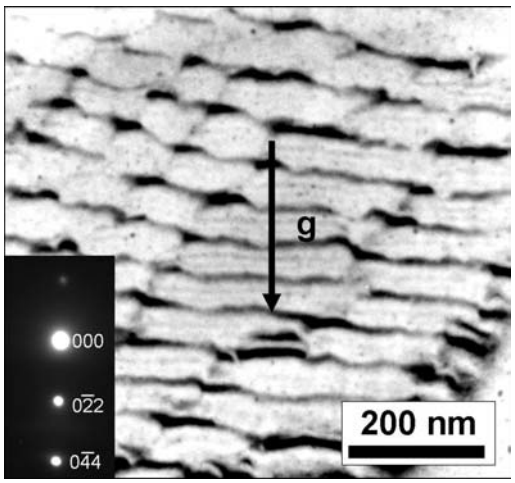


Figure 4: A series of plan view TEM micrographs of the same region as in Fig. 3, taken using different g conditions for Burgers vector analysis of the dislocation network: (a) g=0-4-4 and (b) g=0-44 conditions.

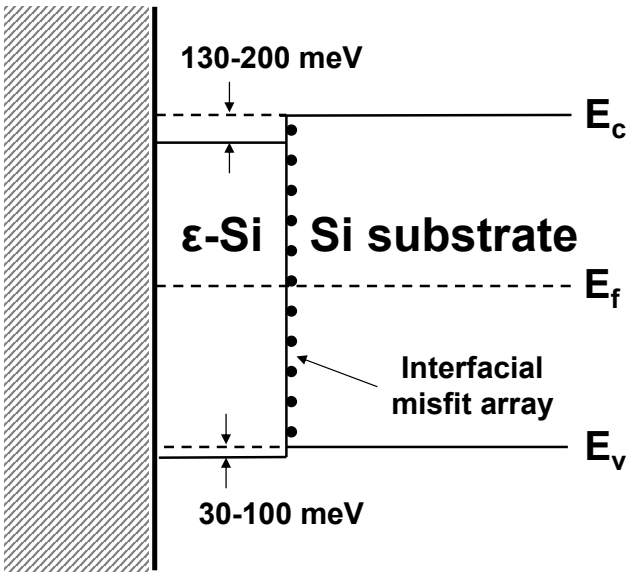


Figure 5: Schematic of the expected internal band alignment of the undoped strained-Si on Si (SSOS) heterostructure.