Compressively Strained Ge Trigate p-MOSFETs

By

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B.S. University of Illinois Urbana-Champaign 2010

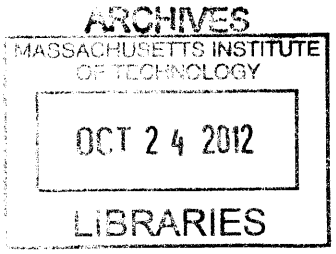
Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

at the

Massachusetts Institute of Technology



September 2012

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Abstract

State of the art MOSFET performance is limited by the electronic properties of the material that is being used, silicon (Si). In order to continue performance enhancements, different materials are being studied for the extension of Si CMOS. One of the materials of interest, particularly for p-MOSFETs, is Ge because it has very high intrinsic hole mobility. Further improvements in hole mobility can be achieved by straining the material. At the same time it is important to study strained Ge transport in device architectures such as trigate MOSFETs. These devices offer the potential for better scalability than planar MOSFETs via improved electrostatics. The investigation of hole mobility in strained Ge trigate ("nanowire") p-MOSFETs is the focus of this work.

To study the effects of strain on Ge as a p-channel material, Strained Germanium Directly on Insulator (SGDOI) substrates were fabricated. The substrates were strained to ~2.4% using lattice mismatch which originates from the growth of Ge on a relaxed $Si_{0.6}Ge_{0.4}$ epitaxial layer. A biaxially strained SGDOI substrate was patterned to form Ge nanowires which were measured by Raman spectroscopy to investigate the strain relaxation from the free surface. Another SGDOI substrate was used for nanowire trigate p-MOSFET fabrication. The semiconductor layer structure for the devices consisted of 10 nm-thick strained-Ge with a 5 nm-thick strained-Si cap. On-chip biaxially strained MOSFETs were compared to asymmetrically strained Ge nanowire devices. Significantly improved mobilities (~2x) were observed for nanowire devices with a width of 49 nm compared to the on-chip biaxially strained Ge controls. These mobilities are ~15x over Si universal hole mobility. The impact of strain on the transport of holes in long channel devices is also studied as a function of nanowire width. Mobility decreased for narrower nanowire MOSFETs, likely associated with increased sidewall line edge roughness scattering in narrow lines.

Acknowledgements

I would first like to thank those who made this work possible. Because I could never have been here without the support of my previous advisors, John Weaver and Xiuling Li, respectively I would like to express my gratitude for the investment that they have previously put in me. I want to first express my gratitude to Judy Hoyt for providing me with guidance and the opportunity to do the science that has been explored in this thesis. I would also like to thank the students before me who have made this work possible: Pouya Hashemi, who developed the processes which I have used to make the devices, and Leonardo Gomez and the other students before him who developed the wafer bonding processes used in this work. Furthermore, I want to express my appreciation for Gary Riggott who has done the epitaxial growth for this work, and the MTL staff who have made the remaining processing possible. Finally, I would like to thank Jamie Teherani for his contributions, the simulations that I have used in my thesis, which were invaluable to understanding the physics in the devices from this study.

Besides those I have directly named here, it is difficult to assign credit where it is due because of the long path that I have taken to get here; there are simply too many people who have influenced what I have become. Chronologically, I must concede thanks to the people who watched me grow; those who taught me to play, to make fire, to do science, and later to drink tea. But those who I must give the most credit are the ones that have directed me in the right direction although not academically. I should first thank those before Illinois for their part in maintaining my sanity with their hospitality, rides and coffee. They will always influence me for better or for worse. I also appreciate those in Illinois and all my mentors who have guided me in research and beyond. Namely, I want to express my appreciation to my friends who advised me at the Y, shared their apartment my last year and formed the beehive. Finally, I would like to express my appreciation to those who I currently spend time with including my groupmates, the people I have spoken to on the 6th floor of MTL and the friends who have already left MIT.

Table of Contents

List of Figures

Chapter 1: Motivation and Background

This chapter details the physics and motivation for the experiments performed in this thesis. First, motivation for germanium, Ge, as a replacement channel material will be discussed. Second, the effects of strain on carrier transport will be introduced. Finally, an explanation for the non-planar architecture of the field effect transistor will be given. The basic approach for this work will be outlined at the end of this chapter.

1.1: Motivation for Ge as a Channel Material

Complimentary Metal-Oxide-Semiconductor (CMOS) has been scaled in size for the past 35 years to increase the density of devices on an integrated circuit and to improve the performance of the devices. The International Technology Roadmap for Semiconductors (ITRS) shows aggressive scaling for silicon (Si) but also notes the need for new channel materials beyond Si to increase the performance [1]. The switching speed of a logic gate is dependent upon the transistor on current. The on current, normalized by width, can be evaluated from the following equation:

$$\frac{I_{on}}{W} \sim \frac{1}{L}\mu_{eff} C_{ox}(V_{DD} - V_{th})^2 \quad (1)$$

where I_{on} is the on-state current, W is the device width, L is the channel length, μ_{eff} is the effective mobility of the carriers, C_{ox} is the gate oxide capacitance, V_{DD} is the operating voltage and V_{th} is the threshold voltage. In the past, the gate length, and C_{ox} has been scaled in order to increase the device density, and performance of MOSFETs, but the potential for performance improvement due to gate length scaling has reached its limit due to carrier velocity limits and short channel effects. The maximum V_{DD} is also limited by the power dissipation, proportional to V_{DD}^2, because of the high density of the devices on the wafer [2]. Recent scaling has been to

decrease power for mobile applications; in order to maximize performance for low power devices, the mobility should be maximized. Therefore, a key method to continue improving device performance is increasing the effective mobility which can be done by changing channel materials or applying strain.

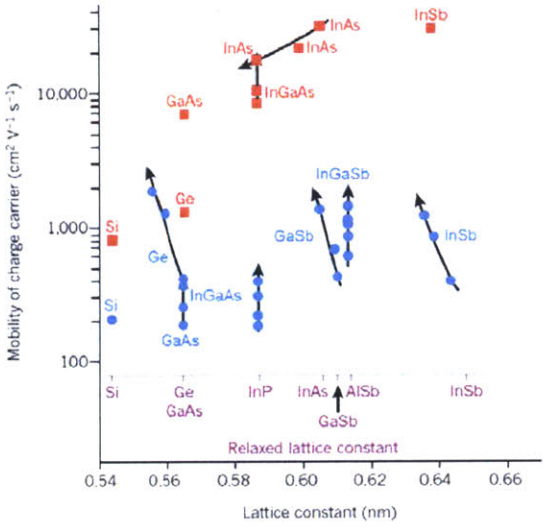

Fig. 1.1.1. The Hall mobilities of (blue) holes and (red) electrons in various materials compared to the lattice constant of the material. The arrows indicate decreasing or increasing lattice constant due to strain that has been applied. This figure is courtesy of Jesus Del Alamo [3].

A wide variety of material choices exists, including column III-column V (III-V) semiconductors and elemental semiconductors as replacements for Si in future CMOS. Their respective mobilities can be seen in Fig. 1.1.1. Ge has the highest hole mobility and is likely to be the simplest to integrate with current Si technology because SiGe is already used in state of art Si p-MOSFETs [4]. Recent work demonstrating high hole effective mobility in strained Ge quantum wells illustrates the promise of Ge FETs [5-7]. The high mobility of Ge should translate to higher currents, and possibly lower V_{DD} implying faster switching and lower power.

1.2: Effects of Strain on the Carrier Transport

Strain can also be applied in order to improve the carrier transport of holes. There are several methods of applying strain which include dielectric stressors [8], embedded source and drain stressors [4], and lattice mismatch strain. Dielectric spacers use a highly stressed thin film which deforms the material underneath it. Strain transfer from the thin film into the source and drain stresses the channel. Embedded source and drain stressors use a film of a different lattice constant to stress the channel. The source and drain stressors are epitaxially grown, and to obtain compressive strain, a larger lattice constant (SiGe) is grown replacing the Si that was previously there. The SiGe is compressively strained and this strain can be transferred into the channel in short channel devices. Finally, lattice mismatch strain from epitaxial growth of layers under the channel can be used to induce strain. By growing a larger or smaller lattice constant, a biaxial strain can be applied. In order to generate the uniaxial strain which is attributed to the two previous methods, nanoscale patterning can be used to relax the strain in one dimension [9, 10].

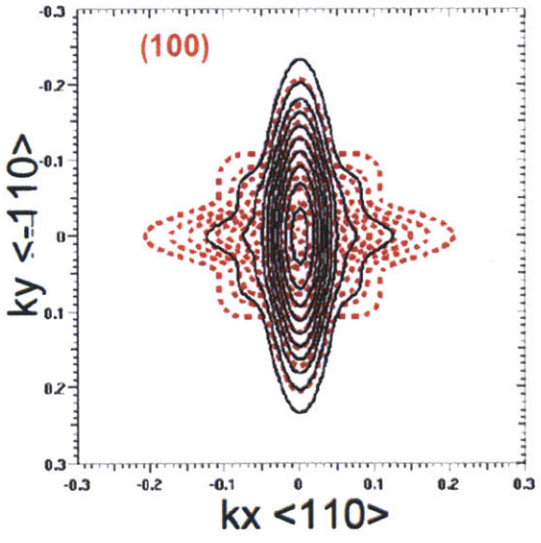

Fig. 1.2.1. The theoretical constant energy contours for Ge for a (100) plane (red) without strain and (black) with compressive strain in the <110> direction [11]. With compressive strain, the

spacing of the energy contours decreases signifying higher hole velocity. © Packan et al. 2008 IEEE.

Strain warps the energy bands (Fig. 1.2.1), and the proper strain (compressive for holes and tensile for electrons) can produce a higher mobility in the transport direction (typically [110]) [11]. Fig. 1.1.2 shows the effect of compressive strain on the Ge valence band. As the energy contours of the valence band move closer together, the velocity of the carriers increase since velocity is proportional to dE/dk. Uniaxial strain has been shown to improve hole mobility more than biaxial strain [12], because it generally has a larger impact on the curvature of the E-k relationship. The carrier effective mass is inversely proportional to the curvature of the E-k diagram.

1.3: Non-planar Device Architecture for Better Short-Channel Device Performance

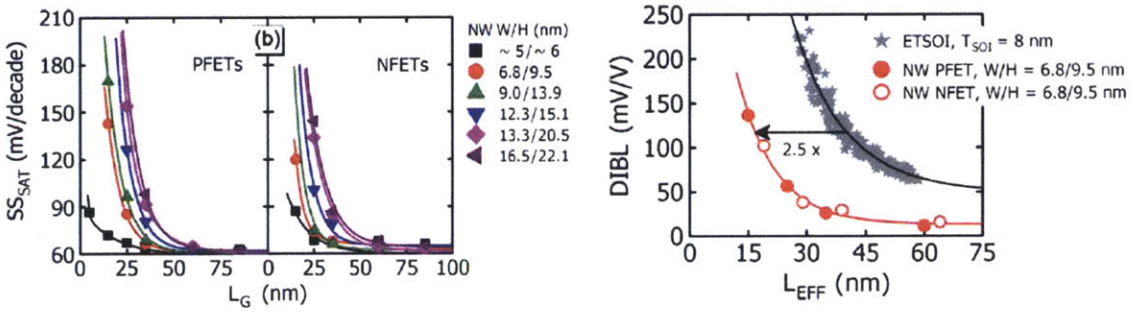

Fig. 1.3.1. (left) The subthreshold swing, SS, as a function of nanowire width and height and (right) the drain induced barrier lowering (DIBL) of nanowire FETs versus extremely thin silicon on insulator (ETSOI). The DIBL is greatly reduced for nanowire FETs of approximately the same thickness [13]. © Bangsaruntip et al. 2010 IEEE.

As devices are scaled, the planar architecture suffers from poor electrostatic control. Evidence of this lies in Intel's decision to switch to a trigate architecture [4]. The non-planar architecture, at the same body thickness, is superior to the planar architecture due to

electrostatics because the gate wraps around the channel (Fig. 1.3.1). In order to maintain a constant drain induced barrier lowering (DIBL) and subthreshold slope in short-channel MOSFETs, the channel thickness needs to be decreased with decreasing gate length. In order to maintain a reasonable thickness, the channel is expected to evolve into a non-planar architecture.

1.4: Approach to Beyond Si High Mobility p-MOSFETs

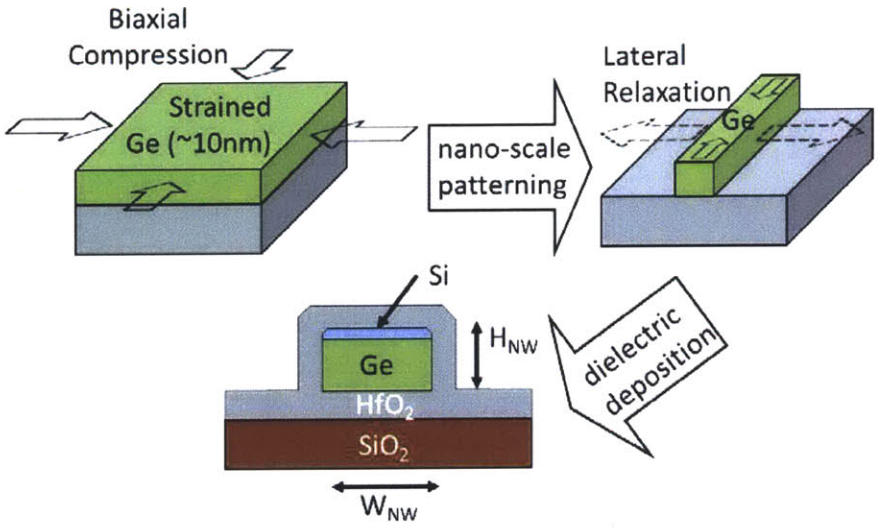

Fig. 1.4.1. A biaxially strained Ge film on insulator is subject to nanoscale patterning. The resulting Ge bar relaxes laterally resulting in asymmetric strain. After nanowire formation, dielectric for the gate is deposited resulting in a trigate nanowire.

The approach used in this work consists of first growing Ge that is biaxially strained from lattice mismatch on a sacrificial Si wafer. HfO_2 and SiO_2 is deposited on top of the epitaxially grown layers which include multiple etch stops. The sacrificial wafer with these epitaxial layers is bonded to a thermally oxidized wafer. The etch-stop layers and the sacrificial Si wafer are removed through chemical etching and mechanical grinding, resulting in a biaxially strained film on insulator. The biaxially strained Ge film on insulator is patterned into thin bars resulting in

relaxation perpendicular to the bar (Fig. 1.4.1). The gate for the MOSFET will wrap around the partially relaxed nanowire on the insulator resulting in a trigate p-MOSFET. The strain and high mobility channel material is used to improve the transport in the channel, and the non-planar architecture is utilized to enable future gate length scalability.

Chapter 2: Fabrication of Biaxially Strained Substrates and Trigate p-MOSFETs

This chapter details the fabrication of Strained Germanium Directly On Insulator (SGDOI) substrates. The substrate fabrication precedes the creation of test structures used to measure the strain by Raman scattering, as well as the device run in which asymmetrically strained Ge trigates and on-chip biaxially strained Ge planar ultra-thin body p-MOSFETs were fabricated. The epitaxial growth of the substrates was performed in an Applied Materials Epi Centura^{TM} reactor. The fabrication of devices was performed in the Microsystems Technology Laboratory at MIT unless otherwise specified.

2.1: Bond and Etch-back Process

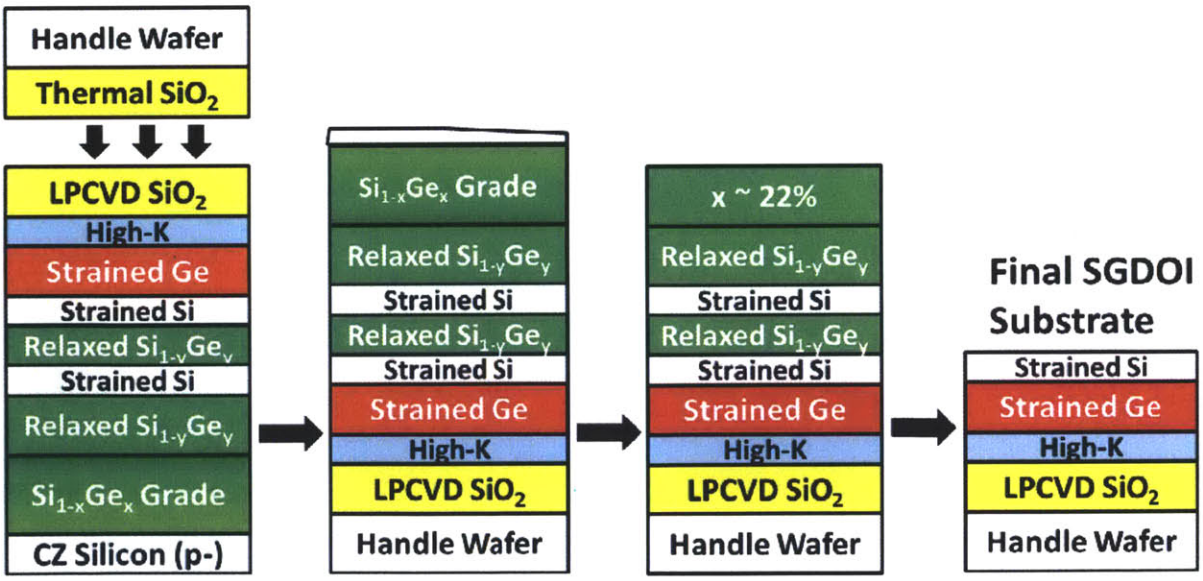

Fig. 2.1.1 Schematic of bond and etch-back process used to form Strained Ge Directly on Insulator 6" substrates. 10 nm-thick strained-Ge is grown pseudomorphic to a relaxed x=40% $Si_{1-x}Ge_x$ layer. After bonding, all layers of the epitaxial wafer except the strained-Si/strained-Ge

are removed. The bottom high-k layer (HfO_2) acts as an etch stop during nanowire formation and can passivate the back Ge-dielectric interface.

Substrate fabrication for SGDOI wafers is similar to previous strained wafers on insulator, i.e. Strained Si on Insulator (SSOI) and Heterostructure on Insulator (HOI) [14, 15]. The epitaxially grown, etch-back structure (schematic in Fig. 2.1.1) used for SGDOI fabrication consists of a graded $Si_{1-x}Ge_x$ buffer layer with a final Ge composition x~0.4. An 11-nm thick strained-Si etch stop was grown on top of the relaxed buffer layer. A final 100-nm thick etch stop of $Si_{1-x}Ge_x$ was grown below 10-nm strained-Si and 10-nm strained-Ge (the final device layers). For reference, the epitaxial growth number of a representative wafer is 6716. The complete flow for the band and etch-back process is shown in Appendix A and a schematic of the process is illustrated in Fig. 2.1.1.

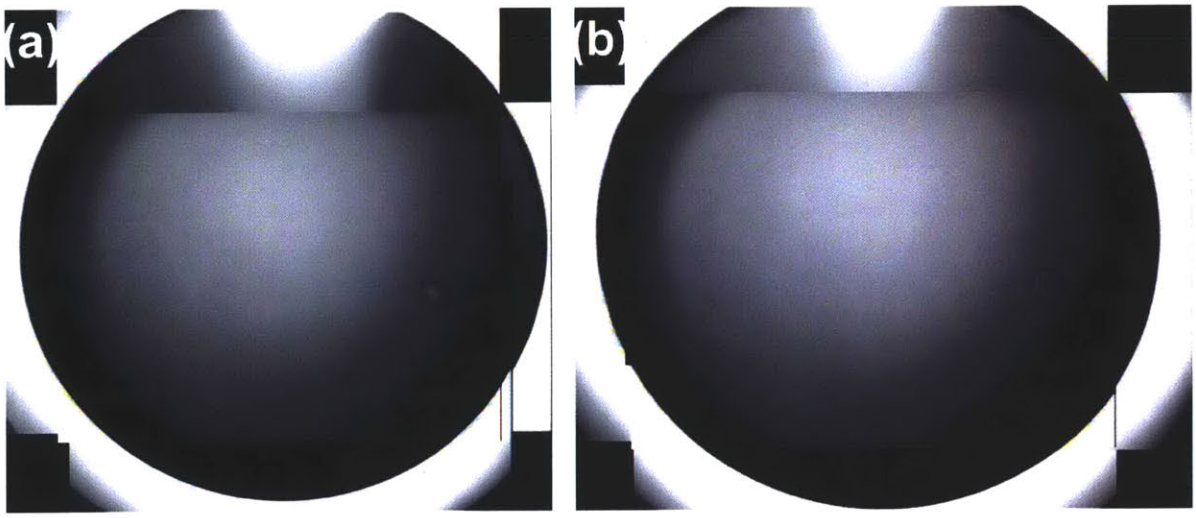

Fig. 2.1.2 Infrared camera images of a 6" diameter wafer pair after (a) wafer bonding, and (b) a 5-hour 300°C post-bond anneal. The shape of the defect is circular after annealing.

Defects and voids in the wafer after bonding can be seen using an infrared camera. The voids are often circular in nature, and can sometimes be removed mechanically using a wafer wand by pushing the air bubble to the edge. Despite the ability to mechanically remove an air

bubble, the associated defect (e.g. dust particle) is usually permanent. Images of a bonded wafer before and after annealing are seen in Fig. 2.1.2.

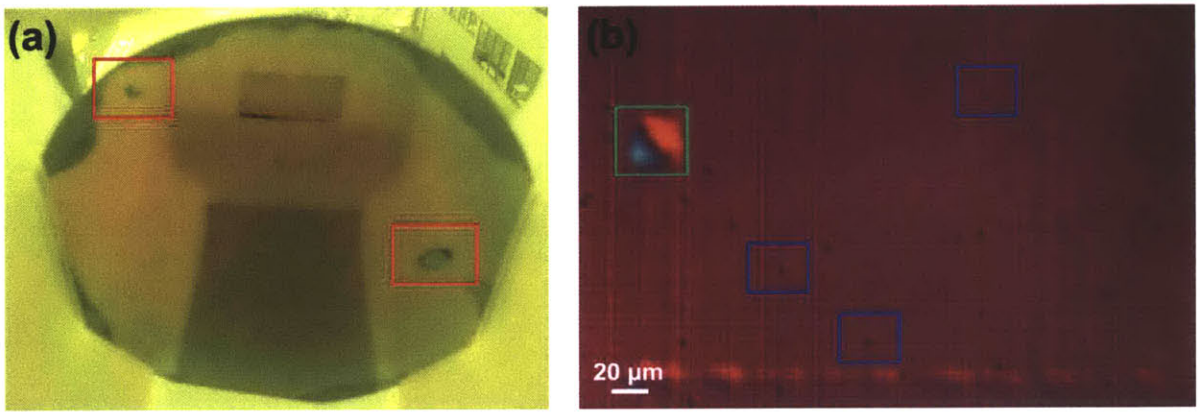

Fig. 2.1.3 (a) Camera image of the wafer in Fig. 2.1.2 after the final etch-back step. The bonding defects, marked by red squares, end up as delaminated regions of the film after etching. The edges of the wafer also have significant portions that are delaminated. (b) A Nomarski image illustrates microscopic defects caused by the final etch. Features circled in blue are microscopic defects caused by etching, and the feature circled in green is a microscopic bonding defect.

Following the bond and etch-back process flow outlined in Appendix A, images of a finished SGDOI substrate are visible in Fig. 2.1.3. The bonding defects, circled in red in Fig. 2.1.3 (a), are clearly evident in the full-wafer image because the defect areas peel off during the etch-back process resulting in a circular void. The Nomarski microscope image in Fig. 2.1.3 (b) reveals the presence of additional defects that are not evident in the full-scale image. There are two types of defects in this image: bonding defects (green) and pinhole defects (blue). The bonding defects propagate along the cross-hatch (the surface undulations that produce the linear features along the [110] directions on the wafer surface [16]), suggesting the possibility that additional CMP may be necessary to remove the cross-hatch of the x=40 % $Si_{1-x}Ge_x$ substrate.

The pinhole defects have a density ranging from $1x10^6$ cm^{-2} to $1x10^7$ cm^{-2} depending upon the location on the wafer, and did not appear on the wafer until after the final etch step. The defects are square in nature and are a few microns in width. In order to understand the origin of these defects, high resolution AFM images were taken. An AFM image of several defects (Fig. 2.1.4) shows that the size of the defects is ~5 μm. The edges of the square are aligned 45 degrees with respect to the cross-hatch (<110>) which is the <100> direction. Upon increasing the magnification, a small, 100 nm pinhole is observed at the center of the defect. The height difference between the pinhole and the rest of the 5 μm defect suggests that the Ge under the Si was removed by the etchant which penetrated through the pinhole. The density and size of the defects suggests that the final etch selectively attacks the threading dislocations resulting in defects in the SGDOI substrate. In the future, the SGDOI defect density can be reduced by using a less dislocation-selective etchant for the final etch step.

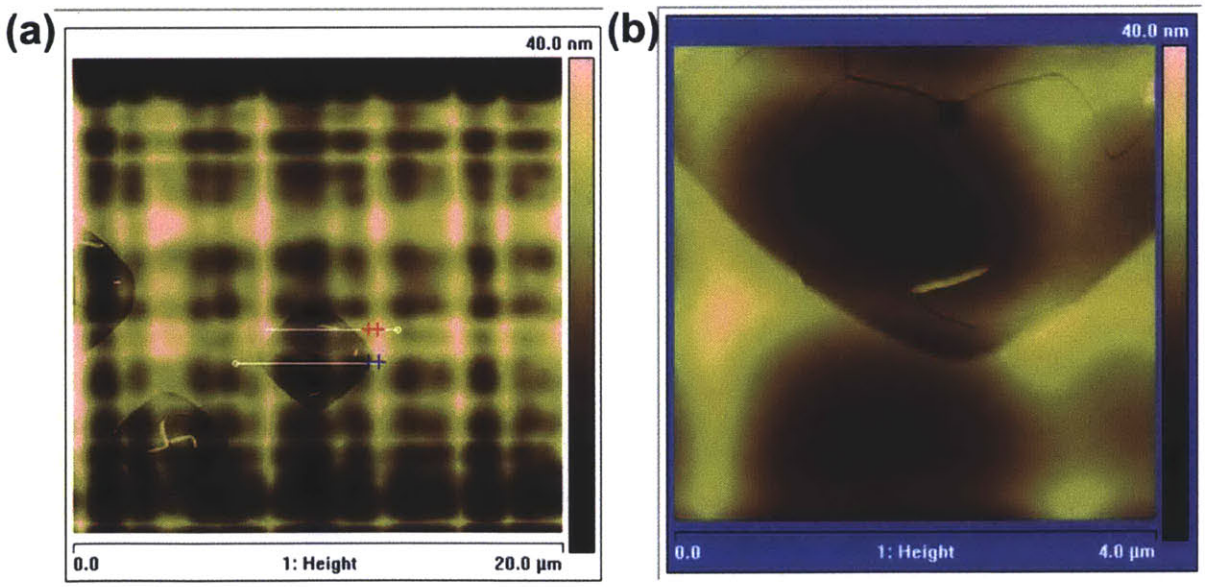

Fig. 2.1.4. (a), (b) AFM images of the microscopic (~5 μm) defects caused by the final etch step. The <110> cross-hatch is in the x and y directions of the image, and the defects are 45 degrees

relative to the x-axis. This suggests that the defects propagate in the <100> directions by etching from a small square.

2.2 Fabrication of Nanopatterned Structures for Raman Characterization

To achieve the desired asymmetric strain, nanowire structures are fabricated via e-beam lithography. As previously mentioned, the free-surfaces generated from the etching of the nanowires allow for relaxation of the transverse strain, ε_x, creating asymmetric strain. In order to experimentally measure the strain relaxation, Raman test structures were fabricated following procedures similar to Ref. [10].

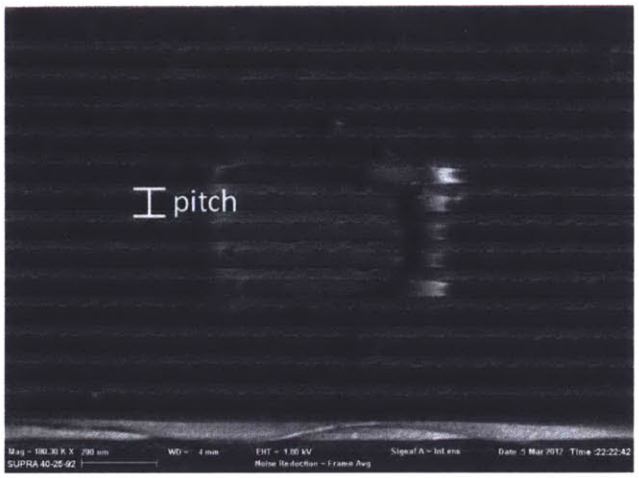

Fig. 2.2.1 SEM image of a Raman bar structure with nanowire width, W_{NW}=25 nm and a 3:1 pitch:width ratio. The square feature in the center of the micrograph is an artifact of the imaging.

Raman test structure fabrication begins with a biaxially strained SGDOI wafer. The as-grown strained Si (s-Si) and strained Ge (s-Ge) thicknesses are nominally 10 nm and 10 nm, respectively. The layer thicknesses are equivalent to those used in strained Ge p-MOSFET device fabrication, but the Raman substrates did not undergo a process to etch alignment markers, which thins the s-Si. In order to mimic this aspect of the device process, the sample used for Raman was ashed for 5 minutes and then dipped in 50:1 DI:HF in an attempt to match the 5 nm

s-Si thickness on the devices, for accurate strain representation. Following this thinning of the s-Si layer, HSQ lines with a 2:1, 3:1 and 4:1 pitch:width ratio were patterned using e-beam lithography along with a large pad (25 x 25 μm) for a biaxially strained reference. The pattern was transferred into the semiconductor layers via dry etching to create the Raman bars. The HSQ was removed using 40 sec. of BOE (7:1 NH_4F:HF) and the Raman bars were imaged via SEM (Fig. 2.2.1). The fabrication of Raman bars with a tight spacing of 2:1 pitch:width ratio was unsuccessful due the un-optimized e-beam lithography dose.

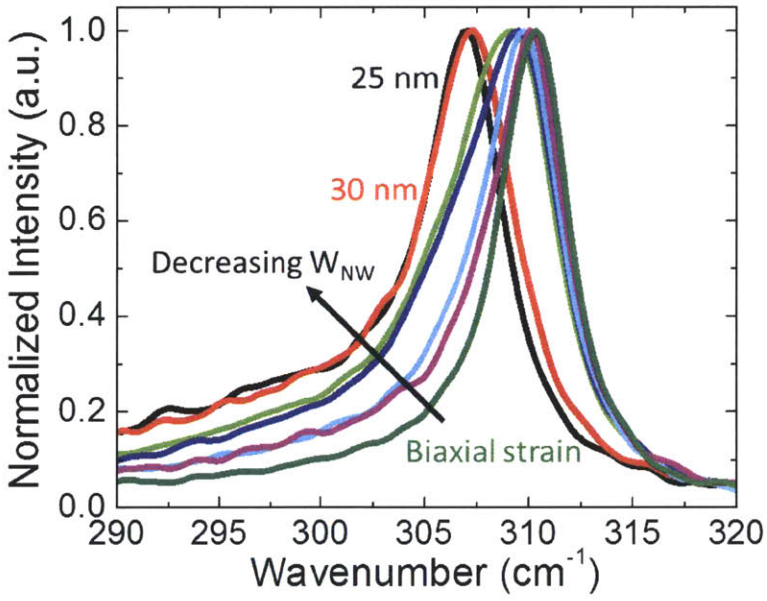

Fig. 2.2.2 Measured Ge Raman spectra for all W_{NW} and the biaxially strained SGDOI. The order of the Raman spectra along the direction of the arrow is biaxial, W_{NW}= 100nm, 80nm, 50nm, 40nm, 30nm, 25nm. The background of the spectra was taken to be the minimum intensity from 250 to 350 cm^{-1}. After background subtraction, the data was normalized to the Ge-Ge peak heigh. Raman data courtesy of Yuanwei Dong and Guangrui Xia.

Micro-Raman spectroscopy was performed at the University of British Columbia using a commercial Horiba micro-Raman setup with a polarized HeCd laser at 442nm. The spectral

resolution of the Raman setup is 0.03 cm^{-1} and the penetration depth is 300 nm which enables probing of the strain for both Si and Ge. The Ge spectra for different wire dimensions are illustrated in Fig. 2.2.2. For the large wires, $W_{NW} > 40$ nm, the Raman peak shifts very little as a function of wire width as seen in Fig. 2.2.3. The Raman peak position does not accurately represent the average strain of the nanowire, but instead, it represents the dominant strain in the nanowire. In order to fully capture the strain relaxation effect, the full width at half maximum (FWHM) was also analyzed. Broadening of the Raman peak is due to the summation of different strain levels into a single peak. Therefore, the more non-uniform the strain, the broader is the Ge-Ge Raman peak. The increase in FWHM with decreasing W_{NW} is caused by increasing non-uniformity in the strain profile. Below a certain width, the FWHM begins to decrease.

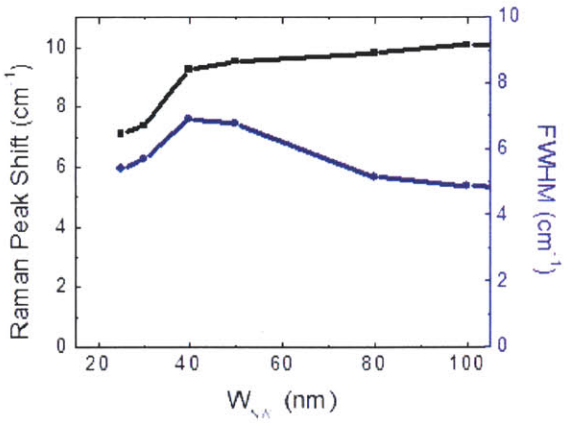

Fig. 2.2.3. Measured Raman peak shift relative to unstrained bulk Ge (black) and full width half maximum (blue) vs W_{NW}. The Raman peak shift and FWHM of the biaxially strained film is 10.3 and 4.05 cm^{-1} respectively.

In order to better understand the data from Raman spectroscopy, strain simulations were performed using nextnano^3 [17] by Jamie Teherani. A boundary condition of 2.4% compressive strain was forced at the Ge/buried oxide interface, which corresponds to a nominally x= 40% Si_{1-}

$_xGe_x$ relaxed buffer layer. Since the sides and top of the structure were defined as free surfaces, the strain in the simulated structure relaxes in order to minimize the total strain energy. Simulated strain profiles for W_{NW}= 26 nm and 49 nm nanowires illustrate non-uniform strain (Fig. 2.2.4).

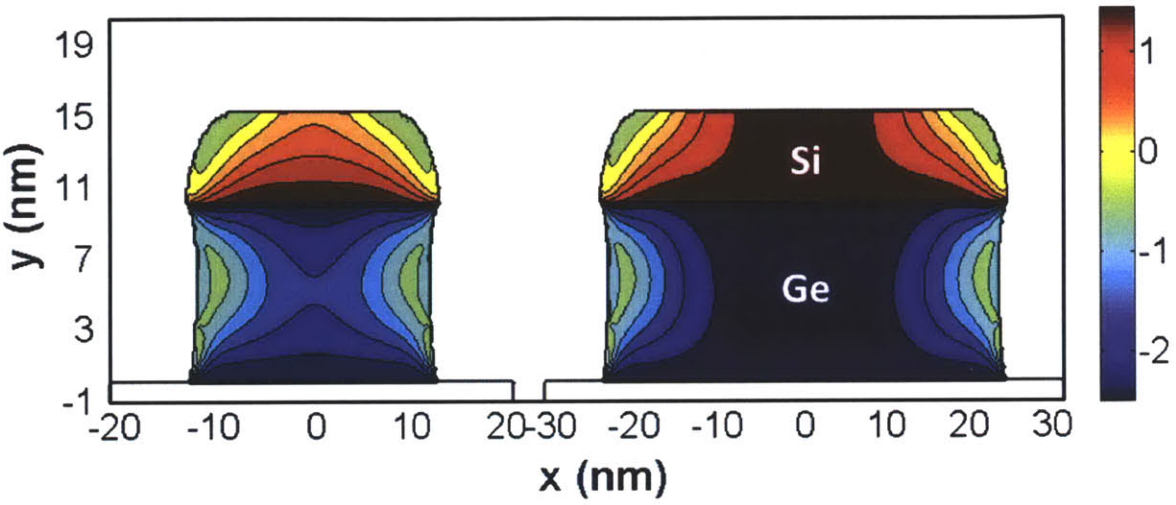

Fig. 2.2.4 Simulated transverse strain (ε_x) profiles (nextnano^3 [17]) for nanowires with W_{NW}=26 nm and 4 9nm respectively; color scale is in % strain. Near the sidewalls, the strain in the x-direction is relaxed from the initial value of -2.4%, derived from Ge grown on a 40% SiGe relaxed buffer layer. Simulations and figure courtesy of Jamie Teherani.

The relaxation of the transverse strain in the Ge nanowires occurs from the two sidewalls. The strain relaxes in a semicircular fashion from the sidewalls because of the s-Si cap above and the oxide below compressively strain the Ge layer. As the nanowire decreases in width from W_{NW}= 49 nm to 26 nm, the two lobes of relaxation converge in the middle of the wire eliminating the biaxial strain at the center. This results in the decrease of the measured Raman FWHM for W_{NW}<30 nm. Despite the uniformity of the strain in the center of the nanowire for W_{NW}=49 nm in Fig. 2.2.4, the strain is not fully biaxial at the center of the nanowire. Fig. 2.2.5 shows a cross-sectional cut of the simulated strain at the center of the Ge layer (y=5 nm)

illustrating that there is some degree of transverse strain relaxation for the majority of the wire. Even small amounts of strain asymmetry can greatly benefit the transport of carriers as seen in previous wafer-bending experiments [18].

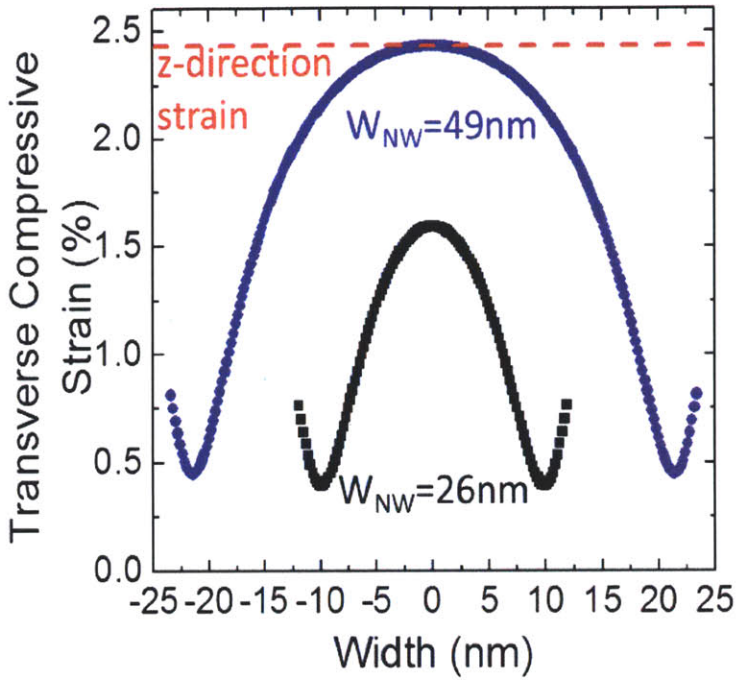

Fig. 2.2.5 Transverse strain (ε_x) profiles at y=5 nm for W_{NW}= 26 and 49 nm. The longitudinal strain (ε_z) is maintained for both cases. The strain is non-uniform and asymmetric ($\varepsilon_x \neq \varepsilon_z$) for both cases.

A comparison of the simulated profile with the experimentally measured strain from Raman spectroscopy is shown in Fig. 2.2.6, by relating the Raman peak shift to the average transverse strain (ε_x). The conversion from Raman peak shift relative to unstrained Ge to ε_x uses two simple assumptions: Raman peak shift is linearly proportional to the average strain and the longitudinal strain, ε_z, is equal to the biaxial strain. The relationship between Raman peak shift and strain is given by [19]:

$$\Delta\omega = -404\frac{(\varepsilon_x+\varepsilon_z)}{2} \quad (2)$$

where $\Delta\omega$ is the Raman peak shift relative to unstrained Ge, ε_x is the transverse strain and ε_z is the longitudinal strain which is 2.54% for the experimental samples. Because of the rough approximation in the measured strain and the difference in the calculated and measured biaxial strain, the measured and simulated average strains do not quite line up. However, the average strain sharply decreases at the same W_{NW} for both simulation and experiment suggesting that the strain profiles produced via simulation are reasonably accurate.

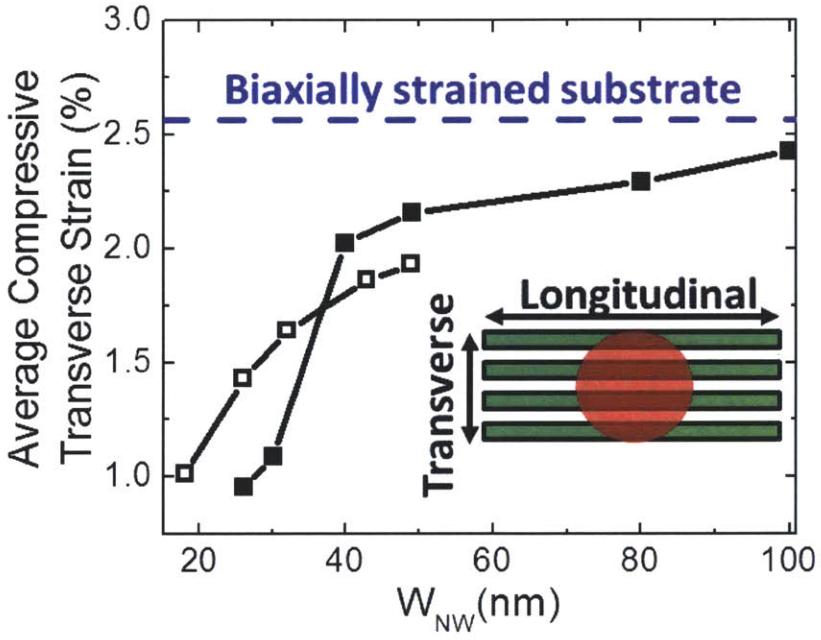

Fig. 2.2.6. Average transverse strain obtained from the Raman peak shift relative to unstrained Ge (solid symbols), and from the simulations shown in Fig. 2 (open symbols). A schematic of the Raman measurement setup is seen in the inset. Simulations courtesy of Jamie Teherani.

2.3: Ge Nanowire Trigate Fabrication

Ge trigate fabrication begins using a SGDOI wafer. The entire detailed process flow is provided in Appendix B. In order to align e-beam lithography to the photolithography, deep

(250nm) e-beam alignment markers must be etched through the HfO_2 etch-stop, which has been crystallized during the LTO densification anneal. One method to etch crystallized HfO_2 is to first use ion implantation to damage the HfO_2 and then to remove it using 50:1 DI:HF. A 5 keV, $4x10^{15}$ cm^{-2} boron implanation was performed using an photoresist mask in order to damage the HfO_2 and the substrate was dipped in 50:1 DI:HF. After a long HF dip (10 minutes), only 1 nm of HfO_2 was removed due to the lack of damage caused by the light boron atoms. A second photo mask was aligned to the previous one, and the sample was implanted once again using a 5keV, $4x10^{15}$ cm^{-2} BF_2 implant. After the second implant, the HfO_2 and part of the buried SiO_2 was removed in 50:1 DI:HF allowing the remaining steps to proceed.

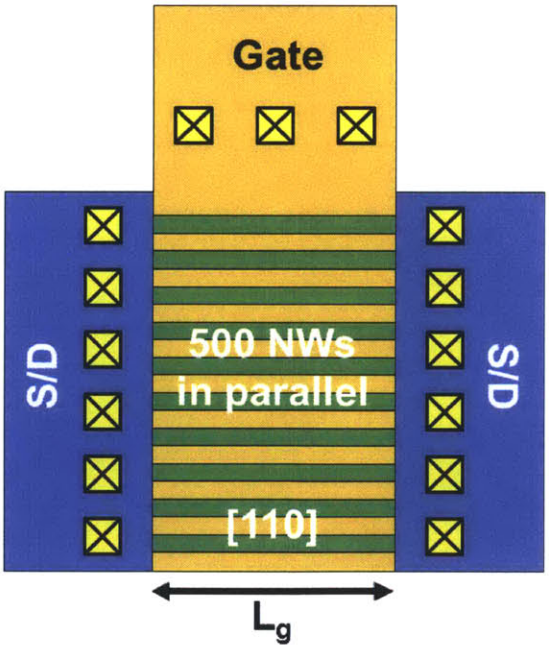

Fig. 2.3.1. Top-down schematic of the mobility-extraction trigate p-MOSFET.

The SGDOI was patterned into the device structure shown in Fig. 2.3.1 using a combination of e-beam lithography and photolithography. E-beam lithography is used to define the nanowires, and photolithography is used to define the source/drain pads. The device structure features 500 nanowires connected in parallel to the source/drain (S/D) pads. The S/D vias are

nominally 500 nm away from the channel. After e-beam patterning, the nanowires were imaged on the SEM die (3 dies away from the center of the wafer) in order to measure the width of the nanowires without affecting the devices of interest. The width of the nanowires after etching was the same as the HSQ bars patterned after e-beam lithography; an image of the HSQ bar is seen in Fig. 2.3.2.

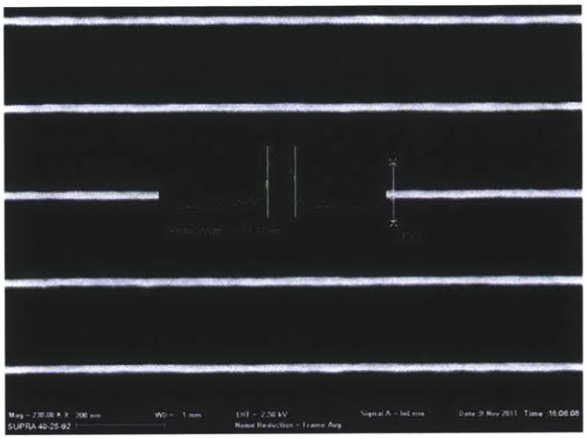

Fig. 2.3.2 SEM image of wires defined by HSQ width=18 nm before dry etching to form the Si/Ge nanowires on the SEM die. All quoted nanowire widths are measured from SEM images of the HSQ before dry etching of the s-Si/s-Ge. The measured W_{NW} is equal to the HSQ width. The nanowire width is defined by the FWHM of the HSQ signal (inset).

The nanowire widths measured in the SEM die were comparable to the nanowire widths measured in the center die. After the creation of the nanowire and source/drain pads, conformal high-κ/metal-gate was deposited via ALD. The gate did not overlap the source/drain pads causing the source and drain junctions to be in the nanowires on some devices resulting in higher than desired series resistance. This can be corrected on future mask designs. Following ion implantation, a standard interlayer dielectric (ILD) and metallization process was used to complete the devices. After device processing, cross-section TEM images of a special test structure with various nanowire widths and a W_{NW}= 18 nm device was performed on the SEM

die by Evans Analytical Group via the lift-out technique using focused-ion beam (FIB). Selected images of W_{NW}= 18 and 49 nm are seen in Fig. 2.3.3. The XTEM images show concave Ge sidewalls from the nanowire dry-etch or the NH_4OH:DI clean that preceded it.

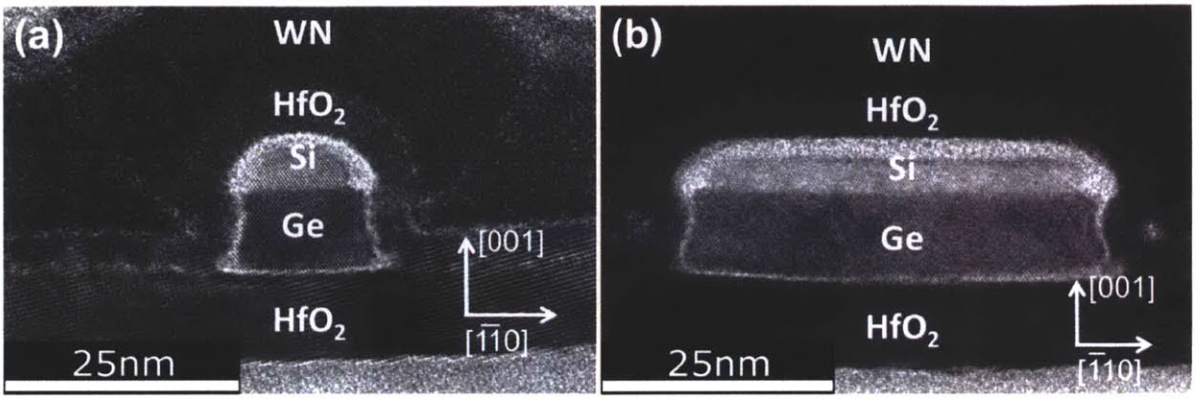

Fig. 2.3.3. Cross-section TEM images of W_{NW}=(a) 18 nm and (b) 49 nm trigate devices after processing. The dry-etch is un-optimized and yields non-vertical sidewalls with a waist. There also appears to be a thick SiO_2 film (~2 nm). Quantum mechanical simulations of planar MOSFETs on the same chip suggest a SiO_2 thickness of 5 Å (courtesy of Jamie Teherani). The discrepancy in the TEM may be due to thickness fluctuations on the Si surface in the nanowire.

Chapter 3: Planar Strained Ge Device Electrical Characterization

The following chapter contains the analysis of SGDOI biaxially-strained, planar, on-chip p-MOSFETs. It is important to carefully analyze on-chip planar devices not only as a comparison to the Ge trigate devices, but also to isolate specific effects which are seen in the more complicated Ge trigate devices. This chapter analyzes the I-V and C-V properties, back-bias characteristics, back-side density of interface state (D_{it}) characterization and series resistance extraction of the planar devices.

3.1: Planar p-MOSFET I-V/C-V Characteristics

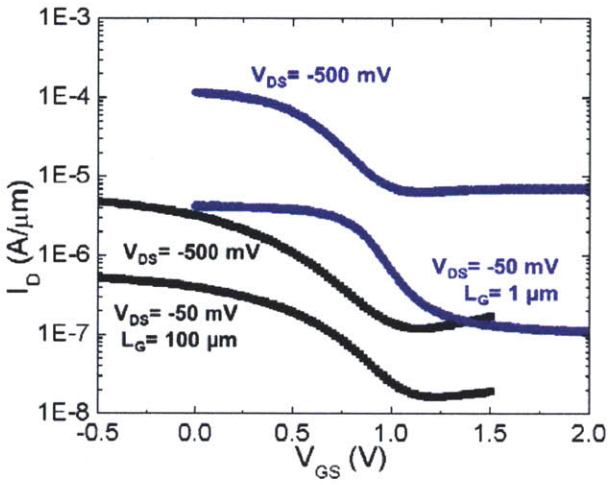

Fig. 3.1.1. Transfer characteristics for (black) L_g= 100 μm and (blue) L_g= 1 μm biaxially strained planar p-MOSFETs.

The transfer and output I-V characteristics for W= 100 μm, L_g= 1 μm and 100 μm are seen in Fig. 3.1.1 and 3.1.2, respectively. The transfer I-V characteristics reveal an $I_{max}/I_{min} < 10^2$, and a poor subthreshold swing (>200 mV/dec) for both devices. In addition, there appears to be a different threshold voltage and I_{min} for different V_{DS}. This would appear to be drain induced barrier lowering (DIBL) which is known to cause this effect in short channel devices. However,

the devices shown here, especially L_g= 100 μm, are long channel and the term "apparent DIBL" will be used in order to designate the V_t shift that is observed as a function of V_{DS}. The apparent DIBL in the current is likely related to the large off-state leakage that is a function of V_{DS}, which also affects the I_{max}:I_{min} ratio and the subthreshold swing. This off-state leakage is also seen in the output characteristics for both devices; the off-state current at V_{DS}= -500 mV is about 1/10 of the on-current for the same V_{DS}. Furthermore, the I_{max}:I_{min} ratio at low V_{DS} is constant with the changing gate length revealing that the off-state current is also scaling as a function of L_g. This suggests that when the gate is biased to turn off the drain current, the device is still on and the drain current cannot be effectively controlled by the gate. The high off-state current suggests that the Fermi level on the backside of the Ge is near the valence band and cannot be properly modulated by the gate. This problem is consistent with either a large, negative fixed charge or D_{it} on the back-side. Two mechanisms for the backside leakage can be imagined in this scenario. Trap assisted emission of holes from the source to the channel can be achieved with phonon assistance and high probability if the Fermi level is close to the valence band. Thermionic emission is also a possibility if the barrier between the source and channel is small which would also produce a similar effect. The mechanism for the I-V leakage cannot be proved by the measurements in this work.

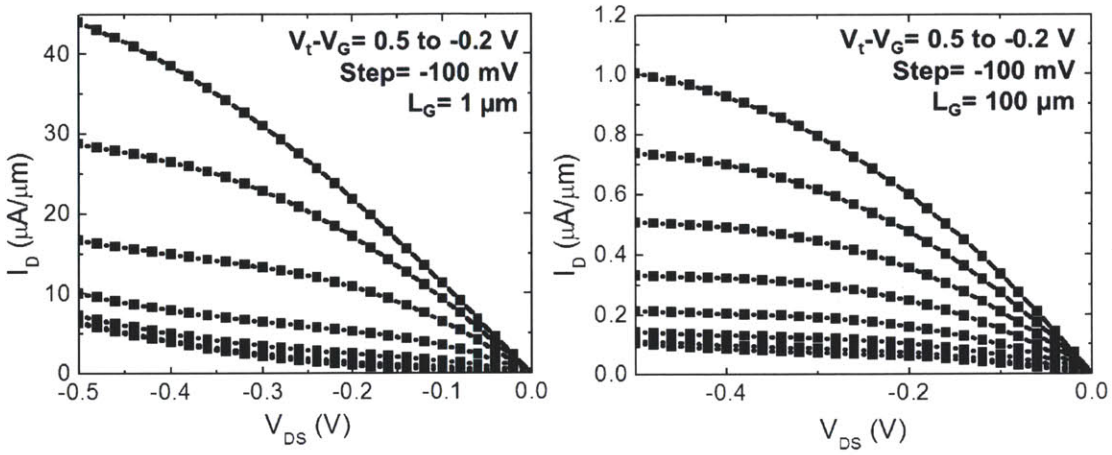

Fig. 3.1.2. Output characteristics for (left) L_g= 1 μm and (right) L_g= 100 μm biaxially strained Ge planar p-MOSFET. The output characteristics for the 1 μm FET do not saturate well and both MOSFETs show an inability to be turned off.

Additional understanding can be derived through capacitance-voltage measurements. The frequency dispersion characteristics of the split C-V curves for L_g= 1 μm and 100 μm (Fig. 3.1.3) show extremely large frequency dispersion especially in accumulation. Accumulation capacitance associated with electrons should not be collected from split C-V because the p-n junction between the source/drain and the channel is supposed to prevent the majority carrier of the channel from being supplied by the source or drain [20]. In a typical bulk MOSFET, the body is contacted to extract the accumulation capacitance, but in these on-insulator devices the body is floating and no accumulation capacitance should be collected. The origin of the accumulation capacitance for these s-Si/s-Ge devices is most likely band to band tunneling (BTBT) from the highly doped source and drain into the silicon cap in the channel due to the band-offsets between Ge and Si (Fig. 3.1.4(b)). The source and drains are highly doped and the valence band of the Ge is close to the Fermi level which also passes through the Si conduction band in the channel in accumulation. By applying a positive bias, electrons should be attracted to the surface of the Si,

but few are present in the channel. Therefore, there are plenty of empty states in the conduction band where electrons can tunnel from the valence band of the Ge source and drain into the conduction band of the channel.

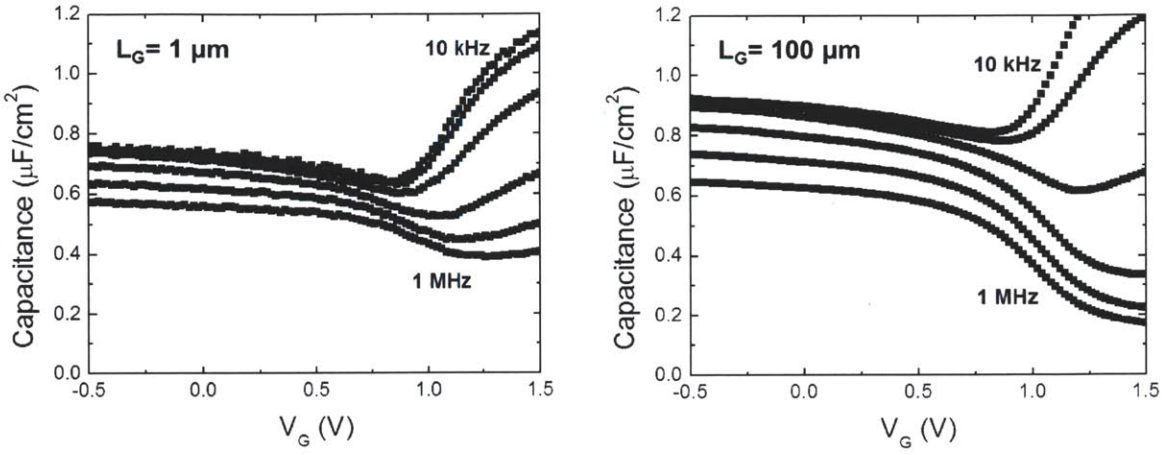

Fig. 3.1.3. Split C-V for (left) L_g= 1 μm and (right) L_g= 100 μm biaxially strained planar p-MOSFET. The CVs show capacitance for the devices even at 1 MHz when then band-to-band tunneling of the electron charge is likely to be eliminated.

While most of the accumulation capacitance can be removed by using high frequencies, >100 kHz, and more ideal C-V curves can be obtained, they are now also affected by series resistance. A large accumulation capacitance still exists suggesting a secondary conduction path between the channel and source/drain when the device is supposed to be off. The remaining capacitance must be due to a back-side conduction path which may be consistent with a trap assisted tunneling mechanism, Fig. 3.1.4(c). A high density of interface traps is expected on the back-side of the device. It is possible that an electron can be captured by a trap in the bandgap of the channel. A trap near the valence band would respond very quickly, and would result in a hole in the valence band of the source or drain. The hole can then be collected out of the source or drain resulting in the capacitance that is seen at high frequencies. Because an

electron is emitted into the channel, the I-V characteristics are not affected by this mechanism. However, it can be imagined that a similar trap assisted tunneling mechanism can allow holes to overcome the barrier of the channel which can be collected out of the drain during normal MOSFET operation.

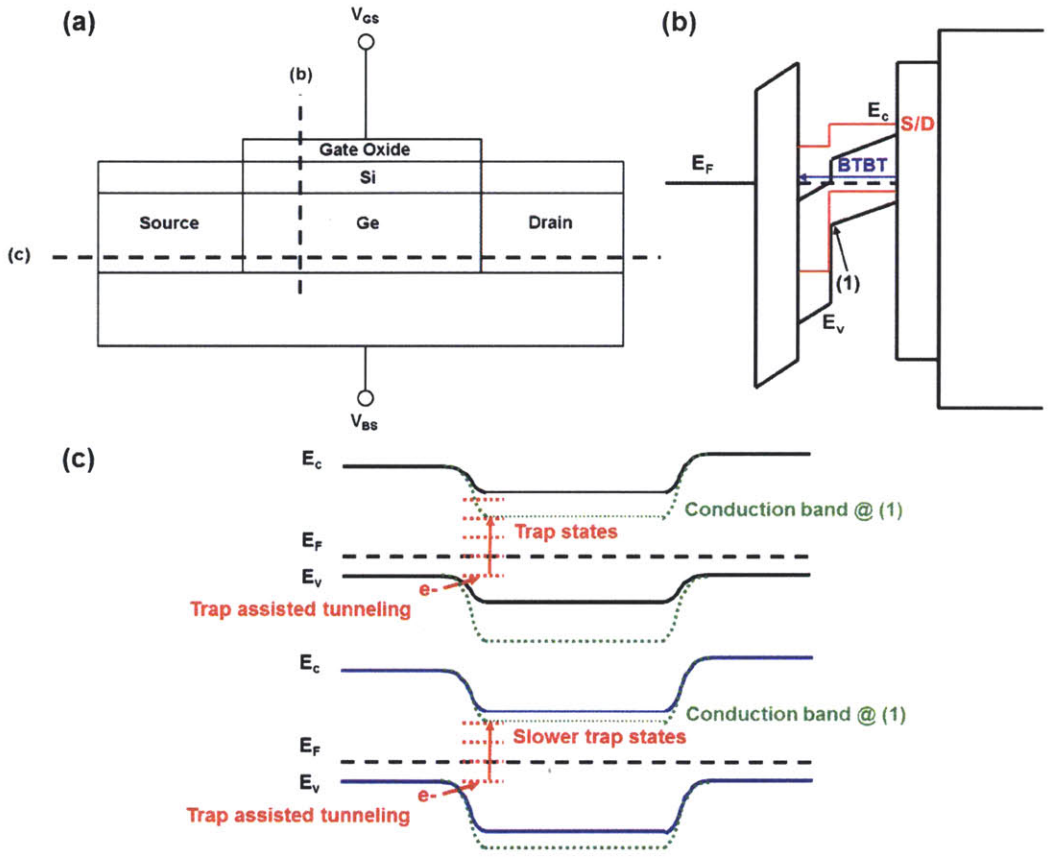

Fig. 3.1.4. (a) Device schematic for a planar device showing the cross-sectional cuts for different off-state leakage mechanisms. (b) Vertical band cross-section illustrating band to band tunneling from the Ge source/drain to the Si channel. (c) Horizontal band cross-section illustrating the effect of back-bias on the trap assisted tunneling path.

In order to explain both I-V and C-V, high D_{it} between the Ge and HfO_2 from the buried oxide is required. An additional fixed charge between the HfO_2 and the semiconductor can explain the inability for the gate to turn-off the device, but it cannot explain the accumulation

capacitance at extremely high frequencies by itself. A temporary solution to both problems is to apply a back-bias. A back-bias can offset the fixed charged between the HfO_2 and SiO_2 in the buried oxide layer by creating a layer of holes in the handle wafer instead of the back-side of the device eliminating the current leakage path. The back-bias is expected to reduce the D_{it} contribution in the accumulation region of the split C-V at high frequencies by pulling down the Fermi level in the channel. Traps in the middle of the Ge bandgap are expected to respond much more slowly than those close to the valence band edge because the barrier to tunnel from the valence band of the source or drain into the intermediate trap state is larger. Back-bias is expected to have drastic effects on the I-V and C-V characteristics of the planar devices.

3.2: Effect of Backbias

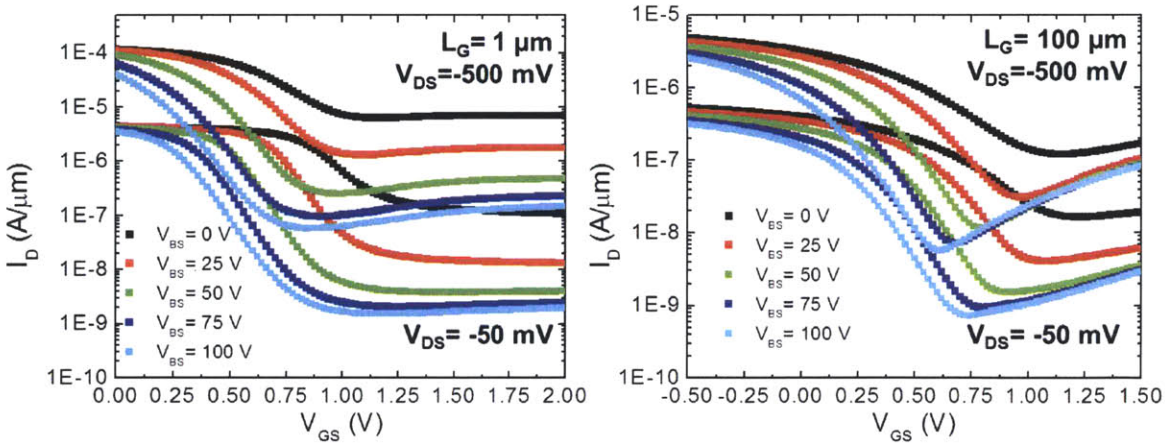

Fig. 3.2.1. Transfer characteristics for (left) L_g= 1 µm and (right) L_g= 100 µm biaxially strained planar p-MOSFET as a function of back-bias. The back-bias improves the SS and decreases the apparent DIBL offset between V_{DS}= -50 mV and V_{DS}= -500 mV.

Back-bias is employed in an attempt to fully turn off the on-chip planar devices. By introducing a positive back-bias on L_g= 1 µm and 100 µm devices (Fig. 3.2.1), the transfer characteristics show a greatly improved off-state current for all V_{DS} and positive V_{BS}. The

apparent DIBL between different V_{DS} curves is also reduced as a function of V_{BS} demonstrating that the apparent DIBL in the I-V characteristics is due to backside leakage and not short channel effects. A reasonable I_{max}:I_{min} ratio, $>10^3$, is achieved for the L_g= 1 μm device and a low I_{min} of 0.7 nA/μm is achieved for L_g= 100 μm. The output characteristics for the devices (Fig. 3.2.2) illustrate normal device behavior. In summary, measurements involving V_{BS} show promise for the planar devices. An improved off-state current and high drive current is observed. Without back-biasing the device to remove the leakage the drive current can be considerably higher if an improved backside interface can be made.

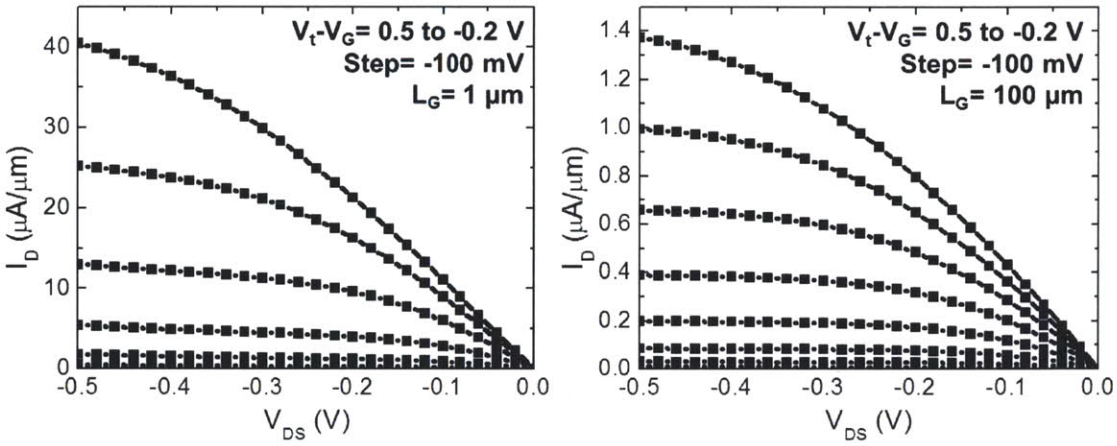

Fig. 3.2.2. Output characteristics for (left) L_g= 1 μm and (right) L_g= 100 μm biaxially strained planar p-MOSFET at V_{BS}= 100 V.

C-V measurements can be used to analyze the mechanism for the decrease in off-state current due to applied V_{BS}. Split C-V was taken at V_{BS}= 100 V for both L_g= 1 μm and 100 μm (Fig. 3.2.3). For L_g= 100 μm, the accumulation charge disappears at f= 100 kHz showing that back-bias is effective at removing the hypothesized trap assisted tunneling path for long channel devices. While the accumulation capacitance is completely removed, minor frequency dispersion

still exists in weak inversion, suggesting that the D_{it} is still interacting with the holes in the device.

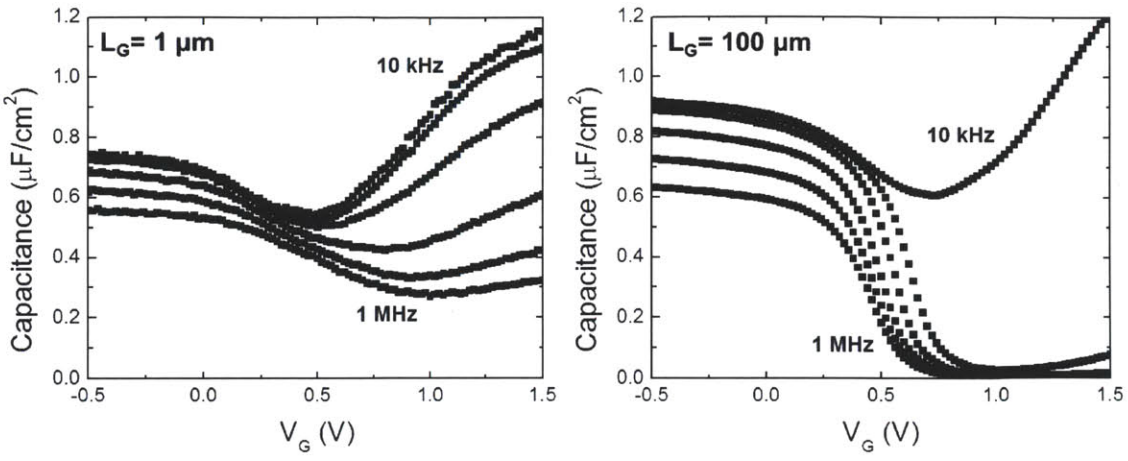

Fig. 3.2.3. Split C-V for (left) L_g= 1 μm and (right) L_g= 100 μm biaxially strained planar p-MOSFET at a back-bias of 100 V.

Unfortunately, the accumulation capacitance is still present at high frequencies for the L_g= 1 μm device, although it is reduced relative to V_{BS}= 0 V. Because the channel of the device is un-doped, the depletion region from the source and drain penetrates deep into the channel preventing the back-bias from being able to fully control the backside surface potential as in the case of L_g= 100 μm. The back-bias results suggest that it is crucial for the backside interface between the Ge and the HfO_2 to have low D_{it}. By removing the D_{it}, it is possible to remove the contamination in the split C-V for more accurate mobility extraction, and achieve a lower off-state current.

3.3: Series Resistance Extraction

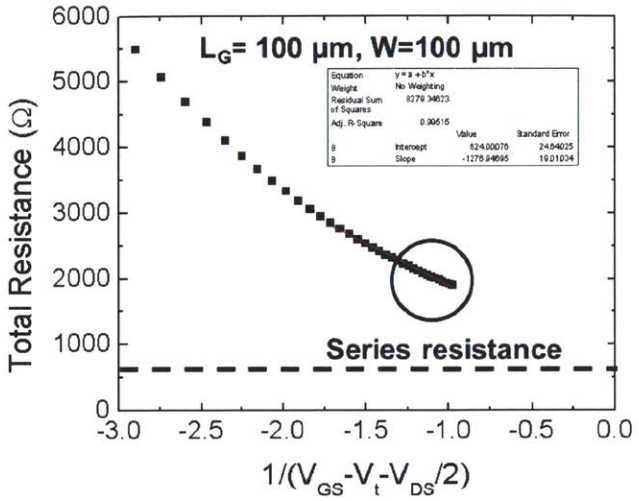

Fig. 3.3.1. The extracted series resistance using the G_0 method for L_g= 100 um. The series resistance is observed to be significantly higher than calculated from the sheet and specific contact resistances.

Understanding series resistance is important for correcting the extracted mobility and for the eventual scaling of these devices. The series resistance can be broken down into four elements: (1) the sheet resistance of the semiconductor, (2) the contact resistance between the metal and semiconductor, (3) the spreading resistance at the edge of the source/drains, and (4) the resistance of the metal vias and pad to the probe. Because the metal pads are thick and the vias are wide, the fourth component of series resistance is assumed to be negligible and is not analyzed. The sheet resistance was extracted to be 372 Ω/sq. using a Van der Pauw structure [21]. The contact resistance was calculated to be ~$1x10^{-6}$ Ω-cm^2 using a Kelvin cross bridge structure [21]. The channel is lithographically 500 nm away from the source and drain vias for these devices. The sheet resistance is expected to account for > 10 Ω of the series resistance and the contact resistance is expected to account for 1-2 Ω. The sheet resistance dominates in this case because the semiconductor film is very thin, and also likely damaged due to the ion implantation.

With further scaling or high mobility devices, it is important to improve the series resistance, specifically the sheet resistance, with an improved source/drain formation process.

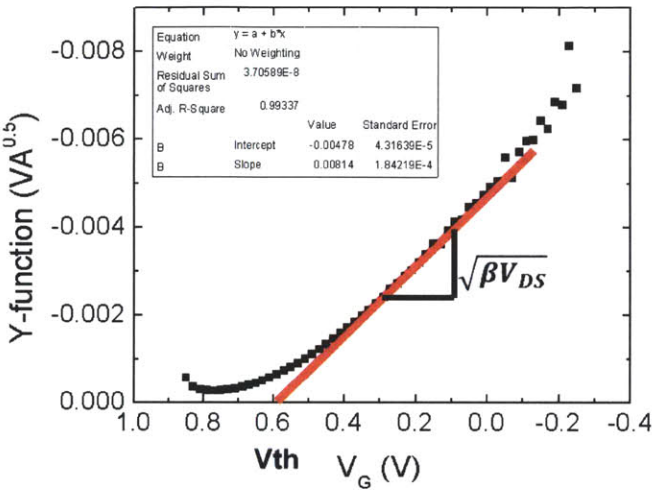

Fig. 3.3.2. Y-function vs V_G of an example MOSFET. β is extracted from the slope and V_t is the x-intercept of the linear extrapolation of the linear regime at low gate overdrive.

The G_0 method was applied to extract the series resistance for channel lengths >10 μm. The G_0 method extracts the series resistance by extrapolating the total resistance vs. inverse gate overdrive, $1/(V_{GS}-V_t-V_{DS}/2)$, to zero [22]. Physically, this means that at infinite gate overdrive there will no channel resistance and the remaining resistance is the series resistance. However, for long channel lengths the series resistance cannot be accurately measured using this method because the overall resistance is much higher than the series resistance. The mobility degradation, circled in Fig. 3.3.1, illustrates that the curve is non-linear at high gate overdrives making the linear extrapolation to infinite gate overdrive an overestimation of the series resistance. In order to deal with this problem, shorter-gate length devices, $L_g < 2$ μm, were used because the series resistance is comparable to their total resistance. Because the contacts for long and short channel devices are the same, the series resistance is assumed to be the same for all planar devices.

Accurate threshold voltage extraction is required for this series resistance calculation because the threshold voltage will affect both the slope and y-intercept resulting in an error in the series resistance.

The Y-function method [23] was chosen in order to accurately extract threshold voltage. The Y-function method models a gate overdrive dependent mobility degradation and series resistance. This method models the linear regime of I_{DS} as:

$$I_{DS} = \frac{\beta V_{gt} V_d}{1 + (\Theta_{10} + \beta R_{SD}(V_g)) V_{gt} + \Theta_2 V_{gt}^2}, \beta = \frac{\mu_0 C_{ox} W}{L_{eff}}, V_{gt} = V_g - V_t \quad (3)$$

Where I_{DS} is the drain current, V_{gt} is the gate overdrive, μ_0 is the carrier mobility, C_{ox} is the gate oxide capacitance, W is the device width, L_{eff} is the effective gate length, V_d is the drain voltage, Θ_{10} and Θ_2 are mobility degradation terms and $R_{SD}(V_g)$ is the gate voltage dependent series resistance. Using this technique, the extraction of threshold voltage is performed by first extrapolating $Y \equiv I_D / \sqrt{g_m}$ vs. V_{GS} in the linear regime at low gate overdrive to avoid mobility degradation effects; the x-intercept is the threshold voltage (Fig. 3.3.2). The extracted threshold voltage includes mobility and series resistance terms which depend upon gate overdrive. Using the above definition of I_{DS}, the Y-function can be derived to be:

$$Y_{mes} = \frac{I_{DS}}{\sqrt{gm}} = \frac{\sqrt{\beta V_d} V_{gt}}{\sqrt{1 - (\Theta_2 + R'_{SD}\beta) V_{gt}^2}} \quad (4)$$

where R'_{SD} is the differential of the series resistance with respect to V_g. β can be extracted through the slope of the Y-function, and Θ_{eff} can be extracted by fitting I_{DS}. Θ_{eff} is defined as:

$$\Theta_{eff}(V_g) \equiv \frac{\beta V_d}{I_{DS}} - \frac{1}{V_g - V_t} = \Theta_{10} + R_{SD}(V_g)\beta + \Theta_2 V_{gt} \quad (5)$$

Θ_{eff} physically is the combination of the series resistance and mobility degradation in the linear regime. By doing this, an initial set of values can be determined; however, the threshold voltage is extracted using a data set that is coupled with the mobility degradation and series resistance. In order to decouple the gate voltage dependent series resistance and mobility degradation terms from the threshold voltage, a new Y function is defined which is independent of these terms:

$$Y_0 = Y_{mes}\sqrt{1-(\Theta_2 + R'_{SD}\beta)V_{gt}^2} \tag{6}$$

Y_0 is a corrected Y-function which is independent of mobility and gate voltage effects. Using Y_0 the previous steps are repeated, and new values of V_t, β and Θ_{eff} are obtained. Θ_{eff}' or Θ_{eff} differentiated with respect to V_G is also extracted in this fitting session. This is iterated until $R^2 >$ 0.997 for the fit of I_{DS}. Iteration can be continued for a better fit, although it would take more time. Ideally with different gate lengths or β values, the series resistance and mobility degradation values can be extracted; however, because of the lack of multiple equivalent L_g devices for the trigate p-MOSFETs the G_0 method was chosen

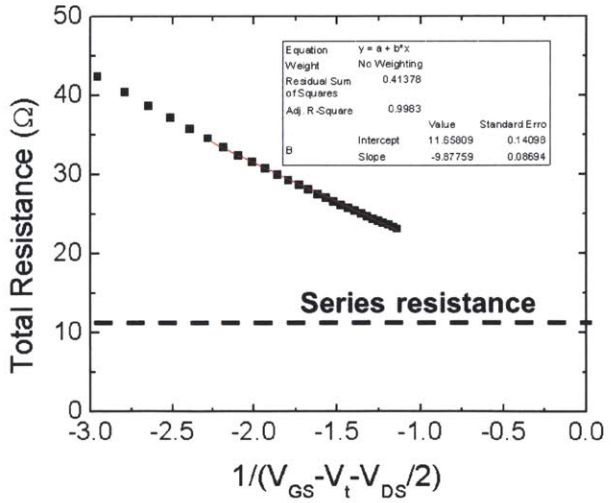

Fig. 3.3.3. $1/(V_{GS}-V_t-V_{DS}/2)$ vs Total resistance used for the G_0 method on L_g= 1 μm planar MOSFET. The series resistance is a large portion of the high inversion resistance (~50%).

For the planar p-MOSFETs the series resistance was extracted to be ~12 Ω as seen in Fig. 3.3.3; which is equivalent to 1.2 kΩ-μm. The series resistance is quite close to the calculated resistance and is greatly limiting the scalability of the device. The series resistance here is 50% of the total resistance at high gate overdrive, and it, primarily the sheet resistance, must be improved in future device runs.

Chapter 4: Device Characteristics of Asymmetrically Strained Ge Trigate p-MOSFETs

This chapter details the analysis of asymmetrically strained Ge trigate p-MOSFETs. The biaxially strained thin s-Si/s-Ge film is transformed into asymmetrically strained nanowires via e-beam lithography and etching. All devices in this section have 500 nanowires in parallel and 5 different nanowire widths were fabricated: 18, 26, 32, 43, and 49 nm for L_g= 10 μm p-MOSFETs. Current-voltage measurements are used to analyze the benefits of the non-planar (trigate) architecture. Mobility is extracted from current-voltage and capacitance-voltage characteristics to analyze the effects of the strain on the transport. Self-consistent Schrödinger-Poisson simulations by Jamie Teherani are also used to help quantify the effect of strain on effective mass.

4.1: Current-Voltage and Capacitance-Voltage Characteristics of Trigate p-MOSFETs

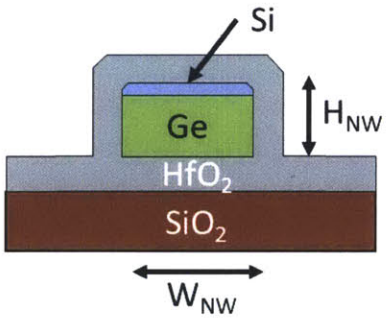

Fig. 4.1.1. Schematic of the cross-section of the channel of the s-Si/s-Ge nanowire trigate p-MOSFET, looking in the direction from source to drain.

A schematic of the nanowire trigate p-MOSFET channel can be seen in Fig. 4.1.1. The cross-section of the trigate shows a s-Ge channel capped by s-Si on top of it. On the top of the s-Si cap, there is a thin interfacial layer of SiO_2, and where there is no Si cap there is GeO_2 due to the ozone used during gate dielectric formation. These dielectrics are encapsulated by HfO_2 deposited via ALD. Due to the geometry of the nanowire, the gate dielectric thicknesses are

different on different surfaces. Due to the presence of SiO_2, and the s-Si cap, the capacitance equivalent thickness, CET= 3.8 nm (extracted from the planar device), of the top-side gate is much thicker than that of the Ge sidewall, which is expected to have a CET of about 1.3 nm [5]from previous planar strained Ge device runs. This asymmetry in the gate dielectric causes the gates at the sidewalls to have much better control of the channel than the top-side gate.

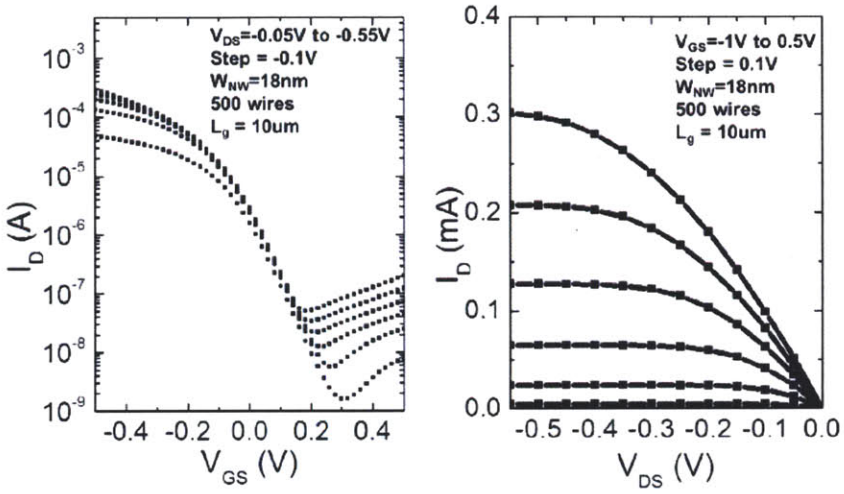

Fig. 4.1.2. (left) Transfer and (right) output characteristics for device, W_{NW}= 18 nm and L_g= 10 μm. The device has SS~85 mV/dec. and $I_{max}/I_{min}>10^4$ for V_{DS}= -50 mV.

Transfer and output characteristics for a device with L_g= 10 μm, and W_{NW}= 18 nm can be seen in Fig. 4.1.2. Without back-bias, the I_{max}/I_{min} is good at all V_{DS}, but better at low V_{DS} where I_{max}/I_{min} approaches 10^5, in stark contrast to the planar p-MOSFETs presented in the previous chapter. Furthermore, the subthreshold swing is also a respectable ~85 mV/decade compared to a SS > 200 mV/decade seen in the planar FETs. The combination of good SS and high I_{max}/I_{min} make these trigate devices state of art for strained Ge. This indicates that the formation of the sidewall affords much better electrostatic control over the back-side leakage mechanism that

prevailed in the planar p-MOSFETs. The sidewall dielectric quality must also be of high quality because of the measured SS. The SS for a planar FET can be approximated by:

$$SS = \frac{kTln(10)}{q}\left(1 + \frac{C_{it}}{C_{ox}} + \frac{C_b}{C_{ox}}\right) \quad (7)$$

where k is Boltzmann's constant, T is the temperature, q is the charge of an electron, C_{it} is the interface trap capacitance, C_{ox} is the oxide capacitance, C_b is the bulk capacitance. For a fully depleted thin body device that is undoped, C_b is negligible. Because of the large asymmetry in the effective gate dielectric thickness, the capacitance of the sidewall dielectric can be assumed to have full dielectric control over the channel. Here, we can use the SS to approximate the sidewall D_{it}. Using this approximation and a SS of 80-85 mV/decade, an approximate D_{it} of $5.5x10^{12}$ - $7x10^{12}$ $cm^{-2}V^{-1}$ is extracted, which is fairly reasonable for Ge, and in good agreement with the value extracted by Hashemi from similarly-processed planar strained-Ge p-MOSFETs [5]. The SS method places an upper bound on the actual sidewall D_{it}.

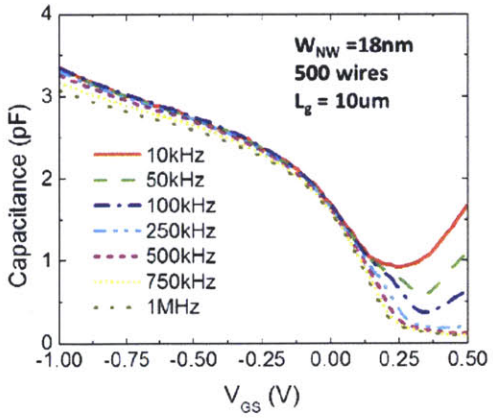

Fig. 4.1.3. Split C-V for W_{NW}= 18 nm and L_g= 10 μm. The C-V shows very little frequency dispersion in the inversion regime as a function of frequency, and the accumulation capacitance can be completely suppressed with little impact on the inversion capacitance.

Because of the good interface and electrostatics, the split C-V measurements for the device also are improved relative to the planar devices (Fig. 4.1.3). While there is large frequency dispersion in the accumulation regime, the accumulation capacitance can be removed at high frequencies with little impact on the inversion capacitance. Mobility can be accurately extracted from 500 kHz split C-V curves which has little contamination from series resistance, D_{it} and accumulation capacitance.

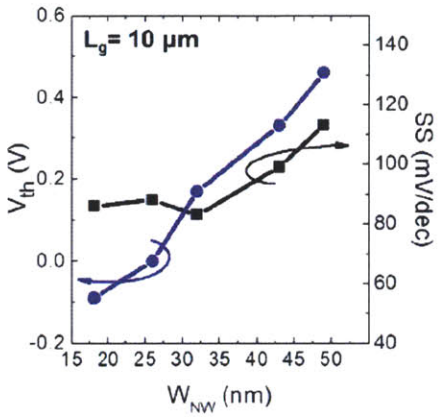

Fig. 4.1.5: V_t and SS vs. W_{NW}. V_t shift as a function of W_{NW} may be caused by back-side/sidewall D_{it}. The planar (biaxial) device used for mobility extraction has a SS and V_t of 205mV/dec. and 0.8V, likely influenced by backside D_{it}.

Both I-V and C-V characteristics change as a function of nanowire width, W_{NW}. The subthreshold swing and threshold voltage, V_t, both vary as a function of W_{NW} (Fig. 4.1.4). The SS stays relatively constant until $W_{NW} \sim 30$ nm and then begins to increase with nanowire width. The threshold voltage steadily moves positive as a function of W_{NW}. The SS is expected to increase as a function of W_{NW} because the SS for the planar FETs was > 200 mV/dec, and an increasingly wide W_{NW} should approach this number. The curious fact is that the V_t changes very dramatically as a function of W_{NW}, with more than 500 mV difference between W_{NW}= 18

nm and 49 nm. Such a large discrepancy cannot be explained simply by strain effects. Instead what is observed here is likely the effect of backside and sidewall D_{it}. While the sidewall D_{it} may have some impact on V_t, it is the same for all trigates; therefore, the impact is most likely due to the backside D_{it}.

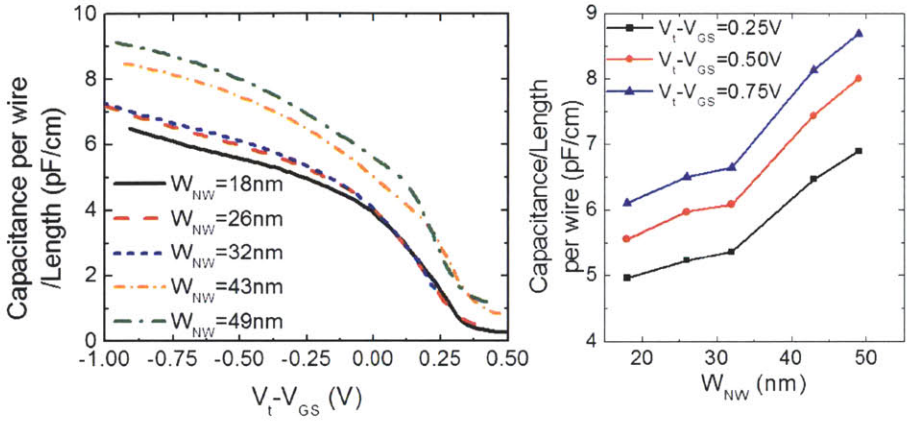

Fig. 4.1.5. (left) Capacitance per wire/length as a function of gate overdrive for different nanowire widths. (right) Capacitance per wire/length as a function nanowire width for fixed gate overdrives. The capacitance does not scale linearly as a function of W_{NW}.

The capacitance at a fixed overdrive is expected to increase linearly as a function of W_{NW}. However, the capacitance (Fig. 4.1.5) does not really increase as expected. For large W_{NW}, the capacitance matches the expected capacitance (CET= 3.8 nm for the top oxide and CET= 1.3 nm for the sidewall oxide) and the slope matches the expected change in capacitance as a function of W_{NW}; i.e. the change in capacitance is due to the change in width or the capacitance of the top gate dielectric. However for small W_{NW}, < 35 nm, the slope of the capacitance vs. width curve is much lower than predicted, and the overall capacitance is higher. Similarly, the minimum capacitance is higher for large W_{NW} indicating possible leakage as well. Simulations in nextnano[3] by Jamie Teherani, predicted that the capacitance should scale linearly with W_{NW}. The

difference between simulation and experiment may be associated with the back-side D_{it}. It is also uncertain as to why the capacitance does not saturate with increasing gate V_G. Simulation, seen in Section 4.3, predicts that the capacitance should saturate as a function of V_G in the voltage range shown in Fig. 4.1.5, and that the slope of the turn-on of the capacitance vs. gate voltage should be sharper. A possible explanation is that the sidewall gate is capable of modulating the back-side D_{it} for small W_{NW} preventing the D_{it} from controlling the off-state current.

4.2: Mobility and Transport for Asymmetrically Strained Nanowires

In order to quantify the benefit of strain to the carrier transport in the asymmetrically strained Ge nanowires, mobility is extracted using the transfer I-V characteristics at low V_{DS} and split C-V. The mobility is expected to increase as a function of decreasing W_{NW} because the strain becomes essentially uniaxial as was previously shown in Ch. 2.

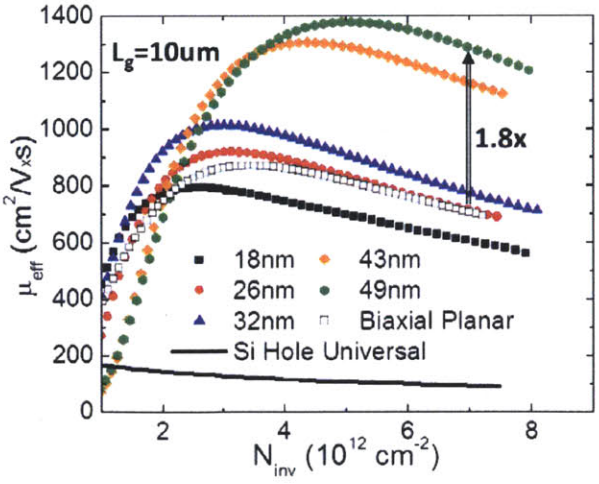

Fig. 4.2.1. Effective hole mobility for trigate and on-chip planar (biaxially strained Ge) FETs and Si hole universal [24]. N_{inv} for trigates is calculated using a conservative

W_{eff}=500•(W_{NW}+2H_{NW}). The mobility of the planar FET was extracted using W=L_g=100 μm. The mobility for W_{NW}=49 nm is ~ 1.8x the biaxial strained Ge mobility at N_{inv} = 7x10^{12} cm^{-2}.

The mobility can be experimentally extracted using the following:

$$\mu_{eff} = \frac{g_d}{L^2 \int_{V(Cmin)}^{V_G} C(V_G) dV_G} \quad \textbf{(8)}$$

where g_d is the output conductance or I_D/V_{DS} for low V_{DS}, $V(C_{min})$ is the voltage where the capacitance reaches its minimum value, and $C(V_G)$ is the capacitance at V_G. $V(C_{min})$ was used as the starting point for integration because a finite capacitance is observed for all nanowires which would otherwise artificially inflate the mobile charge, if the integral was started at higher gate voltage. The mobility was extracted using f= 500 kHz for the L_g= 10 μm trigate devices, and f = 250kHz for the L_g=W= 100 μm planar device. The mobilities for all W_{NW}, the biaxial on-chip control and silicon hole universal for [110]/(100) are shown in Fig. 4.2.1. The inversion charge density, N_{inv} is defined as:

$$N_{inv} = \frac{\int_{V(Cmin)}^{V_G} C(V_G) dV_G}{q W_{eff} L_g} \quad \textbf{(9)}$$

where $V(C_{min})$ is the voltage when the capacitance first reaches its minimum, and $C(V_G)$ is the capacitance at a certain V_G, q is the charge of an electron, W_{eff} is the effective width given by W_{NW} + 2H_{NW}, and L_g is the gate length. Before analyzing the mobilities here there are two key things to note: (1) the estimation of N_{inv} and (2) the effect of series resistance on the extracted mobilities. The effective width was estimated to be a conservative W_{NW} + 2H_{NW}. While this is the full width of the gated nanowire, only the Ge region is active, so the effective width should be slightly less. A second reduction in the effective width can be from the fact that the sidewall is not fully gated. Instead, the HfO_2 from the gate dielectric prevents the metal from fully gating the

sidewall all the way to the bottom of the nanowire. Both of these effects are small, and would make the effective width of the transistor smaller than the value used for the mobility curves.

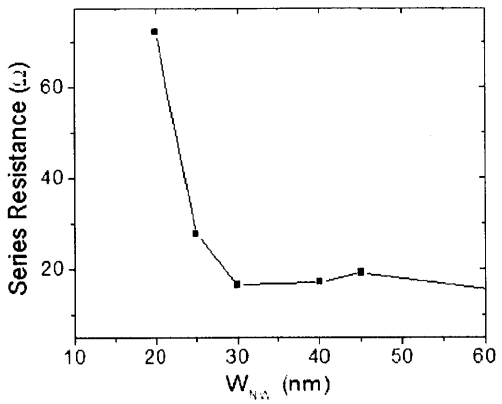

Fig. 4.2.2. Series resistance as a function of W_{NW}. The series resistance was extracted using L_g= 1 μm MOSFETs. The series resistance stays approximately constant past W_{NW}= 30 nm.

There is also slight contamination of the mobility extraction because of the series resistance, even though the gate length is relatively long at 10 μm. Typically the series resistance is not an issue for such a long gate length, but the high mobility of the channel causes the source/drain resistance to be comparable to the channel resistance at high inversion charge. The series resistance for each nanowire width has been extracted for L_g= 1 μm devices in Fig. 4.2.2 using the G_0 method from the previous section. For a structure where the gate overlaps the source and drain pads that were patterned using photolithography, the series resistance would be equal for all of the nanowire widths, ~ 12 Ω, which is the same as the series resistance of the planar FETs. Since there was an error in the mask design and the gate does not overlap the source and drain pads, the series resistance is increased for narrow wires. In order to account for this effect the drain voltage is corrected by:

$$V_{DS}^{int} = V_{DS}^{applied} - R_{SD} I_D \qquad \textbf{(10)}$$

where V_{DS}^{int} in the internal drain voltage that is dropped across the channel, $V_{DS}^{applied}$ is the applied drain voltage, R_{SD} is the source and drain resistance, and I_D is the drain current. The same correction can be made to V_G in order to correct the inversion charge. However, because high values of V_G are applied, ~1 V, the 10% correction to V_{DS}= -50 mV is an insignificant correction to V_G. By adjusting V_{DS} using the extracted series resistances for all W_{NW}, corrected effective mobility vs. N_{inv} curves are obtained (Fig 5.2.3). The series resistance for the planar FET is not corrected, because the series resistance is negligible since mobility was extracted from a device with 10x the gate length of the trigate nanowire MOSFETs.

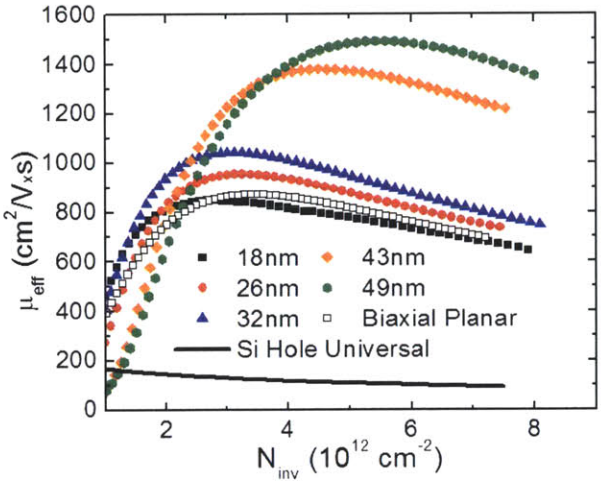

Fig. 4.2.3. Series resistance corrected mobility for trigate and on-chip planar (biaxially strained Ge) FETs and Si hole universal [24].

The comparison of the mobilities before and after the series resistance correction at high inversion charge, Fig. 4.2.4(a), illustrates that the mobility is slightly increasing with increasing nanowire width until W_{NW}> 32 nm. The mobility then increases very rapidly as a function of W_{NW}. In comparison to silicon universal and the biaxially strained Ge, the series resistance

corrected mobility of a W_{NW}= 49 nm Ge nanowire is 15x and 2x higher at N_{inv}= $7x10^{12}$ cm^{-2} respectively.

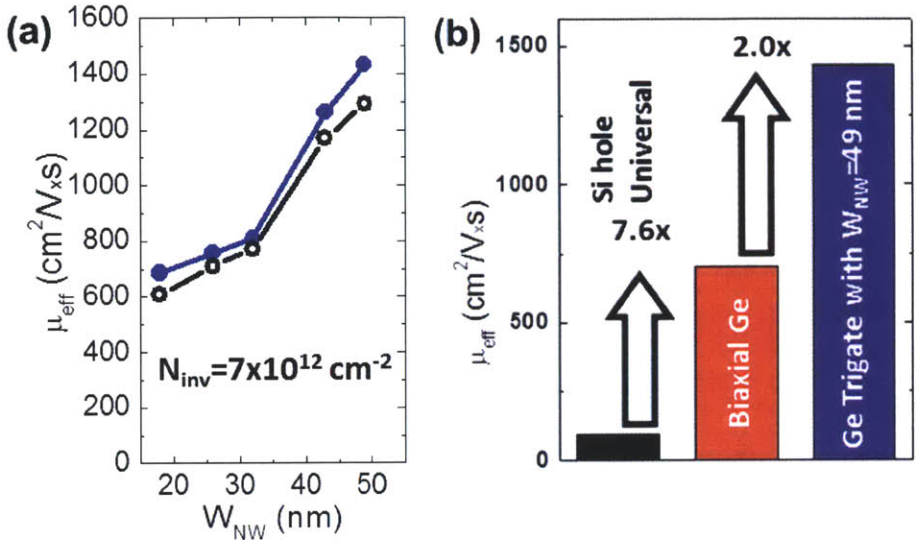

Fig. 4.2.4. (a) A comparison of as-extracted (open symbols) and series resistance corrected mobilities (closed symbols) at N_{inv} =$7x10^{12}$ cm^{-2} for different W_{NW}. The correction increases the mobility by ~ 10%. (b) Mobility comparison at N_{inv} =$7x10^{12}$ cm^{-2}.

There are some interesting characteristics to the mobility curves for various W_{NW}. First, the mobility peak is not at constant N_{inv} as a function of W_{NW}. The mobility peak is at high N_{inv} for large W_{NW} and at lower N_{inv} for smaller W_{NW} and the biaxially strained case. There are two possible explanations for this: (1) the underestimation of W_{eff} due to a smaller than expected contribution to the effective height and (2) the backside D_{it} affects the larger nanowires more than the smaller nanowires since the sidewall gates have decreased electrostatic control over the backside Fermi level. The first would make sense because the change to W_{eff} would be larger for smaller nanowires because the sidewalls are a larger portion of the overall width. Both effects will cause a wider nanowire to have a higher N_{inv} relative to smaller nanowire.

The second observation is that the mobility increases with increasing W_{NW} which contrasts the hypothesis of this experiment. The effective mobility is approximately given by:

$$\mu_{eff} = \frac{q\tau}{m^*} \quad (11)$$

Where q is the charge of an electron or hole, τ is the scattering time, and m^* is the effective mass of the charge carrier. The effective mass of the carriers is expected to decrease with the strain transition from biaxial to uniaxial which will cause the mobility to increase, assuming that the scattering time is constant for the wires. Clearly, the scattering time is not constant as a function of wire width because the mobility is increasing with increasing W_{NW}.

4.3: Scattering and Effective Mass Improvements to Transport in Asymmetrically Strained Ge Nanowires

To quantify the benefit to the transport from scattering time and strain, simulations were performed by Jamie Teherani using nextnano[3]. The simulations performed using nextnano[3] solved the Poisson-Schrodinger electrostatic equation self-consistently using a 6×6 k.p method for the nanowire structure and considers only the effect of the strain on the effective mass (scattering is not treated).

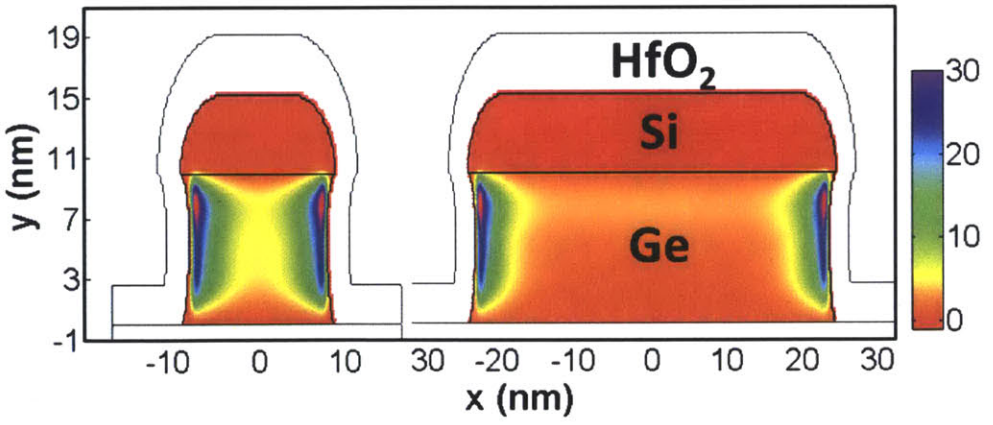

Fig. 4.3.1. Simulated hole densities (nextnano^3) for W_{NW}=18 and 49nm at V_{th}-V_{GS} $\approx$0.2 V, using a 6$\times$6 k.p method; the scale has units of 10^{18} cm^{-3}. The impact of strain on the energy bands was taken into account. The sidewall EOT (~1 nm) is smaller than the top EOT (~1.5 nm) due to differences in the GeO_x and SiO_x interface layers [5, 6]. A large fraction of the carriers are located near the sidewalls because of this and the s-Si/s-Ge valence band offset. The sidewalls are also the regions with the most asymmetric (approaching "uniaxial") strain. Simulations courtesy of Jamie Teherani.

In the simulation, the sidewall (Ge) EOT was modeled to be 1.0 nm of SiO_2 and the dielectric on top of the Si cap was modeled to be 1.5 nm. The strain profiles, previously seen in Section 3.2, were used in the calculation of 80 eigenstates for each of the nanowires. Each eigenstate represents an energy band for the nanowire. 80 eigenstates were simulated in order to capture the spatial distribution of all of the holes in the nanowire during inversion. As a function of gate voltage, the occupation of these eigenstates was calculated in order to obtain the charge density as a function of position for each voltage. Fig. 4.3.1 shows the charge density as a function of position for W_{NW}= 18 and 49 nm. The highest charge density resides primarily in the sidewalls of the nanowires, because the CET is much lower at the sidewalls than the top of the nanowire. For W_{NW}= 18 nm, almost all of the charge is within 5 nm of the sidewall, ~80%, while a much lower percentage (~50%) is at the sidewall for W_{NW}= 49 nm. The strain near the sidewalls is similar for different nanowire diameters. Two lobes of strain relaxation begin at the sidewall, and converge in the middle of the nanowire for W_{NW}< 43 nm; the middle of the nanowire is not biaxially strained for these nanowire diameters.

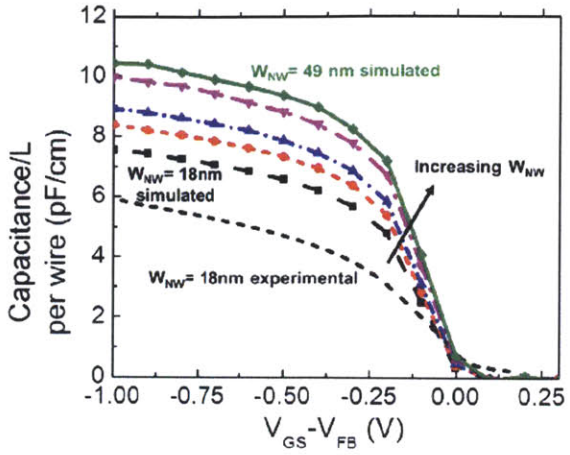

Fig. 4.3.2. Simulated capacitances for W_{NW}= 18, 26, 32, 43 and 49 nm. V_{FB} is defined as the point in the experiment where there is no charge on the gate metal. The experimental capacitance curve for W_{NW}= 18 nm has been shifted by aligning the V_t of the simulation and experiment. The experimental capacitance is shown as a comparison illustrating that the simulated capacitance is higher than expected. Simulations courtesy of Jamie Teherani.

By summing the entire charge for the wire the total charge of the wire can be calculated. An ideal capacitance (change in charge divided by change in voltage) vs. gate voltage can be extracted from the simulations (Fig. 4.3.2) for all nanowire diameters. The experimental curve for W_{NW}= 18 nm is overlaid on top of the capacitance curve. The ideal capacitance curves turn on quicker than the experimental curves, and have a higher maximum capacitance which is shown by the W_{NW}= 18 nm curve. The sharpness of measured turn-on is likely influenced by D_{it}. The difference in the maximum capacitance values is probably caused by the difference in the modeled and experimental sidewall EOT. The EOT for the Si capped region was extracted through quantum mechanical fitting of a planar FET. The sidewall EOT can be independently extracted through iterative fitting, but due to limited computational resources this was not done.

Although the sidewall EOT is not quite right, the simulations still capture the majority of the physics for transport. A different sidewall EOT will slightly change the occupation of the different eigenstates, but should not affect the band diagram. In order to extrapolate the effects of strain to the mobility, the average inverse effective transport mass was calculated by Jamie Teherani. The average inverse effective mass is directly proportional to the effective mobility. The average inverse effective mass for the eigenstates was first calculated by:

$$<\frac{1}{m_z}>_i = \frac{\sum_k \frac{v_z}{p_z} f(k)}{\sum_k f(k)} = \frac{\sum_k \frac{\frac{1}{\hbar}\partial E/\partial k_z}{\hbar k_z} f(k)}{\sum_k f(k)} \quad (12)$$

Where $<1/m_z>_i$ is the inverse effective mass in the transport direction for an eigenstate i, ħ is planck's constant divided by 2π, k_z is the crystal momentum in the z (transport) direction, E is the energy for an specific state, and f(k) is the Fermi function as a function of the crystal momentum. The equation first solves for the inverse effective mass by solving for the velocity in the z direction and dividing it by the momentum. The inverse mass as a function of k is then multiplied by the probability for the occupation of that k vector and then summed and normalized by the total occupation of the eigenstate. A second average over all of the eigenstates is taken to obtain the average inverse effective mass in the transport direction using:

$$\ll \frac{1}{m_z} \gg = \frac{\sum_i <\frac{1}{m_z}>_i F_i}{\sum_i F_i} \quad (13)$$

where $<<1/m_z>>$ is the average inverse effective mass for all eigenstates and F_i is the occupation probability for the eigenstate.

The final simulated inverse effective masses for each of the nanowire diameters (Fig 5.3.3) show a minor dependence upon the wire diameter. The inverse effective mass is normalized by the inverse effective mass of the biaxially strained Ge which was calculated using the same method that has been described here. The theoretical effective mass of the smaller

diameter wires is indeed lower than that of the larger diameter wires as expected. Also, the simulations seem to be quite accurate when comparing the measured mobilities of large W_{NW} with the biaxial case; for W_{NW}= 49 nm the measured mobility is 2x that of biaxially strained Ge, and the inverse effective mass is ~1.6x showing good agreement. For small W_{NW} a large discrepancy between the measured mobilities and inverse effective mass exists. There is a decrease in the measured mobility from W_{NW}= 18 nm and 49 nm, but the simulations predict a 15% decrease in the inverse effective mass. This demonstrates that scattering effects impact the enhancement that is expected from the difference in strain.

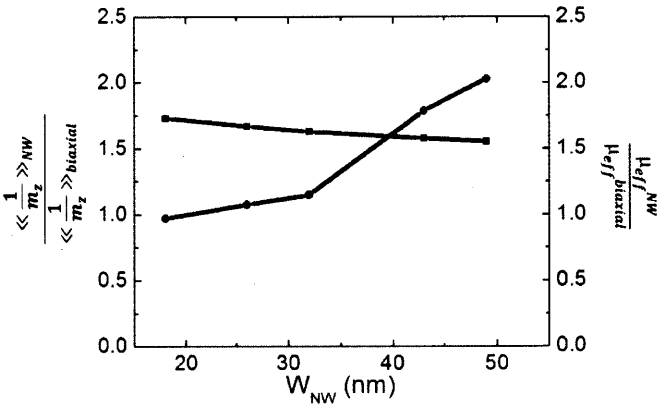

Fig. 4.3.3. The average inverse effective mass in the transport direction (black) and measured mobility enhancement (blue) normalized to the biaxial case as a function of W_{NW} at N_{inv}= 7 x 10^{12} cm^{-2}. A large change in the mobility enhancement is observed with respect to the small change in effective mass.

The increase in scattering rates for W_{NW}< 40 nm causes the mobility to degrade (Fig. 4.3.3) relative to the predicted increase in mobility from the decrease in effective mass. There are many possible reasons for the increase in scattering as a function of decreasing nanowire width such as line edge roughness, remote phonon scattering and differences in the phonon population

due to the non-uniform and asymmetric strain. The most obvious scattering mechanism is caused by the line edge roughness of the nanowire which can be characterized using SEM images. The line edge roughness was found to have a root-mean-square roughness of ~1.2 nm using a MATLAB script written by Tao Yu. The algorithm extracts the edges of the nanowire using contrast detection between the substrate and the HSQ bar or nanowire after etching and HSQ removal. Fewer SEM images were taken of the wires after etching to avoid charging the substrate from the electrons used to take the image. Using the script, the line edge roughness was found to be the same for the HSQ bars directly after e-beam lithography and the Si/Ge nanowires after the HSQ was removed. The line edge roughness is expected to affect thinner nanowires more in terms of scattering [25]. This is plausible because a change of 2 nm will affect the eigenstates more for smaller nanowires compared to a wide wire where the eigenstates are very close in energy.

Scattering associated with the dielectric interface, remote dipole and phonon scattering, are also known to exist. The silicon cap is believed to alleviate some of the scattering by moving the high-κ dielectric away from the Ge channel resulting in much higher mobilities for silicon capped Ge devices [26]. Finally, the effect of phonons on the scattering cannot be ignored. Phonon scattering affects the mobility at intermediate vertical fields, especially around the mobility peak. The combination of the differences in scattering and change in effective mass cause the mobility to be greatly enhanced for large W_{NW}, and high for small W_{NW} despite the additional scattering.

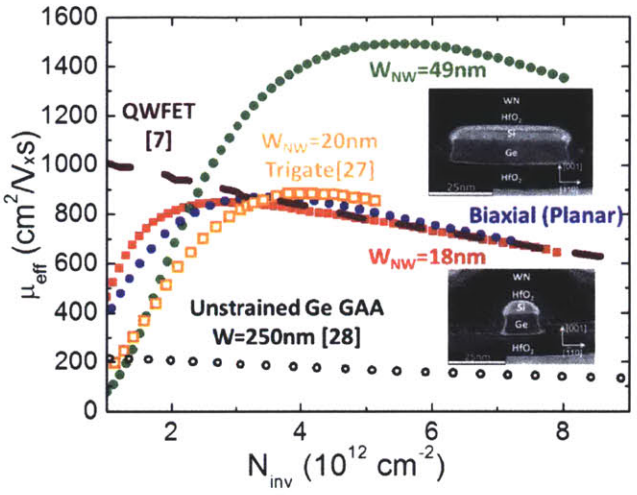

Fig. 5.1.1. Series resistance corrected mobilities (solid symbols) for trigates with W_{NW}=18 and 49 nm vs. previously published results for non-planar and state-of-the-art planar strained Ge FETs with high-k dielectrics. Insets show TEM of NW cross-sections. Biaxially strained and W_{NW}=18nm from this work have mobilities comparable to state-of art strained Ge devices. The W_{NW}=49 nm device shows dramatically improved transport relative to the highest reported strained Ge mobilities [7, 27, 28].

The mobility presented in this work shows promise for the use of asymmetrically strained Ge as a channel material. If the mechanisms for scattering are minimized, especially the line edge roughness, small nanowires promise an even higher mobility than demonstrated here. Fig. 5.1.1 shows the mobilities from W_{NW}= 18 nm, 49 nm and the biaxial strain relative to other strained Ge work that includes high-κ. The uniaxial and asymmetrically strained nanowire devices have the highest mobilities, although the biaxially strained Ge devices also have extremely high mobilites. The promise of high mobilities also requires that the scaling of

contacts and sheet resistance for these benefits to be observed relative to state of the art devices. Contributions of this work are:

- Fabricated Strained Germanium Directly on Insulator (SGDOI) substrates with buried high-κ
- Fabricated on-chip, 2.4% biaxially strained planar and asymmetrically strained nanowire Ge p-MOSFETs using SGDOI substrates
- Demonstrated high mobilities in biaxially strained and asymmetrically strained Ge
- Simulated and experimentally measured strain using Raman spectroscopy in Ge nanowires (Simulations performed by Jamie Teherani and Raman spectroscopy done by Yuanwei Dong and Guangrui Xia)
- Simulated band diagrams, carrier densities and reduction in the effective mass due to strain as a function of nanowire width (All simulations done by Jamie Teherani)

New challenges always arise with the use of undeveloped materials. Because of its small bandgap, Ge will likely be more susceptible to short-channel effects that are very well known in Si, and the ability for strained Ge to turn off at extremely scaled channel lengths will be an important question even with non-planar architectures that minimize these effects. More immediate problems to remedy concern the D_{it} and series resistances. Future work will be directed at improving the D_{it} of dielectric directly on Ge to improve the electrostatic control of the gate and the off-state leakage that has been seen especially in planar Ge p-MOSFETs on SGDOI. The second problem related to the scaling of these devices is the series resistance. Improved series resistance contacts with Ni alloyed raised source/drains will be of interest to reduce the contact resistance for these devices.

Finally, a complimentary n-type MOSFET will be required in order to continue the transition from Si to more advanced materials. Compound, III-V semiconductors are promising,

but the integration between III-V and Ge devices on the same wafer is highly challenging. N-type Ge MOSFETs have been of interest although their performance relative to III-V semiconductors is inferior, but few results have shown promise for full Ge CMOS. A summary of suggested future work includes:

- Development of a different final etch for SGDOI to prevent defect delineating etching
- Improvement of the interface between Ge and HfO_2 to improve sidewall and backside D_{it}
- Change in the metallization of the source and drain contacts to form a lower series resistance contact
- Scaling of asymmetrically strained Ge p-MOSFETs to determine the viability of strained Ge as a channel material
- Preliminary studies on the use of high tensile strained Ge as an n-type channel material for CMOS

Appendix A. SGDOI Substrate Fabrication Process Flow

The procedures outlined below are for the fabrication of SGDOI. The machines utilized in SGDOI fabrication are located in the Microsystems Technology Laboratories at MIT unless otherwise noted.

Epitaxial wafers:

Step #	Step	Details	Machine
1	Pre-Epi RCA	10 min. SC-1, 15s HF, 15min. SC-2, 15s HF	RCA/ICL
1	Epitaxial growth	SiGe, Si and Ge	Epi-Centura
2	High-K passivation	Immediate HfO_2 deposition (~10 nm)	ALD/ICL
3	LTO deposition	Immediate transfer, using dedicated cage, ~500 nm **Note: HfO_2 will be buried after this step**	6C-LTO/ICL
4	LTO anneal	Immediate anneal (550C, 30min.) to densify oxide	A1/TRL
5	Elipsometry	Thickness measurement	UV1280/ICL
6	LTO planarization	Outside vendor – To remove the cross-hatch	Entrepix
7	Post-CMP clean	Double Piranha – Check wafers after double piranha for pinholes (reject wafers if pinhole is present)	Premetal-Piranha/ICL
8	Elipsometry	Thickness measurement	UV1280/ICL

Handle wafers and bonding:

Step	Step	Details	Machine

#			
1	RCA clean	Standard RCA	RCA/ICL
2	Oxidation	Tox=100nm after dry oxidation	5C/ICL
3	Dry surface activation (Both wafers)	Recipe: iaberg-O2, 20s, chamber A	AME5000/ICL
4	Wet surface activation	3 min. Piranha to prevent the piranha from attacking too much of the wafer in case of pinholes in the oxide.	Acidhood-2/TRL
5	Wafer bonding (SDB)	note: no bond chamber	EV620/TRL
6	Post-bond anneal	300C for 5 hours	A1/TRL
7	Wafer Grinding and CMP	Outside vendor	SQI
8	Wafer clean	Double Piranha	Premetal-Piranha/ICL
9	Backside protection	Oxide deposition – 2um of oxide deposited with 4 separate depositions of 0.5um at a time.	DCVD/ICL
10	TMAH etch	~10 hrs until the cross-hatch of the graded buffer layer is visible by eye. It is important to rinse the cassette thoroughly after 50:1 HF removal of the native SiO_2 to prevent salt formation.	TMAH/ICL
11	SiGe etch	1:2:3 $HF:H_2O_2:CH_3COOH$ - 2hours after mixing should be waited for the etch rate to become stable. Etching should be ~15-20 minutes until the entire wafer color stabilizes. The etch rate of the s-Si is ~1nm/min.	Acidhood2/TRL
12	TMAH dip	Remove etch stop 10s. TMAH temperature should be 80C, and the wafer can be removed once the color	Acidhood2/TRL

		stabilizes.	
13	SiGe etch	1:2:3 HF:H_2O_2:CH_3COOH 15s. The wafer should be removed immediately after the color stabilizes.	Acidhood2/TRL
14	Elipsometry	Thickness measurement	UV1280/ICL

Appendix B. SGDOI Substrate Fabrication Process Flow

The procedures outlined below are for the fabrication of asymmetrically strained Ge nanowire trigate p-MOSFETs. The machines utilized in SGDOI fabrication are located in the Microsystems Technology Laboratories at MIT unless otherwise noted.

Step #	Process Step	Process Details	Machine Name
1	Elipsometry	Measure exact Si/Ge thicknesses	UV1280/ICL
2	PR Coating	Recipe: T1HMDS	coater6/ICL
3	Photolithography	E-beam alignment-mark (EAM) layer, Reticle: POUYA-NW-SC1, Recipe: NWSC-EAM Dose: 140 ms Focus: 0 um	i-stepper/ICL
4	PR Developing	Recipe: PUDDLE3	coater6/ICL
5	Etch EAM	Recipes: POUYA SI ETCH1 10s	AME5000/ICL
6	Ion Implantation	5keV 4×10^{15} cm^{-2} B implant	Innovion
7	PR Ashing	Ash 4:15	Asher/ICL
8	Etch HfO2/SiO2	10 min. 50:1 HF	Acidhood2/TRL
9	Ellipsometry	Check SiO2 thickness	UV1280/ICL
10	PR Coating	Recipe: T1HMDS	Coater6/ICL
11	Photolithography	E-beam alignment-mark (EAM) layer, Reticle: POUYA-NW-SC1, Recipe: NWSC-EAM Dose: 140 ms Focus: 0 um	i-stepper/ICL
12	PR Developing	Recipe: PUDDLE3	coater6/ICL
13	Ion Implantation	5keV 4×10^{15} cm^{-2} BF_2 implant	Innovion
14	PR Ashing	Ash 4:15	Asher/ICL
15	Etch HfO2/SiO2	2 min. 50:1 HF	Acidhood2/TRL
16	Ellipsometry	Check SiO_2 thickness	UV1280/ICL

17	Etch until depth 250nm	Add additional time in 50:1, etch rate for SiO_2 ~30nm/min (6 min.)	Acidhood2/TRL
18	Ellipsometry	Check SiO_2 thickness	UV1280/ICL
19	Prebake	at 200°C for 2 minutes on Al foil	Hot-plate/TRL
19	Spin HSQ	Bringing resist to the room temperature, drop by PP pipettes all over the wafer, spin at 1000 rpm for 10s then 3500 rpm for 1 min.	coater/TRL
20	Prebake	at 200°C for 2 minutes on Al foil	Hot-plate/TRL
21	E-beam Exposure	Immediately after spin, using Raith 150™, e-beam energy: 30 keV (with SEM imaging operated at SE mode), field size: 100 μm, beam diameter: 2 nm, areal dose: 1200 $\mu C/cm^2$, beam current: ~230-280 pA	Raith150/SEBL
22	Development	within 8 hrs (often immediately), in 25% TMAH for 60 sec, spin/rinse/dry	Acidhood2/TRL
23	Post SEBL Clean	10:1 H2SO4:DI 1 min.	Acidhood2/TRL
24	Post-SEBL Clean	Ash for 4 min. to make sure latex nanoparticles are removed	Asher-ICL/ICL
25	PR Coating	Recipe: T1HMDS	coater6/ICL
26	Photolithography	Mesa layer, Reticle: POUYA-NW-SC1, Recipe: NWSC-STI-NEW Dose: 140 ms Focus: 0 um	i-stepper/ICL
27	PR Developing	Recipe: PUDDLE3	coater6/ICL
28	Metrology	Check if the photo to e-beam alignment is acceptable, if not go to step 26	SEM/ICL
29	Trigate Etch	POUYA-NW-ETCH: main-etch: 5s 30 sccm Cl_2/30 sccm HBr, soft-etch: 5s 15 sccm Cl_2/45 sccm HBr,	AME5000/ICL

		over-etch: 7s 60 sccm HBr	
30	Metrology	Check to make sure that all of the Si/Ge is removed	UV1280/ICL
31	PR ash	2 minutes ashing	Asher/ICL
32	Remove HSQ	BOE 40s	oxEtch-BOE/ICL
33	Ellipsometry	Verify that the SiO2 is completely removed	UV1280/ICL
34	Pre-ALD Si cap removal/clean	NH4OH:DI 10:1 – To be done with clean quartzware labeled CMOS ALD 1.5 min.	Acidhood2/ICL
35	ALD	Immediate transfer, wafer temp.: 250°C, manifold temp.: 110°C, 5 cycles 60s O_3, 45 cycles HfO_2, bring manifold temp. to 110°C, 1200-1400 cycles WN at 345°C ramp to 355°C	ALD/ICL
36	PR Coating	Recipe: T1HMDS	coater6/ICL
37	Photolithography	Gate layer, Reticle: POUYA-NW-SC1 POUYA-NW-SC1, Recipe: NWSC-FG Dose: 145 ms Focus: 0 um	i-stepper/ICL
38	PR Developing	Recipe: PUDDLE3	coater6/ICL
39	Metrology	Check if the alignment is acceptable, if not ash PR and then go to step 35 until desired alignment is achieved	Microscope/ICL
40	Gate Etch	Recipe: WN-ETCH2: 45 sec main etch, very high selectivity to HfO_2	Rainbow/ICL
41	Ellipsometry	to verify WN is fully etched	UV1280/ICL
42	Ion Implantation	Boron implant, no tilt, dose: 4×10^{15} cm^{-2}, energy: 5 keV	Innovion Corp.
43	PR Ashing	4:15 minutes ashing	Asher-ICL/ICL
44	PR Coating	Recipe: T1HMDS	coater6/ICL

45	Photolithography	Contact via layer, Reticle: POUYA-NW-SC4, Recipe: NWSC-FV4 Dose: 140 ms Focus: 0 um	i-stepper/ICL
46	PR Developing	Recipe: PUDDLE3	coater6/ICL
47	Remove HfO2 in vias	50:1 HF 40s	Acidhood2/ICL
48	PR Ashing	Ash 3 min.	Asher/ICL
49	ILD Deposition	DCVD – Oxide-CHC2kA	DCVD/ICL
50	Elipsometry	t_{ox} = 200-220 nm	UV1280/ICL
51	S/D Activation	at 500°C for 30 min. in N2	A3-Sinter/TRL
52	PR Coating	Recipe: T1HMDS	coater6/ICL
53	Photolithography	Contact via layer, Reticle: POUYA-NW-SC4, Recipe: NWSC-FV4 Dose: 140 ms Focus: 0 um	i-stepper/ICL
54	PR Developing	Recipe: PUDDLE3	coater6/ICL
55	Oxide RIE	Time-controlled partial oxide etch, Recipe: BASELINE OX NEW	AME5000/ICL
56	Elipsometry	t_{ox} = 30 nm at the worst case	UV1280/ICL
57	PR Ashing	Ash 3 min.	Asher/ICL
58	Clean Wafer and open vias	green piranha/timed 50:1 HF to remove remaining SiO2 left in windows, check the oxide etch-rate on dummy wafer first, overetch 10%, etchrate ~ 20 nm/min.	Piranha/ICL
59	Elipsometry	t_{ox} < 1 nm	UV1280/ICL
60	Metal Deposition	Recipe: CAIT-Ti-Al, 1 kÅ Ti/ 1 µm Al deposition + two dummies	Endura/ICL
61	PR Coating	Recipe: T1HMDS	coater6/ICL
62	Photolithography	Metal layer, Reticle: POUYA-NW-SC2, Recipe: NWSC-MV1 Dose: 125 ms	i-stepper/ICL

		Focus: 0 um	
63	PR Developing	Recipe: PUDDLE3	coater6/ICL
64	Metal RIE	Metal Etch, recipe: Pouya-metaletch-AlTi:120 sec + 5 sec overetch	Rainbow/ICL
65	Elipsometry	to verify metal is fully etched	UV1280/ICL
66	PR Ashing	3:30 minutes ashing	Asher-ICL/ICL
67	Forming-Gas Anneal	450°C, 30 min in forming gas (H_2/N_2)	A3-Sinter/TRL

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