Investigation of the Electron Transport and Electrostatics of Nanoscale Strained Si/SiGe Heterostructure MOSFETs

by

Hasan M. Nayfeh

B. S. University of Illinois at Urbana-Champaign (1996)

S. M. Massachusetts Institute of Technology (1998)

Submitted to the

Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2003

Signature of Author_____

Department of Electrical Engineering and Computer Science March 7, 2003

Certified by ____

Dimitri A. Antoniadis, Professor of Electrical Engineering, Thesis Supervisor

Accepted by_____

Arthur C. Smith, Professor of Electrical Engineering, Graduate officer

Investigation of the Electron Transport and Electrostatics of Nanoscale Strained Si/SiGe Heterostructure n-type MOSFETs

by

Hasan Munir Nayfeh

Submitted to the Department of Electrical Engineering and Computer Science on March 7, 2003 in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

Abstract

This thesis presents work aimed at investigating the possible benefit of strained-Si/SiGe heterostructure MOSFETs designed for nanoscale (sub-50-nm) gate lengths with the aid of device fabrication and electrical measurements combined with computer simulation.

MOSFET devices fabricated on bulk-Si material are scaled in order to achieve gains in performance and integration. However, as device dimensions continue to scale, physical constraints are being reached that may limit continued scaling and/or the gains in performance from scaling. In order to continue the benefits of scaling, a possible solution is to change to a strained-Si/SiGe material system where enhanced electron mobility of 1.7-2X has been demonstrated for long-channel n-type devices. The electron mobility enhancement observed for long channel length devices may not be the same for devices with nanoscale gate length. In particular, increased channel doping, which is required to control short-channel effects can result in degraded transport characteristics. In this work, the impact of high channel doping on mobility enhancements in strained-Si n-MOSFETs is investigated experimentally. Increased channel

doping will increase Coulomb scattering interactions increasing its influence on the overall mobility.

Electron transport models were calibrated using experimental data for both strained and un-strained Si devices for various channel doping concentrations. The transport models were then used to investigate, by computer simulation, the performance enhancement of nanoscale strained Si devices for equivalent off-current.

Thesis Supervisor: Dimitri A. Antoniadis

Title: Professor of Electrical Engineering

Acknowledgments

I would like to thank my advisor, Prof. Dimitri Antoniadis for supporting this research project and for teaching me the essentials of being a successful researcher. Prof. Judy Hoyt provided guidance during this work as my co-advisor. Closely working with her taught me fundamental skills in performing high quality research. I would like to thank Prof. Eugene Fitzgerald and his students for providing wafers used in this work and his words of encouragement. Professor Tayo Akinwande acted as a reader for this thesis, and provided moral support throughout my graduate student career.

I have benefited from my fellow students in my research group, both past and present members including: Dr. Mark Armstrong, Dr. Anthony Lochtefeld, Dr. Keith Jackson, Dr. Andy Wei, Dr. Ihsan Djomehri, Ali Khakifirooz, Issac Lauer, Andy Ritenour, and Osama Nayfeh. I would like to thank industry collaboration including Dr. Hitoshi Wakabayshi from NEC Corporation, Japan, Dr. Toshihoko Miyashita from Fujitsu Japan, Dr. Jongwan Jung, SAMSUNG Korea, Dr. Shaofeng Yu, INTEL Corporation. My Semiconductor Research Corporation mentors have provided me with encouragement and helpful advice. They include: Dr. Ken Rim, IBM, Dr. Jack Kavalieros, INTEL, and Dr. H.-S Philip Wong, IBM. I would like to thank Ammar Nayfeh, Ph.D. student from Stanford for exciting discussions on the future of silicon microelectronic devices. This work would not have been possible without the assistance of the MTL staff, including: Dr. Vicky Diadiuk, Bernard Alamariu, Paul Tierney, Joe Walsh, Dan Adams, Kurt Broderick, Paudely Zamora, Michael Hobbs, and Michael McIlrath. I thank my family, most of all my wife **Majd** whose patience and encouragement were instrumental for me to achieve success not only with my Ph.D. research, but life in general. I would like to thank my parent's: my father, Prof. Munir Nayfeh for instilling in me the love of science from an early age, and my mother Hutaf Nayfeh for supporting me and encouraging me to seek excellence in whatever I do. Special thanks to Dr. Fahim Jauhary and Wajiha Abu-Hassan for moral support throughout.

Finally, I thank God for providing for my family and for giving us the gift of a healthy son, Munir who was born during the last year of my Ph.D. research (March 7, 2002).

Contents

1 Introduction

1.1. Motivation.....27

1.2. The Piezoelectric Effect.....29

1.3. Strain-induced Energy Band Splitting.....30

1.4. Inducing Stress in MOSFET channels.....32

1.5. Benefits of short-channel strained Si n-MOSFETs.....36

1.6 Goals of Thesis.....37

1.7. Thesis Organization.....40

2 Inversion Layer Electron Transport in Strained Si n-MOSFETs With High Channel Doping Concentration

2.1. Motivation: Importance of Coulomb Scattering in Short-Channel n-MOSFETs.....42

2.2. Experiments: Fabrication of Long-Channel n-MOSFETs.....44

2.3. Mobility Measurements.....47

2.4. Critical Analysis of Mobility Measurements.....54

2.5. Construction of a Coulomb Mobility Model.....56

2.6. Discussion: Critical Analysis- Why Does Mobility Enhancement Diminish For Carrier Transport Dominated by Coulomb Scattering?.....58

2.6.1. Rutherford's Scattering Formula.....59

2.6.2. Energy Levels in Nanoscale Strained and unstrained Si devices.....60

2.6.3. Evidence from Research Literature.....64

2.7. Summary.....67

3 Investigation of the Performance Enhancement of Nanoscale Strained Si MOSFETs

3.1. Introduction.....68

3.2. Nanoscale Device Structure.....69

3.3. Electron Transport Model Calibration for strained and unstrained Si n-MOSFETs.....71

3.4. Transport Model Calibration (high-lateral electric field).....77

3.5. Influence of loss of Coulomb Scattering Limited Mobility Enhancement on the on-current.....82

3.6. Influence of the strained Si heterostructure on the electrostatics.....85

3.7. Threshold Voltage of Strained Si n-MOSFETs.....86

3.7.1. Influence of Channel Length on the Threshold voltage shift.....94

3.8. DIBL and Sub-Threshold Slope.....96

3.9. Scaling Methodology for nanoscale strained Si MOSFETs.....101

3.10. Conclusions.....103

4 Design of Strained Si/SiGe CMOS Transistors

4.1. Motivation.....105

4.2. Layer Structure.....105

4.3.Electrostatic Modeling.....108

4.4. Modeling of Buried-Channel p-MOSFETs Devices: Quantum Mechanical Simulation.....115

4.5.Scaling to sub-50 nm Gate Length.....120

4.6.Conclusions.....120

5 Conclusion

5.1. Summary of Results.....121

5.2. Suggestions for future work:
Fabrication of nanoscale strained Si n-MOSFETs.....122

5.2. Suggestions for future work:
Ultra-thin body strained Si MOSFETs.....123

References.....126

A Strained Si n-MOSFET Fabrication Process.....140

B Low Resistivity Titanium Germanosilicide Formation at Low Temperature for Strained-Si n-MOSFET Applications.....172

B.1. INTRODUCTION.....172

B.2. EXPERIMENTAL PROCEDURE 174

B.3. RESULTS AND DISCUSSION.....174

B.3.1. Film Morphology and Crystallography.....177

B.4. CONCLUSIONS.....178

List of Figures

Fig. 1.1. Illustration showing applied normal stress, σ, and shear stress τ vectors.

Fig. 1.2. Illustration of strain-induced energy bandsplitting in silicon [4]. The applied stress is assumed to be biaxial and tensile. The strain results in a breaking of the degeneracy in the conduction band so that the in-plane valleys, Δ_4 are increased in energy with respect to the out of plane valleys, Δ_2. The splitting results in improved mobility or reduced resistance.

Fig. 1.3. Calculated kinetically limited critical thickness for strained silicon films grown on $Si_{1-x}Ge_x$ [7]. The calculation is based on misfit formation dynamics.

Figure 1.4. Illustration of a strained Si substrate. The top thin silicon layer is lattice matched with the $Si_{1-x}Ge_x$ virtual substrate beneath, resulting in application of biaxial tensile strain to the layer.

Fig. 1.5. Electron mobility in strained Si n-type MOSFETs versus vertical electric field, E_{eff}. The plot shows enhanced mobility with increased strain achieved by increasing the Ge fraction in the relaxed $Si_{1-x}Ge_x$ layer beneath the strained Si device layer [9].

Fig.1.6. N-type MOSFET I_{on}-I_{off} characteristics demonstrating greater than 15% I_{on} improvement for a particular I_{off}. The gate length of the devices studied is about 70 nm [12].

Fig. 1.7.Source, drain, and super-halo doping contours in a 25 nm n-MOSFET design. The surface doping required is about $5x10^{18}$ cm^{-3} and the pocket doping is approaching $1x10^{19}$ cm^{-3} [13].

Fig. 1.8. Inversion layer electron mobility in bulk Si (unstrained Si) n-MOSFETs versus vertical effective electric field, E_{eff} [14]. Universal behavior with doping is shown, with the behavior changed for the highest doping level studied, where the mobility is degraded and attributed to increased Coulomb scattering.

Fig. 2.1. Experimental measurements showing reduced source-side velocity with decreasing gate length or increased channel doping concentration for sub 50 nm n-MOSFETs [11]. The reduction is attributed to increased Coulomb scattering.

Fig. 2.2. Electron velocity along the channel of a n-MOSFET device with 25 nm channel length computed using full band Monte Carlo/Poisson computer simulations [15]. The source-side velocity is shown to be significantly reduced when Coulomb scattering is properly taken into account. The simulations also show a case where the device simulated uses a metal gate material so that Coulomb interactions between dopants in the gate material are eliminated, resulting in increased velocity.

Fig. 2.3. High-resolution cross-sectional TEM, XTEM of the device layer taken beneath the gate stack of a strained-Si n-MOSFET which consists of a thin pseudomorphic tensile-strained 8 nm-thick Si layer.

Fig. 2.4. Ge molecular fraction relative to Si vs. depth for strained-Si n-MOSFETs for a channel ion implant doping boron dose of $7x10^{13}$ cm $^{-2}$ and a control, non- ion implanted strained-Si sample.

Fig. 2.5. Electron mobility limited by alloy scattering in a Silicon n-MOSFET device versus Ge fraction in the channel of the device. The plot shows the mobility for various interaction potentials [16].

Fig. 2.6. Drain current vs. gate voltage for bulk-Si and strained -Si n-MOSFETs with varying boron channel ion implant doses. The drain voltage V_{ds}, used, 10 mV, is small enough so that the MOSFETs operate in the linear regime of operation, and surface potential variations along the length are small.

Fig. 2.7. Increase in lateral electric field and gate-soure/drain capacitance, C_{gds} normalized to the maximum value of V_{ds}/L for the lateral field and C_{ox} for the capacitance. Both values are plotted versus V_{gs} and show similar dependence demonstrating the accuracy of using C_{gds} experimental data to determine the lateral electric field versus V_{gs}.

Fig. 2.8. Gate to channel capacitance for strained and unstrained Si n-MOSFET devices with varying channel doping concentration. The length and width of the devices are 50 μm, and the oxide thickness is t_{ox}=45 nm.

Fig. 2.9. Channel doping concentration vs. depth from the SiO_2/poly-Si interface for varying boron ion implant doses used for strained-Si and bulk-Si MOSFETs. The profile was determined using secondary ion mass spectrometry, SIMS.

Fig. 2.10. logIV plot of a bulk Si and strained Si n-MOSFET devices with matched threshold voltage. The threshold voltage was matched by doping the strained Si with twice the dose compared to bulk Si.

Fig 2.11. Effective electron mobility versus vertical effective electric field, E_{eff}, for various channel doping concentrations for unstrained and strained Si n-MOSFETs.

Fig. 2.12. Mobility versus effective vertical electric field, E_{eff} demonstrating the influence of the lateral field correction on the mobility extraction at low E_{eff}. The correction tends to reduce the rate of decrease of mobility with E_{eff}.

Fig. 2.13. Mobility enhancement, r, versus vertical effective electric field, E_{eff}, showing reduced mobility enhancement with decreasing E_{eff} for a strained-Si channel doped higher than unstrained. Significant enhancement is observed for similar doping for all E_{eff}.

Fig. 2.14. Coulomb limited mobility in strained Si plotted on a log-log scale versus inversion charge areal density, N_i, calculated for three different channel doping concentrations, N_a. The Coulomb mobility was calculated using a Matthiessen's rule summation for the total mobility based on the measurement data. The data show a power-law dependence on N_i and N_a.

Fig. 2.15. Comparison of measured data with calculated inversion electron mobility vs. E_{eff} in relaxed and strained Si n-MOSFETs with channel doping concentration N_a=3.9x10^{18} cm^{-3} and N_a=5.5x10^{18} cm^{-3} respectively. The analytical expression for Coulomb mobility component was the same for both strained and relaxed Si, while the "universal" component was extracted by fitting to the high Q_i portion of the experimental data for the two cases as described in the text.

Fig. 2.16 Illustration of Rutherford's scattering experiment of alpha particles with a gold foil. The experiment helped lead to the development of the nuclear model of the atom.

Fig. 2.17. Illustration of strain-induced band splitting resulting in a splitting of the six-fold degeneracy in the conduction band into two perpendicular Δ_2 valleys and four parallel Δ_4 valleys where the amount of splitting is given by ΔE_s which is a function of the amount of strain. The lower figure illustrates additional splitting due to quantum confinement of the inversion layer electrons near the Si/SiO_2 surface. The subband energy levels are expressed as E_{ij} where the j is the j^{th} energy level in the i^{th} valley (1: Δ_2, 2: Δ_4) , e.g. E_{11} is the ground state energy for the Δ_2 valley

Fig. 2.18. Percentage occupancy of inversion layer electrons in three subband energy levels in a bulk-Si n-MOSFET device with equivalent oxide thickness and doping as the devices analyzed in this work. The values were calculated using a self-consistent Poisson-Schrodinger computer simulation. The figure demonstrates over 90% of the electron population resides in the three subband levels, E_{11}, E_{12} and E_{21}.

Fig. 2.19(a). Subband energy levels as a function of gate voltage. The plot demonstrates that quantum confinement has split the energy subband energy levels so that the ground state, E_{11}, varies from 100-200 meV from the initial conduction band with no confinement, and that E_{21} and E_{12} are roughly at the same energy level.

Fig. 2.19(b). Subband energy levels as a function of gate voltage for a strained-Si n-MOSFET with 20% relaxed Ge beneath the strained-Si layer. The quantum confinement results in a splitting of the subband energy levels, but, due to strain-induced bandsplitting, E_{21} is lifted in energy relative to E_{12} breaking the degeneracy calculated for the bulk-Si n-MOSFET.

Fig. 2.20. Computer simulations of the enhancement of electron mobility versus strain or percent Ge in the relaxed layer beneath the strained-Si ($Si_{1-x}Ge_x$) for three different optical phonon parameters where the values changed are the phonon energy and deformation potential so that the coupling of inversion layer electrons to higher subband energy levels can be changed [29]. The simulation results are plotted against experimental data and show that close matching occurs for the phonon parameters that have higher coupling (increased deformation potential) and in the limit of no coupling (only intravalley scattering mechanisms) the mobility enhancement is diminished.

Fig. 2.21. Coulomb mobility calculated using a Monte-Carlo simulator with a comprehensive coulomb mobility model incorporated into it [20]. The mobility is plotted for two different values of strain and shows slight enhancement of mobility, supporting the experimental findings of this work.

Fig. 2.22. Experimentally measured increase in mobility versus percent uniaxial strain applied by wafer bending for a short-channel n-MOSFET with L_{eff}=45 nm and long-channel with L_{eff}=10 μm [30]. The plot shows that the dependence of strain on mobility is reduced for the short-channel device that is doped heavily to control short-channel effects compared to the long-channel device whose channel doping is low. The plot indicates that mobility enhancement due to strain decreases for short-channel devices due to the increased coulomb scattering of inversion layer electrons.

Fig. 3.1. Cross-section of a nanoscale n-MOSFET device showing a contour map of the channel doping ("super-halo") and relevant physical dimensions. Relevant dimensions include: gate length=25 nm, oxide thickness=1.4 nm, and junction depth=25 nm. The channel doping reaches as high as $1x10^{19}$ cm^{-3} near the source/drain areas, and drops to $3x10^{18}$ cm^{-3} at the surface indicating a super-steep retrograde profile.

Fig. 3.2. Varying scattering mechanisms present in a MOSFET device. The total carrier mobility is achieved by summing the varying components in a reciprocal Mathiessen's rule summation.

Fig. 3.3 Illustration of the Coulomb mobility model used in this work. The model is composed of two parts, screened and unscreened for low inversion layer concentration, N_i. They are combined piece-wise where the maximum is the mobility.

Fig. 3.4.(a) Close agreement between simulated and measured drain current for various channel doping for strained Si n-MOSFETs. Measured data is shown in symbols and simulation results in dashed lines.

Fig. 3.4 (b). Close agreement between simulated and measured drain current for various channel doping for bulk Si n-MOSFETs. Measured data is shown in symbols and simulation results in dashed lines.

Fig. 3.5 (a) Gate to channel capacitance, C_{gc}, for strained Si n-MOSFETs where measurements are shown in symbols and simulations in lines. Close agreement is shown, demonstrating, that the doping concentration has been calibrated accurately.

Fig. 3.5 (b) Gate to channel capacitance, C_{gc}, for strained Si n-MOSFETs where measurements are shown in symbols and simulations in lines. Close agreement is shown, demonstrating, that the doping concentration has been calibrated accurately.

Fig. 3.6. Inversion layer electron velocity versus lateral electric field for unstrained and strained Si n-MOSFETs. The velocity was computed using a numerical solution of Boltzmann's equation using a Monte-Carlo method [38]. From the figure one can observe that the saturation velocity for strained and unstrained Si are the same and that they approach the saturation velocity at the same rate with lateral electric field, so that the Caughey-Thomas parameters are equivalent.

Fig. 3.7 (a) Conduction band energy versus lateral distance in a 25 nm gate length MOSFET. The relevant injection velocity occurs at the peak of the energy versus distance [42].

Fig. 3.7 (b) Electron velocity versus distance in a 25 nm MOSFET. The figure compares two strained Si devices. The first one, has the Coulomb limited mobility enhanced over unstrained Si by 1.75X, while the second device uses has no enhancement. As can be seen, the influence of loss of enhancement of the Coulomb mobility results in a reduction of the injection velocity by 7%.

Fig. 3.8. On-current reduction due to loss of Coulomb mobility enhancement. The plot shows that for reduced gate length, the influence of Coulomb scattering increases. However, the loss of on-current is less than 10% for devices with gate length approaching 20 nm.

Fig. 3.9. I_{on} vs. I_{off} characteristics for strained and unstrained Si devices with equivalent "super-halo" channel doping. The figure shows that the off-current for strained Si devices is larger than that for unstrained for all gate lengths. The reason for the larger off-current, is reduced threshold voltage for strained Si devices.

Fig. 3.10. Threshold voltage versus gate length for strained and unstrained Si devices. The threshold voltage is defined as the gate voltage that results in a drain current of 10^{-7} A/μm. As can be seen, the threshold voltage for the strained Si devices is 50 mV less tan that for the

unstrained Si devices for all gate lengths studied. The channel doping for both devices, is equivalent to the super-halo doping explained earlier.

Fig. 3.11. Energy bandstucture for a strained and unstrained Si n-type MOSFET versus vertical distance from the Si/SiO_2 interface. Both devices are long-channel with channel doping of $5x10^{18}$ cm^{-3}. The bandstructure is extracted in strong inversion with V_{dd}=0.8 V for both devices. As can be seen, the strained Si device has a smaller bandgap material in the quasi-neutral region compared to unstrained Si by 100 meV [43], and furthermore, conduction and valence bandoffsets exist [43-45].

Fig. 3.12 (a) Bandstructure of a strained Si device for a gate voltage such that no band bending occurs in the quasi-neutral region, $Si_{0.8}Ge_{0.2}$.

Fig. 3.12 (b). Net charge concentration for a strained Si device versus vertical distance from the Si/SiO_2 interface. The gate voltage is set as the value required to obtain zero bandbending in the $Si_{0.8}Ge_{0.2}$ quasi-neutral region. As can be seen, there exists a net charge in the strained Si layer equal to the density of ionized dopants. The doping concentration in the device simulated is $2x10^{17}$ cm^{-3}.

Fig. 3.13. Threshold voltage shift, defined as the difference between the threshold voltages of strained Si devices and unstrained Si devices for varying channel doping concentration. The devices studied are long-channel, with gate length of 1μm, so that only doping effects are analyzed. Close agreement can be seen between the analytical formula discussed in the text and

the MEDICI simulations. The shift appears to be constant with doping, but increased in magnitude for doping concentrations greater than $1x10^{18}$ cm^{-3}. The different components of the shift are also plotted demonstrating that the oxide and flatband voltage shift result in increased magnitude of the threshold voltage shift with increased doping concentration.

Fig. 3.14. logIV characteristics of strained and unstrained Si devices with equivalent uniform channel doping concentration of $5x10^{18}$ cm^{-3}. Two gate length devices are studied, long channel with gate length=1 μm, and short-channel with gate length of 25 nm. The plot shows that the shift in threshold voltage, measured in terms of the shift in the logIV characteristics decreases for reduced gate length.

Fig. 3.15. Illustration of charge sharing in a short-channel MOSFET. For short-channel devices, the source/drain potential support a fraction of the depletion charge in the channel, so that the effective integrated charge supported by the gate (Q_b') is smaller than that for long-channel devices (Q_b)

Fig. 3.16 Sub-threshold slope of strained and unstrained Si devices versus gate length. Both devices have super-halo doping channel doping. The slope is slightly larger for the strained devices, due to a slightly larger depletion region depth, and large dielectric constant.

Fig. 3.17. DIBL versus gate length for strained and unstrained Si devices. Both devices have equivalent super-halo doping concentration. The DIBL is almost equivalent for both devices,

eliminating DIBL as a possible cause of off-current differences between strained and unstrained Si devices.

Fig. 3.18. Depletion region depth versus doping concentration for strained and unstrained Si devices, calculated in strong-inversion. The depletion region was calculated using analytical expression discussed in the text. The deletion depth is smaller for strained Si versus unstrained Si devices for a given channel doping concentration.

Fig. 3.19. Simplified MOSFET structure used to analyze short-channel effects of MOSFETs in terms of their depletion depth, w [47]. The potential in the channel can be expressed in terms of analytical expressions, discussed in the text.

Fig. 3.20. Scalelength for strained and unstrained Si devices versus gate length. As can be seen, the scalelength for the strained Si devices is smaller by 2 nm than the unstrained Si devices. As a result, strained Si devices are more scalable, less short-channel effects. However, they are scalable by only 2 nm, so only a slight gain can be seen, as shown in the text.

Fig. 3.21. On-current versus off-current for three devices: (1) unstrained Si, (2) strained Si with increased gate workfunction over n^+ polysilicon of 55 mV, and (3) strained Si with 13% increased channel doping concentration over unstrained Si. The unstrained Si devices has channel doping equivalent to the super-halo discussed earlier in this Chapter. The figure indicates significant I_{on} enhancement for a fixed I_{off} at channel length of 25 nm, for both strained Si devices.

Fig. 4.1. Ideal heterostructure layer for CMOS transistors for enhanced electron and hole performance over bulk Si. The electron channel is tensile strained Si and the hole channel is compressive strain $Si_{1-x}Ge_x$. Both areas are grown on a virtual substrate of $Si_{1-y}Ge_y$ ($x>y$). The left/right side corresponds to n/p-MOS devices. The dark areas denote the location of the electron or hole channel.

Fig. 4.2. CMOS transistor design that provides for performance enhancement. The electron channel is tensile strained Si and the hole channel is compressive strain $Si_{1-x}Ge_x$. Both areas are grown on a virtual substrate of $Si_{1-y}Ge_y$ ($x>y$). The left/right side corresponds to n/p-MOS devices. The dark areas denote the location of the electron or hole channel. The design is called the "dual-channel design".

Fig. 4.3. Drain current versus gate voltage for the dual-layer n-MOSFET design for varying Ge fraction in the hole layer, x. Increased x results in a deviation in the sub-threshold current where the threshold voltage, V_t is reduced and sub-threshold swing, SS increases.

Figure 4.4. Sub-threshold swing (SS) vs. cap thickness (t_{cap}) for the dual-layer n-MOSFET showing increased SS with reduced t_{cap}. The reduced t_{cap} is attributed to an effective reduction in the depletion depth to $x_d=t_{cap}$.

Fig. 4.5. Band diagram in sub-threshold for two gate voltages resulting in operation in the sub-threshold regime for the dual-layer n-MOSFET device. A large hole concentration is present in

the hole layer, which decreases the depletion region depth and results in increased sub-threshold swing, SS.

Fig. 4.6. Sub-threshold swing (SS) vs. cap thickness (t_{cap}) for the dual-layer n-MOSFET calculate using an analytical expression where the semiconductor capacitance is adjusted due to the large hole concentration in the buried layer. The analytical model shows close agreement with the simulations results allowing for accurate prediction of SS with reduced computation expense.

Fig. 4.7. CMOS design where the $Si_{1-x}Ge_x$ is eliminated from the n-MOS device resulting in improved SS. The layers shown for the p-MOS device are grown, where the top two layers are selectively etched to achieve the n-MOS device. The device is named selective etch.

Fig. 4.8. Sub-threshold swing, SS, of the p-MOSFET "selective etch design" compared to the "dual-channel design". The SS is degraded for both designs, compared to a bulk-Si device with the degradation increased for decreasing t_{cap} and increased Ge fraction for the hole layer, x. SS is larger for the selective etch design compared to the dual-layer design due to the strained-Si layer beneath the hole layer that acts to reduce the depletion layer depth

Fig. 4.9. Proposed CMOS structure. The n-MOSFET design shown to the left is a surface-channel device and does not have a hole channel beneath resulting in low sub-threshold slope. The p-MOSFET design show to the right is a buried-channel design where the top silicon layer acts as a gate oxidation sacrificial layer. Beneath the hole layer is a spacer layer that is equivalent

to the virtual substrate that acts to spatially separate the strained-Si layer from the hole layer. The bottom strained-Si layer is the channel layer for the n-MOSFET device, which is achieved by selectively etching the top three layers for the p-MOSFET device.

Fig. 4.10. Sheet charge density in the surface and buried channel for the proposed p-MOSFET structure for varying cap thickness. The figure shows that significant hole confinement in the buried layer occurs for cap thickness of 2 nm.

Fig. 4.11. Drain current versus gate voltage for the p-MOSFET proposed structure for varying cap thickness. The Ge fraction, *x*, was chosen to be 0.60. The figure shows a shift in threshold voltage and an increase in sub-threshold slope with reduced cap thickness, t_{cap} due to confinement in the buried layer.

Fig. 4.12. Sub-threshold swing (SS) of the proposed p-MOS device plotted versus cap thickness, t_{cap}. The SS peaks for t_{cap}=3 nm and then decreases. The initial increase is attributed to increased confinement in the buried well resulting in an increased effective gate insulator thickness. The decrease of SS for t_{cap}< 3 nm is a result of increased carrier confinement in the buried well resulting in reduced gate insulator thickness with decreased t_{cap}

Fig. 4.13. Scaling behavior of the p-MOSFET proposed structure versus bulk-Si reference. It shows worse short-channel effects (larger DIBL, and larger V_t rolloff) due to the channel layer being buried from the gate insulator interface.

Fig. 5.1. Ultra-thin body strained Si substrate. The ultra thin body strained Si film has a thickness of 1/3 the gate length. The gate length, for the device will be sub-20-nm. The silicon film is lattice matched with the source/drain regions, which are comprised of Si1-xGex material, resulting in the film being under biaxial tensile stress.

Fig. 5.2. Electron concentration versus depth from the top Si/SiO_2 interface for ultra-thin body strained Si MOSFET devices. The electron concentration is plotted for varying film thickness devices. The peak of the electron concentration is 1 nm from the interface. Clearly for film thickness approaching 1 nm, scattering at the back Si/SiO_2 interface becomes important, and results in degraded transport characteristics [69].

Fig. B.1. Germanosilicide and silicide resistivity versus reaction temperature for 50 nm of deposited Ti on silicon and $Si_{0.75}Ge_{0.25}$ substrate. The silicide exhibits typical behavior where the formation of the C49 phase precedes the formation of the C54 phase at higher temperature. The germanosilicide exhibits the low resistivity C54 phase at low temperature and suffers from high resistivity due to Ge agglomeration at higher temperatures.

Fig. B.2 XTEM of a film of $Si_{0.75}Ge_{0.25}$ that had a 30 nm Ti film deposited on it and reacted at 560° C. The image demonstrates a smooth interface and the resistivity is low, 22 $\mu\Omega$ cm

Fig. B.3. XTEM of a film of $Si_{0.75}Ge_{0.25}$ that had a 30 nm Ti film deposited on it and reacted at 800° C. The image demonstrates rough morphology due to Ge agglomeration resulting in an increased resistivity of 70 $\mu\Omega$ cm

Fig. B.4. XTEM of a $Si_{0.75}Ge_{0.25}$ film that had a 30 nm Ti film deposited on it and reacted at 700 ^{o} C. The dark areas correspond to $Si_{1-x}Ge_x$ areas due to Ge agglomeration and the light areas are $Ti(Si_{1-x}Ge_x)_2$. The resistivity was measured to be 28 $\mu\Omega$ cm, which is larger than the resistivity of the film that was reacted at 560^{o} C, 22 $\mu\Omega$ cm.

Fig. B.5 XRD data from a $Ti(Si_{1-x}Ge_x)_2$ film that was reacted at 560^{o} C. The solid lines indicate the peaks of the C54 $TiSi_2$ phase. The data exhibit a shift of the (311) crystallography peak from 2-theta of 39.2^{o} to 38.5^{o} due to the presence of Ge in the silicide.

List of Tables

Table 1.1 Target transistor delay, from the 2002 International Technology Roadmap For Semiconductors (ITRS) [2], versus gate length for high-performance n-MOSFET transistors, where shaded values represent transistors required that have unknown manufacturable solutions.

Table 1.2. Piezoresistive coefficients for n and p-type Silicon [3]

Table 1.3. Elastic coefficients for Silicon [8]

Table 3.1. Analytical expressions for mobility limited by the three dominant scattering mechanisms for inversion layer carriers in a MOSFET device: Coulomb, acoustic phonon, and surface-roughness.

Table 3.2. Definitions of the symbols used in the analytical mobility model expressions.

Table 3.3(a-b) Calibrated mobility model coefficients for strained (b) and unstrained Si (a). Increased coefficients for the strained Si mobility model of 1.75X over unstrained Si is used for acoustic-phonon and surface-roughness limited mobility, while equivalent coefficients are used for Coulomb scattering limited mobility.

Table 3.4. Material parameters used for the analysis of strained and unstrained Si devices. Constants obtained from the literature [43-45].

Chapter 1

Introduction

1.1. Motivation

Every three years, a chip manufacturing generation, the semiconductor industry manufactures a high-performance microelectronics logic chip with a four-fold increase in the number of components, according to Moore's Law of Scaling [1]. Moore's Law, which was published in 1965, has accurately predicted the number of components/chip, which is indicative of the computing power of the chip. In particular, during the past 30 years from 1971-2002, the number of components has increased from 2,000 to 42 million. The exponential increase in the number of components/chip with time is predominantly due to the scaling of the size of the discrete transistor device, the MOSFET, in particular scaling the gate length. This scaling results in not only more components/chip, but also increased chip performance of ~20% per generation. Maintaining increased performance of 20% per generation, and tolerable power dissipation, is becoming an increasingly difficult challenge as device gate length scales below 50 nm in this decade and 25 nm into the next decade. One striking example of the difficulty is the leakage current through the gate insulator, which is scaled commensurately with the gate length. The gate insulator, SiO_2, has reached a thickness of 1 nm, or 5 atomic layers thick in current chip

manufacturing, resulting in increased gate leakage due to quantum-mechanical tunneling, and as a result, increased power dissipation. A roadmap for the semiconductor industry which tabulates the physical dimensions and target figures of merit for high-performance logic transistors required for a given chip generation, the International Technology Roadmap For Semiconductors, ITRS [2], indicates the required switching delay of a transistor device. In Table 1.1., values highlighted do not have known solutions in terms of manufacturability.

Year of Production	**2001**	**2004**	**2007**	**2010**	**2013**	**2016**
Technology Node (nm)	130	90	65	45	32	22
Printed Gate Length (nm)	90	53	35	25	18	13
High-Performance n-MOSFET Delay (pS)	1.6	0.99	0.68	0.39	0.22	0.15

Table 1.1 Target transistor delay, from the 2002 International Technology Roadmap For Semiconductors (ITRS) [2], versus gate length for high-performance n-MOSFET transistors, where shaded values represent transistors required that have unknown manufacturable solutions.

Clearly, a means of improving the transport properties of silicon MOSFET devices is required. One method is to change the material that the transistor is fabricated in, with the constraint that the material results in a small change in well-established silicon-based CMOS processing techniques. One promising method of achieving improved transport and not introducing added process complexity is to induce strain in the silicon MOSFET channel.

1.2 The Piezoelectric Effect

The modification of the carrier mobility of Silicon through the application of stress, the piezoelectric effect, is a well-known effect and was first reported by *Smith et. al.* [3], who observed increased carrier mobility with the application of stress to bulk-Si material. An illustration of the experimental setup showing the applied stress vectors is shown in Fig. 1.1.

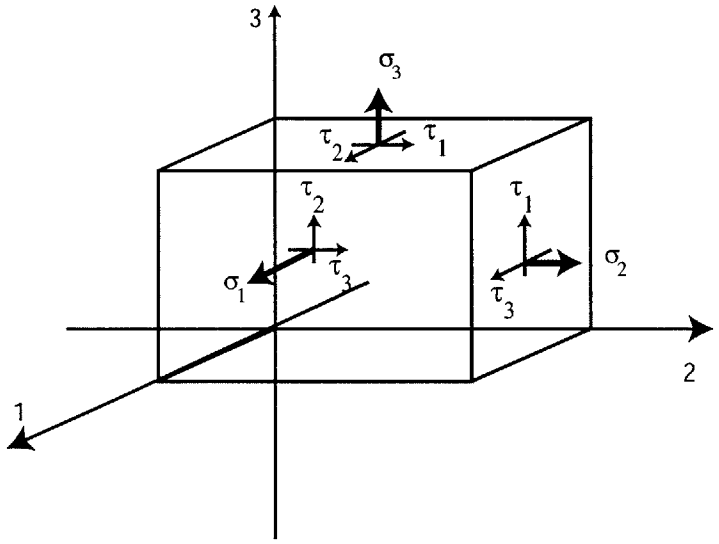

Fig. 1.1. Illustration showing applied normal stress, σ, and shear stress τ vectors.

Using the notation in Fig. 1.1, the change in resistivity, ρ for a particular direction can be related to the applied stress, assuming zero shear stress, as:

$$\frac{\Delta\rho_i}{\rho} = \pi_i^j \sigma_j \qquad \text{Equation 1.1}$$

The piezoelectric coefficients measured for moderately doped p-type and n-type silicon, shown in Table 1.2 indicate that an applied tensile stress parallel to the direction of current flow will result in reduced resistance or increased electron mobility for n-type Si, while a perpendicular stress will increase the resistance. The question then arises- how can stress effects, analogous to the piezoelectric effect be used to improve the mobility of n-MOSFET devices?

Material <100> **Silicon**	**Piezoresistive coefficient [10^{-6}/atm]** π_{11}	π_{12}	π_{44}
p-type ($1.5x10^{15}$ cm^{-3})	6.8	-1.1	142.7
n-type ($4x10^{14}$ cm^{-3})	-105.6	55.2	-14.0

Table 1.2. Piezoresistive coefficients for n and p-type Silicon [3]

1.3. Strain-induced Energy Band Splitting

Before examining how stress can be used to improve the performance of MOSFET transistors, it is instructive to analyze the effect of strain on the microscopic properties of a semiconductor. In particular, strain results in energy band splitting, and can be explained in terms of deformation potential theory where strain can be related to changes in the energy band structure [4]. An example of stress resulting in bandsplitting is the influence of biaxial tensile strain on the conduction energy band levels in silicon. It is well known that the conduction band of silicon is six-fold degenerate. However, the application of biaxial tensile strain results in a breaking of this degeneracy. An illustration of the bandsplitting is shown in Fig. 1.2. The two-fold degenerate in-plane valleys (Δ_2) are lowered in energy, while the four-fold degenerate out of

plane valleys (Δ_4) are raised in energy. The amount of energy splitting between the Δ_2 and Δ_4 valleys is a function of the amount of induced strain.

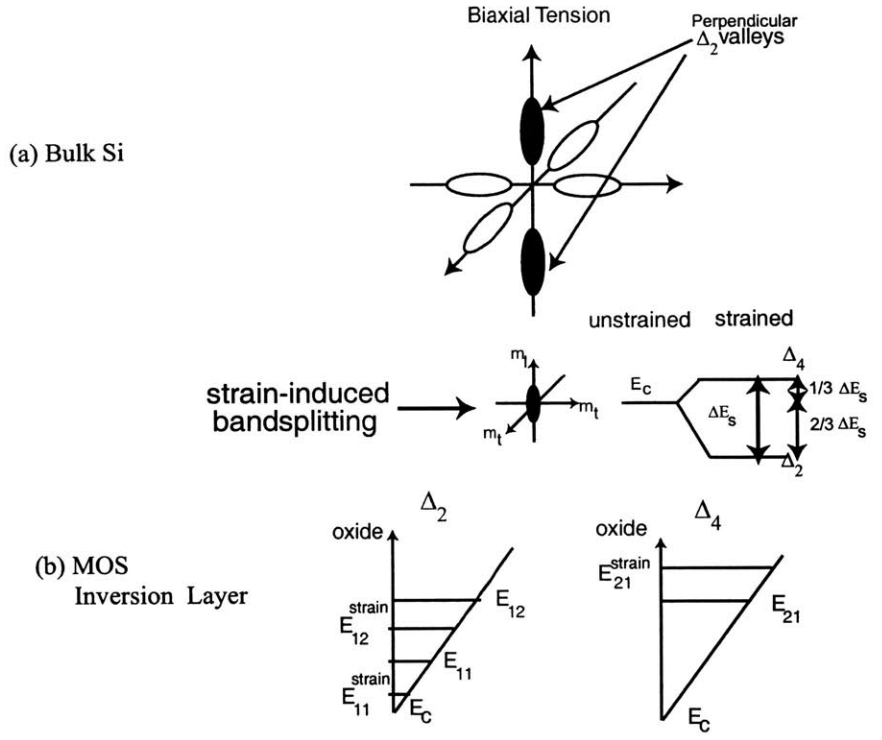

Fig. 1.2. Illustration of strain-induced energy bandsplitting in silicon [4]. The applied stress is assumed to be biaxial and tensile. The strain results in a breaking of the degeneracy in the conduction band so that the in-plane valleys, Δ_4 are increased in energy with respect to the out of plane valleys, Δ_2. The splitting results in improved mobility or reduced resistance. The top part (a) represents bulk Si, while the bottom (b) is for a MOS inversion layer. For the MOS inversion layer, there is additional energy splitting due to electron confinement near the Si/SiO_2 interface.

Since the bands are split, the number of final states for scattering events is reduced, increasing the scattering time, or increasing the mobility and reducing the resistance. Moreover, the conductivity effective mass is also reduced, since the relative population of the heavier electron mass Δ_4 is reduced. These two effects of reduced scattering time and reduced mass, can be related to mobility in an analytical expression by:

$$\mu = \frac{e\tau}{m_c^*} \qquad \text{Equation 1.2}$$

where τ is the momentum scattering time, and m_c* is the conductivity effective mass. In the next section, the used of stress in improving the mobility of electrons in MOSFET transistors will be discussed.

1.4. Inducing Stress in MOSFET channels

Inducing stress in MOSFET channels can be achieved via the technique of pseudomorphic growth of thin silicon layers on relaxed $Si_{1-x}Ge_x$ layers [5]. Due to the lattice mismatch between Si and $Si_{1-x}Ge_x$, the Si layer is under biaxial tensile strain where the amount of strain increases for increased x. The relaxed $Si_{1-x}Ge_x$ layer is typically grown epitaxially. In this work a vertical, hot-wall ultrahigh vacuum chemical vapor deposition UHVCVD reactor was used. SiH_4 and GeH_4 precursors are utilized to grade the Ge fraction to the desired composition at a rate of roughly 10% Ge/μm. The layer is then topped by a 1.5 μm uniform Ge composition cap. The slow grading rate and high growth temperature results in completely relaxed graded layers with threading dislocation densities of approximately 10^5 cm^{-2} . In order to maintain low surface roughness chemical mechanical polishing was performed [6]. Next, the wafers were

reloaded into the reactor for $Si_{1-x}Ge_x$ deposition with 1 um thickness. Finally, the reactor temperature is then dropped to 650° C for the deposition of the strained Si device layer. Strained Si thickness less than the equilibrium critical thickness is chosen to minimize misfit dislocation introduction during elevated processing temperatures [7]. The calculated critical thickness for strain relaxation based on misfit dislocation dynamics is shown below in Fig. 1.3.

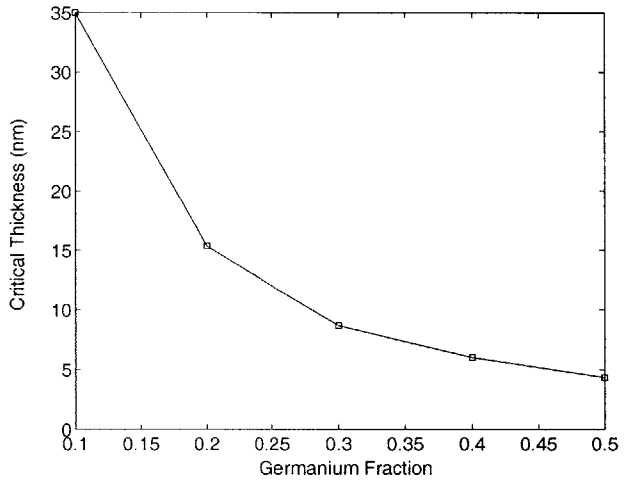

Fig. 1.3. Calculated kinetically limited critical thickness for strained silicon films grown on $Si_{1-x}Ge_x$ [7]. The calculation is based on misfit formation dynamics.

The resulting layers can then be used as a substrate for the fabrication of strained Si MOSFET devices as illustrated in Fig. 1.3.

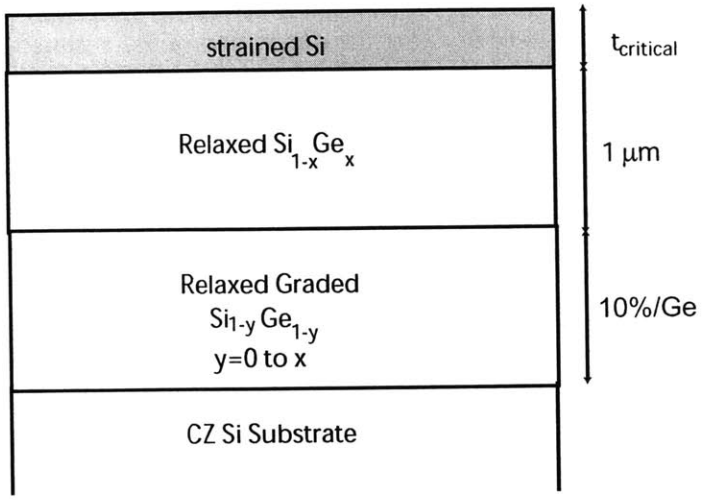

Figure 2.4. Illustration of a strained Si substrate. The top thin silicon layer is lattice matched with the $Si_{1-x}Ge_x$ virtual substrate beneath, resulting in application of biaxial tensile stress to the layer.

The amount of strain induced in the strained silicon layer in the plane, the parallel strain tensor is given by [8]:

$$\varepsilon_{parallel} = \frac{a_{substrate}}{a_{thin-film}} - 1 \qquad \text{Equation 1.2.}$$

The parallel strain tensor can be related to the perpendicular tensor through Poisson's coefficient, ν:

$$\frac{\varepsilon_{parallel}}{\varepsilon_{\perp}} = -\nu \qquad \text{Equation 1.3}$$

The stress and strain vectors are related through Hooke's Law:

$$\sigma_{ij} = C_{ij}\varepsilon_{ij} \qquad \text{Equation 1.4}$$

where the elastic coefficients for silicon are given by [8]:

C_{11} (GPa)	C_{12} (Gpa)	C_{44} (Gpa)
165.77	63.93	79.67

Table 1.3. Elastic coefficients for Silicon [8]

Using these equations, the stress vectors for silicon grown on a relaxed $Si_{0.8}Ge_{0.2}$ layer can be calculated. The lattice constants can be determined by interpolating between the lattice constant of pure Ge, a_{Ge}=5.65 A and Silicon, a_{Si}=5.43. The equilibrium lattice constant for strained-Si is equivalent to Silicon so that $a_{thin\text{-}film}$=5.43 A, while that of $Si_{0.8}Ge_{0.2}$ is equal to $a_{substrate}$=5.476 A, giving: σ_{11}=1.37 GPa and σ_{12}=3.11 GPa. Therefore, a lattice mismatch of approximately 1% results in a stress on the order of GPa. The question to ask is: to what extent does an induced stress of about 1 GPa increase electron mobility in n-MOSFET devices? It appears that significant mobility enhancement can be achieved by inducing a stress on the order of 1 GPa. Electron mobility measurements of long-channel n-type strained Si devices show enhanced electron mobility of 1.7 fold over unstrained-Si control devices for a wide range of vertical electric field [9] for a strained Si substrate using a $Si_{0.7}Ge_{0.3}$ virtual substrate. However, in order for strained Si technology to be of practical use, the enhanced electron mobility observed for long-channel devices should result in improved drain current for deeply scaled short-channel devices.

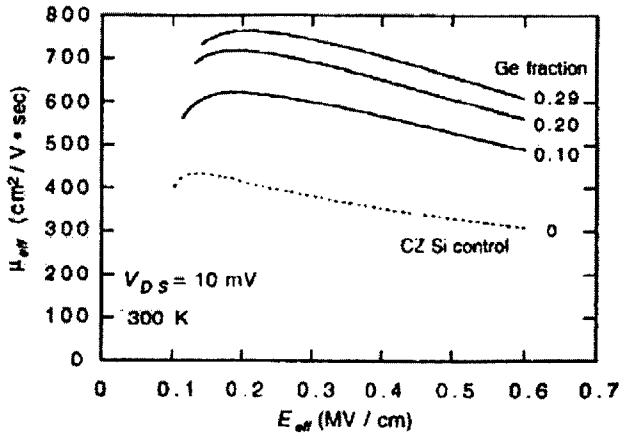

Fig. 1.5. Electron mobility in strained Si n-type MOSFETs versus vertical electric field, E_{efff}. The plot shows enhanced mobility with increased strain achieved by increasing the Ge fraction in the relaxed $Si_{1-x}Ge_x$ layer beneath the strained Si device layer [9].

1.5. Benefits of short-channel strained Si n-MOSFETs

Recent measurements of the virtual source velocity of inversion layer electrons in bulk Si n-MOSFET devices with sub-50-nm gate length, a key indicator of device performance, show that the injected velocity is about one-half of the ballistic thermal limit, B, defined as when the source-side velocity is equal to the thermal velocity of carriers in the source [10]. The B factor can be related to the influence of long-channel low-lateral electric field mobility on the drain current of short-channel devices by the following relation [11]:

$$\frac{\partial I_d}{I_d} = (1-B)\frac{\partial \mu}{\mu} \qquad \text{Equation 1.5.}$$

As a result, increasing low-lateral field mobility should result in increased drain current for short-channel devices. Indeed, strained-Si devices with 70 nm gate length have been fabricated and show improved drain current over unstrained-Si control devices demonstrating the capability of strained-Si to improve the performance of short-channel devices [12].

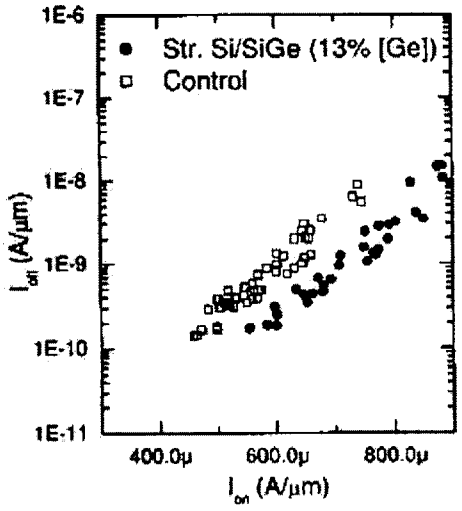

Fig.1.6. N-type MOSFET I_{on}-I_{off} characteristics demonstrating greater than 15% I_{on} improvement for a particular I_{off}. The gate length of the devices studied is about 70 nm [12].

1.6 Goals of Thesis

Improved transport properties of short-channel n-type MOSFETs has been demonstrated using strained Si/SiGe heterostructures with little penalty in processing complexity. However, as MOSFETs device gate length is scaled to less than 50 nm, channel doping concentration is increased to achieve electrostatic integrity resulting in stronger Coulomb interactions between

inversion layer carriers and dopants. An example of the channel doping concentration required in a 25 nm MOSFET is illustrated below in Fig. 1.6. As shown in the figure, the surface doping required is about $5x10^{18}$ cm^{-3} and the halo pocket doping concentration near the source/drain required is about $1x10^{19}$ cm^{-3} [13].

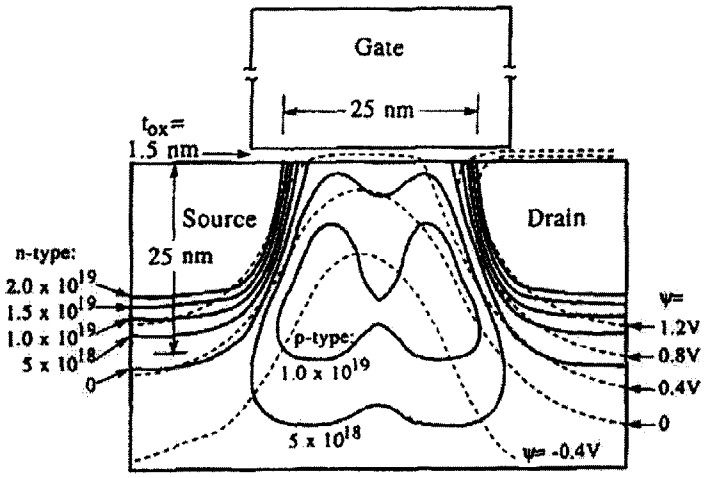

Fig. 1.7. Source, drain, and super-halo doping contours in a 25 nm n-MOSFET design. The surface doping required is about $5x10^{18}$ cm^{-3} and the pocket doping is approaching $1x10^{19}$ cm^{-3} [13].

Degradation of long-channel low-lateral field electron mobility with increased channel doping has been demonstrated experimentally. For low doping concentrations, the mobility versus vertical field, E_{eff} displays universal behavior, and for high doping concentration, greater than $1x10^{18}$ cm^{-3}, the mobility is less than the universal expected mobility, and is explained in terms of increased Coulomb interactions between the inversion layer carrier and channel dopants, as shown in Fig. 1.7. [14].

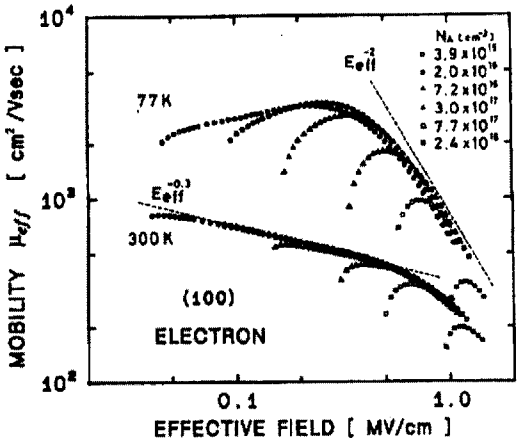

Fig. 1.8. Inversion layer electron mobility in bulk Si (unstrained Si) n-MOSFETs versus vertical effective electric field, E_{eff} [14]. Universal behavior with doping is shown, with the behavior changed for the highest doping level studied, where the mobility is degraded and attributed to increased Coulomb scattering.

In order to determine the performance improvement of nanoscale strained Si n-MOSFETs, defined as having less than 50 nm gate length, the following question needs to be answered: what is the influence of increased Coulomb interactions on the mobility enhancement observed in strained-Si n-MOSFETs? In this thesis, experiments combined with computer simulations are used in order to determine the performance improvement of strained Si n-MOSFETs over bulk Si (unstrained Si). Nanoscale strained Si devices are evaluated by comparing to unstrained Si for the same off-current. Therefore, analysis of the influence of the heterostructure on the electrostatics was performed. The thesis then discusses work aimed at investigating the practicality of implementing strained Si/SiGe heterostructures in a CMOS manufacturable

substrate. A heterostructure layer structure is proposed that provides for enhanced n-and p-type MOSFETs over bulk Si and tolerable electrostatics in terms of sub-threshold behavior.

1.7. Thesis Organization

In Chapter 2 an experimental investigation of the influence of high channel doping on the inversion layer electron transport in strained Si n-MOSFETs is discussed. The experimental results are used to calibrate transport models available in typical semiconductor device computer simulation programs. In Chapter 3, the mobility model is used to predict the performance enhancement of sub-50-nm strained Si n-MOSFETs over bulk Si. Next, in Chapter 4, a substrate that can accommodate both enhanced performance n-and p-type strained Si/SiGe MOSFETs where the devices have tolerable turn-off characteristics in terms of sub-threshold behavior is proposed. Finally, the thesis concludes with suggestions for future work with the emphasis on the implementation of a strained Si on insulator (SSOI) substrate that has the potential of lower leakage and superior performance than the strained Si/SiGe substrate.

Chapter 2

Inversion Layer Electron Transport in Strained Si n-MOSFETs With High Channel Doping Concentration

In this chapter, the dependence of electron inversion layer mobility on channel doping required for sub-50-nm MOSFETs is investigated in strained Si and compared to co-processed unstrained Si. For high vertical effective electric field, E_{eff}, the electron mobility in strained Si displays universal behavior with effective field, E_{eff}, and shows enhancement of 1.5-1.7X compared to unstrained Si. For low E_{eff}, deviation from universal behavior is observed for both the strained and unstrained devices. The mobility of the strained Si devices approaches that of the unstrained Si. The decrease in mobility enhancement is attributed to Coulomb scattering of inversion layer electrons with channel dopants. The mobility data is used to calibrate existing transport models in available in a commercial semiconductor simulation program. The calibrated transport model can then be used to study transport in nanoscale strained Si MOSFETs.

2.1. Motivation: Importance of Coulomb Scattering in Short-Channel n-MOSFETs

Recent measurements of the source-side velocity, v_{source} of inversion layer electrons in bulk Si n-MOSFET devices with sub-50-nm gate length, a key indicator of device performance, show reduced velocity with decreasing gate length as shown in Fig. 2.1. [11]. The measured velocity is normalized with respect to the maximum velocity attainable for a MOSFET, the thermal velocity in the source, $v_{thermal}$ so that a ratio of 1 corresponds to a ballistic MOSFET where no scattering events occur in the channel. Reduced source-side velocity is hypothesized to be due to increased Coulomb scattering between the inversion layer electrons and channel

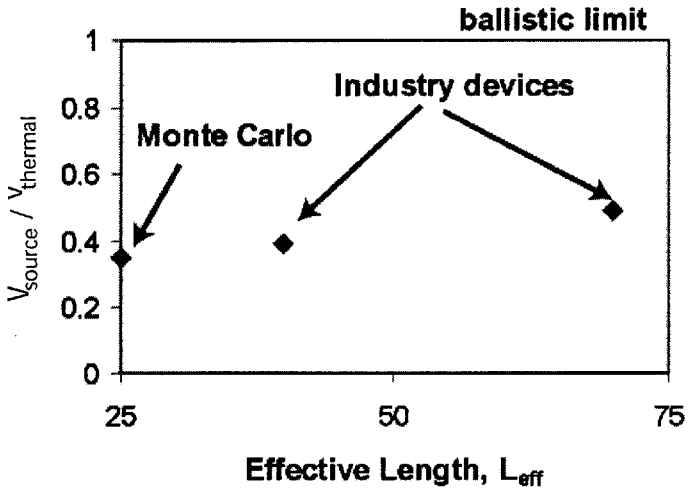

Fig. 2.1. Experimental measurements showing reduced source-side velocity with decreasing gate length or increased channel doping concentration for sub 50 nm n-MOSFETs [11]. The reduction is attributed to increased Coulomb scattering.

dopants. In fact, full-band self-consistent Monte-Carlo/Poisson computer simulations show that Coulomb interactions in short-channel n-MOSFET devices result in a significant reduction of the source-side electron velocity as shown in Fig. 2.2 [15]. Reduced source-side velocity results in degraded device performance, motivating the study of dependence of electron mobility on channel doping in strained Si n-MOSFETs. In this chapter, the dependence of inversion layer electron mobility in strained Si n-MOSFETs fabricated using a typical MOSFET process with channel doping concentration ranging from $1x10^{17}$-$6x10^{18}$ cm^{-3} is discussed. The electrical measurements are then used to calibrate existing transport models.

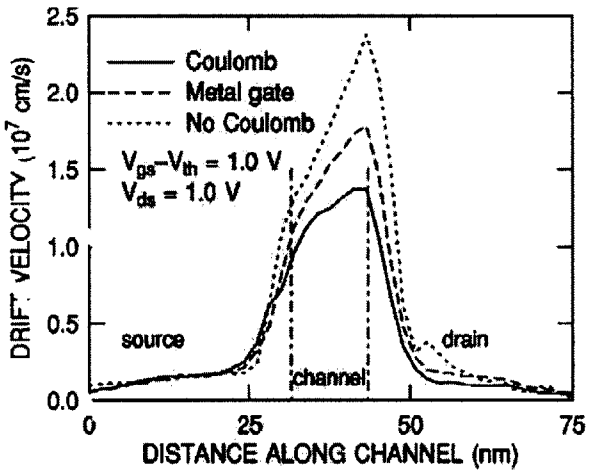

Fig. 2.2. Electron velocity along the channel of a n-MOSFET device with 25 nm channel length computed using full band Monte Carlo/Poisson computer simulations [15]. The source-side velocity is shown to be significantly reduced when Coulomb scattering is properly taken into account. The simulations also show a case where the device simulated uses a metal gate material so that Coulomb interactions between dopants in the gate material are eliminated, resulting in increased velocity.

2.2. Experiments: Fabrication of Long-Channel n-MOSFETs

The strained Si substrates used in this work were grown epitaxially on relaxed SiGe in a vertical, hot-wall ultrahigh vacuum chemical vapor deposition UHVCVD reactor using SiH_4 and GeH_4 precursors. The SiGe virtual substrates were grown on Si to a Ge content of 20% confirmed by Secondary Ion Mass Spectrometry (SIMS) at 900 °C and were topped by a 1.5 μm uniform composition cap after a chemical mechanical polishing of the $Si_{0.8}Ge_{0.2}$ surface. The reactor temperature was then dropped to 650 °C for the deposition of the strained Si device layer. The samples were doped *in situ* p-type to concentrations of $1x10^{17}$ cm^{-3} using B_2H_6 for all layers. High-resolution cross-sectional transmission electron microscopy (XTEM) showed the starting strained Si thickness to be 180 A-thick. Next, a MOSFET process followed where active-area isolation was achieved using a field ion implant followed by a 2000 A-thick deposited low-temperature field oxide. The process flow details are given in Appendix A. After the active areas were opened, Boron channel ion implantation with energy of 10 keV and dose ranging from 1-$7x10^{13}$ cm^{-2} was performed. At equal doping levels, the threshold voltage V_t is reduced in strained Si n-MOSFETs compared to unstrained by ~100 mV for 20% Ge substrate, to be discussed in more detail in Chapter 3. In order to closely match V_t, the channel boron ion implant doses were chosen to be 1.5 to 2X larger for the strained Si devices. Next the gate stack was formed by growth of a 5 nm dry oxide at 800° C for 30 minutes followed by the deposition of polysilicon gate at 625° C. The gate stack was then patterned and etched followed by source/drain and gate ion implant and activation using a high-temperature 1000° C spike anneal.

Metal contacts were formed using 1000 A Ti/1 μm Al followed by sinter in forming gas at 425° C for 30 minutes. XTEM of the gate stack, shown in Fig. 2.2 shows 8 nm-thick strained-Si layer remains. This indicates that 10 nm was lost due to process cleaning and gate oxide growth steps.

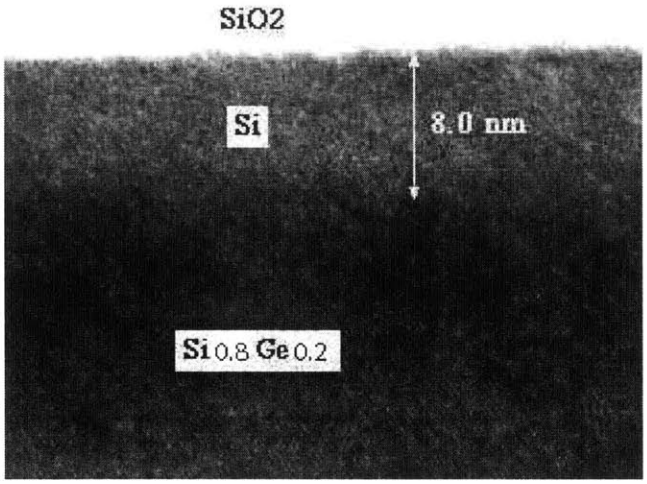

Fig. 2.3. High-resolution cross-sectional transmission electron microscope (XTEM) of the device layer taken beneath the gate stack of a strained-Si n-MOSFET which consists of a thin pseudomorphic tensile-strained 8 nm-thick Si layer. XTEM courtesy of Xiaoman, National Semiconductor.

One concern with using high temperature process steps is germanium diffusion from the $Si_{0.8}Ge_{0.2}$ virtual substrate to the device surface area. The presence of germanium can result in reduced carrier mobility due to alloy scattering of inversion layer electrons. The germanium concentration versus depth, measured using SIMS indicates a low surface Ge molecular fraction of 10^{-3} as shown in Fig. 2.3.

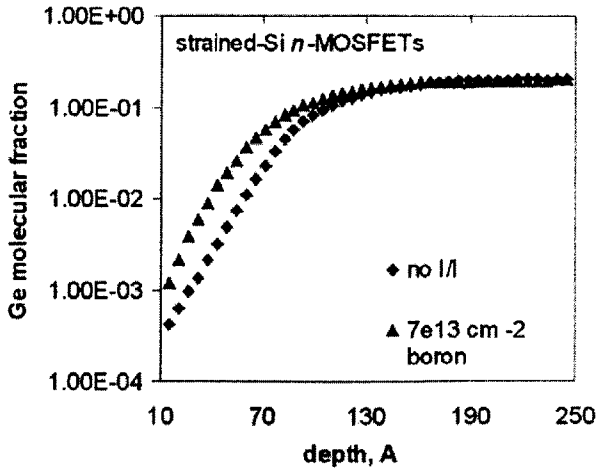

Fig. 2.4. Ge molecular fraction relative to Si vs. depth for strained-Si n-MOSFETs for a channel ion implant doping boron dose of $7x10^{13}$ cm^{-2} and a control, non- ion implanted strained-Si sample.

This surface Ge concentration is not large enough to result in significant alloy scattering. The alloy scattering mobility for varying Ge concentration is shown in Fig. 2.4. calculated by assuming that alloy scattering results in a local change in the Coulomb potential [16]. The plot demonstrates that alloy scattering mobility for this Ge content is extremely large, on the order of

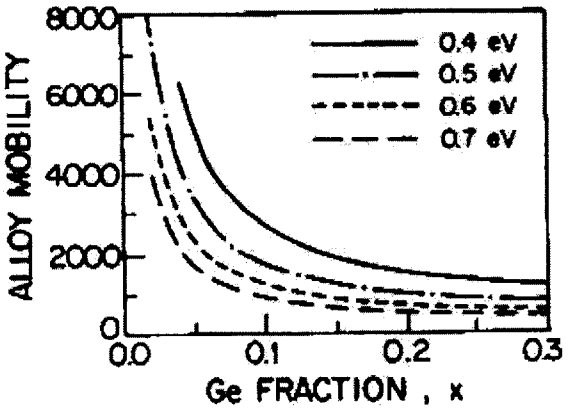

Fig. 2.5. Electron mobility limited by alloy scattering in a silicon n-MOSFET device versus Ge fraction in the channel of the device. The plot shows the mobility for various interaction potentials [16].

several thousand, much larger than mobility typically measured in MOSFET devices. Therefore, the influence of alloy scattering on transport measured in this work is negligible.

2.3. Mobility Measurements

Electron mobility measurements on 50x50 μm^2 devices with electrical oxide thickness, t_{ox}=5 nm were extracted using the split-CV method [17]. Long channel devices were used to measure mobility so that parasitic values such as source/drain resistance are a small fraction of the total device resistance. The mobility, μ, was calculated for gate voltage V_{gs} greater than the linearly extrapolated threshold voltage so that drain current per width (I_d/W) is drift dominated.

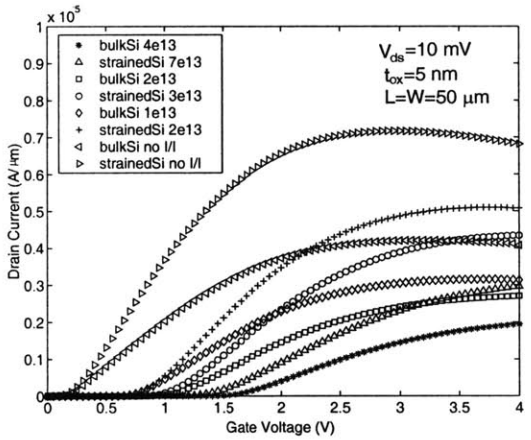

Fig. 2.6. Drain current vs. gate voltage for bulk-Si and strained -Si n-MOSFETs with varying boron channel ion implant doses. The drain voltage V_{ds}, used, 10 mV, is small enough so that the MOSFETs operate in the linear regime of operation, and surface potential variations along the length are small.

As a result, the expression:

$$\mu = \frac{I_d}{WQ_i E_{lat}} \qquad \text{Equation 2.1}$$

can be used, where I_d is measured at a drain voltage (V_{ds}) of 10 mV and Q_i is the inversion layer charge where Fig. 2.6. shows a typical I_d vs. V_{gs} plot. The lateral electric field, E_{lat} is often set to V_{ds}/L, though this is valid only in strong inversion. To improve accuracy in weak inversion near threshold, a correction factor, $f(V_{gs})=C_{gc}/C_{ox}$ was used such that: $E_{lat}=f(V_{gs})V_{ds}/L$, where C_{gc} is the gate to channel capacitance and C_{ox} is the capacitance in strong inversion [17]. Computer simulations were performed to calculate the lateral electric field versus gate voltage in a MOSFET device with oxide thickness and typical channel doping concentration used in this experimental work, and compared to calculated f factor using the expression above. The results indicate close agreement, as shown in Fig. 2.7 demonstrating the accuracy of the method. The effective vertical field, E_{eff}, was calculated using the expression, $E_{eff} = \frac{Q_b + Q_i/2}{\varepsilon_s}$ where Q_i was determined by integrating gate to channel capacitance, C_{gc} to the applied V_{gs} where Fig. 2.8. shows the C_{gc} data for varying channel doped strained and unstrained Si devices. The bulk charge, Q_b was determined using the expression $Q_b = \sqrt{2qN_a\varepsilon_s\varphi_s}$ where ε_s is the semiconductor dielectric constant where the dielectric constant of $Si_{0.8}Ge_{0.2}$ was taken to be 13.1 and q is the elementary electron charge. The channel doping concentration, N_a was determined using inverse modeling technique [18] using measured SIMS profile as an initial guess. A constant profile over the depletion region was assumed based on the SIMS data which shows larger doping used for the strained Si devices as shown in Fig. 2.6.

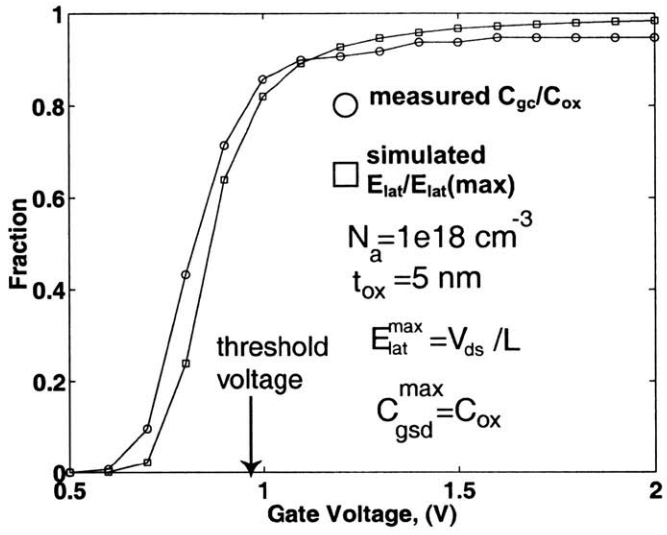

Fig. 2.7. Increase in lateral electric field and gate-soure/drain capacitance, C_{gc} normalized to the maximum value of V_{ds}/L for the lateral field and C_{ox} for the capacitance. Both values are plotted versus V_{gs} and show similar dependence demonstrating the accuracy of using C_{gc} experimental data to determine the lateral electric field versus V_{gs}. Note that mobility was calculated above the threshold voltage, which is indicated in the arrow in the plot, for these conditions.

Larger channel doping concentration for the strained Si devices compared to unstrained was implemented in order to compare strained Si and unstrained Si devices with similar threshold voltage. Fig. 2.10. shows an example of matched threshold voltage achieved by implanting the strained Si device with a dose twice as large as the unstrained Si.

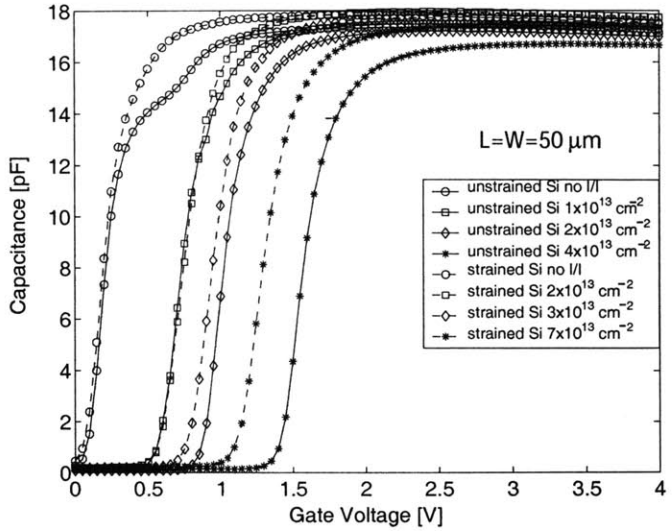

Fig. 2.8. Gate to channel capacitance for strained and unstrained Si n-MOSFET devices with varying channel doping concentration. The length and width of the devices are 50 μm, and the oxide thickness is t_{ox}=45 nm.

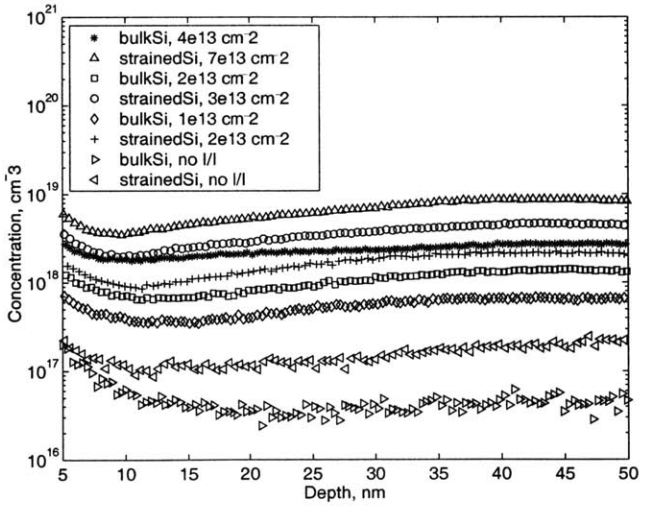

Fig. 2.9. Channel doping concentration vs. depth from the SiO_2/poly-Si interface for varying boron ion implant doses used for strained-Si and bulk-Si MOSFETs. The profile was determined using secondary ion mass spectrometry, SIMS.

The surface potential ϕ_s was calculated using the expression: $\varphi_s = \frac{2k_bT}{q} \ln \frac{N_a}{n_i}$ where n_i is the intrinsic carrier concentration which was adjusted for strained Si using a smaller bandgap of 0.96 eV and k_bT/q at room temperature is 26 meV. The mobility data presented in Fig. 2.8 show that at high Q_i, the strained mobility plotted vs. E_{eff} displays universal behavior independent of doping with enhancement of 1.5-1.7X over unstrained Si. The unstrained Si data also show universal behavior and agree closely with previously reported data [19]. At low Q_i, deviation from universal behavior is observed for both the strained and unstrained devices. At low Q_i and high doping, the mobility for strained Si devices decreases with decreasing E_{eff}.

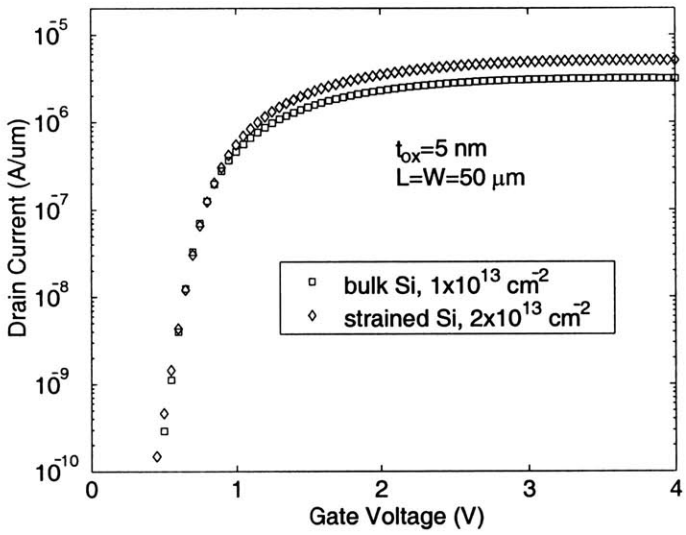

Fig. 2.10. logIV plot of bulk Si and strained Si n-MOSFET devices with matched threshold voltage. The threshold voltage was matched by doping the strained Si with twice the dose compared to bulk Si.

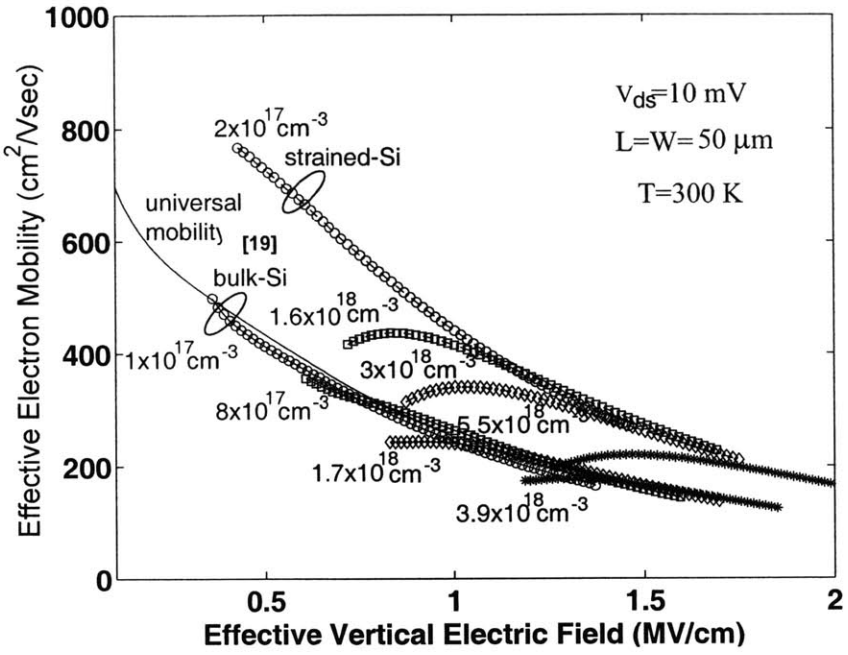

Fig 2.11. Effective electron mobility versus vertical effective electric field, E_{eff}, for various channel doping concentrations for unstrained and strained Si n-MOSFETs.

towards the un-strained Si data. The decrease is likely due to Coulomb scattering by channel dopants agreeing with theoretical predictions that the enhancement of strained Si electron mobility over unstrained Si is reduced when Coulomb scattering is the dominant carrier scattering mechanism [20]. It should be noted that the strength of the Coulomb interaction encountered by inversion layer electrons in the devices reported in this work is stronger than in advanced sub-50-nm devices that would have carefully tailored 2D halo doping profiles that result in reduced surface doping to achieve maximum performance.

2.4. Critical Analysis of Mobility Measurements

Next, a critical analysis of the mobility measurement was performed. In particular, the influence of the correction for E_{lat} on the mobility measurements was investigated. The influence of the correction is expected to be greatest at low E_{eff}, near gate voltages corresponding to the threshold voltage of the device. At high E_{eff}, where inversion layer carriers have effectively screened Coulomb scattering events, the measured enhancement over unstrained Si match previously measured data quite closely [21-22]. The unstrained Si mobility data follows previously reported mobility in unstrained Si, for high E_{eff}, demonstrating the accuracy of the measurement technique used in this work at high E_{eff}. In order to investigate the influence of the correction to Elat on the mobility, the mobility was extracted both with and without i.e. (Elat=Vds/L) the correction factor. The plot in Fig. 2.12 shows that when the correction is not used, the mobility falls off faster for low E_{eff}, compared to the case when the mobility is extracted using the correction factor. The data with the correction also demonstrates slightly larger mobility enhancement (see Fig. 2.13) showing that that conclusion made in this work that mobility enhancement of strained Si devices is reduced over unstrained Si at low E_{eff} is not an artifact of using the correction. Quite the contrary, the use of the correction provides greater mobility measurement accuracy for gate voltages near threshold voltage. Greater accuracy for that voltage range is important for determining the Coulomb scattering limited mobility.

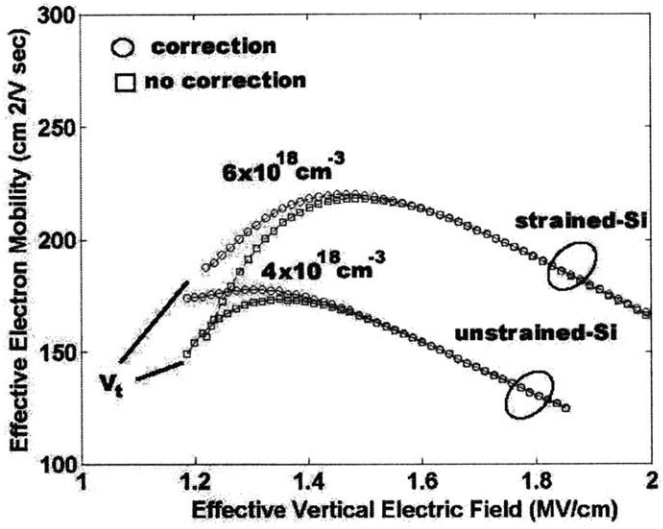

Fig. 2.12. Mobility versus effective vertical electric field, E_{eff} demonstrating the influence of the lateral field correction on the mobility extraction at low E_{eff}. The correction tends to increase the mobility at low E_{eff} (near $V_{gs}=V_t$)

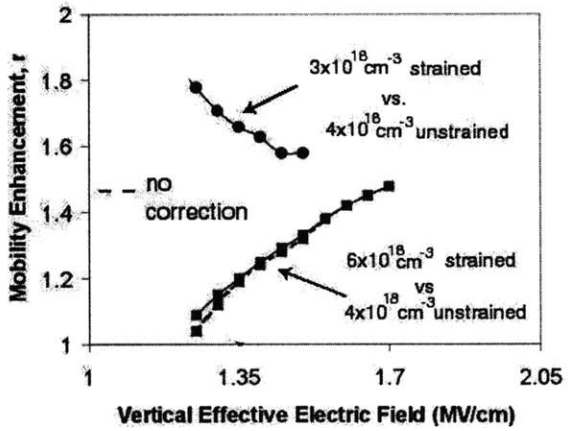

Fig. 2.13. Mobility enhancement, r, versus vertical effective electric field, E_{eff}, showing reduced mobility enhancement with decreasing E_{eff} for a strained-Si channel doped higher than unstrained. Significant enhancement is observed for similar doping for all E_{eff}. The correction factor f has negligible influence on the extracted mobility enhancements, r.

2.5. Construction of a Coulomb Mobility Model

The departure from universal behavior in the Coulomb scattering dominant regime allows for accurate extraction of the Coulomb mobility for strained and unstrained (relaxed) Si n-MOSFETs for various doping concentration. The total mobility, μ_{total} for relaxed and strained Si respectively is assumed to follow a two-term model (Matthiessen's rule) where: $(\mu_{total}^{relaxed})^{-1} = (\mu_{universal}^{relaxed})^{-1} + (\mu_{coulomb}^{relaxed})^{-1}$ and $(\mu_{total}^{strain})^{-1} = (\mu_{universal}^{strain})^{-1} + (\mu_{coulomb}^{strain})^{-1}$ where $\mu_{coulomb}$ is the Coulomb-limited mobility and $\mu_{universal}$ comprehends phonon and surface scattering for the respective material as discussed later. The dependence of $\mu_{coulomb}^{strain}$ on N_a and N_i, shown in Fig. 2.14 is a power law dependence where $\mu_{coulomb}^{strain} = AN_a^{-\beta}N_i^{\alpha}$ where A is a constant, 2.89x10^9 cm/Vsec with $\alpha=\beta\approx 1$, and N_a is expressed in units of cm^{-3} and the inversion charge areal

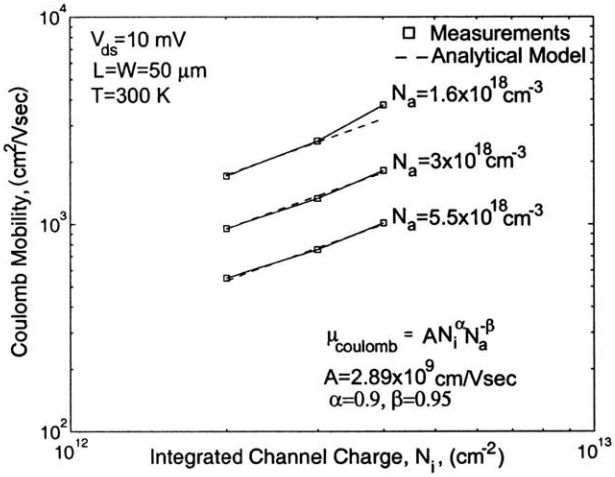

Fig. 2.14. Coulomb limited mobility in strained Si plotted on a log-log scale versus inversion charge area density, N_i, calculated for three different channel doping concentrations, N_a. The Coulomb mobility was calculated using a Matthiessen's rule summation for the total mobility based on the measurement data. The data show a power-law dependence on N_i and N_a.

density, N_i, in cm^{-2}.

Theoretical calculations of Coulomb scattering for relaxed Si MOSFET inversion layer carriers, that assume Coulomb scattering is an elastic mechanism and results in deflection of carriers through small angles, predict a power-law dependence of $\mu_{coulomb}$ and exponents for N_a and N_i close to 1 agreeing with the experimental findings in this work [23]. Moreover, it is hypothesized that $\mu_{coulomb}^{strain} \approx \mu_{coulomb}^{relaxed}$ (see section 2.6 for critical analysis) [20]. We test this by using our analytical expression for $\mu_{coulomb}^{strain}$ to calculate $\mu_{total}^{relaxed}$ and μ_{total}^{strain} (using Matthiessen's rule as above) for unstrained and strained Si channel doping concentrations, N_a=3.9x10^{18} cm^{-3} and N_a=5.5x10^{18} cm^{-3} respectively, resulting in similar V_t. Good agreement of calculated and measured data for both cases is shown in Fig. 2.15. Analytical universal mobility expressions for

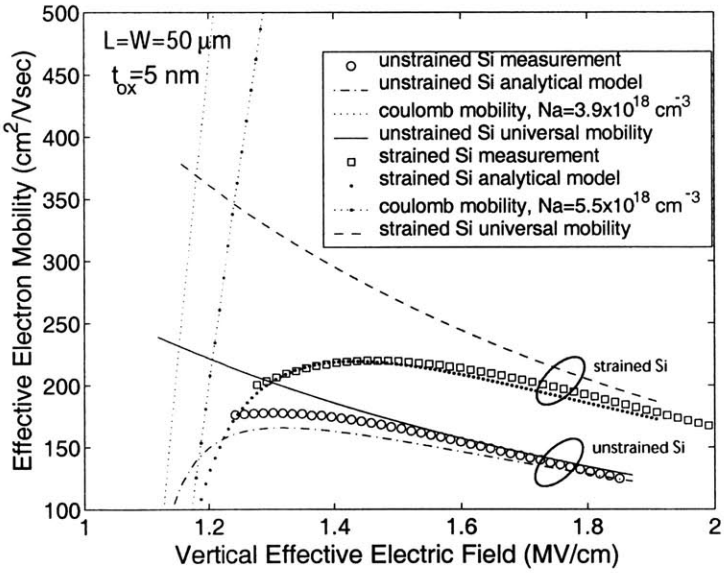

Fig. 2.15. Comparison of measured data with calculated inversion electron mobility vs. E_{eff} in relaxed and strained Si MOSFETs with channel doping concentration N_a=3.9x10^{18} cm^{-3} and N_a=5.5x10^{18} cm^{-3} respectively. The analyti expression for Coulomb mobility component was the same for both strained and relaxed Si, while the "univers component was extracted by fitting to the high Q_i portion of the experimental data for the two cases as described in the te

strained and unstrained devices at high E_{eff}, where phonon and surface-roughness are the dominant scattering mechanisms for electron transport were calculated by fitting the expression, $\mu_{universal} = \frac{\mu_o}{1+(\frac{E_{eff}}{E_o})^{\eta}}$, to the high E_{eff} measurement data in this work for all doping concentrations. The fitting parameters found that provide reasonable fit are: relaxed Si: μ_o=560, E_o=0.95, ν=1.80, and for strained Si: μ_o=1020, E_o=0.88, ν=1.93. The ratio of the universal mobility of strained to unstrained is equal to the enhancement observed experimentally, 1.75 X. Furthermore, the coefficients follow the work of *Liang et al.* [24] closely.

2.6. Discussion: Why Does Mobility Enhancement Diminish For Carrier Transport Dominated by Coulomb Scattering?

In this section, a critical review of Coulombic scattering of electrons in strained Si n-MOSFET devices is performed. The goal of this section is to understand intuitively based on physical explanations, why electron mobility is not enhanced in the Coulomb dominated regime. This will be accomplished by first discussing Rutherford's gold foil experiment, which will give insight on the scattering of electrons with nuclei. Next, Coulomb scattering in semiconductors will be discussed in terms of quantum mechanical calculations of discrete energy states. Finally, both experimental and theoretical results from the literature will be discussed that support the findings of this work.

2.6.1. Rutherford's Scattering Formula

Rutherford studied the scattering of alpha particles from a gold foil, which led him to propose the nuclear model of the atom in 1911. The angle of scattering can be related to the mass, velocity, and impact parameter of the incident particle as illustrated in Fig. 2.16 below [25].

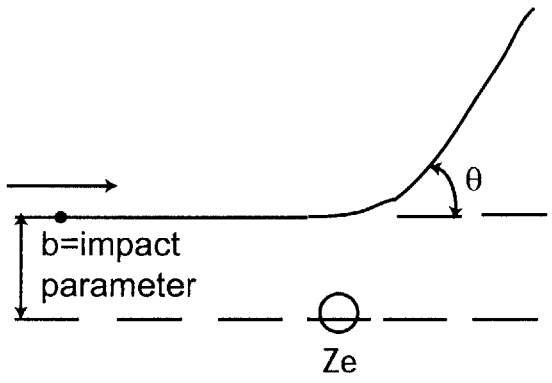

Fig. 2.16 Illustration of Rutherford's scattering experiment of alpha particles with a gold foil. The experiment helped lead to the development of the nuclear model of the atom.

Assuming that scattering is due to the Coulomb interaction between the α–particle and the positively charged nucleus, the target is thin enough to consider only single scattering, and that the nucleus is massive and fixed, and finally that the scattering is elastic, the angle can be expressed as:

$$\cot(\theta/2) = \frac{4mv^2 b\pi\pi}{2ze^2} \qquad \text{Equation 2.2.}$$

In a semiconductor, the angle of scattering is discrete not continuous. As a result, to understand Coulomb scattering in strained Si, an understanding of the energy levels is required. In particular the scattering time, $\tau(\kappa)$ can be calculated by summing scattering rates over all possible final momentum states [26]:

$$\frac{1}{\tau(k)} \propto \int_{k'} S(k,k')(1-\cos(\theta))dk' \qquad \text{Equation 2.2}$$

Where, $S(k, k')$ is the transition rate from state k *to* k', θ is then angle between k and k' and k' is the final momentum state. Clearly, if the number of final states, k' decreases, the scattering time will increase. Therefore, an accurate understanding of the energy states is required, and is discussed in the next section.

2.6.2. Energy Levels in Nanoscale Strained and unstrained Si devices

Next, the sub-band energy levels in the conduction band of strained and unstrained Si nanoscale MOSFETs were determined using a self-consistent Poisson-Schrodinger solver [25]. Fig. 2.17 below illustrates the energy levels in the conduction band of a strained Si n-type MOSFET. Typically, for bulk-Si, the six energy levels in the conduction band are degenerate in energy. For a nanoscale MOSFET, the levels are split due to quantum-mechanical confinement of inversion layer electrons in the perpendicular direction. Two sets of discrete levels are created, due to differing perpendicular effective mass where for the perpendicular valleys: m_l=0.98 mo

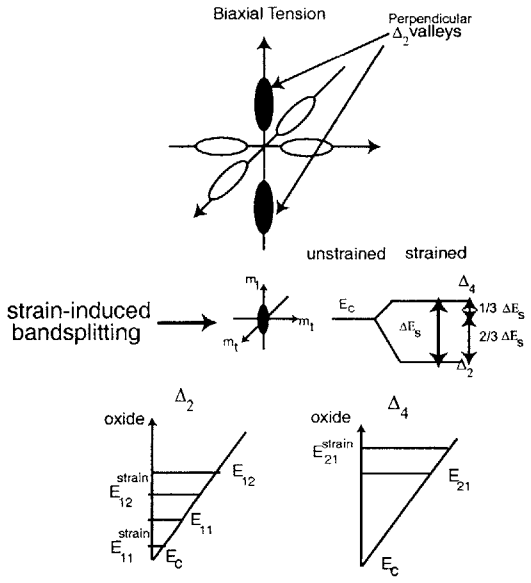

Fig. 2.17. Illustration of strain-induced band splitting resulting in a splitting of the six-fold degeneracy in the conduction band into two perpendicular Δ_2 valleys and four parallel Δ_4 valleys where the amount of splitting is given by ΔE_s which is a function of the amount of strain. The lower figure illustrates additional splitting due to quantum confinement of the inversion layer electrons near the Si/SiO_2 surface. The subband energy levels are expressed as E_{ij} where the j is the j^{th} energy level in the i^{th} valley (1: Δ_2, 2: Δ_4) , e.g. E_{11} is the ground state energy for the Δ_2 valley.

and the parallel valleys: m_t=0.19 mo. The discrete energy levels can be determined by approximating the potential as an Airy potential, giving the solutions [27]:

$$E_j = \left(\frac{3hqF}{4\sqrt{2m_\perp}}(j+3/4)\right)^{2/3} \qquad \text{Equation 2.3}$$

Where j is an integer, F is the electric field, and h an q is fundamental physical constants.

As a result, the two-fold degenerate valleys will have smaller energy than the perpendicular four-fold degenerate valleys. Biaxial tensile strain will increase the energy splitting between the four-

fold and two-fold valleys, where the amount of splitting can be related to the Ge fraction (x) in the virtual substrate by: $\delta E_s = 670x\ meV$ [28]. Self-consistent Poisson-Schrodinger computer simulations show that for unstrained Si n-MOSFET devices with oxide thickness and doping concentration equivalent to those studied experimentally in this work larger than 95% of the electron population reside in three subband energy levels: E_{11}, E_{12}, and E_{21} as shown in Fig. 2.18 . E_{ij} is the subband energy level of the i^{th} valley where i=1 represents the two-fold degenerate perpendicular Δ_2 valleys and i=2 the four-fold degenerate parallel Δ_4 valleys and j is the subband energy index where j=1 is the ground state.

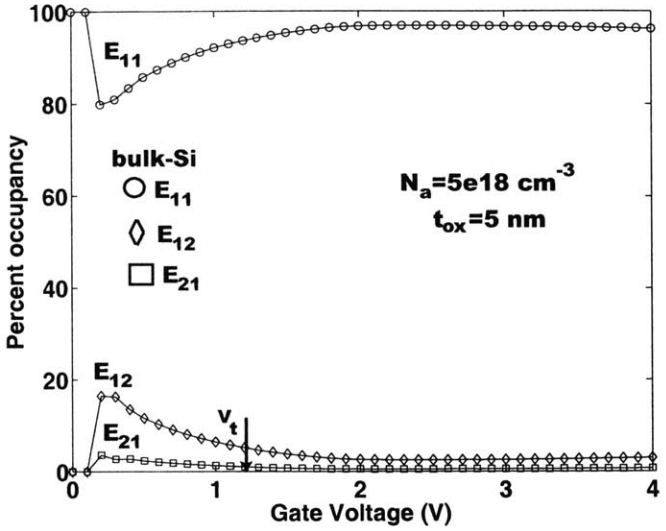

Fig. 2.18. Percentage occupancy of inversion layer electrons in three subband energy levels in a bulk-Si n-MOSFET device with equivalent oxide thickness and doping as the devices analyzed in this work. The values were calculated using a self-consistent Poisson-Schrodinger computer simulation. The figure demonstrates over 90% of the electron population resides in the three subband levels, E_{11}, E_{12} and E_{21}. The distribution of the electrons among the three sub-bands depends upon the density of states for the sub-bands. The density of states varies widely and thus there is some controversy over the details of the electron distribution among the sub-bands [C. Bowen, private communication].

These three subband energies are then calculated as a function of V_{gs} for both bulk-Si and strained-Si devices as shown in Fig. 2.19 (a-b). The results indicate that in terms of electron population occupancy, the strained-Si and bulk-Si devices are almost equivalent. Since Coulomb scattering is an elastic scattering mechanism, the number of final states to scatter into after a Coulomb scattering event for electrons in strained-Si and bulk-Si n-MOSFETs are comparable unlike the case of intervalley scattering where scattering involves coupling to higher subband

energy levels in the form of intervalley scattering mechanisms. Therefore, a loss of enhancement should be expected for carrier transport dominated by Coulomb scattering.

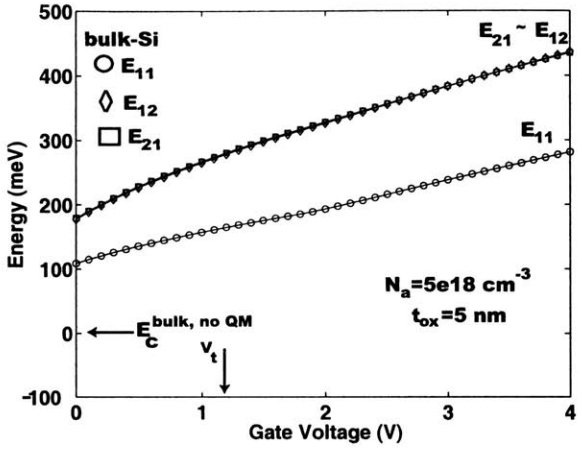

Fig. 2.19(a). Subband energy levels as a function of gate voltage. The plot demonstrates that quantum confinement has split the energy subband energy levels so that the ground state, E_{11}, varies from 100-200 meV from the initial conduction band with no confinement, and that E_{21} and E_{12} are roughly at the same energy level.

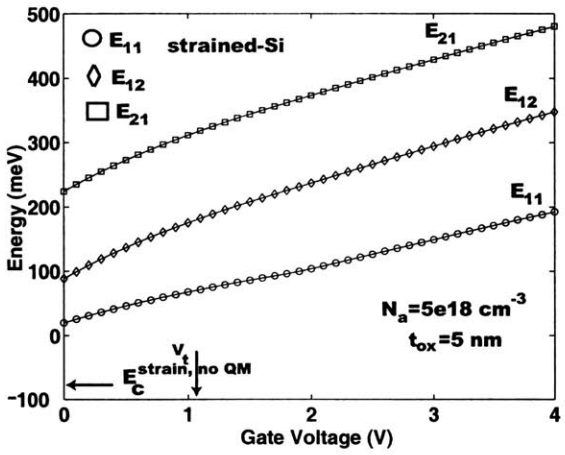

Fig. 2.19(b). Subband energy levels as a function of gate voltage for a strained-Si n-MOSFET with 20% relaxed Ge beneath the strained-Si layer. The quantum confinement results in a splitting of the subband energy levels, but, due to strain-induced bandsplitting, E_{21} is lifted in energy relative to E_{12} breaking the degeneracy calculated for the bulk-Si n-MOSFET.

2.6.3. Evidence from Research Literature

Further evidence of a loss of mobility enhancement for carrier transport dominated by

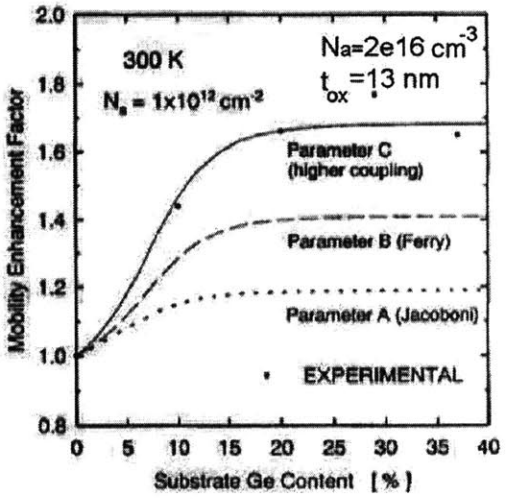

Fig. 2.20. Computer simulations of the enhancement of electron mobility versus strain or percent Ge in the relaxed layer beneath the strained-Si ($Si_{1-x}Ge_x$) for three different optical phonon parameters where the values changed are the phonon energy and deformation potential so that the coupling of inversion layer electrons to higher subband energy levels can be changed [29]. The simulation results are plotted against experimental data and show that close matching occurs for the phonon parameters that have higher coupling (increased deformation potential) and in the limit of no coupling (only intravalley scattering mechanisms) the mobility enhancement is diminished.

Coulomb scattering is demonstrated through the observation that in order to match experimental mobility enhancement measurements of strained-Si n-MOSFETs it is necessary to increase the coupling of the inversion layer electrons to optical phonons that result in intervalley scattering processes [29]. Computer simulations varying the coupling strength through the deformation potential and optical phonon energy demonstrate that increased coupling is required to match experimental data as shown in Fig. 2.20. In the limit of weaker coupling or intravalley scattering, the enhancement is shown to collapse This result supports the findings in this work that electron mobility dominated by Coulomb scattering (i.e. intravalley scattering) is not enhanced in strained-Si over bulk-Si devices.

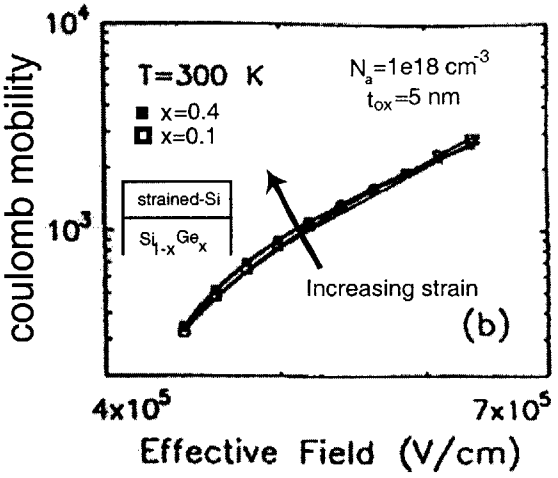

Fig. 2.21. Coulomb mobility calculated using a Monte-Carlo simulator with a comprehensive coulomb mobility model incorporated into it [20]. The mobility is plotted for two different values of strain and shows slight enhancement of mobility, supporting the experimental findings of this work.

Monte-Carlo simulations that incorporate a comprehensive Coulomb mobility model demonstrate a loss of electron mobility enhancement for carriers dominated by Coulomb scattering due to strain [20]. The n-MOSFET devices simulated have equivalent oxide thickness, t_{ox}=5 nm to the devices fabricated in this work and have highly doped channels of N_a=1e18 cm^{-3}. The coulomb mobility was extracted for two values of strain applied by varying the Ge content in the $Si_{1-x}Ge_x$ relaxed layer beneath the strained-Si. The results shown in Fig. 2.21 indicate that Coulomb mobility is only slightly enhanced with strain supporting the findings from this work

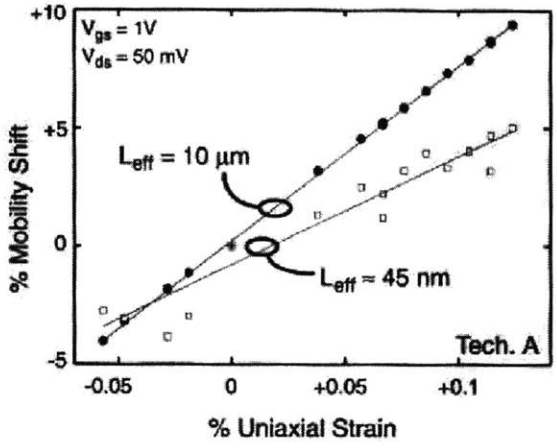

Fig. 2.22. Experimentally measured increase in mobility versus percent uniaxial strain applied by wafer bending for a short-channel n-MOSFET with L_{eff}=45 nm and long-channel with L_{eff}=10 µm [30]. The plot shows that the dependence of strain on mobility is reduced for the short-channel device that is doped heavily to control short-channel effects compared to the long-channel device whose channel doping is low. The plot indicates that mobility enhancement due to strain decreases for short-channel devices which is likely associated with the increased Coulomb scattering of inversion layer electrons.

Finally, experimental evidence of reduced mobility enhancement of inversion layer carriers in the Coulomb scattering dominated regime of transport for strained-Si is demonstrated by investigating the dependence of mobility on uniaxial strain for short-channel MOSFET devices, and comparing to long-channel as shown in Fig. 2.16 [30]. The results show that the influence of uniaxial strain on mobility enhancement is reduced for the short-channel devices, which have increased doping concentration to control short-channel effects compared to the long device. This result indicates that electron mobility enhancement due to strain is reduced for short-channel devices that have high doping concentration

2.7. Summary

In summary, for the relatively large Q_i range corresponding to various channel doping levels, we have demonstrated universal electron inversion layer mobility in strained Si enhanced by 1.5-1.7X relative to unstrained Si. At low Q_i, it is found that the Coulomb scattering mobility for unstrained and strained Si are closely matched, are inversely proportional to N_a and proportional to Q_i, due to screening. The findings reported in this Chapter will help to calibrate existing transport models in semiconductor computer simulation programs so that electron transport in nanoscale strained Si MOSFETs can be studied, which is the topic of Chapter 3.

Chapter 3

Investigation of the Performance Enhancement of Nanoscale Strained Si MOSFETs

In this Chapter, electron transport models are calibrated using the experimental data discussed in Chapter 2. The transport models are then used to investigate the performance enhancement measured in terms of on-current, of strained Si over un-strained Si devices with nanoscale gate length for the same off-current, I_{off}. Using the transport models, the influence of Coulomb scattering interactions on performance benefits is discussed, and a scaling methodology that maximizes on-current and minimizes off-current is presented.

3.1. Introduction

As demonstrated in Chapter 2, a clear understanding of Coulomb scattering of inversion layer electrons with channel dopants in strained Si devices is required to accurately determine performance benefit. An important contribution to this understanding, based on theoretical and experimental work, shows that electron mobility limited by Coulomb scattering is not enhanced

in strained Si devices compared to unstrained Si [31-32]. Despite the reduced enhancement, significant improvement of the on-current I_{on}, which is indicative of performance, for strained Si devices over unstrained with 80 nm gate length has been demonstrated experimentally [33]. However the specific contribution of various physical mechanisms that can result in reduced performance: Coulomb scattering, self-heating, non-stationary transport, is unknown. In addition, process variation, in particular channel doping concentration and parasitic source/drain resistance, complicate direct comparison of strained and unstrained Si devices. In this Chapter, the influence of Coulomb scattering on I_{on} for strained Si devices with gate length less than 50 nm is investigated with the aid of computer simulation, where experimental data is used for the calibration of transport models. Next, using the transport models, a scaling methodology for strained Si devices is proposed that maximizes the on-current and minimizes off-current, where the variables used are gate-workfunction, and channel doping.

3.2. Nanoscale Device Structure

A cross-section of a nanoscale device with 25 nm gate length and super-halo channel doping concentration is shown below in Fig. 3.1 and is consistent with the 65 nm technology node listed in the 2002 ITRS to be manufactured in the year 2005. As can be seen, the relevant dimensions both in the vertical and horizontal direction is at the nanoscale. The electrical oxide thickness used is 1.4 nm, which includes quantum mechanical effects. A metal gate with workfunction equivalent to n^+ polysilicon was used to eliminate depletion effects in strong-inversion. In order to alleviate short-channel effects, the junction depth is 25 nm. The source/drain parasitic resistance does not exceed 10-15% of the total channel resistance [34]. Clearly, in order to analyze this device in terms of its drain current characteristics, a transport

model is required that is dopant dependent, and that takes into account high-lateral electric field effects, in particular, velocity saturation and electron energy conservation. In the next section, transport models will be calibrated versus doping concentration. This will be followed by a discussion of accurate modeling of velocity saturation and non-stationary transport effects.

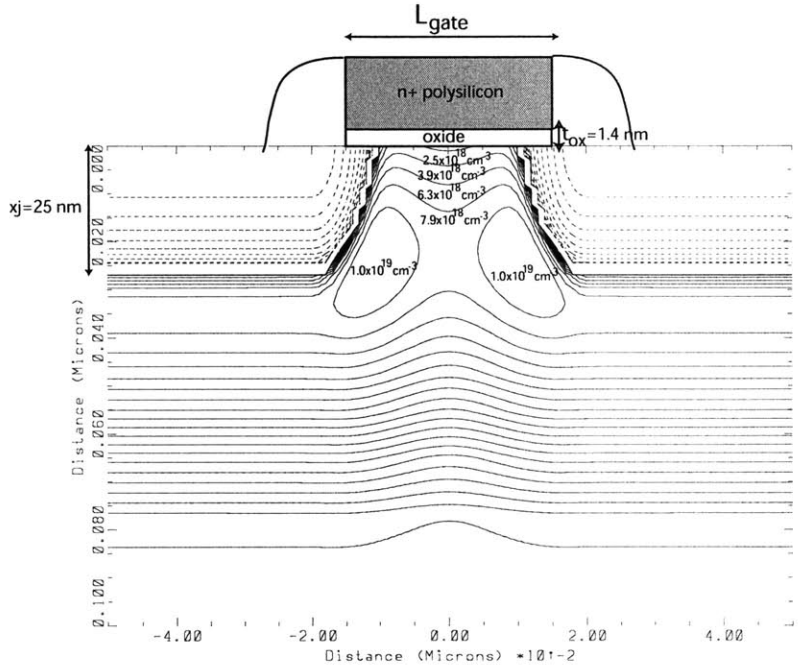

Fig. 3.1. Cross-section of a nanoscale n-MOSFET device showing a contour map of the channel doping ("super-halo") and relevant physical dimensions. Relevant dimensions include: gate length=25 nm, oxide thickness=1.4 nm, and junction depth=25 nm. The channel doping reaches as high as $1x10^{19}$ cm^{-3} near the source/drain areas, and drops to $3x10^{18}$ cm^{-3} at the surface indicating a super-steep retrograde profile.

3.3. Electron Transport Model Calibration for strained and unstrained Si n-MOSFETs

A physical based mobility model, that assumes a Matthiessen's rule summation for the various scattering mechanisms for inversion layer carriers in a MOSFET device [35] and is available in the MEDICI simulator [36] was calibrated for both strained and unstrained Si n-MOSFETs using the experimental measurements discussed in Chapter 2. Inversion layer electron mobility, μ, is approximated by the sum of three mobility terms:

$$\frac{1}{\mu} = \frac{1}{\mu_{coulomb}} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \qquad \text{Equation. 3.1}$$

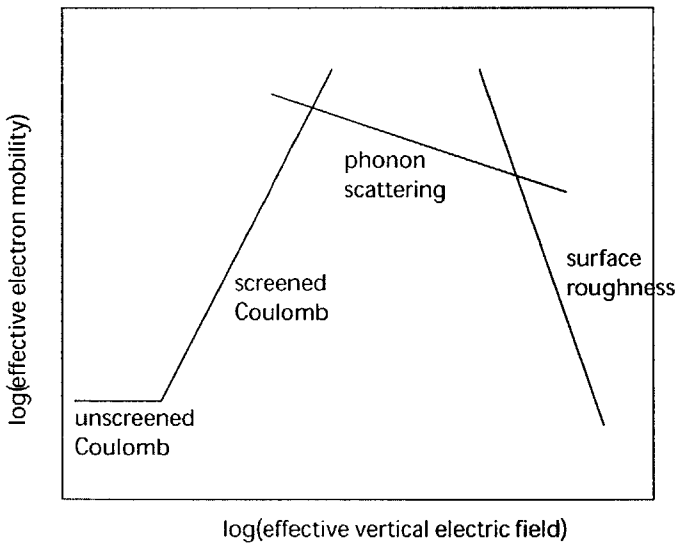

Fig. 3.2. Schematic illustration of the vertical effective electric field dependence of various scattering mechanisms present in a MOSFET device. The total carrier mobility is achieved by summing the varying components in a reciprocal Mathiessen's rule summation.

where $\mu_{coulomb}$ comprehends mobility limited by Coulomb scattering, μ_{ac} acoustic phonon scattering, and μ_{sr} surface-roughness scattering. An illustration of the three scattering mechanisms, and how they sum up to the total mobility is shown in Fig. 3.2.

The empirical relations for each term are given in Table 3.1 where the symbols are defined in Table 3.2.

Scattering Mechanism	Empirical Relationship
Coulomb	$\mu_{coulomb} = \max(\mu_{screened}, \mu_{unscreened})$ $\mu_{screened} = A\frac{n^{\gamma}}{N_a^{v}}$ $\mu_{unscreened} = \frac{D}{N_a^{\eta}}$
Acoustic phonon	$\mu_{ac} = \frac{\alpha}{E_{\perp}} + \frac{\beta N_a^{0.0284}}{T(E_{\perp})^{1/3}}$
Surface-roughness	$\mu_{sr} = \frac{\delta}{E_{\perp}^2}$

Table 3.1. Analytical expressions for mobility limited by the three dominant scattering mechanisms for inversion layer carriers in a MOSFET device: Coulomb, acoustic phonon, and surface-roughness.

Symbol	Definition
A, D, α, β, δ, γ, η, ν	Constants
$E_{\perp}$	Local vertical electric field
N_a, n	Doping concentration, total electron concentration
T	Lattice temperature

Table 3.2. Definitions of the symbols used in the analytical mobility model expressions.

The Coulomb limited mobility consists of two terms: a screened mobility, $\mu_{screened}$ for high inversion layer electron concentration, N_i such that sufficient screening of Coulomb interactions between inversion layer electrons and channel dopants has occurred, and an unscreened mobility, $\mu_{unscreened}$ that is independent of N_i. [37] The terms are combined by assuming a piece-wise relationship such that :

$$\mu_{coulomb} = \max(\mu_{screened}, \mu_{unscreened}). \qquad \text{Equation. 3.2.}$$

The expression can be visualized below in Fig. 3.3.

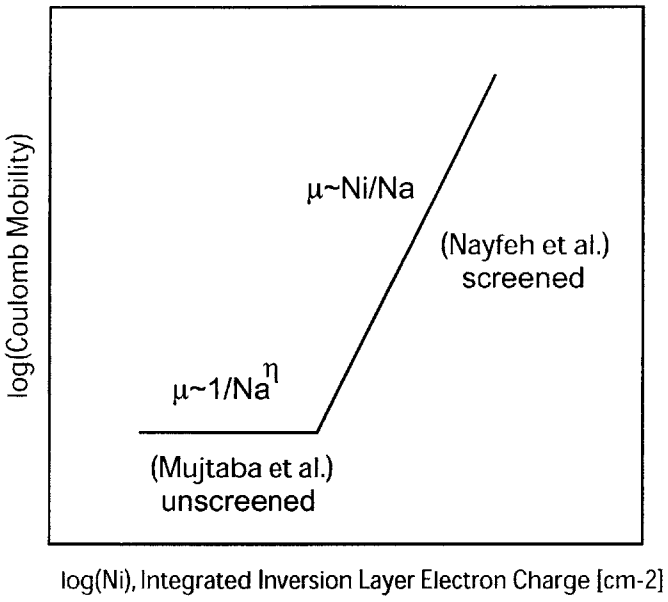

Fig. 3.3 Illustration of the Coulomb mobility model used in this work. The model is composed of two parts, screened and unscreened for low inversion layer concentration, N_i. They are combined piece-wise where the maximum is the mobility.

The channel doping concentration, N_a was determined using inverse modeling technique as explained in Chapter 2. Measured drain current for gate voltage larger than the threshold voltage was used to calibrate the constants used in the empirical mobility expressions. Close agreement between simulated and measured drain-current for strained and unstrained Si devices for varying channel doping concentration was achieved as shown in Fig. 3.4 (a-b). In addition, the gate to source/drain capacitance agrees closely as shown in Fig. 3.5 (a-b), demonstrating that the oxide and channel doping concentration assumed are accurate. The constant terms used for the various mobility terms for strained and unstrained devices are shown in Table 3.3(a-b) for physical

variables expressed in cgs units. The constants for $\mu_{unscreened}$ were computed based on a first-principles calculation of Coulomb scattering with channel dopants [38]. The constant terms for μ_{ac} and μ_{sr} are 1.75X larger for strained Si over unstrained Si, and are equivalent for $\mu_{coulomb}$ as was demonstrated in Chapter 2.

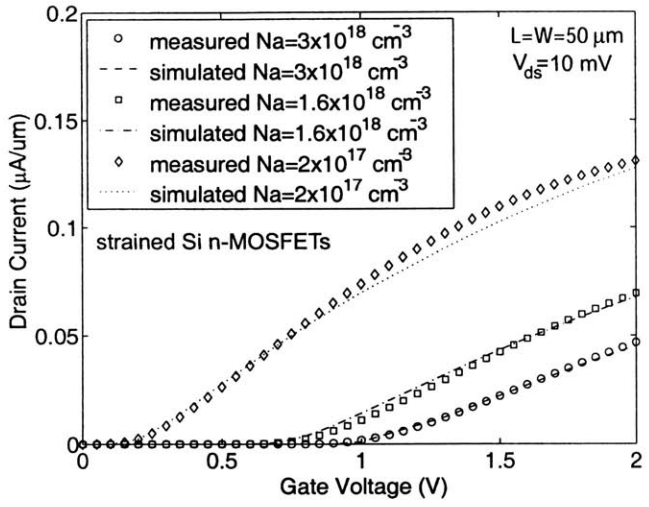

Fig. 3.4.(a) Close agreement between simulated and measured drain current for various channel doping for strained Si n-MOSFETs. Measured data is shown in symbols and simulation results in dashed lines.

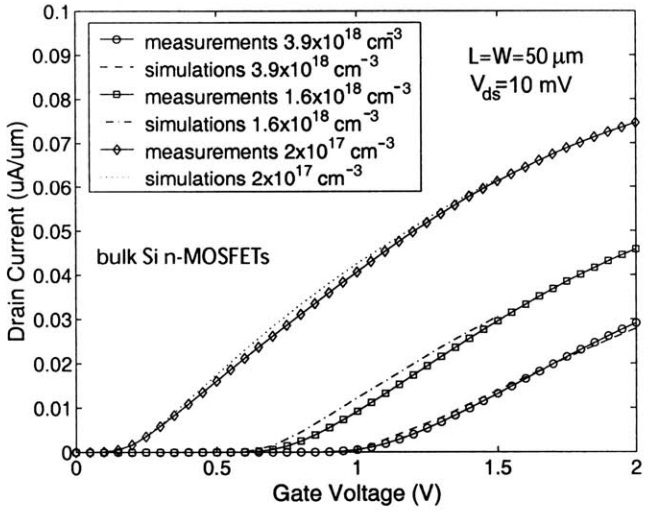

Fig. 3.4 (b). Close agreement between simulated and measured drain current for various channel doping for bulk Si n-MOSFETs. Measured data is shown in symbols and simulation results in dashed lines.

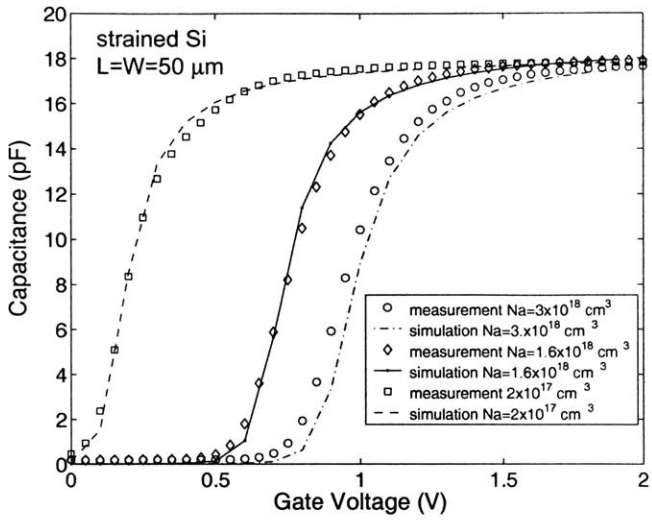

Fig. 3.5 (a) Gate to channel capacitance, C_{gc}, for strained Si n-MOSFETs where measurements are shown in symbols and simulations in lines. Close agreement is shown, demonstrating that the doping concentration has been calibrated accurately.

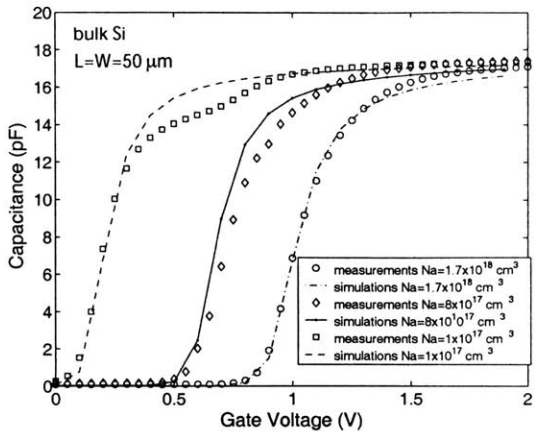

Fig. 3.5 (b) Gate to channel capacitance, C_{gc}, for strained Si n-MOSFETs where measurements are shown in symbols and simulations in lines. Close agreement is shown, demonstrating that the doping concentration has been calibrated accurately.

unstrained Si

Acoustic Phonons	$\alpha=1.02\times10^{6}$	$\beta=3.7\times10^{6}$	
Surface-Roughness	$\delta=9.49\times10^{14}$		
Coulomb screened	**A=2700**	$\gamma=0.90$	$\nu=0.95$
Coulomb unscreened	$D=3.86\times10^{9}$	$\eta=0.386$	

Table 3.3(a-b) Calibrated mobility model coefficients for strained (b) and unstrained Si (a). Increased coefficients for the strained Si mobility model of 1.75X over unstrained Si is used for acoustic-phonon and surface-roughness limited mobility, while equivalent coefficients are used for Coulomb scattering limited mobility.

strained Si

Acoustic Phonons	α=1.79x10^6	β=6.48x10^6	
Surface-Roughness	δ=1.66x10^{15}		
Coulomb screened	A=2700	γ=0.90	ν=0.95
Coulomb unscreened	D=3.86x10^9	η=0.386	

Table 3.3(b)

3.4. Transport Model Calibration (high-lateral electric field)

Next, high lateral electric field transport parameters were calibrated for strained and unstrained Si devices based on published numerical simulations of the Boltzmann transport equation calculated by Monte Carlo simulation [38]. In particular, fitting of the coefficients in the Caughey-Thomas expression [39] that relate lateral electric field, E_{lat} to carrier mobility, μ:

$$\mu = \frac{\mu_{low}}{[1+(\frac{\mu_{low}E_{lat}}{v_{sat}})^{\beta}]^{1/\beta}} \qquad \text{Equation 3.3.}$$

was performed, where μ_{low} is the low-lateral electric field mobility, v_{sat} is the saturation velocity and β is a fitting factor. Fig. 3.3. shows close agreement between the fit expression and the published computer calculations using β=1.25 and v_{sat}=0.9x10^7 cm/s for both strained and unstrained Si devices. The result that the high lateral electric field parameters are equivalent for

strained and unstrained Si devices is not surprising given that the influence of strain on optical phonon energy is small [40].

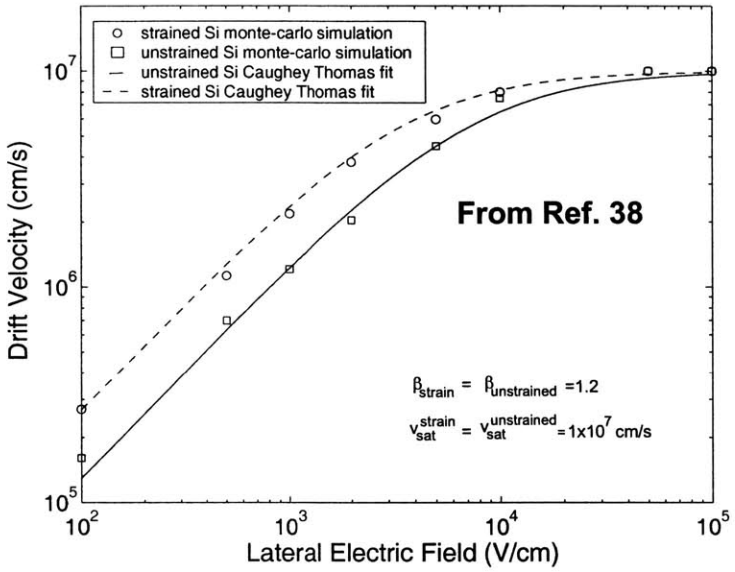

Fig. 3.6. Inversion layer electron velocity versus lateral electric field for unstrained and strained Si n-MOSFETs. The velocity was computed using a numerical solution of Boltzmann's equation using a Monte-Carlo method [38]. From the figure one can observe that the saturation velocity for strained and unstrained Si are the same and that they approach the saturation velocity at the same rate with lateral electric field, so that the Caughey-Thomas parameters are equivalent.

In addition to velocity saturation effects, in order to accurately determine current in nanoscale devices, non-stationary transport modeling is required. In particular, the energy-balance equation was solved self-consistently with the semiconductor transport equations. A simple argument can be made validating the use of non-stationary transport for devices with gate length less than 25 nm by assuming that transport is dominated by scattering with a momentum time of τ_m and that drift is the dominant transport mechanism due to an applied electric field, E. The electron velocity can then be related to E and the scattering time by:

$$m\frac{dv}{dt} = -qE - \frac{mv}{\tau_m}. \qquad \text{Equation. 3.4.}$$

where m is the particle mass, v is the velocity and q is the fundamental electron charge equal to $1.6\text{x}10^{19}$ C, and t is time.

The solution to this differential equation is:

$$v(t) = \frac{q\tau}{m}E(1 - e^{-t/\tau_m}) \qquad \text{Equation. 3.5}$$

The solution demonstrates that a slow rise of the velocity occurs with time where in the limit of very long time the velocity reaches a steady-state maximum. The distance traveled by the electron at steady-state is:

$$d = \frac{q\tau_m^2}{em}E$$ Equation. 3.4.

Typical low-field mobility and lateral electric field in short-channel silicon MOSFET devices is 200 cm^2/Vsec and E=10^4 V/cm, giving: τ_m=.03 ps. As a result, the distance to reach steady state is approximately *d=20 nm* demonstrating that non-stationary transport modeling is required for devices with length close to 25 nm. The key parameter used for non-stationary transport modeling, the energy relaxation time, τ_w, was set to the default value of 0.1 ps for the unstrained Si devices. In order to determine τ_w for strained Si devices, τ_w was related to low-field mobility using the energy balance equation assuming a displaced Maxwellian for the electron temperature distribution and is expressed in Eq. 3.5:

$$v\frac{\partial w}{\partial x} = -qv\mathrm{E} - \frac{k_b}{n}\frac{\partial}{\partial x}(nvT_e) - \frac{1}{n}\frac{\partial}{\partial x}(\kappa\frac{\partial T_e}{\partial x}) - \frac{w - w_o}{\tau_w}$$ Equation. 3.5.

Where the symbols are defined as:

τ_w: Energy relaxation time

κ: Electron Thermal Conductivity

w: Electron kinetic energy

w_o: Equilibrium energy ($\frac{3}{2}k_bT_e$)

T_e: Electron Temperature

E: Electric field

n: electron volume density

Assuming homogeneous steady-state conditions, the energy relaxation time can then be related to the low-lateral electric field mobility, μ_o, fundamental physical constants q, k_b, electron temperature, equilibrium temperature of 300 K, T_o, and saturation velocity [41]:

$$\tau_w = \frac{3}{2}\frac{k_b T_o}{q}\frac{\mu_o}{v_{sat}^2}\frac{1}{1+T_e/T_o} \qquad \text{Equation. 3.6.}$$

Eq. 3.6 shows energy relaxation time is directly proportional to low-lateral electric field mobility. As a result, the energy relaxation time for unstrained Si can be related to that of strained Si by a multiplier factor equal to the low-lateral electric field mobility so that:

$$\tau_w^{strain} = 1.75\tau_w^{unstrained} \qquad \text{Equation. 3.7.}$$

Equipped with a transport model, nanoscale strained and unstrained Si devices can be studied and the performance benefit determined. First, an investigation of the influence of loss of Coulomb scattering limited mobility *enhancement* will be presented.

3.5. Influence of loss of Coulomb Scattering Limited Mobility Enhancement on the on-current

Chapter 2 demonstrated experimental evidence that the Coulomb scattering limited mobility for strained Si devices is not enhanced compared to unstrained Si. The question to ask is

what is the impact of the loss of enhancement on nanoscale devices. To answer this question, two devices were constructed, both strained Si. However, the transport model was adjusted for one of the strained Si devices so that its Coulomb scattering limited mobility is enhanced compared to unstrained Si by 1.75X. The two devices were compared, using a super-halo doping concentration that is 13% (to be discussed later) greater than the super-halo doping concentration shown in Fig. 3.1. For equivalent channel doping concentration, the threshold voltage of the devices are equivalent, so a comparison at equivalent gate voltage, of 0.8 V results in equivalent inversion layer electron concentration. Therefore, a comparison of the source-side electron velocity, can be used to determine the influence of Coulomb scattering.

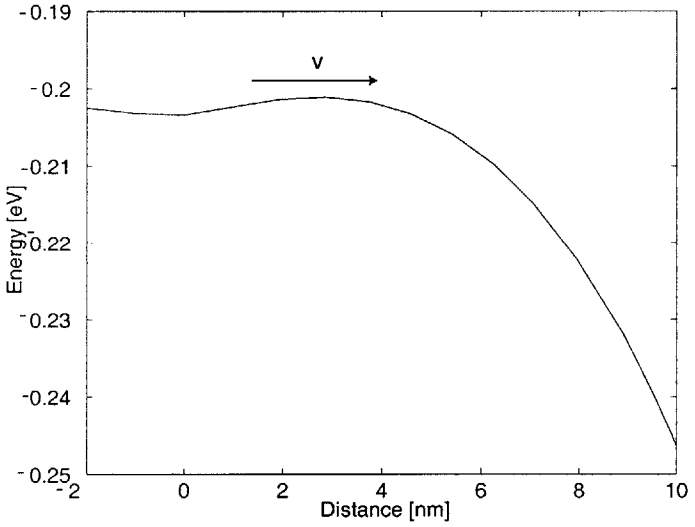

Fig. 3.7 (a) Conduction band energy versus lateral distance in a 25 nm gate length MOSFET. The relevant injection velocity occurs at the peak of the energy versus distance [42].

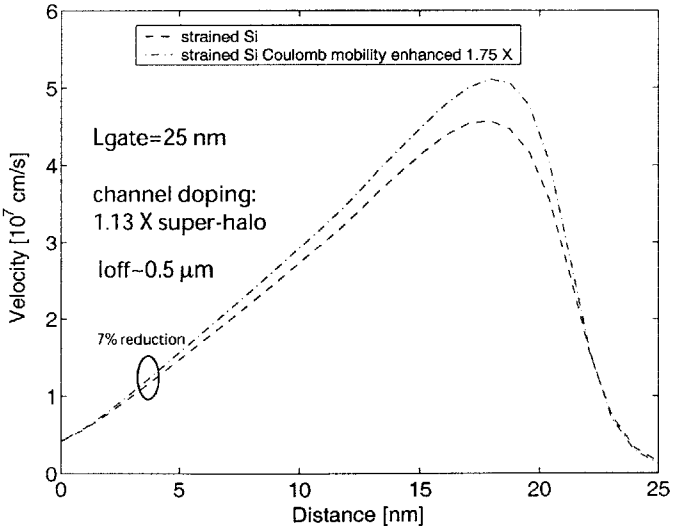

Fig. 3.7 (b) Electron velocity versus distance in a 25 nm MOSFET. The figure compares two strained Si devices. The first one, has the Coulomb limited mobility enhanced over unstrained Si by 1.75X, while the second device uses has no enhancement. As can be seen, the influence of loss of enhancement of the Coulomb mobility results in a reduction of the injection velocity by 7%.

Electron velocity was extracted near the source, defined as the maximum of the conduction band energy as shown in Fig. 3.4 (a) [42]. The electron velocity versus channel length for 25 nm gate length, shown in Fig. 3.4 (b), demonstrates a 7% reduction in source-side velocity. Investigation of the loss of performance enhancement versus channel length show that the enhancement loss increases with decreasing channel length but never exceeds 10% for greater than 20 nm gate length devices. As device gate length is scaled the surface doping increases, as the halo doping

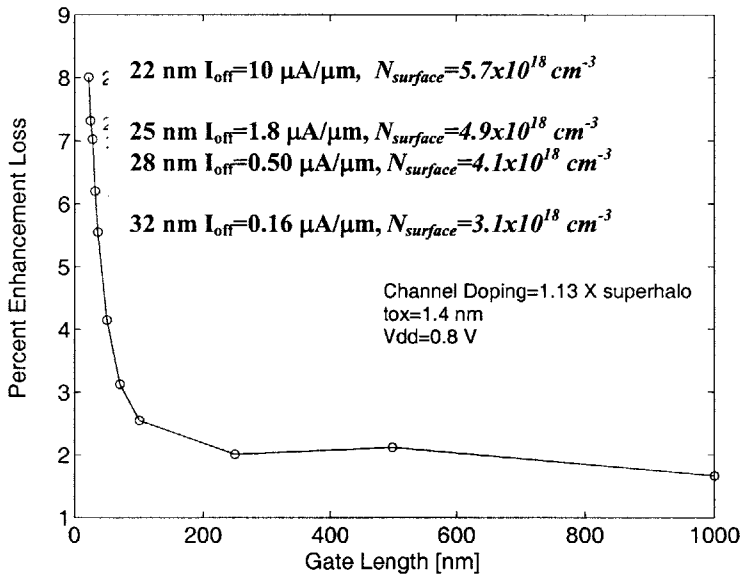

Fig. 3.8. On-current reduction due to loss of Coulomb mobility enhancement. The plot shows that for reduced gate length, the influence of Coulomb scattering increases. However, the loss of on-current is less than 10% for devices with gate length approaching 20 nm.

moves into the channel increasing the influence of Coulomb scattering. The plot shows that for sub-20 nm devices, Coulomb scattering will result in 10% or greater loss in the on-current,

motivating the study of alternative structures such as fully depleted strained Si on insulator that has very low channel doping.

3.6. Influence of the strained Si heterostructure on the electrostatics

As explained briefly in Chapter 2, the threshold voltage of strained Si devices is less than that for unstrained Si. Reduced threshold voltage for strained Si devices can be demonstrated by analyzing the difference in the I_{off} vs. I_{on} characteristics, using the same device structure explained earlier for strained and unstrained devices. The channel doping for the unstrained and strained Si devices are equivalent and equal to the super-halo doping shown in Fig. 3.1. The plot shows, where the variable changing is the gate length that the off-current for the strained Si devices is always larger than for the un-strained Si, demonstrating smaller threshold voltage. Clearly, the strained Si threshold voltage needs to increase by either increasing the channel doping or adjusting the gate workfunction. Before, analyzing which method is superior, it is instructive to study the threshold voltage

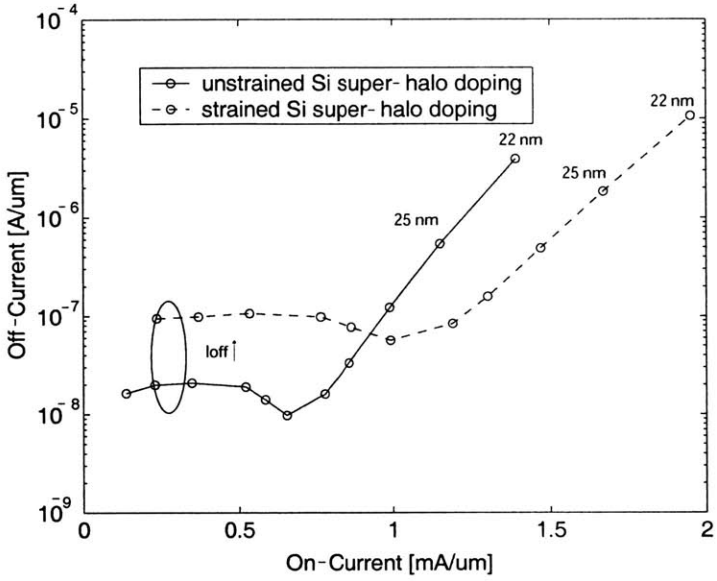

Fig. 3.9. I_{on} vs. I_{off} characteristics for strained and unstrained Si devices with equivalent "super-halo" channel doping. The figure shows that the off-current for strained Si devices is larger than that for unstrained for all gate lengths. The reason for the larger off-current, is reduced threshold voltage for strained Si devices.

3.7. Threshold Voltage of Strained Si n-MOSFETs

Plotting the simulated threshold voltage versus gate length and comparing to un-strained Si devices reveals that the shift in threshold voltage between strained and unstrained devices is about 50 mV. It should be noted that as the device length is reduced, the channel doping increases, due to encroachment of the halo pocket doping into the channel. The simulated threshold voltage is defined as the gate voltage necessary to result in 10^{-7} A/μm drain current. In order to understand the reason behind this shift, it is instructive to review the bandstructure of strained Si.

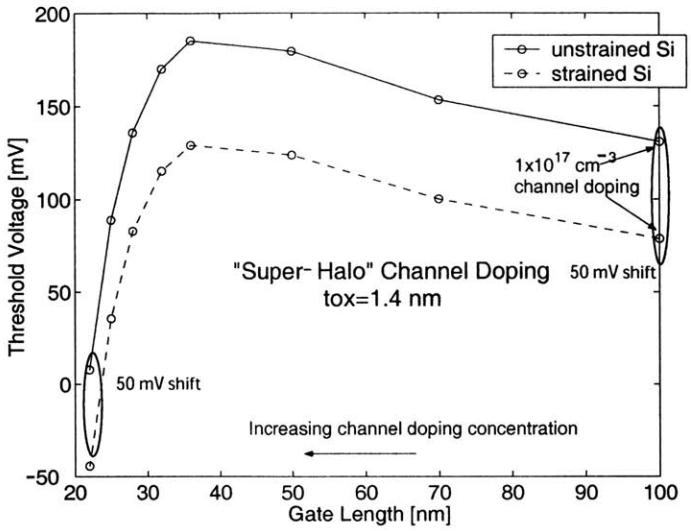

Fig. 3.10. Simulated threshold voltage versus gate length for strained and unstrained Si devices. The threshold voltage is defined as the gate voltage that results in a drain current of 10^{-7} A/μm. As can be seen, the threshold voltage for the strained Si devices is 50 mV less than that for the un-strained Si devices for all gate lengths studied. The channel doping for both devices, is equivalent to the super-halo doping explained earlier.

Figure 3.11 shows the energy band structure at mid-channel is a cross-section at mid-channel for a long-channel device with $5x10^{18}$ cm^{-3} uniform channel doping. In the strained Si device conduction and valence band offsets exist relative to the relaxed quasi-neutral $Si_{0.8}Ge_{0.2}$. The electron affinities for relaxed $Si_{0.8}Ge_{0.2}$ are assumed to be equal which is accurate for low Ge concentration. The increased electron affinity of strained Si versus unstrained Si contributes to a lower threshold voltage. In addition, the bandgap of the quasi-neutral region for the strained Si device, $Si_{0.8}Ge_{0.2}$ is smaller by 100 meV compared to the bandgap of un-strained Si. In addition, the role of the valence band offset is to shift the flatband voltage. To understand how the material

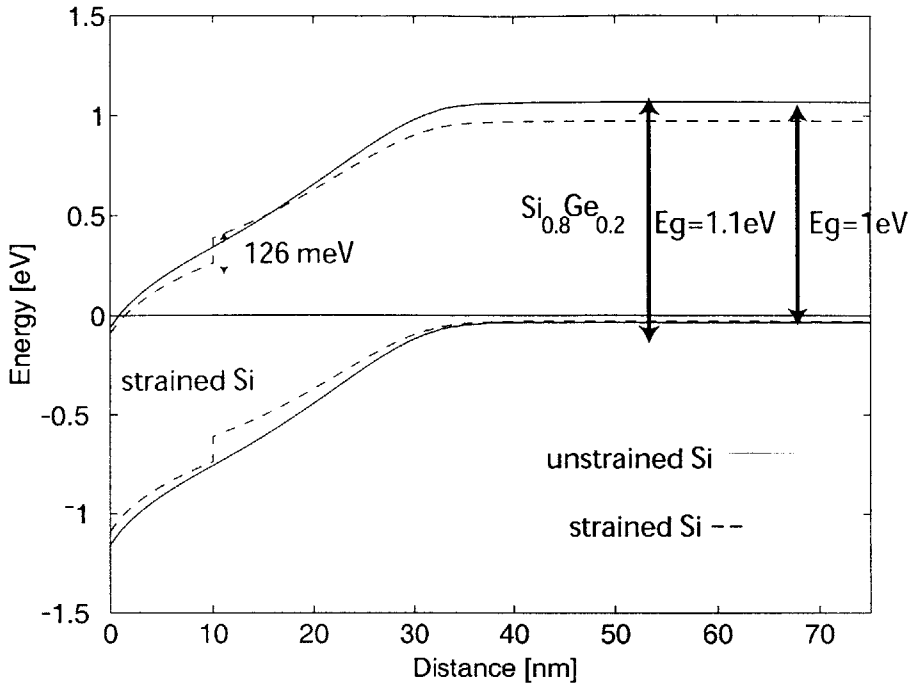

Fig. 3.11. Energy bandstucture for a strained and unstrained Si n-type MOSFET versus vertical distance from the Si/SiO_2 interface. Both devices are long-channel with channel doping of $5x10^{18}$ cm^{-3}. The bandstructure is extracted in strong inversion with V_{dd}=0.8 V for both devices. As can be seen, the strained Si device has a smaller bandgap material in the quasi-neutral region compared to unstrained Si by 100 meV [43], and furthermore, conduction and valence bandoffsets exist [43-45].

differences result in different electrostatic behavior, an analytical expression for the threshold voltage shift can be constructed. The threshold voltage shift defined as:

$$\Delta V_t = V_t^{strained} - V_t^{unstrained} \qquad \text{Equation 3.7.}$$

The threshold voltage shift can then be broken up into three components: (1) flatband voltage shift (ΔV_{fb}), (2) semiconductor voltage drop shift ($\Delta\phi_s$), and (3) oxide voltage drop shift ($\Delta\phi_{ox}$):

$$\Delta V_t = \Delta V_{fb} + \Delta\phi_s + \Delta\phi_{ox} \qquad \text{Equation 3.8.}$$

The semiconductor potential shift is a function of the material differences in particular, the intrinsic electron potential, and conduction band offset in strained Si. It can be expressed as:

$$\Delta\phi_s = \phi_s^{strainedSi} - \phi_s^{Si} \qquad \text{Equation 3.9.}$$

Where $\phi_s^{strainedSi}$ and ϕ_s^{Si} can be expressed as:

$$\phi_s^{strainedSi} = \frac{k_b T}{e}[\ln\frac{N_a}{n_i^{Si_{1-x}Ge_x}} + \ln\frac{N_a}{n_i^{strainedSi}}] - \Delta E_c \qquad \text{Equation 3.10}$$

$$\phi_s^{Si} = \frac{2k_b T}{e}\ln(\frac{N_a}{n_i^{Si}}) \qquad \text{Equation 3.11}$$

The constants are defined as: N_a, channel doping concentration, k_b boltzmann's constant, T is the lattice temperature, and n_i is the intrinsic concentration, and ΔEc is the conduction bandoffset between $Si_{1-x}Ge_x$ and strained Si. The ΔEc can be related to the Ge concentration as: ΔEc=0.53x

[44]. The intrinsic electron concentrations can be related to the effective density of states and the bandgap as:

$$n_i = \sqrt{N_c N_v} e^{-E_g/2kT} \qquad \text{Equation 3.12}$$

Where the effective density of states for the valence and conduction band are a function of the effective density of states mass by:

$$N_{c,v} \propto (m^*_{de,h})^{3/2} \qquad \text{Equation 3.13}$$

The oxide potential shift can be expressed as:

$$\Delta\phi_{ox} = \gamma(\sqrt{\phi_s^{strainedSi}} - \sqrt{\phi_s^{Si}}) \qquad \text{Equation 3.14.}$$

where the body coefficient, γ is defined as:

$$\gamma = \frac{\sqrt{2\varepsilon_s e N_a}}{C_{ox}}$$ Equation 3.15

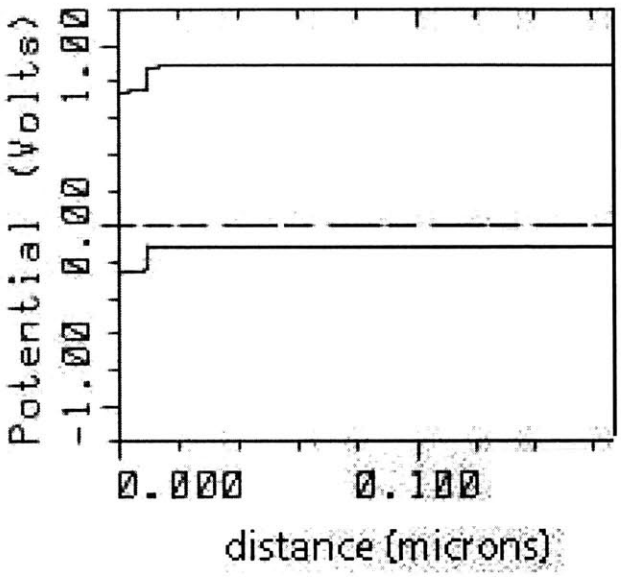

Fig. 3.12 (a) Bandstructure of a strained Si device for a gate voltage such that no band bending occurs in the quasi-neutral region, $Si_{0.8}Ge_{0.2}$.

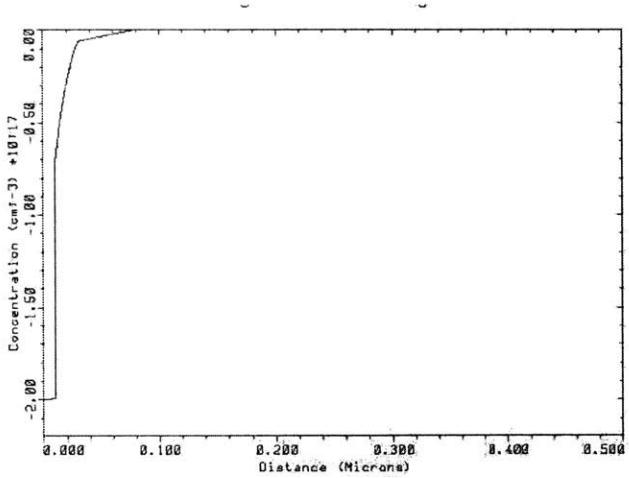

Fig. 3.12 (b). Net charge concentration for a strained Si device versus vertical distance from the Si/SiO_2 interface. The gate voltage is set as the value required to obtain zero bandbending in the $Si_{0.8}Ge_{0.2}$ quasi-neutral region. As can be seen, there exists a net charge in the strained Si layer equal to the density of ionized dopants. The doping concentration in the device simulated is $2x10^{17}$ cm^{-3}.

The flatband voltage shift is dependent on the material differences, with the bandgap of the quasi-neutral region being the largest. In addition, since the strained Si device is a heterostructure layer, there does not exist a flatband voltage. Rather, a reference voltage will be defined such that the no band bending occurs in the SiGe layer. A cross-section showing the bandstructure and net charge for this condition is shown in Fig. 3.9 (a-b). The figure shows that when the SiGe

layer has zero charge, or no band bending, a charge density exists in the strained Si layer equal to *eNa*. The charge is equivalent to a depletion charge, and results in a voltage drop across the strained Si layer, that tends to reduce the threshold voltage. The charge in the strained Si layer is imaged at the gate and is negative and therefore works to increase the threshold voltage. Based on this analysis, the flatband voltage shift can be expressed as;

$$\Delta V_{fb} = E_g^{Si} - E_g^{Si_{1-x}Ge_x} + \frac{kT}{e}\ln\frac{N_v^{Si}}{N_v^{Si_{1-x}Gex}} + \chi^{Si} - \chi^{Si_{1-x}Ge_x} + \frac{eN_a t_{Si}}{C_{ox}} - \frac{eN_a t_{Si}^2}{2\varepsilon_{Si}} \qquad \text{Equation 3.16}$$

The analytical equation was then compared to MEDICI computer simulations, where threshold voltage is defined as the voltage for which the surface concentration is equal to the bulk doping concentration. The strained and unstrained Si devices simulated have t_{ox}=1.4 nm, and varying doping concentration.

Material Parameter	**Strained Si**	**$Si_{0.8}Ge_{0.2}$**	**unstrained Si**
Bandgap, E_g [eV]	1.0	1.0	1.1
Electron Affinity, χ [eV]	4.16	4.04	4.05
Effective electron density of states, N_c [cm-3]	$9.42x10^{18}$	$2.42x10^{19}$	$2.82x10^{19}$
Effective hole density of states, N_v [cm-3]	$8.61x10^{18}$	$1.49x10^{19}$	$1.83x10^{19}$
Intrinsic concentration, n_i [cm^{-3}]	$4.0x10^{10}$	$8.44x10^{10}$	$1.48x10^{10}$

Table 3.4. Material parameters used for the analysis of strained and unstrained Si devices. Constants obtained from the literature [43-45].

The material constants used are summarized in Table. 3.4. It should be noted that increased dielectric constant for SiGe alloy material was shown to influence the threshold voltage to a very small extent. The results presented in Fig. 3.10 for a virtual substrate of $Si_{0.8}Ge_{0.2}$ and strained Si thickness of 100 A demonstrate close agreement for channel doping less than 10^{18} cm^{-3}. For higher channel doping the depletion region depth approaches the strained Si thickness, so that the above model requires modification. The analytical formula does predict, though, the doping concentration at which the shift begins to increase. The shift appears to be constant with doping, and then increases in magnitude for channel doping concentration of 10^{18} cm^{-3}. To understand the cause of increased magnitude of threshold voltage shift the plot shows the shift broken up into its three components. As can be seen, the semiconductor potential shift appears to be constant with doping, but the oxide and flatband voltage shift increase in magnitude with increased doping. If the shift becomes larger with increased doping concentration, the question arises concerning the simulated devices with varying channel length and super-halo doping discussed at the start of this section: why is the calculated shift in Fig. 3.10 the same for all channel lengths, when the surface doping concentration is increasing with gate length scaling?

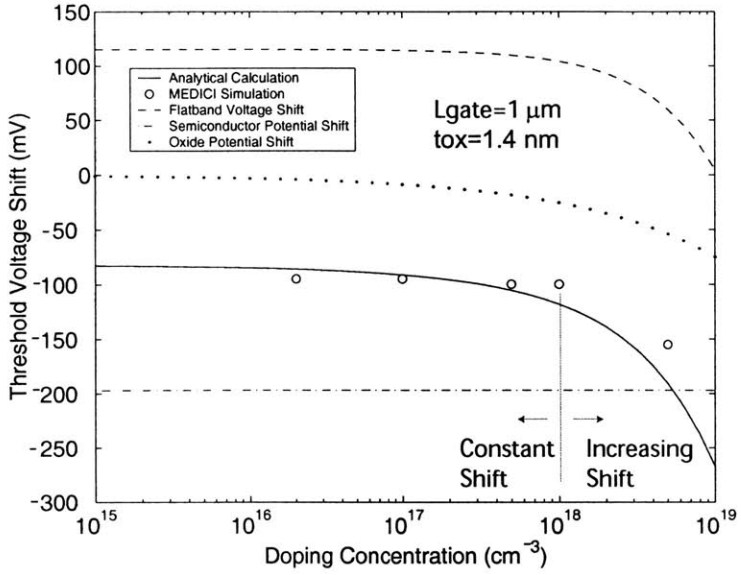

Fig. 3.13. Threshold voltage shift, defined as the difference between the threshold voltages of strained Si devices and unstrained Si devices for varying channel doping concentration. The devices studied are long-channel, with gate length of 1 μm, so that only doping effects are analyzed. Close agreement can be seen between the analytical formula discussed in the text and the MEDICI simulations. The shift appears to be constant with doping, but increased in magnitude for doping concentrations greater than $1x10^{18}$ cm^{-3}. The different components of the shift are also plotted demonstrating that the oxide and flatband voltage shift result in increased magnitude of the threshold voltage shift with increased doping concentration.

3.7.1. Influence of Channel Length on the Threshold voltage shift

In order to study the effect of channel length on the threshold voltage shift, devices were studied with equivalent uniform channel doping of $5x10^{18}$ cm^{-3}.

The shift in the logIV characteristics for low applied drain voltage, V_{ds}=50 mV, was calculated for L_{gate}=25 nm and L_{gate}=1 μm. As shown below in Fig. 3.11, the influence of channel length on the threshold voltage shift can be explained in terms of charge sharing. Specifically, as the device gate length is reduced, the effective channel charge is reduced due to charge sharing from the source/drain potential.

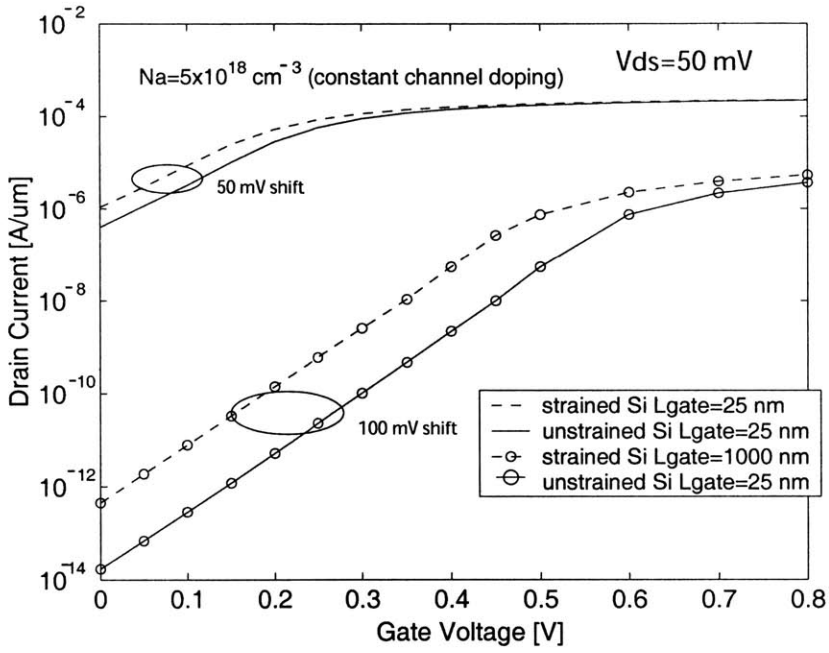

Fig. 3.14. logIV characteristics of strained and unstrained Si devices with equivalent uniform channel doping concentration of $5x10^{18}$ cm^{-3}. Two gate length devices are studied, long channel with gate length=1 μm, and short-channel with gate length of 25 nm. The plot shows that the shift in threshold voltage, measured in terms of the shift in the logIV characteristics decreases for reduced gate length.

An illustration of charge sharing, shown below in Fig. 3.12, demonstrates that the effective depletion charge imaged by the gate is reduced from a long-channel value of Q_b to a smaller value of Q_b' for short channel devices.

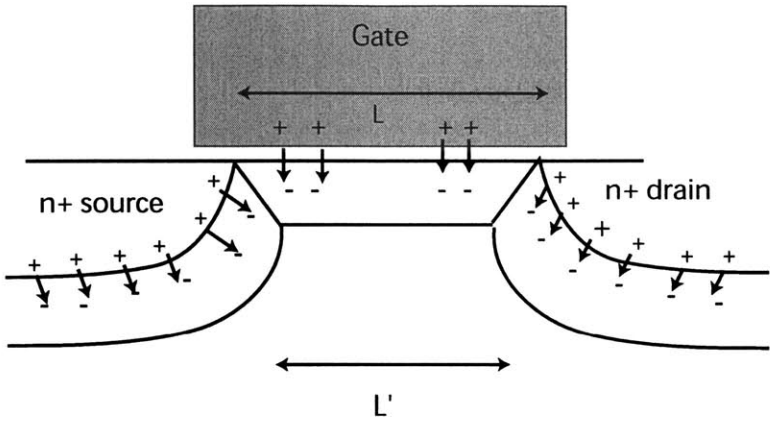

Fig. 3.15. Illustration of charge sharing in a short-channel MOSFET. For short-channel devices, the source/drain potential support a fraction of the depletion charge in the channel, so that the effective integrated charge supported by the gate (Q_b') is smaller than that for long-channel devices (Q_b). *After Yau et al. [46]*

The charge sharing results in reduced threshold voltage, and is observed experimentally as the well-known threshold voltage rolloff characteristics with gate length. In particular, the threshold voltage can be expressed as [46]:

$$V_t = V_{fb} + 2\phi_b + {Q_b'}/{C_{ox}} \qquad \text{Equation 3.17}$$

As a result, the charge supported by the gate decreases for reduced gate length, and as demonstrated in the previous section, decreased doping results in smaller threshold voltage shift.

3.8. DIBL and Sub-Threshold Slope

Drain induced barrier lowering and sub-threshold slope also influence the logIV characteristics. An accurate understanding of the differences in these two parameters for strained

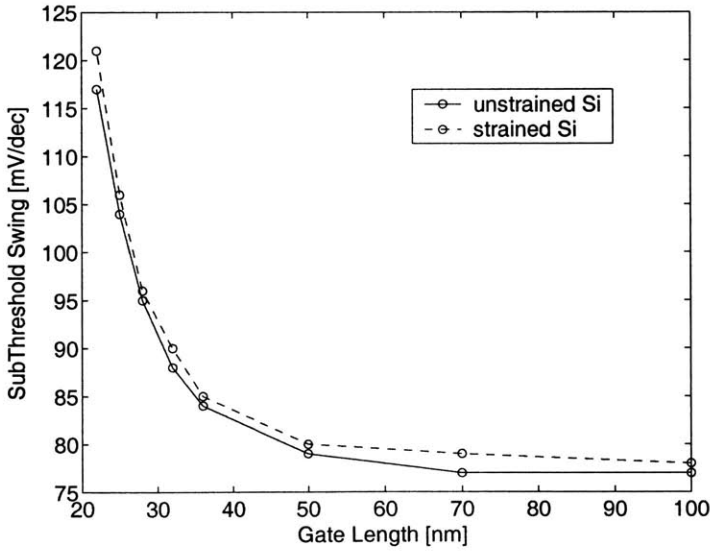

Fig. 3.16 Sub-threshold slope of strained and unstrained Si devices versus gate length. Both devices have super-halo doping channel doping. The slope is slightly larger for the strained devices, due to a slightly larger depletion region depth, and larger dielectric constant.

and unstrained Si devices is required. Fig. 3.12 shows the sub-threshold slope versus gate length for strained and unstrained Si devices, with equivalent super-halo channel doping. The plot shows that the sub-threshold slope for the strained Si devices is slightly larger for all gate lengths, but less than 5% larger. As a result, sub-threshold slope differences do not result in off-current differences. Slightly larger sub-threshold slope for strained Si devices is due to a smaller depletion depth for the same gate voltage and slightly larger dielectric constant. Next the DIBL was analyzed versus gate length and was shown to be almost equivalent as shown in Fig. 3.13. Therefore, since the DIBL and sub-threshold slope are almost equivalent, threshold voltage shift is the cause of larger off-current for strained Si versus unstrained Si devices.

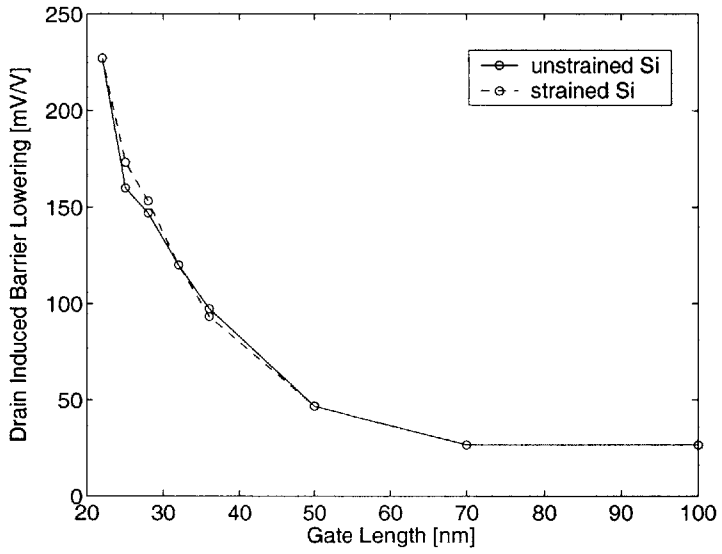

Fig. 3.17. DIBL versus gate length for strained and unstrained Si devices. Both devices have equivalent super-halo doping concentration. The DIBL is almost equivalent for both devices, eliminating DIBL as a possible cause of off-current differences between strained and unstrained Si devices.

Finally, a critical analysis of the electrostatics was performed to investigate the scaling behavior of strained Si devices. Devices were analyzed by varying one parameter- the depletion depth, based on the analytical expression for threshold voltage discussed in the previous section. Since the semiconductor potential is reduced for strained Si versus unstrained Si devices for the same gate voltage, the depletion depth is reduced for the same channel doping as shown in Fig. 3.15 above. The depletion region depth can be related to the scalability of a device. In particular, reduced depletion depth, results in decreased short-channel effects.

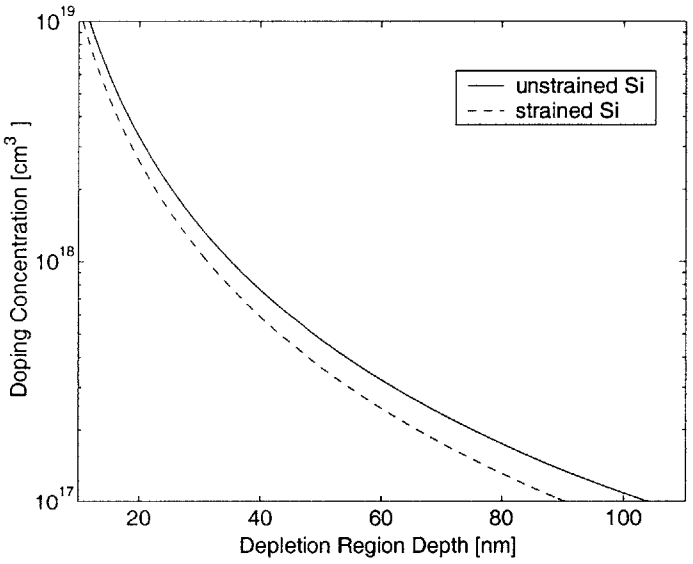

Fig. 3.18. Depletion region depth versus doping concentration for strained and unstrained Si devices, calculated in strong-inversion. The depletion region was calculated using the threshold voltage equation expression discussed in the previous section. The deletion depth is smaller for strained Si versus unstrained Si devices for a given channel doping concentration.

A method of studying the effect of varying the depletion depth on the short-channel effects of MOSFETs, is to study a simplified device with structure shown below in Fig. 3.16 [47].

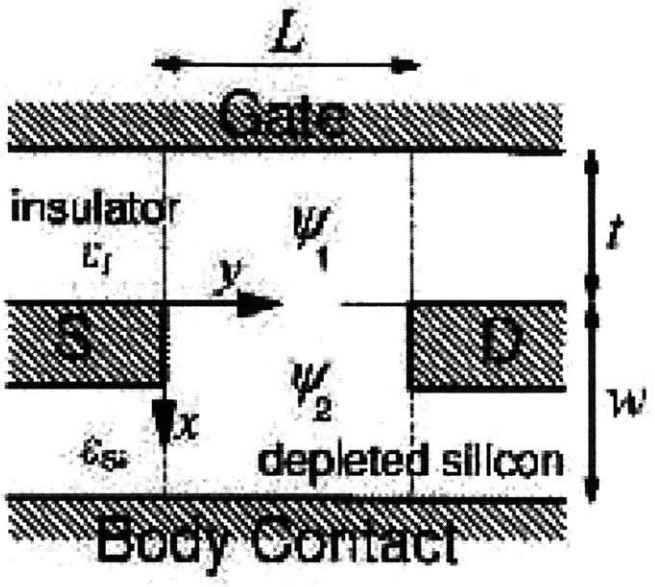

Fig. 3.19. Simplified MOSFET structure used to analyze short-channel effects of MOSFETs in terms of their depletion depth,w [47]. The potential in the channel can be expressed in terms of analytical expressions, discussed in the text.

The key parameters are t, the oxide thickness, w the depletion region thickness in strong-inversion condition, and L the gate length. The potential in the middle of the channel can be expressed as a function of these key parameters [42]:

$$\phi_{center} \propto e^{-\pi L/2\Lambda} \qquad \text{Equation 3.18}$$

$$\varepsilon_s \tan(\pi t/\Lambda) + \varepsilon_I \tan(\pi w/\Lambda) = 0 \qquad \text{Equation 3.19}$$

The symbols are defined as: ε_s, semiconductor dielectric constant, ε_I, insulator dielectric constant, w, depletion depth, Λ, is a constant with units of length and is defined as the scalelength. A device with tolerable short-channel effects should have $L/\Lambda > 1.5$. Using this

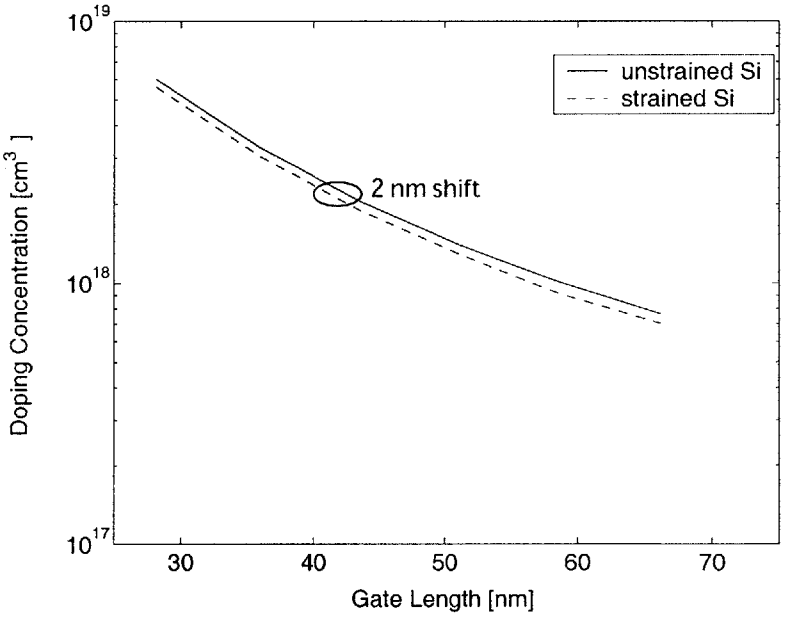

Fig. 3.20. Doping concentration for strained and unstrained Si devices versus gate length. As can be seen, the scalelength for the strained Si devices is smaller by 2 nm than the unstrained Si devices. As a result, strained Si devices are more scalable. However, they are scalable by only 2 nm, so only a slight gain can be seen, as shown in the text.

formulation, strained and unstrained Si devices were compared in terms of their scalelength

versus gate length. As shown below in Fig. 3.17, the scalelength of strained Si devices is reduced compared to unstrained Si, but by only roughly 2 nm. Therefore, strained Si will help scaling but only slightly. This finding is consistent with the previous section that showed similar short-channel effects, analyzed in terms of DIBL and sub-threshold slope for strained and unstrained Si devices.

3.9. Scaling Methodology for nanoscale strained Si MOSFETs

As shown previously, strained Si devices simulated in this work have a threshold voltage of approximately 50 mV less than the unstrained Si for equivalent channel doping concentration, and for all gate length devices. In order to match threshold voltage, either the gate workfunction or channel doping concentration for the strained Si devices should increase. To study the two methods, two strained Si devices were studied, one with gate workfunction 55 mV larger than n^+ polysilicon, and the other with 13% larger channel doping concentration than the super-halo discussed previously. Both devices were compared to unstrained Si devices with super-halo doping for varying gate channel lengths. The results presented in terms of I_{on} vs. I_{off} characteristics, show significant on-current enhancement, of 30% for a given I_{off} for 25 nm gate length strained Si devices, consistent with the 65 nm technology node. The results also show that the gains in I_{on} in using a gate workfunction material are minimal, demonstrating that increased doping appears to be a more practical solution to match I_{off} with unstrained devices. The current increase of 30% is about 7% lower than theoretically predicted assuming a ballistic limit of 0.5

for the 25 nm devices. B=0.5 would predict a 37% increase, or one-half of the 75% increase in low-lateral electric field mobility. The reduced I_{on}, is attributed to loss of enhancement of the Coulomb scattering limited mobility. The results indicate that the surface doping concentration should be minimized to enjoy the full benefits of strained Si devices, and that increasing channel doping is a practical method of matching I_{off} to unstrained devices in the 25 nm gate length regime.

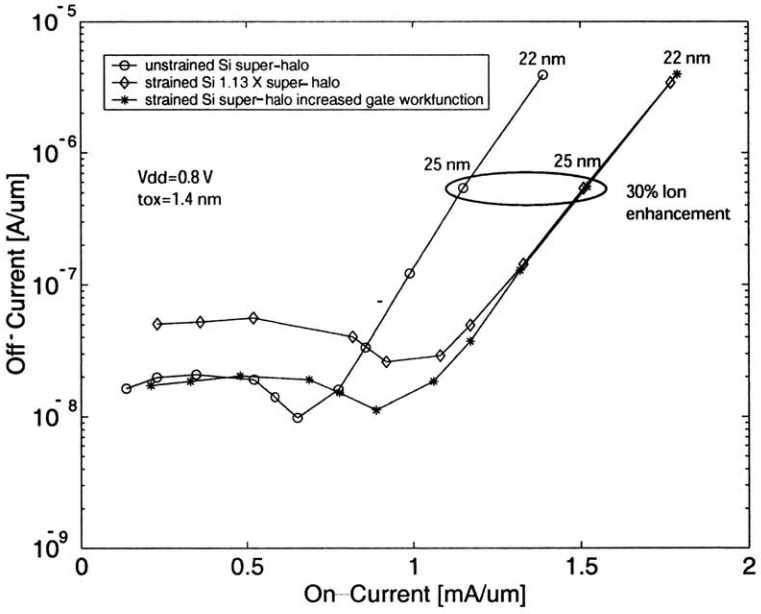

Fig. 3.21. On-current versus off-current for three devices: (1) unstrained Si, (2) strained Si with increased gate workfunction over n^+ polysilicon of 55 mV, and (3) strained Si with 13% increased channel doping concentration over unstrained Si. The unstrained Si devices have channel doping equivalent to the super-halo discussed earlier in this Chapter. The figure indicates significant I_{on} enhancement for a fixed I_{off} at channel length of 25 nm, for both strained Si devices.

3.10. Conclusions

In conclusion, this chapter has demonstrated that strained Si nanoscale n-MOSFETs will result in significant drain current enhancement over unstrained Si devices, for the same off-current. The influence of Coulomb scattering on on-current for 25 nm channel length devices was demonstrated to be less than 10%. The electrostatics of strained Si devices were analyzed, and it was shown, that for equivalent channel doping concentration, the off-current is larger compared to unstrained Si. The larger I_{off} was shown to be due to reduced threshold voltage. The dependence of threshold on doping concentration and channel length was presented. Specifically, it was shown that for increased channel doping concentration, the threshold voltage shift increases, and for reduced channel length, the shift is reduced, for equal doping concentration. The analysis of the electrostatics showed that threshold voltage shift is the prime indicator of I_{off} differences between strained and unstrained devices. Finally, a scaling methodology was presented for nanoscale devices. It was shown that increased halo doping over unstrained Si devices is a practical solution that results in significant drain current enhancement, and equivalent off-current.

Chapter 4

Design of Strained Si/SiGe CMOS Transistors

In this Chapter, a strained Si/SiGe CMOS design is proposed, with the aid of computer simulations that provides for enhanced electron and hole transport and well-behaved electrostatics. The electron channel is tensile strained-Si grown on relaxed $Si_{1-y}Ge_y$ virtual substrate and a high Ge content $Si_{1-x}Ge_x$ ($x>y$) under compressive strain is used for the hole channel. Computer simulations show that the proposed structure has optimum electrostatics in terms of sub-threshold behavior. The short-channel effects of the design for sub-50-nm MOSFETs are shown to be similar to bulk-Si demonstrating ability for extending conventional bulk-Si CMOS scaling.

4.1. Motivation

It is well known that enhanced performance n-and p-type MOS devices have been demonstrated using strained Si/SiGe heterostructures [48-51]. A key question is the integration of both n-and p-type devices on a single substrate for CMOS application. Surface channel strained Si structures provide enhanced electron mobility, but relatively small enhanced hole mobilities at the high vertical effective electric fields associated with bulk devices. Sadek et al. proposed a strained Si/SiGe layer design substrate for enhanced performance CMOS application based on a MODFET scheme resulting in deviation from conventional bulk CMOS design [52]. In this Chapter, a strained Si/SiGe CMOS design is proposed that has design complexity similar to bulk-Si CMOS where n-and p-type devices are based on surface and near-surface channel designs while providing for both enhanced electron and hole transport and well-behaved electrostatics. The scaling behavior of the proposed design is studied for sub-50-nm gate lengths with the aid of computer simulations incorporating quantum mechanical effects and compared to bulk-Si.

4.2. Layer Structure

The key question for the layer design is how to achieve enhanced electron and hole mobility over bulk Si. In addition, both mobilities should be close in value resulting in well-balanced CMOS design. Electron mobility enhancement of 1.7-2X has been demonstrated in strained Si films grown on SiGe, and enhanced hole mobility of 3-4X in compressively strained $Si_{1-x}Ge_x$ grown on relaxed $Si_{1-y}Ge_y$ (x>y) resulting in enhanced and similar performance for n-type and p-type MOS devices [53]. The enhanced transport for electrons and holes are explained

in terms of reduced conduction electron/hole mass and by energy splitting of the bandstructures at the conduction/valence band resulting in reduced momentum scattering rates [54-55]. A CMOS structure that takes advantage of enhanced electron/hole mobility in strained Si/SiGe structures is shown in Fig. 4.1, which is impractical to implement since the optimum n-and p-type devices cannot be formed on the same substrate.

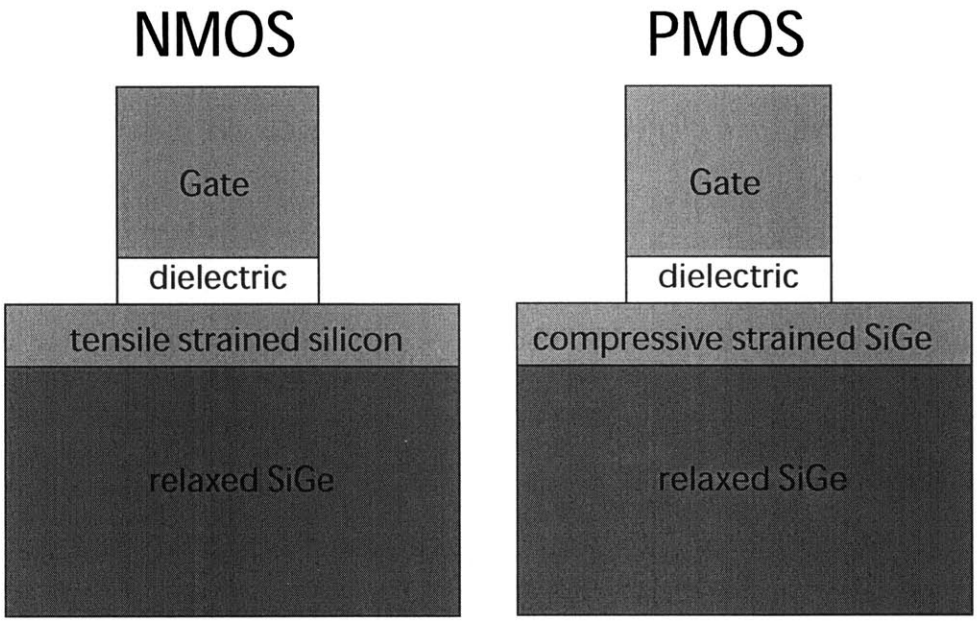

Fig. 4.1. Ideal heterostructure layer for CMOS transistors for enhanced electron and hole performance over bulk Si. The electron channel is tensile strained Si and the hole channel is compressive strain $Si_{1-x}Ge_x$. Both areas are grown on a virtual substrate of $Si_{1-y}Ge_y$ ($x>y$). The left/right side corresponds to n/p-MOS devices. The dark areas denote the location of the electron or hole channel.

In addition, the formation of a gate insulator on $Si_{1-x}Ge_x$ is not well understood where oxidation results in a poor interface in terms of increased interface trap density [51]. A structure

that is symmetric, equivalent layer structures for n-and p-type devices, and uses a silicon cap layer for the p-MOS device to facilitate oxidation, is shown in Fig. 4.2 and is named a "dual-channel design".

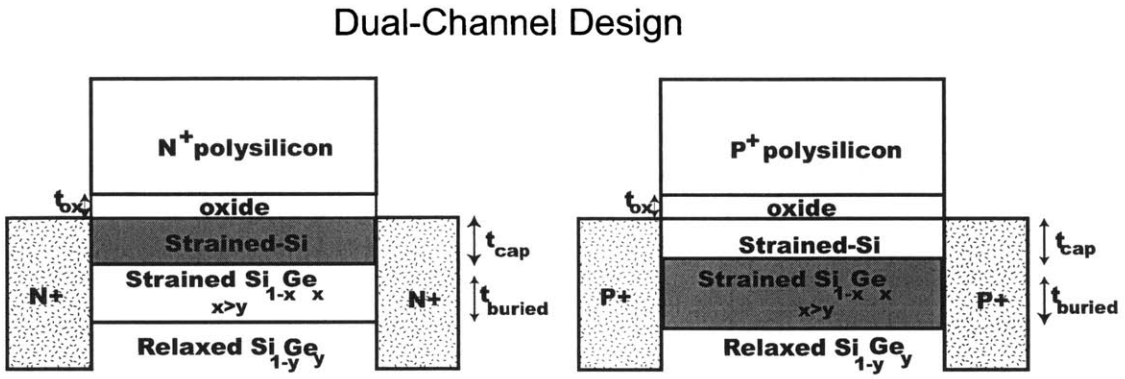

Fig. 4.2. CMOS transistor design that provides for performance enhancement. The electron channel is tensile strained Si and the hole channel is compressive strain $Si_{1-x}Ge_x$. Both areas are grown on a virtual substrate of $Si_{1-y}Ge_y$ ($x>y$). The left/right side corresponds to n/p-MOS devices. The dark areas denote the location of the electron or hole channel. The design is called the "dual-channel design".

The thickness of all layers is constrained to be thinner than the critical thickness for strain relaxation [57]. All layer structures are built on a virtual substrate that is achieved by starting with a Si substrate and growing a graded SiGe buffer to the lattice constant of $Si_{1-y}Ge_y$ in order to minimize threading dislocations [58].

4.3. Electrostatic Modeling

Next, the electrostatics of the optimum layer structure in terms of performance benefit was investigated. In particular, the sub-threshold behavior, which is indicative of power dissipation, was studied as a function of layer thickness and Ge concentration in the hole channel, x using MEDICI computer simulations [59]. In order for the simulations to be relevant for sub-50-nm designs, device parameters for an effective gate length (L_{eff}) technology of 25 nm are used. The devices that were modeled have channel lengths of 1 μm in order to study intrinsic effects of the heterostructure (i.e. short-channel effects are not involved).

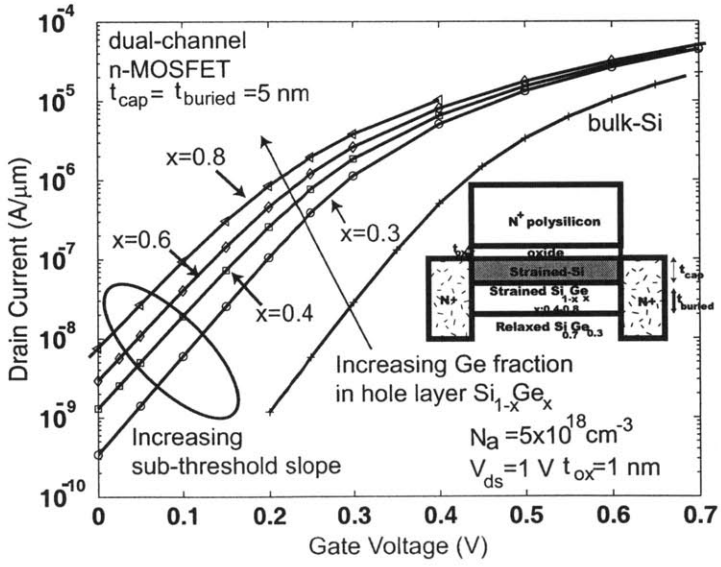

Fig. 4.3. Drain current versus gate voltage for the dual-layer n-MOSFET design for varying Ge fraction in the hole layer, x. Increased x results in a deviation in the sub-threshold current where the threshold voltage, V_t is reduced and sub-threshold swing, SS increases.

Drain current characteristics of the n-MOSFET device, for varying cap thickness, t_{cap}, show increased sub-threshold swing, SS and reduced threshold voltage with increased x and decreased t_{cap} as shown in Fig. 4.3 and 4.4.

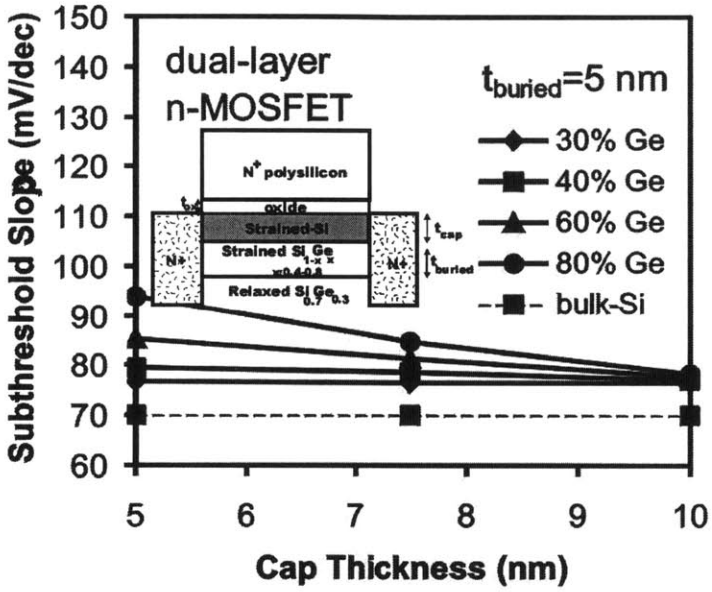

Figure 4.4. Sub-threshold swing (SS) vs. cap thickness (t_{cap}) for the dual-layer n-MOSFET showing increased SS with reduced t_{cap}. The increased SS is attributed to an effective reduction in the depletion depth to x_d=t_{cap}.

It is hypothesized that the existence of a high-content Ge buried layer, within the space-charge region, increases the semiconductor capacitance due to charge modulation by the gate voltage where the capacitance has dielectric thickness equivalent to t_{cap}. The increased semiconductor capacitance results in increased SS. Large hole concentration occurs in the sub-threshold regime of operation due to a significant valence band offset between strained-Si/$Si_{1-x}Ge_x$, which acts to

readily confine holes. Fig. 4.5 plots the band diagram at mid-channel for the case studied

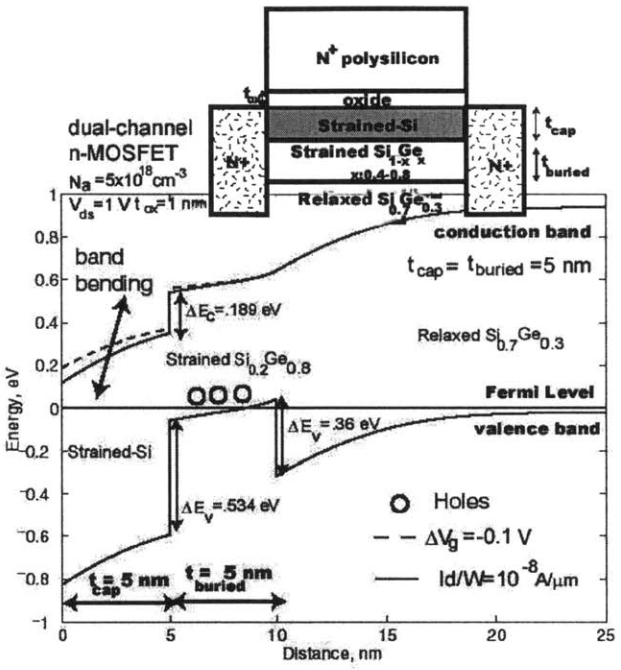

Fig. 4.5. Band diagram in sub-threshold for two gate voltages resulting in operation in the sub-threshold regime for the dual-layer n-MOSFET device. A large hole concentration is present in the SiGe layer, which decreases the depletion region depth and results in increased sub-threshold swing, SS.

(x=0.80, y=0.30) [60].

The increase in sub-threshold swing becomes more pronounced for increased x, suggesting a fundamental tradeoff between performance and power dissipation, since increased x results in increased hole mobility and at the same time, increased valence band offset, ΔE_v as shown in Fig. 4.5. The hypothesis that the buried hole layer increases the semiconductor capacitance was tested by using the analytical expression for sub-threshold swing:

$SS = (1 + \frac{\varepsilon_s}{\varepsilon_{ox}} \frac{t_{ox}}{x_d})60$ mV/dec where ε_s and ε_{ox} are the semiconductor and oxide dielectric constants, t_{ox} is the electrical oxide thickness, and x_d is the maximum depletion layer depth. For devices with buried layers, x_d is replaced by t_{cap} if $t_{cap} < x_d$ which is the case for the devices studied in this work which have channel doping $N_a = 5x10^{18}$ cm^{-3} resulting in x_d ~15 nm. Using the analytical

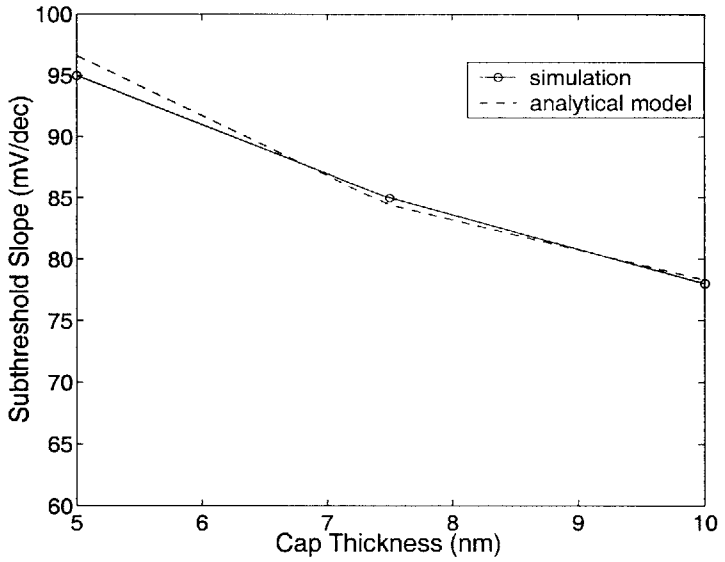

Fig. 4.6. Sub-threshold swing (SS) vs. cap thickness (t_{cap}) for the dual-layer n-MOSFET calculate using an analytical expression where the semiconductor capacitance is adjusted due to the large hole concentration in the buried layer. The analytical model shows close agreement with the simulations results allowing for accurate prediction of SS with reduced computation expense.

expression, the calculated SS matches the simulated SS for x=0.80 for various t_{cap} as shown in Fig. 4.6.

Increased dielectric constant of $Si_{1-x}Ge_x$ material, calculated by interpolating between the dielectric constant of Si, 11.9 and Ge, 16 and the buried channel thickness, t_{buried}, were both

verified to have negligible effect on SS further supporting the hypothesis. The results demonstrate that a n-MOS design that does not have a material that readily confines holes beneath the transport channel (strained Si) is required to optimize the sub-threshold behavior, suggesting that the "dual-channel" is not an optimum CMOS design. An example of a design that eliminates the $Si_{1-x}Ge_x$ layer beneath the strained Si layer, shown in Fig. 4.7, is named the selective etch design.

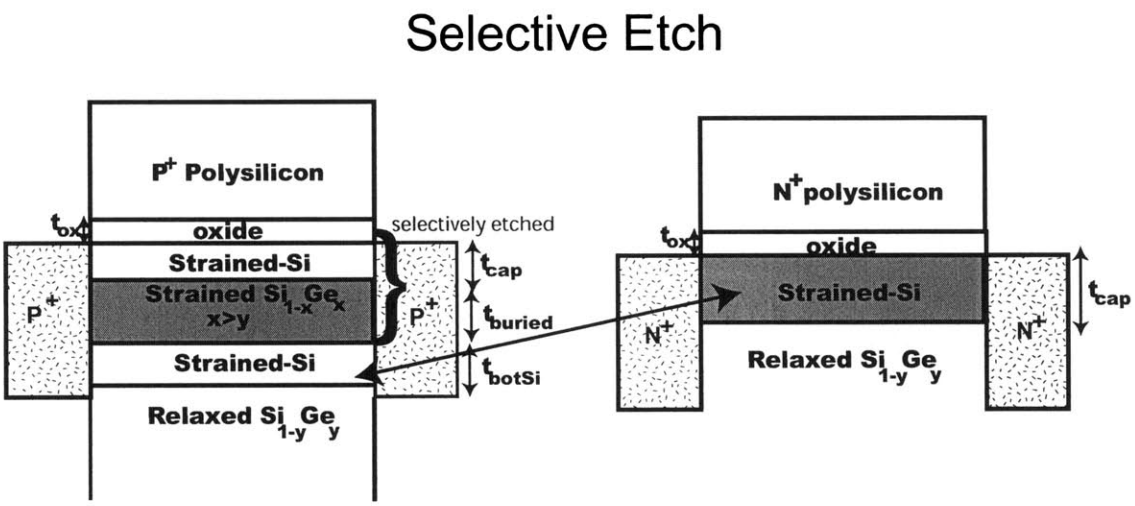

Fig. 4.7. CMOS design where the $Si_{1-x}Ge_x$ is eliminated from the n-MOS device resulting in improved SS. The layers shown for the p-MOS device are grown, where the top two layers are selectively etched to achieve the n-MOS device. The device is named selective etch.

The heterostructure layers, shown for the p-MOS device, are first grown using the graded buffer technique as explained previously. Next CMOS processing proceeds, where after well definition and isolation, areas dedicated for n-MOS devices undergo a selective etch of the top layers where wet chemical solutions that etch Si/SiGe with selectivity to both materials respectively are readily available [61]. The electrostatics of the design, investigated using computer simulation, and compared to the p-MOS dual-channel design show larger SS, as shown

in Fig. 4.8 and is due to a similar effect as observed for the n-MOS devices where in general, it is found that sub-threshold behavior is degraded when a channel of opposite polarity is present beneath the transport channel, for cases where the layers are located inside the space-charge region.

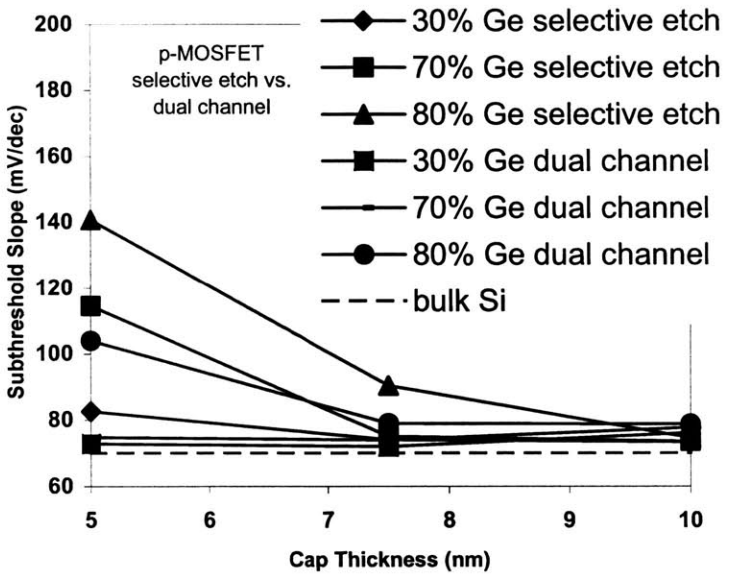

Fig. 4.8. Sub-threshold swing, SS, of the p-MOSFET "selective etch design" compared to the "dual-channel design". The SS is degraded for both designs, compared to a bulk-Si device with the degradation increased for decreasing t_{cap} and increased Ge fraction for the hole layer, x. SS is larger for the selective etch design compared to the dual-layer design due to the strained-Si layer beneath the hole layer that acts to reduce the depletion layer depth. The channel doping for the devices studied are $5x10^{18}$ cm-3 uniform, and the oxide thickness t_{ox}=1.5 nm.

It is expected that the buried heterostructure layers will be inside the depletion region since the space-charge layer is reduced with gate length scaling by increasing channel doping, and is on the order of less than 20 nm for sub-50-nm devices, greater than the critical thickness for strain relaxation. In order to improve the SS behavior, the strained Si layer, which is the electron

channel for the n-MOS devices is separated from the $Si_{1-x}Ge_x$ layer by including a $Si_{1-y}Ge_y$ spacer layer as shown in Fig. 4.9 resulting in a structure that is optimum in terms of performance and sub-threshold behavior and is named the proposed structure.

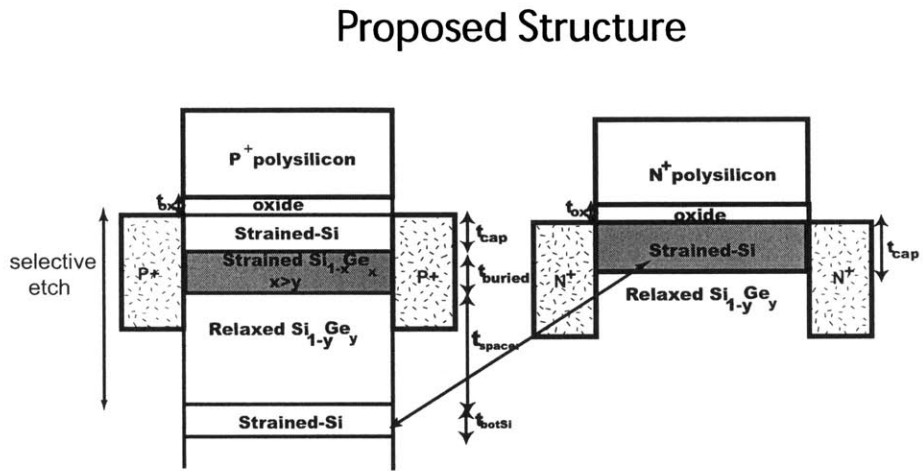

Fig. 4.9. Proposed CMOS structure. The n-MOSFET design shown to the left is a surface-channel device and does not have a hole channel beneath resulting in low sub-threshold slope. The p-MOSFET design show to the right is a buried-channel design where the top silicon layer acts as a gate oxidation sacrificial layer. Beneath the hole layer is a spacer layer that is equivalent to the virtual substrate that acts to spatially separate the strained-Si layer from the hole layer. The bottom strained-Si layer is the channel layer for the n-MOSFET device, which is achieved by selectively etching the top three layers for the p-MOSFET device.

The Ge content of the SiGe spacer layer is equivalent to that of the virtual substrate, so that it is lattice matched, with appropriate thickness, t_{spacer} that places the location of the bottom strained Si layer outside the space-charge region. The proposed structure eliminates the hole channel beneath the electron channel so that the Ge fraction can be increased for the p-MOS device, increasing performance enhancement and minimizing the SS, and therefore the power dissipation. The threshold voltages, V_t, of the proposed structure, which will be studied later in this paper, is reduced for both n-and p-type devices so that investigation of alternative gate material with varying workfunction is required.

4.4. Modeling of Buried-Channel p-MOSFETs Devices: Quantum Mechanical Simulation

Since the proposed p-MOS device is buried-channel, with the potential of being a surface device if a suitable gate insulator can be found, the design is more complicated than a surface-channel [63]. In particular, a competition for hole concentration exists between the strained Si cap layer and the $Si_{1-x}Ge_x$ buried well where it is preferred, in terms of performance benefit, for holes to occupy the buried well. This is the case since carrier mobility near the Si/SiO_2 interface is degraded due to increased surface roughness scattering and the hole mobility enhancement of tensile strained Si is degraded compared to $Si_{1-x}Ge_x$, especially at high vertical electric fields [64]. To investigate hole occupancy, calculations were performed using the DESSIS simulator incorporating quantum mechanical effects using the density gradient method where device parameters equivalent to the devices discussed earlier were used with y=0.30 and x=0.60 [65]. The lower effective hole mass in strained $Si_{1-x}Ge_x$ layers was taken into account by adjusting the

constant term, which is inversely proportional to mass in the quantum potential expression [66]. The mass of relaxed $Si_{1-x}Ge_x$ is an approximation since compressive strain results in a deformation of the valence band shape so that a single mass cannot be used [67]. The simulations show that $t_{cap}< 2$ nm is required to achieve significant hole confinement in the buried well, where the ratio of holes in the buried layer to the cap is roughly 50% for $t_{cap}=2$ nm as shown in Fig. 4.10.

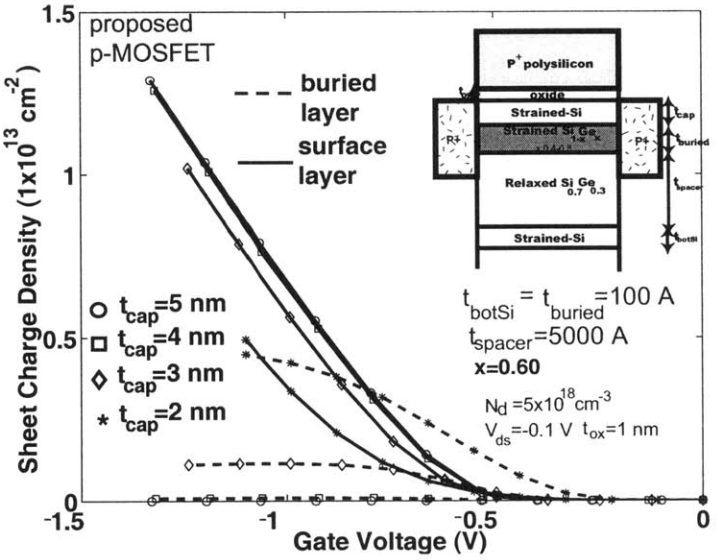

Fig. 4.10. Sheet charge density in the surface and buried channel for the proposed p-MOSFET structure for varying cap thickness. The figure shows that significant hole confinement in the buried layer occurs for cap thickness of 2 nm.

For $t_{cap}=2$ nm, the hole concentration in the buried layer shows a dependence upon gate voltage which reaches a plateau for V_{gs} approaching 1 V indicative of screening of the buried charge by

the inversion layer. The voltage of 1 V where the concentration reaches a plateau is suitable since higher magnitude voltages will not be used for sub-50-nm high-performance logic transistors. The results also indicate that a 10 A variation in t_{cap} changes the buried channel hole concentration occupancy significantly. The drain current characteristics versus gate voltage further demonstrate the sensitivity of the electrostatics to t_{cap}, where for decreasing t_{cap} (2-5 nm) the magnitude of the threshold voltage is reduced indicating increased hole confinement in the buried well as shown in Fig. 4.11.

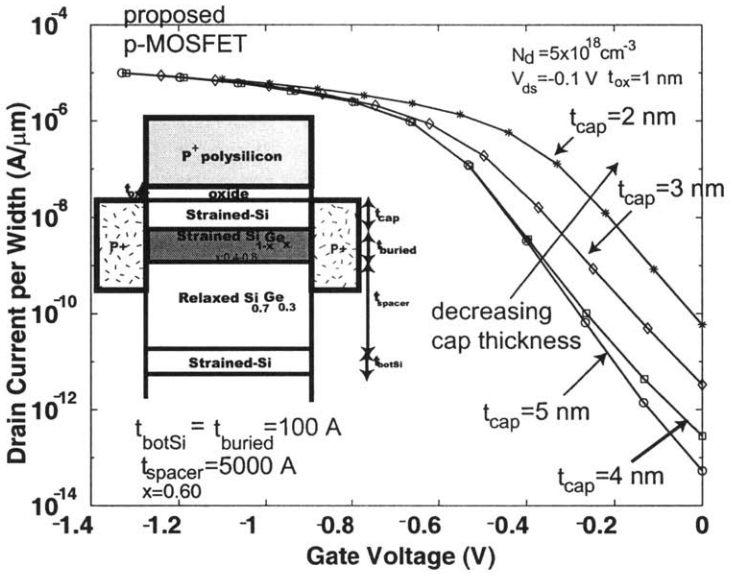

Fig. 4.11. Drain current versus gate voltage for the p-MOSFET proposed structure for varying cap thickness. The Ge fraction, *x,* was chosen to be 0.60. The figure shows a shift in threshold voltage and an increase in sub-threshold slope with reduced cap thickness, t_{cap} due to confinement in the buried layer.

Investigation of the SS dependence upon t_{cap} shows a peak for t_{cap}=3 nm and a decrease with reduced t_{cap} as shown in Fig. 4.12. The initial increase is attributed to increased confinement in the buried well resulting in an increased effective gate insulator thickness. The decrease of SS for t_{cap}< 3 nm is a result of increased carrier confinement in the buried well resulting in reduced

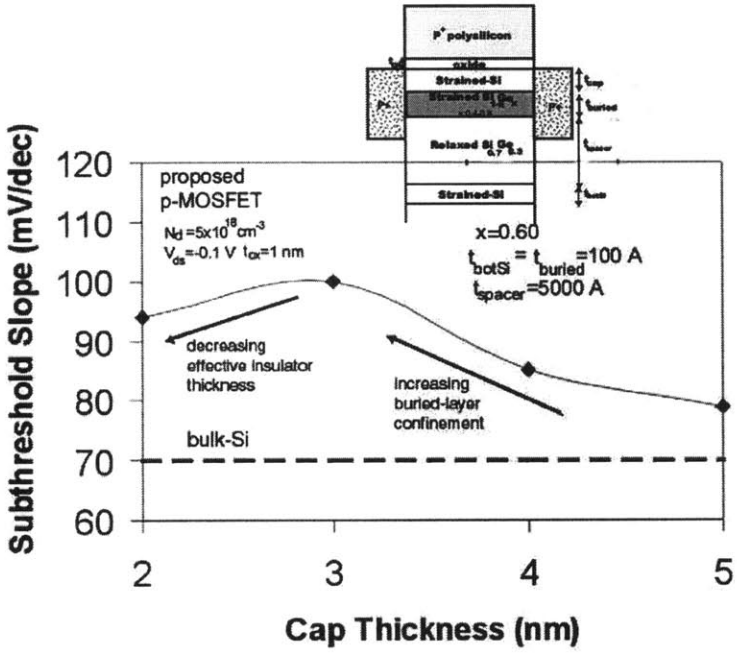

Fig. 4.12. Sub-threshold swing (SS) of the proposed p-MOS device plotted versus cap thickness, t_{cap}. The SS peaks for t_{cap}=3 nm and then decreases. The initial increase is attributed to increased confinement in the buried well resulting in an increased effective gate insulator thickness. The decrease of SS for t_{cap}< 3 nm is a result of increased carrier confinement in the buried well resulting in reduced gate insulator thickness with decreased t_{cap}.

gate insulator thickness with decreased t_{cap}. The computer simulation results show that the

performance enhancement and power dissipation of the design are very sensitive to t_{cap} and therefore the processing steps used since t_{cap} is affected by the surface cleaning and gate oxidation, a disadvantage in terms of manufacturing, and motivation for the study of direct-deposition of gate insulators on $Si_{1-x}Ge_x$.

4.5. Scaling to sub-50 nm Gate Length

After determining an optimum CMOS structure, the potential of the structure in extending conventional bulk-Si CMOS was investigated by studying the short-channel behavior for device parameters suitable for L_{eff}=25 nm as studied earlier, with x=0.60, y=0.30, and t_{cap}=2

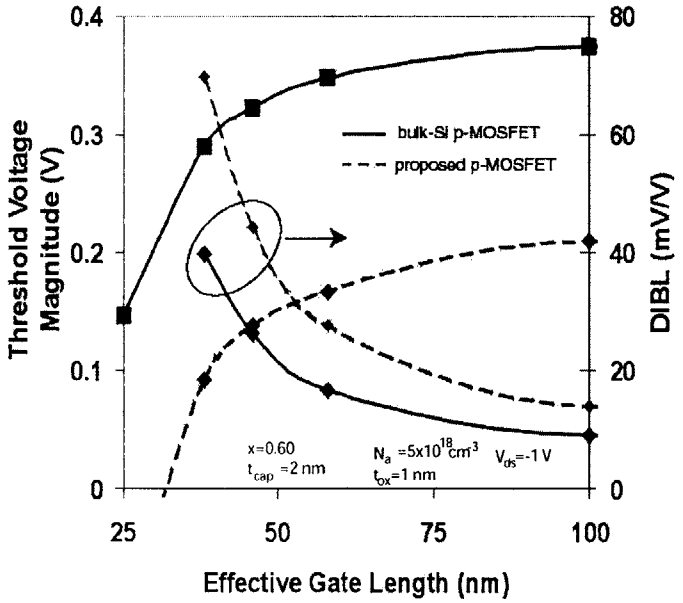

Fig. 4.13. Scaling behavior of the p-MOSFET proposed structure versus bulk-Si reference. It shows worse short-channel effects (larger DIBL, and larger V_t rolloff) due to the channel layer being buried from the gate insulator interface.

nm. The key parameters studied are the threshold voltage and drain induced barrier lowering (DIBL) dependence upon gate length. The p-MOS device was studied versus gate length, and as expected demonstrates increased DIBL and accelerated threshold voltage rolloff as shown in Fig. 4.14. This is the case since the carriers in sub-threshold where DIBL and V_t are measured, are effectively buried for the $Si_{1-x}Ge_x$ layer resulting in an increased gate insulator thickness. To reduce the short-channel effects, a smaller t_{cap} is required, or elimination of the cap and direct deposition of a high-K oxide on $Si_{1-x}Ge_x$. Another method is to increase the channel doping concentration. In addition to increased short-channel effects, the threshold voltage is also lower for all gate lengths necessitating alternative gate material with work function ~200 mV less than p^+ polysilicon. As a result, two different workfunction materials are required perhaps using a metal gate such as $Ti_{1-y}N_y$ with varying N composition [68]. Despite the increased short-channel effects, methods exist to reduce them and, furthermore, the increase is not too large and might be tolerable depending upon the power requirements of the design.

4.6. Conclusions

Analysis of the electrostatics of possible strained Si/SiGe CMOS designs has led to the discovery of an optimum design in terms of electrostatics and transport increase capability. The electron channel is tensile strained-Si grown on relaxed $Si_{1-y}Ge_y$ virtual substrate and a high Ge content $Si_{1-x}Ge_x$ ($x>y$) under compressive strain is used for the hole channel. Computer simulations demonstrate that the proposed design has the ability for extending conventional bulk-Si CMOS scaling into the sub-50-nm gate length regime.

Chapter 5

Conclusion

5.1. Summary of Results

This work has demonstrated that nanoscale strained Si n-MOSFETs are promising candidates for improving the transport properties of conventional bulk Si devices. This was shown by computer simulations, where transport models were calibrated based on experimental data. The electrostatics of strained Si nanoscale MOSFETs were analyzed and it was shown that there is no benefit in terms of short-channel effects in using strained Si. However, it was shown that the off-current is larger and a scaling methodology was presented that results in significant on-current enhancement at equivalent off-current. Experimentally, the Coulomb scattering limited mobility was found to not be enhanced over unstrained Si devices. It was shown that the loss of enhancement results in a less than 10% reduction in on-current for devices scaled to gate lengths as small as 20 nm. However, it was also shown that for sub-20-nm devices, the loss of enhancement is greater than 10%, which is significant given that Moore's law of scaling requires a 20% increase in Ion for a new scaling generation. As a result, the study of alternative substrates is required. One promising substrate is a fully-depleted ultra-thin body strained Si substrate. Such a device does not require doping to control short-channel effects, eliminating Coulomb

scattering effects. In the next section future work will be discussed that will help in attaining this substrate.

5.2. Suggestions for future work: Fabrication of nanoscale strained Si n-MOSFETs

Before discussing the fully-depleted strained Si substrate, more questions need to be answered in order to understand the fundamental device physics of strained Si devices. The results in this thesis should be verified experimentally by fabrication of strained Si n-MOSFETs with varying lengths reaching nanoscale. In specific, the threshold voltage shift with unstrained Si devices should be measured, and characterized as a function of gate length, and channel doping and compared to the analytical equations discussed in this work. Moreover, channel doping splits should be performed, to find a doping condition that results in maximum performance benefits. Comparing the performance benefits of strained Si devices with advanced 2D halo channel doping profiles to uniform doping devices can clarify the issue. This can be done by comparing the on-current, I_{on} at the same I_{off} for high V_{ds}. Since it was shown that Coulomb scattering results in reduced performance benefits, high performance strained Si devices should be fabricated such that the processing steps avoid high temperature steps, in order to avoid dopant diffusion to the channel area.

5.3. Suggestions for future work: Ultra-thin body strained Si MOSFETs

As explained in section 5.1, an ultra-thin body strained Si device would result in not only improved performance, but also, improved electrostatics, measured in terms of short-channel effects. An illustration of such a substrate is shown below in Fig. 5.1. The source/drain regions are comprised of $Si_{1-x}Ge_x$ and act as a virtual substrate for the ultra-thin body silicon film so that

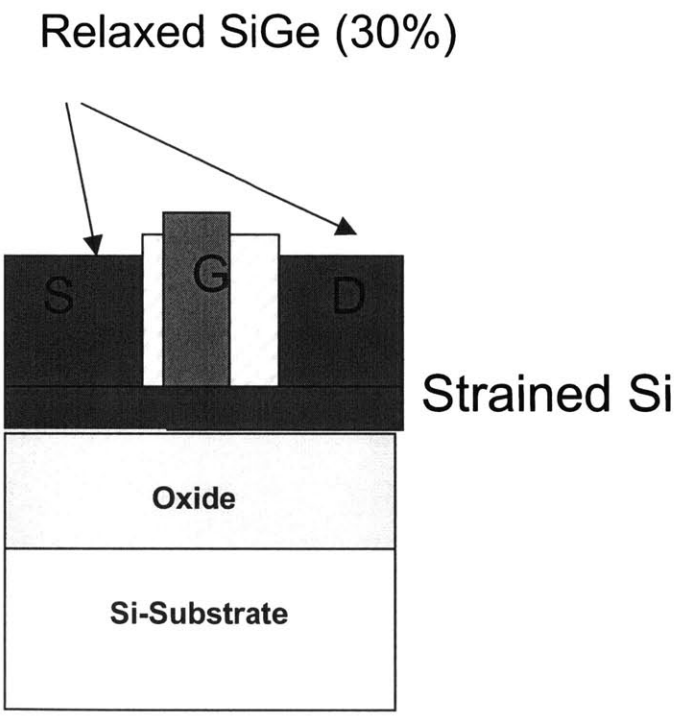

Fig. 5.1. Ultra-thin body strained Si substrate. The ultra thin body strained Si film has a thickness of 1/3 the gate length. The gate length, for the device will be sub-20-nm. The silicon film is lattice matched with the source/drain regions, which are comprised of Si1-xGex material, resulting in the film being under biaxial tensile stress.

the film is under biaxial tensile strain. The thickness of the film should be 1/3 the gate length. For a sub-20-nm gate length device, the film thickness required is less than 7 nm. It has been observed experimentally that electron transport in films with thickness less than 4 nm is degraded due to scattering at the back Si/SiO_2 interface [69]. Computer simulations, showing the electron concentration computed using a 1D self-consistent Poisson-Schrodinger computer simulation, show that the wavefunction is 1 nm from the top Si/SiO_2 interface (see Fig. 5.2).

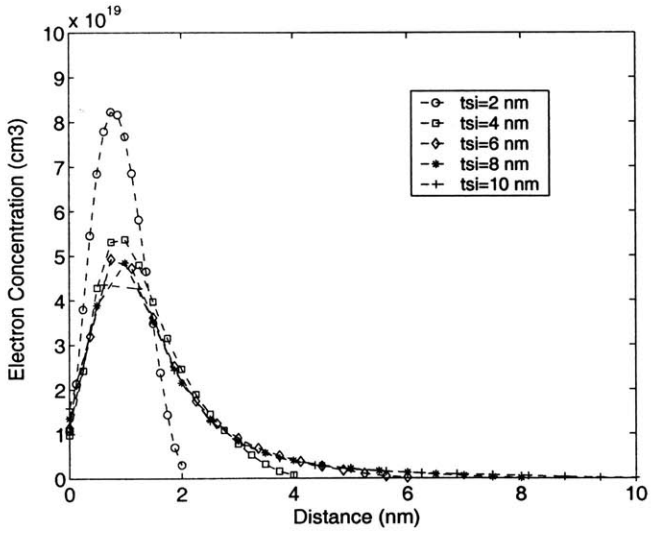

Fig. 5.2. Electron concentration versus depth from the top Si/SiO_2 interface for ultra-thin body strained Si MOSFET devices. The electron concentration is plotted for varying film thickness devices. The peak of the electron concentration is 1 nm from the interface. Clearly for film thickness approaching 1 nm, scattering at the back Si/SiO_2 interface becomes important, and results in degraded transport characteristics [69].

Clearly, transport models for ultra-thin body strained Si material are required in order to analyze the benefit of such a device over ultra-thin body unstrained Si. Future work should involve the fabrication of such a substrate, and measurement of the transport characteristics, so that transport models can be constructed to study extremely short-channel devices, sub-20-nm gate length.

References

[1] G. E. Moore, "Cramming More Components, Onto Integrated Circuits", *Electronics,* Vol. 38, No. 8, April 1965.

[2] 2002 *International Technology Roadmap For Semiconductors, ITRS.*

[3] C. S. Smith, "Piezoresistance Effect in Germanium and Silicon", *Physical Review*, Vol. 94, No. 1, pp. 42-49, 1954.

[4] J. Bardeen, W. Schockley, "Deformation Potentials and Mobilities in Non-Polar Crystals", *Physical Review* Vol. 80, No. 1, October 1950, p. 72-80.

[5] E. A. Fitzgerald, Y. –H. Xie, D. Monroe, P. J. Silverman, J. M. Kuo, A. R. Kortan, F. A. Thiel, B. E. Weir, "Relaxed Ge_xSi_{1-x} structures for III-V Integration with Si and high mobility two-dimensional electron gases in Si", *Journal of Vacuum Science Technology B,* Vol. 10, No. 4, pp. 1807-1819, July 1992.

[6] E. A. Fitzgerald, *Annu. Rev. Mater. Sci.* pp. 417-454 1994.

[7] J. W. Matthews and A. E. Blakeslee, "Defects in Epitaxial Multilayers. I. Misfit Dislocation", *Journal of Crystal Growth*, Vol. 27, pp. 118-125, 1974.

[8] M. V. Fischetti, S. E. Laux, "Band structure, deformational potentials, and carrier mobility in strained Si, Ge, and SiGe alloys", *Journal of Applied Physics,* Vol. 80, No. 4, August 1996, p. 2234-2251.

[9] J. Welser, J. L. Hoyt, J. F. Gibbons, "Electron Mobility Enhancement in Strained-Si n-Type Metal-Oxide-Semiconductor Field-Effect Transistors", *IEEE Electron Device Letters*, Vol. 15, No. 3, p. 100-102. March 1994.

[10] M. S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET, *IEEE Electron Device Letters*, Vol. 22, No. 6, pp. 293-295, June 2001.

[11] A. Lochtefeld, D. A. Antoniadis, "On experimental Determination of Carrier Velocity in Deeply Scaled NMOS: How Close to the Thermal Limit?" *IEEE Electron Device Letters*, Vol. 22, No. 2, February 2001.

[12] K. Rim, J. Chu, H. Chen, K. A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, H.-S. Wong, "Characteristics and Device Design of sub-100-nm strained Si n- and pMOSFETs,", *2002 VLSI Symposium.*

[13] Y. Taur, C. H. Wann, D. J. Frank, "25 nm CMOS Design Considerations", *1998 IEEE Electron Devices Meeting,* pp. 789-792.

[14] S. Takagi, A. Toriumi, M. Iwase, H. Tango, "On the Universality of the Inversion Layer Mobility in Si MOSFETs: Part I: Effects of Substrate Impurity Concentration" *IEEE Transactions on Electron Devices,* Vol. 41, No. 12, Dec. 1994.

[15] M. V. Fischetti, S. E. Laux, "Long-range Coulomb interactions in small Si devices. Part I: Performance and Reliability", *Journal of Applied Physics*, Vol. 89, No. 2, Jan 2001.

[16] T. Manku, A. Nathan, "Electron Drift Mobility Model for Devices Based on Unstrained and Coherently Strained $Si_{1-x}Ge_x$ Grown on <001> Silicon Substrate", *IEEE Transactions on Electron Devices* Vol. 39, No. 9, pp. 2082-2089 1992.

[17] C. G. Sodini, T. W. Ekstedt, J. L. Moll, "Charge accumulation and mobility in thin dielectric MOS transistors" *Solid-State Electronics*, Vol. 25, No. 9, 1982, pp. 833.

[18] I. J. Djomehri, D. A. Antoniadis, "Inverse Modeling of sub-100 nm MOSFETs using I-V and C-V", *IEEE Transactions on Electron Devices,* Vol. 49, No. 4, pp. April 2000.

[19] S. Takagi, A. Toriumi, M. Iwase, H. Tango, "On the Universality of the Inversion Layer Mobility in Si MOSFETs: Part I: Effects of Substrate Impurity Concentration" *IEEE Transactions on Electron Devices,* Vol. 41, No. 12, Dec. 1994.

[20] F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva, P. Cartujo, "Coulomb scattering in strained-silicon inversion layers on $Si_{1-x}Ge_x$ substrates", *Applied Physics Letters,* Vol. 69, No. 6, Aug. 1996.

[21] K. Rim, J. L. Hoyt, J. F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si n-MOSFETs, *IEEE Transactions on Electron Devices,* Vol. 47, No. 7, July 2000.

[22] J. Welser, J. L. Hoyt, J. F. Gibbons, "Electron Mobility Enhancement in Strained-Si n-

Type Metal-Oxide-Semiconductor Field-Effect Transistors", *IEEE Electron Device Letters*, Vol. 15, No. 3, p. 100-102. March 1994.

[23] A. Mujtaba, S. Takagi, R. Dutton, "Accurate Modeling of Coulombic Scattering, and its Impact on Scaled MOSFETs," *1995 Symposium on VLSI Technology.*

[24] M-S Liang, J. Y. Choi, P-K. Ko, C. Hu, "Inversion-Layer Capacitance and Mobility of Very Thin Gate-Oxide MOSFET's, *IEEE Electron Device Letters,* Vol. 33, No. 3, March 1986 pp. 409-413.

[25] Rutherford, "Scattering of the α and β particles by matter and structure of the atom" *Philosophical Magazine*, May 1911.

[26] M. Lundstrom, "Fundamentals of Carrier Transport", *Vol. X Modular Series on Solid State Devices,* 1990.

[27] F. Stern, W. E. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit", *Physical Review*, Vol. 163, 1967, p. 816.

[28] Th. Vogelsang, K. R. Hofmann, "Electron transport in strained Si layers on $Si_{1-x}Ge_x$ substrates", *Applied Physics Letters* Vol. 63, No. 2, July 1993.

[29] S. Takagi, J. L. Hoyt, J. J. Welser, J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors" *Journal of Applied Physics,* 1996; 80(3): p. 1567-77

[30] A. Lochtefeld, D. A. Antoniadis, "Investigating the relationship between electron mobility and velocity in deeply scaled NMOS via mechanical stress, *IEEE Electron Device Letters,* Vol. 22, No. 12, December 2001, p. 591-593.

[31] H. M. Nayfeh, C. W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, D. A. Antoniadis, "Influence of High Channel Doping on the Inversion Layer Electron Mobility in Strained Si n-MOSFETs", *IEEE Electron Device Letters*, April 2003

[32] F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva, P. Cartujo, "Coulomb Scattering In Strained-Silicon Inversion Layers on $Si_{1-x}Ge_x$ Substrates", *Applied Physics Letters*, Vol. 69, No. 6, Aug. 1996, p. 797-799.

[33] K. Rim, J. L. Hoyt, J. F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si *n*-MOSFETs", *IEEE Transactions on Electron Devices,* Vol. 47, No. 7, July 2000, p. 1406-1415.

[34] P. D. Agnello, "Process Requirements for continued scaling of CMOS- the need and prospects for atomic-level manipulation", *IBM Journal of Research and Development,* Vol. 46, No. 2/3, March/May 2002, p. 317-336.

[35] C. Lombardi, S. Manzini, A. Saporito, M. Vanzi, "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices", *IEEE Transactions On Computer-Aided Design,* Vol.7, No.11, November 1988, p.1164-1171.

[36] MEDICI, Version 1999.4.0, AVANT! Corp.

[37] A. Mujtaba, S. Takagi, R. Dutton, "Accurate Modeling of Coulombic Scattering, and its Impact on Scaled MOSFETs," *1995 Symposium on VLSI Technology,* p. 99-100

[38] Th. Vogelsang, K. R. Hofmann, "Electron Transport In Strained Si Layers on $Si_{1-x}Ge_x$ Substrates", *Applied Physics Letters* Vol. 63, No. 2, July 1993, p. 186-188.

[39] D. Caughey, R. Thomas, *IEEE Proceedings*, Vol. 55, p. 2192, 1967.

[40] Z. Sui, I. P. Herman, "Effect of strain on phonons in Si, Ge, and Si/Ge heterostructures", *Physical Review B*, Vol. 48, No. 24, December 1993, p. 17938-17953.

[41] P. F. Bagwell, D. A. Antoniadis, T. P. Orlando, "Quantum Mechanical and nonstationary Transport Phenomena in Nanostructured Silicon Inversion Layers", *VLSI Electronics Microstructure Science,* Vol. 18, 1989, p. 346-355.

[42] M. S. Lundstrom, "Elementary Scattering Theory of the Si MOSFET", *IEEE Electron Device Letters*, Vol. 18, No. 7, July1997, p. 361-363.

[43] R. Braunstein, A. Moore, F. Herman, "Intrinsic Optical Absorption in Germanium-Silicon Alloys", *Physical Review*, Vol. 109, No. 3, February 1958, p. 695-710.

[44] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained-layer heterostructures", *IEEE Journal of Quantum Electronics,* QE-22, Vol. 9, 1986, p. 1696.

[45] C. G. Van de Walle, R. M. Martin, "Theoretical Calculations of heterojunction discontinuities in the Si/Ge system", *Phys. Rev. B,* Vol. 34, No. 8, 1986, p. 5621.

[46] L. D. Yau, "A simple theory to predict the threshold voltage of short-channel IGFETs", *Solid-State Electronics,* Vol. 17, p. 1059.

[47] D. J. Frank, Y. Taur, H-S P. Wong, "Generalized Scale Length For Two-Dimensional Effects in MOSFET's, *IEEE Electron Device Letters*, Vol. 19, No. 10, Oct. 1998, p. 385-387.

[48] K. Ismail, S. F. Nelson, J. O. Chu, B. S. Meyerson, "Electron Transport Properties of Si/SiGe heterostuctures: Measurements and device implications", *Applied Physics Letters*, Vol. 63, No. 5, pp. 660-662, August 1993.

[49] K. Ismail, J. O. Chu, B. S. Meyerson, "High Hole Mobility in SiGe Alloys for Device Applications", *Applied Physics Letters*, Vol. 64, No. 23, pp. 3124-3126, June 1994.

[50] K. Rim, J. L. Hoyt, J. F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si *n*-MOSFETs, *IEEE Transactions on Electron Devices,* Vol. 47, No. 7, July 2000.

[51] J. Welser, J. L. Hoyt, J. F. Gibbons, "Electron Mobility Enhancement in Strained-Si n-Type Metal-Oxide-Semiconductor Field-Effect Transistors", *IEEE Electron Device Letters*, Vol. 15, No. 3, p. 100-102. March 1994.

[52] A. Sadek, K. Ismail, M. A. Armstrong, D. A. Antoniadis, F. Stern "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors", *IEEE Transactions on Electron Devices*, Vol. 43, No. 8, pp. 1224-1232, August 1996.

[53] C. W. Leitz, M. T. Currie, M. L. Lee, Z. –Y. Cheng, D. A. Antoniadis, E. A. Fitzgerald, "Hole Mobility Enhancement in strained $Si/Si_{1-y}Ge_y$ p-type Metal-Oxide-Semiconductor-Field-Effect Transistors Grown on Relaxed $Si_{1-x}Ge_x$ ($x<y$) Virtual Substrate" *Applied Physics Letters,* Vol. 79, 4246, 2001.

[54] S. Takagi, J. L. Hoyt, J. J. Welser, J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors" *Journal of Applied Physics,* 1996; 80(3): 1567-77

[55] J. M. Hinckley, J. Singh, "Hole Transport Theory In Pseudomorphic $Si_{1-x}Ge_x$ Alloys Grown On Si(001) Substrates", *Physical Review B*, Vol. 41, No. 5, Feb. 1990, pp. 2912-2926

[56] S. S. Iyer, P. M. Solomon, V. P. Kesan, A. A. Bright, J. L. Freeouf, T. N. Nguyen, A. C. Warren, "A Gate-Quality Dielectric System For SiGe Metal-Oxide-Semiconductor Devices", *IEEE Electron Device Letters*, Vol. 12, NO. 5, May 1991, pp. 246-248.

[57] J. W. Matthews and A. E. Blakeslee, "Defects in Epitaxial Multilayers. I. Misfit Dislocation", *Journal of Crystal Growth*, Vol. 27, pp. 118-125, 1974.

[58] E. A. Fitzgerald, *Annu. Rev. Mater. Sci.* 1994: 417-54.

[59] MEDICI, Version 1999.4.0, AVANT! Corp.

[60] C. G. Van de Walle, R. M. Martin, "Theoretical Calculations of Heterojunction Discontinuities in the Si/Ge System", *Physical Review B,* Vol. 34, No. 8, pp. 5621-5634, October 1986.

[61] Z-Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, D. A. Antoniadis, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates" *IEEE Electron Device Letters,* July 2001; 22(7): 321

[62] S. V-Vandebroek, E. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. Stork, J. B. Johnson, "SiGe-Channel Heterojunction *p*-MOSFET's", *IEEE Transactions on Electron Devices*, Vol. 41, No. 1, January 1994.

[63] K. Rim, J. Welser, J. L. Hoyt, J. F. Gibbons, "Enhanced Hole Mobilities in Surface-Channel Strained-Si p-MOSFETs, *IEEE Electron Devices Meeting,* 1995.

[64] DESSIS, Version 7.5.5 ISE, Integrated Systems Engineering, Zurich, Switzerland

[65] A. Wettstein, A. Schenk, W. Fichtner, "Quantum Device-Simulation with the Density-Gradient Model on Unstructured Grids", *IEEE Transactions on Electron Devices*, Vol. 48, No. 2, February 2001.

[66] T. Manku, A. Nathan, "Effective Mass for Strained p-type $Si_{1-x}Ge_x$", *Journal of Applied Physics,* Vol. 69, No. 12, June 1991.

[67] Th. Vogelsang, K. R. Hofmann, "Electron transport in strained Si layers on $Si_{1-x}Ge_x$ substrates, *Applied Physics Letters* Vol. 63, No. 2, July 1993.

[68] H. Wakabayashi, Y. Saito, K. Takeuchi, T. Mogami, T. Kunio, "A dual-metal gate CMOS Technology Using Nitrogen-Concentration-Controlled TiN_x Film" *IEEE Transactions on Electron Devices,* Vol. 48, No. 10, Oct. 2001, pp. 2363-2369.

[69] T. Mizuno, N. Sugiyama, T. Tezuka, T. Numata, T. Maeda, S. Takagi, "Design for Scaled Thin film strained-SOI CMOS devices with Higher Carrier Mobility, *2002 IEEE Electron Devices Meeting*, p. 31.

[70] K. Rim, J. L. Hoyt, J. F. Gibbons, "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's, *IEEE Transactions on Electron Devices*, Vol. 47, No. 7, July 2000.

[71] P.D.Agnello, V.P. Kesan, M. Tejwani, J. A. Ott, "Titanium Silicide/Geraminide Formation on Submicron Features for High Mobility SiGe Channel Field Effect Transistors", *Journal of Electronic Materials*, Vol. 23, No. 4, 1994, p. 413-421.

[72] K. Rim, PhD Thesis Stanford University, 1999.

[73] D.B. Aldrich, Y. L. Chen, D. E. Sayers, and R. J. Remanich, S. P. Ashburn, M. C. Ozturk, "Stability of C54 titanium germanosilicide on a silicon-germanium alloy substrate", *Journal of Applied Physics*, Vol. 77, No. 10, May 1995, p. 5107-5114

[74] Z. Wang, D. B. Aldrich, Y. L. Chen, D. E. Sayers, R. J. Nemanich, "Silicide formation and stability of Ti/SiGe and Co/SiGe", *Thin Solid Films*, Vol. 270, 1995, p. 555-560.

[75] J. B. Lai, L. J. Chen, "Effects of composition on the formation temperatures and electrical resitivities of C54 titanium germanosilicide in $TiSi_{1-x}Ge_x$ systems, *Journal of Applied Physics*, Vol. 86, No. 3, p. 1340-1345.

[76] S. Zaima, Y. Yasuda, "Study of reaction and electrical properties at Ti/SiGe/Si (100) contacts for ultralarge scale integrated applications", J. Vac. Sci. Technol. B, Vol. 16, No. 5, Sep/Oct. 1998, p. 2623-2628.

[77] E. A. Fitzgerald, Y.-H. Xie, P. J. Silverman, A. R. Kortan, B. E. Wier, L.C. Feldman, "Relaxed Ge_xSi_{1-x} Structures for III-V Integration with Si and High Mobility Two Dimensional Gases in Si", *Journal of Vacuum Science Technology B,*. Vol. 10, No. 4, 1992, p. 1807

[78] L . J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape", *Phil. Res. Rep.* Vol. 13, Feb. 1958, p. 1-9.

[79] K. Maex, "Silicides for Integrated Circuits: $TiSi_2$ and $CoSi_2$", *Materials Science and Engineering*, R11, Nos. 2-3, Nov. 1, 1993, p. 53-103.

\

[80] Y. Taur, T. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

[81] S. Ashburn, D. T. Grider, M. Ozturk, G. Harris, D. M. Maher, "Self-Aligned Formation of C54 Titanium Germanosilicide using rapid thermal processing and application to raised, ultra-shallow junctions", *Mat. Res. Soc. Symp*, Vol. 320,1994, p. 311-316.

[82] P. Gas, G. Scilla, A. Michel, F. K. LeGoues, O. Thomas, F. M. d'Heurle, Journal of Applied Physics, Vol. 63, 5335, (1988)

Appendix A

Strained Si n-MOSFET Fabrication Process

Below is the process traveler for the fabrication of strained and unstrained Si devices in the MTL Integrated Circuits Laboratory, ICL. The text gives a detailed description of the daily fabrication work performed.

****

I. Zero Alignment:

****

A. Alignment Mark Formation
- I will etch 1-1.5um trenches and use those as alignment marks.

==========

MACHINE: ICL HMDS DATE: 01/29/2001 16:28:02 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/29/2001 16:28:02

End 01/29/2001 16:28:03

Comments:
20 wafers.

==========

MACHINE: ICL coater6 DATE: 01/29/2001 16:35:50 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/29/2001 16:35:57

End 01/29/2001 17:10:06

Comments:
20 wafers. I do a double coat so that I get approximately 2um of resist.

==========

MACHINE: ICL stepper2 DATE: 01/29/2001 17:13:58 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/29/2001 17:14:00

End 01/29/2001 19:25:48

Comments:
20 wafers. Used mask EBEAMCA. 0.5 seconds, focus=251.

==========

MACHINE: ICL developer DATE: 01/29/2001 19:26:57 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/29/2001 19:26:57

End 01/29/2001 19:26:58

Comments:
20 wafers.
==========
=
MACHINE: ICL AME5000 DATE: 01/30/2001 16:12:04 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/30/2001 15:49:53

End 01/30/2001 16:12:06

Comments:
19 wafers. Using recipe undoped poly (Cl2, HBr, NF3).
Etch rate of silicon is ~7
3A/sec. I want to etch 1 um so put in for 137 seconds.
==========
=
MACHINE: ICL asher DATE: 01/30/2001 17:33:22 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/30/2001 17:33:27

End 01/30/2001 17:33:25

Comments:
19 wafers.
==========
MACHINE: ICL P10 DATE: 01/30/2001 17:58:00 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/30/2001 17:58:00

End 01/30/2001 17:58:00

Comments:
1 wafer. Measured step height. I get 1.5um.
Therefore, the etch rate is 110A/sec for undoped poly.
==========
==========

II. ISOLATION

A. Field Implant
==========
MACHINE: ICL HMDS DATE: 01/30/2001 17:57:13 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot ld_ipfoc: ld_ipfoc

Start 01/29/2001 18:19:23

End 01/30/2001 17:57:14

Comments:
19 wafers.
==========

MACHINE: ICL coater6 DATE: 01/30/2001 19:36:16 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/30/2001 19:36:25

End 01/30/2001 19:36:25

Comments:
19 wafers + 1 focus expo wafer.
==========
MACHINE: ICL stepper2 DATE: 01/31/2001 10:56:50 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/31/2001 08:44:35

End 01/31/2001 12:28:54

Comments:
19 wafers. Field Implant photolithography.
Used mask EBEAM CF. Used 0.240/232.
SIMS die: (8,2), (8,7), (1,2), (1,7).
Used TMASK CF for SIMS die.
==========
MACHINE: ICL developer DATE: 01/31/2001 15:43:40 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/31/2001 15:43:40

End 01/31/2001 15:43:40

Comments:
19 wafers.
==========
==========
MACHINE: ICL coater6 DATE: 01/31/2001 15:44:13 USER: hnayfeh

PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/31/2001 15:44:14

End 01/31/2001 15:44:15

Comments:
19 wafers. Hard bake at 130C for 1 min.
==========
=
The marks were misaligned by 1um in the x and 0.5um in the y.
The offsets are not correct. I have to tune the offset every time
I do a job. So, I'll
ash the wafers and redo. I also found resist in the corners,
so the exposure time is too short. I'll increase it to 0.26sec.
==========
=

MACHINE: ICL asher DATE: 01/31/2001 18:45:09 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/31/2001 18:45:10

End 01/31/2001 18:45:10

Comments:
19 wafers.
I had some trouble with the asher... the wafer would get stuck inside
the chamber. I think it is due to the wafer falling off the arm due
to bad contact.
==========
=
MACHINE: ICL HMDS DATE: 01/31/2001 18:46:24 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 01/31/2001 18:46:24

End 01/31/2001 18:46:24

Comments:
19 wafers.
==========
=
When using a new mask the offsets can be off by as much as 50um. Several
runs need to be done in order to fine tune them. The offset value
that is put in the job is the distance of the alignment mark
from the center of the lens.
This value will be shifted compared to the coordinates that are in
the mask design. The stepper looks at 2 die. The theta die is (6,1)
the x/y die is (6,8). It goes to these die and then uses the offset
to look for the mark on the wafer. This way, the stepper aligns
the level to the mark and the mark's coordinates are calibrated
to the center of the lens.
==========
==
MACHINE: ICL stepper2 DATE: 02/01/2001 14:28:24 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/01/2001 09:00:00

End 02/01/2001 14:46:16

Comments:
19 wafers. This is a rework. The correct offsets for job hasan ca are:
x=3.05040 and y=4.2071. The alignment was dead on for a wafer
that was used to tune the offset values.
==========
== MACHINE: ICL developer DATE: 02/01/2001 15:54:38 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/01/2001 15:54:40

End 02/01/2001 15:54:40

Comments:
19 wafers.
==========
==
MACHINE: ICL coater6 DATE: 02/01/2001 15:55:26 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/01/2001 15:55:27

End 02/01/2001 15:55:28

Comments:
19 wafers.
==========
=
Checked the alignment of the wafers. They are all "dead on".
So the field implant is aligned to the zero level. I will now
send out for implant at Wakefield. SGOI had the worst alignment.
It is 0.3um too left in the x.
That is fine for this experiment.
==========
=
Field Implant: Boron, 3e13/25keV, 7 degree tilt,
0 degree rotation. 19 wafers. Send to Implant Sciences.
The implant was chosen so that the concentration
is ~1e18cm^-3 uniform from the surface to ~500A away.
==========
=
The wafers are back from implant. I need to clean them in order
to proceed. I'll first do a blue p-clean to remove the resist
and then a green one to clean and I'll conclude with a 15 sec
50:1HF dip. The p-cleans will be abbreviated to 7 mins since
I have very thin films. I did an inspection of one of the wafer
after implant and there are no abnormalities. I inspected
the wafers after 30 seconds in the blue p-clean and the
resist was gone. I continued so that the end result is total
7 minutes.
==========
I'll now deposit 3200A of LTO using tube A7. To get into the tube
I'll do a modified thin film clean (7min p-clean, 15sec 50:1HF dip,

10min sc2 clean). I'm overshooting the thickness from 3000A because
I want to make sure that I have at least 3000A. The rate used yesterday
was 126.3 A/min. So, the time is 25min and 19 seconds. I am running
6 etch dummies also, so I have a full boat.
==========
MACHINE: ICL rca DATE: 02/08/2001 17:05:52 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/08/2001 17:05:52

End 02/08/2001 17:05:53

Comments:
25 wafers.
==========
The SC2 bath was at 80C during the clean.
==========
MACHINE: ICL tubeA7 DATE: 02/09/2001 13:12:57 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/09/2001 07:44:43

End 02/09/2001 13:12:58
Comments:
25 wafers. TT=3200A. time: 25 mins 19 secs. Used middle boat.
All values are averaged over the wafer. Used rec462. Most in: 3350A.
Most out: 2848. On wafer non-uniformity: Most in: 3501-2981 angstroms.
Most out: 2935-2781 ang.
==========
==
My LTO thickness ranges from 3501-2781A. The non-uniformity on wafer
becomes better as the wafers move out. I found that the wafers that
are pointing out are thicker than the ones pointing by 100-200A. All the
details are in my clean lab book.
==========
==
Today, I am doing the photolithography for the field oxide etch.
I open up windows at the active areas so that oxide will
be etched there. The mask I will use is ebeamCD. It is a dark
field mask. The SIMS blocks will be shot using the mask already in
the stepper (all clear) since I don't want any oxide to be there.
==========
=
MACHINE: ICL HMDS DATE: 02/12/2001 10:15:15 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/12/2001 10:24:32

End 02/12/2001 10:24:33

Comments:
25 wafers.
==========
=
MACHINE: ICL coater6 DATE: 02/12/2001 10:35:57 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/12/2001 10:35:58

End 02/12/2001 10:36:00

Comments:
25 wafers.
==========
I'll now do a photo expo to determine the optimum exposure time

and focus. The range for exposure time is: 0.12-0.26. The focus is
from 250-228. Best exposure/expo: 0.24/232
==========
After the photo expo, I'll fine tune the key offsets.
The offsets work just fine- I'll shoot all the wafers.
==========
MACHINE: ICL stepper2 DATE: 02/12/2001 18:03:05 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/12/2001 18:03:06

End 02/12/2001 18:03:06

Comments:
25 wafers.
==========
5 of the wafers had misalignment of > 0.6. The rest of the wafers have
misalignment < 0.2 at worse. I'll redo the 5. The camera was not
working properly. The picture has lots of noise. That made the
alignment much more difficult than usual and was the result of the severe
misalignment of the 5 wafers.
==========
Today I am starting the process of etching the field oxide
from the active areas. To do this, I am checking if this can
be done by wet etch in 50:1 D.I:HF. I found the etch rate in
the HF to be 438A/min for undensified LTO. I measured dummy wafer
MP001 using nanospec. I got: TBLCR: (2913, 3067, 3062, 3071, 3000).
I aimed to etch with 20% over etch. So the time is 1.2*3071=3685A/438=
8 mins and 25 secs. I did this and after the D.I. rinse, I saw
dewetting inside the scribe lines indicating the LTO was completely
etched away. I then ashed the wafer and I'll look at it in the SEM
tomorrow morning with P. Tierney.
==========
**A quick note regarding field oxide thickness:
The oxide required to make vth above 10V is 750-1000A.
During the process, 1250A are
etched away due to 50:1 HF cleans. This is a pessimistic calculation
since I am assuming the LTO will not be densified after the
reox step. So, an oxide thickness of 2000-2250A is necessary to have
an effective isolation. My thinnest oxide is 2750A so I am in the safe
zone with some flexibility in case I have to do an extra clean for
some reason or wet etch of titanium.
==========
I tried imaging the wafer etched with 50:1 HF with the ICL SEM. I could
see the features but the edge looked very blury, so I would not
be able to decipher the angle. I then sputtered some Pt on the sample
since I suspected that charging was causing the image to be poor.
However, this made it more difficult to image. I lost all contrast.

I then sputtered ~200A of Al using the endura and I got the same problem.
The conclusion: I will have to use the ZEISS at the NSL. I'll look at
a cross section. To give better contrast, I'll dip in HF so that ~400A
of LTO will be etched (~1 min in 50:1). That will help the image look
more crisp.
==========
I measured dummy wafer L061 using the nanospec in the trl since the camera
for the UV1280 is still broken. I get TBLCR: (3084, 3220, 3008, 3202, 3154)
==========
I created a recipe called HASANFOX. It is modified from Isabella LTO.
I add a O2 gas to the etch step. I will try three different O2 flow rates:
5 sccm, 10 sccm, and 15 sccm and look at the angle.
I tried using 10 sccm O2 but the resist was all etched away
and I attacked the field oxide underneath.
The selectivity is 8:1 resist: LTO. That is way too high. I need
to back off on the O2. However, I need to get a decent angle.
So, I'll reflow the resist at 150C for 1 min. That gives an angle to start
with and I'll reduce the O2 flow rate to 5 sccm for
main etch.
==========
=
MACHINE: ICL AME5000 DATE: 02/21/2001 16:49:06 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/20/2001 14:00:00

End 02/20/2001 18:00:00

Comments:
3 wafers. Calibrating recipe HASANFOX.
==========
HASANFOX:
step1:stabilize 20sec, O2 20sccm, 200mTorr, 0 Watts
step2:descum 20sec, O2 20sccm, 200mTorr, 100Watts, 50Gauss, -1000V
step3:stabilize 25sec, CF4 15sccm, CHF3 10sccm, O2 5sccm, 200mTorr, 0 Watts
step4:etch CF4 15 sccm, CHF3 10 sccm, O2 5 sccm, 200mTorr, 350Watts, 50
Gauss.

Etch rate of LTO undensified: y=20*(t-6.8)
Etch rate of positive resist: y=28.7*(t+43.5)

To etch 2500A of LTO, 0.48um of resist are etched away. Therefore,
the resist will hold up to the etch.
==========
I prepared 3 samples to look at in the SEM:
1) MT060 8 mins in 50:1 HF
2) T061 Resist reflow+ HASANFOX
3) P149 HASANFOX

To image I need to do sample preparation. I will deposit ~1000A of
polysilicon. After that, I'll cleave a piece from the wafer and then
etch ~400A of LTO (~1 minute in 50:1 HF). I'll look at the sample
in the Zeiss in the NSL. D. Carter will continue my training at 9:00 a.m.
==========
MACHINE: ICL tubeA6 DATE: 02/21/2001 17:00:39 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/21/2001 13:00:00

End 02/21/2001 17:00:41

Comments:
4 wafers. Rec461. TT=1000A. Time: 19.34 minutes. Measured thickness: ~1100A.
==========
=
I tried imaging the samples. There are 2 problems. First of all,
there are not enough features making it almost impossible to
find anything. I'll correct this by using mask EBEAM CM. It has
SEM lines. Also, there is too much overhang of the poly indicating
that the oxide etch done to delineate the layers was too long.
J. Carter indicated that he does not think it is necessary to
do the HF dip. So, I'll repeat the experiment.
==========
=
MACHINE: ICL AME5000 DATE: 02/23/2001 09:25:42 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/22/2001 18:00:00

End 02/23/2001 20:00:00

Comments:
2 wafers. Used rec. HASANFOX. Got for etch rate: y=19.65*(t-1.12) of LTO.
==========
=
MACHINE: ICL pre-metal DATE: 02/23/2001 09:28:01 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/22/2001 17:44:00

End 02/23/2001 18:00:00

Comments:
3 wafers. 50:1 HF to complete LTO etch. Aimed to leave 500A of
LTO after RIE etch.
==========
==
MACHINE: ICL asher DATE: 02/23/2001 09:29:33 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/23/2001 09:29:34

End 02/23/2001 09:29:34

Comments:
3 wafers. Removal of resist.
==========
=
I noticed on the optical microscope that after 2 minutes of
ashing there was still resist in some closed features and
at the scribe lines. I repeated the ash for 3 minutes to
remove any left over.
==========
=

MACHINE: ICL rca DATE: 02/23/2001 09:31:25 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot rajdeep-1: rajdeep-1

Start 02/23/2001 08:25:20

End 02/23/2001 09:31:33

Comments:
3 wafers.
==========
==
I notice that the wafer that was etched entirely by 50:1 HF
lost most of it's features. It appears that the resist lifted off
during the etch since I was severly undercutting the pattern.
I'll drop the wafer, M151 and continue with the other two.
==========
=
MACHINE: ICL tubeA6 DATE: 02/23/2001 15:29:15 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 02/23/2001 10:49:34

End 02/23/2001 15:29:15

Comments:
2 wafers. Rec461. TT=1000A.
Time: 19mins and 20 seconds. Got 880 angstroms average for the wafer.
==========
==
MACHINE: ICL tubeA7 DATE: 03/14/2001 09:22:50 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/02/2001 00:00:00

End 03/02/2001 00:00:00

Comments:
25 wafers. Did for 21 minutes. I got ~2700A. My wafers were all
located at the middle boat. The variation was very small.
This dep. was done after the installment of new quartz.
==========
=
I am repeating the field oxide step because the O2 was too high in the etch
and the resist was not holding up enough and I am worried that I have too
much
lateral etching of the resist.
==========
=
MACHINE: ICL HMDS DATE: 03/14/2001 09:35:13 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/07/2001 00:00:00

End 03/07/2001 00:00:00

Comments:
25 wafers.

```
================================================================================
=

MACHINE: ICL stepper2          DATE: 03/14/2001 09:37:45   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 03/07/2001 00:00:00

End   03/07/2001 00:00:00

Comments:
25 wafers.
================================================================================
=
I had to change the job offsets slightly to get good alignment. My worst
alignment in the x was 0.4um. The y alignment was dead on.
================================================================================
=
MACHINE: ICL developer         DATE: 03/14/2001 09:39:24   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 03/07/2001 00:00:00

End   03/07/2001 00:00:00

Comments:
25 wafers.
================================================================================
=
I then etched 4 dummy wafers that I'll use to SEM. I used HASANCM pattern
since it has SEM lines. I calibrated HASANFOX. I got an etch rate:
y=30.60*(t-4.5). I made splits on the O2 flow rate SCCM, 1, 2, 3, and 4.
I found that the selectivity of resist etch rate: LTO etch rate is for
1,2,3,and 4
respectively are: 1.4:1, 2.1:1, 2.5:1, 2.8:1. I aimed to leave 300A
of LTO, but I got 500A. The etch rate changed overnight. I etched the
remaining using 50:1 HF. I measured the etch rate and it is 400A/min.
I dipped for 2 minutes. After imaging in the microscope, I noticed
resist debris. This shows that the resist is attacked during the HF dip and
it
peels off. Next time, I'll ash the resist and keep the remaining LTO
so that it can be used as a protection layer for the active area when
I go to implant my SSR I/I. The upper bound of selectivity is 4.3:1 so
that the resist will hold up to the etch.
================================================================================
=
MACHINE: ICL AME5000           DATE: 03/14/2001 09:40:21   USER: hnayfeh
NIL
Start 03/14/2001 09:28:36

End   03/14/2001 09:45:36

Comments:
25 wafers.
================================================================================
=
I will now deposit ~1000A of poly over the wafer to facilitate the SEM
```

imaging.
==========
=
MACHINE: ICL rca DATE: 03/14/2001 09:46:09 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot dgsr102: dgsr102

Start 03/14/2001 09:27:31

End 03/14/2001 09:46:44

Comments:
4 dgsr102, 3 implanted poly, 3 nitridestack#1, 4 monitor wafers, and 4
Hasan's wafers. Piranha in sc1 bath, 50:1 HF dip 15sec, and sc2.
==========
=
MACHINE: ICL tubeA6 DATE: 03/14/2001 15:35:34 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/14/2001 09:47:35

End 03/14/2001 15:35:37

Comments:
4 wafers. rec461 for 19 mins and 20 secs. TT=1000A.
Actual thickness obtained is
I used the middle boat. I got TBLCR: 811, 751, 806, 823, 756
==========
I will image tomorrow morning with Paul Tierney using the SEM at the NSL
that is for the MTL. Paul said to cleave a piece that is approximately
the size of a die- 10mm.
==========
I imaged with the SEM. The result is that the 1 SCCM O2 etch gave an
angle of 30-35 degrees. That's good for me. I'll use that. The selectivity
to resist is ~1:1 so I am fine.
==========
MACHINE: ICL AME5000 DATE: 03/15/2001 20:02:35 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/15/2001 18:00:00

End 03/15/2001 20:29:57

Comments:
16 wafers. Used HASANFOX got 24A/min for LTO.
==========
=
I got the following formula for the etch rate:
y=23.73*(t+2.32). The selectivity to resist is 1.6:1. That's good enough.
I aimed to leave 500A on the wafers, but I raised that to 700A for the
SiGe wafers to be more safe since I can't trust the ellipsometer measurement
completely although the dielectric constant is 7% different, 11.9 vs. 12.7.
I'll remove the resist and then etch the remainder in 50:1HF. I want to
remove the resist since I have fear it will be removed like last time.
This could be due to the resist getting weaker after the etch plus attack
by the 50:1. I can afford losing field oxide. My vth will be above 10V
as long as the oxide is above 1000A.

```
================================================================================
=
MACHINE: ICL asher              DATE: 03/16/2001 09:34:27   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sigefet1: sigefet1

Start 03/16/2001 09:34:28

End   03/16/2001 09:34:29

Comments:
16 wafers.
================================================================================
=
MACHINE: ICL pre-metal          DATE: 03/16/2001 11:03:35   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sigefet1: sigefet1

Start 03/16/2001 11:03:36

End   03/16/2001 11:03:36

Comments:
16 wafers.
================================================================================
=
I aimed to etch 1000A of LTO in order to clear up the active areas. That
leaves me with 1700-1500A of field oxide. That's plenty for the isolation.
================================================================================
Inspected wafers with microscope etch looks great!
================================================================================
I measured the field oxide. It ranges from 1500A to 1800A. I measured
the active area. I get 25A of oxide. This is just a native oxide. The
wafers dewetted in the etched areas indicating that the oxide was
completely removed.
================================================================================
**********
```

III. BODY IMPLANTS

```
**********

Today, I am blocking off the right side of all wafers so that I can
do the body implant. The plan is the following:

        Ns      Si          SiGe
=================================
1)      5e17    1e13        2e13
2)      1e18    2e13        3e13
3)      2e18    3e13        4e13
4)      3e18    4e13        5e13
5)      4e18    5e13        6e13
6)      5e18    6e13        7e13
7)      6e18    7e13        8e13

N: No I/I
doses: 1, 2, 3, 4, 6, 7

25A N2O:
1) 1,7
```

2) 2,6
3) 3,N
4) 4,6

65A N2O:
1) 1, N
2) 3, 6

65A O2:
1) 1, N
2) 3, 6

I created a pass under the hasan ca file. It's pass 3, so hasan ca, 3. It blocks the left side of the wafer.
I will do a large exposure 0.50 seconds, to ensure that the resist is removed from the left side. Therefore, the left side is getting the I/I.

==========

MACHINE: ICL HMDS DATE: 03/22/2001 12:23:03 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/22/2001 12:41:55

End 03/22/2001 12:41:55

Comments:
16 wafers.

==========

MACHINE: ICL coater6 DATE: 03/22/2001 12:44:16 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot 152JSum1: 152JSum1

Start 03/22/2001 10:33:57

End 03/22/2001 12:44:16

Comments:
16 wafers.

==========

LEFT side of wafer gets the first body I/I.

==========

MACHINE: ICL stepper2 DATE: 03/22/2001 12:44:51 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/22/2001 12:44:52

End 03/22/2001 13:36:30

Comments:
16 wafers.

==========

March 26, 2001: Send out wafers for first Body I/I to Wakefield.

All implants are Boron 10keV 7 TILT 0 ROTATION

LEFT SIDE RECIEVES THE IMPLANT

FRONT SCRIBE/BACK SCRIBE

SLOTS 1-3: 1e13
1)CEBD2241SI0.20B0E0/NOTHING
2)CEBD2245SI0.20B0F0/NOTHING
3)CEBD2244SI0.20B0E6/NOTHING

SLOTS 6-9: 2E13
6)CEBD2247SI0.20B0F4/NOTHING
7)CEBD2307SI0.20B0G1/312.3
8)CEBD2312SI0.20B0G7/312.2
9)CEBD2308SI0.20B0G3/312.4

SLOTS 12-15: 3E13
12)CEBD2348SI0.20BOH0/NOTHING
13)CEBD2243SI0.20B0E4/NOTHING
14)CEBD2242SI0.20B0E2/NOTHING
15)CEBD2152SI0.20B0F0/310.1

SLOTS 18-21: 4E13
16)CEBD2248SI0.20B0E6/NOTHING
17)CEBD2149SI0.20B0E6/309.2
18)CEBD2862SI0.20B0F6/312.6
19)CEBD2148SI0.20B0E4/309.3

SLOTS 24: 5E13
24)CEB2158SIO.20B0G4/309.4

==========

Today, 03/30/2001, I got the wafers back from implant. The left side was implanted. I will now strip and then clean the wafers so that I can coat the left side and implant the right side. I'll strip by doing a 10min p-clean in the blue and then I'll clean by doing a 5 min green p-clean. I'll finish up with a 5 sec 50:1 HF dip.

==========

MACHINE: ICL pre-metal DATE: 03/30/2001 16:18:28 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 03/30/2001 16:18:28

End 03/30/2001 16:18:28

Comments:
16 wafers.

==========

Inspected wafers by eye. The resist was gone after the blue p-clean. The bath turned to a yellowish color indicating resist has been stripped. After the green p-clean and HF dip and rinse, I could see dewetting in the active areas.

==========

Today, I'll block off the left side so that I can implant the right side. 6 wafers will not receive an additional implant. They were not included for this photo step. See lab book for exact wafers excluded.

==========

```
MACHINE: ICL HMDS              DATE: 04/02/2001 09:29:23   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 04/02/2001 10:33:27

End   04/02/2001 10:33:27

Comments:
10 wafers.
================================================================================
=  MACHINE: ICL coater6          DATE: 04/02/2001 17:37:09   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 04/02/2001 17:37:09

End   04/02/2001 17:37:09

Comments:
10 wafers.
================================================================================
=
  MACHINE: ICL stepper2         DATE: 04/02/2001 17:37:47   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 04/02/2001 17:37:47

End   04/02/2001 17:37:48

Comments:
10 wafers.
================================================================================
 MACHINE: ICL developer        DATE: 04/02/2001 18:09:18   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 04/02/2001 18:09:19

End   04/02/2001 18:09:19

Comments:
10 wafers.
================================================================================
=
   MACHINE: ICL coater6          DATE: 04/02/2001 18:35:14   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 04/02/2001 18:35:15

End   04/02/2001 18:35:15

Comments:
10 wafers. Hard bake.
================================================================================
Right side will receive the implant. I created a pass under hasan ca.
It's hasan ca, 4. It blocks off the left side of the wafer.
================================================================================
Send off wafers to Wakefield for I/I APRIL 3, 2001
Species: Boron, Energy: 10kev, tilt: 7, rotation 0
```

RIGHT SIDE RECEIVES IMPLANT

Wafer count: 10 wafers

Slots 1-3: 5e13
1)CEBD2247SI0.20B0F4/NOTHING (2E13/5E13)
2)CEBD2243SI0.20B0E4/NOTHING (3E13/5E13)
3)CEBD2242SI0.20B0E2/NOTHING (3E13/5E13)

Slots 7-10: 6e13
7)CEBD2152SI0.20B0F0/310.1 (3E13/6E13)
8)CEBD2248SI0.20B0F6/NOTHING (4E13/6E13)
9)CEBD2862SI0.20B0F6/312.6 (4E13/6E13)
10)CEBD2148SI0.20B0E4/309.3 (4E13/6E13)

Slots 13-14: 7e13
13)CEBD2241SIO.20B0E0/NOTHING (1E13/7E13)
14)CEBD2158SIO.20BOG4/309.4 (5E13/7E13)

Slot 17: 8e13
17)CEBD237SI0.20B0G1/312.3 (2E13/8E13)
==========
=
Today, I'm testing a recipe to grow ~45A of oxide. I'll try 800C for 25 minutes using Tube A1 rec. 144. I'll grow the oxide on 2 p-prime dummies 5-10 ohm*cm.
==========
MACHINE: ICL rca DATE: 04/03/2001 15:43:03 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/03/2001 16:02:06

End 04/03/2001 16:54:42

Comments:
2 wafers.
==========
MACHINE: ICL tubeA1 DATE: 04/03/2001 18:38:30 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/03/2001 16:55:17

End 04/03/2001 18:38:31

Comments:
2 wafers. rec. 144 for 25 minutes. 800C O2 oxidation.
I measure 43 angstroms on the ellipsometer.
==========
=
So, 800C for 25 minutes gives 43 angstroms of oxide. That's good enough for my thick oxide split. Tube A1 rec. 144
==========
=
****

IV. Gate Stack

****

```
================================================================================
=
MACHINE: ICL pre-metal          DATE: 04/09/2001 10:17:39   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sgsr201: sgsr201

Start 04/09/2001 09:58:54

End   04/09/2001 10:17:41

Comments:
10 wafers. Blue p-clean for resist removal,
Green p-clean, then 10 sec 50:1 HF dip.
================================================================================
==
MACHINE: ICL rca                DATE: 04/09/2001 10:20:42   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sigefet1: sigefet1

Start 04/09/2001 10:20:43

End   04/09/20010 10:20:43

Comments:
15 wafers. 10 min p-clean, d.i rinse, 15 sec 50:1 HF dip,
d.i. rinse, 15 min sc2 clean, d.i. rinse, spin dry.
================================================================================
==
I noticed that after the p-clean, the resistivity of the d.i. rinse
bath wash high. As a result, I performed 2 d.i. rinses.
================================================================================
==
MACHINE: ICL tubeA1             DATE: 04/09/2001 13:25:56   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sigefet1: sigefet1

Start 04/09/2001 10:23:27

End   04/09/2001 13:28:20

Comments:
16 wafers. Rec 144. 800C for 25 minutes in O2 ambient. TT=45 angstroms.
I measure 44-45 angstroms.
================================================================================
=
MACHINE: ICL tubeA6             DATE: 04/09/2001 16:41:47   USER: hnayfeh
PROCESS: NONE                   WAFERSETS: Lot sigefet1: sigefet1

Start 04/09/2001 16:41:48

End   04/09/2001 16:41:49
Comments:
16 wafers. Rec. 461, 625C dep, for 26 minutes. Used middle boat.
Used first 16 slots of that boat.
TBLCR, Most in: (1457, 1468, 1465, 1472, 1451).
Most out: (1549, 1546, 1553, 1547, 1541).
```

```
================================================================================
=
Wafers with thick oxide underneath, field oxide or poly dummy thickness
look green. The other wafers look like silicon, greyish tint. You can't
tell that there is poly-si on it.
================================================================================
=
Today, I will do the 25A N2O gate oxide stack. I will use tubeA1 recipe
161 for 10 minutes. I will download the recipe just when I began my cleaning.
That will reduce the temperature to 450C so that when I load the wafers
I will not get any oxidation while the boat goes in. First I do boat
out, then once the boat is out, I download recipe 161. I do this while
I am cleaning. The tube then goes down from 750C to 450C. It takes
about 1 hour for that to happen. I monitor the temperature on the computer
screen.
================================================================================
=
MACHINE: ICL rca              DATE: 04/10/2001 08:20:38   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 04/10/2001 08:20:41

End   04/10/2001 09:14:36

Comments:
16 wafers.
================================================================================
=
MACHINE: ICL tubeA1           DATE: 04/10/2001 14:19:21   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 04/10/2001 09:15:28

End   04/10/2001 14:19:22

Comments:
16 wafers. Rec. 161. 750C N2O gate oxidation.
FF=10 minutes. TT=25 angstroms. Thickness measured:
24-25 ansgtroms 5 point measurement.
================================================================================
==
I used the N2O ellipsometer program to measure the thickness. It
is very uniform across the wafer. The GOF was about 0.92 for all
measurements.
================================================================================
==
MACHINE: ICL tubeA6           DATE: 04/10/2001 17:44:58   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 04/10/2001 14:20:48

End   04/10/2001 17:44:59

Comments:
16 wafers. Rec. 461 625C dep temp. FF=26 min, TT=1500 angstroms.
Measured: TBLCR
Most Out: (1534, 1539, 1536, 1534, 1534)
```

Most In: (1494, 1505, 1502, 1507, 1495)
I used the middle boat first 16 slots from the left side.
==========
==
Wafers that have thick oxide underneath have a green color.
==========
=
MACHINE: ICL HMDS DATE: 04/11/2001 08:53:16 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/11/2001 08:53:17

End 04/11/2001 08:53:17

Comments:
24 wafers.
==========
=
Inside stepper recipe hasan cd, I created a pass labeled "1". It
exposes all die except for 2 SIMS die. The bottom 2 die will have polysilicon
and the top 2 die will be for S/D so they will be exposed.
==========
=
MACHINE: ICL coater6 DATE: 04/11/2001 08:53:53 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/11/2001 08:53:55

End 04/11/2001 15:51:04

Comments:
16 wafers.
==========
MACHINE: ICL stepper2 DATE: 04/11/2001 15:51:39 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/11/2001 15:51:40

End 04/11/2001 15:51:40

Comments:
16 wafers.
==========
=

MACHINE: ICL developer DATE: 04/11/2001 15:52:14 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/11/2001 15:52:15

End 04/11/2001 15:52:15

Comments:
16 wafers.
==========
=
MACHINE: ICL coater6 DATE: 04/11/2001 15:52:47 USER: hnayfeh

PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/11/2001 15:52:47

End 04/11/2001 15:52:48

Comments:
16 wafers. Hardbake.
==========
=
Today, I will do the polysilicon gate etch. I'll use recipe KEITHCP.
First, I will clean chamber B. Then, I'll do a 15 second BOE dip,rinse,
and spin dry and load into the loadlock and begin pumpdown immediately.
This is in order to remove the native oxide on the polysilicon.
I do the clean to minimize residual carbon that will reduce the selectivity
to oxide. To measure the selectivity to oxide, I need a wafer with
oxide on it with patterned resist so that the carbon will be included
for the calculation.
==========
=
The etch recipe is as follows:

main: 20sccm Cl2, 20sccm HBr, Power=300W, P=200mTorr, B=50Gauss
over: 40sccm HBr, Power=100W, P=100mTorr, B=50Gauss

I measured the following etch rates:

ymain=64.2*(t-2.2)
yover=18.2*(t-2.64)

where t is in seconds.

I started with a wafer having 1500A of poly. I etched the first
1000A using the main and then etched the remainder using the over
etch. I did a 40% overetch.

I imaged using the SEM. The etch has a foot and there are many
poly-si particles left on the surface. I assume that the reason is
that the overetch step is too long causing too much polymerization.
Today, I'll make the main etch step longer. I'll aim to etch 1300A instead
of 1000A and etch the remainder using the overetch aiming for 40% over.

I measured the selectivity to oxide by etching a bare wafer with gate
oxide on it for 2 minutes. I measured 24A etched after 2 minutes. This gives
roughly 12A/minute. This gives a selectivity of 90:1. Granted, the wafer
does not have resist on it, so the selectivity is an upper bound as carbon
residue will reduce the selectivity.

==========
=
Step1: Clean the chamber
Step2: 15 sec boe dip
Step3: d.i. rinse and dry
step4: load and pump down
step5: etch 1300A main etch
step6: etch 40% overetch
step7: measure remaining oxide

step8; 10 min p-clean to remove polymers
step9: ash for 1 minute

I measured a thinner oxide than I expected after etching. I got 25A left indicating that 20A had been etched. I did not expect that.

I measured the selectivity using a 45A wafer patterned with poly pattern resist mask. I get:

yoxide=0.306*(t-0.716) this gives a selectivity to polysilicon of ~70:1. If that's the case, this does not predict the remaining oxide that I measured.

==========

MACHINE: ICL AME5000 DATE: 04/19/2001 09:45:30 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 04/19/2001 09:45:30

End 04/19/2001 12:57:35

Comments:
5 wafers.

==========

Today I am doing two things: I am making 10 1500A polysi/1000A thermal oxide dummies for etching. Also, I am coating one wafer with the new focus settings that P. Tierney has found and then I'll etch it using the AME and then image.

==========

MACHINE: ICL tubeA6 DATE: 05/07/2001 13:14:31 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/07/2001 09:22:13

End 05/07/2001 13:14:32

Comments:
10 wafers. rec 461 26 minutes. TT=1500A.

==========

I will use the resist that I patterned the first time because the stepper is down- problem with the wafer height sensor.

I will do the gate etch.

==========

MACHINE: ICL AME5000 DATE: 05/10/2001 11:45:41 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/10/2001 11:45:43

End 05/10/2001 11:45:43

Comments:
16 wafers.

==========
=
etch rate calibrated on dummies:

ymain=67.4*(t-1.94)
yover=15.8*(t-0.5)

I measured the etch rate of thermal grown oxide using the overetch.

I get 0.44A/sec. Therefore, the selectivity of oxide to poly is ~ 36:1

I will etch 1000A of poly using the main etch and then do a 70% overetch.
All etches are preceded by a 15 sec BOE dip and rinse and immediate load
into the loadlock to keep any native oxide to a minimum.

The times I used were: 17sec main, 54 sec over. The amount of oxide etched
is about 15A. This is sufficient overetch to remove any poly stringers
at the edge of the active area.

After etching I imaged a crossection of SEM lines. The etch leaves a rough
line due to a bad resist develop. The resist roughness was imaged into the
poly-Si.

I etched the lot wafers and imaged under a optical microscope. I notice that
there is a region in the middle of each wafer that has a resist spot.
This is due to it being underdeveloped. I believe that the developer
spray gun was not uniformily placed over the wafer spatially.

I also notice that the smallest line that came out was 0.6 microns. I also
noticed that the line depends on the orientation of the line, whether it is
going from up or down, or left to right. I got smaller lines for those
going from up to down. This indicates there is stigmatism with x and y
directions.

I noticed that there is a mask error. The 0.20 and 0.25 um lines written
on the mask have a section of the line cutoff.

Wafer 312.2 had die where the resist lifted off. It appears to be bad photo.

I then did a 10 min p-clean in the blue to remove the resist and
a 10 min p-clean in the green so that the wafers can go to the rca
to be cleaned for the reox step.

No HF dips will be performed for any of the etches because the gate
oxide is exposed at the edges of the gate.
==========
==
MACHINE: ICL pre-metal DATE: 05/10/2001 11:55:08 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/10/2001 11:55:09

End 05/10/2001 11:55:09

Comments:
10 min blue, 10 min green.
==========
****

V.Reoxidation

****
==========
MACHINE: ICL rca DATE: 05/11/2001 10:24:33 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/11/2001 10:24:34

End 05/11/2001 10:24:36

Comments:
18 wafers.
==========
The clean was: 10 min p-clean, 2 d.i. rinses, 15 min sc2 clean at ~75C,
2 d.i. rinses, and dry.
No HF dip and No sc1.
==========
MACHINE: ICL tubeA2 DATE: 05/11/2001 11:46:24 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot chargethis: chargethis

Start 05/10/2001 09:39:55

End 05/11/2001 11:46:29

Comments:
17 wafers. Rec110. 800C for 10 min. TT=30 angstroms.
==========
Thickness measured on dummy wafer: 35angstroms
==========
****

VI. Source/Drain

****
==========
Send out for S/D and poly implant
energy=10keV, dose=5e15~ cm^-2, phosphorus
Sent to: Ion Implant Services, Sunnyvale, CA
==========
Wafers are back. 2 p-cleans blue then green. No HF dip. Necessary so that
wafers can go into the RTA.
==========
MACHINE: ICL pre-metal DATE: 05/14/2001 13:51:12 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

```
Start 05/14/2001 13:51:13

End   05/14/2001 13:51:13

Comments:
17 wafers.
================================================================================
==
MACHINE: ICL RTA2             DATE: 05/14/2001 17:02:09   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/14/2001 17:02:15

End   05/14/2001 17:02:16

Comments:
17 wafers. 1000C 1 sec anneal.
================================================================================
=
Measured resistivity of poly blank wafer by measuring sheet resistance.
I get: 3-4e-3 ohm*cm. This corresponds to greater than 8e19 cm^-3 doping.
That's very good.
================================================================================
=
**********************************
```

VII. Contact Cuts/Backend Processing

```
**********************************
================================================================================
=
Today, I'll deposit the ILD. I will aim to deposit 2500A of LTO.
I'll use rec462 for 20 minutes.
================================================================================
=
MACHINE: ICL rca
           DATE: 05/15/2001 10:02:55   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/15/2001 10:02:57

End   05/15/2001 10:02:57

Comments:
24 wafers.
================================================================================
=
MACHINE: ICL tubeA7           DATE: 05/15/2001 17:18:55   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/15/2001 10:03:37

End   05/15/2001 17:18:57

Comments:
24 wafers. rec462 for 20 minutes. TT=2500. Measured: 2500-2000A
going farther out. Used the middle boat. This is for a wafer span of 24.
```

```
================================================================================
=
I performed a hardbake at 130C for 60 seconds so that I can remove
the backside. Backside: 2500A LTO/30A reox/1500A poly/25-45A gate oxide/1500A
field oxide.
I'll do a BOE dip to remove the LTO and reox. I'll etch the poly in the
AME5000.
================================================================================
=
MACHINE: ICL coater6          DATE: 05/15/2001 17:47:07   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/15/2001 17:47:08

End   05/15/2001 17:47:08

Comments:
16 wafers.
================================================================================
==
Etch rate of BOE for undensified LTO: 63A/sec.
I'll do a 100% overetch:
2500*2=5000A. 5000A/63=~80sec=1min and 20seconds.
================================================================================
==
MACHINE: ICL oxide            DATE: 05/15/2001 17:54:15   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/15/2001 17:54:17

End   05/15/2001 17:54:17

Comments:
16 wafers.
================================================================================
==
I will continue the backside clear. I need to clear the polysilicon.
I'll use the KeithCP recipe mainetch step. It etches at about 50A/sec.
I'll aim to etch double the poly thickness so 2*1500A=3000A. That will
require 60 seconds. I'll add an extra 15 seconds for 'luck'.
Before etching, I perform a 15 sec BOE dip to remove native oxide.
8 wafers at a time are done.
================================================================================
=
MACHINE: ICL oxide            DATE: 05/16/2001 12:56:10   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1

Start 05/16/2001 12:56:11

End   05/16/2001 12:56:11

Comments:
16 wafers.
================================================================================
=    MACHINE: ICL AME5000         DATE: 05/16/2001 12:56:56   USER: hnayfeh
PROCESS: NONE                 WAFERSETS: Lot sigefet1: sigefet1
```

Start 05/16/2001 12:56:57

End 05/16/2001 14:18:40

Comments:
16 wafers.
==========
=
After etching in the AME, I noticed that the greenish color at
the back of the wafer is gone. Evidence that the poly has been etched.
I then did another BOE dip to remove the field oxide.
The LTO is densified since it has been through the high-T processing
steps. I'll assume that the rate is 1/2 so about 30A/sec. I have 1700A
of LTO. I'll aim to etch 4000A to be safe. That requires a time of
4000/30=133 seconds. So, 2 minutes and 15 seconds is sufficient.
==========
=
MACHINE: ICL oxide DATE: 05/16/2001 15:01:35 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/16/2001 15:01:35

End 05/16/2001 15:01:35

Comments:
16 wafers
==========
=
I did the BOE dip. The backside dewets indicating that the oxide is
gone. The backside is now clear!
Next, I'll strip the resist using p-clean for 10 minutes. I'll use
the blue quartzware.
==========
=
MACHINE: ICL pre-metal DATE: 05/16/2001 15:04:33 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 05/16/2001 15:04:37

End 05/16/2001 15:04:41

Comments:
16 wafers.
==========
=
The resist looks gone from the naked eye. Looked at a wafer
under the optical microscope. Resist appears to be gone. Need
a more deteminant method... Ready for contact cut litho!
==========
=

The stepper has been down for about 1 month. I will try to do contact
cuts today...
==========
=
MACHINE: ICL HMDS DATE: 06/14/2001 14:45:59 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/14/2001 14:46:00

End 06/14/2001 14:46:02

Comments:
24 wafers.
==========
=
Too many problems with the stepper. I cannot align because the camera image is horrible. When I can barely make out the cross on the XY portion of the split screen, the theta mark is not in view. Tried changing the flat setting to no avail.
==========
=

I'll meet with Paul tomorrow... he's out right now :(
==========
=
Camera problem fixed! Paul tightened the connection with his hands. I can now see clearly.
==========
=

MACHINE: ICL HMDS DATE: 06/15/2001 10:18:34 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/15/2001 10:18:36

End 06/15/2001 10:18:37

Comments:
24 wafers.
==========
=
MACHINE: ICL coater6 DATE: 06/15/2001 10:19:15 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/15/2001 10:19:18

End 06/15/2001 10:19:18

Comments:
24 wafers.
==========
=
MACHINE: ICL stepper2 DATE: 06/15/2001 16:51:56 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/15/2001 16:51:58

End 06/15/2001 16:51:58

Comments:
24 wafers. CC level. Dark field mask. Used 0.3/231.
Alignment better than 0.3um
in x/y for a significant fraction of the die.

This is true for all wafers.
==========
=
Today, I'll etch the contact cuts using the AME5000. I'll use
recipe HASANFOX.
==========
MACHINE: ICL AME5000 DATE: 06/25/2001 15:06:26 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/25/2001 15:06:29

End 06/25/2001 18:24:00

Comments:
16 wafers.
==========
=
I measured the etch rates on dummy wafers that have the same pattern.
I get: y=23.13*(t-1.43). The amount of LTO on the wafers varied from
2000-2700A. I aimed to etch 1750A using the AME and etch 1200A using the
BOE dip. The etch rate in BOE is: y=3120A/min. I did the AME for 77 seconds
and the BOE for 23 seconds. I did one wafer first. It looks great
using the naked eye and I looked under the optical microscope and it
looks good.
==========
=
MACHINE: ICL asher DATE: 06/25/2001 18:27:33 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/25/2001 18:27:34

End 06/25/2001 18:27:35

Comments:
16 wafers.
==========
=
Resist was removed using the asher. I programmed 2 min/wafer. Tomorrow,
I will deposit the metal: 1000Ti/1um Al. It will be preceded by a pre-metal
clean, and a 50:1 HF dip to remove any native oxide. I will do it in the
endura.
==========
=
Today, I'll deposit the Metal.
First, I'll do a pre-metal clean and follow it up with 15 sec 50:1 HF dip.
That should only etch ~100A of the undensified LTO. I will do eight wafers
at a time.
==========
=
I have 16 device wafers and 5 dummy wafers.

dummy1:1um Al
dummy2:1000A Ti
dummy3:1000A Ti
dummy4:1000A Ti/1um Al
dummy5:1000A Ti/1um Al
dummy6:1000A Ti/1um Al

First Step: I'll clean 8 device wafers and all the six dummy wafers. I'll immediately load the device wafers and deposit the metal. After I am done, I'll deposit the dummy wafers. I don't care about native oxide formation for the dummies since there are just etch dummies.

Second Step: I'll clean the other 8 device wafers and then immediately load into the endura.

==========

MACHINE: ICL pre-metal DATE: 06/26/2001 16:08:19 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/26/2001 16:08:20

End 06/26/2001 16:08:20

Comments:
24 wafers.

==========

MACHINE: ICL endura DATE: 06/26/2001 10:33:31 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/26/2001 10:33:32

End 06/26/2001 16:07:15

Comments:
22 wafers. 1000A Ti and 1um Al.

==========

I will do the metal photolithography this evening.

==========

MACHINE: ICL HMDS DATE: 06/27/2001 13:34:28 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 13:34:31

End 06/27/2001 13:34:31

Comments:
24 wafers.

==========

MACHINE: ICL coater6 DATE: 06/27/2001 13:35:02 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 13:35:03

End 06/27/2001 13:35:04

Comments:
24 wafers.

```
================================================================================
=
MACHINE: ICL stepper2          DATE: 06/27/2001 13:32:57   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 06/26/2001 18:00:00

End   06/27/2001 21:30:00

Comments:
24 wafers.
================================================================================
=

I found the optimum condition to be 0.20/231. The 0.26 exposure was too large
metal level is always less than other levels due to reflection. I had
to fine tune the exposure. 0.17 resulted in some resist in between the
metal connections where the poly line is.
================================================================================
=
Today: I will etch the metal using the rainbow. J. Walsh will train
me on it. I have 1000A Ti and 1um Al.
================================================================================
=

MACHINE: ICL TrainingICL       DATE: 06/27/2001 15:27:48   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 13:30:00

End   06/27/2001 15:27:55

Comments:
training with J. Walsh on rainbow machine.
================================================================================
==
MACHINE: ICL rainbow           DATE: 06/27/2001 15:49:07   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 13:46:04

End   06/27/2001 15:49:09

Comments:
16 wafers. 1000ATi/1umAl.
================================================================================
=
15 seconds of Ti etch in recipe 22 resulted in all the metal being
etched and 100-200A of the underlying LTO weree etched. This is what
I used. J. Walsh told me that after etching I have to do a dump rinse
immediately.
================================================================================
=
MACHINE: TRL acid-hood         DATE: 06/27/2001 17:39:34   USER: hnayfeh
PROCESS: NONE                  WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 17:39:35
```

End 06/27/2001 17:39:35

Comments:
16 wafers. D.I. rinse.
==========
=
I then ashed the wafers in the ICL. They look great! resist is gone, metal
appears underneath.
==========
=
MACHINE: TRL asher DATE: 06/27/2001 17:40:54 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/27/2001 17:40:55

End 06/27/2001 17:40:55

Comments:
16 wafers.
==========
==
Tomorrow morning I'll do the sinter and that will be the end!
==========
==
Sinter in Forming Gas. 400C for 40 minutes. Use Tube A3. Nitrogen
set at 51%. Purge and wait for temperature to reach 400C for load
and center. This takes about 10 minutes. After that, turn on forming
gas- channel 7 and set it at 40%. Turn off N2 chan1. Keep wafers inside
for 40 mins. See lab book for more details.
==========
=
MACHINE: TRL tubeA3 DATE: 06/28/2001 13:40:03 USER: hnayfeh
PROCESS: NONE WAFERSETS: Lot sigefet1: sigefet1

Start 06/28/2001 13:40:04

End 06/28/2001 14:17:56

Comments:
16 wafers. Sinter 400C for 40min.
==========

Appendix B

Low Resistivity Titanium Germanosilicide Formation at Low Temperature for Strained-Si n-MOSFET Applications

A single-step, low temperature reaction of titanium with a N^+ arsenic ion implanted $Si_{0.75}Ge_{0.25}$ layer that achieves low sheet resistance for the source/drain regions of strained-Si *n*-MOSFET devices has been developed. Thin ~70 nm titanium germanosilicide films with resistivity 22 Ω cm were obtained from a single-step RTA anneal at 560° C for 4 minutes using titanium source material. High resolution cross-sectional TEM shows the germanosilicide to be microstructurally smooth. X-ray diffraction indicates that the low-resistivity C54 phase was formed. The resistivity versus reaction temperature was measured and demonstrates a slow monotonic increase from 560°-700°C, followed by a sharp increase for higher temperatures. Cross-sectional TEM images show increased microroughness with temperature due to Ge diffusion into the C54 grain boundaries.

B.1. INTRODUCTION

It is well known that MOSFETs fabricated on tensile strained-Si layers grown on relaxed SiGe exhibit significant enhancement of electron and hole mobility, and current drive, at a given

channel length. Such devices are promising candidates for extending the performance limits of silicon MOSFET technology [70]. A challenge in the fabrication of sub 50 nm strained-Si *n*-MOSFETs is the formation of low resistance source/drain regions that are comprised of relaxed $Si_{1-x}Ge_x$ material. Several groups have reported on the reaction of titanium with $Si_{1-x}Ge_x$, but most studies have emphasized temperatures above 650° C [71-76]. Agnello et al. [71] studied the reaction of Ti with Si_{1-x} Ge_x films and demonstrated degraded film morphology with temperature due to Ge agglomeration in the temperature range of 700-800° C. Reaction temperatures less than 700° C were not explored. In addition, the ion implanted dopant species studied was phosphorous, not arsenic which is the typical dopant of choice for the source/drain in *n*-MOSFET devices. Rim [72] found a monotonic increase in germanosilicide resistivity for temperatures above 650° C. This work demonstrates a single-step, low temperature reaction (560° C) of titanium with a N^+ arsenic ion implanted $Si_{0.75}Ge_{0.25}$ layer that achieves low sheet resistance for the source/drain regions of *n*-MOSFET. Thin ~70 nm titanium germanosilicide films with resistivity 22 Ω cm were obtained from a single-step RTA anneal at 560° C for 4 minutes using titanium source material. High resolution cross-sectional transmission electron microscopy, (XTEM) showed the germanosilicide to be microstructurally smooth and indicated no formation of $Si_{1-z}Ge_z$ areas at C54 $Ti(Si_{0.75}Ge_{0.25})_2$ grain boundaries. X-ray diffraction (XRD) measurements demonstrate that the low resistivity C54 $Ti(Si_{0.75}Ge_{0.25})_2$ phase was formed. The resistivity versus reaction temperature of the germanosilicide demonstrates a slow monotonic increase of the resistivity for the temperature range of 560° C-700° C followed by a sharp increase due to the formation of $Si_{1-z}Ge_z$ areas at the C54 grain boundaries.

B.2. EXPERIMENTAL PROCEDURE

The wafers were grown by UHVCVD of a 1 μm $Si_{0.75}Ge_{0.25}$ relaxed layer grown on top of a graded $Si_{1-x}Ge_x$ buffer layer (x=0-0.25) in order to minimize threading dislocation density in the relaxed layer [77]. Arsenic was then ion implanted at a dose of $3x10^{15}$ cm^{-2} and energy of 15 keV, typical ion implant conditions for the deep source/drain regions in *n*-MOSFET devices. The implant was then activated and the damage was annealed by a RTA process that consisted of a short "spike anneal" temperature at 1000° C. Prior to Ti deposition, the wafers were cleaned by immersing in a solution of 3:1 H_2SO_4:H_2O_2 for 10 minutes followed by removal of the native oxide by immersing in a 50:1 HF solution for 30 seconds. The samples were then loaded in an Applied Materials Endura sputtering system with a base pressure of less than $1x10^{-8}$ Torr, where 50 nm of Ti was deposited. Thermal reaction was performed in a AGA RTA system under N_2 ambient flow of 10 sccm, for temperatures ranging from 560° C-800° C. The reaction time at 560° C was 4 minutes, and at all other temperatures it was for 30 seconds. Remaining unreacted Ti, TiN, and TiO films were then etched using a solution of 9:1 H_2SO_4:H_2O_2 for 10 minutes.

B.3. RESULTS AND DISCUSSION

Electrical Characterization

The behavior of the germanosilicide and silicide films with respect to the reaction temperature at which they were formed were analyzed by measuring the resistivity versus reaction temperature. The resistivity was obtained using the expression $\rho=R\square/t_s$ where R□ is the sheet resistance in

Ω and t_s is the silicide thickness in cm. The sheet resistance was determined using the Van der Pauw technique [72] and the silicide thickness was obtained using XTEM images of the resulting germanosilicide or silicide film. The resistivity versus temperature is shown in Fig. 1.

The measurements indicate that the reaction of Ti with the control silicon wafer exhibits typical behavior since the higher resistivity C49 phase, which has a resistivity in the range of 40-

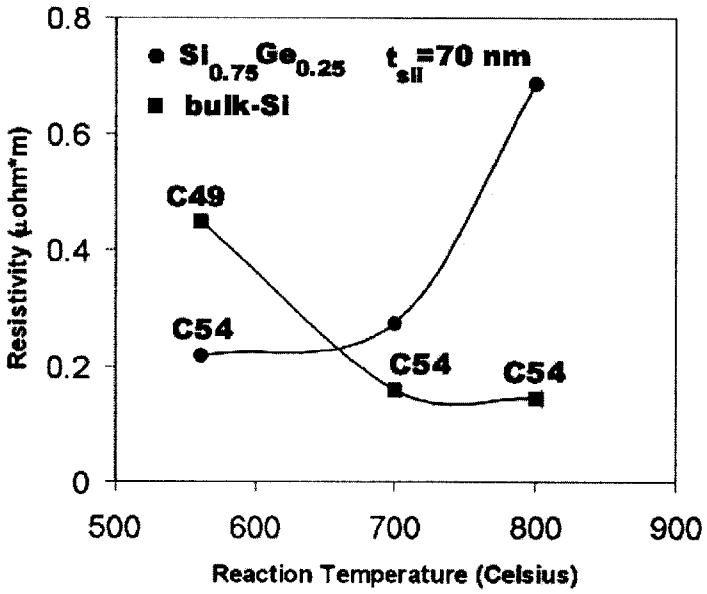

Fig. B.1. Germanosilicide and silicide resistivity versus reaction temperature for 50 nm of deposited Ti on silicon and $Si_{0.75}Ge_{0.25}$ substrate. The silicide exhibits typical behavior where the formation of the C49 phase precedes the formation of the C54 phase at higher temperature. The germanosilicide exhibits the low resistivity C54 phase at low temperature and suffers from high resistivity due to Ge agglomeration at higher temperatures.

60 μΩ cm, is formed at 560° C and the low resistivity C54 phase appears to have been formed at around 700° C, since the resistivity is in the range of 12-15 μΩ cm [78]. The germanosilicide, on the other hand, exhibits different behavior. The low resistivity phase appears to have been formed at the low 560° C temperature and is not preceded by a high resistivity phase as is the case with Si. The resistivity then increases slowly with temperature and then sharply increases for temperatures greater than 700° C, which will be shown to be due to Ge agglomeration into the $Ti(Si_{0.25}Ge_{0.75})_2$ grain boundaries from XTEM images.

The sheet resistance of germanosilicide with thinner as-deposited titanium was also explored, although XTEM of the film was not performed to determine the silicide thickness. The sheet resistance achieved after the deposition of 20 nm of Ti and reaction at 560°C is 4 Ω/□, which should be acceptable for sub 50 nm *n*-MOSFET devices. We can estimate the germanosilicide thickness by assuming that the ratio of the as-deposited Ti to the $Ti(Si_{1-x}Ge_x)_2$ thickness achieved when 50 nm of Ti were deposited, which is 1.4, is the same for the case of 20 nm of Ti deposited, resulting in a germanosilicide thickness for 20 nm of Ti deposition of roughly 28 nm. A germanosilicide film 28 nm in extent is less than one third of the deep source/drain junction depth which is ~100 nm for sub 50 nm MOSFETs; thereby, minimizing the chance of Ti spiking to the isolation junctions [79]. We should note that the value of 1.4 is different than the expected ratio of 2.2 and we speculate that this is due to the ambient N_2 gas reacting with the Ti during the RTA reaction resulting in the formation of TiN [73]. We observe in the XTEM images a thin layer on top of the germanosilicide film before the selective etch, and we speculate that this is TiN.

B.3.1. Film Morphology and Crystallography

XTEM imaging along with XRD analysis was performed to explore the resistivity behavior of the germanosilicide film with reaction temperature. Fig. B.2-4 show XTEM images of the $Si_{0.75}Ge_{0.25}$ film after titanium reaction at 560° C, 800° C, and 700° C showing a degradation of the morphology with increasing reaction temperature.

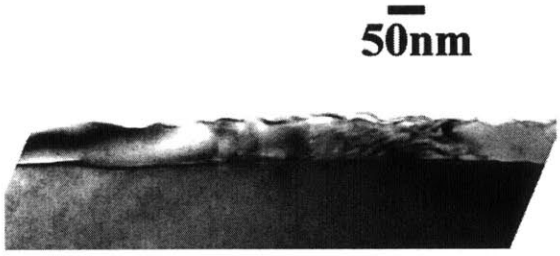

Fig. B.2 XTEM of a film of $Si_{0.75}Ge_{0.25}$ that had a 30 nm Ti film deposited on it and reacted at 560° C. The image demonstrates a smooth interface and the resistivity is low, 22 μΩ cm

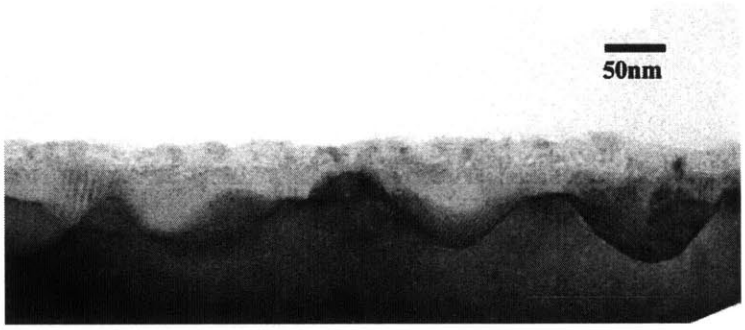

Fig. B.3. XTEM of a film of $Si_{0.75}Ge_{0.25}$ that had a 30 nm Ti film deposited on it and reacted at 800° C. The image demonstrates rough morphology due to Ge agglomeration resulting in an increased resistibility of 70 μΩ cm

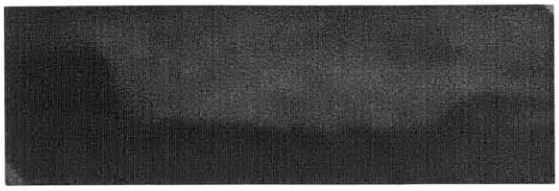

Fig. B.4. XTEM of a $Si_{0.75}Ge_{0.25}$ film that had a 30 nm Ti film deposited on it and reacted at 700 ° C. The dark areas correspond to $Si_{1-x}Ge_x$ areas due to Ge agglomeration and the light areas are $Ti(Si_{1-x}Ge_x)_2$. The resistivity was measured to be 28 μΩ cm, which is larger than the resistivity of the film that was reacted at 560° C, 22 μΩ cm.

The degradation of morphology with reaction temperature was reported by Aldrich et al. [76] who observed Ge agglomeration into C54 $Ti(Si_{1-y}Ge_y)_2$ grain boundaries forming $Si_{1-z}Ge_z$ rich areas from XTEM images. They demonstrated that the formation of the $Si_{1-z}Ge_z$ was thermally activated since the morphology was degraded with increased reaction temperature.

Although the resistivity data indicates that the reaction at 700° C results in a satisfactory germanosilicide film, our XTEM images show that the germanosilicide film is not optimized due to the formation of $Si_{1-z}Ge_z$ areas degrading the morphology. We speculate that this will then result in the 700° C film having a degraded contact resistance to the N^+ source/drain regions as compared to the 560° C germanosilicide film, since at 560° C the $Si_{1-z}Ge_z$ islands have not formed at the $Ti(Si_{1-x}Ge_x)_2$ grain boundaries.

XRD was performed on the germanosilicide film that was formed at 560° C to verify that the film is in the $Ti(Si_{1-x}Ge_x)_2$ C54 phase. The XRD data are shown in Fig. B.5 where the solid

lines indicate the peaks of the C54 $TiSi_2$ phase. The data exhibit a shift of the (311) crystallography peak from 2-theta of 39.2° to 38.5°. We speculate that this could be due to the presence of Ge in the silicide since the XRD peak of C54 $TiGe_2$ occurs at 37.5° which is lower than the location of the (311) peak of C54 $TiSi_2$ [80]. The location of the 2-theta peak for C54 $Ti(Si_{0.75}Ge_{0.25})_2$ was calculated to be at 38.7° by performing a linear interpolation from the 2-theta location of $TiGe_2$ and $TiSi_2$. We should note the other C54 $TiSi_2$ peaks were not detected for unknown reasons.

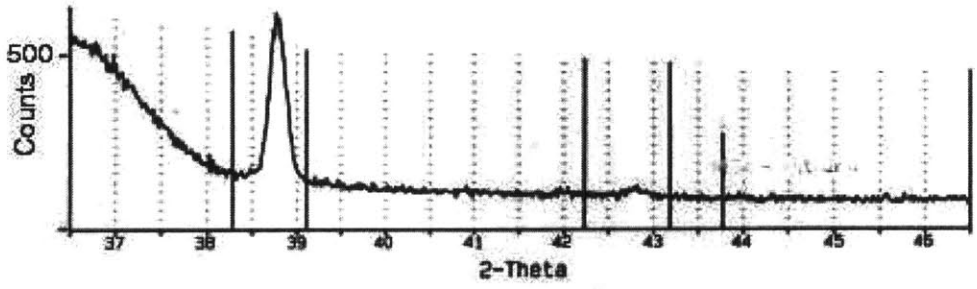

Fig. B.5 XRD data from a $Ti(Si_{1-x}Ge_x)_2$ film that was reacted at 560° C. The solid lines indicate the peaks of the C54 $TiSi_2$ phase. The data exhibit a shift of the (311) crystallography peak from 2-theta of 39.2° to 38.5° due to the presence of Ge in the silicide.

B.4. CONCLUSIONS

A single-step, low temperature reaction of titanium with a N^+ arsenic ion implanted $Si_{0.75}Ge_{0.25}$ layer that achieves low sheet resistance for the source/drain regions of *n*-MOSFET devices has been developed. Thin ~70 nm titanium germanosilicide films with resistivity 22

Ω cm were obtained from a single-step RTA anneal at 560° C for 4 minutes using titanium source material. High resolution TEM examination showed the germanosilicide to be microstructurally smooth and indicated no formation of Si_{1-z} Ge_z rich islands in the C54 $Ti(Si_{0.75}Ge_{0.25})$ grain boundaries. X-ray diffraction was used to demonstrate that the low resistivity $TiSi_2$ C54 phase was formed. We studied the resistivity versus reaction temperature of the germanosilicide and demonstrated a slow monotonic increase of the resistivity for temperatures form 560°C-700°C followed by a sharp increase in resistivity due to Ge agglomeration, which was confirmed by XTEM.