Morphology and Performance in Pentacene

by

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Massachusetts Institute of Technology

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of
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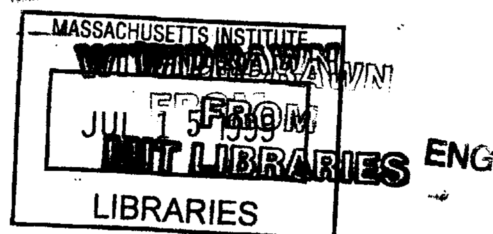
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Abstract

Organic semiconductors for use in thin film insulated gate field effect transistors are discussed. The general structure and properties of this class of materials are presented, along with specific examples for the high performing organic semiconductor material pentacene. Several experiments attempting to correlate the morphology, performance, and effective trap density of pentacene with the deposition conditions were performed. Conditions varied were thickness, substrate temperature, and the placement of the electrodes. No correlation was found between any parameters and thickness or substrate temperature. The electrode placement correlated strongly with morphology and performance. In particular, the placement of electrodes onto the substrate before the pentacene halved the effective mobility and encouraged the formation of small grains in the channel. Finally, the use of high dielectric constant insulators for reducing the threshold voltage and improving the effective mobility at these small voltages was explored. A device produced using a room temperature process on a polycarbonate structure with a mobility of 0.27 $cm^2/(Vs)$ at 5V was constructed.

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The greatest thanks, however, must go to my mentor and co-worker at IBM, Christos Dimitrakoupoulos whose project I joined almost four years ago. His help and teaching have guided my development in every way during my time at IBM and MIT. It is not an exaggeration to say that he has taught me everything I know, and this project is his work as much as it is my own.

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Introduction

Motivation/applications

With the proliferation of computing devices an increased need for new semiconductors has developed. Crystalline semiconductors currently serve as active materials in most computing and signal processing applications. Polycrystalline materials have found a niche in several markets, most notably small displays and photovoltaics. Amorphous semiconductors have found wide use as the active material in the backplanes of active matrix liquid crystal displays. The latter two thin film technologies represent a large market, and are enabling technologies for a number of portable computing applications.

The performance of amorphous silicon materials is quite poor by crystalline semiconductor standards. Amorphous silicon can, however, be cost-effectively deposited onto transparent substrates and processed into working devices. While expensive, this process has proven to be the most competitive for displays and other large area active matrix devices (such as x-ray detection systems).

Target properties

Despite the existence of many established large area thin film technologies, several desirable properties are still lacking. None of these materials can be processed at room temperature. While some work has reported successful polysilicon and amorphous silicon devices on polymeric substrates (1,2), the ability to process a large areas at room temperature with consistent properties is still not present. The use of polymeric substrates is believed to be an important step in reducing the cost and weight of these

display systems. Inorganic semiconducting materials are brittle, and their flexibility is limited. Also, the need for high temperature processability requires the use of heavy, fragile, and rigid glass or quartz substrates. While some work has been performed to create flexible TFTs using these inorganic materials (3), it is still not known how to make a truly conformable (or, at a minimum, more durable) complete display.

Organic semiconductors could solve these problems. They are flexible thin films which are easily deposited onto room temperature substrates. Many have a preexisting semiconducting character and do not require doping. They are also resistant to many types of environmental contamination. These materials have great potential for use in low cost-large area electronics such as imaging systems, RFID tags, small memories, and smartcards.

History

Most organic semiconductor work has focussed on the use of insulated gate field effect transistors (also referred to as MOSFETs, MISFETSs or IGFETs). Although some work has been done to make bipolar devices (4,5), most organic semiconductors are p-type, limiting their use to MOSFETs. The first reported organic MOSFETs were made from polythiophene, a conjugated polymer (6). These materials are characterized by a great deal of charge delocalization along the carbon backbone of their structure through pi bonds.

Several other conjugated materials have been evaluated for their semiconducting ability. Rod-shaped oligomers have performed best due to their ability to self-assemble into large grains. This is believed to help the transport through the material, and a material of this type is investigated in this thesis. Hexithiophene, and a better ordered

end substituted alpha hexithiophene have been investigated by a number of groups (7, 8, 9). Several circuits have been demonstrated, and integration of these materials with inorganic systems to produce complementary circuits has also been explored. Similar conjugated oligomers, but with fused benzene instead of thiol rings, have also been found to be semiconducting. The best performing organic semiconductor to date, pentacene, is of this type.

State of the art

Research continues with many of these organic semiconductors. Much of it focusses on determining the single crystal characteristics of these materials, improving the ordering, and discovering new materials with better performance and better processability. The following table summarizes representative properties reported in the recent literature for several important materials, both organic and inorganic:

Material	Mobility	On/Off ratio	Special properties	Reference
hydrogenated amorphous silicon	1.2 $cm^2/(V \cdot s)$	$>10^7$	Low temp. possible	10
polysilicon on polymer	60 $cm^2/(V \cdot s)$	$5 \cdot 10^5$	Low temp possible	2
polysilicon on quartz	262 $cm^2/(V \cdot s)$	10^6		11
pentacene	0.6 $cm^2/(V \cdot s)$	10^5		12
hexithiophene	10^{-3} $cm^2/(V \cdot s)$	100		7
α-hexithienylene	0.08 $cm^2/(V \cdot s)$	10^6		13
Regioregular poly (3-hexylthiophene)	0.045 $cm^2/(V \cdot s)$	10	Soluble	14
PTV	0.22 $cm^2/(V \cdot s)$	100	Soluble	15

Figure 1- Table listing competitive thin film semiconductor materials

Most semiconducting oligomers are difficult to process. High performing materials are generally insoluble in common solvents, and therefore cannot be

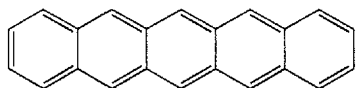
spin-coated or solution cast (6, 16). They are also intolerant of exposure to many common solvents and will degrade if exposed to photoresists, or even water, due to relaxation of internal strain upon exposure which deforms the material (17). This makes blanket deposited films nearly impossible to pattern. To date only shadow and step isolation techniques have been successful in isolating these oligomeric materials (18).

There are several reports in the literature of projects developing n-type organic semiconductors. One relatively unstable but effective material is C-60, successfully used by a group at Bell Labs (5). C-60 has the limitation that it rapidly degrades on contact with moist air. Other materials suffer from low performance. Success in finding a stable n-type material would be important for low power complementary logic applications.

Background

Conduction Theory

The theory of conduction in semiconducting organic materials is not generally agreed upon, but a combination of optical, electrical, and chemical experiments have provided significant insight into the functioning of these materials. The structure of pentacene is shown below:



Formula: $C_{22}H_{14}$
Molecular Weight: 278.35
Melting point: 573K
Vapor Pressure at 444K=0.00161 Pa

Figure 2-Basic structure and properties of pentacene

(Reference: 19)

Pentacene absorbs in the blue region of the spectrum, and has an optical bandgap of 2.8eV (20). Attempts to calculate the electrical bandgap through theoretical calculations have met with some difficulty, primarily because of an unusually strong phonon-electron interaction in the material. This effect localizes the carriers to each molecule and prevents an extended Blotch-like state from forming. This destroys the electron energy levels needed for a true band structure to exist (20). Further complicating matters, true carrier hopping is not observed. While it is expected that there should be a strong temperature dependence for the mobility of hopping carriers, this is not observed at all temperature ranges and the actual mechanism is still under debate (20, 21).

Normally, one expects approximately a $T^{-3/2}$ temperature dependent mobility in a crystalline material (22). In many materials (including silicon and germanium) phonon interaction effects alter this function, since phonon scattering is also modulated by the temperature change. In pentacene a temperature dependence on mobility is observed only at low temperatures. At higher temperatures the mobility becomes constant. This has been explained by several authors by the band-to-hopping transition of the material's electronic structure. According to this hypothesis, above a certain temperature the phonon activity is high enough to force a localization of the carriers by reduce the overlap amongst molecules. At this point, the Bloch extended wave function is destroyed and there is no ballistic transport from which the electrons may be scattered from. The mobility is then dominated by the mechanism which governs movement from molecule to molecule, which in the case of benzologues has been experimentally observed to be temperature independent (21).

At best, a band-like structure is a valid assumption only at lower temperatures, where fewer phonons exist and the phonon disruption of the lattice is weaker. In this regime the phonons may scatter the electrons, modulating the mobility, but do not affect the electronic character of the material. Alternative attempts to explain the conduction through thermionic emission have been complicated by this temperature independence, since one would expect increased temperature to provide additional energy to overcome the activation barrier. This mechanism is a matter of current research.

Conjugation

The pentacene molecule (as well as most other organic semiconductors) exhibits a large degree of electron delocalization along its length. As in benzene and other benzologues, a large amount of resonance delocalizes the electrons within each molecule. This property is known as conjugation. The molecule is also planar (23), which permits the molecule to arrange into a regular closely packed crystal structure. van der Waals interactions further encourage packing of the pentacene. This permits some overlap of the pi bonds amongst molecules. This also provides a degree of inter molecule delocalization which, while much weaker than that normally observed in crystalline materials and scatters readily as noted above, permits this ordinarily insulating material to possess a semiconducting character. The following diagram illustrates the electron bonding pattern:

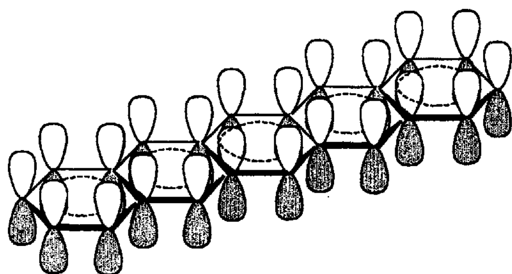


Figure 3-Drawing showing pi electron distribution in pentacene

This presentation emphasizes the p-type orbitals in the aromatic hydrocarbon chain. The sp_2 electrons all lie in a plane (experimentally observed to be almost exactly 120° apart), and the remaining pi orbital extends normal to this plane. It is this extended pi bonding which provides both the resonance stability of pentacene (which contributes to its oxidation resistance, amongst other properties) and the semiconducting character of the material. Additionally, since the pi electrons are delocalized along the entire molecule the movement, or even loss, of a carrier is not as energetically significant as it would be in a single atom since the energy gain or loss is shared through the molecule.

The weak localization of the electrons in pentacene surrounds much of the problem present in defining its electrical properties. The optical properties are primarily governed by the interaction of light with individual molecules, as in most organic systems. This is in contrast to the situation in crystalline materials, where the optical properties are determined from (relatively) macroscopic structure. Many electrical properties, however, are governed by the delocalization of the electrons amongst these molecules. To complicate matters, one normally expects a transition from discrete to continuous energy states as one considers systems ranging in size from the atomic to the large molecular scale (24). Pentacene falls in between, complicating estimates of its carriers' energy levels.

Despite these difficulties devices made using organic semiconductors are very well modeled by the same equations used for traditional semiconductors. The electrical characteristics will be treated using the traditional semiconductor terminology, and the material will be spoken of as if it has a definite Fermi level, bandgap, etc. This is the standard treatment used in the literature (25).

It should be noted that even though these materials are well described using traditional semiconductor equations, the parameters used in the modeling are not necessarily analogous to those used for crystalline semiconductors. To first order at least, any system whose conductivity is linearly related to the electric field will be modeled adequately by the same equations as silicon regardless of any relationship between its physical properties and model parameters. The threshold voltage in pentacene, for example, cannot be predicted in the usual manner. Instead, the threshold voltage is most significantly affected by the density of the traps in the material and the effect that this will have on the conductivity (35). It is merely a notational convenience to refer to this parameter as the threshold voltage, and it will not give us any reliable information about the position of the Fermi level, for example. Other examples of this phenomenon, most notably in the definition of mobility, are common.

HOMO/LUOMO

In organic materials there is generally a discrete set of energies which are occupied by the electrons within each molecule. Looking to minimize the energy in the system, these electrons generally fall to the lowest energy orbital states permitted by quantum exclusion rules. The energy states adjacent to the occupancy level (analogous to the Fermi level) are known as the frontier levels. The HOMO and LUMO are the highest

occupied molecular orbital and the lowest unoccupied molecular orbital, respectively. These energies are important in discussing chemical reactivity, and it is also the promotion of carriers to and from the HOMO and the LUMO that accounts for many of the optical properties, the formation of polarons, and so forth. This should not be confused with an extended Bloch function, however--this energy gap is not caused by interactions among molecules, but by the nature of the molecular orbitals within each molecule.

One classic example of this phenomenon is in the organic molecule butadiene. Here, as in pentacene, the electrons are pi-delocalized along a double bond in the center of the molecule. The orbital states are more easily visualized due to the geometry of the problem, i.e. the linear series of carbon molecules. One can approximately model the electron states within the molecule a particle in a box problem, with the length of the bond as the width of the potential well. The electron states correspond to the states of the electrons in the well problem. There are two electrons in the pi-system for butadiene. A chemist might view these states as higher energy states of the merged pi orbitals. A physicist might view the problem as one of entrapment of the electrons in a well. Both views yield results which are surprisingly close to experiment.

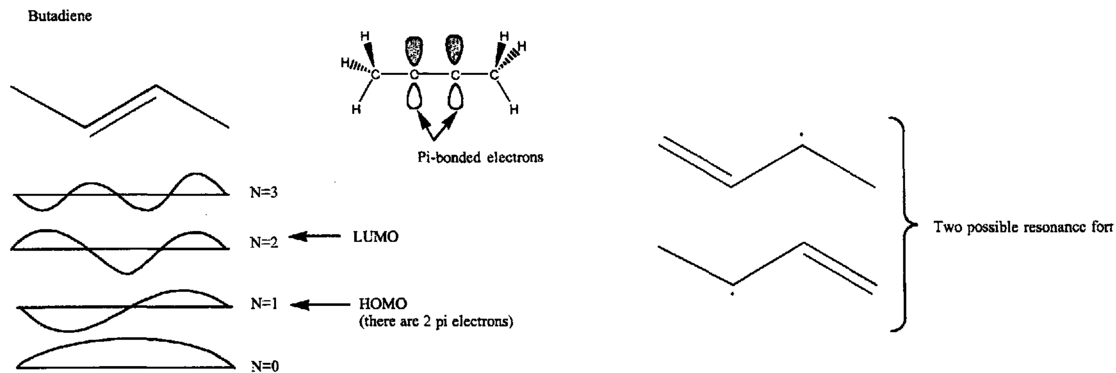


Figure 4--Diagram explaining HOMO and LUMO states, using butadiene as an example.

(26)

Accumulation Layer and Significance of the Interface

Pentacene, like most organic semiconductors, is p-type. This means that conduction in the material is dominated by positively charged carriers, namely holes. In an MOS type structure, these holes are attracted to the interface of the semiconductor with the gate insulator whenever a negative gate bias is applied. The device is then said to be in accumulation. The following diagram demonstrates this and the analogous band diagram of a crystalline semiconductor (27):

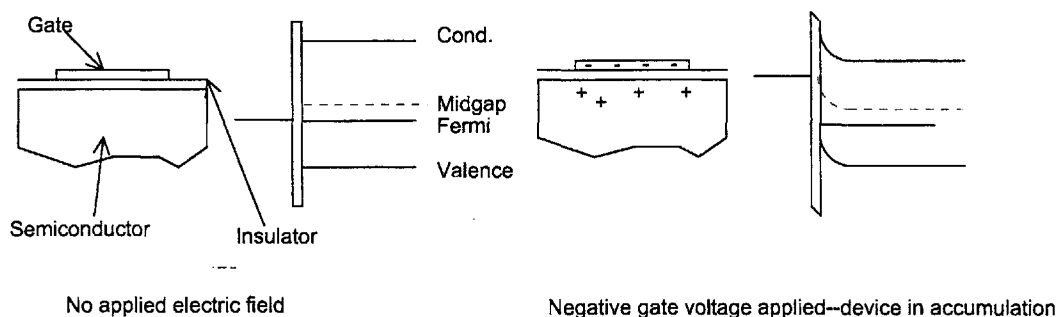


Figure 5--Energy band diagram for a TFT

Just as in conventional semiconductors, carriers are drawn to the semiconductor-insulator interface by the vertical gate field, and can then be driven across

the channel by a horizontal applied electric field. The application of a positive gate field induces a depletion increases the difficulty of driving carriers across the channel.

It has been demonstrated that the accumulation region in hexithiophene, a similar organic material, is only several monolayers thick and lies right at the interface between the insulator and semiconductor (28). It therefore follows that only the properties of the material against that interface will affect most of the electrical performance. This has been preliminarily demonstrated in pentacene in one experiment by depositing a high quality thin first layer and then covering with lower quality, more easily grown material (29). Confirmation of this effect with better control and more samples is needed, however, to quantify the conditions under which the interface is optimal.

It is the morphology of the deposited pentacene which is responsible for its excellent semiconducting properties. When vacuum deposited onto SiO_2, pentacene forms a self assembled triclinic structure with the following lattice constants (30):

a (Å)	7.90	α (°)	101.9
b (Å)	6.06	β (°)	112.6
c (Å)	16.01	γ (°)	85.8

Fig. 5.5--Crystal parameters for pentacene.

It has been demonstrated using x-ray analysis that the first few monolayers are significantly more highly ordered and form what is known in the literature as the single crystal phase (31). Dipole interactions cause a mutual repulsion between the hydrophilic SiO_2 and the non-polar pentacene. This repulsion causes the pentacene molecules to stand up on end during deposition to minimize contact with the substrate. Further increasing the packing and order, the thermodynamics of the situation favor travel over some distance for each deposited molecule to be stabilized by a van der Waals attraction

standing next to another pentacene molecule. Once several layers have been formed, however, the incoming molecules are shielded from the substrate and are willing to travel less than before. This encourages more frequent nucleation. As a consequence smaller grains form, in a structure known in the literature as the thin film phase. This is typical of Stransky-Krastanov growth. A highly ordered underlayer of only several monolayers forms, with a polycrystalline form growing in islands (i.e. grains) above. Eventually the pentacene molecules are so screened from the substrate dipole that they no longer stand on end. This leads to the formation of randomly oriented grains of material on top of a thick pentacene layer.

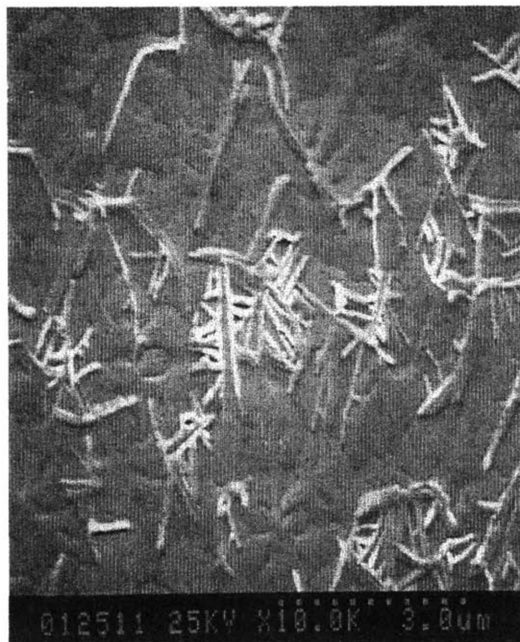


Fig. 6--This micrograph shows the structure of pentacene formed during a deposition. The material initially segregates into grains, and eventually shields the substrate so well that randomly oriented grains form on top. Both of these phases are visible in the micrograph. Fig. 11 shows the thin film phase.

The self-assembly of pentacene onto SiO_2 at room temperature does not form its thermodynamically most stable form. When pentacene is deposited onto heated

substrates a slightly tighter, more stable form of the crystal packing is observed. This phase begins to form at around 60 °C. This phase has slightly closer pentacene molecules than the room-temperature kinetically favored thin-film phase. Because the crystal constants are close in magnitude, the corresponding x-ray peaks for both forms overlap somewhat. A peak splitting is observed in the x-rays while the two phases coexist (caused by the superposition of two separate diffraction patterns whose peaks are near each other). At further elevated temperatures only the more stable packing structure exists, and a single set of peaks is again observed in the diffraction analysis. Another effect observed is increased grain size as temperature is increased (31,32). This is expected from the increased surface mobility of the pentacene.

Device Structure and Fabrication

The devices used for this study are all test devices fabricated using an inverted TFT layout. The layout and process are summarized in the following diagram:

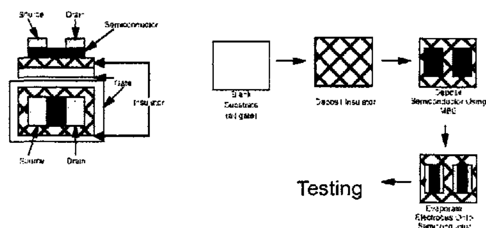


Fig. 7--The structure and fabrication flow of a pentacene TFT

For typical experimental devices a heavily doped (n++) silicon wafer was used as a common gate. Thermally grown SiO_2 500nm thick served as a gate insulator most samples. Pentacene was then deposited in UHV conditions through a molybdenum shadow mask. Typical background pressures were 10^{-8} torr, achieved by the use of two turbopump evacuated loadlocks and an ion pump. As recieved (Fluka, 97%+ purity)

pentacene was loaded into ceramic crucibles and then heated to 265 degrees C. The sample had not been purified. Very repeatable characteristics were observed from this arrangement, however. All of the samples were deposited within a short time from the same pentacene load. In addition, the sample of pentacene had been used in a number of other depositions and had spent an extended time in high vacuum. This treatment helped eliminate relatively volatile contaminants and reduce material variability between depositions. After pentacene deposition 60nm of gold were deposited through a set of silicon membrane shadow masks to form the source and drain electrodes. The sample was then tested.

Several special systems were constructed specifically for this project. Fully custom testing software was programmed in Visual Basic to automate the testing process and also enable the collection of impedance and capacitance spectra using existing equipment. A special UHV stage was also designed and built which incorporated a thermoelectric element to heat and cool the substrate during deposition.

For this thesis, three sets of samples were prepared. In each set only one variable exists amongst the samples. In one set, FETs were deposited in an environment where the substrate temperature was varied. In another set, FETs were deposited at different thicknesses onto SiO_2 substrates with and without pre-patterned gold electrodes. The samples without electrodes then had gold deposited onto them, as usual. In the final set the gate insulator was varied. It is from the variation within these sets of samples that I hope to draw my conclusions. The initial hypotheses were:

-Higher temperature samples would show a larger grain morphology

-Higher temperature samples would have a higher mobility

-Higher temperature samples would have fewer traps

-Thicker samples with electrodes on top would have a smaller mobility

-Thicker samples with electrodes underneath would have the same mobility

-All thicker samples would have smaller on/off ratios than the corresponding thinner samples

-Gate insulators with higher dielectric constants will show superior performance

Applications and Relevance to Figures of Merit

There are several potential applications for these materials. They generally fall into one of two categories: current supply and logic. In both, three characteristics are desirable: infinite switching speed, zero power consumption, and infinite current carrying capability. In PMOS logic and capacitor charging the switching delay is affected by the following factors (assuming all other factors constant):

- Increases linearly with gate capacitance and other parasitics
- Decreases linearly with current driving capability
- Is constant with supply voltage (assuming symmetrical switching)

So the goals are then to:

- Increase current drive
- Decrease stray parasitics

Many parasitics are under the designer's control. For example, material selection and layout for the interconnect can significantly affect circuit performance. In this study

leakage through gate insulators was a problem when an alternative material to SiO2 was considered. Other parameters may be traded off for optimal performance-- current handling and power consumption, for example, may be exchanged in most applications, as can gate leakage and gate capacitance.

Of the parameters under the designer's control, the most significant is the current drive. The current in an FET in saturation is given by:

$$I_{D_{SATURATION}} = \frac{W}{L}\frac{\mu_{effective}C_O}{2}(V_G - V_T)^2$$

Where I_{DS} is the saturation drain-source current, W is the device width, L is the channel length, C_O is the normalized gate capacitance, V_G is the gate voltage, V_T is the threshold voltage, and $\mu_{effective}$ is the field effect mobility of the semiconductor (27 p 76).

For a given device there are two options to increase the current flow at a given supply voltage and geometry--to increase the mobility or to increase the gate capacitance. Increasing the gate capacitance also increases the parasitic capacitance of the system, and it is not a priori clear that this will benefit the circuit. This issue will be addressed later. Increasing the supply voltage will also increase the current flow, but increases the power consumption and usually does not increase the speed of digital circuits. Increasing the mobility is the only other certain way to increase the current flow.

Several theories exist to explain the mobility variation among samples (28, 32, 33). The difficulty in controlling sample characteristics limits the ability to confirm any single conclusion. It is generally agreed, however, that trap states exist in the pentacene which can capture and delay charges or scatter charges (33). A higher density of these traps, therefore, would decrease the field effect mobility, discussed further below. The

nature of these trap states still remains unclear. In hexithiophene it has been demonstrated that these states are generated at grain boundaries (28). While some evidence exists that this is true in pentacene, there exist few attempts to directly measure the trap density of pentacene in the literature electrically (34). The precise nature of the trap states remains unknown.

Basic Parameter Analysis

Mobility

Organic FETs are adequately modeled by the equations normally used for inorganic semiconductor materials (25). One of the more significant modeling parameters (and the only material parameter included in the simplest model) is the effective device mobility. It is well known that this parameter is not equal to the bulk mobility in any semiconducting material due to a number of scattering effects an FET experiences not present in the bulk material (27). The conventional square-law FET equations are (for the triode and saturation regions, respectively) (27):

$$I_{D_{TRIODE}} = \frac{W}{L}\frac{\mu_{effective}C_O}{2}[2(V_G - V_T)V_D - V_D^2]$$

$$I_{D_{SATURATION}} = \frac{W}{L}\frac{\mu_{effective}C_O}{2}(V_G - V_T)^2$$

Where I_D is the drain current, V_G is the gate-source voltage, V_D is the drain-source voltage, W is the channel width, L is the channel length, C_O is the unit capacitance of the gate dielectric, and $\mu_{effective}$ is the effective device mobility.

Taking partial derivatives we find:

$$\frac{\partial I_{D_{TRIODE}}}{\partial V_G} = \frac{W}{L}\mu_{effective} C_O V_D$$

$$\frac{\partial \sqrt{I_{D_{SATURATION}}}}{\partial V_G} = \sqrt{\frac{W}{2L}\mu_{effective} C_O}$$

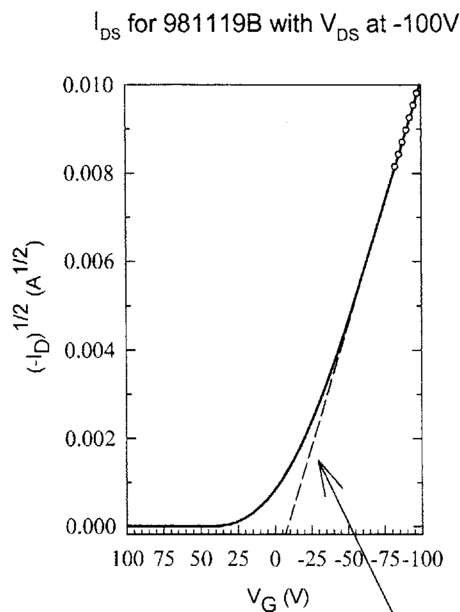
And solving for the mobility,

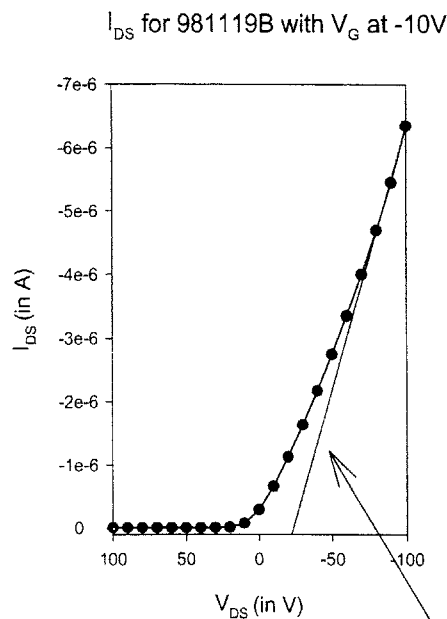
$$\mu_{effective} = \frac{L}{W C_O V_D}\frac{\partial I_{D_{TRIODE}}}{\partial V_G}$$

$$\mu_{effective} = \frac{2L}{W C_O}\left(\frac{\partial \sqrt{I_{D_{SATURATION}}}}{\partial V_G}\right)^2$$

The two observed mobilities are generally similar, and each is significant for different applications. It should be noted that small barriers to charge injection at the electrodes can decrease the effective mobility in the triode region and make it significantly smaller than that in saturation.

To more explicitly demonstrate the data extraction the following figure graphically indicates the parameters used for the analysis:





This slope is used for the saturation mobility

This slope is used for the linear region mobility

Fig. 8--These graphs show the drain-source current as a function of the gate voltage (on the left) with the drain-source voltage fixed at -100V, and as a function of the drain-source voltage with the gate voltage fixed at -10V. The saturation current's square root is plotted to simplify the algebra.

Mobility link to morphology

One of the hypotheses for this experiment was that a morphology with fewer traps would also yield samples with higher mobility. The theoretical basis for this expectation is outlined below.

Traps, which will be treated as scattering centers, may be classified into two categories-- charged and uncharged. In both cases a larger number of traps causes a decrease in material mobility. The change in the mobility, however, is carrier velocity dependent in the charged trap case and velocity independent when the traps are uncharged. Additional field dependence may be seen from passivating certain trap states by filling them with carriers. Indeed, evidence in pentacene presented later shows that

the mobility is dependent on the gate--and not drain-source--field, indicating that traps of this nature exist. This further implies that many of the traps in pentacene are charged and operate through a capture (and possibly also an electrostatic) scattering mechanism. Other scattering effects, such as phonon scattering, further complicate drawing any conclusions.

Mobility may be defined by looking at a group of charges moving through a material. If a solid contains N scattering sites per unit volume, a carrier with velocity v will pass $N^{1/3}v$ scattering sites per second. The mobility may then be determined by imagining a number of electrons starting off with the same velocity v_i in the same direction. After scattering, a distribution of velocities $U(\theta)$ will develop, with θ being the angle to the original direction and $U(\theta)$ being the fractional distribution in normalized units. The current will change as:

$$\frac{\partial I}{\partial t} = (I_{final} - I_{initial})(N^{1/3}v)$$

$$= (N^{1/3}v)(qnv)(\int_{\theta_1}^{\theta_2} U(\theta)\cos(\theta)d\theta - 1)$$

where the limits of integration over angle are the range of electron deflection. (22 p 185) The mobility is given by the average velocity seen for a unit charge in a given field; the usual definition is given by:

$$\mu = \frac{v}{E}\frac{q}{-e}$$

Where E is the electric field, q is the charge of the carrier, v is the velocity, and e is the unit electron charge. If we consider instead the decay of charge in a zero electric field possessing a certain amount of energy, we can express the mobility in the form of the Einstein relation:

$$\mu = \frac{qD}{kT} = \frac{q}{m^*}\frac{< v^2\tau >}{< v^2 >}$$ where τ is the relaxation time of the current. (22 p 190)

This explicity separates the diffusivity into the right hand side of the numerator ($D=<v^2 \tau>$) , and expresses the remaining constants in known terms. What remains is to then integrate the current over its scattering profile to determine the diffusivity and thus the net decay. In the case of a collision, the scattering is isotropic. For deflection scattering, the scattering profile depends on the charge on each site, the velocity of the carriers, the average distance between the charge centers, etc (the details are relatively complex). In either case, an increase in the number of charge centers decreases the time between collisions without changing the velocity (which is an intrinsic material property modulated by phonon scattering). It is in this way that the mobility is lowered without a change in the velocity of the charge carriers between the charge centers (which is not materially affected by a small change in the number of scattering centers). The net carrier velocity will, however, be decreased. This is well established in silicon (43).

Mobility Results

The following chart details representative mobilities observed in the experimental samples. The 'Variable' column lists the experimental differences from the control

sample. If one temperature is listed, that was the substrate temperature during the deposition. If two temperatures are listed, the sample was deposited in two steps--one high temperature step and then a room temperature overlayer. The samples which differ in thickness are listed by their deposition times.

Sample name	Variable	Mobility (cm^2/V sec)	Configuration
Control--981104C	24° C	0.16	Electrodes on top
981104A	40° C	0.19	Electrodes on top
981028A	50° C	0.16	Electrodes on top
981119A	60° C	Sample not conducting	Electrodes on top
981104B	40° C + 24° C	0.15	Electrodes on top
981028B	50° C + 24° C	0.14	Electrodes on top
981119B	60° C + 24° C	0.05	Electrodes on top
981119A	5 min (330A)	0.22	Electrodes on top
981119B	5 min (330A)	0.16	Electrodes on bottom
981119C	10 min (650A)	0.25	Electrodes on top
981119D	10 min (650A)	0.13	Electrodes on bottom
981119E	20 min (1,300A)	0.15	Electrodes on top
981119F	20 min (1,300A)	0.03	Electrodes on bottom

Fig. 9--Thickness experiment parameters and data. Data is listed is from saturation region analysis, V_{DS}=-100V, A1 device (1500x64 micrometers)

All samples were prepared with the highest degree of control possible. The samples with the same date were all prepared in the same pumpdown, and the high temperature layers were deposited simultaneously on the same sample puck. The low temperature layers were deposited using a shield over the high-temperature only sample, and a room temperature control was also taken to insure that there were no irregularities in the deposition. All of the timed thickness samples were deposited in the same vacuum

using multiple sample holders. The deposition rate was observed using a quartz crystal monitor and was the same for all of the samples.

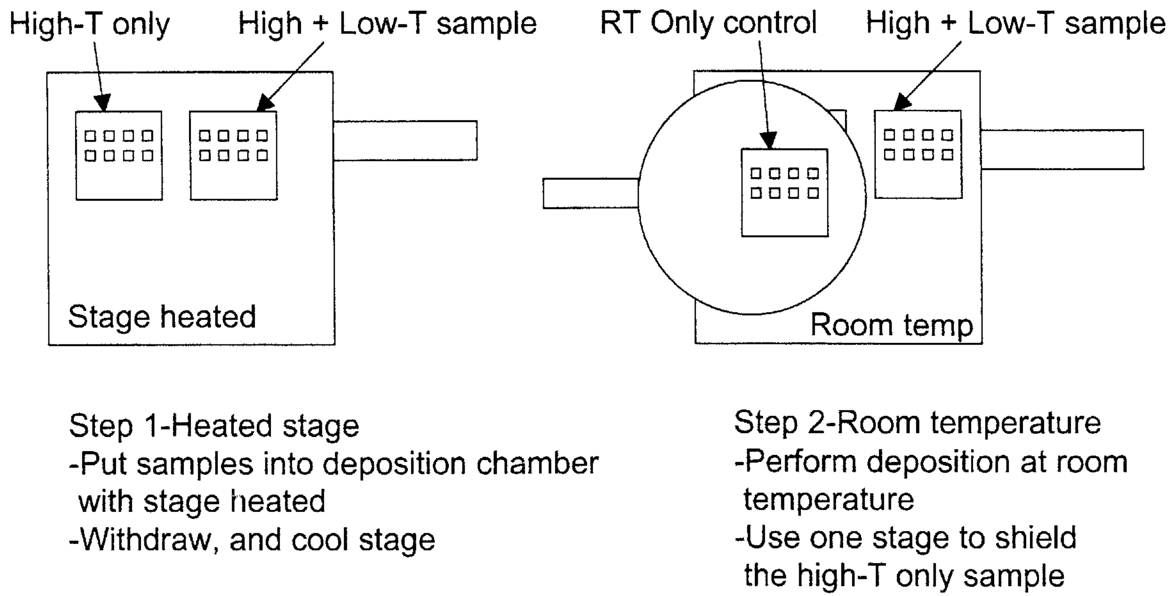


Fig. 10--Diagram showing sample holder layout during deposition of thickness controlled samples.

Several conclusions may be drawn from this data. The first is that there is no significant variation among the samples made at elevated temperatures. Even when tested across four devices on each wafer no large difference is observed among the samples. The 60° sample was not able to be tested due to discontinuity in the active layer. The following SEM clearly demonstrates the structure of the active layer. Because of the relatively high temperature, pentacene atoms were being desorbed from the surface at almost the same rate as that with which they were being deposited. This led to a very thin layer which also clearly shows several phases of the pentacene growth.

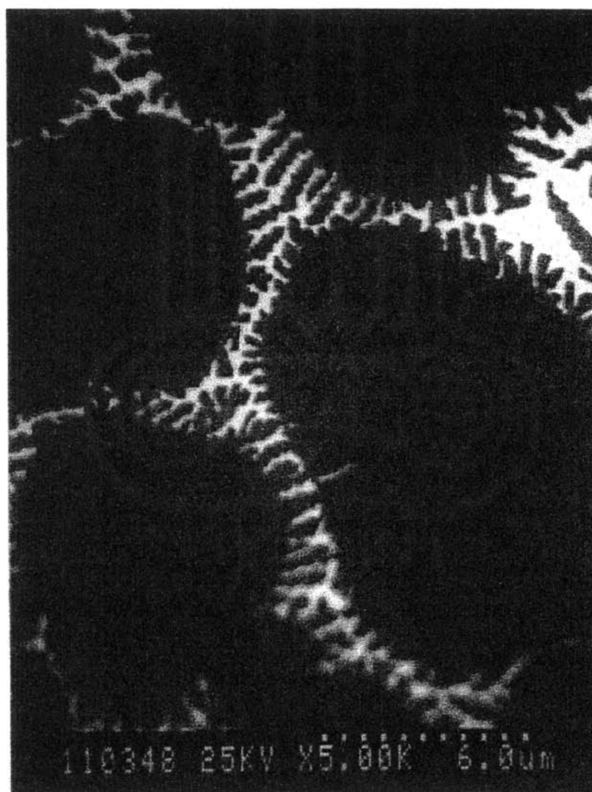


Fig 11--In this micrograph, several phases of pentacene growth may be observed. This film, from sample 981028A, was grown at 50 degrees C on SiO_2. It is somewhat thinned due to the desorption of pentacene molecules from the surface. Very large islands may be seen forming over the thin single-crystal layer, small seed crystallites, and Stransky- Krastanov grains may also be observed growing on the larger islands. This micrograph contains all of the stages of the growth process described in the text.

The idea of using two layers of pentacene was suggested by two papers--one in which amorphous silicon devices were made using two layers, and another in which pentacene devices were made using an almost identical two-layer process (29, 36). Both studies hypothesized that if the first layer was grown carefully the device performance would increase, even if a continuous layer could not be formed in this way. Both studies hypothesized and concluded that only the first few monolayers participate in conduction, and as a consequence only the ordering of these few layers would be significant to overall device performance. This was not found to be the case for this study. It is possible that

these samples were formed at a temperature of unfavorable morphology, or that the temperatures used were not high enough for the better packed single crystal phase to form. The transition between the two phases occurs around 60° C (31).

The thickness samples do, however, show an interesting trend. The first, and most significant, is that the effective mobility of the samples with the pentacene laid on top of the electrodes is much lower for all thickness samples. This is caused by a difference in the morphology in the two cases. Pentacene deposited onto gold forms a highly microcrystalline ordering--there is no driving force for the pentacene to stand up on end since the metal shields the pentacene from dipole forces caused by the SiO_2. Indeed, pentacene has been directly observed to lie down on conducting substrates using STM (23). In the center of the channel the pentacene forms the crystalline structure previously discussed. Near the edge of the channel, however, the microcrystalline organization of the material seen on the electrodes is followed. This leads to two possible effects--an increase in the trap density due to an increase in the grain boundaries, and an increase in the contact resistance. Both would lead to a smaller effective mobility. The following SEM demonstrates this effect.

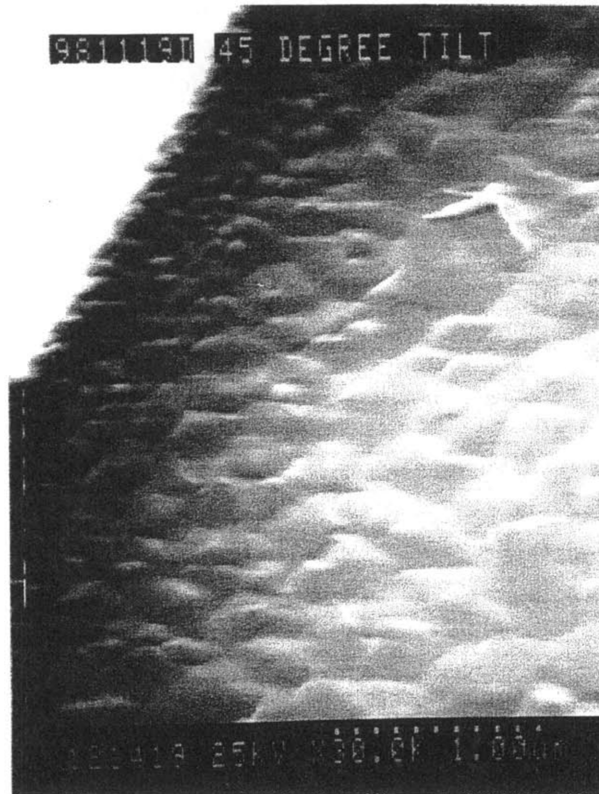


Fig. 12--In this micrograph, the gold electrode onto which the pentacene was evaporated is in the upper left. Towards the right is the center of the chennel, where the pentacene was evaporated onto SiO_2. This micrograph makes clear the small grain region which exists in the channel near the electrode, which is believed to be the cause of reduced mobility and higher contact resistance.

The other trend observed, which has been confirmed by a number of other sample runs, is that that thicker samples (starting over 1000Å) with electrodes on top tend to have a lower mobility as the samples become thicker. This is believed to be because the electrons have to travel through the thickness of the pentacene (which is highly resistive) to reach the active layer during accumulation. The following diagram demonstrates this graphically:

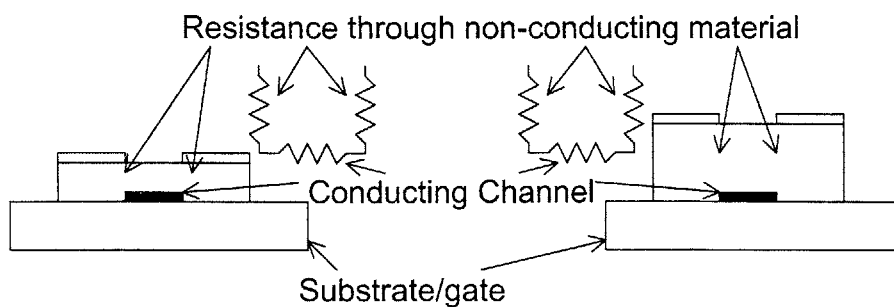


Fig 13--Depiction of the resistance through the pentacene film normal to the substrate

The diagram emphasizes the resistance in the transverse region of the transistor, demonstrating the problem. The samples considered in this study do not span a large enough range of thickness to show this trend. This can only be quantified by looking at a large number of samples to compensate for process variation amongst devices. The quantitative side of this issue will not be addressed in this thesis. It should be noted, however, that this is another reason to use as thin a film as possible in these devices. Another interesting area of research would be to elucidate the transport mechanism normal to the accumulation layer and the effect of process parameters on its performance.

It has been observed before that using a thin layer reduces the parasitic channel conductance without affecting current handling (to a point). Therefore, for a maximum on/off ratio as thin a film as possible should be used (37). Parasitic channel conductance has almost no effect on the mobility, however. While the device is in accumulation the channel sits in parallel to the parasitics and clearly dominates them. The ratio of the channel conductance in accumulation to the parasitic conductance is approximately equal to the ratio of the magnitude of the current in the device at the operational gate voltage to that at zero gate voltage. This exceeds 10^4 in most devices.

Relative trap density

The trap density is a more complex topic than mobility, in particular because of the uncertain nature of the traps in pentacene. It is widely believed, however, that the mobility in pentacene devices is trap limited, and a means of at least ranking the relative trap densities in different devices would be valuable. This section will propose two such systems to measure the relative trap densities using direct electrical measurements, making no reference to the mobility.

There are several types of structures referred to as 'traps.' Recombination and trapped charges will not be addressed here. Instead, the focus will be on mid-gap levels which can capture and scatter carriers traveling through the channel. Some controversy still exists as to their nature (e.g. contrast 12 and 6), but it is generally accepted that there are several states with definite localized energy levels. It is further believed that it is the density of these states which accounts for the variation in mobility among pentacene transistors with different morphologies (32). This study does not analyze enough samples to make any statistically significant conclusions on the link between morphology and mobility. It does propose a method for more directly measuring the relative density of some of these traps.

The following is the model generally used for an MOS capacitor which includes the effect of traps in its performance (38,39):

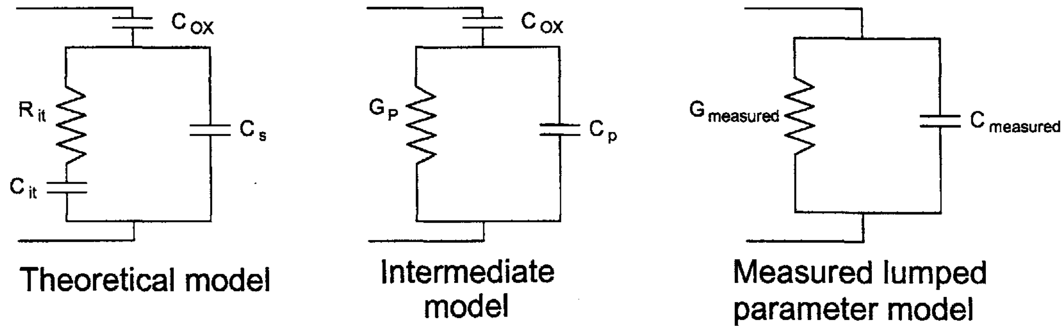


Fig. 14--Lumped parameter models used to mdescribe trap activity in MOS capacitors

C_{ox} is the series oxide capacitance, C_s is the semiconductor capacitance (i.e. the capacitance which appears due to the variation in the depletion depth), and R_{it} and C_{it} are a first order parasitic leg, which represent the effect of the traps in the device. All quantities are assumed normalized.

The RC leg on the left is an approximation, based on the capture/release time constants of all of the different traps. Each individual trap can be modeled as an RC system which determines the time constant, the amount of charge it will capture, and how much energy is lost each time a charge is released. Formally, this may be modeled as:

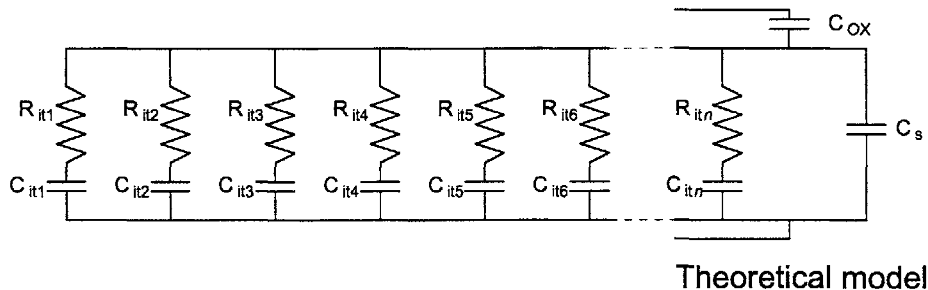


Fig 15--Distributed trap model from which the lumped above are extracted

In this model, each trap may be viewed as having a single capacitance and resistance element associated with it. It is a simple step to see how traps with the same

time constant may be aggregated into individual legs. This system may then be further simplified into the form initially presented by recognizing that the system is still first order, and that the capacitances may be lumped without loss of generality. This leads to a three capacitor system for the MOS-C. The only further complication is that a first order system is measured by the impedance analyzer, so the relationship between the measured parameters and the simplified model must be examined.

It has been demonstrated that the following relationships exist (38):

$$C_p = C_S + \frac{C_{it}}{1 + (\varpi \tau_{it})}$$

$$\frac{G_p}{\omega} = \frac{\varpi G_m C_{ox}^2}{G_m^2 + \varpi^2 (C_{ox} - C_m)}$$

Determining the trap density then follows three steps:

(1) measuring a lumped device

(2) extracting the theoretical model component values from the lumped parameter measurements

(3) correlating the R_{it} and C_{it} with the physical measurements and determining the trap density distribution

Capacitance method

Several attempts have been made to measure the trap density as a function of the MOS capacitor (40, 41). Basically, these techniques make use of the fact that the RC pair that the traps form in the model presented above serves as a low-pass filter.

Measurements made at low frequency can then be correlated with those made at high frequencies and analyzed to determine the value of the RC leg parameters. Some of the variations try to determine the energy of the traps in the distribution. Unfortunately, the high sensitivity of this technique to measurement errors and model of trap distribution used has caused these methods to be subjected to sharp criticism. They retain some value, however for the determination of relative trap values and as a quick method of comparison.

It must be emphasized that even though the density of trap states at the interface is what is most interesting in pentacene, that this is not exclusively an interface trap measurement technique. This will measure traps a short depth into the bulk, up to the edge of the depletion layer. In pentacene this is a nontrivial thickness. The interface trap density can, however, be compared by looking at the relative trap densities at voltages which correspond to the observed threshold voltages. It is at this point that one would expect the edge of the depletion region to be near the surface.

To understand the how the trap centers contribute to an energy loss, consider the following experiment. If a step of charge is instantaneously applied across the MOS-C in depletion, the amount of charge moved would be governed by the density of carriers and the electric field. In particular, the instantaneous capacitance would be given by the familiar formula:

$$C = \frac{\varepsilon}{thickness} \text{ where } thickness = Q/N_p$$

(units normalized to area)

Thickness is the thickness of the depletion region, and N_p is the effective carrier density in the material. N_P is governed by the properties of the material, since it is not extrinsically doped. As time passed, however, the traps in the region affected by the change in charge would start to fill. This would increase the effective N_p by providing additional sites for charge to sit. This would also decrease the thickness of the depletion region, increasing its effective capacitance. The same amount of charge is present in both cases, and the energy given by the capacitor is given by:

$$E = \frac{Q^2}{C}$$

Because the capacitance increases while the charge remains constant there is less energy available after a short wait. This energy goes into heating up the lattice, and is unrecoverable. Capacitance meters typically apply sinusoids to measure the value of the capacitance. The capacitance value measured under those circumstances is that caused by the normal charge sites and the trap centers which are fast enough to populate and depopulate in time. Sweeping the frequency in partial depletion while performing a capacitance test therefore allows different traps to participate. Sweeping at a sufficiently high frequency allows probing of the intrinsic material (assuming the carriers can keep up). Sweeping at a low frequency allows almost every trap site and normal charge site to participate. By measuring the capacitance under these two conditions I have tried to estimate the trap density in the material.

There remains one last consideration--that of the depth of the measurement. This technique can only measure the traps along the depletion surface. Sweeping the bias

voltage used during the measurement allows probing of some of the material bulk by moving the depletion frontier to different areas. As noted before, the density at the interface can be inferred by looking at the trap value when the depletion region is near the surface. This would be the case when the gate voltage is near threshold. In the semiconductor analogy, this situation can also be considered near flatband, since it is at the threshold voltage that the traps are filled and a linear increase in free carriers at the surface may be expected as a function of gate voltage.

The technique finally settled on is a variation on one reported at length in the literature (41). Its most major simplification is that it discards all information about time constants in favor of simplicity and a single number for traps that are slow enough to be measured. The technique begins with the measurement of an MOS device's capacitance at a range of frequencies and bias voltages. -35V-35V and 1000Hz-5MHz was used for this study. The device was also measured both optically and electrically to determine its area, and all measurements were normalized to the area. Next, the capacitance curves were transformed to remove the effect of the oxide capacitance, leaving only the depletion capacitance in parallel with the trap R-C leg. The following formula gives this capacitance (C_p in the above model):

$$C_p = \frac{C_{ox} C_{observed}}{C_{oc} - C_{observed}}$$

Once C_p is established, C_d can be determined by looking at its value at high frequency. The low-pass filter formed by the interface traps blocks the parameter analyzer signal at high frequency and the leg does not appear. C_{it} (the effective interface

trap capacitance) can then be determined by subtracting C_d from the low frequency value of C_p.

A set of typical data is shown below:

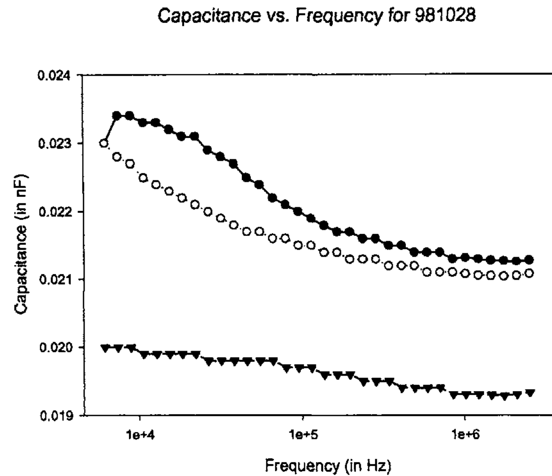


Fig. 16--Typical capacitance frequency curve, showing the characteristic decrease in capacitance as the frequency rises. This effect, not present in control samples, confirms the existence of traps.

Once the capacitance is known the interface trap density can be determined by integrating over voltage through the bias voltage sweep measured. This assumes that the capacitance stays reasonably constant over the step used. It is this part of the procedure that introduces three dimensionality into the calculation. This is because this integration samples information taken at several depths of the material and produces an aggregate trap density which includes some bulk behavior. It is, however necessary to get a quantitative estimate of the trap density. 5V steps were used in this study because of the time needed to obtain each sample set. A typical data integration is shown below:

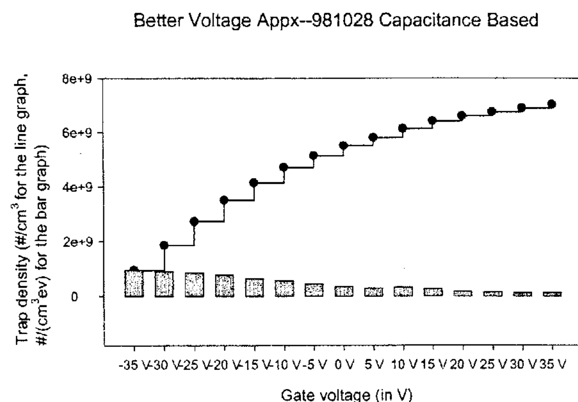


Fig. 17--Typical integration of trap density per unit area per eV to get areal trap density.

There are still limitations to this technique. For example, the depletion area changes in thickness, which affects the voltage drop across the affected pentacene (i.e. the capacitance formed between the top of the depletion layer and the metal electrode). The data was also recalculated to accommodate this effect (this is accounted for in the data set shown above).

Conductance method

Another, more widely used technique for determining the trap density is the conductance method (42). One of its major advantages is that the conductance seen across an MOS capacitor does not depend on the oxide capacitance. This eliminates a major objection to the capacitance method. In most other respects the conductance method is quite similar to the capacitance method. The only additional problem is the need to assume a distribution for the trap states. The actual conductance of the pentacene is immaterial, since no DC current flows through the oxide, and the displacement current flowing is negligible (typically in the fA range).

Each trap state has a characteristic time constant with which it can accept or release a charge. The conductance method relies on the observation of a pole generated by the R-C leg of the MOS capacitor model when the equation is divided by the frequency (to cancel a pesky zero in the numerator). Typical conductance data (in which the conductance is divided by the angular frequency to simplify things) looks like:

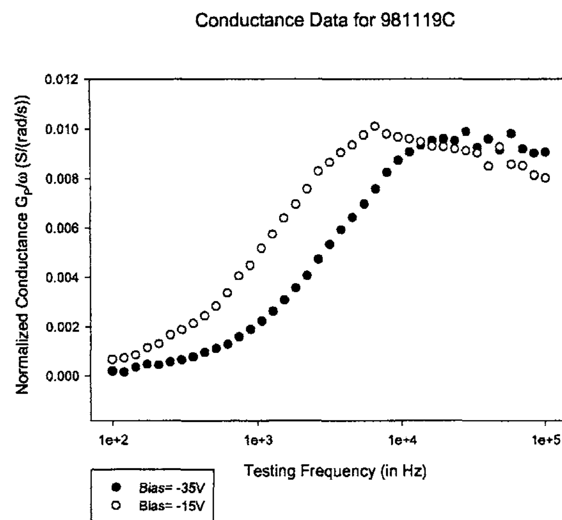


Fig. 17--Typical conductance/frequency curve, showing characteristic peaking

This is plotted on semilog axes to simplify the peak extraction. Once the peak height and width is known, any of several standard assumptions may be made concerning the trap distribution. The data is then fit to the model using the peak location, height, and width. The trap density at that voltage is then determined.

The data sets obtained were analyzed using two trap density distribution assumptions, both of which are based on a Gaussian curve. One assumes a number of parameters (38), whereas the other accommodates additional peak spreading due to potential fluctuations at the surface due to trapped charge, thickness inhomogeneity, or

other effect (38, 39). In the simpler of the two techniques, the interface trap density is given by:

$$D_{it} \approx \frac{2.5}{q}\left[\frac{G_P}{\varpi_{\max}}\right]$$

In the other technique, a parameter is first calculated using the ratio of the magnitude of $\frac{G_P}{\varpi_{\max}}$ to that at either $\omega_{max/5}$ or ω_{max*5}. A set of curves is used to estimate two parameters--σ, the standard deviation of the potential at the surface, and f_D, another correction factor. The analytic relationship is rather complicated and a graphical or numerical analysis is necessary. The trap density is then calculated by (39, 42):

$$D_{it} = \left(\frac{G_P}{\varpi}\right)_{\varpi_{\max}} (f_D(\sigma)q)^{-1}$$

Data

The following chart summarizes the calculated trap densities from -35-35V using the four techniques described earlier, both integrated through -35V-35V and through density at threshold:

Sample	Conductance #1	Conductance #2	Capacitance #1	Capacitance #2
981028A	1.03E+10 cm^{-2}	1.29E+10 cm^{-2}	2.07E+10 cm^{-2}	7.02E+09 cm^{-2}
at threshold			2.39E+09 cm^{-2}ev^{-1}	7.69E+08 cm^{-2}ev^{-1}
981030A	7.92E+10 cm^{-2}	9.40E+10 cm^{-2}	3.49E+11 cm^{-2}	2.03E+10

				cm^{-2}
at threshold			6.16E+10 $cm^{-2}ev^{-1}$	1.88E+09 $cm^{-2}ev^{-1}$
981104A	2.03E+10 cm^{-2}	2.47E+10 cm^{-2}	1.20E+11 cm^{-2}	1.04E+10 cm^{-2}
at threshold			1.17E+10 $cm^{-2}ev^{-1}$	8.33E+08 $cm^{-2}ev^{-1}$
981106A	2.14E+10 cm^{-2}	2.30E+10 cm^{-2}	5.74E+10 cm^{-2}	9.65E+09 cm^{-2}
at threshold			7.13E+09 $cm^{-2}ev^{-1}$	8.54E+08 $cm^{-2}ev^{-1}$
981111A	9.38E+08 cm^{-2}	9.76E+10 cm^{-2}	7.08E+09 cm^{-2}	1.31E+10 cm^{-2}
at threshold			5.01E+08 $cm^{-2}ev^{-1}$	8.93E+08 $cm^{-2}ev^{-1}$
981119A	3.33E+10 cm^{-2}	3.22E+10 cm^{-2}	1.94E+11 cm^{-2}	1.41E+10 cm^{-2}
at threshold			2.24E+10 $cm^{-2}ev^{-1}$	1.40E+09 $cm^{-2}ev^{-1}$
981119C	2.88E+09 cm^{-2}	3.12E+09 cm^{-2}	4.53E+09 cm^{-2}	4.85E+09 cm^{-2}
at threshold			6.39E+08 $cm^{-2}ev^{-1}$	5.81E+08 $cm^{-2}ev^{-1}$
981119E	1.85E+10 cm^{-2}	1.50E+10 cm^{-2}	6.21E+09 cm^{-2}	4.60E+09 cm^{-2}
at threshold			4.21E+08 $cm^{-2}ev^{-1}$	3.12E+08 $cm^{-2}ev^{-1}$

Where conductance #1 is the Nicollian-Goetzberger method which compensates for the field inhomogeneity on the surface (which was small for almost all samples), conductance #2 is the approximate conductance method, capacitance #1 blindly integrates assuming all of the gate voltage falls across the trap capacitance, and capacitance #2 uses the depletion capacitance value known to determine the voltage drop across the trap capacitor.

While there is significant variation between values for the same sample, there is one remarkable result when the samples for each experiment are ranked according to trap density:

Thickness variation ranking (lowest number is smallest density):

		Cond #1	Cond #2	Cap #1	Cap #2
981119A	Thickest	3	3	3	3
981119C	Medium	1	1	1	2
981119E	Thinnest	2	2	2	1

Temperature variation:

		Cond #1	Cond #2	Cap #1	Cap #2
981119C	24 °C	1	1	1	1
981028A	50 °C	2	2	2	2
981030A	60 °C	4	4	4	4
981104A	40 °C	3	3	3	3

The consistency across the two major techniques indicates that the measurements may have promise as a relative measure of trap density. Correlating these measurements to morphology or deposition conditions, however, may prove substantially more difficult. The small sample set used here would not allow any definitive conclusions in any case, but explaining why the 50 °C sample, for example, has a higher trap density than the room temperature sample may prove difficult. Clearly more study of a wider temperature range is needed.

It was noted earlier that the surface may be probed by looking at the charge density near threshold. This was done for each device using the capacitance and method. The rankings of charge densities at threshold and overall charge densities are identical.

Improvement of a device using a high-K dielectric

Trap states which can capture charges lie inside the frontier levels of the material. It follows, therefore, that they cause the greatest number of problems when they are not filled but lie near the Fermi level. It follows that when the Fermi level is drawn above the trap levels they fill and the electrons can pass through unimpeded.

A variation of mobility with gate voltage had been observed in organic semiconductors in the past (28). No direct observation of the variation against the field strength was tested, however, until recently.

A major criticism of organic semiconductors to date has been their need for large operating voltages to achieve high mobilities. A review of the literature indicates that almost all reports of high mobilities are taken at -100V gate bias (which is the highest voltage a popular metrological instrument, the HP 4145B will produce). Without a clear understanding of the nature of this trend, however, it was not clear how the operating voltage would be reduced.

If the mobility variation was caused by a barrier at the electrodes, then the gate field would not be significant, but the voltages used in the drain-source field would. By using a variety of dielectrics with high dielectric constants it was possible to demonstrate that the mobility observed was almost precisely a function of the electric field at the interface for a number of dielectric materials. The following diagram demonstrates the trend of mobility vs. electric field for a number of dielectric materials:

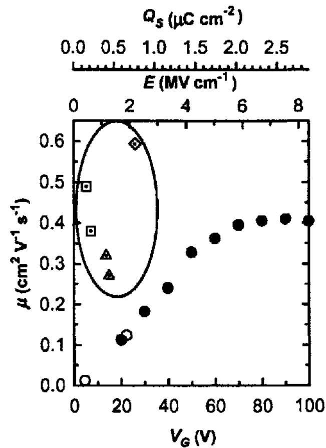


Fig. 18--Mobility dependence on electric gate field. The points are all plotted against the electric field strength on the x-axis, shown on the top labels. The bottom labels represent the gate voltage needed to achieve this field with a 5000A oxide. This voltage scales down linearly with increased gate capacitance. The open and closed circles (many of which overlap) are 5000 and 1000A oxides, respectively. The other symbols represent other dielectric systems.

(figure from 12) The circles (both filled and open) represent various thicknesses of SiO_2. Triangles represent BZT, squares, BST, and diamonds Si_3N_4.

The experimental evidence from a set of BZT samples will be presented here. The mobility observed from a representative sample is shown below:

Sample	Insulator	Mobility	Voltage tested	Threshold	Max current
980604A	BZT 1280A	0.13	5V	0V	$8*10^{-6}$ A
971023B	BZT 1220A	0.27	14V	-5V	$2*10^{-4}$ A

Figure 19--Data from high dielectric constant samples

This process has produced the highest performance organic TFT at low voltages to date (12). The protocol followed for these samples is almost identical to that normally used. For the BZT samples a platinum gate with a Ti adhesion layer was deposited onto polycarbonate using e-beam evaporation through a molybdenum mask. The BZT was

then sputtered at room temperature. The characteristics for the polycarbonate sample (980604A) is shown below, as is a picture of the device:

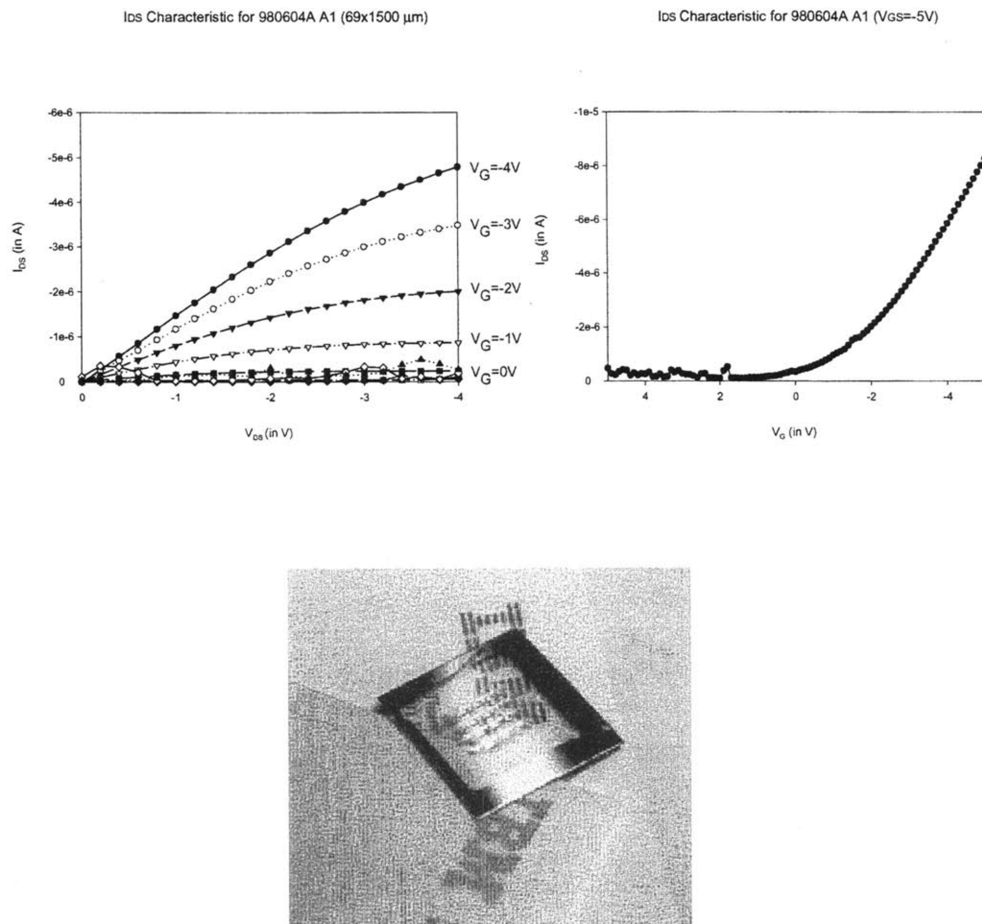


Fig. 20--Pentacene on BZT on polycarbonate device--photograph and characteristic curves.

These samples indicate the achievement of the aforementioned goal--to attain high mobility at low operating voltages. The effect of the extra gate capacitance is the same as applying an increased voltage. More carriers are drawn to the accumulation surface in the high-K samples than the control samples, and the traps are thus saturated earlier. The scattering from the traps is reduced, and the carriers are free to travel through the

semiconductor with greater ease. This is observed macroscopically as a higher effective mobility.

This experiment also provides additional evidence explaining the nature of the traps in pentacene. That some traps can be passivated indicates that many of the significant scattering sites are charged. It also implies that the mobility limitation observed is not source-drain field dependent. If this can be confirmed through further experiment it would indicate that trapping and release, and not electrostatic scattering (which is velocity and therefore source-drain field dependent), is the dominant carrier impediment. This could lead to additional information about the nature of traps in pentacene and how to passivate them.

Analysis of benefit to circuit performance

Logic Circuit Example

The benefit of using a higher dielectric constant material is not a priori clear. Increased gate capacitance may under some circumstances be a liability and slow device performance. The next section will demonstrate that even without a mobility change the use of such a dielectric will not be detrimental to the performance of a simple circuit. I will then further demonstrate that because of the mobility gain there is a definite performance improvement available from such a process.

The first circuit which will be considered is a ring oscillator:

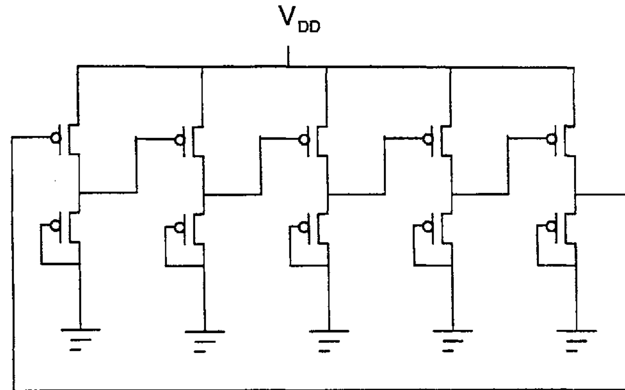


Fig 21--Representative PMOS ring oscillator circuit

The oscillation frequency of a ring oscillator is governed by the switching time of the inverters and their ability to drive the next load. The number of inverters over three does not play a significant role. While in the 'output low' state, the current output of an inverter is governed by the current carrying capability of the diode-connected transistor. This is given by

$$I_{outlow} = \frac{W_2}{L_2}\mu C_{ox}\left(\frac{V_T^2}{2}\right).$$

with W_2 and L_2 the dimensions of the diode-connected transistor. For this section C_{ox} is the normalized gate capacitance and other capacitances are regular, absolute values. V_{DS} of the diode connected transistor equals the threshold voltage through feedback in the circuit. The current handling capability of the 'output high' state is given by:

$$I_{outhigh} = \frac{W_1}{L_1}\mu C_{ox}((V_{dd} - 2V_T)V_T - \frac{V_T^2}{2}) - \frac{W_2}{L_2}\mu C_{ox}(V_{dd} - 2V_T)^2$$

neglecting any body effect. The basic effect is that the current carrying capability scales linearly with the gate capacitance. This bodes well for the switching time. For devices with the same dimensions, the load on the next stage also scales linearly with the capacitance. The switching time constant is given by:

$$\tau_{switching} = R_{out} C_{in}$$

Where R_{out} is the output resistance of the inverter, and C_{in} is just the area of the input gate times C_{ox}. R_{out} is just $\frac{\partial V_{out}}{\partial I_{out}}$. Since this is a first order system, a simple way to determine the magnitude of the time constant is by assuming no parasitic gate resistance and approximate the transistor as a current source. Using the current drive and gate capacitance together we find:

$$Q = CV = It$$

$$\frac{\partial V}{\partial t} = \frac{I}{C}$$

$$\tau_{charging} = \left(\left(\frac{\partial V}{\partial t}\right)_{t=0}\right)^{-1} (V_{dd})^{-1} = \int_0^{V_{smalll}} \frac{C}{I} dv$$

It is this $\tau_{charging}$ which determines the switching time in the circuit. Written explicitly for the output off condition:

$$\tau_{charging} = \left(\left(\frac{\partial V}{\partial t}\right)_{t=0}\right)^{-1} (V_{dd})^{-1} = \frac{C}{I V_{dd}} = \frac{C_{ox} W_1 L_1}{\frac{W_2}{L_2} \mu C_{ox} (\frac{V_T^2}{2}) V_{dd}} = \frac{W_1 L_1}{\frac{W_2}{L_2} \mu (\frac{V_T^2}{2}) V_{dd}}$$

Because it depends only on I and C, both of which increase linearly with the gate capacitance for the turning on and turning off condition, the effect of the increased gate capacitance cancels. To first order, the value of the gate capacitance has no effect. In practice, where the parasitic capacitance is much larger than the gate capacitance, the benefit of the increased gate capacitance on speed is even more pronounced.

There is a second order effect which should be noted here. Because the mobility is increased when the higher gate capacitance is used, the switching time decreases. μ appears only in the denominator of the charging time constant. It is therefore unequivocal that the increased gate capacitance is beneficial to logic circuits of this type regardless of the magnitude of other circuit parameters.

This representative circuit example shows that the increased gate capacitance is not a liability in circuits when the device dimensions, material parameters, and supply voltages are held constant. Even though there is an extra delay in charging the transistor, this is compensated for through increased current through the semiconducting layer. This means that there will be some additional power loss, but no extra circuit delays. Normally, because of the increased power loss, this would be undesireable. The increased mobility, however, improves circuit performance is both cases illustrated above. This improved material performance also offers designers the opportunity to resize the circuits to occupy less area or trade some of the additional speed for power consumption.

Conclusion

Organic semiconductor technology, while still in its infancy, has promise for the future. It provides a number of the design requirements needed for low cost displays and several other applications. Advances are still needed in the areas of processability, reproducibility, and metrology for these materials. This thesis presents some attempts to advance the processing and metrology of pentacene. An attempt to vary the morphology of the material through temperature variation was made. A variation in the contacts was made. A modified technique based on previous work and a standard silicon technique were applied to measure the relative trap densities of the materials. Several parameters were observed--morphology, mobility, and trap densities.

Several conclusions can be drawn from this study. While no strong link was found to temperature for any properties, it was demonstrated that the mobility depends heavily on the morphology near the contacts. It is therefore preferable to deposit pentacene onto SiO_2 than onto a metal such as Au. It was also demonstrated that two methods of measuring the trap density produce consistent results. This indicates that it may be possible to directly electrically measure the trap densities in pentacene.

Several additional studies are suggested by this work. One is to study the morphology of the pentacene while varying process parameters. It has been shown that superior morphology improves the device performance (32), but only temperature has been studied as a varied parameter. Coupled electrical measurements, SEM or AFM micrography, and x-ray analysis can provide additional insight to the morphology characteristics which affect performance.

Attempts to seed the pentacene crystal by using a progressively larger array of mask sets can also be tried. This would permit the growth of larger grains than would

form naturally by permitting growth only near regions already oriented by preexisting pentacene. If successful, this would permit the probing of a macroscopically single-crystal pentacene.

Finally, a theory of conduction was developed. To test and apply this idea, devices employing a different dielectric were used to increase the effective device mobility. A mechanism for this mode of operation was presented. This is based on work published in Dimitrakopoulos, *et al.* (12). It was also demonstrated using two test circuit cases that the use of a high dielectric constant insulator in the transistors does not provide a speed penalty despite the increased gate capacitance. This is important if this technology is to be applied to logic or control applications.

Organic materials posses great promise and mystery. It is through a greater understanding of their properties and processing that we will be able to use them effectively in applications. Their unique properties and problems provide a fertile area for further research, and a large potential for novel and profitable applications.

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