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Monolithic III-V/Si Integration

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Abstract

We summarize our work on creating substrate platforms, processes, and devices for the monolithic integration of silicon CMOS circuits with III-V optical and electronic devices. Visible LEDs and InP HBTs have been integrated on silicon materials platforms that lend themselves to process integration within silicon fabrication facilities. We also summarize research on tensile Ge, which could be a high mobility material for III-V MOS, and research on an in-situ MOCVD Al₂O₃/GaAs process for III-V MOS.

Introduction

Monolithic III-V/Si has been a long-term dream for the semiconductor industry. At first, the concept began as a simple notion that the best features and utility of III-V materials and devices could be married to the benefits of silicon manufacturing. Its modern incarnation has evolved from interest in helping an integrated system in silicon continue to miniaturize with increased performance benefit.

Although the challenge of monolithic III-V/Si began as a technical investigation of GaAs epitaxy on silicon substrates, technical solutions must be considered in the context of manufacturing paths to viable short, medium, and long term applications.

To that end, we describe our foci of research in monolithic III-V/Si integration in the context of technical materials challenges, incorporating solutions into substrate platforms that allow for silicon process integration and manufacturing, and producing monolithic III-V/Si devices that have viability in short-term and long-term applications.

Monolithic III-V+Si CMOS

III-V devices have found important applications in electronic systems, and silicon CMOS is the driver of digital electronics. Thus, in III-V+Si CMOS, our goal is to combine the benefits and strengths of III-V devices with silicon CMOS where monolithic design brings the greatest benefit to the integrated circuit.

We have designed a substrate material, which we term silicon on lattice engineered substrate (SOLES), to allow the co-integration of III-V devices and silicon crystalline template devices in a silicon design and processing environment.[1] SOLES consists of a silicon substrate upon which a III-V crystalline template is created, followed by a surface silicon layer. Thus, a template for III-V growth is inserted into the middle of a silicon sandwich. In the first fabrication of such a platform, we have used Ge as the template material. Fig. 1 is a transmission electron microscope cross-section of a second-generation SOLES platform with Ge inserted as the III-V template. The first version of SOLES uses a Si/SiGe/Ge graded structure instead of the Si/SiO₂/Ge structure shown in Fig. 1.

Figure 1: XTEM of a SOLES substrate with an embedded Ge template

The SOLES substrate is quite flexible in that the buried template can be composed of any material that can be produced metamorphically on a large silicon substrate. For example, graded composition SiGe layers can be used to create a surface Ge layer on silicon. A thin layer can be transferred to a silicon substrate using exfoliation and silicon dioxide as the bonding material, which forms the bottom of the SOLES structure as seen in Fig.1. A silicon surface layer is added through a similar process.

The advantage of this substrate design is that it eases process integration for III-V+CMOS circuits.

The wafer is easily accepted by a silicon fabrication facility, as the surface is silicon and the substrate is silicon; thus, the wafer is a silicon wafer from a fab perspective. Also, the entire front-end of the silicon CMOS process can be executed first on a planar substrate. After the front-end is complete, areas that require III-V devices will be etched to expose the Ge, where III-V epitaxy can occur. After III-V device processing, the structure can be designed such that the back-end vias to both the silicon and III-V devices can be co-planar, an important feature for utilizing leading-edge back-end silicon technology.

We have fabricated visible III-V LEDs on the SOLES substrates to test their viability for integrated optoelectronics.[2] Fig. 2 is a TEM cross-section of a read AlInGaP LED grown lattice-matched to the Ge template layer in a SOLES substrate.

Figure 2. Cross section TEM micrograph of the p+Si/AlInGaP LED grown in a window formed on the SOLES substrate.

Figure 3. Optical micrograph of an operating visible

LED in the SOLES substrate window area. Silicon contact metallurgy was used for the LED contact. The edge of the window cut into the SOLES can be seen at the edge of the micrograph.

A window was etching through the top silicon layer and SiO₂ layer to expose the Ge template. Note that the entire structure was grown and terminated in the same epitaxial run with p+-Si. The reason for this final silicon cap (in an MOCVD machine that supports both silicon-germanium precursors as well as III-V precursors) was to show that ohmic contacts could be fabricated with silicon-based metallurgical contacts. Fig. 3 is an optical micrograph of the “Si LED” in operation, and light put from the LED on SOLES is higher than that on a control GaAs substrate, most likely due to an optical effect from the multilayered SOLES substrate.

To test III-V electronic devices on the SOLES, or more specifically, GeOI (the bottom half of the SOLES), and to prepare the module for full process integration sequence with CMOS, the Raytheon-Paradigm-MIT-Teledyne-IQE-SOITEC team has fabricated InP HBTs on GeOI and SOLES. InP HBTs have very high frequency performance, and integration with silicon CMOS would allow for novel analog-mixed signal circuits in which I/O can utilize very high frequency InP HBTs, with slower digital circuitry performed in trailing-edge silicon CMOS. InP HBTs have an even larger lattice on silicon, and therefore a metamorphic III-V layer must be deposited on the Ge template to shift the lattice to InP.

Figure 4. Cross-section TEM of a InP HBT on a GeOI substrate. Note the lack of threading dislocations in the InP HBT. The metamorphic AlInAs can be seen as the dense network of dislocations above the GaAs.

Fig. 4 is a TEM cross-section showing the InP HBT epitaxy on the GOI platform. Note the lack of threading dislocations in the relatively low magnification

cross-section, revealing that the threading dislocation density must be less than 10^8 cm^{-2} . Regarding electrical performance, the Gummel plot overlaying control InP HBT with the InP/GeOI HBTs shows that gain is nearly identical. Fig. 5 is a plot of gain vs. frequency, revealing a f_t of 224GHz and a f_{max} of 219 GHz. Using models from silicon MOSFETs and these InP HBTs, we are now moving forward with the full monolithic process to fabricate COSMOS (compound on silicon MOS).

Figure 5. Gain vs. Frequency for the InP/GeOI HBT.

III-V MOS

As opposed to III-V+Si CMOS, III-V MOS aims to incorporate III-V material into the channel of a MOSFET, creating a new device. III-V MOS is a new device since there are several challenges in creating a non-silicon MOS device. The purpose is to create a channel with very high electron mobility such that MOSFET drive currents can continue to scale properly as gate length shrinks. If III-V MOS is to be used for all devices on the substrate, then the SOLES platform is not needed. However, a good compromise between decreasing band gap and increasing mobility, as lattice constant is increased in the III-V materials, is InGaAs.

We have used the Ge-on-insulator (GOI, the bottom of the SOLES structure in Fig. 1) platform to create relaxed InGaAs with lattice constants as large as the lattice constant of InP. This relaxed large lattice on silicon was accomplished by compositionally grading III-V materials on the GOI substrate. The GOI substrate is necessary as it removes the thick engineered SiGe layer that is used to achieve high quality Ge on silicon. The reason the thickness must be removed is that graded III-V layers introduce more thickness such that both graded layers on a silicon substrate would create too much thermal stress, leading to film cracking.

Another key problem to solve for III-V MOS is to

create a dielectric/III-V interface that can be easily manufactured. We have achieved interface defect densities at a dielectric/GaAs interface as low as $2 \times 10^{11} \text{ cm}^{-2}$ using an in-situ MOCVD process for Al_2O_3 gate dielectric deposition. An in-situ MOCVD process is desired since it is easily manufactured and also minimizes contamination problems since the gate dielectric can be deposited in-situ after channel deposition and monolayer control of the dielectric/channel interface. Fig. 6 is a plot of CV output as a function of various frequencies, revealing a relatively low degree of dispersion for dielectric/III-V interfaces.

Figure 6. C-V curves from MOS capacitors created from an in-situ $\text{Al}_2\text{O}_3/\text{GaAs}$ process introduced in an MOCVD reactor. There is relatively low dispersion.

Besides III-V channels, highly strained tensile Ge is predicted to have very high hole and electron mobility, a good candidate for future MOS. With the larger InGaAs lattice on silicon mentioned above, we have also been able to deposit planar tensile biaxial Ge. In-situ monolayer control in MOCVD for initiating Ge on InGaAs was also required (as in the Al_2O_3 result) in order to achieve planar tensile Ge films.

Applications

The nature of monolithic III-V/Si applications that can actually drive III-V/Si CMOS into the marketplace is as critical as the technological feats we have accomplished. We speculate that analog-mixed signal applications are a likely candidate for III-V+Si CMOS, and that die size must start small and using trailing-edge silicon fabrication facilities. This strategy leads to a financially solvent path that can grow die size and wafer volume over time, eventually leading to state-of-the-art Si CMOS integration with III-V electronic and optical devices.

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