Two-Dimensional Materials for Electronic Applications

by

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ABSTRACT

The successful isolation of graphene in 2004 has attracted great interest to search for potential applications of this unique material and other members of the two-dimensional materials family in electronics, optoelectronics and their interface with the biological systems. At this early stage of 2D materials research, many opportunities and challenges co-exist in this area. This thesis addresses the following issues which are crucial for 2D electronics to be successful, focusing on developing graphene for RF electronics and MoS_2 for digital applications: (1) Development of some of the first graphene-based devices for high frequency applications; (2) Development of compact physical models for graphene transistors; and (3) Understanding the carrier transit delays in graphene transistors. In addition, this thesis proposes and experimentally demonstrates a completely new concept - Ambipolar Electronics - to take advantage of the unique properties of graphene for RF applications. Based on this new concept, a family of novel applications are developed that can significantly simplify the design of many fundamental building blocks in RF electronics, such as frequency multipliers, mixers and binary phase shift keying devices. In the last part of the thesis, the applications of other emerging 2D materials from the transition metal dichalcogenides family, such as molybdenum disulfide (MoS_2), is also explored for potential application in digital electronics, especially as a new material option for high performance flexible electronics. The future opportunities and potential challenges for the applications of the 2D materials family are also discussed.

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Chapter 1. Introduction

1.1. History of Two-Dimensional Crystals Research

It has been eight years since the first electrical characterization of graphene, a material consisting of a single layer of sp^2-bonded carbon atoms arranged in a honeycomb lattice [1][2]. Thought to be an impossible goal for many decades, its successful isolation in 2004 not only led to intensive research by physicists and chemists but also inspired renewed interest in carbon-based electronics from device engineers and circuit designers around the world [3][4]. Rapid progress has been made in the past few years to develop applications for graphene. Many interesting ideas have been demonstrated in the laboratory setting and some attractive products may emerge at the industrial scale in the coming years. Some of the promising applications include RF electronics [5][6][7][8], advanced sensors [9], semitransparent electrodes and electronics [10], low power switches [11], solar cells [12], battery energy storage [13], and tunable plasmonic devices for THz and mid-infrared applications [14][15].

In addition to its unique properties, it should be highlighted that graphene is only the beginning of an emerging 2D materials family. 2D materials, such as molybdenum disulfide (MoS_2) [16] and other members of the transition metal dichalcogenides family, represent the ultimate scaling of the material's dimension in the vertical direction. Nano-electronic devices built on 2D materials offer many benefits for further miniaturization following Moore's Law [17][18] and as a high-mobility option in the rising field of large-area and low-cost electronics that is currently dominated by low-mobility amorphous silicon [19] and organic semiconductors [20][21]. MoS_2, a 2D semiconductor material, is also attractive as a potential complement to graphene [5][6][22] for constructing digital circuits on flexible and transparent substrates, while its 1.8 eV bandgap as measured by photoluminescence [23][24], and potentially even a higher electronic bandgap due to the excitonic energy, is advantageous over silicon for suppressing the source-to-drain tunneling at the scaling limit of transistors [25]. Recently, various basic electronic components have been demonstrated based on few-layer MoS_2, such as field-effect transistors (FETs) [26][27][28], sensors [29] and phototransistors [30]. For engineers, 2D materials offered a new dreamland for creation and innovation. The unique properties of 2D materials have attracted

intense research activities to take advantage of this new material system for improving existing electronic, optoelectronic and sensing applications and inventing new ones.

For a long time, the research community thought that strictly two-dimensional (2D) crystals may not exist [31][32]. Theorists predicted in the first half of the last century [33] that a low-dimensionality crystal would mostly likely disintegrate at any finite temperature due to large displacement of lattice atoms resulting from diverse sources of thermal fluctuations. The typical amplitude of such displacements was predicted to be on the same order as the inter-atomic distance of the material. Mermin expanded this theory in a later publication [34] and the argument was overwhelmingly supported by experiments that followed, a key evidence being the experimental observation that the melting points of thin film materials rapidly reduce with decreasing film thickness [35][36]. This seemingly solid understanding of atomic monolayers led to the long-standing belief that such materials can only be epitaxially grown on top of bulk single

(a)   (b)
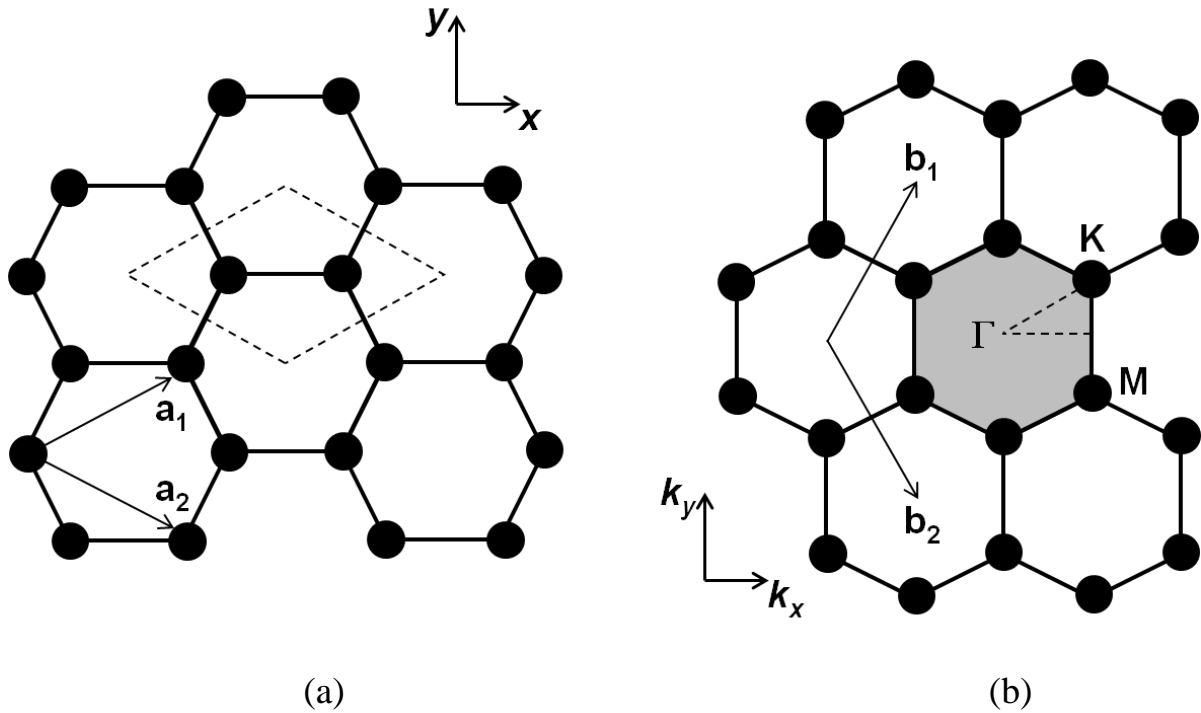
Figure 1-1 The lattice and reciprocal lattice structure of monolayer graphene (a) Lattice structure of monolayer graphene. (b) The reciprocal lattice of monolayer graphene. The dotted rhombus in (a) and the shaded hexagon in (b) are the unit cell and Brillouin zone of monolayer graphene. a_i (i=1,2) are the real space unit vectors and b_i (i=1,2) are the reciprocal lattice vectors. Γ, K and M are the high symmetry points in the 2D reciprocal lattice.

crystal substrates with a matching crystal lattice, but cannot exist in their free-standing form. This common belief stood almost unchallenged until 2005, when Novoselov et al. [1] and Zhang et. al. [2] published the experimental discovery of isolated graphene and subsequently other 2D atomic crystals, such as hexagonal boron nitride, niobium diselenide and molybdenum disulfide [37]. Although there have been other independent reports of monolayer carbon materials isolation [38][39][40][41], some even long before the reports from Novoselov et. al. and Zhang et. al., it is the works in 2004 and 2005 that have clearly elucidated its unusual electronic properties and generated the worldwide effort in exploring both the fundamentals and the new applications of these materials.

Reports on the synthesis of monolayer and few-layer graphene date back to the 1960s in the early work of Boehm through the reduction of graphene oxide [38]. In Boehm's study, X-ray diffraction, the thickness of these layered materials, and the specific surface areas of these films were characterized. Other methods for preparing mono-layer and few-layer graphene became available in the years that followed, including approaches based on graphite intercalation compounds (GICs) [42][43][44][45][46][47][48][49][50][51][52][53], methods based on the mechanical exfoliation of few-layer flakes from bulk-like materials [54], techniques using the vacuum graphitization of SiC by the group of Walt de Heer [55], and more recently large scale synthesis of graphene by chemical vapor deposition methods [56][57]. In 2004 and 2005, Novoselov et al. and Zhang et al. successfully isolated few-layer, and later single-layer, graphene using the mechanical exfoliation technique and elucidated some of its key physical properties and phenomenon. This discovery marked the real beginning of the efforts in exploring both the physics and applications of graphene as well as other members of the 2D material family. Since then, we have seen an exponential increase in the research activity in graphene and related 2D materials, leading to enormous progress in developing both fundamental understanding and new applications. While this thesis focuses mainly on the later, we start in the next sub-section in reviewing some of the basics properties of graphene and other 2D materials.

1.2. Basics of 2D Materials

1.2.1. Electronic Properties of Graphene

Graphene is made of sp^2 hybridized carbon atoms arranged in a hexagonal honeycomb lattice [3]. The sp^2 hybridization between the s-orbital and two p orbitals lead to a trigonal planar structure with a formation of σ bond between carbon atoms. Figure 1-1 shows the lattice structure of graphene. The unit cell of graphene lattice consists of two carbon atoms A and B shown inside the dotted rhombus in Figure 1-1(a). In Cartesian coordinates, the real space unit vectors $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ can be expressed as:

$$\boldsymbol{a_1} = \left(\frac{\sqrt{3}}{2}a, \frac{a}{2}\right), \qquad \boldsymbol{a_2} = \left(\frac{\sqrt{3}}{2}a, -\frac{a}{2}\right)$$

(1-1)

where the lattice constant of single-layer graphene is $a = |\boldsymbol{a_1}| = |\boldsymbol{a_2}| = 1.42 \times \sqrt{3} = 2.46$ Å. Figure 1-1(b) shows the reciprocal space of graphene. The shaded region represents the reciprocal space unit cell, which can be described by reciprocal lattice unit vectors $\boldsymbol{b_1}$ and $\boldsymbol{b_2}$:

$$\boldsymbol{b_1} = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{a}\right), \qquad \boldsymbol{b_2} = \left(\frac{2\pi}{\sqrt{3}a}, -\frac{2\pi}{a}\right)$$

(1-2)

with a reciprocal space lattice constant equal to $\frac{4\pi}{\sqrt{3}a}$. The reciprocal space unit cell vector $\boldsymbol{b_1}$ and $\boldsymbol{b_2}$ are rotated from real space unit vectors $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ by 30°. K and Γ are the corner and the center of the hexagon in Figure 1-1(b) while M is the mid-point of the edge in the shaded Brillouin zone.

The σ-bonds in graphene arise from the sp^2 covalent bonding between neighboring carbon atoms. In monolayer graphene, three of the four valence electrons hybridize in an sp^2 configuration to form the strong σ bonds while the last electron of the carbon atoms forms the half-filled $2p_z$ orbital normal to the plane of hexagonal carbon lattice, resulting in π covalent bonds. There are three atomic orbitals of sp^2 covalent bonding for each carbon atom, $2s$, $2p_x$, and $2p_y$. The strong σ bonds are the main reason for the mechanical strength and structural robustness of the lattice structure in carbon allotropes. Governed by the Pauli principle, these

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lower energy levels form a deep fully filled valence band. These strong covalent bonds make graphene the thinnest, and yet the strongest material ever measured, being at least five to ten times stronger than steel [58][59]. On the other hand, the *p*-orbital are perpendicular to the planar atomic lattice. The *p*-orbital from neighboring carbon atoms can bind covalently to form the electronic π band. These half-filled π bands to a great extent define the physical properties of strongly correlated system, and are responsible for the carrier transport properties of graphene. Based on modern band-structure studies of graphene, the material demonstrates typical properties as a semimetal. The electronic excitations however exhibit a unique linear dispersion with properties resembling "relativistic" particles. The conduction band and the valence band in pristine graphene meet at a single point around which the wave functions of electrons are described by the Dirac equation. This band-structure description is supported by most existing experimental data.

The basics of the π–band structure of graphene can be understood using a simple tight-binding model [60][61]. The model, which is justified due to graphene's strong in-plane bonding between carbon atoms, is sufficient for explaining many physical phenomena in graphene and provides good approximations in describing its π–bands for many practical purposes. Here, a simple version of the model will be derived to help understand the electronic band structure of graphene at low excitation energies. A more detailed derivation of the tight-binding model for sp^2 bonded carbon atomic lattice can be found in the literature [3][60][61].

Under the tight-binding theory, the electrons are assumed to be tightly bound to their respective host atoms. The interactions between the electrons and the neighboring lattice atoms are assumed to be very weak. Under this assumption, the unperturbed eigenfunctions of the Hamiltonian of a single isolated atom are represented as atomic orbitals, and the crystalline potential as perturbations, leading to the Bloch state representation of the electronic states. The basis functions for describing the electronic structure of single-layer graphene relies on the two Bloch functions Φ_A and Φ_B derived from the p_z orbital of the two carbon atoms at A and B sites (Figure 1-1). A 2×2 Hamiltonian matrix $H_{ij} = \langle \Phi_i | H | \Phi_j \rangle$ with four elements coupling Φ_A and Φ_B forms the characteristic equation. In the simple form of the tight-binding formulation where only the nearest neighbor interactions are considered, we have the diagonal elements of the matrix

$\mathcal{H}_{AA} = \mathcal{H}_{BB} = \epsilon_{2p}$ where ϵ_{2p} is the $2p$ level energy of an individual carbon atom. The off-diagonal elements $\mathcal{H}_{AB}$ are given by:

$$2\mathcal{H}_{AB} = -\gamma_0\left(e^{i\mathbf{k}\cdot\mathbf{R1}} + e^{i\mathbf{k}\cdot\mathbf{R2}} + e^{i\mathbf{k}\cdot\mathbf{R3}}\right) = tf(k)$$

(1-3)

Eq.(1-1) is a direct result of the nearest neighbor assumption where the three terms comes from considering the interaction between the three nearest B atoms and the A atom. Here, $-\gamma_0$ is the nearest neighbor transfer integral ($\langle\varphi_A|\mathcal{H}|\varphi_B\rangle$). With the x, y coordinates given in Figure 1-1, we have

$$f(k) = e^{ik_xa/\sqrt{3}} + 2e^{-ik_xa/2\sqrt{3}}\cos\left(\frac{k_ya}{2}\right)$$

(1-4)

Since the Hamiltonian forms a Hermitian matrix, we have $\mathcal{H}_{AB} = \mathcal{H}_{BA}^*$, which are complex conjugates of each other. We also have the overlapping integral matrix defined as $S_{ij} = \langle\Phi_A|\Phi_B\rangle$ and the explicit form of $\mathcal{H}$ and $\mathcal{S}$ are as follows:

$$\mathcal{H} = \begin{pmatrix} \epsilon_{2p} & tf(k) \\ tf(k)^* & \epsilon_{2p} \end{pmatrix}, \qquad \mathcal{S} = \begin{pmatrix} 1 & sf(k) \\ sf(k) & 1 \end{pmatrix}$$

(1-5)

By solving the equation $\det(\mathcal{H} - E\mathcal{S}) = 0$, we have engenvalues $E(\mathbf{k})$ for the graphene π-bands, which can be obtained with respect to the wave-vector $\mathbf{k}$:

$$E(\mathbf{k}) = \frac{\epsilon_{2p} \pm tw(\mathbf{k})}{1 \pm sw(\mathbf{k})}$$

(1-6)

where $w(\mathbf{k}) = \sqrt{|f(\mathbf{k})|^2} = \sqrt{1 + 4\cos\frac{\sqrt{3}k_xa}{2}\cos\frac{k_ya}{2} + 4\cos^2\frac{k_ya}{2}}$

The plus and minus signs in the $E(\mathbf{k})$ relation above are for bonding and anti-bonding states of the π-bands due to symmetric and anti-symmetric coupling between Φ_A and Φ_B.

Figure 1-2 shows the calculated $E(\boldsymbol{k})$ dispersion relation for the π-bands of single-layer graphene. Here, we used $\epsilon_{2p} = 0$, $t = -3.033$ eV, and $s = 0.129$ [62]. The zero-bandgap at the K and K' points are a direct consequence of the two atoms at A and B sites being distinctly different while also having complete symmetry equivalence. In other compound atomic crystals like boron nitride where the atoms at A and B sites are of different elements, the resulting energy dispersion has a bandgap due to different values of ϵ_{2p} for the different elements. In Figure 1-2, the upper half of the band structure comes from the anti-bonding π-band energy while the lower half describes the bonding π-bands.

For energy dispersion relation close to $E = \epsilon_{2p}$, the dispersion relation for graphene can be further simplified by assuming the overlapping s to be zero, in which case, we have:
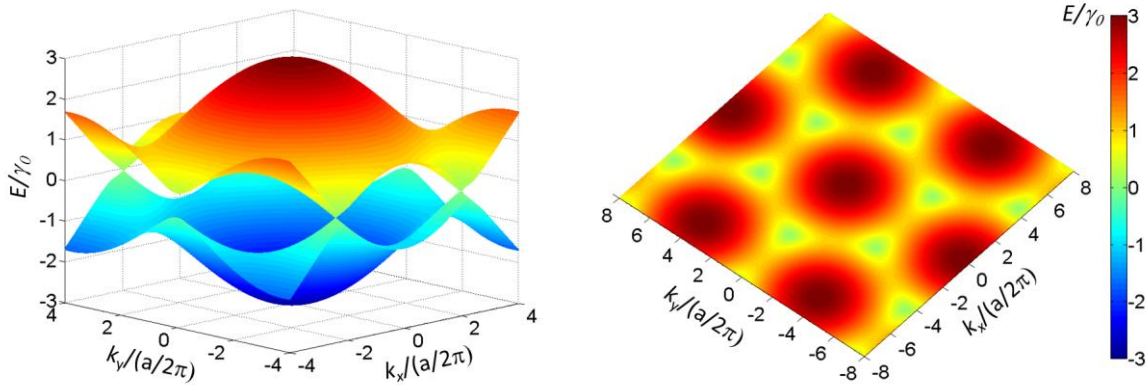
Figure 1-2 The 2D energy dispersion relation of monolayer graphene (a) The energy dispersion relation for monolayer graphene [3]. The conduction band and valence band touches at the K and K' points. (b) Top-view of the E-k relation showing correspondence with the hexagonal reciprocal lattice in Figure 1-1(b). The corresponding high symmetry points Γ, K and M are indicated.

$$E(k_x, k_y) = \pm t \sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}}$$

(1-7)

the energy states have $\pm 3t$, $\pm t$ and 0 with a band width $6t$ at the high symmetry points Γ, M and K in the Brillouin zone, respectively (Figure 1-1).

Wallace et. al. [63] have shown that about the K and K' points, graphene has a linear dispersion relation. This is also clear from Figure 1-2. In the literature, the first order terms in the Taylor expansion of eq. (1-7) is often used to describe this relation, which gives:

$$E^{\pm}(k) = \pm \hbar v_F |k|$$

(1-8)

where v_F is the Fermi velocity ($\sim 10^8$ cm/s) given by

$$v_F = \sqrt{3}(\gamma_0 a / 2\hbar)$$

(1-9)

a is the lattice constant of graphene. It is worth noting that eq. (1-8) is also the dispersion relation resulting from solving a massless Dirac Hamiltonian [64] at the K (K') point. To explain the transport properties of graphene near the Fermi level as well as most optical experiments in the visible frequency range, this linear energy dispersion relation is usually sufficient. The resulting density of state (DOS) of single-layer graphene is

$$D(E) = \frac{2E}{\pi(\hbar v_F)^2}$$

(1-10)

As a result of its unique bandstructure, electrons in graphene under low-energy excitations exhibit the properties of massless, chiral, Dirac fermions [1]. This particular low-energy dispersion relation closely resembles the massless fermions where the electrons in graphene have the signature of "relativistic" particle, such as photons. Since the Dirac fermions in graphene move with a Fermi velocity v_F that is 300 times slower than the speed of light, it allows many unusual quantum mechanical properties to be observed at much smaller speeds [65][66]. Under the influence of magnetic field, Dirac fermions in graphene show new physical phenomena resulting from its unique electronic properties compared to conventional electrons [67][68]. This includes the experimental observation of an anomalous integer quantum Hall effect [1][2]. The

large cyclotron energies allow such phenomenon to be observed at room temperature [69], which is not possible in the more traditional 2D electron gas of Si or III-V compound semiconductors [70].

The relativistic behavior of Dirac fermions in graphene has always been emphasized by the physicists as one of the key feature of graphene electronic properties. The chemists, on the other hand, explain it based on the orthogonality and non-interacting nature of π and π^* states. The linear dispersion relation is also a result of these two orthogonal states. Hence, many of graphene's unique properties derive from both its structure and the strong covalent bonds, leading to a material that has very high stiffness and high optical phonon frequency. Because of the high optical phonon frequency in graphene (1600 cm^{-1} compared to ~500 cm^{-1} in silicon and ~300 cm^{-1} in III-V compounds like InP and InAs), the carriers in pristine graphene experience much less optical phonon scattering than in the conventional semiconductors. The low optical phonon scattering, combined with the zero rest mass and very high Fermi velocity of the carriers, makes it potentially much easier to operate graphene devices into the ballistic regime than in Si or III-V devices. It has been experimentally proven that carrier in graphene can transmit without scattering over micro-meters of distance at room temperature [71], making the material particularly suited for high speed electronics.

The analysis above is primarily based on the assumption that graphene is pristine and free-standing. From an application perspective, the carrier movement in graphene is much more complicated than the basic theory. There has been intense research in trying to understand the role played by the various scattering mechanisms in affecting the carrier transport in graphene under realistic application conditions, such as those due to charged impurities from the substrate [72][73], lattice defects in graphene [74], adatoms on graphene surface and ripples due to the atomically thin structure of graphene [75]. Unlike in 3D bulk materials, graphene exhibits flexural behavior due to the out-of-plane phonon modes so that a carrier in graphene moves along a locally curved surface lacking mesoscopic structural uniformity. While placing graphene on a support substrate can stabilize the material to a certain extent, it also introduces additional scattering mechanisms that can slow down the carrier movements. The speed of carrier movement in semiconductors or semimetals like graphene under low bias conditions is often characterized by its mobility, a term relating the low-field carrier velocity to the applied electric

field. The mobility of graphene is influenced by many factors, and recognizing the major scattering mechanisms limiting the transport properties of graphene is important for developing and understanding device technology. Several key scattering mechanisms have been identified to be critical in graphene. Scattering of carriers by charged impurities is believed to have a key influence on the speed of carrier movement in graphene [72], particularly at lower temperatures. Such impurities have many sources, such as dangling bonds and charged particles on or in the substrate, or adatoms and molecules on graphene surface. For unscreened Coulomb scattering, Refs. [76][77] suggest that the scattering time is proportional to the carrier energy state E while the conductance of graphene is proportional to carrier density n_s. In reality, the Coulomb potential of the charged impurities can be screened by the carriers in the graphene that clouds around the impurity potential. The presence of charged impurity scattering in graphene is evidenced by the observation of a linear conductance vs. carrier density characteristic. However, the same linear conductance vs. carrier density relation can also arise from uncharged defect potentials when these effects become strong enough to create mid-gap states [78]. Such theory is supported by recent experimental observation of linear conductance vs. n_s resulting from strong defect scattering on intentionally damaged graphene. The second key scattering mechanism in graphene is the short-range scattering resulting from the interaction between the Dirac fermions with localized defects [77][79][80]. Short range scattering potentials lead to a scattering time that is proportional to $1/E$, but does not depend on temperature. Finally, deformation potential scattering, mostly due to acoustic phonons [78][81] and optical phonons, are another important scattering mechanism in graphene. Especially at elevated temperatures above 300 K, optical phonons play a dominant role in restricting carrier movements in graphene [82]. It is still in debate whether the optical phonon in graphene [82] or the polar optical phonon in the underlying SiO_2 [83] is playing a more important role in limiting graphene conductivity at high temperatures while others suggest both factors may need to be taken into account [84].

The carrier transport in graphene is strongly influenced by the interplay between these different scattering mechanisms. The importance of each scattering mechanism varies significantly across different substrate media, graphene material quality, temperature range and the cleanness of the sample. As a result, the mean-free-path of graphene, a term used to quantify the average distance traveled by carriers before scattering events occur, varies from micrometers in suspended

graphene and graphene on the inert 2D h-BN substrate [71], to below 100 nm in graphene on a SiO$_2$ substrate [85], all at room temperature. The carrier mobility in graphene also changes significantly over a wide range from 100,000 cm^2/V.s at 240 K [86] in suspended graphene, to around 25,000 cm^2/V.s at high carrier density on a h-BN substrate [87], to about 10,000 cm^2/V.s on SiO$_2$ at room temperature [54], while the carrier mobility in graphene synthesized by Cu-mediated chemical vapor deposition technique varies from 3000 cm^2/V.s to 6000 cm^2/V.s due to the intrinsic limit of the material being polycrystalline, the wrinkles and defects that are

E$_g$=0 eV   **E$_g$=6.0 eV**

Atomic Crystals: Graphene, h-BN   **TMOs (Transition Metal Oxides): MoO$_3$, LiCoO$_2$**

TMDs (Transition Metal Dichalcogenides):   **III-VI/V-VI Compounds (Ga,In)$_2$Se$_3$, Bi$_2$(Se,Te)$_3$**
MoS$_2$,WS$_2$,NbSe$_2$ (MX$_2$)
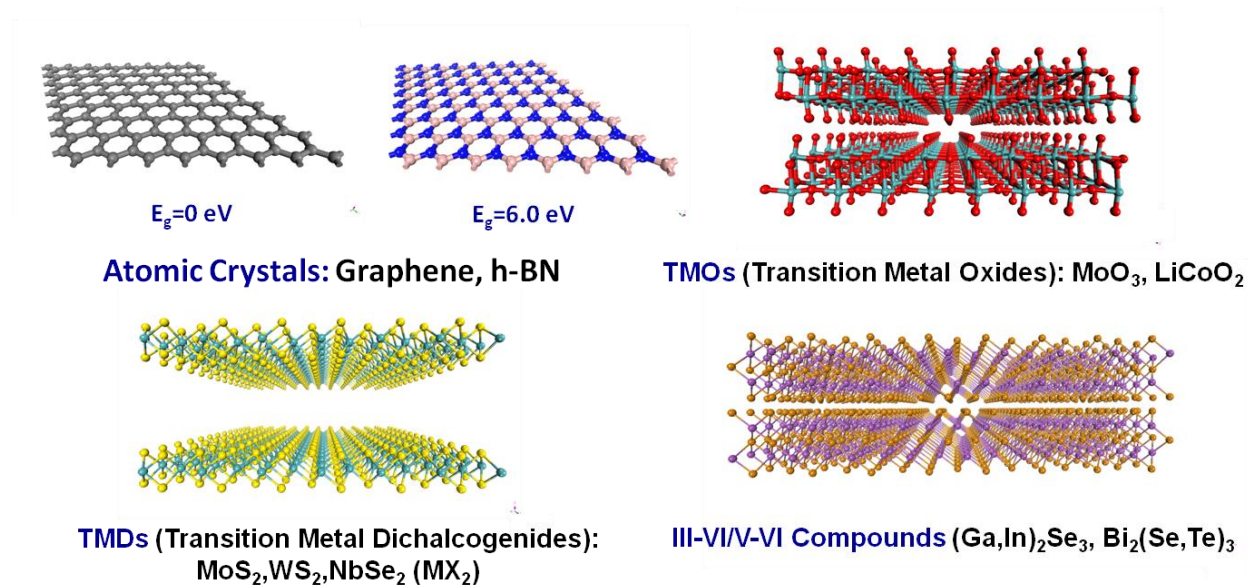
Figure 1-3 Schematics of the 2D lattice structure of the key members from the 2D materials family. The 2D materials family, which includes atomic crystals such as graphene and h-BN, members of the transitional metal dichalcogenides family, members of the transition metal oxides family, and members of other compound material families.

associated with its transfer process, and the interaction with the substrate optical phonons. This will be discussed in more detail in later chapters. Nevertheless, the excellent transport properties of graphene even in its CVD grown polycrystalline form, combined with its optical transparency, chemical resistance, and mechanical flexibility, offers us a unique material for electronics and optoelectronics applications with a conductivity rivaling that of metals, and a Fermi level and carrier density that can be tuned by electrical biasing.

1.2.2. Electronic Properties of Other 2D Materials

The 2D materials family goes far beyond graphene. Recent years have seen the emergence of many other members of the 2D materials family, from atomic crystals such as h-BN, to members of the transition metal dichalcogenides (TMD, MoS_2, WS_2, $NbSe_2$ (MX_2)) family, transition metal oxides (TMO, MoO_3, $LiCoO_2$) family, and some member of the III-VI/V-VI Compounds families (($Ga,In)_2Se_3$, $Bi_2(Se,Te)_3$) (Figure 1-3). This leads to an extremely versatile system of 2D materials whose members range from metal, semi-metal, semiconductor, to topological insulators and even superconductors (Figure 1-4). These materials have been known for a long time. What is new is the ability to make them in few layer form.

In this section, we will discuss briefly about the properties of some of the TMD materials,

Graphene

- Ambipolar conduction
- Best thermal conductivity (in plane)
- Record e-/h+ mobility

Bilayer Graphene

$E_g = f(E)$

- Direct bandgap, controlled by E-field
- Potential for exciton condensate

Single-layer MoS_2

$E_g = 1.8$ eV

- Excellent semiconductor
- Suitable for scaled electronics
- Valleytronics

h-BN

$E_g = 6.0$ eV

- Outstanding dielectric and substrate
- Ideal passivation
- tunneling barrier

semi-metal (Graphene); semiconductor (MoS_2, WS_2); insulator (hBN); metal and superconductor

Figure 1-4 The unique physical properties of 2D materials. The 2D materials display a rich array of physical properties and a versatile system of materials from semimetal, to semiconductor, to insulator, metal and even superconductors.

normally termed as MX_2 (M=Mo, W; X=S, Se). These materials, discovered in bulk form more than 40 years ago [88][89], have attracted extensive research efforts in the fields of

nanotribology, catalysis, energy harvesting, and optoelectronics [27][90][91][92][93][94][95][96][97][98][99][100]. Broken inversion symmetry and indirect-to-direct bandgap transitions of TMDs are observed when the dimension is reduced from multi-layers to monolayer [23][24][101]. In a typical layered TMD (LTMD) monolayer structure, the transition metal layer is sandwiched between two chalcogen layers by covalent forces and the different molecular MX_2 layer are stacked on top of each other with weak van der Waals forces [89]. The LTMD monolayers, being considered as the thinnest semiconductor materials, offer many advantages for scaling of electronic devices [102][103]. The transistor fabricated with the exfoliated MoS_2 monolayer displays a high on-off current ratio and good electrical performance [27][102][104]. Moreover, MoS_2 is considered as a promising candidates for replacing platinum as the catalysts for hydrogen generation [99]. Recent theoretical predictions suggest that defect sites of single layer MoS_2 can assist the dissociation of water, offering a new chemical route for developing hydrogen as a clean and sustainable energy source [105].

The demonstration of spin- and valley-selective excitation in monolayer MoS_2 by polarized optical pumping also suggests rich opportunities in exploring these new materials for valleytronics and valley-based optoelectronic application [106][107][108][109][110]. The broken inversion symmetry of the monolayer and the strong spin-orbit coupling can lead to a fascinating interplay between the spin and valley physics. This property enables simultaneous control over the spin and valley degrees of freedom, and creates an avenue towards developing ultra-low-power integrated spintronics and valleytronics. Analogues of MoS_2, such as a single-layer WSe_2, are expected to exhibit even stronger spin-orbit coupling with heavier transition metal elements. The LTMD monolayers also have their conduction band minimum well aligned to the valence band maximum with optically measured bandgaps ranging from 1.49 eV ($MoSe_2$) to 2.05 eV (WS_2) [101][111]. A strong emission in the visible frequency range is promising for optoelectronic applications [23][24]. Most optoelectronic devices, including flexible electronics, require a good technique to integrate high-quality and preferably large-area LTMD monolayers on diverse surfaces. A synthetic approach for direct growth of LTMD monolayers on various substrates and a feasible transfer process after growth are highly needed for the accomplishment of novel hybrid structures by integrating LTMD monolayers with other layer materials such as metallic graphene, insulating hexagonal boron nitride (h-BN) and so on [112].

1.3. Current Status of 2D Material Transistor Technology

1.3.1. Graphene Field-effect Transistors

Transistor technology underlies many electronics, optoelectronics and sensing applications and recent years have seen active research in developing field-effect transistors based on graphene and other 2D crystals. While the lack of a bandgap in graphene imposes serious limitations on its application for digital electronics, many RF circuits do not require the existence of a bandgap and can be realized in devices with a low on-off current ratio. The excellent mobility of graphene, combined with its high saturation velocity, thermal conductivity and micrometer-scale ballistic transport, makes this material an outstanding candidate for the next generation high frequency transistors and low noise amplifiers. Thanks to these properties, graphene transistors show high current density and excellent electrostatic confinement which increase the conversion efficiency, reduce their noise level (especially using bilayer graphene [113]), and improve the operating frequencies of future amplifiers.

Research activities in developing graphene-based field effect transistors (GFETs) started at the same time as the first isolation of this material. The first GFET was fabricated on a SiO_2/Si substrate in 2004 [1]. A 300-nm-thick SiO_2 layer was used as the gate dielectric, and its thickness was chosen to enable optical imaging of single- and few-layer graphene. At the same time, the heavily doped silicon substrate underneath served as a back-gate to modulate the conductivity of the graphene channel. This structure is the most commonly used in physics experiments due to its simplicity, but is certainly not ideal for RF applications because of the thick gate dielectric and large parasitic capacitances introduced by the conductive substrate [114]. For such applications, a much more scaled transistor device structure with a top-gate is necessary. The first top-gated GFET was fabricated by Lemme *et al*. [115] in 2007. Meric et al. [116] demonstrated the first GFETs with high frequency current-gain in 2008, which exhibits a similar $1/f$ dependence of short circuit current gain on frequency as compared to conventional silicon and III-V transistors. Since then, the performance of radio frequency (RF) GFETs has quickly improved. IBM demonstrated the first RF GFET with sub-micrometer gate length in late 2008 [117]. This device, with a gate length of 150 nm, demonstrated a f_T of 26 GHz after de-embedding the measurement pad parasitics. Shortly after this result, Hughes Research Laboratories (HRL) reported RF GFETs with f_T=5 GHz and a gate length of 2 μm using

graphene grown on SiC wafers [118]. In 2010, researchers at IBM reported an f_T of 100 GHz using graphene on SiC with a gate length of 240 nm [119], and in the same year, Duan's group at the University of California at Los Angeles fabricated a GFET using a nanowire gate that gives an f_T, after de-embedding measurement pad parasitics, of 300 GHz [120]. Although the progress in fabricating high performance RF GFETs has been very rapid in recently years and the prospect of using GFETs for applications in RF circuit is bright, many challenges still remain before graphene may be incorporated into integrated RF circuits. Also, the extracted value of f_T in graphene devices is sensitive to the technique used for de-embedding the pad effects and can easily lead to significant errors. These issues will be discussed in detail in Chapter 4.

1.3.2. Field-effect Transistors based on other 2D Materials

More recently, there has also been increasing interest in the transistor technology based on other members of the 2D materials family, particularly the transition metal dichalcogenides in their single- and few-layer form. In fact, the demonstration of field-effect modulation of carriers and current in layered TMD materials dates back to even before the experimental evidence of an electric-field effect in graphene. In a paper published in early 2004, Podzorov et. al. [121] showed high mobility FET devices based on layered structures of WSe_2. However, the work did not attract much attention at that time and subsequent research effort in this field was focused on graphene devices. A couple of years later, in 2006, Novoselov et. al. [37] extended their exfoliation technique, which was used in their groundbreaking work of graphene, to also allow the creation of single- and few-layer micro-flakes of LTMD materials. Splendiani et. al. [24] later characterized the bandgap in few-layer TMDs based on their photoluminescence and Mak et. al. [23] studied the shifting trends in the Raman spectrum of these materials. But the interests in layered TMD for electronics application did not intensify until the seminal paper by Radisavljevic et. al. [27] that demonstrated the first field-effect transistor based on single-layer MoS_2. Although there are several drawbacks in the performance of the transistor shown in that work, such as the lack of current saturation in the device and the accuracy of mobility extraction, the paper nevertheless inspired unprecedented interest in these materials for electronic applications and beyond. Fully integrated single- and few-layer MoS_2 circuits working as basic building blocks of digital and analog electronics, such as inverters, NAND gates, static random access memory (SRAM) and ring oscillators, have all been demonstrated [102]. Despite the rapid

progress in the past few years, this field is by all means still in its infancy at this point and many aspects of the device technology are still in the very early stage of development.

1.4. Thesis Outline

This thesis has three main goals. First, we aim to identify the main problems that limit the high frequency performance of graphene transistors and demonstrate novel solutions to overcome them, with the broader target of using this material in conventional high frequency electronics and ubiquitous electronics. Through systematic analysis of device characteristics and the development of advanced fabrication technologies, we aim to understand the key limitations on the high frequency of graphene transistors, demonstrate state-of-the-art devices and project performance trends for graphene FETs. The second goal is to demonstrate novel applications of graphene transistors for analog signal processing that can utilize its unique combination of ambipolar conduction with a very high mobility. Completely new designs of frequency multipliers, mixers and phase shift keying devices have been demonstrated that rely on the symmetrical "V" shape characteristics of graphene to realize these functionalities, which would take a much more complicated circuit with several times more device components to realize in conventional Si CMOS electronics. Finally, layered TMD materials, in particular single- and few-layer MoS_2, are used as a new 2D materials for digital logic applications. Here, we aim to develop understanding of the device performance while also demonstrating circuit level applications. Device technology will be developed based on both exfoliated flakes and CVD grown large area single-layer materials to explore the performance potential of these new electronic materials while also demonstrating the scalability of the synthesis and device fabrication technology.

The thesis is organized as follows:

In chapter 2, the various synthesis technologies for obtaining single- and few-layer 2D materials will be reviewed. This chapter will also discuss our recent work in developing the synthesis methods for obtaining large area single-layer TMD materials by chemical vapor deposition techniques, which is done in close collaboration with Prof. Jing Kong's group at MIT. Most materials used in this thesis work are obtained using growth methods introduced in this chapter.

In chapter 3, the basic operation principles of graphene FETs are outlined. This chapter will start from a detailed characterization of carrier mobility in graphene. Studies of contact and substrate effects on device performance will be presented. The important concepts and figures-of-merits of DC characteristics are described. Also, a concise description of the standard fabrication process is provided. A virtual source carrier injection velocity based compact model is also proposed for developing insight to the device behavior and the drain-induced minimum shift effect are briefly discussed.

In chapter 4, the RF performance of graphene FETs fabricated at MIT is analyzed in detail. Factors limiting the RF performance of graphene FETs are analyzed, particularly focusing on understanding and optimizing the parasitic components of the devices. A method for analyzing the carrier transit delay in graphene FETs is proposed, derived from a previous version of the technique used for analyzing III-V HEMTs. New processing technologies that minimize parasitic components in the device operation are developed to improve the f_T performance of the device. A process that relies on the fabrication of T-shaped gate as the mask for subsequent metallization to create self-aligned device structures is also proposed. The effects of different de-embedding techniques on the value of the extracted f_T are also described to highlight the importance of a unified de-embedding technique in analyzing graphene RF FETs.

In chapter 5, we propose the concept of ambipolar electronics, a new concept for analog circuit design first proposed through this thesis work. Several novel analog circuit applications of graphene ambipolar electronics are demonstrated, which operates well into the gigahertz frequency range. The frequency multipliers application is analyzed in detail, while other applications such as mixers and phase shift keying devices are also described.

In chapter 6, the transistor technology of LTMD materials will be discussed. In this chapter, we also address a few key challenges that are critical to the future application of 2D materials in electronics and optoelectronics, focusing on tackling the challenges to construct fully integrated multi-stage logic circuits based on these materials and in resolving the scalability issues of both the materials and fabrication technology of single-layer TMD by demonstrating electronic devices and circuits on large area CVD grown MoS_2. The former demonstrates the capability of 2D materials for complex digital logic and the later solves the scalability issue that underlies many potential industrial level applications of this emerging materials family. These circuits

were fabricated entirely on the same chip for the first time thanks to the seamless integration of both depletion-mode (D-mode) and enhancement-mode (E-mode) MoS_2 transistors. The transistors show multiple state-of-the-art characteristics, such as current saturation, high on/off ratio ($>10^7$), and record on-state current density (>23 µA/µm). This demonstration of integrated logic gates, memory elements and a ring oscillator operating at 1.6 MHz represents an important step towards developing 2D electronics for both conventional and ubiquitous applications, offering materials that can combine silicon-like performance with the mechanical flexibility and integration versatility of organic semiconductors.

In chapter 7, a summary and conclusions are presented. Future work to further expand the frequency performance of graphene FETs beyond mm-wave frequencies is discussed. Research directions to investigate the electronic and optoelectronic application of 2D materials are also provided.

Chapter 2. Synthesis of 2D Materials

2.1. Graphene Synthesis

The capability of synthesizing scalable and high quality two dimensional crystals is fundamental to the future applications of this emerging materials system, especially from an industrial perspective. The synthesis of 2D materials can follow two general paths. Top-down approaches, such as mechanical exfoliation and liquid phase exfoliation, take advantage of the weak interaction between layers of 2D crystals that allows individual 2D layers to be separated from its bulk form. On the other hand, bottom-up approaches, such as chemical vapor deposition and vacuum graphitization of SiC, allow truly scalable techniques for obtaining wafer-scale thin films of single-layer 2D materials. In this chapter, the four key methods for synthesizing single- and few-layer graphene will be discussed while new techniques for synthesizing transition metal dichalcogenides, such as MoS_2 and WS_2, will also be presented.

2.1.1. Micro-Mechanical Exfoliation

Cleaving bulk graphite through mechanical exfoliation, or the famous "scotch tape" method, is one of the most straightforward ways of obtaining high quality single crystal mono-layer graphene or multi-layer crystalline Bernal stacked graphene where the neighboring layers are oriented at 60° relative to each other [122]. This method requires the application of a sufficiently large force perpendicular to the top hexagonal carbon plane for overcoming its Van der Waals' coupling with adjacent layers. Early attempts of mechanical exfoliation had been demonstrated through the use of scanning probe microscopy (SPM) cantilevers [123][124][125][126][127], which however cannot create large flakes of graphene due to the intrinsic limitations of the SPM based technique.

The major breakthrough came in 2004 when Novoselov etc. [54] reported the first successful isolation of few-layer graphene using adhesion tape for peeling off graphene layers, giving rise to a simple way of obtaining a high quality single crystalline graphene flake. Many variations of the method have been developed in the following years. In a typical process, square HOPG flakes (20μm to 2 mm in length) are first prepared, which is then stuck to photoresist. Adhesive tape is then used to peel off graphite sheets from the photoresist. While the bulk of the graphite sheets is removed from the photoresist, some single- to few-layer graphene sheets stays. These

layers can be transferred onto any substrate by releasing them from the photoresist through an acetone treatment. This method is extremely versatile and allows the creation of not just graphene, but also other 2D materials such as h-BN, MoS_2, WS_2, etc. Since then, the technique has been used in demonstrating a wide range of novel physical phenomena in 2D material systems, such as the quantum electrodynamics in graphene [1][2] and the spin-valley coupling in single-layer MoS_2 [107][108]. However, this mechanical exfoliation process also suffers from major shortcomings. Although, it generates graphene flakes of the highest quality, the size of the graphene sheets that can be formed using this method is limited to only tens of micrometers. The size limitation, together with poor yields and difficulty in controlling flake location, hinders its potential for commercialization. Consequently, this method has found its most applications in preparing graphene for laboratory experiments, studying theoretical behavior, or as a reference for benchmarking other synthesis techniques of 2D materials.

2.1.2. Synthesis by Chemical Routes

Chemical techniques offer an alternative route for synthesizing graphene. The general approach of chemical synthesis relies on introducing intercalation between graphite layers to weaken the interlayer Van der Waals bonding, which can eventually lead to the separation of individual layers. The process starts from the formation of a graphite intercalation compound (GIC) when bulk graphite is immersed into concentrated sulfuric and nitric acid. The GIC expands the graphite lattice and results in an increase of the inter-layer distance. Ultrasonic techniques are then often used to finally break the now much-weakened inter-layer coupling, allowing exfoliated graphite sheets to form. Single layer graphene can also be synthesized using this approach from graphite through forming graphene oxide (GO) as a possible GIC [12][47][48][53]. In ref. [47], GO was first synthesized with sulfuric acid, sodium nitrate, and potassium permanganate, which can then be easily dispersed in aqueous solution, assisted by the inter-layer electrostatic repulsion introduced by the intercalated hydroxyl and ether groups. The dispersed GO solution can be deposited on an arbitrary substrate where the GO can be subsequently reduced to form graphene sheets. Several other chemical exfoliation methods have also been proposed to form graphene following the similar general approach. More details of the reduced GO are also discussed in [128][129].

The chemical exfoliation techniques offer numerous advantages over mechanical exfoliation to form graphene. Firstly, the chemical methods of obtaining graphene are of very low cost and have excellent scalability. With the flexibility offered by the liquid phase graphene solution, the graphene synthesized by this method can be spin coated on any substrate choice, and is favorable for obtaining large quantities of the material that can be applied to any type of substrate and surfaces. On the other hand, significant challenges and some fundamental limitations also exist for developing chemically synthesized graphene for electronic and optoelectronics applications. The chemically derived graphene material often suffers from degraded electronic properties due to the defects created during the oxidation and reduction process. Such defects typically reduce the mobility of graphene to well below 1000 cm^2/V.s, which is several times lower than CVD synthesized graphene. However, in some other applications that rely on the chemical functionalization of graphene, such defects can actually be attractive for acting as active sites to enhance reactions with other chemicals. For example, these carbon materials obtained through a chemical route are actively being explored for many electrochemical applications, such as energy storage [130][131][132][133] and for enhancing the conductivity of other less conductive materials in the form of nanocomposite materials [134][135].

2.1.3. Graphene by Epitaxial Growth on SiC

Vacuum graphitization of epitaxially grown silicon carbide was probably the first method that allowed the synthesis of uniform high quality single- and few-layer graphene at the wafer-scale. In this method, graphene is directly prepared on the single crystalline wide-bandgap silicon carbide substrate, which is heated to about 1,400 ℃ in vacuum. Under such conditions, the top silicon atoms sublimate and graphene is formed on the surface. This method produces wafer-scale graphene with good quality, though its transport properties are normally worse than the exfoliated flakes due to the rough terraced interface layer formed during the growth process, as well as significant electron doping due to the substrate [55].

Among the many hexagonal forms of SiC, 6H-SiC with AB-stacking or 4H-SiC with ABC-stacking are often used for the epitaxial vacuum graphitization for forming graphene. The morphology and quality of the resulting graphene depends strongly on the crystal orientation of the topmost layer of SiC that is exposed on the surface, being either a Si-face or a C-face along the c-axis. In the high-temperature annealing method first developed by Van Bommel et al. [39],

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it is found that after heating SiC between 1000 and 1500 °C in ultra-high vacuum (UHV) below 10^{-10} Torr, the formation of thin graphite layers was observed. Low electron energy diffraction (LEED) and Auger electron spectroscopy (AES) confirmed that the resulting graphene on the Si-face of SiC can be single crystalline and was epitaxial with the SiC lattice. For graphene formed on the C-face SiC, the material was often polycrystalline and exhibited a range of in-plane orientations relative to the underlying SiC lattice [136][137][138][139].

While the detailed growth mechanism is still a topic for further investigation in the graphene growth community, it is understood that the formation of graphene on SiC follows three main steps [136][137][138][139], including the high temperature sublimation of Si atoms from the SiC surface, the reconstruction of a C-rich surface, and the graphene growth initiated from nucleation centers at the step sites. The general process begins from the treatment of the SiC substrate surface in hydrogen at 1600 °C for surface curing. The sample is then annealed at 800-1000 °C in a Si flux for surface reconstruction to form a Si-rich surface. Subsequent treatment at 1100-1250 °C converts the Si-rich surface to a C-rich surface through the desorption of Si, which leaves behind extra carbon contents on the sample surface. The following high temperature treatment at 1200-1350 °C leads to reconstruction of the surface where the C atoms reorder themselves to form the graphene structure. The key to obtaining high quality graphene films on SiC using this method lies with the control of the intermediate structures that to a large extent defines the homogeneity of the final C-rich surface and the quality of the graphene product. Many factors during the growth process, such as temperature, pressure and other chamber condition, are critical. The phase transformation temperature and time for desorption are shown to vary over hundreds of degrees and several orders of magnitude, respectively [140]. At this point, there are different processes for surface treatment and the conditions for surface reconstruction vary significantly across the various groups.

The epitaxial growth of graphene on SiC has some important advantages for electronic applications, offering wafer-scale high-quality graphene materials and the merit of high thermal conductivity SiC substrate. On the other hand, some significant challenges also remain in developing this technique for the industrial level production of graphene. On the positive side, the graphene synthesized through this technique is naturally attached to the SiC substrate underneath. Hence, epitaxial graphene on SiC avoids the transfer step for electronics application,

which is necessary for example in CVD grown graphene. Many problems that are associated with this uncontrolled process, such as cracks and wrinkles that often appear during the transfer, are eliminated. Since graphene is directly created on top of a wide bandgap material, that is naturally a good insulator and excellent thermal conductor, it can facilitate the heat dissipation in high current density graphene transistors, making the material highly amenable for electronic applications. On the other hand, much experimental and application flexibility is lost due to the graphene being restricted to only one particular substrate, which for example is not favorable for integration with existing Si CMOS electronics. The process is also very expensive. The price of a single crystalline SiC wafer itself is much higher than substrates used in other methods such as metals for CVD graphene growth. More importantly, the process requires specific SiC since only 4H-SiC (0001) or 6H-SiC (0001) are suitable for the graphene growth, though there are some possibility that alternative inexpensive SiC on Si substrates may also allow graphene growth [141][142]. Another contribution to the high cost of the growth comes from the process itself. The high temperature UHV process requires elevated capital and power expenses. The thermal budget required also makes the process incompatible with standard back-end processing. In attempts to alleviate this problem, lower temperature processes has been developed using Ni-coated SiC [143]. Although this alternative approach can reduce the process temperature to 750 °C, it prevents the direct growth of graphene epitaxially matched to the SiC underneath. Finally, the UHV process places stringent requirements on process control. The precise control of the Si desorption rate is subject to variations induced by environmental effects, such as degassing and oxygen impurities in an Ar-ambient. Finally, it is common for graphene synthesized using this technique to have multiple layers and further process optimization is necessary if particular applications specifically require single-layer graphene.

2.1.4. Graphene Synthesis by Chemical Vapor Deposition

  Chemical vapor deposition based techniques offers what is probably the most flexible and versatile methods for graphene synthesis. Most of the graphene materials used in subsequent chapters are obtained using this technique. We believe the CVD synthesis method and its many variations stand uniquely among all other graphene synthesis technologies and are the most promising for many of graphene's potential applications. This higher-throughput and CMOS-compatible technology offers better materials properties and greater process flexibility than any other alternative. For a long time, transition metals, such as Ni and Cu, have been used to promote the formation of sp^2 carbon bonds, leading to materials such as graphite and carbon nanotubes [144][145][146][147][148][149]. The transition metals play the role of catalysts in these reactions where the partially filled d-orbitals and intermediate carbide phase lowers the
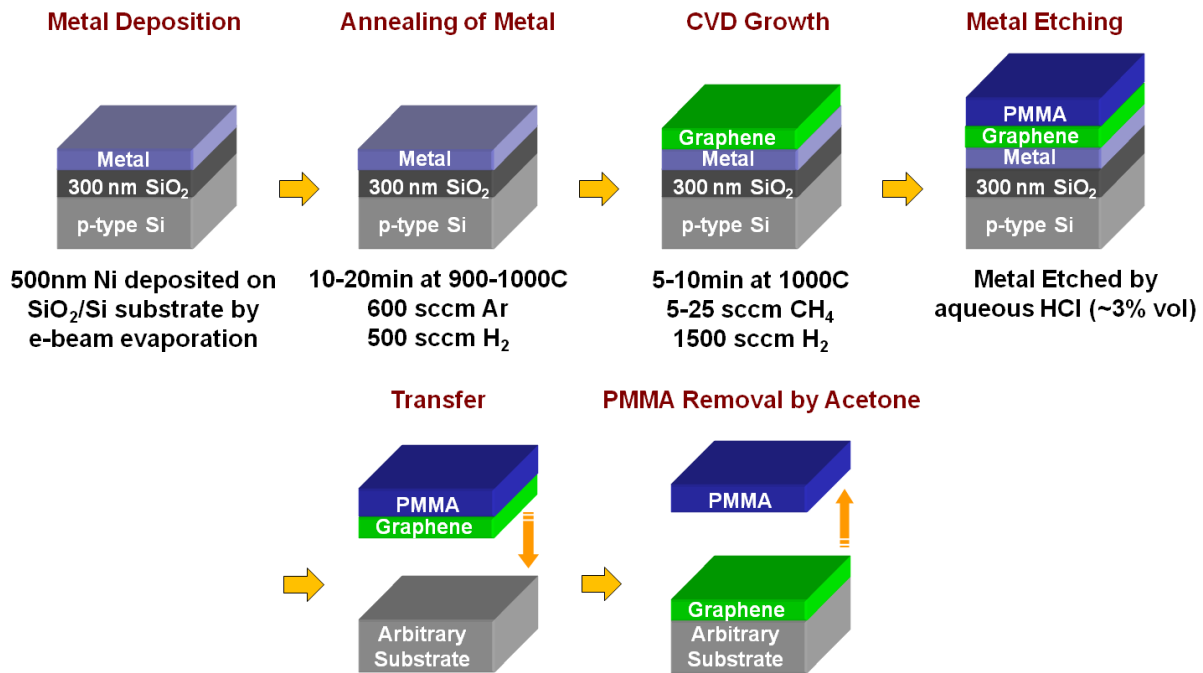
Figure 2-1 The chemical vapor deposition process and the related transfer technique for growing large area monolayer graphene. The transfer technique allows the graphene sheets to be placed onto any arbitrary substrate after growing the graphene on the metal. Many variations of this process have been developed over the years, including using e-beam evaporated metal, copper metal foils, and the roll-to-roll process that allows 30 inch graphene sheets be produced and placed on a transparent plastic substrate [142].

activation energy of the reactions and facilitates the formation of carbonaceous species.

The earlier attempts to synthesize graphene by the CVD method used Ni as the catalyst [56][150] [151][152], a transition metal that was also widely used in the synthesis of graphite and carbon nanotubes. Reina et al. successfully developed the first atmospheric pressure CVD (APCVD) [56][151] method for synthesizing large-area single- to few-layer graphene. After the growth, poly(methyl methacrylate) (PMMA) is coated on the graphene film and the Ni substrate is etched away in aqueous HCl solution. Films are then transferred onto polished Si wafers with a 300 nm thermally-grown SiO_2 on top (Figure 2-1). This was a major breakthrough at the time because it was the first time large-area thin film graphene could be synthesized at low cost without an expensive vacuum process, and in which the thin film could also be transferred to any arbitrary substrate. It is believed that the surface segregation of carbon on Ni plays a significant role in the growth process where the solubility of carbon in Ni changes significantly over a wide range of temperature (Figure 2-2). At high temperatures, typically around 1000 °C, the CH_4 gas
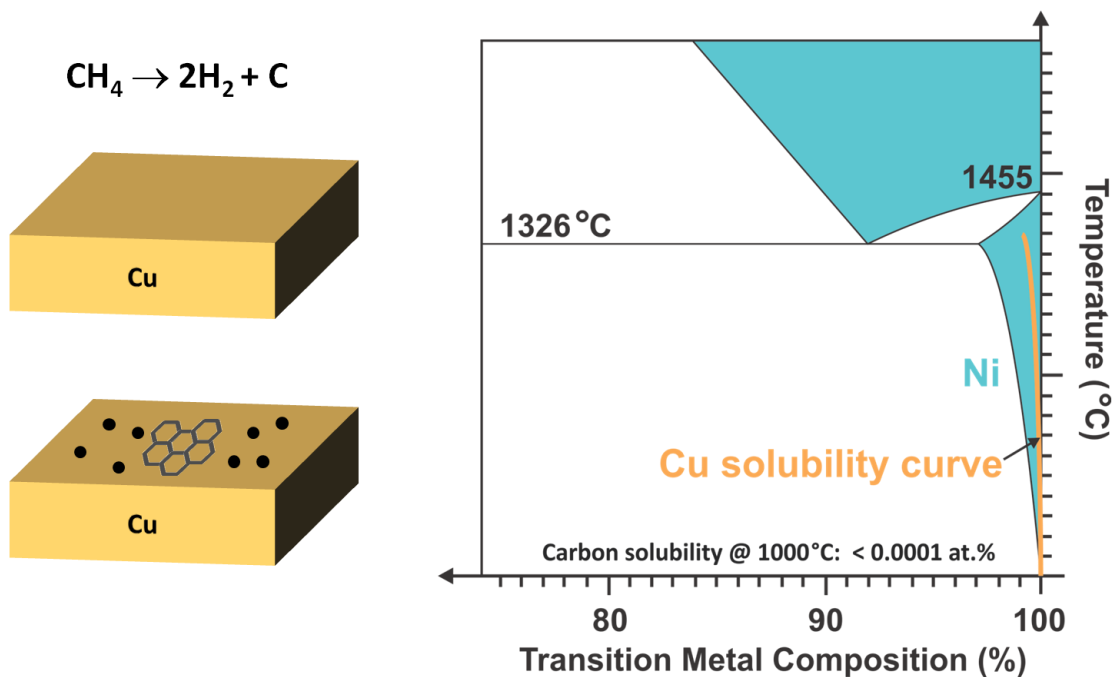
Figure 2-2 Schematic illustration of the CVD process for growing graphene on copper and the solubility curves of carbon in Ni and copper. At temperature around 1000 ℃, methane gas decomposes into hydrogen and carbon. Due to the much lower solubility of carbon in Cu compared to other metals such as Ni, the region near the copper surface saturates quickly and most of the carbon for graphene formation is from the gas phase through surface adsorption. For the growth of graphene on Ni, the segregation-precipitation process is more dominant due to the higher solubility of carbon in Ni, leading to a less controllable process. Multi-layer regions can often form at the grain boundaries where easy pathways exist for carbon to precipitate to the surface.

decomposes and its carbon content dissolves in the Ni substrate. Upon cooling, supersaturated carbon precipitates out of Ni due to decease in solubility. Since the grain boundaries of Ni provide a convenient diffusion path for carbon atoms to reach the surface, the resulting graphene at the grain boundary is more likely to be multi-layer. Although there have been reported techniques for controlling the cooling rate or using single-crystalline Ni to increase the coverage of single-layer graphene, it is challenging to achieve high uniformity single-layer graphene in this Ni-catalyzed process. Later, it became clear that a new catalyst metal with lower carbon solubility could be a better option than Ni. Therefore, Cu, which has a low carbon solubility up to temperatures near 1000°C (Figure 2-2), was chosen by Li et al. to synthesize large-area uniform single-layer graphene by the low pressure CVD (LPCVD) process [81]. The mechanism of graphene growth on a copper substrate differs significantly from techniques using a Ni catalyst. Although the details of the Cu-mediated CVD growth mechanism is still a topic of active research, recent work based on a Raman spectroscopy study using the C13 isotope revealed the re-assembly of thermally decomposed carbon species on copper surface through a self-limiting nucleation and growth process that is typically not hindered by substrate grain boundaries. The resulting graphene demonstrates high mobility above 4000 cm^2/V.s and coverage of single-layer region over 95% of the wafer area (Figure 2-3). The general process for CVD graphene growth on a copper substrate includes hydrogen annealing of copper foils, the CVD process where the carbon is delivered into the copper substrate from CH_4 precursors, and finally the controlled cooling step (Figure 2-2). Copper foils are first annealed at 1000 ℃ in H_2 (350 mTorr for 30 minutes). This step not only removes possible native oxide that may exist on the copper surface, but also re-crystallizes copper to increase its grain size and reduce the density of grain boundaries. In the next step, the copper foil is exposed to CH_4 under low-pressure conditions (1.6 Torr) at 800-1000 ℃. A graphene thin film forms on the copper foil surface mostly through nucleation due to the low solubility of carbon on copper. The subsequent cooling step can also affect the uniformity of the graphene film and the formation of multi-layer regions. Finally, the graphene film is transferred by either a wet or dry process to an insulating substrate for subsequent device fabrication.

The low cost growth method described above and its associated transfer technology was a truly remarkable discovery in graphene synthesis because large-area uniform single-layer graphene
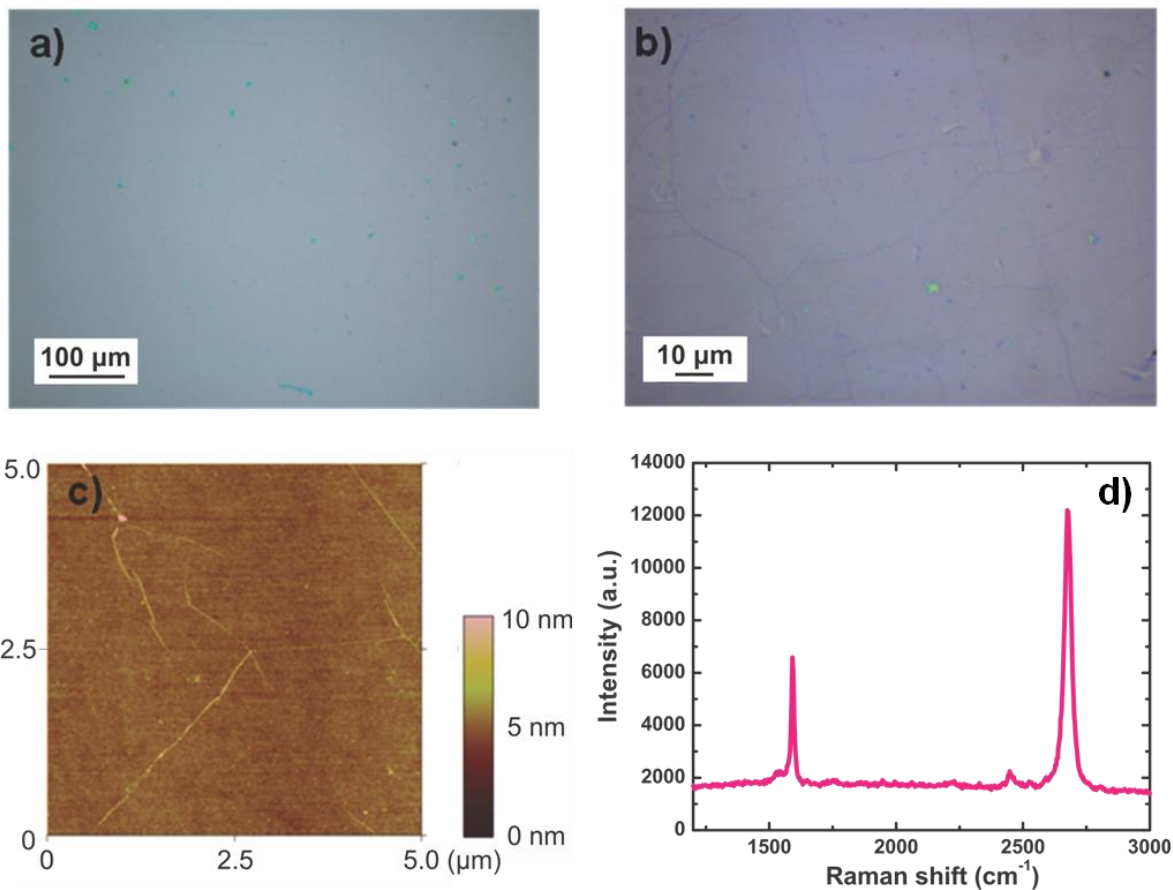
Figure 2-3 Monolayer graphene grown by CVD using a Cu catalyst and transferred onto SiO_2 substrate (a) and (b) optical micrograph of CVD-grown graphene. Using a Cu substrate, single-layer graphene with uniformity greater than 95% is obtained. (c) AFM image of the graphene obtained with a Veeco Dimension 3100 system showing excellent uniformity. (d) Raman spectrum using a Nd:YAG laser at 532 μm confirms the presence of monolayer

can now be obtained on any substrate. Many variations of this method have been subsequently reported [84][85][86][87][88][89][90]. This widely used technique also ignited many possibilities for practical industrial level applications, particularly in enabling roll-to-roll processing. 30 inch single-layer graphene films on a plastic substrate have been demonstrated by Samsung Electronics for applications as transparent electrodes in flexible display devices [153].

On the other hand, many challenges still remain in developing CVD based graphene synthesis technology for practical applications. The quality of the Cu-mediated CVD graphene is less than ideal and worse than the single-crystalline graphene obtained from mechanical exfoliation. The nucleation based growth mechanism makes it difficult to obtain graphene with large domains, a single crystalline region where the hexagonal lattice of grapheen has the same in-plane
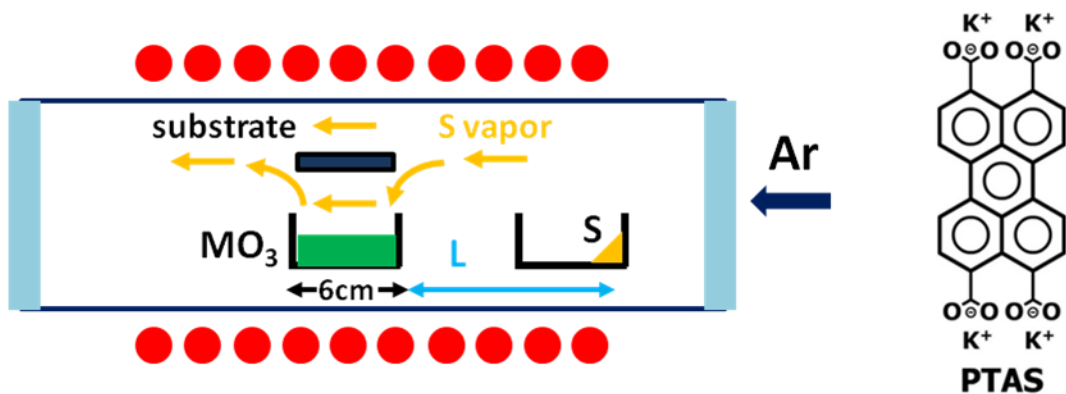
Figure 2-4 The growth setup and the process parameters for CVD growth of MoS_2 and WS_2. Schematic diagram of our experimental setup for the synthesis of a LTMD monolayer and the molecular structure of the PTAS salt used in the growth process to facilitate nucleation. MO_3 in the figure referes to various types of transition metal oxides, e.g. MoO_3 and WO_3 for MoS_2 and WS_2 growth respectively.

crystallographic orientation. The typical domain size is on the order of tens of micro-meters. Moreover, since graphene is synthesized on a metal substrate, it is necessary to etch the catalyst metal and transfer the graphene thin film onto an insulating substrate before it can be used for electronic applications. The transfer process, which can be accomplished with either wet or dry processes, can lead to mechanical damage of the very thin film while also introducing uncontrolled doping due to etchant residues and incomplete removal of residues from the support polymers also results in a deterioration of the graphene quality. Some attempts have been made to grow graphene directly on insulating substrates [154], though the resulting graphene is not of comparable quality to the Cu-CVD technology.

2.2. Synthesis of Layered TMD 2D Crystals by Chemical Vapor Deposition

We have briefly described the basic properties of layered transition metal dichalcogenides 2D crystals in Chapter 1. The effort to synthesize TMD 2D crystals is still in its infancy. Several techniques, including various kinds of exfoliations [23][24][27][155], physical vapor deposition [16][97], and chemical vapor deposition [156][157][158], have been demonstrated recently. Most of the previous work on 2D LTMD research was based of graphene flakes obtained through mechanical exfoliation, and the synthesis of large-area single-layer LTMD remains as a significant challenge. Recently, we have collaborated with Prof. Jing Kong's group at MIT in

developing an ambient-pressure-chemical-vapor-deposition (APCVD) process with a perylene-3,4,9,10- tetracarboxylic acid tetrapotassium salt (PTAS) as a seed for synthesizing 2D transition metal disulfides (MS_2). This method demonstrates it is possible to accurately control the growth of single- and few-layer forms of these materials at the wafer-scale. Interestingly, this approach also allows the growth of crystalline MS_2 monolayers on various substrates, including quartz, sapphire, Si particles and TiO_2 aggregates. The process is independent of the substrate lattice orientation and surface morphology.
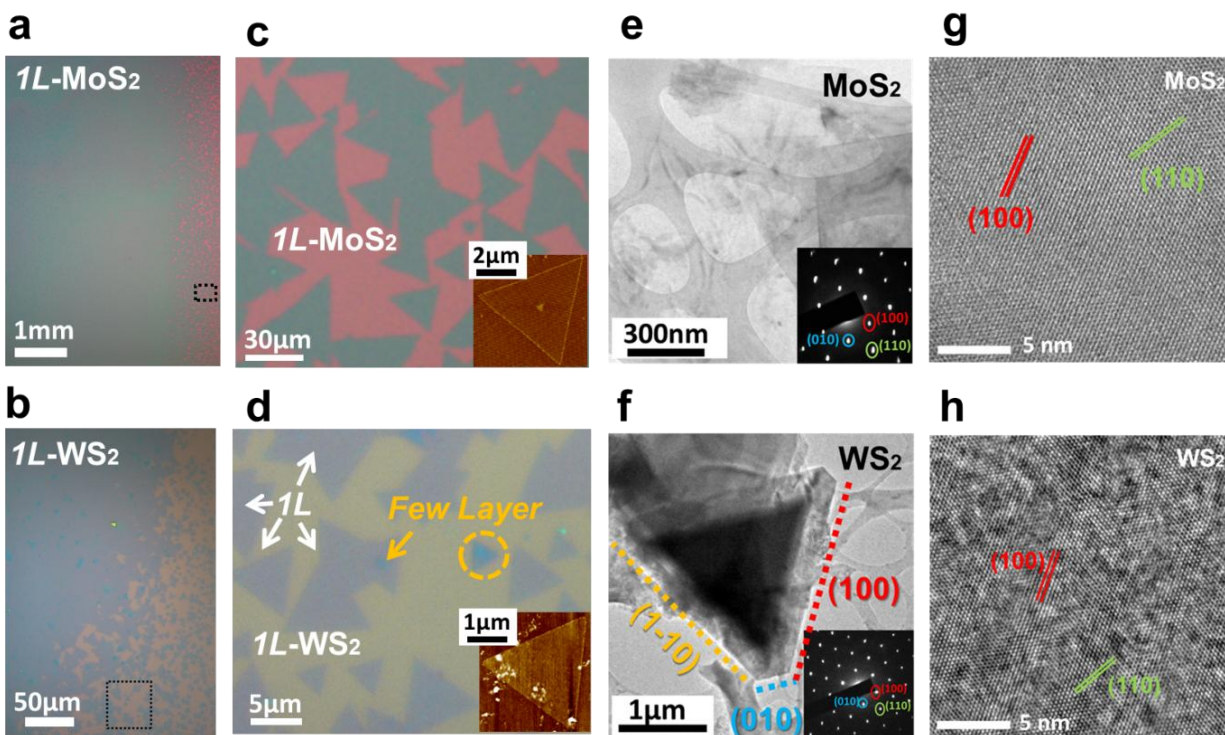
Figure 2-5 Optical microscope images (OM), high resolution TEM images (HRTEM) and selected area electron diffraction pattern (SAED) of single-layer MoS_2 and WS_2 growth by CVD (a, b) OM images of a MoS_2 and WS_2 monolayer near the edge region (c, d) the enlarged OM images in the marked area with the inset showing the corresponding AFM images (e, f) Low magnification and (g, h) high resolution TEM image of as-grown MoS_2 and WS_2 monolayers. Insets in (e, f) show the corresponding SAED patterns.

	temperature	Gas flow	MO₃	S	L
MoS_2	650℃	10 sccm	0.03 g	0.01 g	18cm
WS_2	800℃	7 sccm	1 g	0.015g	20cm

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Table 2-1 Growth conditions for MoS_2 and WS_2 monolayers.

Figure 2-4 shows the experimental set-up for the CVD synthesis of single-layer MoS_2, using S and MoO_3 as the precursor, and perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) as the seed [156]. Following the procedures proposed in Ref. [159], the PTAS solution is first prepared using perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA). The growth substrate is treated with piranha solution and the sample is then sonicated in acetone, IPA and DI water for 10 minutes each to clean away any surface residue. The substrate is then coated uniformly with the aqueous solution of PTAS salt, which was allowed to dry and the PTAS salt crystallized on the sample surface. In the samples shown in Figure 2-5, PTAS solutions of concentration 0.1mM and 5M are used for the synthesis of MoS_2 and WS_2, respectively. A schematic of the synthesis setup is shown in Figure 2-4. The synthesis of MoS_2 and WS_2 uses two precursors in their solid form. The sulfur (S, 99.5%, Alfa) powder is placed in the right ceramic crucible while high purity transition metal oxides MoO_3 (99%, Aldrich) or WO_3 (99%, Aldrich) powders were used as the other reactants for MoS_2 and WS_2 synthesis, respectively. Ar gas flows in the chamber at ambient pressure during the entire growth process. The sample coated with PTAS salt is placed upside-down on top of the second ceramic crucible. During the synthesis, the chamber is heated to the growth temperature, which is typically 650 °C for MoS_2 and 800 °C WS_2, for 5 minutes at a heating rate of 20 °C/min. Table 2-1 lists the detailed parameters used.
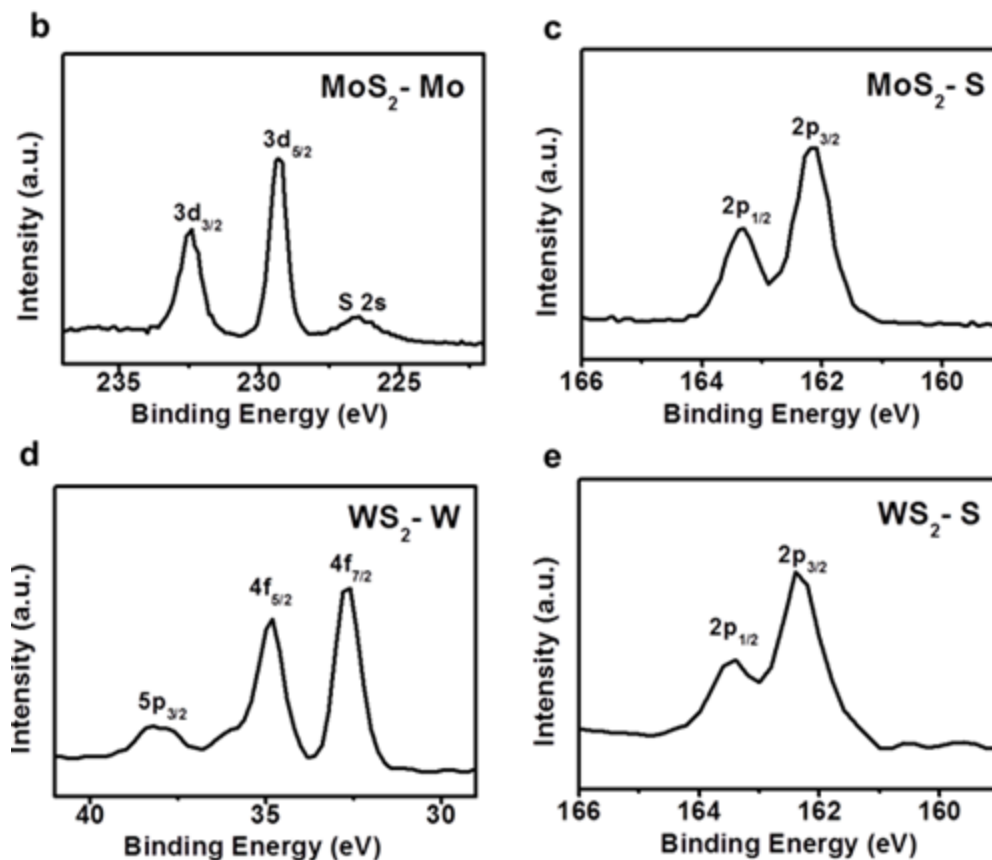
Figure 2-6 The X-ray photoelectron spectra for MoS_2 and WS_2 samples (a) Mo 3d (b) S 2p orbits of the as-grown MoS_2 and (a) W 4f (b) S 2p orbits of the as-grown WS_2.

Figure 2-5 shows the resulting layers obtained using the described growth technique on a SiO_2 substrate. We can see that the growth is initiated at random locations of PTAS crystals and grows outwards in an equilateral triangle shape. Within each triangle, the material is single crystalline while the overall thin film is polycrystalline. From the inset of Figure 2-5(c), we can see that there exists a small triangular island Figure 2-5(d) (see arrows) at the center of the equilateral triangle with the same edge orientation to the underneath single-layer MoS_2 domain. It indicates that the growth may have initiated at the center of each triangular domain where nucleation starts on PTAS seed crystals. An additional layer may also grow near the site at the center of the domain where the seed is located. As shown in Figure 2-5(c) and (d), the resulting MoS_2 and WS_2 thin films have a thickness of 0.71 and 0.86 nm, respectively, as measured by atomic force microscopy (AFM), confirming the 2D crystals are in their single-layer form. The single-crystalline triangular domain can reach tens or even hundreds of micrometers in size before they

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merge with the neighboring domain to form a continuous polycrystalline single-layer thin film on the sample. The growth setup available to us allows the synthesis of centimeter scale samples where the size is only limited by the size of the chamber, which is a 2 inch tube in this case. In the best samples, single-layer MoS_2 and WS_2 cover over 95% of the total sample area. It is also observed that as the domain size increases during the growth, the as-grown domains meet each other during later stages of the growth process where domain boundaries and defects form. Multi-layer region can sometimes form either at the site of these boundary defects at the edges of the domain or at the center of the domain where the nucleation seeds are located. We also notice a few small clusters may sometimes pile up at the edge, indicating the incorporation of adatoms into the crystal of as-grown MoS_2 domains may exist as an energy barrier for the further layer growth. This is reasonable considering the covalent bonding of the in-plane lattice, the facet domain shape and the specific edge orientations. Few inhomogeneous islands and few-layer domains are seen, which may result from an inhomogeneous aggregation of the seeds, as marked in Figure 2-5(d).To further investigate the initial growth of MS_2 with the facet MS_2 domain, the crystal structure and the edge structure of the as-grown MS_2 domains are studied with transmission electron microscopy (TEM). In Figure 2-5(e), (f), (g), (h), the high resolution TEM images of MS_2 and the corresponding SAED pattern with [001] zone reveal the same hexagonal lattice structure with the same lattice spacing of 0.27 and 0.16 nm assigned to the (100) and (110) planes. As shown in Figure 2-5(g) and (h), the domain facets clearly align along (100), (010), and (1-10) planes. In Figure 2-6, the stoichiometry and chemical configurations of monolayer MS_2 are verified with X-ray photoelectron spectroscopy (XPS). These binding energies of MS_2 are consistent with the reported values for MoS_2 and WS_2 [158][160]. The stoichiometry (S/Mo and S/W ratio) of the MoS_2 is 2.01, while that of WS_2 is 1.9, confirming the presence of MoS_2 and WS_2 in the respective samples.
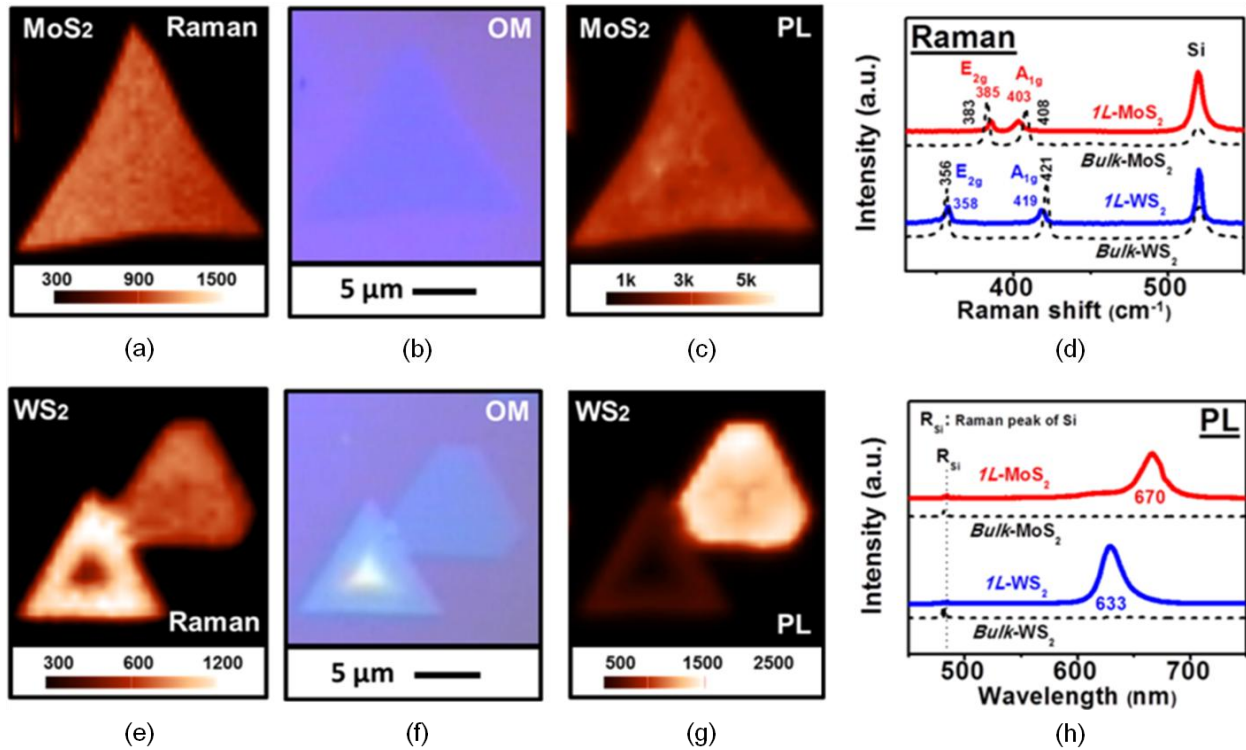
Figure 2-7 Corresponding Raman spectroscopy, optical microscopy (OM), and photoluminacence (PL) mapping of MoS_2 and WS_2. Mapping of (a) Raman peak intensity, (b) OM image, and (c) PL peak intensity of a MoS_2 monolayer; (d) mapping of Raman peak intensity, (e) OM image, and (f) PL peak intensity of WS_2 flakes. Comparisons of MS_2 monolayer and bulk on (g) Raman spectra and (h) PL spectra. Both Raman and PL experiments were performed in a confocal spectrometer using a 473 nm excitation laser. The WS_2 sample shows

Figure 2-7 shows the Raman and photoluminescence (PL) characteristics of single-layer regions of MoS_2 and WS_2. For the MoS_2 sample, we can see that within an individual equilateral triangle, the material is single-crystalline and of high uniformity as indicated by the Raman mapping. For the WS_2 sample, we have shown two triangles, being single- and multi-layer regions respectively. The corresponding optical microscope (OM) images are also given. The PL mapping of both MoS_2 and WS_2 shows a strong PL response for the single-layer regions due to the direct bandgap nature of these materials in their single-layer form. For the multilayer region of WS_2, the direct PL response disappears due to the material having an indirect bandgap as the number of layers increases. The Raman spectrum of single-layer MoS_2 shows characteristic peaks at Raman shift of 385 cm^{-1} and 403 cm^{-1}, corresponding to the E_{2g} and A_{1g} phonon modes. For single-layer WS_2, peak positions for E_{2g} and A_{1g} are at 358 cm^{-1} and 419 cm^{-1}, respectively. The position of the photoluminescence peaks are at 670 nm wavelength for single-layer MoS_2 and 630 nm

wavelength for WS_2, corresponding to direct bandgaps of 1.8 eV and 2.0 eV [24][161][162], respectively. This measurement, however, does not take into account the effects of exciton binding energies and the transport bandgap in these materials can be distinctively higher than the values mentioned above [163].

In Figure 2-5(a), (b), (c), (d), the growth process was interrupted so that the individual triangular single-crystalline regions can be identified. In the best samples, high quality uniform continuous single-layer MoS_2 was obtained. Optical micrograph and Raman spectroscopy confirmed that single-layer MoS_2 with uniformity greater than 95% can be grown at centimeter-scale (Figure 2-8), which is only limited by the size of the reaction furnace. AFM data confirms the thickness of the material is about 6.9 Å, typical of single-layer MoS_2 (Figure 2-8). The success in developing the scalable synthesis of single layer MoS_2 opens the door to many potential applications in electronics, some of which will be discussed in Chapter 6 of this thesis.
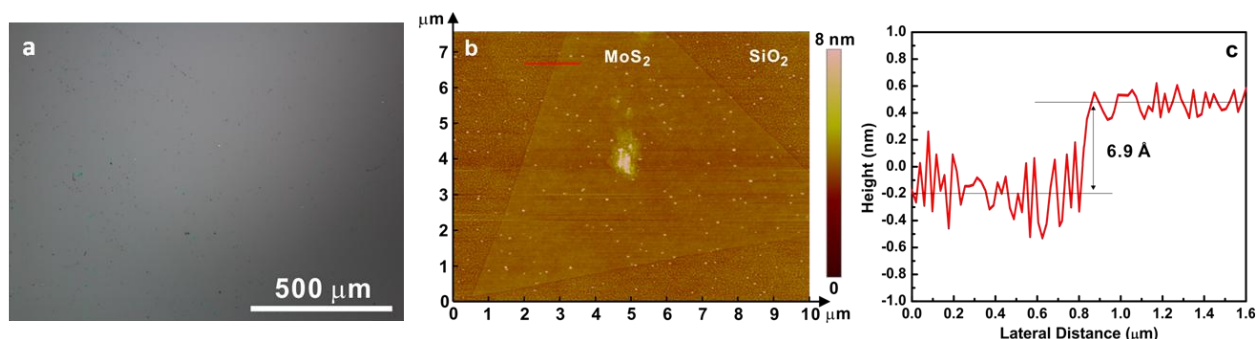
Figure 2-8 Optical micrograph and AFM images of CVD grown single-layer MoS_2 (a) Optical micrographs of single-layer MoS_2 sheets grown by the PTAS-seed based CVD method. MoS_2 obtained shows great uniformity with more than 95% of the area covered by single-layer MoS_2. This is the first time high quality single-layer MoS_2 could be grown at wafer scale. Since the material can be grown directly on any insulating substrates that are stable at the growth temperature, such as SiO_2 and sapphire, no transfer step is required. The material is hence free of wrinkles, which are common sources of mobility degradation frequently associated with the transfer of CVD grown graphene. (b) AFM images and (c) cross-sectional profiles of the single-layer MoS_2 thin film grown by CVD. The coated PTAS seeds act as a nucleation site to initiate the growth. In this sample, the CVD growth process is intentionally stopped before the growth initiated from neighboring seeds merges. The AFM image hence shows the single-layer MoS_2 grown in an equilateral-triangle pattern that is determined by its underlying lattice structure. The CVD single-layer MoS_2 in Figure 2-8(c) has a thickness of 6.9 Å, typical for single-layer MoS_2 sheets.

Chapter 3. Graphene Device Technology

The main theme of this chapter focuses on developing graphene transistor technology. The work is focused on transistors on large-area CVD graphene and addresses issues from CVD graphene mobility, contact resistance, dielectrics, and the general fabrication technology of graphene devices. A new virtual source carrier injection model is also developed to understand the device behavior and its virtual source carrier injection velocity. Other issues related to the transport study and current saturation in graphene FETs are also discussed.

3.1. Device Fabrication

Here, we discuss the general process for fabricating graphene field-effect transistors. The discussion in this sub-section aims to give a detailed description of the process and various techniques used in the construction of high performance graphene devices. Some of the issues discussed here, such as mobility and contacts, are also fundamental to many other applications of graphene in electronics and optoelectronics.
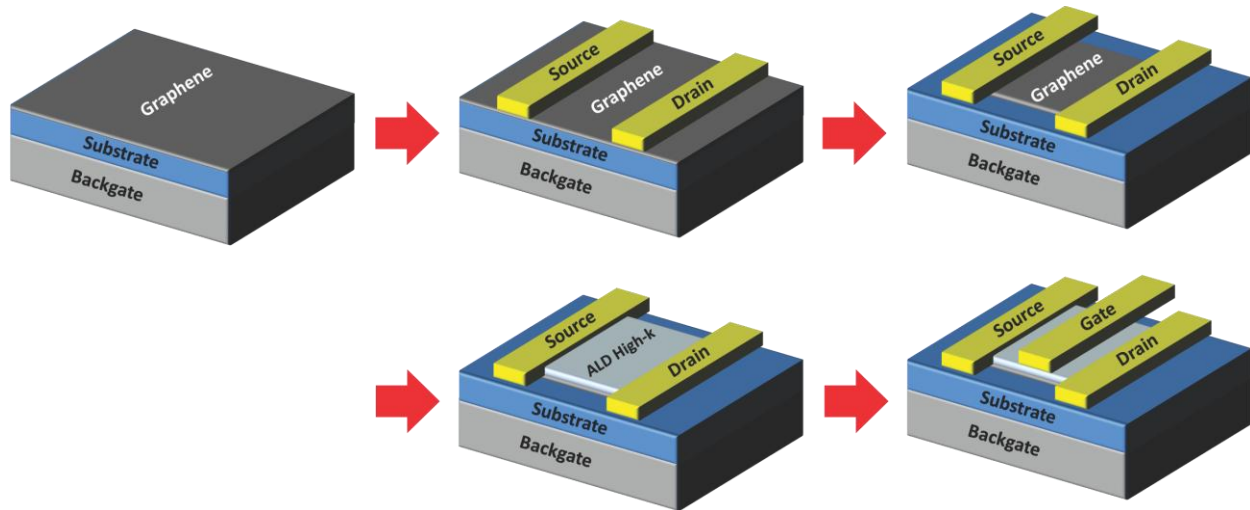
Figure 3-1 Process for fabricating graphene field effect transistors. Graphene is first placed on any arbitrary substrate using the transfer process following CVD growth. Optical or e-beam lithography defines the source and drain contact region where appropriate metals are deposited by e-beam evaporation or sputtering. Device isolation is then achieved by patterned etch using oxygen plasma. The high-k gate dielectric is deposited by atomic layer deposition (ALD). Typical dielectrics used include Al_2O_3 and HfO_2. The deposition of dielectrics is often assisted by the inclusion of a seed-layer to promote adsorption of precursors and subsequent nucleation during the ALD process,

which is made more challenging due to the lack of dangling bonds on graphene surface. The gate electrode is defined and metalized in the final step to form the complete transistor structure.

Figure 3-1 illustrates the general process for building graphene transistors. The fabrication of the GFET typically starts with a sample where graphene thin film is placed on top of a supporting substrate. There are also reports about field effect transistors fabricated on suspended graphene thin film [164], in which case the process can be very different from the substrate-based fabrication. Since the study of suspended graphene device is beyond the scope of this thesis, we only introduce the substrate based technology here, which provides more robust and reliable ways for making graphene transistors that may lead to eventual applications at industrial scale. Here, the substrate can be any arbitrary wafer material and even flexible substrates like plastics, paper and textile. The ohmic contacts of the GFETs are formed by depositing a 2.5 nm Ti/ 45 nm Pd/ 15 nm Au metal stack by e-beam evaporation. Device isolation is achieved by O_2 plasma etching for 20s at 50 W of RF forward power with 20 sccm of gas flow rate that mixes He and O_2 in 4:1 ratio.

The dielectric of the device, which provides a medium for achieving electrostatic control of the channel by the gate, plays a very important role in influencing the performance of the device. The interface between the gate dielectric and graphene also causes carrier scattering and induce charge trappers in a similar way as the substrate. Depositing dielectrics on top of graphene has always been a challenging process due to the lack of dangling bonds on the 2D material surface, where the strong sp^2 hybridized bonds are all in plane while only weak π-band exists perpendicular to the 2D sheet. The gate dielectric for graphene transistors is typically formed by an atomic layer deposition (ALD) process, which is a commonly used technique for depositing oxides, nitrides and also metal thin films. An ALD deposition cycle usually involves exposure of the sample to a sequence of gas phase chemical reactants, called the precursors. Most ALD processes involve two such precursors. In each ALD cycle, the precursors are adsorbed sequentially onto the sample surface where reaction takes place in a self-limiting manner. In most cases, each reaction cycle leads to the formation of an atomic or molecular layer of thin film and thicker films can be deposited by repeating the same reaction cycle for as many times as required to achieve the desired film thickness. The final film thickness can be confirmed by

ellipsometry measurements. A typical ALD process consists of repeated cycles of the four characteristic steps: 1. Exposure of the sample to the first precursor. The first precursor is usually an organometallic compound. 2. Purging the reaction chamber to remove the un-reacted precursors and by-products from the first step. 3. Exposure of the sample to the second precursor. In some processes, other treatment, such as exposure to plasma, is also used to complete the monolayer thin film formation and reactivate the surface for reaction with the first precursor. 4. Purging the reaction chamber. The ALD process is generally a surface-controlled process with self-limiting reactions, which give rise to extremely uniform thin film deposition conformal to the surface.

The adsorption of the precursors on graphene surface is often more challenging than on materials with 3D lattice where plenty of unsatisfied bonds can assist the reaction during the atomic layer deposition (ALD) process typically used for high-k material formation. Low temperature processes to reduce the desorption rate, chemical functionalization based methods for promoting precursor adsorption, and seed based techniques to allow better nucleation have all been attempted in the literature with a variation of dielectric quality and resulting mobility in the graphene underneath. Typical gate dielectrics used for GFETs in the literature are Al_2O_3 [165], SiO_2, HfO_2 [166], and special polymer layers [119]. Due to the inert nature of the graphene surface, the formation of gate dielectric on top of graphene often needs a pre-deposition initialization step, which can either be a process to create nucleation sites, or a chemical functionalization step, to promote its adhesion. Recent work by the researchers in IBM [166] developed a new process where the gate is buried, the dielectric is directly deposited on top of SiO_2 substrate, and then graphene is transferred on top of the dielectric layer. In this way, 4 nm of high quality HfO_2 can be deposited as the gate dielectric for GFETs. However, such methods using buried gate may cause other problems such as an unprotected surface and exposure of graphene to air that can harm the performance of the GFETs. In our work, the typical dielectric deposition exploits a two-step seeding-and-growing process to form high-k dielectrics. For example, a 15 nm layer of Al_2O_3 can be formed by first depositing a 3 nm Al layer on the graphene surface by electron-beam (e-beam) evaporation, which is then naturally oxidized in air. This first Al_2O_3 film serves as the initial nucleation layer to promote adhesion of the subsequent 12 nm of Al_2O_3 deposited by atomic layer deposition (ALD), using H_2O as the precursor and

trimethyl aluminum (TMA) as the Al source [165].

Finally, the top gate is formed with low resistivity metal to reduce gate resistance, typically a 30 nm Ni/ 200 nm Au/ 50 nm Ni metal stack is used in our work, but many other options for the metal stack are possible so long as the resistance can be kept low and the metal stack can stick well to the gate dielectric.

The process mentioned above should be viewed as only a general framework of graphene device fabrication while many variations of the process has been reported by various groups in the literature and also in later sections of this thesis. Some special technology exists, for example, in building graphene devices designed to operate at radio frequency (300 MHz~300 GHz). T-shape gate process is sometimes used to reduce gate resistances by allowing a larger cross-sectional area while still keeping a very short channel length to facilitate rapid carrier transition across the device. Self-aligned processes are also used to reduce access resistances of the device. Some of these topics will be discussed in more details in Chapter 4.

3.2. Carrier Mobility

In the past two centuries, many theories of electrical conduction have been formulated to explain the movements of carriers and the observed electrical properties of materials, with various degrees of success. But it is not until the extended development of quantum mechanics theory that a generally acceptable picture of electrical transport took shape. The carrier density n and mobility μ are the two key parameters defined under the modern theory of electrical conduction that can characterize the intrinsic transport and conduction properties of materials. In this section, we characterize the mobility of graphene on various substrates using several different techniques including Hall effect measurements, field-effect measurements, and also using the Fourier-Transform Infrared (FT-IR) measurements of the frequency dependent Drude conductivity.

3.2.1. Carrier Mobility from Hall Effect

The fundamental physical principle underlying Hall effects is the Lorentz force, which is the vector combination of two basic forces: the electric force and the magnetic force. When a charge carrier moves along an electric field in the presence of a magnetic field that is perpendicular to

its direction of motion, the carrier also experiences a magnetic force $-q\boldsymbol{v} \times \boldsymbol{B}$ acting at right angle to both directions as often determined by the right hand rule. The total force is the Lorentz force $\boldsymbol{F}$, equal to $-q(\boldsymbol{E} + \boldsymbol{v} \times \boldsymbol{B})$. q is the elementary charge, E is the electric field, v is the carrier velocity, and B is the magnetic field. For given values of $\boldsymbol{B}$, the measured value of current I, and the measured hall voltage v_{H}, the sheet carrier density can be determined as:

$$n_s = \frac{IB}{q|V_{H|}}$$

(3-1)

Since Van der Pauw structures can be used to measure the sheet resistivity R_S of graphene and R_S is inversely proportional to both sheet carrier density and mobility, Hall mobility can be obtained as follows:

$$\mu = \frac{|V_H|}{R_S I_B} = \frac{1}{q n_s R_S}$$

(3-2)

To measure the Hall mobility of CVD graphene, Hall-bar structures were fabricated using the standard fabrication process on various substrates. Figure 3-2(a) compares the Hall mobility and its dependence on carrier density of Cu-mediated CVD graphene transferred onto SiO_2 substrates with that of exfoliated and SiC epitaxial graphene on various substrates. The mobility of CVD graphene is in the range of 1000 to 4000 cm^2/V.s for sheet carrier density in the range of 10^{12} to 10^{13} cm^{-2}.

To study the transport properties in graphene, the graphene/300 nm SiO_2 samples were measured in the temperature range of 4.2 to 300 K at high vacuum of 10^{-6}~10^{-8} Torr. Figure 3-3 shows the mobility dependence on carrier density for single-layer graphene at different temperatures. The mobility generally reduces with increasing carrier density and it also decreases with increasing temperature, especially above 200 K. At low temperature, the behavior can be explained by a combination of Coulomb scattering by impurities and short-range scattering by defects in graphene. The overall mobility is related to the total scattering rate, which can be

calculated using Matthiessen's rule: $\frac{1}{\mu_{total}} = \frac{1}{\mu_C} + \frac{1}{\mu_{sr}}$. The Coulomb scattering limited mobility μ_C was typically independent of carrier density in single-layer graphene and is a constant while the short-range scattering limited mobility was inversely proportional to n_s. The solid lines in Figure 3-3 shows the fit to the data using this relation and μ_C is extracted to be around 5000 cm^2/V.s. Assuming a drift-diffusion transport, the mean free path can also be estimated using $\ell = \hbar\mu\sqrt{\pi n}/q$. At characteristic carrier density $n = 3 \times 10^{12}$ cm^{-2}, we have $\ell \sim 80$ nm at room temperature in the CVD samples presented in Figure 3-3.

Figure 3-4 shows that the mobility of single layer graphene decreases as temperature increases, especially at temperatures above 200 K. The carrier density and temperature dependence of mobility suggests the key scattering mechanism shifts from Coulomb to phonon scattering as carrier density and temperature increase. At temperature above 200 K, carrier scattering became dominated by surface polar phonons of the SiO$_2$ substrate, which produce an electric field that influence the potential variations in graphene lattice. The strength of coupling decreases exponentially with the separation between the substrate and the graphene sheet. Since the scattering rate due to surface polar phonon can be expressed as:

$$\frac{1}{\tau_{sub}} \propto \sum_i \frac{c_i}{e^{\hbar\omega_i/k_BT} - 1}$$

(3-3)

we have $\hbar\omega_1 = 59$ meV and $\hbar\omega_2 = 155$ meV being the two main surface phonon modes in SiO$_2$. This explains the temperature dependence of mobility. On the other hand, the dielectric screening of Coulomb scattering and short-range scattering limited mobility both usually have very weak dependence on temperature for $k_BT \ll E_F$.
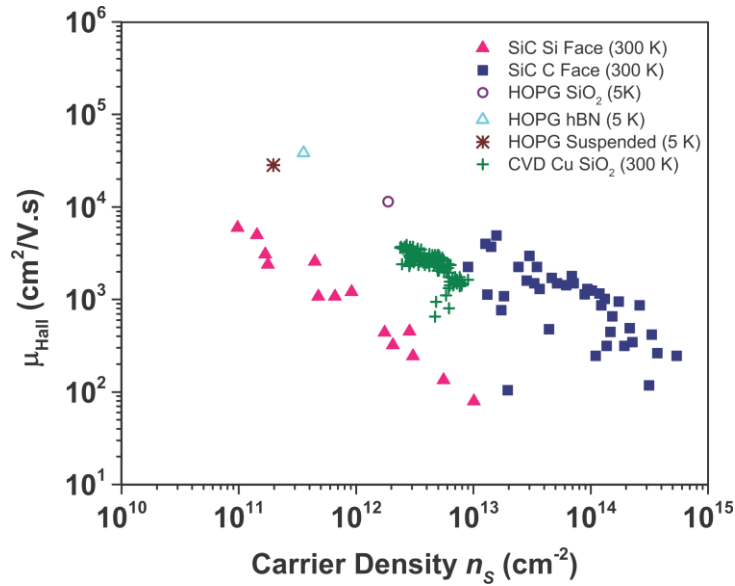
Figure 3-2 Comparison of Hall Effect mobility in CVD, HOPG and SiC graphene placed on various substrates at room temperature. The exfoliated HOPG graphene shows the highest mobility compared to CVD graphene and graphene from vacuum graphitization of SiC. Suspended HOPG graphene and HOPG graphene on h-BN substrate, both from exfoliation, shows mobility around 30,000 to 50,000 cm^2/V.s at 5 K. HOPG graphene on SiO_2 substrate shows a mobility around 10,000 cm^2/V.s at 5 K with carrier density of 2×10^{12} cm^{-2}. CVD graphene grown on Cu and transferred to SiO_2 substrate shows higher mobility than graphene grown on the Si-face SiC, but lower mobility than C-face SiC.
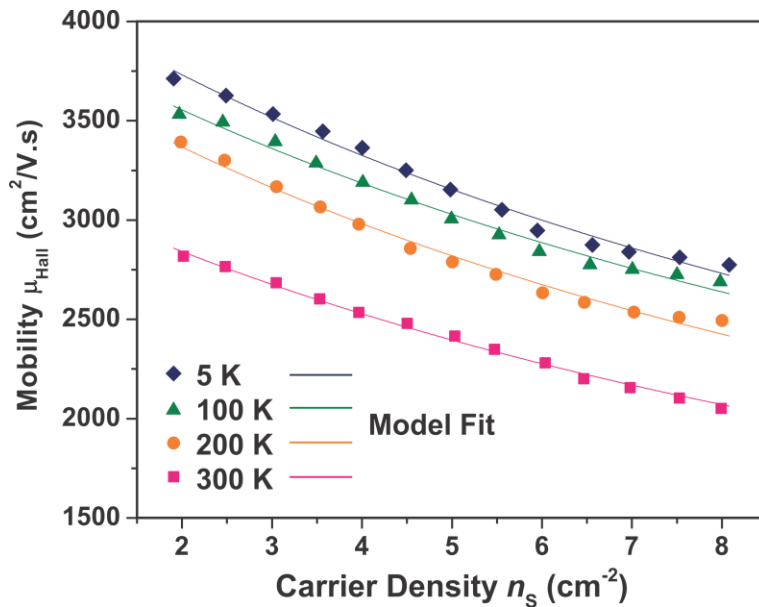
Figure 3-3 Carrier density and temperature dependence of carrier mobility in graphene. Dependence of Hall mobility for holes on carrier densities in monolayer graphene at temperatures from 5 K to 300 K. At low temperature, the dominant scattering mechanisms are Coulomb scattering by charged impurities and short range scattering by lattice

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defects. The symbols show the measured data while the solid lines are model fit using $\frac{1}{\mu_{total}} = \frac{1}{\mu_C} + \frac{1}{\mu_{sr}}$. At temperature above 200 K, the thermally excited surface polar phonons of the SiO_2 substrate will start to play a significant role in limiting the carrier mobility.
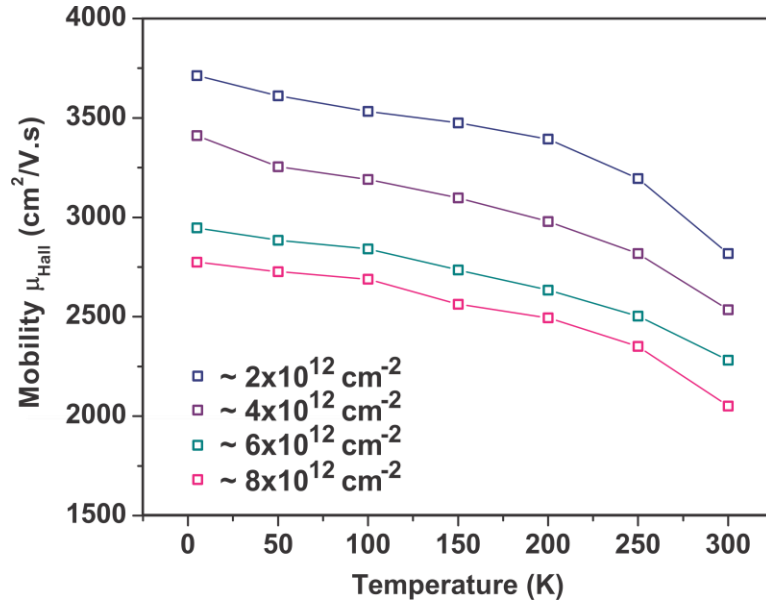
Figure 3-4 Temperature and carrier density dependence of carrier mobility in graphene. Dependence of Hall mobility for holes on temperature in monolayer graphene at carrier density from 2×10^{12} cm^{-2} to 8×10^{12} cm^{-2}. The mobility in monolayer graphene decreases more rapidly with increasing temperature when the temperature is above about 200 K. This is primarily due to scattering by thermally excited surface polar phonons of the SiO_2 substrate.
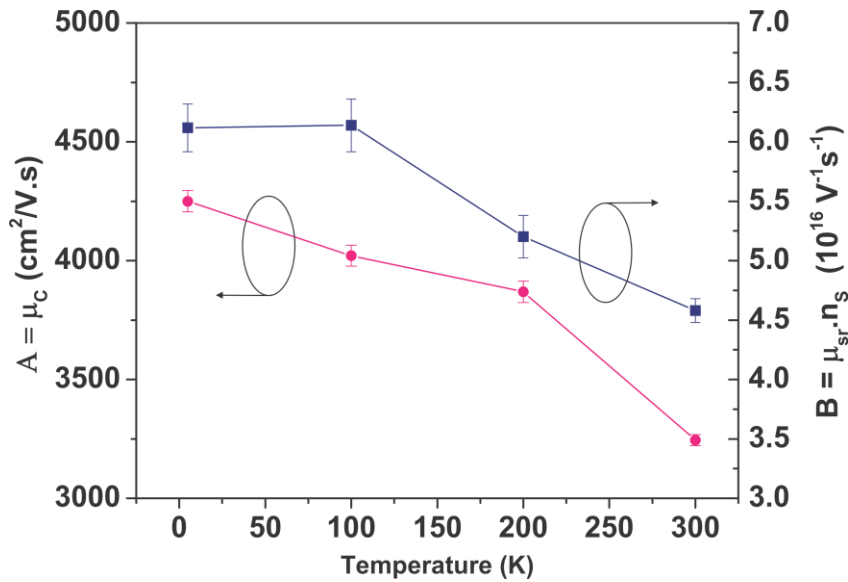
Figure 3-5 Dependence of μ_C and $B=\mu_{sr}.n_s$ on temperature as extracted in Figure 3-3. Both μ_C and B decease as temperature increases, indicating increasing scattering rate with temperature that is related to scattering by substrate surface polar phonon.

3.2.2. Carrier Mobility Extraction from Electric Field Effect

The carrier mobility can also be extracted from the field effect modulation of conductivity in transistor devices. The field effect mobility is defined by the derivative of the Drude formula:

$$\mu_{FE} = \frac{1}{C}\frac{d\sigma}{dV_G}$$

(3-4)

where C is the capacitance leading to the field effect modulation of charges. σ is the DC channel conductivity and V_G is the bias on the modulating gate. The contact resistances will have an effect on the extracted field effect mobility if two-probe measurements are used, often leading to an underestimation of the actual mobility. The effect of contact resistance on the extracted field effect mobility can be described by eq. (3-5) and eq. (3-6)

$$\mu_{FE} = \frac{g_m(V_G)}{V_{DS}C_{ox}}\frac{L_{DS}}{W} = \frac{\mu_{Hall}(V_G)}{\left(\frac{2R_C}{R_{sh}(V_G)}\frac{W}{L_{DS}}+1\right)^2}$$

(3-5)

$$R_{tot} = \frac{V_{DS}}{I_D} = 2R_C + \frac{1}{q\mu_{Hall}\sqrt{n_{imp}^2 + C_{ox}/q(V_G - V_{Dirac})}}\frac{L}{W}$$

(3-6)

where L_{DS} is the drain-source separation; V_{DS} is the drain-source bias; R_C is the contact resistance; n_{imp} is the impurity charge, C_{ox} is the gate capacitance, V_{Dirac} is the charge neutrality point; g_m is the transconductance; μ_{Hall} is the Hall mobility; R_{sh} is the sheet resistance of graphene.

Figure 3-7 shows the field effect mobility extracted for two graphene devices. Two different processes were used when fabricating these two transistors, resulting in different contact resistances due to metal/graphene interface quality for the respective devices. The details of the

two fabrication processes and analysis of contact resistance will be discussed in Section 3.3.2. The dotted lines are fit to the data using eq. (3-5). The total resistances of the devices are plotted as a function of the back-gate bias in Figure 3-6(a) (with the dotted lines in Figure 3-6(a) fitted using eq. (3-6)) while the corresponding output characteristics are shown in Figure 3-6(a).

(a)   (b)
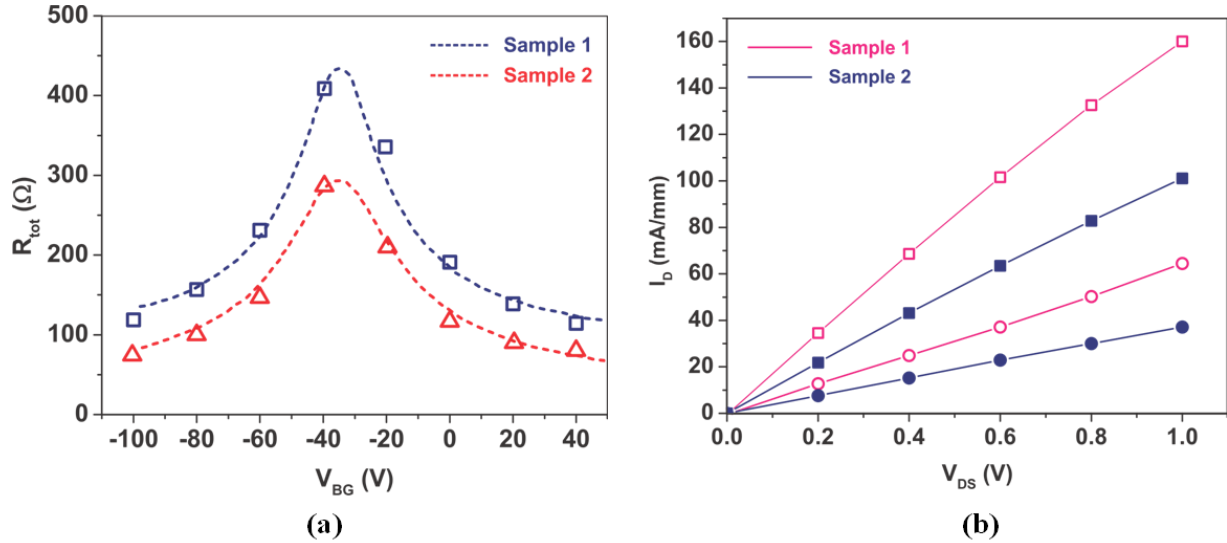
Figure 3-6 Total resistance and output characteristics of two graphene transistors fabricated using the standard process and the inorganic sacrificial layer process as illustrated in Figure 3-14. (a) Total resistance versus V_{BG} for samples 1 and 2 including fitting from eq. (3-6), L_{DS} = 6 μm. (Squares) Dirac point and (Circles) $n_p= 6 \times 10^{12}$ cm^{-2}. (b) I_D versus V_{DS} for samples 1 and 2.
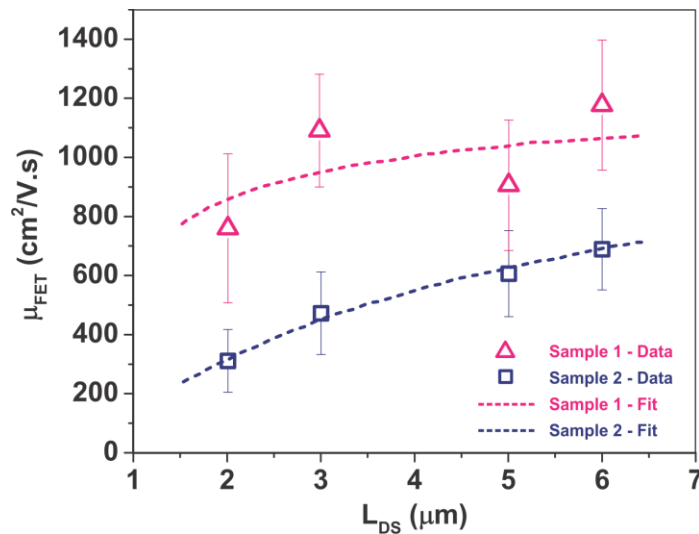
Figure 3-7 Field effect mobility of two graphene transistors fabricated using the standard process and the inorganic sacrificial layer process as illustrated in Figure 3-14. Field effect mobility μ$_{FET}$ versus L$_{DS}$. (dotted lines) Fits from

eq. (3-5) (fit parameters: μ_{Hall} = 1200 cm^2/V.s. The contact resistance in Sample 1 is five times higher than the contact resistance in Sample 2).

The higher contact resistance of Sample 1 results in its higher total resistance and lower output current levels compared to Sample 2 under similar bias conditions. Due to the contact resistance effect, the field effect mobility extracted for Sample 1 using the 2-probe method is significantly higher than in Sample 2 (Figure 3-7), though the data for both devices in Figure 3-7 can be fitted with the same value of Hall mobility of 1200 cm^2/V.s. The improved contact resistance in Sample 1 allowed a better agreement between μ_{FET} and μ_{Hall} than that in Sample 2. The Hall mobility μ_{Hall} in both of the samples was measured between 2000–3000 cm^2/V.s depending on the carrier concentration at 300 K (see Figure 3-3 and Figure 3-4).

Fitting Parameters from eq. (3-6); μ_{Hall} = 1200 cm^2/V.s		
	RcW ($\Omega.\mu m$)	n_{imp} (10^{12} cm^{-2})
Sample 1	132-573	1-1.2
Sample 2	1955-2440	0.9-1.0

Table 3-1 Fitting parameters used in Figure 3-7

3.2.3. Scattering Rate and Carrier Mobility from Dynamic Drude Conductivity

The dynamic conductivity of materials can be understood based on the classical Drude model. When light passes through graphene, the absorption of light due to band-to-band transition is restricted by Pauli blocking where the transition can only happen for absorption of light at frequencies corresponding to energy above $2\Delta E_F$ (Figure 3-8). On the other hand, there is also a response peak at low frequency corresponding to the Drude dynamic conductivity. Transmission and absorption spectrum measurements of light passing through graphene often carry the signature of this dynamic conductivity and the resulting spectrums provide alternative methods for extracting carrier scattering rate and carrier mobility in graphene that relies fully on optical measurements.

In the 1900, Paul Drude proposed a classical model that can partially describe the behavior of moving carriers in a conductor. The model applies well for explaining DC and AC conductivity and the Hall Effect near room temperature in conductors. Under the Drude model, the movement of conduction electrons resembles the particles in an ideal electron gas. The only interaction

between electrons and lattice ions, impurities or lattice defects is by direct collision. The model makes the independent electron assumption, which ignores any long-range interaction between the electron and the lattice ions or between the electrons. Using a Nicolet-8700 FT-IR spectrometer in combination with a liquid-helium-cooled silicon bolometer, the response of carriers in the 2D electron gas of large-area single-layer CVD graphene to incoming light excitation can be characterized in the far-infrared frequency range. On the same sample, we characterize the transmission spectrum through a reference area without graphene T_0 and through the graphene area T. The extinction ratio, $1-T/T_0$, was then obtained, which strongly depends on the dynamic conductivity $\sigma(\omega)$ of the graphene sheet as follows:

$$1 - \frac{T}{T_0} = 1 - \frac{1}{\left|1 + \frac{Z_0\sigma(\omega)}{(1 + n_{sub})}\right|^2}$$

 (3-7)

Here, ω is the frequency of the incident light, n_{sub} is the refractive index of the SiO$_2$ substrate. Z_0 is the vacuum impedance. $\sigma(\omega)$ is the dynamic conductivity. The dynamic conductivity of a conductor can be derived based on the classical Drude model where we have the following equation of motion for an individual carrier in conductor.

$$m\frac{d\boldsymbol{v}}{dt} = q\boldsymbol{E} - m\frac{\boldsymbol{v}}{\tau}$$

(3-8)

m is the effective mass; $\boldsymbol{v}$ is the carrier velocity and $\boldsymbol{E}$ is the applied external electric field. The equation is a basic statement of the classical relation between the acceleration of a carrier and the total force that is exerted on it. The first term on the right side of the equation describes the electromagnetic force on the carrier due to the incident light and the second term accounts for the carrier scattering, which resembles a damping term or a macroscopic friction force proportional to -$\boldsymbol{v}$. If we have oscillating AC input electrical field acting on the carriers in a conductor, the dynamic conductivity is related to the Drude weight D, the frequency of the incident light ω and the scattering width Γ as follows:

$$\sigma(\omega) = \frac{iD}{\pi(\omega + i\Gamma)}$$

(3-9)

Eq. (3-7) and (3-9) leads to the following relation:

$$\Rightarrow \quad 1 - \frac{T}{T_0} = 1 - \frac{(1 + n_s)^2}{\left[(1 + n_s) + \frac{P_1 \cdot P_2}{x^2 + P_2^2}\right]^2 + \left[\frac{P_1 \cdot x}{x^2 + P_2^2}\right]^2}$$

$$\text{where: } \omega = x, \, P_1 = \frac{Z_0 D}{\pi} \Rightarrow D = \frac{\pi P_1}{Z_0}, \, P_2 = \Gamma$$

(3-10)

Hence, by fitting eq. (3-10) with P_1 and P_2 as the fitting parameters to the measured data, we are able to extract both the scattering width and the Drude weight. Since the Drude weight is proportional to $\sqrt{n_s}$, the carrier density can be extracted as follows:

$$D = \frac{v_F \cdot e^2}{\hbar}\sqrt{\pi|n_s|} \Rightarrow n_s = \frac{1}{\pi}\left[\frac{D}{2\pi\left(\frac{e^2}{h}\right) \cdot v_F}\right]^2$$

(3-11)

Finally, the mobility of carriers is related to the Drude weight, the carrier density and the scattering width.

$$\mu = \frac{D}{e \cdot n_s \cdot \pi \cdot \Gamma}$$

(3-12)

Figure 3-9(a) shows the schematic illustration of the device and measurement setup. Figure 3-9(b) shows the FT-IR spectroscopy setup. We first measured and computed the extinction ratio spectrum of the CVD graphene sample with respect to a backgate bias from -50 V to 50 V in step of 10 V (Figure 3-10(a)). The test structure has CVD graphene grown using the Cu-mediated

method and transferred onto 90 nm SiO_2 with low-doping Si as the backgate. The laser spot has a diameter of 2 mm. The back-gate bias modulates the carrier density in graphene, leading to changes in its dynamic conductivity and hence the measured extinction ratio. At low frequency, the extinction changes from 35% to 5 % as the back-gate sweeps from -50V to 50V. At higher frequencies, the change in extinction ratio is smaller, but the electrical modulation of Drude conductivity is significant in the entire range of frequencies measured from low frequency below 50 cm^{-1} wave-number (1.5 THz) to above 600 cm^{-1} wave-number (18 THz). The modulation of Drude conductivity by electrical biasing allows the dynamic conductivity of the materials at THz frequency to be changed by electrical signals. The results clearly demonstrated the potential of graphene devices for THz modulator and mixer applications in optoelectronic communication. More importantly, the method allows a new way to extract the transport properties of graphene.

By fitting eq. (3-10) to the measured extinction ratio data, we can extract the Drude conductivity D and scattering rate Γ of the single-layer graphene film. Figure 3-10(b) shows the fitted curves and the measured data for the extinction spectrum. For the clarity of display, we only show data points for every 20 V change in V_{BG}, as well as the data at V_{BG}=0 V, but the model fits the data very well at all bias points. Figure 3-10(d) shows the corresponding total scattering rate as a function of carrier density. The extracted dependence of carrier mobility and Drude weight D on the carrier density is shown in Figure 3-10(c). The carrier mobility shows a similar dependence on the carrier density measured from Hall-bar structures as previously noted in Figure 3-3 with μ increasing from slightly above 1000 cm^2/V.s at 1.7×10^{13} cm^{-2} to around 4000~5000 cm^2/V.s at low carrier density below 10^{12} cm^{-2}. The $1/\mu = 1/\mu_C + 1/\mu_{sr}$ relation is fitted (solid green line) to the extracted mobility dependence on carrier density, which gives a Coulomb scattering dominated mobility $A = \mu_C = 4066$ cm^2/V.s and the short-range scattering coefficient of $B=\mu_{sr}n_S = 2.5 \times10^{16}$ $V^{-1}s^{-1}$. Again, the Coulomb dominated mobility is almost independent of the carrier density and the scattering at high density is dominated by short-range carrier scattering.
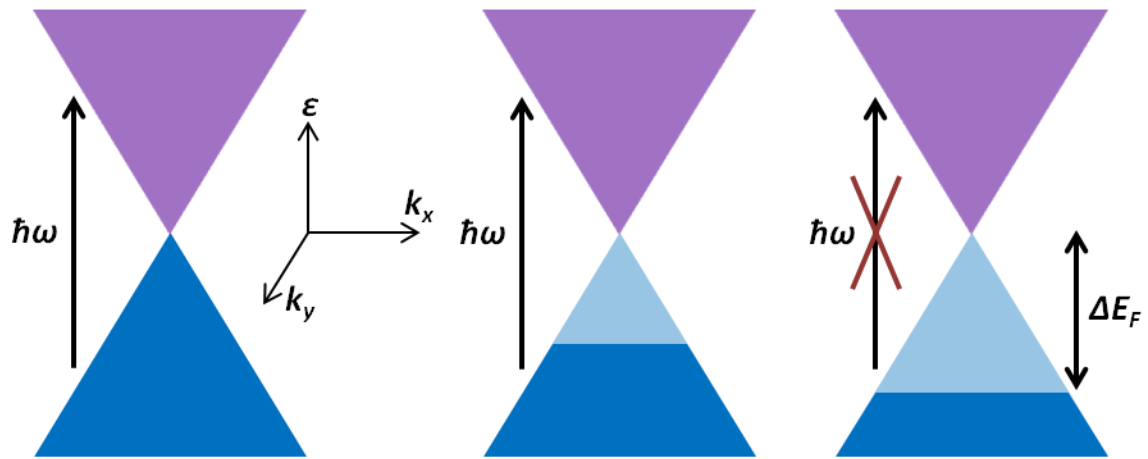
Figure 3-8 Schematic band structure of graphene for various levels of doping (only one valley is shown) and Pauli blocking of photon absorption in graphene.
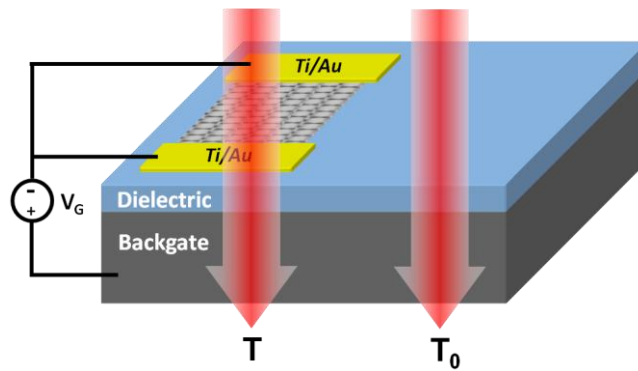
Figure 3-9 Schematic illustration of the FT-IR measurements in determining the extinction spectrum of graphene subject to electrostatic bias. The modulation of carrier density in graphene leads to changes in its dynamic conductivity and response to the incident far-infrared electromagnetic waves.
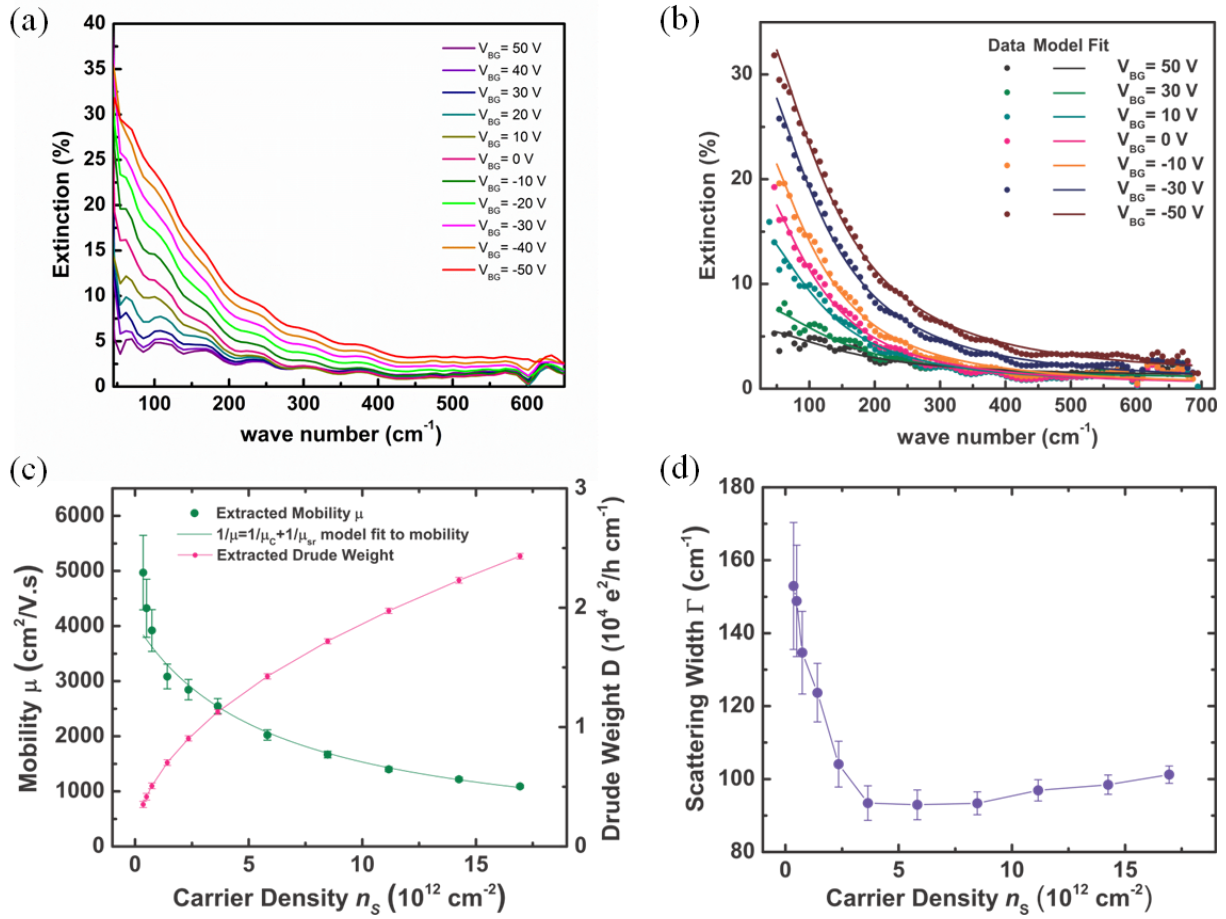
Figure 3-10 Extinction spectrum of CVD graphene sample subject to electrical biasing by the back-gate (a) Extinction spectrum of the graphene sheets at various back-gate bias conditions applied through 285 nm SiO_2 dielectric. As V_{BG} various from -50 V to 50 V, the extinction ratio is modulated by up to 30% at low frequency. (b) Model fit eq. (3-7), eq. (3-9), eq. (3-10) to the measurement data. Only the bias conditions V_{BG} from -50 to 50 V in step of 20 V and $V_{BG}= 0$ V are shown for clarity while the model fits the measurement data well at all bias conditions. Following eq. (3-11) and eq. (3-12), the mobility, Drude weight and carrier density can all be extracted. (c) Extracted mobility (green dots and solid line) and Drude weight (pink dots and solid line) as a function of carrier density. (d) Extracted scattering rate as a function of carrier density. All measurements were performed at room temperature in a nitrogen environment.

3.3. Metal Contacts for Graphene

Contact resistance is an important aspect of any electronic and optoelectronic devices that determines the efficiency of carrier injection from external circuitry to the intrinsic device region. Achieving a low contact resistance is imperative for developing graphene device applications. Based on the present technology, the contact resistance of graphene transistors (~200–2,000

$\Omega.\mu m$ [167][168][169][170]) is still higher than in Si MOSFETs (20–50 $\Omega.\mu m$ [171]), but is almost comparable to some III-V devices. The contact resistance contributes to the total source and drain access resistances of the device, R_S and R_D. Large R_S and R_D increase the time required to charge and discharge the various capacitances in the intrinsic transistor, which is also known as the parasitic delay time, and hence limits the short-circuit current gain cut-off frequency f_T of the transistor, an important figure of merit for the high frequency performance of a transistor that is related to the intrinsic speed of carrier movement in the device. In addition, large R_S and R_D also reduce the maximum oscillation frequency f_{max} of the device, which characterize the high frequency power gain of a transistor, since these resistive components are sources of power loss, which degrades the device power gain. A more in-depth definition of both f_T and f_{max} of transistors will be given in Chapter 4.
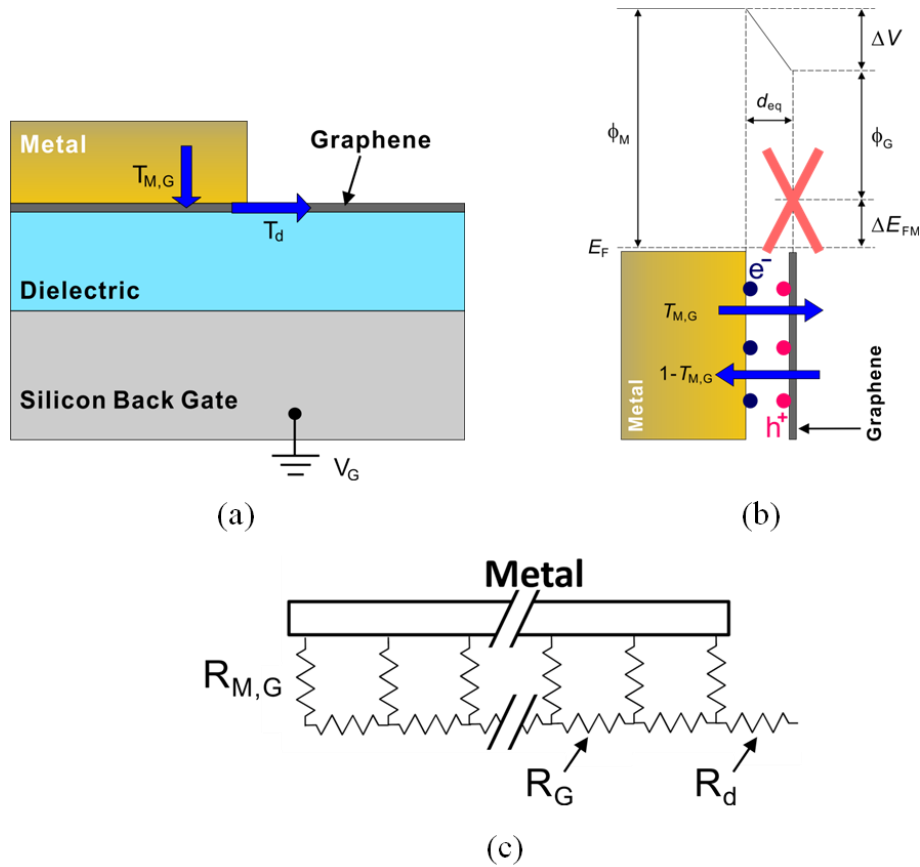
Figure 3-11 Schematic representation of metal/graphene contacts (a) Schematic of the basic structure of a metal/graphene contact interface. Many factors affect the contact resistance. The two key processes of carrier movements are transmission of carrier across the metal/graphene interface and transport of carrier out of the graphene region under the metal contact. (b) Schematic of the electronic band as seen by the carriers transmitting

between metal and graphene. ϕ_G and ϕ_M are the workfunctions of monolayer graphene and metal respectively. ΔE is the Fermi level position of graphene relative to the Dirac point. The shift of Fermi level away from the Dirac point is due to the combined effects of both the impurity doping in graphene and doping by the contacting metal. ΔV is the total built-in potential difference between graphene and metal. d_{eq} is the equilibrium separation between the metal and graphene. $T_{M,G}$ is the transmission coefficient of carrier injection from metal to graphene. (c) Schematic of the key components contributing to the contact resistance. $R_{M,G}$ is the inverse of conductivity for carrier injection from metal to graphene. R_G is the resistance of the monolayer graphene underneath the metal contact. R_d accounts for any additional barrier to carrier movement out of the contact region.

Figure 3-11 shows a detailed schematic of the graphene-metal junction. There are three major contributions to the contact resistance in graphene devices: 1) the interface quality, 2) the sheet resistance of graphene underneath the metal, and 3) the effect of the work function mismatch between the graphene underneath the metal and the graphene in the channel. The most common metal selection is that of Ti/Pd or Ti/Au contacts, due to the previous work in carbon nanotube contacts, which simulates strong interactions between titanium or palladium with carbon as predicted by density functional theory [172][173].

Unfortunately, there is still a large dispersion in the literature for the contact resistance between graphene and these metal layers. This is probably due to the high sensitivity of graphene-metal contacts to the fabrication technology and contamination. As mentioned previously, organic residues due to the use of polymer resist during device fabrication are often difficult to remove from the graphene surface due to van der Waals forces and the inability to use oxygen plasma to clean up photoresist residue after lithography. Various routes to ensure clean interfaces have been proposed, including a controlled oxygen descum [168] and the use of an Al_2O_3 sacrificial layer [174]. Recent work at IBM [175] also shows a strong dependence of the contact resistance on the size of the contact metal when the size of the metal pads scale below the transfer length. This poses new challenges for scaling graphene devices to the deep sub-micrometer regime.

3.3.1. Contact Resistance Characterization

The resistance of the metal/graphene contact can be extracted using the transmission line measurement (TLM). This technique relies on characterizing the scaling behavior of the total resistance for a series of metal/graphene contacts separated by a range of distances. Standard semiconductor characterization probes are used to apply a voltage between each pair of contacts and the resulting current flowing between the contacts is measured, which will give the total

resistance between the contacts. Since the current is injected from the first probe into the contact, which flows through the sheet of graphene and is collected at the second contact by the other probe, the total resistance of any two contact structure as measured by this technique is a linear combination of the two contact resistances and the resistance of the sheet of graphene in-between. Typically, 4-probe techniques are used to separate the current measurements, using probe 1 and 4, from the voltage measurements, using probe 2 and 3. This will eliminate the error resulting from possible potential drop in the current measuring probes using 2-probe technique.

   If the total resistance is measured for several two contact structures with the contacts separated by a range of distances, we can plot the total resistance as a function of the distance separating each pair of contacts. If normalized with respect to the length and width of the graphene channel, we will have a linear plot where the slope is related to the sheet resistance of graphene and the y-intercept is resistance of two contacts forming the test structure. We first measure the total resistance of six back-gate graphene devices with drain-source separation from 2 μm to 12 μm at 300 K with a drain bias of 10 mV. The use of transmission line measurement for extracting the contact resistance is justified since the source-drain separation is much larger than the mean-free-path of carriers and the transport is fully diffusive. Figure 3-12(a) plots the total resistance as a function of back-gate bias where the minimum conduction point is at 29 V with minimum variations across the six devices. Figure 3-12 shows the Pd/graphene contact resistance as characterized by TLM technique. The contact resistance has a clear dependence on the back-gate bias. This is because the back-gate can electrostatically dope the graphene under the contacts. A heavier electrostatic doping increases the carrier density, and hence the conductivity, of graphene and lead to reduction in the R_G contribution to the contact resistance as shown in Figure 3-11. The contact resistance is close to 250 ±25 Ω.μm in the heavily p-type doped region (V_G-V_{Dirac}= -30 V) and 290 ±30 Ω.μm in the heavily n-type doped region (V_G-V_{Dirac}= 30 V) (Figure 3-12). In addition, the p-type branch shows a lower contact resistance than the n-type branch, indicating that the Pd/graphene junction favors p-type carrier injection due to the large work-function of Pd. The contact resistance increases significantly close to the Dirac point, reaching around 900 Ω.μm, due to the graphene becoming more resistive. The error bar also increases due to the total resistance becoming larger and slight variation in V_{Dirac} can leads to greater error. Larger resistance values are also used in extrapolating the contact resistances, resulting in large absolute

error. Figure 3-13(a) shows the dependence of contact resistance on temperature. For the heavily p-doped region (V_G-V_{Dirac}= -25 V), the contact resistance decreases with temperature from 250 ±25 Ω.µm at 300 K to 195 ±25 at 10 K. For the heavily n-doped region (V_G-V_{Dirac}= 25 V), the contact resistance decreases with temperature from 320 ±25 Ω.µm at 300 K to 220 ±25 at 10 K. The solid lines are linear fits to the respective data. This trend of decreasing contact resistance with temperature is mainly due to the improving carrier mobility in the graphene region underneath the metal contacts (Figure 3-13(b)), leading to improved conductivity of graphene at low temperature and hence lower R_G contribution to the contact resistance (Figure 3-11). The electron and hole mobility of graphene increase from around 2000 cm^2/V.s to 3500 cm^2/V.s and from around 2200 cm^2/V.s to 3800 cm^2/V.s as temperature reduces from 300 K to 5 K.

(a)   (b)
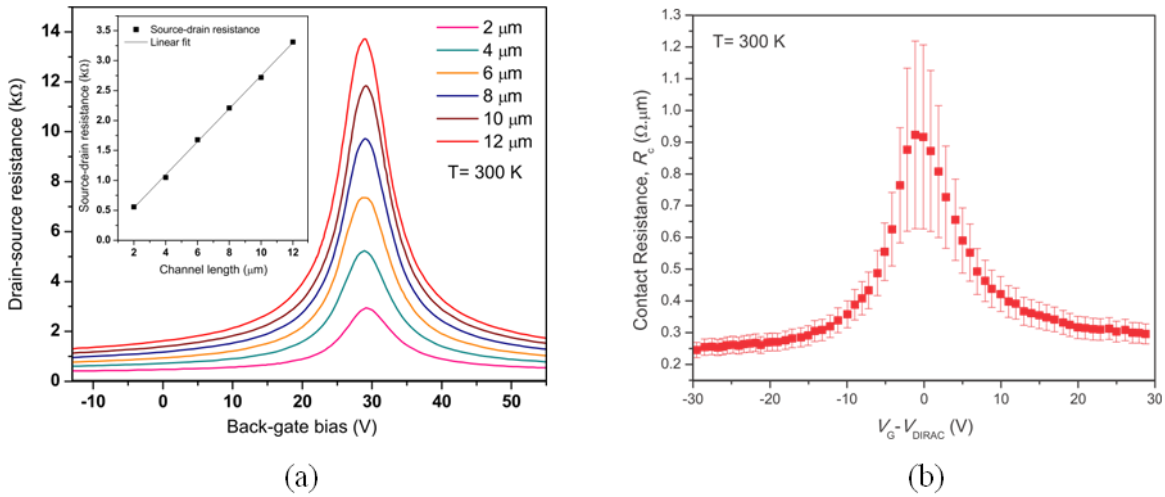
Figure 3-12 Pd/Graphene contact resistance at 300 K (a) Extraction of Pd/graphene contact resistance by transmission line methods (TLM). Source-drain resistance of six devices with source-drain separation from 2 to 12 µm at T=300 K. Inset: source-drain resistance vs. channel length of the devices, T= 300 K and V_{BG}=40 V. The linear fit allows the extraction of sheet resistance from the slope and contact resistance from the intercept with the vertical axis. (b) The extracted contact resistance as a function of V_G-V_{Dirac} at T=300 K.

(a)   (b)
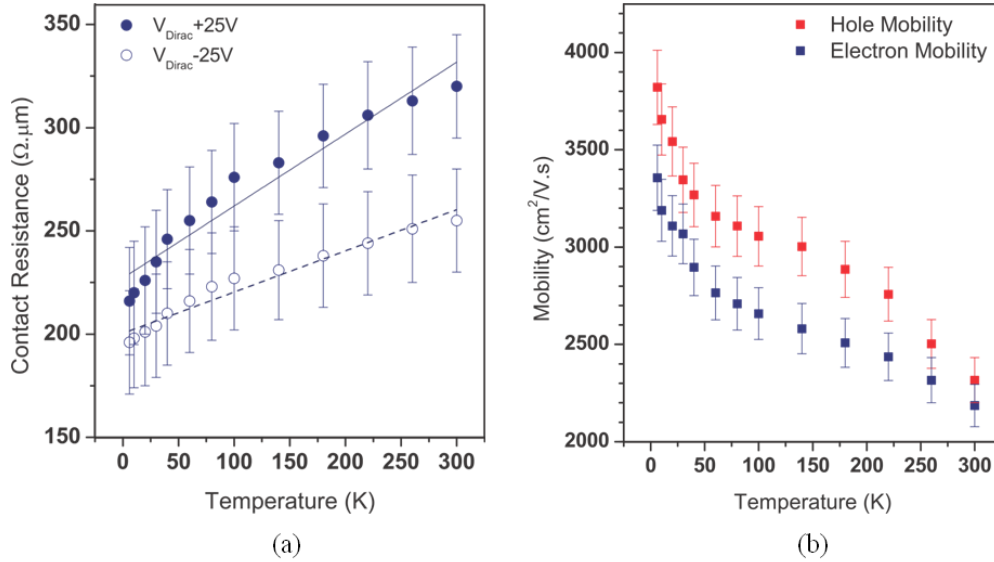
Figure 3-13 Temperature dependence of Pd/Graphene contact resistance and carrier mobility for electron and hole carriers in graphene (a) Pd/Graphene contact resistance versus temperature for electron and hole carriers in the graphene under the metal region. The back-gate is biased to V_{Dirac}+25 V and V_{Dirac} -25 V. The contact resistance reduces from around 300 Ω.μm at 300 K to 220 Ω.μm at 5 K for n-type carriers; and reduces from around 250 Ω.μm at 300 K to 195 Ω.μm at 5 K for p-type carriers. The Pd contact favors p-type carrier injection to graphene. The decrease in contact resistance with temperature is mainly due to the increasing mobility of graphene. (b) temperature dependence of mobility in graphene for electron and hole carriers.

(a)   (b)
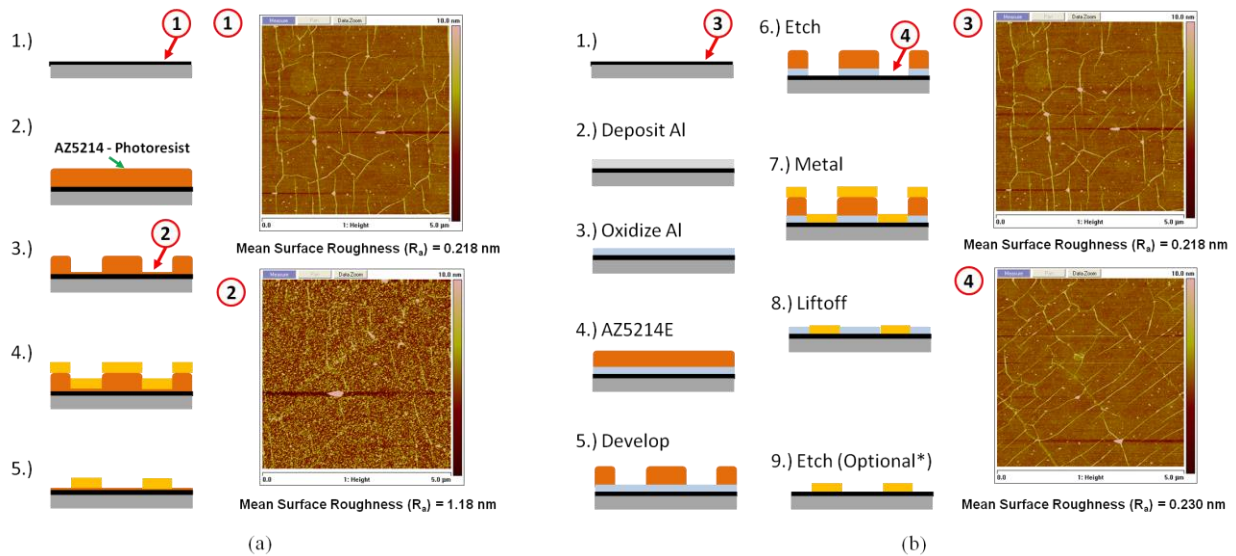
Figure 3-14 Standard and inorganic sacrificial layer processes for making metal/graphene contacts. Process flow for (a) Sample 1 going through the standard process and (b) Sample 2 going through the inorganic sacrificial layer process. The AFM characterization of graphene sample surfaces (for Sample 1 and Sample 2) before and after the two lithography processes, respectively, are also shown.

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3.3.2. Effect of Metal/Graphene Interface Quality on Contact Resistance

In the early stage of graphene technology development, the surface contaminants play a significant role in limiting the contact resistance of graphene transistors. The most significant sources of the contamination may be due to the various steps of the device fabrication process, particularly when organic resists are used during lithography and graphene transfer. Figure 3-14(a) shows the AFM characterization of the graphene surface immediately after it has gone through an optical lithography step using AZ5214E resist, but before the ohmic metal has been deposited. The graphene surface immediately following the resist development shows a surface arithmetic-mean roughness R_a and a root-mean-square roughness R_q of 1.18 and 1.00 nm, respectively. For comparison, a CVD graphene sheet transferred onto a reference SiO_2/Si wafer without further processing results in R_a= 0.218 nm and R_q= 0.2 nm. The quality of the graphene surface is clearly compromised due to the resist residues leftover after development. Such contaminations exist from most resists, including the e-beam resists such as PMMA that is commonly used for graphene transfer and patterning. Traditionally, oxygen plasma ashing is used to remove organic residue leftover from resist processing in creating a clean surface for ohmic metal deposition. However, such treatments exhibit low selectivity between the organic compound of the resists and graphene. Another technique commonly used to remove organic resist residue after graphene transfer is by forming gas annealing. This method is not suitable for the liftoff process due to the high temperature > 200 °C that can lead to resist reflow.

Here, we introduce a new process for forming ohmic contact that can allow a clean graphene surface to be preserved before ohmic metal deposition. The key idea is to use an inorganic sacrificial layer between the organic resists and the graphene surface. The inorganic sacrificial layer, which can be removed after patterning and before metal deposition through acidic etching, prevents the graphene sheet to be in direct contact with the organic resists during the patterning process, allowing a much cleaner surface to be preserved. Figure 3-14(b) highlights the new fabrication process and its comparison with the standard contact technology. Sample 2, which went through the inorganic sacrificial layer process, had a 5-nm Al cap layer deposited by electron-beam (e-beam) evaporation and oxidized under ambient conditions after transfer to the Si wafer, whereas Sample 1, which went through the standard process, did not have one. Device fabrication starts with the patterning of the ohmic contacts shown in Figure 3-14. A metal stack

with 1.5-nm Ti/45-nm Pd/15-nm Au is deposited by e-beam evaporation and patterned by liftoff with AZ5214E photoresist and AZ422 developer. In Sample 2, the Al cap layer is etched by the AZ422 developer, which contains dilute tetra-methyl ammonium hydroxide (TMAH), leaving a pristine graphene surface behind, as described in Figure 3-14(b). To ensure a uniform gate dielectric between ohmic contacts, as well as electrical isolation, the remaining Al cap is then removed using AZ422.

Figure 3-6 and Figure 3-7 show the total resistances and output characteristics of two devices on Sample 1 and Sample 2. Table 3-1 shows the extracted contact resistances and the fitting parameters used based on eq. (3-5) and (3-6) and in extracting the contact resistance. With a cleaner interface before ohmic metallization in Sample 2, the contact resistances are reduced from 2000–2500 $\Omega \cdot \mu m$ in Sample 1 to 200–500 $\Omega \cdot \mu m$. The estimated contact resistance values for Sample 2 also agree well with transmission-line measurements (TLM). This method of extracting the contact resistances based on eq. (3-5) and (3-6) offers a way to estimate the contact resistance directly from transistor current-voltage relations.

3.4. DC Analysis of Graphene Field Effect Transistors

3.4.1. DC Analysis of Graphene FETs

  A typical graphene transistor takes the usual form of a field-effect device,

Figure 3-1, where the carrier is injected from the source and collected at the drain. The carrier transport across the channel region is determined by the quality and properties of the channel materials itself, the dielectric medium that encapsulates the channel, and also the potential profile along the channel that is influenced by both the gate and drain biases. The gate controls the current flow both by modulating the carrier density in the channel and by influencing the carrier dynamics. The first graphene device showing field-effect carrier modulation was developed by Novoselov el al. [54] on exfoliated graphene and through the use of a 300 nm thick SiO_2 dielectric with doped silicon as the back gate. The thickness of the dielectric is specifically chosen [176] to allow direct identification of single- and few-layer graphene using optical microscope through their difference in optical contrast.

Many models have been developed to reproduce the electrical charge and conduction in graphene exist [1][76][177][178]. Most of these, however, focus on the first-principle calculation of band structure, tunneling effects and carrier transport. These models are generally insufficient or too complex and resource-intensive for device and circuit-level modeling. Models derived from first principles and the massive computational modeling/simulation that is usually associated with it can sometimes obscure the key physical insights behind the GFETs operation. For engineering applications, it is often critical to increase the understanding of device operation, allowing timely identification of problems and optimization of device performance. For this purpose, it is often useful to develop compact physical models that can elucidate sufficient device physics to allow general analysis and optimization of device performance. In this section we will focus on developing a compact analytical description of graphene devices that is also sufficient for explaining practical operation of graphene FETs.

Over the past few years, a few device level models have also been proposed for graphene field-effect transistors (GFET) [179][180][181][182]. Ref. [179] and [180] present two different device level models for bi-layer GFETs with bandgaps tunable by a vertical electric field. Ref. [181] proposes a low complexity current-voltage model for Schottky-barrier graphene nanoribbon (GNR) transistors and Ref. [182] derives a device model for GFETs based on epitaxial graphene on SiC. However, the results of all these models [179][180][181][182], though giving great insight into the device physics, has not been compared to any experimental data.

A quasi-analytical modeling approach for GFETs with gapless large-area graphene channels is presented in Ref. [183]. The model allows the calculation of the I-V characteristics, the small-signal behavior, and the cutoff frequency of GFETs. Another compact physical model for GFETs was presented in Ref. [184] and [185]. This model was derived directly from conventional MOSFET models [186][187][188] and gives a qualitative explanation of graphene transistor operation in the ambipolar region. However, the empirical square-root charge-voltage relation used in Ref. [184][185] does not distinguish between electron and hole charges, preventing quantitative physical insight into device operation in the ambipolar region. In addition, both models (Ref. [183][19] and Ref. [184][185]) are only validated with experimental data from long-channel GFETs ($L_G > 1$ μm). Hence, their applicability to sub-micrometer short-channel

GFETs, which should dominate potential high frequency electronic applications, still awaits verification.

Recently, a new class of semiempirical physics-based compact models strictly based on carrier charge and transport has been proposed for short-channel Si MOSFETs [189][190][191][192]. In this thesis, this virtual source model is extended to GFETs, with the goal of providing a simple and intuitive understanding of the underlying carrier transport in graphene transistors, as well as to provide the basis for a numerically efficient compact model. The model shows very good agreement with experimental data with only a small set of fitting parameters and is valid for predicting the I-V characteristics of GFETs, accounting for the combined effects of drain-source voltage (V_{DS}), top-gate voltage (V_{TGS}) and back-gate voltage (V_{BGS}). The model also quantitatively describes the ambipolar region as a combination of a p-type and an n-type channel, and can allow the extraction of the source carrier injection velocity for benchmarking the performance potential of GFETs against conventional RF transistor. The model can potentially be implemented in Verilog-A codes for simulating graphene circuit performance.

3.5. Source Injection Velocity Model for Dual-gate Graphene Field Effect Transistors

Figure 3-15 shows the general structure of the GFETs and defines the main variables used in this paper. The operation of the ambipolar graphene transistors differ significantly from unipolar Si MOSFETs. The channel charges contributing to current are always electrons in n-channel Si MOSFETs and always holes in p-channel Si MOSFETs in all regions of operation of the devices. In GFETs, however, the conduction in this zero bandgap material is by electrons at high gate bias when the Fermi level is above the charge neutrality point at every point in the channel (Region I in Figure 3-17), and by holes at low gate biases when the Fermi level is below the charge neutrality point anywhere in the channel (Region III in Figure 3-17). However, in the region where the device channel transits from n-type to p-type, the conduction is by both electrons and holes. This is called the ambipolar region (Region II in Figure 3-17), and was first explained in Ref. [184]. Assuming $V_{DS}>0$, the channel conduction in this region is by electrons injected from the source and holes injected from the drain, which meet and recombine in pairs at a point in the channel. Hence, the channel conduction in a GFET exhibits characteristics of an n-type FET, a p-

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type FET and also the transitional ambipolar behavior with both an n-type section and a p-type section in the channel, depending on bias conditions. The model proposed in this section divides the characteristics of a GFET into these three operation regions. The boundaries between the three operation regions are determined by the position of the recombination point (also called "the minimum charge point" in some literature) along the channel for given bias conditions. Specifically, the device is in the ambipolar region (Region II) if the recombination point exists between the source and drain in the channel. Otherwise, the device is in Region I or III. We will start by deriving the current-voltage relation in each operation region of the device. Then, the position of the recombination point and hence the operation region boundaries will be explicitly derived for operation Region II. It is important to note that while the device is symmetrical we define here as "Source" the terminal that is sourcing electrons (sinking holes) and "Drain" the terminal that is sinking electrons (sourcing holes).
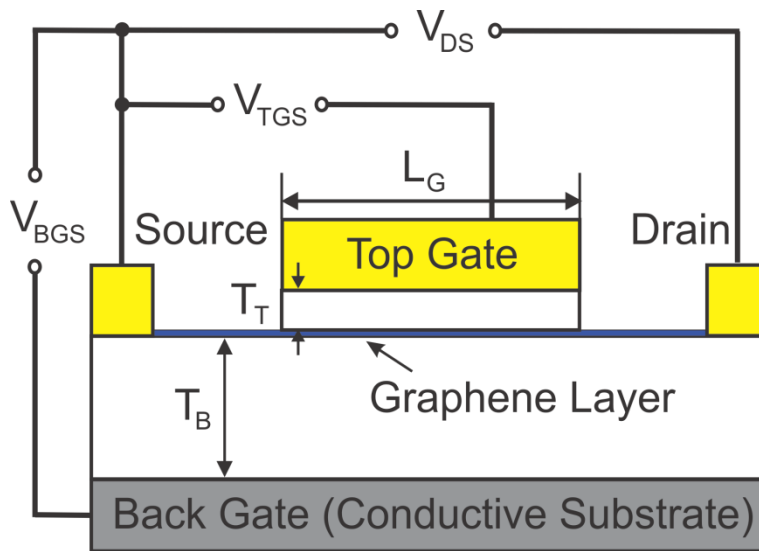
Figure 3-15 Diagram of the graphene device analyzed in this work and definition of key voltage variables.
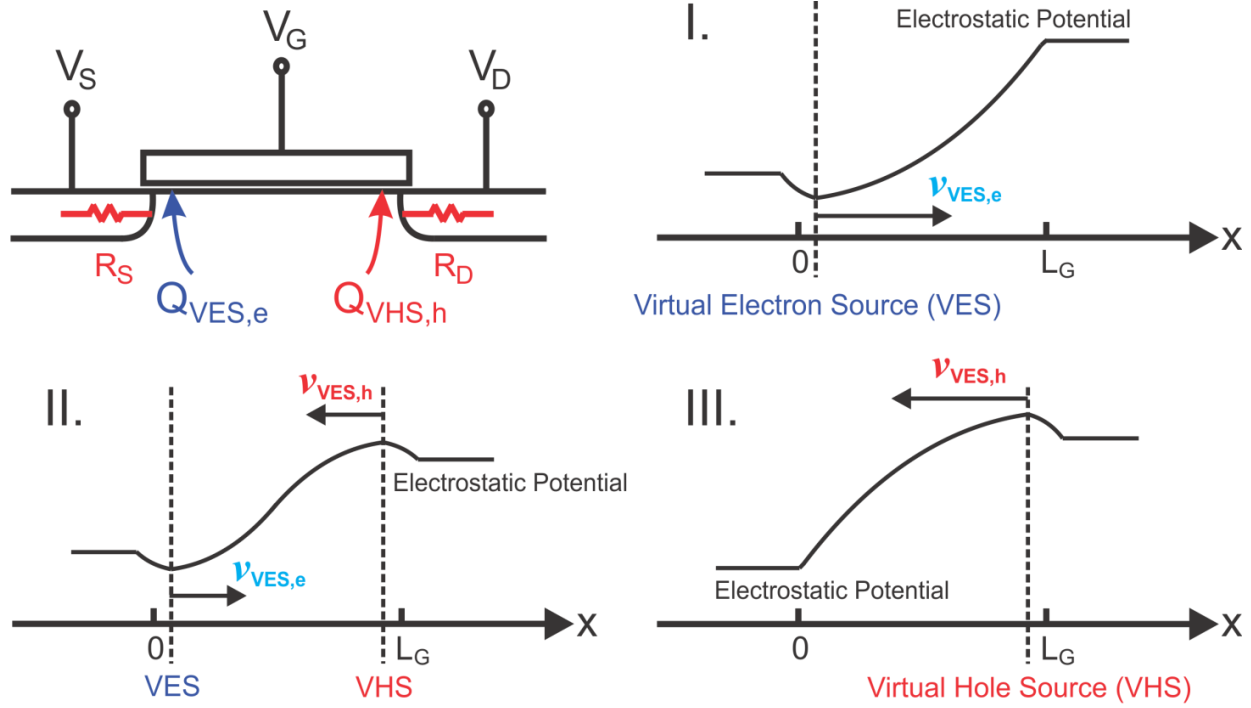
Figure 3-16 Schematic diagram of the cross-section of a GFET device and electrostatic potential profile alongt he channel. The virtual electron source (VES) point and the virtual hole source (VHS) point in the channel are defined for a GFET. The electrostatic potential along the channel and the position of VES and VHS are shown for a GFET operating in each of the three operating regions as defined in Figure 3-17. Unless it is explicitly stated otherwise, all sheet charge density and carrier velocity for n-type and p-type channel used in this paper are defined at the virtual electron source and the virtual hole source respectively.
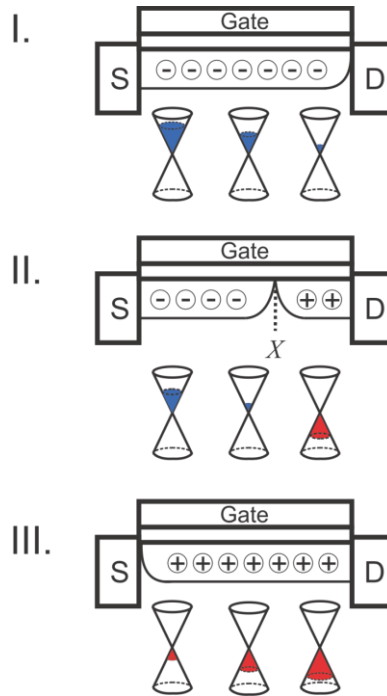
Figure 3-17 Conical-shape band structure and distribution of charge carriers in the channel at different operation regions of GFETs. Assuming $V_{DS}>0$, in Region I: the device has n-type carriers everywhere in the channel. In Region II: the device has n-type carriers at the source side of the channel and p-type carriers at the drain side of the channel. This is the ambipolar region. Point X is the recombination point. In Region III: the device has p-type carriers everywhere in the channel.

Device Operation in Region I

When the GFETs are operating in Region I, only electron charge is present in the entire channel and the device operation is similar to that in an n-type Si MOSFET. The virtual source model in [189] can be applied directly to GFETs to describe the conduction in this operation region. At the virtual electron source (VES) defined as shown in **Figure 3-16**, we have the following general relation between current ($I_{DS,I}$), channel sheet charge density ($Q_{VES,e}$), and carrier velocity ($v_{VES,e}$) [189][193][194] that is valid for both saturation and non-saturation regions:

$$I_{DS,I}/W = Q_{VES,e}v_{VES,e}F_s$$

(3-13)

where W is the device width. $v_{VES,e}$ is the local electron carrier velocity at the virtual electron source, which is a very important parameter for modern FETs. Its relation to ballistic transport

velocity v_θ and its importance in limiting the drive current for device operating in the quasi-ballistic regime has been discussed in detail in Ref. [193][194][195][196]. In GFETs, injection velocity carries even greater significance due to graphene's long ballistic transport length (≈ 0.3 µm at room temperature [197][198]). The virtual-source electron charge density induced by the top-gate of the GFET can be approximated by the empirical function in eq. (3-14) [189]. Eq. (3-14) is adopted from the charge-voltage relation previously used in Si MOSFET models [187][188][189], which, as shown in this work, also serves well to empirically reproduce the dependence of the charge on the bias voltages in graphene devices:

$$Q_{VES,e} = C_{TG} n \phi_t \ln\left(1 + \exp\frac{V'_{TGS} - V_{t,e}}{n\phi_t}\right)$$

(3-14)

C_{TG} is the top-gate capacitance per unit area. n is analogous to the sub-threshold coefficient in a Si MOSFET and its value is related to the bandgap of the channel material. In GFETs, n typically has much larger values than in Si MOSFETs due to graphene's zero bandgap. This bandgap-dependent term, which is considered as a fitting parameter in this work, gives the additional flexibility to the model of making it also applicable to bi-layer graphene FETs or graphene nano-ribbon FETs in which significant bandgaps can exist. ϕ_t is the thermal voltage given as $k_B T/q$. V'_{TGS} is the top-gate-to-source voltage of the intrinsic part of the device. $V_{t,e}$ is the effective threshold voltage for gate induced electron charge in the channel, which is given as:

$$V_{t,e} = V_{TG,min} + \Delta V$$

(3-15)

where $V_{TG,min}$ is the top-gate voltage at the point of minimum conductance and is given as (Ref. [184]):

$$V_{TG,min} = V_{TG,min0} + \frac{C_{BG}}{C_{TG}}\left(V_{BG,min0} - V'_{BGS}\right)$$

(3-16)

The effect of the back gate voltage V'_{BGS} on channel charge is explicitly modeled as a shift to the overall top gate minimum conduction point $V_{TG,min}$. C_{BG} is the back-gate capacitance per unit

area. $V_{BG,min0}$ is the back-gate minimum conduction point voltage. V'_{BGS} is the intrinsic back-gate-to-source voltage. $V_{TG,min0}$ is the top-gate voltage at the minimum conduction point without the back-gate effect. ΔV accounts for the difference between $V_{TG,min}$ and the effective threshold voltage for electron charge $V_{t,e}$. In principle, ΔV can be experimentally estimated from the drain current-gate voltage characteristics of the GFET, but it is considered as a fitting parameter here. In this work, V'_{TGS}, V'_{BGS} and V'_{DS} will be referred to as the *intrinsic voltages*, i.e. the voltages that are applied to the intrinsic transistor region, given by the externally applied voltage corrected for potential drops across the access regions: $V'_{TGS} = V_{TGS} - I_{DS}R_s$, $V'_{DS} = V_{DS} - I_{DS}(R_s + R_D)$ and $V'_{BGS} = V_{BGS} - I_{DS}R_s$. V_{TGS}, V_{BGS} and V_{DS} will be referred to as the *external voltages*.
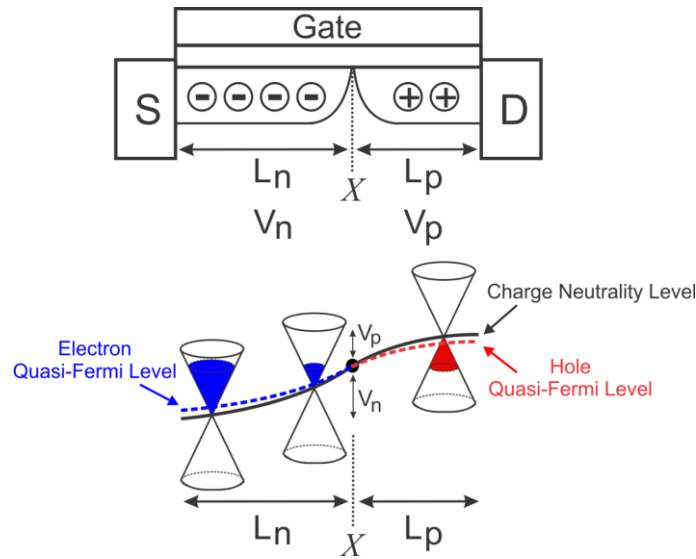
Figure 3-18 Schematics of the cross-section of a GFET operating in ambipolar region and the charge distribution in the channel. The charge neutrality level is also shown, which connects the charge neutrality points for all positions along the channel. The dotted line shows the variation of quasi Fermi levels along the channel. Due to the semimetallic nature of graphene, the quasi Fermi levels for electrons and holes closely follow the potential profile in the channel. Point X is the recombination point. L_n and L_p are the length of the n-type and p-type sections of the channel respectively. V_n and V_p are the potential drop across the respective n-type and p-type sections.

In eq. (3-13), F_s is introduced as a saturation factor to empirically describe the transition of device operation from non-saturation to saturation region when the drain-to-source voltage increases. Similar to the saturation function proposed for Si devices in Ref. [189] adopted from [199][200], F_s takes the following form:

$$F_S = \frac{V'_{DS}/V_{DSAT}}{\left(1+(V'_{DS}/V_{DSAT})^\beta\right)^{1/\beta}}$$

(3-17)

V'_{DS} is the intrinsic drain-to-source voltage. V_{DSAT} is the saturation voltage, β is a fitting parameter relevant for transition from low-field non-saturation region to high-field saturation region. It is found in this work that $\beta = 1.8$ gives good fitting for both electron and hole conduction in graphene transistors. Typical values of β for Si MOSFETs were found between 1.8 for electrons and 1.6 for holes in [189]. It is clear from eq. (1) that the saturation factor, eq. (3-17), is defined to satisfy: $I_{DS,I} = 0$ for $V'_{DS} = 0$, and $\lim_{V'_{DS}\to\infty} I_{DS,I} = Q_{VES,e}v_{VES,e}W = I_{DSAT}$, which gives the saturation current.

The derivation of saturation voltage V_{DSAT} for Si MOSFETs in Ref. [189], which is by relating the definition of low-field channel conductivity in the vicinity of $V_{DS} = 0$ to its physical dependency on sheet charge and mobility, is also valid for graphene transistors. Here, we quote the result:

$$V_{DSAT} = \frac{v_{VES,e}L_G}{\mu}$$

(3-18)

V_{DSAT}, as expressed in this form, is only dependent on carrier transport properties $v_{VES,e}$, μ, and device geometry L_G, and is independent of the fitting parameter β. L_G is the gate length of the device. μ is the channel carrier effective mobility, which is in general a function of the top-gate, the back-gate, and the drain-to-source voltages [82][201]. μ is assumed to be a constant here for simplicity.

Finally, graphene transistors always have a minimum current that cannot be fully pinched off by the gate. This is accounted for by adding a minimum current I_{min} to the drain current $I_{DS,I}$ where

$$I_{min} = \frac{V'_{DS}}{R_p} = \frac{V'_{DS}}{L_G/\mu \cdot W \cdot Q_{min}}$$

(3-19)

μ is the channel carrier effective mobility. Q_{min} is the minimum charge in the channel, which cannot be modulated by the gate, giving rise to I_{min}. Q_{min} is mainly due to disorder and thermal excitation as discussed in Ref. [76][165][202]. $\frac{1}{R_p} = \frac{\mu \cdot W \cdot Q_{min}}{L_G}$ is the equivalent additional conductance contributed by the minimum charge Q_{min} to the channel. In this work, Q_{min} is considered as a fitting parameter.

Device Operation in Region III

When the GFETs are operating in Region III, only hole charge is present in the channel and the device operation is similar to that of p-channel Si MOSFETs. The formulation of the model for Region I is also valid for the hole channel in Region III. However, it is important to note that the drain side of the device acts as an "injection source" for holes when the device is operating in Region III. The holes are injected from the drain side of the device and collected by the source of the device, opposite to that for electrons. Hence, the virtual source for hole injection is effectively at the drain side of the device, which is defined as the "virtual hole source (VHS)" in Figure 3-16. Both the charge and injection velocity for the hole channel should be evaluated at this point. Applying eq. (3-13) to hole charge at VHS, we have

$$I_{DS,III}/W = Q_{VHS,h} v_{VHS,e} F_s$$

(3-20)

$v_{VHS,h}$ is the local hole carrier velocity at the virtual hole source. $v_{VHS,h}$ is assumed to be equal to $v_{VES,e}$ in this paper. $Q_{VHS,h}$ is the hole charge at the virtual hole source:

$$Q_{VHS,h} = C_{TG} n \phi_t \ln \left(1 + \exp \frac{-V'_{TGD} + V_{t,h}}{n \phi_t} \right)$$

(3-21)

$V_{t,h}$ is the effective threshold voltage for gate induced hole charge in the channel, which is given as:

$$V_{t,h} = V_{TG,min} - \Delta V$$

(3-22)

The expressions for F_s derived for Region I is also valid for hole conduction. Similar to that in Region I, the minimum current I_{min}, given by eq. (3-19), needs to be added to $I_{DS,III}$ for the device operating in Region III.

Device Operation in Region II

In this region of device operation, both electrons and holes are present in the channel. Assuming V_{DS}>0, the channel charge distribution can be schematically described by Figure 3-18. Point *X* in Figure 3-18 marks the recombination point. As shown in Figure 3-18, the part of the channel to the left of the recombination point has electron conduction and the part of the channel to the right of the recombination point has hole conduction. L_n is the length of the electron section of the channel, which is the distance from VES to the recombination point. L_p is the length of the hole section of the channel, which is the distance from the recombination point to VHS. V_n and V_p are the potential drops across the electron and hole sections of the channel respectively. Hence, we have

$$L_n + L_p = L_G \text{ and } V_n + V_p = V'_{DS}$$

(3-23)

I_n and I_p are the currents in the electron and hole sections of the channel respectively. By current continuity, we have

$$I_n = I_p$$

(3-24)

$$\text{where} \qquad \frac{I_n}{W} = Q_{VES,e} v_{VES,e} F_{s,e}$$

(3-25)

$$\frac{I_p}{W} = Q_{VHS,h} v_{xVHS,h} F_{s,h}$$

(3-26)

$F_{s,e}$ and $F_{s,h}$ are the saturation factor for the electron section and hole section of the channel respectively, and are given as

$$F_{s,e} = \frac{V_n/V_{DSAT,e}}{\left(1+(V_n/V_{DSAT})^\beta\right)^{1/\beta}} \quad \text{where } V_{DSAT,e} = \frac{v_{VES,e}L_n}{\mu}$$

(3-27)

$$F_{s,h} = \frac{V_p/V_{DSAT,h}}{\left(1+(V_p/V_{DSAT})^\beta\right)^{1/\beta}} \quad \text{where } V_{DSAT,h} = \frac{v_{VHS,h}L_p}{\mu}$$

(3-28)

In addition, since electrons and holes recombine at the recombination point *X*, this point must be a point of minimum charge, i.e. a charge neutrality point where the channel carrier density is minimum. In other words, the recombination point *X* should be defined as the point along the channel where the channel potential is equal to the minimum conduction point of the GFET, i.e. the point where the quasi Fermi levels are equal to the charge neutrality level in Figure 3-18. Hence, we have

$$V'_{TGX} \overset{\text{def}}{=} V_{TG,min} \implies V'_{TGX} = V_{TG,min} = \frac{V_{t,h} + V_{t,e}}{2} \implies -(V'_{TGD} + V_p) + V_{t,h} = (V'_{TGS} - V_n) - V_{t,e}$$

(3-29)

where V'_{TGX} is the voltage between the top-gate and the recombination point. Hence, we can solve the set of six equations, eq. (3-23) - (3-26) and eq. (3-29), for the six unknowns L_n, L_p, V_n, V_p, I_n, and I_p. It is clear from the expressions of the saturation factor $F_{s,e}$ and $F_{s,h}$ that this set of equations can only be solved numerically. In addition, since internal voltages are required to evaluate the charge and current, iterations are needed to obtain self-consistent solutions of voltage and current, increasing the computational load in evaluating the model. However, the computation can be significantly reduced with little loss of accuracy by simply assuming a linear potential drop across the channel when the device is operating in the ambipolar region, which gives

$$\frac{V_n}{L_n} = \frac{V_p}{L_p}$$

(3-30)

By solving for the four unknowns L_n, L_p, V_n and V_p from the four equations, eq. (3-23) and eq. (3-29) - (3-30), we have

$$L_n = \frac{L_G}{1 + \dfrac{V'_{TGS} - (V_{t,e} + V_{t,h})/2}{(V_{t,e} + V_{t,h})/2 - V'_{TGD}}}$$

(3-31)

The current is evaluated by eq. (3-25) or eq. (3-26) depending on the relative saturation levels of the electron and hole sections, i.e. if $F_{s,h} > F_{s,e}$, we have $I_{DS,II} = I_{DS,II,e} = Q_{VES,e} v_{VES,e} F_{s,e}$ and if $F_{s,h} < F_{s,e}$, we have $I_{DS,II} = I_{DS,II,h} = Q_{VHS,h} v_{VHS,h} F_{s,h}$. Although the current continuity approach has stronger physical basis, the linear approximation requires much less computation with very little loss of accuracy in calculating the current. Hence, we use the linear approximation method to evaluate L_n, L_p, V_n and V_p for all results presented in later in this section. Finally, as in Region I and Region III, the minimum current I_{min} needs to be added to $I_{DS,II}$ for devices operating in Region II.

Determination of the Operation Region

A very important step in the model evaluation is to determine which operation region the device is in for a given gate and drain bias. This can be determined by the location of the recombination point X, i.e. by the value of L_n and L_p. Assuming $V_{DS} > 0$, we have:

(a) If $L_p < 0$, i.e. $L_n > L_G$, the hole section of the channel does not exist and the entire channel has electron as the carrier. Hence, the GFET is operating in Region I. The current is evaluated using the model formulation derived for Region I.

(b) If $L_p > L_G$, i.e. $L_n < 0$, the electron section of the channel does not exist and the entire channel has hole as the carrier. Hence, the GFET is operating in Region III. The current is evaluated using the model formulation derived for Region III.

(c) If $0 < L_p$, $L_n < L_G$, the channel has an electron section to the left of the recombination point and a hole section to the right of the recombination point (Figure 3-17). The device is in Region II and we use the model formulation derived for Region II to evaluate the current.

Note that for $L_p = 0$ and $L_n = L_G$, we have $I_{DS,I} = I_{DS,II}$; and for $L_p = L_G$ and $L_n = 0$, we have $I_{DS,II} = I_{DS,III}$, which ensures the continuity of the model between the three operation regions.

Figure 3-19 summarizes the main steps in evaluating the model and the iteration loop needed to achieve self-consistent values of current and voltage since internal voltages are required to evaluate the charge and current.

Modulation of Access Resistance by Back-gate

Several papers have reported that the parasitic series resistance of GFETs, which includes both the contact resistance and the resistance of the access region, is a function of the applied vertical electric field [165][174][203]. This dependence is due to the modulation of the charge density in the contact and access region. Since the access region and the region underneath the contacts, i.e. excluding the region under the top-gate, are only modulated by the back-gate, this series resistance is only a function of the back-gate voltage and is independent of the top-gate voltage. Assuming the resistance of these regions is inversely proportional to the carrier density present, we have the following equation describing this dependency:

$$R_S = R_0 + \frac{r_1}{Q_{BGS,access}}$$

(3-32)

$$R_D = R_0 + \frac{r_1}{Q_{BGD,access}}$$

(3-33)

where R_0 and r_1 are fitting parameters. The source access region charge $Q_{BGS,access}$ and the drain access region charge $Q_{BGD,access}$ can be approximated as the sum of the charge induced by the back gate in the respective regions and the minimum charge Q_{min}:

$$Q_{BGS,access} = C_{BG}^* n_{BG} \phi_t \ln\left(1 + \exp\frac{|V_{BGS}' - V_{BG,mino}|}{n_{BG}\phi_t}\right) + Q_{min}$$

(3-34)

$$Q_{BGD,access} = C_{BG}^* n_{BG} \phi_t \ln\left(1 + \exp\frac{|V_{BGD}' - V_{BG,mino}|}{n_{BG}\phi_t}\right) + Q_{min}$$

(3-35)

n_{BG} is the back-gate equivalence of n, which is analogous to the sub-threshold coefficient in Si MOSFETs and is considered as a fitting parameter. C_{BG}^* is the back-gate capacitance in the source and drain access region without the screening effect from the top-gate. C_{BG}^* is in general different from the back-gate capacitance C_{BG} in the channel region, which has the screening effect from the top-gate since the graphene channel is not a perfect conductor. Since it would involve fairly complicated electrostatics to fully capture the screening effect of the top-gate on C_{BG}, in this paper we assume $C_{BG} = C_{BG}^*$ for simplicity. V_{BGD}', given by $V_{BGD}' = V_{BGD} + I_{DS}R_D$, is the intrinsic back-gate-to-drain voltage, where V_{BGD} is the external back-gate-to-drain voltage.
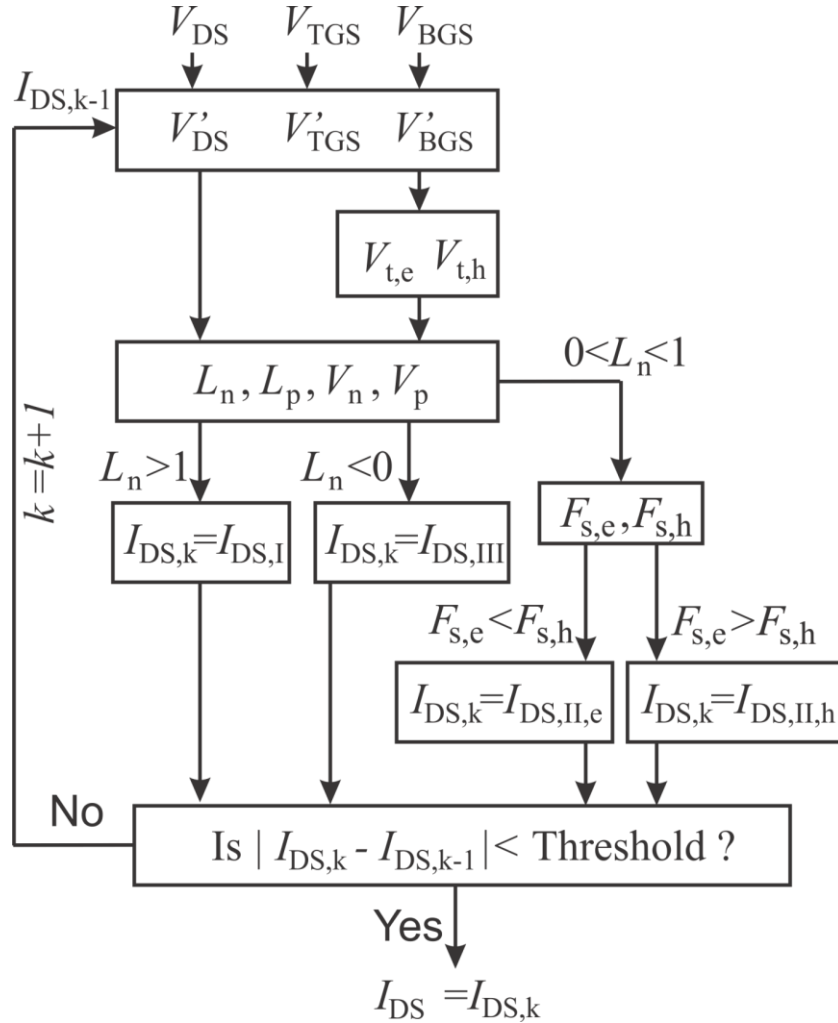
Figure 3-19 Flow diagram of the iteration steps for evaluating the virtual source carrier injection model. Main steps in evaluating the model and the iteration loop needed to achieve self-consistent solutions of current and voltage. k is

the iteration step index. $I_{DS,k}$, hence, denotes the drain current evaluated in k^{th} step of the iteration process. The choice for the iteration threshold is arbitrary. Generally, a smaller threshold value gives more accurate results, but requires more computation. An iteration threshold value of 10^{-6} mA/mm is used for the results presented in Section IV.

Model Results and Discussions

In this section, the results from the above model are compared with experimental data taken from a typical GFET fabricated in our lab. For the fabrication of the GFET, single-layer graphene films were grown by CVD on copper substrates [57]. Copper foils annealed at 1000 ℃ in H_2 (350 mTorr for 30 minutes) are exposed to CH_4 under low-pressure condition (1.6 Torr) to initiate graphene growth. After the growth, PMMA is coated on the graphene film and the copper substrate is etched away in copper etchant and diluted HCl. Films are then transferred onto polished Si wafers with a 300 nm thermally-grown SiO_2 on top. Mono-layer graphene with uniformity greater than 95% is obtained (Figure 2-3). The ohmic contacts of the GFETs are formed by depositing a 2.5 nm Ti/ 45 nm Pd/ 15 nm Au metal stack by e-beam evaporation. Device isolation is achieved by O_2 plasma etching.

The gate dielectric of 15 nm Al_2O_3 is formed in two steps. A 3 nm Al layer is first deposited on the graphene surface by electron beam evaporation, which is then naturally oxidized in air. This first Al_2O_3 film serves as the initial nucleation layer to promote adhesion of the subsequent 12 nm of Al_2O_3 deposited by atomic layer deposition (ALD), using H_2O as the precursor and trimethyl aluminum (TMA) as the Al source [39]. The top gate is formed with a 30 nm Ni/ 200 nm Au/ 50 nm Ni metal stack. DC characterization of the devices was performed using an Agilent 4155C Parameter Analyzer. The devices were measured at room temperature under vacuum (1.1×10^{-4} Torr) to reduce hysteresis. The device dimensions are shown in Table 3-2 (a), which also includes the parameters used in the compact device model.

I_{DS} vs. V_{TGS} and V_{BGS}

Figure 3-20(a) shows the top-view of the three-dimensional plot generated from the model for I_{DS} as a function of both V_{TGS} and V_{BGS} for V_{DS}=1.1 V. There are two distinct ridges of minimum conduction for the GFET due to modulation of the channel and series resistance respectively. The deeper vertical ridge is due to the modulation of the channel region by both the top and back gate. The shallower horizontal ridge is due to the back-gate modulation of the

source and drain series resistance, which includes both the contact resistance and access region resistance.

Figure 3-20(b), (c) and (d) compare the model with measured data. In Figure 3-20(b), V_{BGS} is kept constant at 0 V and V_{TGS} is swept from -1 V to 3 V. A family of curves is shown for V_{DS} increasing from 0.35 V to 1.1 V in steps of 0.25 V. There is a clear dependence of the top-gate minimum conduction point on V_{DS}, which is due to both the increased potential drop across the source series resistance and the increased potential variation along the channel region as V_{DS} increases. In Figure 3-20(d), V_{TGS} is kept constant at 1.41 V and V_{BGS} is swept from -30 V to 40 V. Again, a family of curves is shown for V_{DS} increasing from 0.35 V to 1.1 V in steps of 0.25 V. In both the top-gate and back-gate sweeps, the ambipolar V-shape characteristics for GFETs are observed. The model gives very good agreement with the experimental data in all bias combinations. In Figure 3-20(c), V_{TGS} is kept constant at 0 V and V_{BGS} is swept from -50 V to 100 V. This is a sweep similar to the one in Figure 3-20(d) only at a slightly different top-gate bias. The I_{DS}-V_{BGS} characteristic, however, shows a kink, which can be decomposed into two separate minimum conduction points that correspond to the back-gate modulation of the channel and of the series resistance respectively.

In the devices analyzed here, the gate length is approximately equal to the distance between the source and drain electrodes (i.e. $L_{DS} \approx L_G$). The series resistances are therefore dominated by the contact resistances. The fitted contact resistance varies between 2.5 kΩ.µm and 4.2 kΩ.µm and it agrees well with the contact resistance measured by transmission line measurements [174], which gives values between 3 kΩ.µm and 5 kΩ.µm, depending on back-gate bias. The fitted mobility is 1500 cm^2/V.s. This is very close to the mobility obtained from Hall measurements after the top gate dielectric is deposited, which varies between 1400 cm^2/V.s and 1700 cm^2/V.s, depending on gate bias. The model extracts a virtual source injection velocity of $v_{VES,e} = v_{VHS,h} = 1.2 \times 10^7$ cm/s in this long channel device (L_G= 5µm).

I_{DS} vs. V_{TGS} and V_{DS}

Figure 3-21(a) shows the three-dimensional plot generated from the model for I_{DS} as a function of both V_{TGS} and V_{DS}, for V_{BGS}=0 V. In Figure 3-21(b), curves A-D are cuts of Figure 3-21(a) at the corresponding dotted lines. The modeled results are shown as solid lines and the experiment

data is shown as dots. In all the plots, V_{BGS} is set to 0 V. Again, the model gives excellent agreement with the experimental data. In addition, the model can fully capture the kink in the I_{DS} vs. V_{DS} characteristics due to GFETs operating in the ambipolar region with an n-type channel section on the source side and a p-type channel section near the drain side. For example, in curve D of Figure 3-21, with V_{BGS}=0 V and V_{TGS}=2 V, the channel is n-type everywhere in the channel (Region I) at low V_{DS}, i.e. L_n/L_G ratio is greater than 1. As the V_{DS} increases to about V_{DS}=0.8 V, the device operation starts to transit from Region I to the ambipolar region (Region II) and the recombination point appears near the drain, i.e. $0 < \frac{L_n}{L_G} < 1$. From approximately V_{DS}=0.8V to V_{DS}=1.2 V, the device is in the ambipolar region (Region II); and with increasing $V_{DS,}$ the recombination point migrates from the drain side to the source side as the electron section of the channel shrinks and the hole section extends. In this operation region, the potential drop across the electron section, V_n, stays relatively constant while the potential drop across the hole section, V_p, increases proportionally as V'_{DS} increases. Hence, in the early stage of Region II when V_{DS} is still relatively low, the recombination point is closer to the drain side as the electron section still dominates the channel, the channel current stays relatively constant due to a relatively constant V_n, leading to the kink in the I_{DS} vs. V_{DS} characteristics. In addition, the fact that the effective length of the electron channel L_n is less than the gate length L_G means the device has a lower V_{DSAT}, i.e. device saturation occurring at a much lower drain voltage, in this operation region than in Region I and III. This also leads to the current staying constant because the additional increment in potential across the channel only gives marginal increase in the current, which is already close to saturation. In the later stage of Region II when V_{DS} is much higher, the recombination point is closer to the source side as the hole section starts to dominate the channel. V_p increases proportionally with V'_{DS}, causing the current to start rising again with increasing V_{DS}. For V_{DS}>1.2 V, the recombination point reaches the source side and the channel becomes p-type everywhere (Region III), i.e. $\frac{L_p}{L_G} > 1$ and $\frac{L_n}{L_G} < 0$. The current in the channel continues to rise in this operation region until it can saturate for a second time at a much higher drain bias.

The device, however, will not pass through the ambipolar region as V_{DS} increases from 0 V to more positive biases if the GFET starts with a p-type channel everywhere. In terms of the energy level diagram in Figure 3-18, it means that, at V_{DS}=0 V, the Fermi level is above the charge

neutrality level (p-type) everywhere in the channel. As V_{DS} increases, which can cause the charge neutrality level on the drain side to rise but have minimum effect on the source side charge neutrality level, the quasi Fermi level (for holes) will always stay below the charge neutrality level everywhere in the channel, resulting in a p-type channel and no ambipolar operation in the GFET for all positive drain bias, i.e. for all $V_{DS}>0$ V. For example, in curves A and B in Figure 3-21(a), the top-gate biases are at $V_{TGS}=$ -1 V and 0 V respectively, making the channel p-type everywhere at low drain bias. Figure 3-21(a) shows that the device is never in the ambipolar region as V_{DS} increases, which is evidenced by the absence of the kink in the I_{DS}-V_{DS} characteristics.

Modeling Short-channel Devices

Figure 3-22 plots the modeled and experimental data for a short-channel, reported as $L_G=240$ nm, top-gated GFET in Ref. [119]. To the best of our knowledge, this is the GFET whose gate-length is among the shortest in literature. The physical dimensions of the device reported in Ref. [119] and the parameters used in the model, are listed in Table I(b). Since the GFET in Ref. [119] only has top-gate, it allows a few simplifications to the model. First, the back-gate effect is removed by setting $C_{BG}=0$ in eq. (3-16). In addition, eq. (3-32) and eq. (3-33) can be reduced to a single constant by setting $r_1 = 0$, since there is no back-gate to modulate the series resistance. Figure 3-22(b) compares the model results (solid line) for I_D-V_{TGS} (transfer characteristics) with data from Fig. 1B of Ref. [119] (dashed line); although there is a discrepancy between the model and those measured data, nevertheless the model results agree very well with I_{DS}-V_{GS} data point mapped from Fig. 1C of Ref. [119] under the same bias conditions (blue dots). Hence, we attribute the discrepancy to the variation in experiment data in Fig. 1B and 1C of Ref. [119], possibly due to measurements being taken under slightly different conditions. The model extracts a virtual source velocity of $v_{VES,e} = v_{VHS,h} = 2.5 \times 10^7$ cm/s in this device. The injection velocity for this device is significantly higher than the injection velocity in the device in Figure 3-20 and Figure 3-21, probably due to its much shorter gate length (240 nm compared to 5 μm). The fitted source resistance is WR_s=578 Ω.μm and the fitted mobility μ=1600 cm^2/V.s agrees very well with the measured values given in Ref. [119] and its supplementary information.

Virtual Source Velocity

The model presented in this section allows the extraction of a key parameter in FET operations for graphene transistors, which is the virtual source carrier injection velocity. Figure 3-23 compares the virtual source carrier velocity extracted for GFETs using the model reported in this paper with that in modern Si MOSFETs and the state-of-the-art III-V HFETs. For similar gate length, Figure 3-23 shows that the source carrier velocity in graphene is much higher than the source carrier velocity in modern Si MOSFETs [190][191], and also higher than the source carrier velocity in the state-of-the-art III-V HFETs [204], showing the great potential of graphene devices for high frequency applications. In GFETs, the carrier velocity also increases as gate length is reduced, following the same trend as in Si MOSFETs and III-V HFETs, explained by increased carrier ballisticity with reduced channel length.
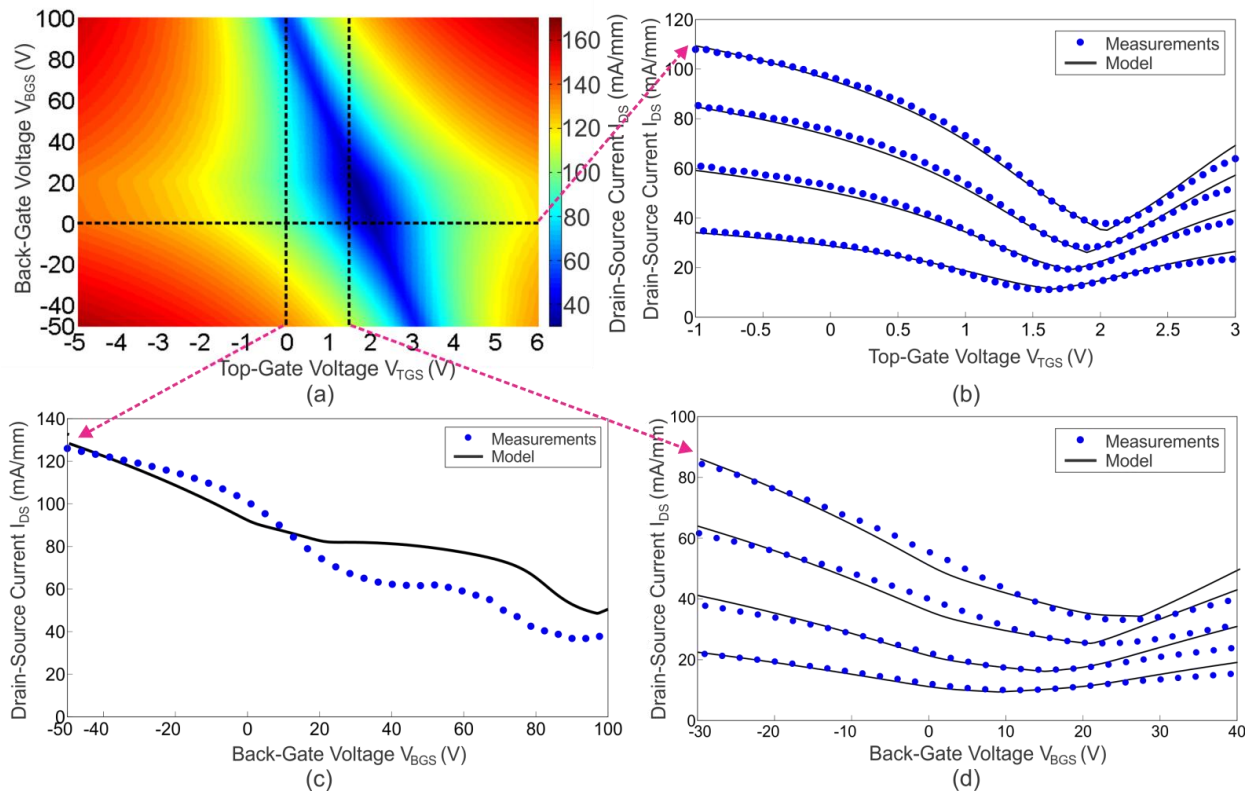
Figure 3-20 Model evaluation and comparison with experimental data for the transfer characteristics of a dual gate graphene transistor (a) Top-view of the three-dimensional plot of I_{DS} vs. V_{TGS} and V_{BGS} at V_{DS}=1.1 V: The two distinct ridges of minimum conduction in the GFET are clearly visible. (b), (c) and (d) are cross-section in (a) at the corresponding dotted lines. The model results are shown as solid lines and the experiment data is shown as dots. In (b), V_{BGS} is kept constant at 0 V and V_{TGS} is swept from -1 V to 3 V. A family of curves is shown for V_{DS} increasing from 0.35 V to 1.1 V in step of 0.25 V. In (c), V_{TGS} is kept constant at 0 V and V_{BGS} is swept from -50 V to 100 V. The I_{DS}-V_{BGS} characteristics shows a kink, which is due to two separate minimum conduction points from the back-

gate modulation of the channel and the series resistance respectively. (d) V_{TGS} is kept constant at 1.41 V and V_{BGS} is swept from -30 V to 40 V. A family of curves is shown for V_{DS} increasing from 0.35 V to 1.1 V in step of 0.25 V.

(a)   (b)
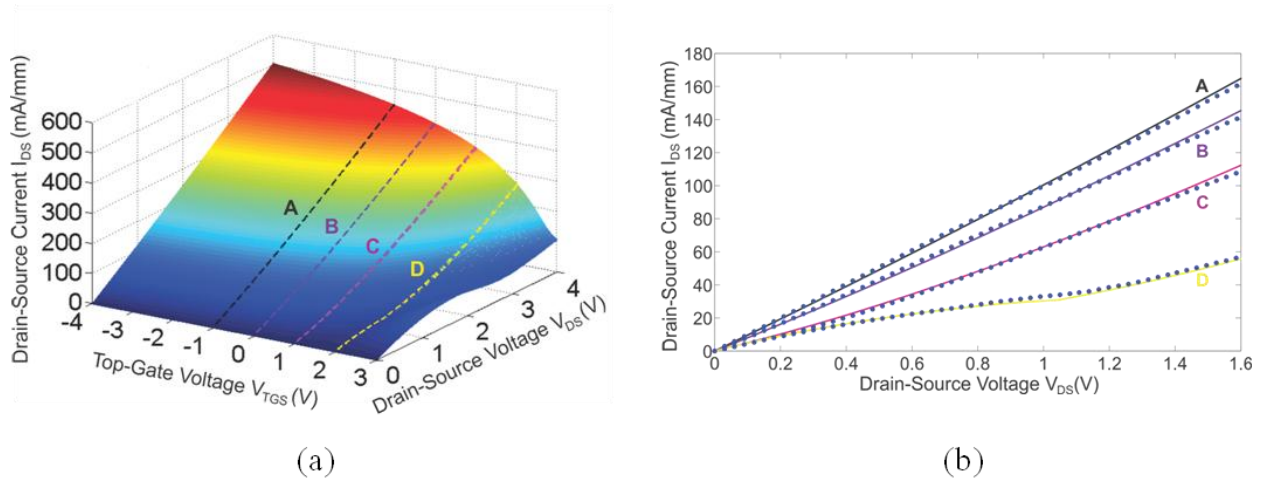
Figure 3-21 Model evaluation and comparison with experimental data for the transfer characteristics of a dual gate graphene transistor (a) Three-dimensional plot of I_{DS} vs. V_{TGS} and V_{DS} at V_{BGS}=0 V: For curve D, the device starts with an n-type channel at low V_{DS} due to a high top-gate bias voltage. As V_{DS} increases, the device channel transits from n-type to p-type. The I_{DS} vs. V_{DS} cross-section shows a characteristic kink due to the transitional ambipolar region (Region II). The current continues to increase when the channel becomes entirely p-type. For curves A and B, the device starts with a p-type channel at low V_{DS} due to a low (or negative) top-gate bias and the device never operates in the ambipolar region for all positive V_{DS}. (b) Curves A-D are cross-section in (a) at the corresponding dotted lines. The model results are shown as solid lines and the experiment data is shown as dots. V_{BGS}=0 V in all plots.

DEVICE PHYSICAL DIMENSION	GFET
T_T (Al$_2$O$_3$)[nm]	15
T_B (SiO$_2$) [nm]	300
L_G [μm]	5
L_{DS} [μm]	5
W [μm]	25
C_{TG} [μF/cm^2]	0.39
C_{BG} [μF/cm^2]	0.0085
β	1.8
$V_{TG, min0}$ [V]	1.24
$V_{BG, min0}$ [V]	11
ΔV [V]	0
n	11.2
n_{BG}	49
$v_{VES,e}$, $v_{VHS,h}$ [10^7 cm/s]	1.2
μ [cm^2/V.s]	1500
WR_0 [kΩ.μm]	1.0
r_1 [10^{-4} V.s/cm^2]	3.6
Q_{min} [10^{-7} C/cm^2]	1.1

(a)

DEVICE PHYSICAL DIMENSION	GFET
T_T [nm]	10 nm poly-hydroxystyrene and 10 nm HfO$_2$
T_B (SiC) [nm]	Insulating Substrate
L_G [μm]	0.24
L_{DS} [μm]	Not Specified in Ref. [115]
W [μm]	30
C_{TG} [μF/cm^2]	0.195 (Given in Ref. [115])
C_{BG} [μF/cm^2]	Zero (No Back Gate)
β	1.8
$V_{TG, min0}$ [V]	-3.1
$V_{BG, min0}$ [V]	N.A.
ΔV [V]	1.8
n	14.6
n_{BG}	N.A.
$v_{VES,e}$, $v_{VHS,h}$ [10^7 cm/s]	2.5
μ [cm^2/V.s]	1600
WR_0 [kΩ.μm]	0.578
r_1 [10^{-4} V.s/cm^2]	N.A.
Q_{min} [10^{-7} C/cm^2]	0.92

(b)

Table 3-2 Parameters used in fitting the virtual source carrier injection model (a) Device physical dimensions for the GFET modeled in Fig. 6 and 7. The parameters used in the model are given. (b) Device physical dimensions from Ref. [119] for the GFET modeled in Figure 3-22. The parameters used in the model are given.
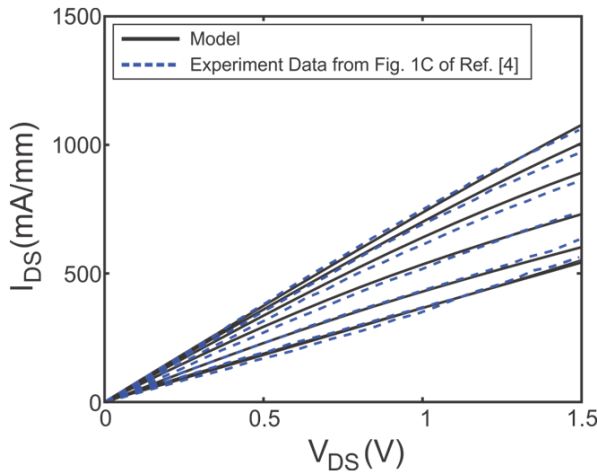
(a)
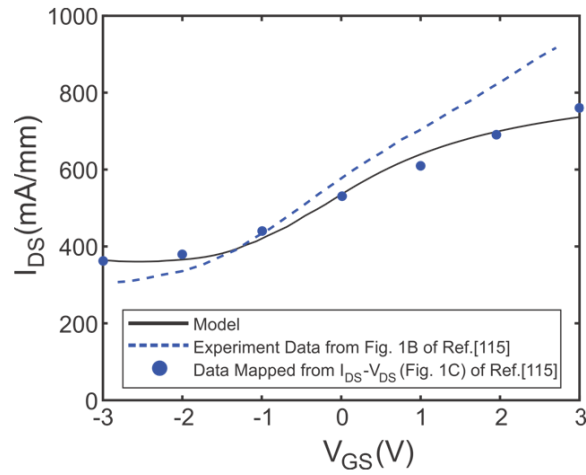
(b)

Figure 3-22 Fitting of virtual source carrier injection model to the device data in Ref. [119]. (a) Model (solid line) vs. Experiment Data (dotted line) for I_{DS}-V_{DS} characteristics of a short channel GFET with L_G=240 nm. The experiment data is from Fig. 1C of Ref. [119]. The gate voltage increases from -3 V to 3 V in step of 1 V. (b) Model (solid line) vs. Experiment Data (dotted line) for I_{DS}-V_{GS} characteristics for the same GFET. The experiment data (dashed line) is from Fig. 1B of Ref. [119]. The blue dots show the experiment data for I_{DS}-V_{GS} mapped directly from the I_{DS}-V_{DS} characteristics in Fig. 1C of Ref. [119]. The model has discrepancy with the experiment data (dashed line), but shows good agreement with the mapped data (blue dots). The discrepancy is hence attributed to variations in measurement condition when data in Ref. [119] is obtained.
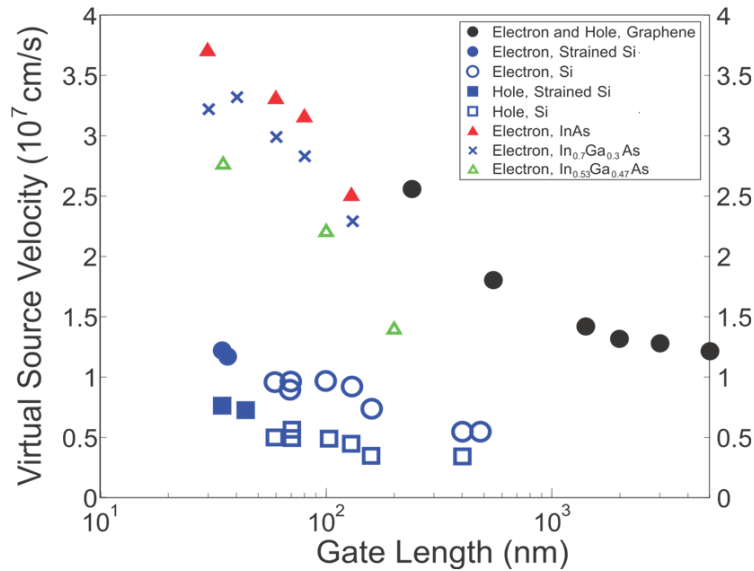
Figure 3-23 Virtual source injection velocity vs. gate length for graphene transistors, modern Si MOSFETs and the state-of-the-art III-V HFETs. The virtual source velocity in graphene devices is much higher than in Si MOSFETs and also higher than in the state-of-the-art III-V HFETs for similar gate lengths in the range of 200-250 nm, demonstrating the great potential of graphene for high frequency applications. Source carrier injection velocity for all the GFETs are extracted using the model reported in this paper. The DC I-V characteristics for GFETs with gate lengths of 550 nm and 240 nm are taken from Ref. [119]. The Si MOSFETs source carrier injection velocity data is from Ref. [191]. The InGaAs and InAs source carrier injection velocity data is from Ref. [204].

3.6. Drain-Induced-Minimum-Shift (DIMS) Effect on Current Saturation in GFETs

The first graphene field effect transistor (GFET) was fabricated in 2004, the lack of current saturation in GFETs has been an important issue awaiting solutions. A reasonable level of current saturation is needed to achieve enough power gain for RF applications, as well as to demonstrate true transistor behavior in graphene devices. In addition, current saturation is an indispensible transistor device feature required for building current sources, which are critical components of most analog circuits. However, the zero bandgap of graphene prevents GFETs from behaving like Si devices where saturation is obtained by drain pinch-off in long channel devices and by velocity saturation in short channel devices [205]. Band-to-band tunneling (BTBT) is also more significant in the zero-bandgap graphene channel, making graphene behave like a semi-metal, preventing current saturation in short channel GFETs even though velocity saturation may occur [184][206]. On the other hand, current pseudo-saturation may be realized

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due to the drain-induced minimum conductance point shift (DIMS) where the increase in the drain-to-source voltage magnitude, $|V_{DS}|$, causes the minimum conduction point of the device to shift to more positive gate voltage, V_{GS}, for positive V_{DS}, and to shift to more negative V_{GS} for negative V_{DS} bias [207][208][166]. For example, in n-FET operation at a constant V_{GS}, by driving the effective device bias point closer to the minimum conduction point as V_{DS} increases, this effect can off-set the current increase due to increasing V_{DS}, hence achieving saturation-like behavior in the device.

Thus, when analyzing the current saturation behavior in GFETs, particularly in short channel devices, it is important to distinguish between current saturation that is due to DIMS and current saturation that is due to true velocity saturation. In this work, we quantitatively analyze the DIMS effect and its influence on current saturation in graphene FETs. We will also derive quantitative relations that may be used during device design to predict and control the DIMS-induced current saturation.

DIMS-Induced Current Saturation in GFET

It has been observed by several independent research groups that as the drain voltage increases in a GFET, it can induce a shift in the minimum conduction point [207][208][166]. This is because, for long channel GFETs, the lack of bandgap results in the absence of depletion region on the drain side of the device. Hence, the device never pinches off and the drain has strong influence on the potential profile in the channel. For short channel GFETs, the influence of the drain voltage on the channel becomes even stronger. This effect leads to almost linear potential variations across the channel [209]. The minimum conduction (V_{GS}) point of the GFET is not the voltage at which the Fermi level in a local region of the graphene channel reaches the charge neutrality level, rather it is the point where the device reaches its minimum conduction when the channel has electrons injected from the source side (cathode, or more negative terminal) and hole injected from the drain side (anode, or more positive terminal), and the two types of carriers recombine at the middle of the channel (Figure 3-24). Hence, if we only consider the intrinsic device, i.e. assuming the source and drain access resistances $R_S=0$ and $R_D=0$, the shift in the minimum conduction point $\Delta V_{\text{GS,min}}$ can be approximated to first order as $k\Delta V_{DS}$ (Figure 3-24),

where ΔV_{DS} is the change in the drain-source bias voltage and k is a constant proportionality factor. For devices with symmetrical electron/hole branch conductivity, k would be close to ½.

For a given small increase in the drain-source voltage ΔV_{DS}, the current I_{DS} increases by $\frac{\Delta V_{DS}}{r_{ch}}$, where r_{ch} is the resistance of the graphene channel. At the same time, the increase in the drain-source voltage shifts the minimum conduction point of the device by $k\Delta V_{DS}$. This causes the curves on the electron branch to shift right and bring the current level on the electron branch closer together for a given increase in drain voltage. The ratio between the shift in I_{DS} and the shift in $V_{GS,min}$ is exactly equal to the transconductance of the device. Hence, we have the following equation describing the change in the drain current ΔI_{DS} when the drain-source voltage changes by ΔV_{DS}:

$$\Delta I_{DS} = \frac{\Delta V_{DS}}{r_{ch}} - k\Delta V_{DS}g_m$$

(3-36)

And the output conductance can be written as:

$$g'_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{1}{r_{ch}} - kg_m = g_{ch} - kg_m$$

(3-37)

The small-signal output conductance of a graphene device is equal to the channel conductance minus half (typically, k~1/2) of the transconductance of the device. DIMS induced current pseudo-saturation is maximized when $g_{ch} \approx kg_m$.

From the analysis above, it is clear that DIMS-induced current saturation is easier to achieve in devices with low g_{ch} and high g_m (Figure 3-24). This may explain some observations in the literature. First, the current saturation in GFETs is more likely to occur in long channel devices than in short channel devices [210][211]. This is because the long channel devices have lower g_{ch}. Second, the current saturation is also more likely to occur for devices with high carrier mobility (such as graphene on hBN [210]) and devices with low effective oxide thickness (EOT)

in the gate dielectric [166]. Both high mobility and thin EOT lead to high transconductance g_m that can help to achieve DIMS-induced current saturation in GFETs.

A signature of this DIMS-induced current saturation effect in the device output characteristics is that the current saturation can only occur for one particular type of carriers, i.e. electron current saturation for positive V_{DS} (and hole current saturation when V_{DS} bias is negative) (Figure 3-25). This is clearly observed in the device output characteristics reported in the literature [184][166][210], where current saturation is only observed in one carrier type (holes with V_{DS} being negative). The schematic diagram in Figure 3-25 also illustrates this. It can be seen that with gate bias at lines B and C in the transfer curves on the electron conduction side with increasing V_{DS} will crowd together due to DIMS, leading to possible current saturation. On the other hand, if the gate voltage is biased at dotted line A in Figure 3-25, the device will not show current saturation. In fact, the I_{DS}-V_{DS} curves may even become super-linear [210] because the current levels along the dotted line A can have larger separation due to the positive shift in $V_{GS,min}$.

Separating DIMS Effects

Given the significant DIMS effect in GFETs, to accurately extract saturation velocity, it is necessary to carefully account for this effect in measurements and models. Here, we propose a technique that may be used for measuring DC output characteristics of GFETs in order to separate DIMS effects from true current saturation. To eliminate DIMS effects, we can apply symmetric V_{DS} bias at the source and the drain. For example, to apply a V_{DS}=1 V, we can apply -0.5 V at the source (V_S) and +0.5 V at the drain (V_D), instead of V_S=0 V and V_D=1.0 V. We call this the *symmetric bias technique*. Figure 3-26(e) and Figure 3-26(f) show the results of applying this technique to GFETs fabricated in our laboratory. The graphene material is grown using CVD method on copper foils and then transferred to SiO_2 substrate. The mobilities in graphene transferred onto 300 nm silicon dioxide are typically 2,220±170 cm^2/V.s (for a sheet charge density n_S= 5.5±0.6×10^{12} cm^{-2}). The ohmic contacts of the GFETs are first formed by depositing a 2.5 nm Ti,45 nm Pd,15 nm Au metal stack by e-beam evaporation using a pre-ohmic aluminum capping process [174]. The gate dielectric consists of 16 nm Al_2O_3 formed by naturally oxidizing e-beam evaporated Al and the top gate electrode is made of 60 nm-thick Al. Figs. 3(a) and 3(b)

show that for V_S=0 V and V_D>0 V, the current saturates on the electron conduction side, but not on the hole conduction side. For V_S=0 V and V_D<0 V (Figs. 3(c) and 3(d)), the current saturates on the hole conduction side, but not on the electron conduction side. When we applied symmetric bias to the device (Figure 3-26(e) and Figure 3-26(f)), the DIMS-induced current saturation is eliminated. Since the device does not show current saturation under the symmetric bias condition for both electron and hole conduction branches, we can conclude that the device has not reached velocity saturation in the voltage range measured and that the saturation behavior observed in Figure 3-26(a) and Figure 3-26(b) is only due to the DIMS effect.

Here, we have analyzed the impact of drain-induced-minimum-shift on the current saturation behavior in GFETs. When reporting current saturation behavior in GFETs, it is important to distinguish true velocity saturation from current saturation that is due to DIMS effects. A technique for experimentally separating DIMS-induced current saturation from the true carrier velocity induced current saturation behavior in GFETs has been proposed.
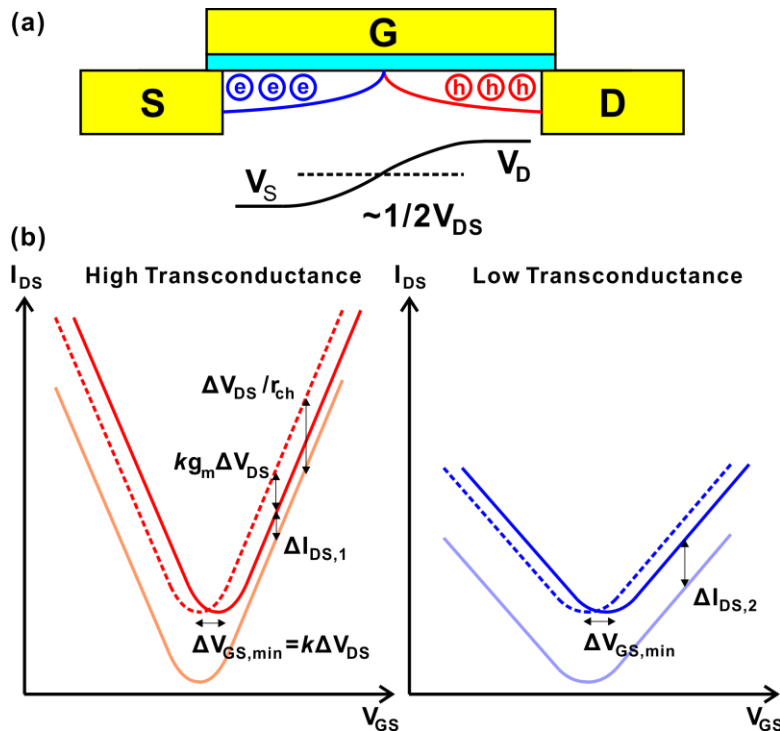
Figure 3-24 Drain-induced-minimum-shift in graphene transistors (a) Simplified potential profile in the GFET channel when the device is biased at the minimum conduction point. (b) Effect of the transconductance, g_m, on the DIMS-induced current saturation in two devices with different g_m. Clearly, for g_{m1}>g_{m2}, $\Delta I_{DS,1} < \Delta I_{DS,2}$.
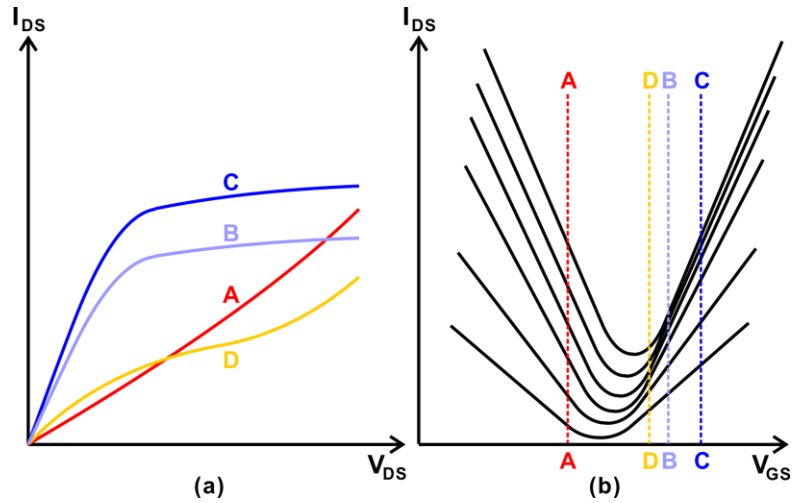
Figure 3-25 Correspondence between output characteristics and the transfer characteristics of graphene transistors subject to drain-induced-minimum-shift. Schematic diagram describing the DIMS-induced current saturation in GFETs for $V_S=0$ V and $V_D>0$ V. (a) I_{DS} vs. V_{DS} and (b) I_{DS} vs. V_{GS}. It is clear that the positive V_{DS} can cause the minimum conduction point to shift positive and result in the transfer curves crowding together on the electron conduction side in (b). Curves B and C in (a), which correspond to lines B and C in (b), will have current saturation. Curve A in (a), which corresponds to line A on the hole conduction side in (b), will have no current saturation, and can even become slightly super-linear.
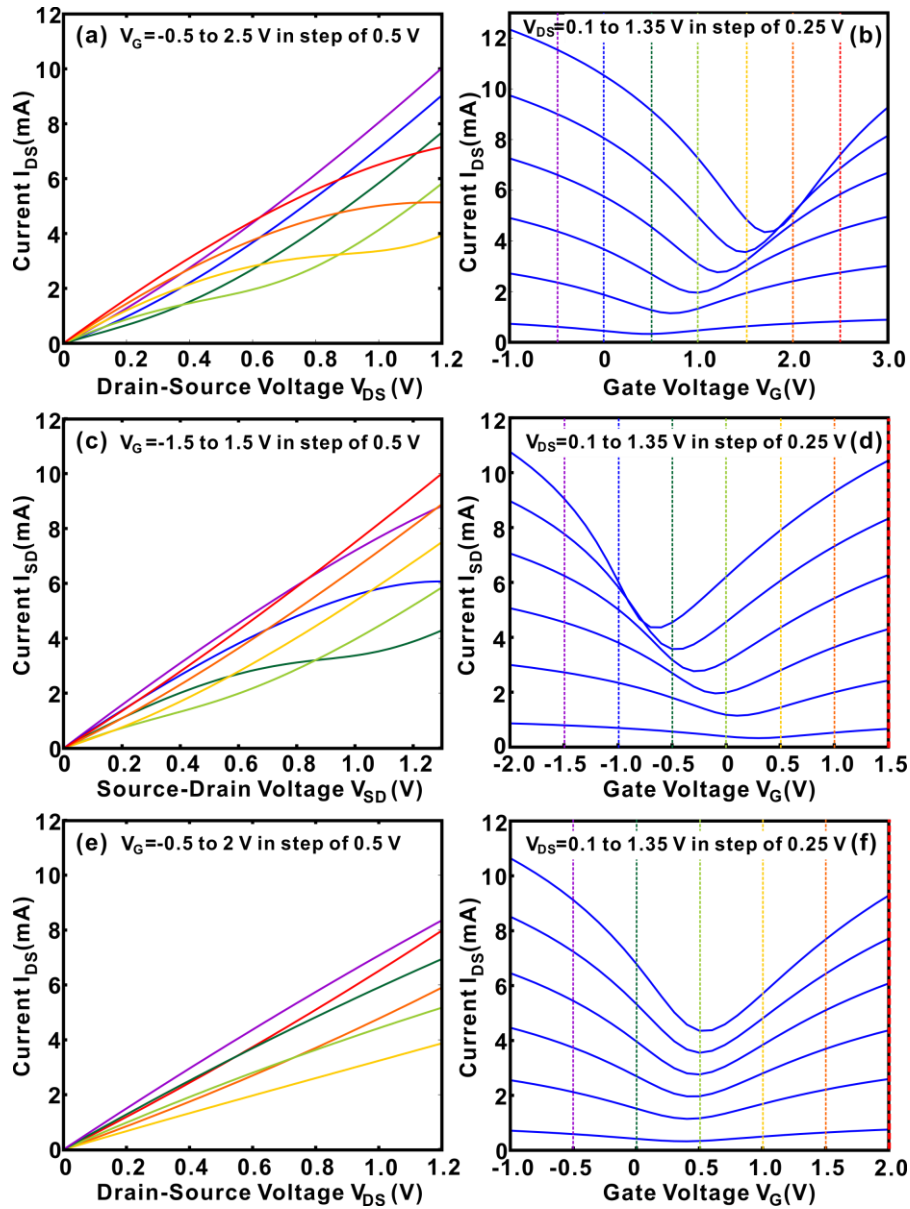
Figure 3-26 Experimental result of DIMS-induced current saturation in GFETs (a) For $V_S=0$ V and $V_D>0$ V, the current saturates on the electron conduction side, but not on the hole conduction side. (b) For $V_S=0$ V and $V_D<0$ V, the current saturates on the hole conduction side, but not on the electron conduction side. (c) With symmetric bias t the DIMS induced current saturation is eliminated. The device shown above does not have true velocity saturation. The current saturation observed in (a) and (c) are only due to DIMS effects. The output characteristics in (a), (c) and (e) are taken at gate biases that correspond to the dotted lines of the same color in (b), (d) and (f), respectively. All data is taken from the same device with $L_G=2\mu m$ and $L_{DS}=2$ μm. More device details are given in the text. The Si substrate is grounded.

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Chapter 4. Graphene Device for RF Applications

4.1. Basics of RF Analysis

4.1.1. Two-Port Network and *S*-Parameters

When electromagnetic (EM) signals propagate at low frequencies, the wavelength of the signal is many times longer than the physical dimension of the relevant object of interests. Under such conditions, the phase of the signal is of little interests for analyzing the propagation of these EM waves in the medium. This is typically the case in electronic circuits operating close to DC conditions where the circuits can be easily described using non-phase-shifting elements such as resistance and DC voltage supplies. However, when the operation frequency of electronic devices increases, particularly when it approaches and exceeds the microwave frequency range (300 MHz-300 GHz, $\lambda=1$ m~1 mm), the wavelength of the electrical signal traveling within the device structure starts to become comparable to the physical size of the device itself. As a result, the incident and reflected waves become distinguishable and the phase shift between the input voltage and the resultant current can no longer be ignored with respect to the dimension of the device. Hence, the low-frequency approach of device analysis and conventional circuit theory cease to be valid for analyzing such devices and circuits. Even though the operation of any high frequency electronic devices in the microwave frequency range is fundamentally governed by the Maxwell′s equations that describe the classical electromagnetism, the resulting solutions would be tedious, computationally expensive and lacking high level insight to the critical aspects of device physics. For most device level studies, we are more interested in the terminal quantities of the device such as voltage and current relation at the input and output port, while the detailed propagation of electromagnetic waves within the device structure is of lesser concern and the device of interest may be represented at a level of abstraction using lumped element approach. For this purpose, the terminal behavior of the high frequency transistors can be well characterized by the two-port network theory while the device itself can be described by lumped-element approach using the small-signal equivalent circuit model. It is worth noting that this approach of understanding the RF transistors is particularly useful at the microwave frequency range where the frequency is high enough that many of the parasitic components of the device can no longer be ignored. On the other hand, the frequency is still low enough compared to

optical wavelengths, at which a continuous element representation of the device should be used and full details of wave propagation within the device structure becomes important. Hence, as far as we are concerned in this Chapter, we can employ a lumped-element representation to analyze high frequency graphene transistors, which allow deep insight about the device operation to be developed that is useful for device design and optimization with relatively simple formulations.

A Port 1 (Signal Input)   Port 2 (Signal Output)   **B** Port 1 (Signal Input)   Port 2 (Signal Output)

Gate o—i_1— Two-Port Network —i_1— o Drain   Gate o— a_1 / b_1 —Two-Port Network— a_2 / b_2 —o Drain
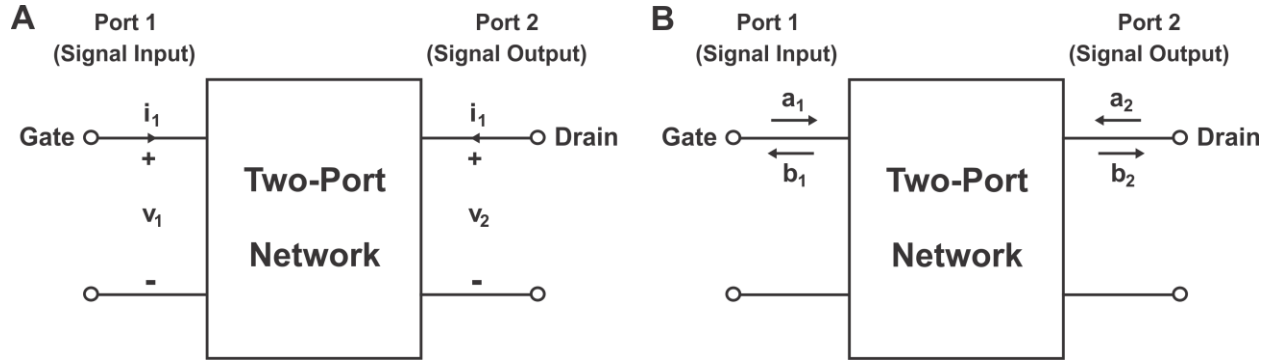
Figure 4-1 Schematic representation of 2-port networks(a) 2-port network with currents and voltages defined as the terminal quantities at the input and output. i_1 and v_1 are current and voltage at the input port (Port 1). i_2 and v_2 are current and voltage at the output port (Port 2). (b) 2-port network with incident and reflected waves defined as terminal quantities at the input and output. a_1 and b_1 are incident and reflected power waves at the input port (Port 1). a_2 and b_2 are incident and reflected power waves at the output port (Port 2).

Two-port network theory can be used to characterize the behavior of any transistor [212]. A two-port network has an input port P1 and an output port P2 (Figure 4-1). If we denote the currents at the input and output ports as i_1 and i_2, the respective voltages as v_1 and v_2, then the two-port network can be fully described by a matrix relating the voltages and currents as far as the external behavior of the device is concerned. We have,

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

$$v_1 = z_{11}i_1 + z_{12}i_2$$

$$v_2 = z_{21}i_1 + z_{22}i_2$$

$$z_{11} = \frac{v_1}{i_1}\bigg|_{i_2=0} \qquad z_{12} = \frac{v_1}{i_2}\bigg|_{i_1=0} \qquad z_{21} = \frac{v_2}{i_1}\bigg|_{i_2=0} \qquad z_{22} = \frac{v_2}{i_2}\bigg|_{i_1=0}$$

(4-1)

where z_{11} is the open circuit input impedance, z_{22} is the open circuit output impedance, z_{12} is the open circuit reverse transfer impedance and z_{21} is the open circuit forward transfer impedance. These so-called Z-parameters are just one of the several equivalent ways for representing a two-port network. Other formulation of the characteristic matrix is also possible using for example Y-parameter, H-parameters or S-parameters, which essentially represents the same information about the 2-port network in different forms. However, in characterizing high frequency two-port networks, it is usually more desirable to use the S-parameters. Although Z- (impedance), Y- (admittance) and H- (hybrid) parameters are conceptually easy to understand and are more closely related to current and voltage quantities often used in DC characterization, it is usually difficult to achieve open or short circuit termination at high frequency, which are essential conditions for extracting the Z- and Y-parameters. On the other hand, the S-parameters can conveniently overcome these issues allowing fast and accurate characterization of two-port networks.

Scattering parameters or S-parameters refer to the matrix elements that relate the forward traveling waves to the backward traveling waves at both the input and output ports of a network system. For a two-port network, we define a_1 and b_1 as the incident and reflected power wave variables at P1, a_2 and b_2 as the incident and reflected power wave variables at P2. a_1, a_2, b_1 and b_2 are defined in terms of the total current and voltage as follows:

$$a_1 = \frac{V_1 + Z_0 I_1}{2\sqrt{Z_0}} \qquad a_2 = \frac{V_2 - Z_0 I_2}{2\sqrt{Z_0}}$$

$$b_1 = \frac{V_1 - Z_0 I_1}{2\sqrt{Z_0}} \qquad b_2 = \frac{V_2 + Z_0 I_2}{2\sqrt{Z_0}}$$

(4-2)

The relation can be inverted to express the currents and voltages in terms of the wave variables:

$$V_1 = \sqrt{Z_0}(a_1 + b_1) \qquad V_2 = \sqrt{Z_0}(a_2 + b_2)$$

$$I_1 = \frac{1}{\sqrt{Z_0}}(a_1 - b_1) \qquad I_2 = \frac{1}{\sqrt{Z_0}}(b_2 - a_2)$$

(4-3)

Z_0 is the characteristic impedance, which is designed to be 50 Ω in most systems. The linear equations describing the two-port network are

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

(4-4)

The S-parameters s_{11}, s_{12}, s_{21}, and s_{22} are:

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2=0}$$ is the input reflection coefficient with the output terminated by a matched load

($a_2=0$ when $Z_L=Z_0$).

$$S_{12} = \frac{b_1}{a_2}\bigg|_{a_1=0}$$ is the output reflection coefficient with the input terminated by a matched load

($V_S=0$ when $Z_S=Z_0$).

$$S_{21} = \frac{b_2}{a_1}\bigg|_{a_2=0}$$ is the forward transmission gain with the output terminated by a matched load.

$$S_{22} = \frac{b_2}{a_2}\bigg|_{a_1=0}$$ is the reverse transmission gain with the input terminated by a matched load.

  The key benefits of using S-parameters for transistors and other active devices characterization lies in the fact that it is much easier to measure these parameters than the impedance and admittance matrix elements. In measuring most other parameters, it is often necessary to maintain open and short circuits at the input and output ports of the device. While it is easy to achieve at low frequency, the open and short termination can be very hard to obtain at high frequency due to the presence of inevitable lead inductance and capacitance. Such measurements must rely on tuning stubs to create open and short conditions at each frequency, which is often complicated, tedious and have poor accuracy. Measurements of S-parameters, on the other hand, only requires the signal termination in one direction of transmission, which can be easily achieved using termination resistance that matches the characteristic impedance of the system, i.e.

$Z_L = Z_0$. Unlike terminal voltages and currents, traveling wave variables also have the same magnitude at any location along a lossless transmission line. Hence, the excitation source and the device under test (DUT) can be separated by some distance during the measurements as long as they are connected by low-loss transmission lines.

4.1.2. Small-signal Equivalent Circuits Analysis of Field Effect Transistors

A transistor device operating at microwave frequency may be best described by the small signal-equivalent circuit model, which treats the transistor device as a circuit (Figure 4-2). Here, the term "small-signal" means that the signal voltage level in the device is on the order of the thermal voltage, which is $k_B T/q = 26$ mV at 300 K. Under such constraints, the various non-linear characteristics of the graphene transistor, as well as the associated parasitic effects, can be linearized around the particular bias conditions at which the device is operating. So for each bias point, we have a lumped-element model to describe the device, typically taking the linear term from the Taylor expansion of the large-signal characteristics of the transistor.

Table 4-1 shows the key elements in a typical small-signal equivalent circuit for a transistor where the physical origin of each component is described.
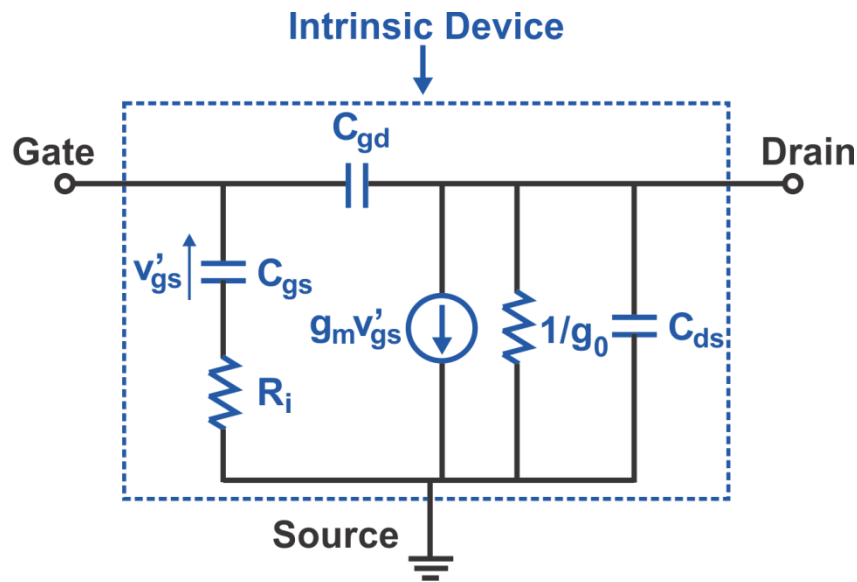
Figure 4-2 The small-signal equivalent circuit for the intrinsic part of a transistor device. Only the intrinsic components of the device are included.

		Name	Physical Origin
Intrinsic	C_{gs}	Gate-source capacitance	Modulation of gate charge by gate-source bias
	C_{gd}	Gate-drain capacitance	Modulation of gate charge by gate-drain bias
	C_{ds}	Drain-source capacitance	Capacitance between drain and source electrodes (e.g. substrate capacitance)
	R_i	Input resistance	Lumped element approximation of the distributed channel resistances
	R_{gd}	Gate-drain resistance	Complement of R_i to reflect symmetrical nature of the device
	g_m	Transconductance	Drain current gain resulting from variation in the gate voltage bias
	τ	Transconductance delay	Time delay between the change in the gate bias and the drain current. This leads to a phase difference between the gate voltage and drain current in steady state at high frequency
	g_0	Output conductance	Differential drain current change with respect to variation in drain voltage bias
Extrinsic	R_g	Gate resistance	Resistance of the gate electrode to gate current flow
	R_d	Drain resistance	Resistance of the drain region leading to the intrinsic channel. It mainly consists of two components: the contact resistance and resistance of the access region of the device on the drain side
	R_s	Source resistance	Resistance of the source region leading to the intrinsic channel. It mainly consists of two components: the contact resistance and resistance of the access region of the device on the source side

Table 4-1 The key elements in a typical small-signal equivalent circuit for a transistor. The name and physical origin of each component are also listed.

In graphene transistors, the drain current is influenced by both the drain-source voltage and gate-source voltage. The partial derivatives of the drain-source current I_{DS} with respect to V_{GS}

and V_{DS} are common parameters in a small-signal model to account for these effects, which are called the transconductance g_m and output conductance g_0 in the device community.

$$g_m = \frac{dI_{DS}}{dV_{GS}}\bigg|_{V_{DS}=constant}$$

(4-5)

$$g_0 = \frac{dI_{DS}}{dV_{DS}}\bigg|_{V_{GS}=constant}$$

(4-6)

In some models, a delay time τ may also be used to account for the delay between changes in V_{GS} and the response in the drain-source current. As the gate voltage induces current changes in the channel through a capacitance, the carrier charge and discharge process gives rise to the delay in the response and phase shift between the applied voltage and the resulting current. This leads to a frequency dependent phase shift to g_m as given below:

$$g_m(\omega) = g_m e^{-j\omega\tau}$$

(4-7)

where $\omega = 2\pi f$ is the angular frequency of the signal. However, for the output conductance, the delay can usually be ignored since the dependence of I_{DS} on V_{DS} is mostly due to short-channel effects, leakage or channel length modulation effects where minimum charging and discharging processes are involved.

At high frequency, the capacitive components also play an equally important role as the current-voltage components, g_m and g_o, in determining the transistor performance. The key capacitive elements include the charge voltage coupling between the gate, source and drain electrodes, C_{gs}, C_{gd}, and C_{ds}, defined as:

$$C_{gs} = \frac{dQ_G}{dV_{GS}}\bigg|_{V_{DS}=constant}$$

(4-8)

$$C_{gd} = \frac{dQ_G}{dV_{DS}}\bigg|_{V_{DS}=constant}$$

(4-9)

$$C_{ds} = \frac{dQ_D}{dV_{DS}}\bigg|_{V_{DS}=constant}$$

(4-10)

where Q_G is the charge on the gate electrode and Q_D is the charge on the drain electrode. Finally, the model also includes a few resistive components. R_i is a lumped element approximation of the distributed channel resistances associated with the time to charge and discharge the gate capacitance C_{gs}. Now, we have most of the elements constituting the intrinsic part of the device. Figure 4-3 shows a more complete view of the transistor under small-signal conditions. R_S and R_D account for the access resistances on the drain and source side, respectively, while R_G is the resistance of the gate electrode itself. The inductive effects of each electrode as well as the capacitive effects contributed by the measurement pads are also included.
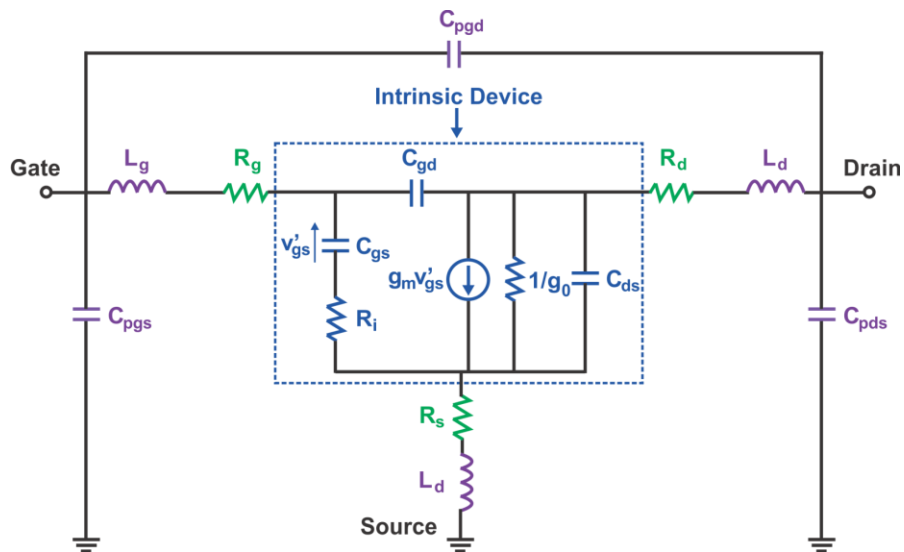
Figure 4-3 The extended small-signal equivalent circuit model for a transistor device, including the capacitive, inductive and resistive effects of the measurement pads.

4.1.3. RF Characteristics of a Graphene Transistor

In assessing the high frequency performance of graphene transistors, we mainly focus on the short-circuit current gain cut-off frequency f_T of the transistor. The maximum oscillation frequency, which characterizes the unity power gain frequency of the transistor, is also reported for some of the transistors, but the key effort here is in improving the f_T of the device. The f_T and f_{max} of the device can be measured as the frequency at which the short-circuit current gain h_{21} and the unilateral power gain U of the device reach unity, respectively. The f_{max} can also be characterized from the unity maximum stable gain (MSG) or the maximum available gain (MAG) depending on the device stability. h_{21}, U, MSG and MAG can all be extracted directly from the measured S-parameters of the device after the parasitic effects contributed by the measurement pads has been de-embedded. All the three gain quantities should in principle lead to the same extracted f_{max}.

From the small-signal equivalent circuit model, we can derive the dependence of f_T on the physical parameters and understand what are the key aspects of the device that are limiting the f_T and f_{max} of the transistor. Here, we will only go through a simplified version of the small-signal model while a more general expression relating f_T and the key parasitic components will also be given.
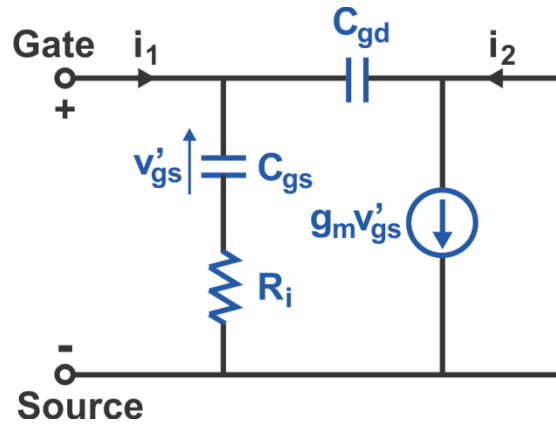
Figure 4-4 The small-signal analysis of the device with output shorted. Only the key intrinsic components of the device are shown.

The f_T is defined to be the frequency at which the current gain of the device $|h_{21}| = |i_2/i_1|$ is unity with the output short-circuited as shown in

Figure 4-4. Here, we only consider the intrinsic part of the device while also ignoring the effects of the output conductance g_0 and the drain-source capacitance C_{ds} that is usually much smaller than C_{gs} and C_{gd}. Standard circuit analysis leads to the following expressions for i_1 and i_2:

$$i_1 = \frac{V_{gs}}{\frac{1}{j\omega C_{gs}} + R_i} + \frac{V_{gs}}{\frac{1}{j\omega C_{gd}}}$$

(4-11)

$$i_2 = g_m e^{-j\omega\tau} v_{gs} = g_m e^{-j\omega\tau} \frac{\frac{1}{j\omega C_{gs}}}{\frac{1}{j\omega C_{gs}} + R_i} V_{gs}$$

(4-12)

$$|h_{21}| = \left|\frac{i_2}{i_1}\right| = \left|\frac{g_m e^{-j\omega\tau}}{j\omega(C_{gs} + C_{gd}) - \omega^2 C_{gs} C_{gd} R_i}\right| \cong \frac{g_m}{2\pi f(C_{gs} + C_{gd})}$$

(4-13)

The approximation in the last step made the assumption that $\omega^2 C_{gs} C_{gd} R_i \ll \omega(C_{gs} + C_{gd})$, which is typically the case in most transistor structures. Hence, the intrinsic short-circuit current gain cut-off frequency of the transistor can be obtained by setting eq. (4-13) to unity and f_T is given by:

$$f_T = \frac{g_m}{2\pi f(C_{gs} + C_{gd})}$$

(4-14)

Another expression for f_T that is directly based on the physical quantities of the transistor, is give as [205]:

$$f_T = \frac{v_{sat}}{2\pi L_g}$$

(4-15)

where eq. (4-15) can be obtained by substituting $g_m = v_{sat}(C_{gs} + C_{gd})/L_g$. Here, we can see that f_T value of a transistor has fundamental physical basis and is directly related to both the intrinsic carrier dynamics and the gate length of the device to the first order approximation. In other words, it is directly related to carrier transit delay, which is the time taken for the carrier to move from the source to the drain of the device. However, eq. (4-14) and (4-15) do not account for the extrinsic circuit elements such as R_s, R_d, and g_0, which are critical in graphene devices, especially when the gate length becomes shorter. A more rigorous treatment of the small signal model, where all the key parasitic components in the active region of the device shown in Figure 4-3 are accounted for, leads to the following more general expression for f_T [213]:

$$f_T = \frac{g_m/(2\pi)}{[C_{gs} + C_{gd}] \cdot [1 + (R_S + R_D)g_0] + C_{gd} \cdot g_m \cdot (R_S + R_D)}$$

(4-16)

The power gain cut-off frequency f_{max} on the other hand depends on both the current gain and voltage of the device. Figure 4-5 shows a commonly used small signal equivalent circuit for estimating the power gain of a transistor. Simple circuit analysis yields the following expression for calculating the current gain $|h_{21}|$ and voltage gain $|A_v|$.
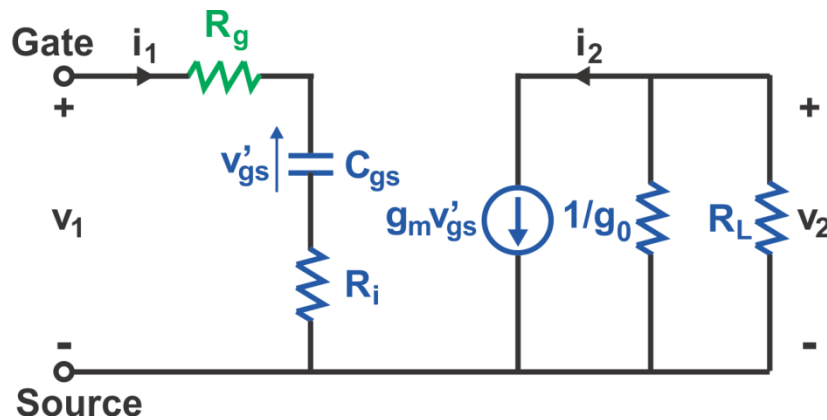
Figure 4-5 The small-signal equivalent circuit for estimating the power gain of a transistor device. The gate resistance R_G is included in the model, in additional to the key components of the intrinsic device.

$$|h_{21}| = \left|\frac{i_2}{i_1}\right| = \frac{g_m}{2\pi f C_{gs}} = \frac{f_T}{f}$$

(4-17)

$$|A_v| = \left|\frac{v_2}{v_1}\right| = \frac{g_m(r_0//R_L)}{\sqrt{1 + \omega^2 C_{gs}^2(R_g + R_i)^2}} \cong \frac{g_m(r_0//R_L)}{\omega C_{gs}(R_g + R_i)}$$

(4-18)

Here the approximation in the last step assumes $1 \ll \omega^2 C_{gs}^2(R_g + R_i)^2$. $r_0 = 1/g_0$. Since the maximum oscillation frequency f_{max} is defined under the condition of conjugate matched load for maximum power transfer to the load. In this case, we have $r_0 = R_L$. The resulting power gain is:

$$|A_P| = \frac{1}{2} \cdot \left|\frac{i_2}{i_1}\right| \cdot \left|\frac{v_2}{v_1}\right| = \left(\frac{f_T}{f}\right)^2 \frac{r_0}{4(R_g + R_i)}$$

(4-19)

By setting the power gain to unity leads to the expression for f_{max}:

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{r_0}{R_g + R_i}}$$

(4-20)

Here, it is interesting to point out that the f_{max} of a transistor not only increases linearly with f_T, but also has additional inverse square root dependence on the output conductance, the gate resistance, and the R_i of the device. This differs particularly from f_T where there is no dependence on the gate resistance R_g and f_{max} has a much stronger dependence on the output conductance since in eq. (4-20), the inverse square root dependence on g_0 combines with the weak dependence on g_0 in the f_T expression. A more rigorous treatment that also takes into account the remaining parasitic components of the device leads to the following complete expression for f_{max}:

$$f_{max} \cong \frac{f_T}{2}\sqrt{\frac{1}{(R_g + R_s + R_i)g_0 + (2\pi f_T)R_g C_{gd}}}$$

(4-21)

4.1.4. On-chip S-parameters Characterization

On-chip microwave measurements of the devices fabricated during this thesis were carried out using vector network analyzers [212]. The fundamental purpose of microwave network analysis is to accurately measure the incident, reflected and transmitted signals related to a linear network that is embedded within a transmission line medium. The same information can be defined in different forms and the resulting characteristics of the network is often given in terms of impedance, admittance, reflection coefficient, VSWR, return loss, S-parameters. Similarly, the transmission coefficient can be given in terms of insertion loss, transmission, gain, group delay and insertion phase. Because the measurement concerns the traveling waves on a transmission line environment where the characteristic ratios are functions of positions on the transmission line, it is necessary to define a reference plane with respect to which we report the characteristic transmission and reflection ratios. Very often, the reference plane is defined at the surface of contact of the outer conductors of a mating pair of coaxial connectors or a pair of waveguide flanges, though the choice can be arbitrary in principle.

Figure 4-6 shows the schematic of a vector network analyzer. Most VNAs available today have one integrated RF signal generation source, and supports a pair of input and output ports with automatic solid-state forward and reverse measurement switches. Either test port 1 or test port 2 can serve as the input or receiving port. Newer VNA models such as Agilent N5242A support two signal generators and hence two pairs of input and output ports, which allows additional measurement capabilities such as two-tune linearity measurement of RF power amplifiers and mixer characterization. For the S-parameter measurements in this work, we use Agilent 5230A that supports a single pair of input and output ports. Each of the input and output port has a pair of directional couplers that allows the measurement of signal power in forward and reverse directions and the subsequent automated extraction of S-parameters.

The S-parameter measurement starts with careful calibration of the on-chip test setup using a standard impedance calibration substrate following either Short-Open-Load-Through (SOLT) or Line-Reflection-Reflection-Match (LRRM) methods. The errors from VNA measurements consists of systematic, random and drift errors. Systematic errors are repeatable errors across different measurements. The calibration step mainly accounts for such consistently fixed errors,

which are mainly due to mismatch and leakage in the measurement setup, isolation across the reference and test signal paths, and frequency response of the system. On the other hand, drift and random errors are non-repeatable and cannot be eliminated by means of calibration. Drift errors are usually contributed by frequency, temperature and other physical discrepancies in the measurement setup between calibration and actual measurement, while random errors are often due to variations in environmental noise and connection repeatability. The quality of the calibration is verified to ensure the S_{11} and S_{22} on a standard through pattern is below -45 dB and S_{12} and S_{21} are less than ±0.01 dB.
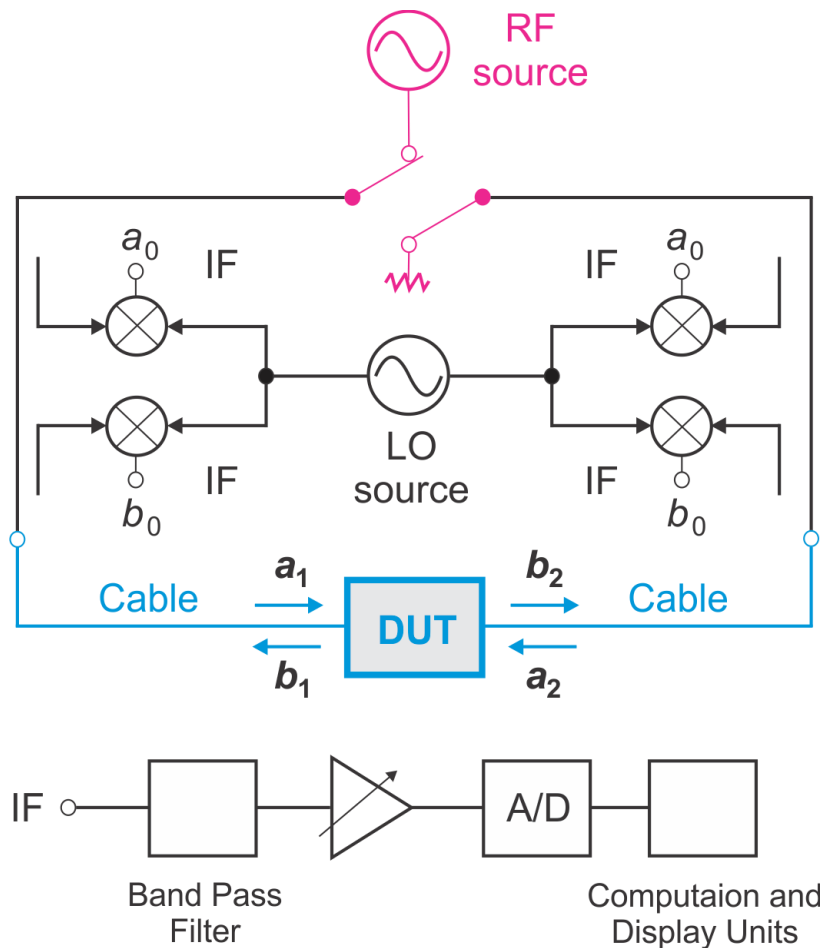
Figure 4-6 Schematic diagram showing the key internal structure of a vector network analyzer.

In the calibration step, we moved the reference plane of measurement from the internal receivers of the VNA to the tip of the GSG (ground-signal-ground) probes that are in touch with the device under test (DUT) (Figure 4-7). To allow the GSG probes to measure the DUT, RF test

pads are often created that match the pitches of the GSG probes (Figure 4-7). The entire test structure is designed in a way to allow an easy path for the high frequency electromagnetic wave signals to reach the active device region from the GSG probes. So the S-parameters output by the VNA include both the active device and the capacitive, inductive and resistive effects of the contact pads. However, we are only interested in characterizing the active device, so an additional step called "de-embedding" is needed to exclude the contact pad effects on the measured S-parameters. In other word, with the de-embedding step, we would like to further move the reference plane from location 1, which is given by measurements after calibration, to location 2 that is the active device.
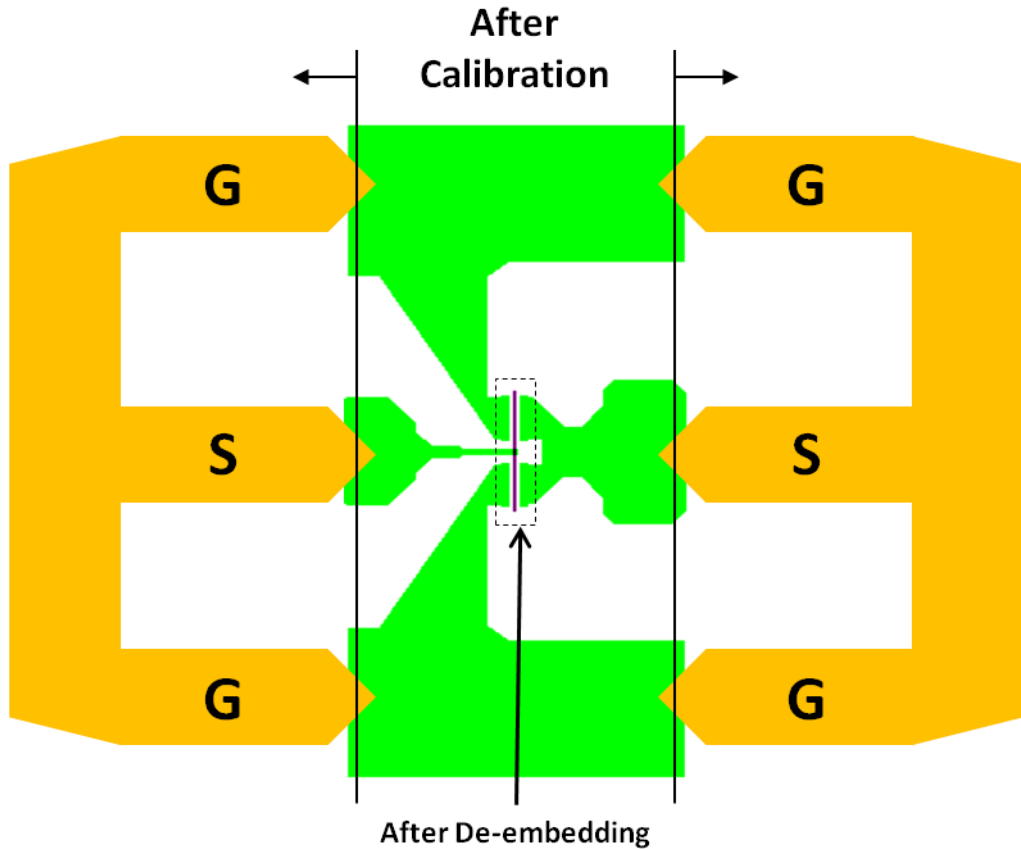
Figure 4-7 Schematic layout of a two-finger graphene transistor under RF measurement. The S-parameters measured by the vector network analyzer and corrected by the error matrix extracted from the calibration step still includes the effect of the measurement pads. We will be able to reach the S-parameters of the active device region after de-embedding the measurement pad effects. Many different de-embedding strategies are possible. In this thesis, we use the open-short de-embedding technique.

In this work, the de-embedding procedure follows the well-established standard open-short method. S-parameters of the extrinsic device are measured, together with the S-parameters of the open and short test structures. The layouts of these open and short structures are identical to that of the active device except in the graphene channel. We denote the directly measured S-parameter without de-embedding as $S'_{11}, S'_{22}, S'_{12}, S'_{21}$. Using the S-parameter measured on the open and short test structures, we can remove the pad parasitic effects from $S'_{11}, S'_{22}, S'_{12}, S'_{21}$ to obtain the S-parameters for the intrinsic part of the device $S_{11}, S_{22}, S_{12}, S_{21}$. The de-embedding follows the equation below after the S-parameters were converted into Y-parameters [214][215][216].

$$Y_{OS} = [(Y_{DUT} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}]^{-1}$$

(4-22)

where Y_{DUT} is the Y-parameter matrix of the device under test as converted from the measured S-parameters $S'_{11}, S'_{22}, S'_{12}, S'_{21}$. The first term in eq. (4-22) removes the parallel components while the second term removes the series components. The S-parameters of the intrinsic part of the device, $S_{11}, S_{22}, S_{12}, S_{21}$, can then be obtained by converting Y_{OS} into S-parameters (Figure 4-8).
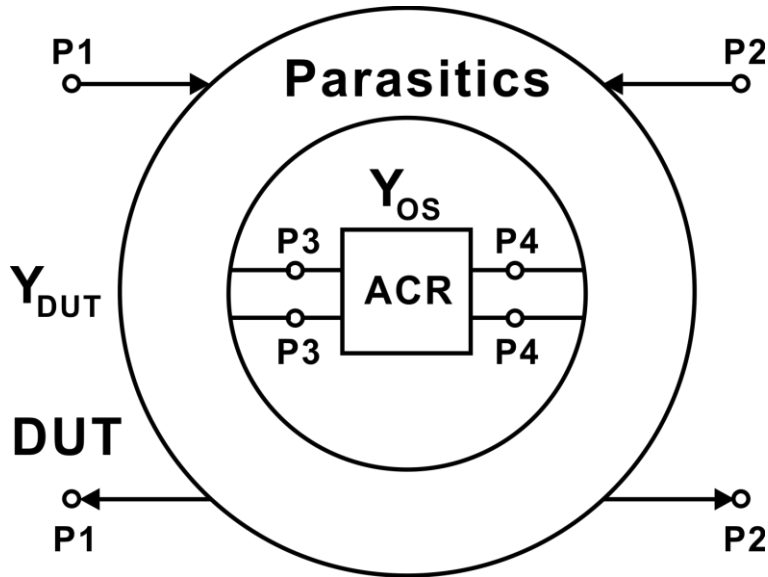
Figure 4-8 General four-port schematic of the parasitics to be de-embedded. Ports 1 and 2 measure the device under test (DUT), whereas ports 3 and 4 are connected to the active device region (ACR).

The directly measured S-parameters give the extrinsic current gain of the device that also includes the effects from pad parasitics, following the equation below:

$$h'_{21} = \frac{-S'_{21}}{(1-S'_{11})(1+S'_{22})+S'_{12}S'_{21}}$$

(4-23)

The current gain of the intrinsic (i.e. after de-embeding the pad parasitics) device can be obtained from $S_{11}, S_{22}, S_{12}, S_{21}$ as:

$$h_{21} = \frac{-S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

(4-24)

Both $|h'_{21}|$ and $|h_{21}|$ exhibit an $1/f$ dependence. The current gain cut-off frequency before de-embedding, f'_T, is the frequency at which $|h'_{21}|$ becomes unity while the current gain cut-off frequency after de-embedding, f_T, is the frequency at which $|h_{21}|$ becomes unity.

In designing the DUT and the RF contact pads, it is important to keep the pad parasitics small in order to achieve accurate extraction of f_T. For example, consider a simpler version of the de-embedding method: the "open" de-embedding, the formula for "open de-embedding" is:

$$Y_O = Y_{DUT} - Y_{open}$$

(4-25)

Assuming the measurement errors are uncorrelated, the error in Y_O is:

$$\epsilon(Y_O) = \epsilon(Y_{DUT}) + \epsilon(Y_{open})$$

(4-26)

where $\epsilon(Y_{DUT})$ and $\epsilon(Y_{open})$ are the errors from the RF characterization of the device and the open structure, respectively, which can be caused by factors including calibration error, background noise and thermal effects. It is clear that when Y_{open} becomes a significant fraction of Y_{DUT}, we will be subtracting between two large numbers. The percentage error in Y_O, hence, becomes high. The error in the de-embedded Y-parameter Y_O is also carried over when the Y-

parameters are converted to S-parameters for calculating h_{21} and hence leads to error in the extracted f_T. Due to possible errors in the S-parameter measurements of the device, the open structure and the short structure, the extracted f_T may be either over-estimated or under-estimated. As the de-embedding ratio increases, the percentage error in the extracted f_T may also get larger.

Test Structure Design: Open and Short Pads

Figure 4-9 shows the basic design of the DUT for RF measurements and the corresponding design of open and short test structures. This design of open and short pads is well aligned with the industrial RF characterization standard used for measuring silicon and III-V based devices. On the other hand, another set of open and short test structure designs (Figure 4-10) may sometimes be used for studying the intrinsic performance potential and the intrinsic carrier dynamics of graphene devices. The two sets of test structures are identical except for the gate region of the open pattern. In the standard open pattern, the gate electrode stops at region outside the active device area while the more aggressive de-embedding structure has the gate electrode of the open pattern extending into the active device region. The key difference is that in the more aggressive de-embedding, a large portion of the gate capacitances especially the fringe component that dominates shorter-channel device and the gate resistance R_G are removed from the final reported S-parameter of the active device. As a result, there is usually a large difference between the f_T values reported by these two methods with the aggressive de-embedding technique leading to f_T values many times larger than using the standard de-embedding. However, depending on the purpose of study, the two methods have their respective benefits. The standard de-embedding method should be used for benchmarking graphene device performance with conventional semiconductor devices, such as Si and III-V compounds while the more aggressive de-embedding method allows a way for measuring the more intrinsic performance of the graphene transistors, allowing studies of the ultimate performance potential and scaling trend of graphene FETs. The difference in extracting the f_T results using these two methods will be compared in Section 4.3 of this chapter.
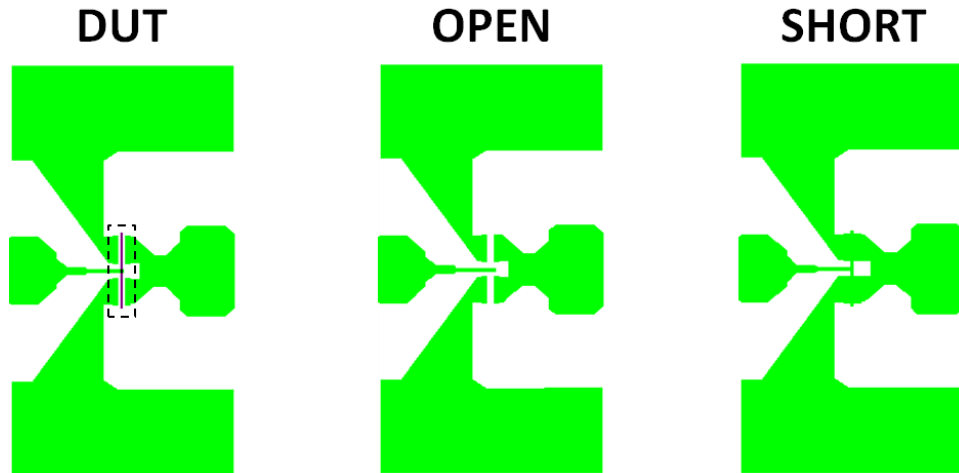
Figure 4-9 The device under test, the open structure and the short structure used in the standard de-embedding process.
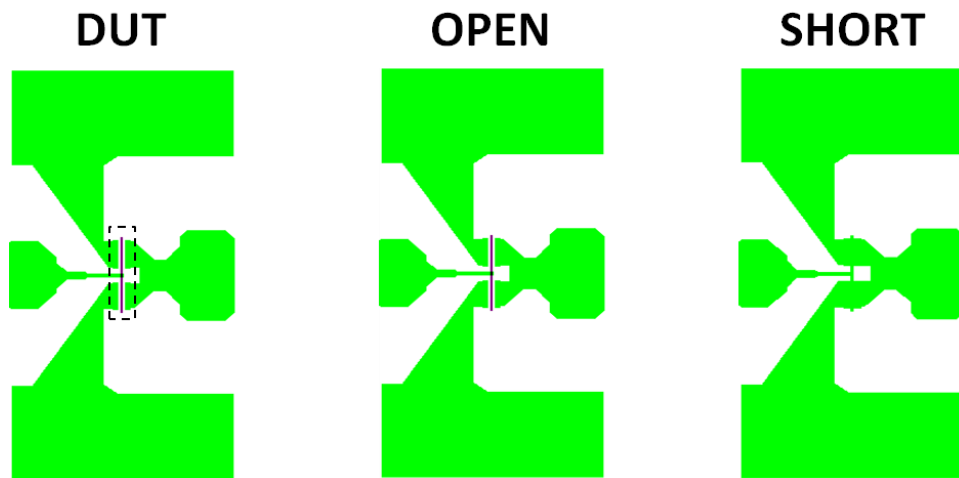
Figure 4-10 The device under test, the open structure and the short structure used in an alternative de-embedding process that allows better access to the intrinsic performance of the transistor.

4.2. Graphene Field Effect Transistors for RF Applications

A significant part of the work in this thesis has focused on developing high frequency graphene RF transistors. Although pushing for better performance metrics such as f_T and f_{max} is important, the focus of this thesis is on understanding the device physics that is limiting the performance and demonstrating new device concepts and structures. This part of the thesis will demonstrate

several novel device structures and analyze their RF performances. New methods will also be proposed to analyze their carrier transit delays.

Figure 4-11 shows the f_T and f_{max} characterization of a typical long channel CVD graphene transistor fabricated on a SiO$_2$/Si substrate. For this long channel device with gate length L$_G$= 1.6 μm and channel width of 2×25 μm, the f_T of the device is 3.6 GHz and f_{max} is 6.5 GHz. The scaling behavior of the graphene transistors is shown in Figure 4-11(b). Figure 4-3 lists the small signal equivalent circuit parameters for two devices with the same gate lengths. The device structure is far from being optimized for RF applications. In this sub-section, we explore new designs of graphene device that improves the substrate quality, reduces gate resistance or allows self-alignment of source and drain contacts. The new designs can lead to significant improvements in the RF performance with the highly scaled devices reaching intrinsic performance at hundreds of GHz range.

	V$_{SUB}$ = 0 V	V$_{SUB}$ = -50 V
f_T (GHz)	2	3.5
R_S (Ω.mm)	5.6	2.2
R_d (Ω.mm)	6.6	2.3

Table 4-2 Effect of substrate bias on small signal access resistances. V_{ds}=3 V, V_{gs}= 1.5 V.

Device	Vds (V)	Vgs (V)	Cgs (pF/mm)	Cgd (pF/mm)	g$_{m,ext}$ (mS/mm)	Rs (Ω.mm)	$f_{T,ext}$
1	3	1.5	3.3	2.5	120	2.2	3.0
2	3	1.5	3.6	2.6	115	2.2	2.8

Table 4-3 Main elements of the small signal equivalent circuit of two graphene transistor with L_g = 1.6 μm and a channel width of 2×25 μm^2.
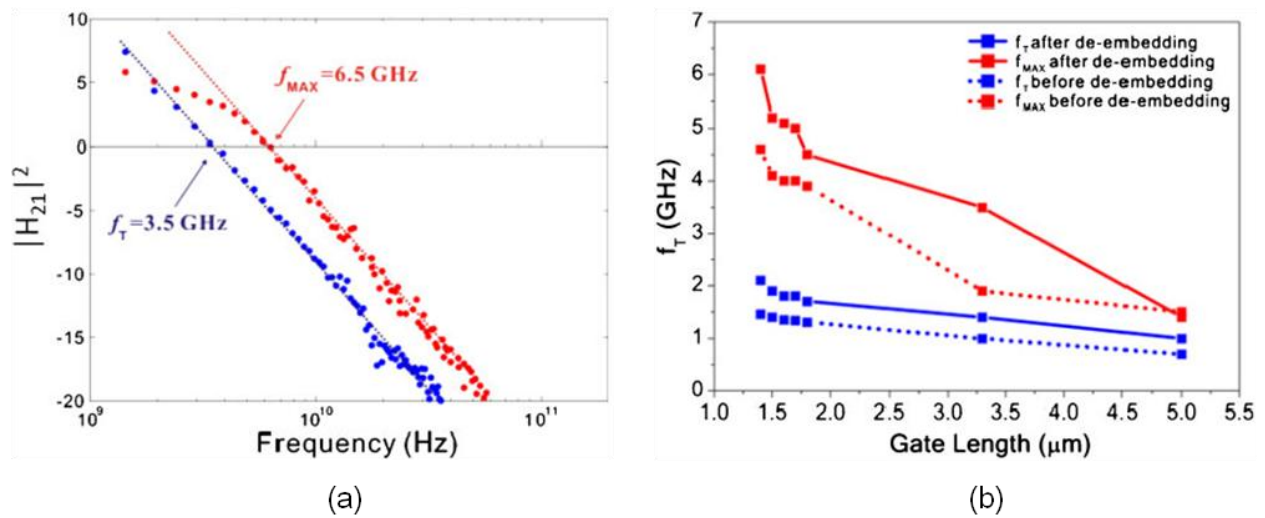
Figure 4-11 RF performance and scaling behavior of graphene transistors (a) RF performance of a long channel (L_G= 1.6 μm) CVD graphene transistor. (b) The scaling behavior of micrometer-scale CVD graphene transistors.

4.2.1. BN/Graphene/BN FETs: Benefits of Inert 2D Crystal Substrates

Most of today's RF GFETs are fabricated on either SiO_2 [120] or SiC [119] substrate. Graphene was first isolated on SiO_2 due to the ability to identify single layer graphene using optical microscopes while the growth of graphene on SiC provides a natural substrate for these devices. However, neither SiO_2 nor SiC are ideal substrates for graphene. One problem with thermally grown SiO_2 (a few hundred nm thick) is that it often leads to a high surface roughness, as shown in Figure 4-12. In addition, the oxide typically has a large density of charge traps and defects. Graphene on SiC, on the other hand, suffers from a terraced rough substrate surface that can limit device performance by scattering charge carriers flowing in the active graphene layer [55]. Hence, in order to take full advantage of the ultra high mobility promised by graphene, we need to either remove the substrate [217] or use a better one. Although suspended graphene sheets have shown the highest mobility ever measured at room temperature in any semiconductor, the fragile suspended graphene membrane leads to many fabrication challenges and reliability issues. An alternative approach is to use a better substrate, such as hexagonal boron nitride (hBN) [87], which has the same atomic structure as graphene and shares many of its properties. The 2D planar structure of hBN also gives this material an ultra flat surface (Figure 4-12(a)) that is also free of dangling bonds and charge traps. Hence, it provides an ideal environment for graphene to

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sit on. Recent work has shown carrier mobility as high as 40,000 cm^2/V.s in bilayer graphene (BLG) on hBN at room temperature [87].

In this sub-section, we demonstrate the first BN/Graphene/BN RF field effect transistor, which has hBN as both the substrate and the gate dielectric with bilayer graphene as the channel material. This novel structure can preserve the high carrier mobility in the bilayer graphene channel and hence has a great potential for high frequency transistor applications.

The fabrication process of the BN/Graphene/BN devices studied in this work is summarized in Figure 4-13(a-d). A hexagonal boron nitride flake is first exfoliated on a SiO$_2$/Si substrate. A separate SiO$_2$/Si sample is then coated with polyvinyl acetates (PVA) and polymethyl methacrylate (PMMA); and bilayer graphene flakes from natural graphite are exfoliated on top of the PMMA and transferred using the technique described in Ref. [218]. A flip chip bonder is used in the transfer process to allow for an accurate alignment between the hBN flake and the bilayer graphene flake. The alignment accuracy is within 1-2 μm. Figure 4-13(e) shows an optical micrograph of a bilayer graphene flake transferred on top of an hBN substrate. Then, the source and drain contacts are defined by e-beam lithography and formed by depositing a 0.7 nm Cr /50 nm Au metal stack using thermal evaporation. The contact resistance is typically 200 Ω.μm. After that, a second layer of hBN is exfoliated, aligned and transferred on top of the bilayer graphene channel. This second hBN flake becomes the top gate dielectric of the GFET. Figure 4-13(f) shows the device after the source and drain contacts are made and the top hBN layer has been transferred. Finally, the top gate of the device is defined by e-beam lithography and formed by a 10 nm Ti/40 nm Au multilayer using e-beam evaporation. Figure 4-13(g) and 2(f) show the finished device, which has a gate length L$_G$=450 nm and source-drain distance L$_{DS}$=850 nm. The width of the device active region is 3 μm. The top gate dielectric has a thickness of 8.6 nm as measured by atomic force microscopy (AFM), which gives a top-gate capacitance of 0.39 μF/cm^2. The conductive Si substrate forms the bottom gate of the device with a dielectric consisting of 285 nm SiO$_2$ plus the hBN substrate layer. The top and bottom gate capacitances ratio is $C_{TG}/C_{BG} \approx 30$.

Figure 4-14(a) shows the transfer characteristics (I$_{DS}$ vs. V$_{GS}$) of the fabricated transistor. At V$_{DS}$=1 V, the device achieves a high current density close to 1.2 A/mm. The minimum

conduction point of the transistor is very close to 0 V. This indicates negligible doping effects from both the hBN substrate and the hBN top gate dielectric. Typically, bilayer graphene on hBN substrate produced in our laboratory show Hall mobility in excess of 15,000 cm^2/V.s. In addition, there is very little mobility degradation after the second hBN layer (i.e. the top gate dielectric) is transferred on top. The maximum transconductance g_m is close to 250 mS/mm. The extrinsic DC transconductance is mainly limited by the access resistances and gate capacitance, not the mobility.

Figure 4-15(a) shows the RF performance of the device. With L_G=450 nm and at V_{DS}=1 V, the device has a current-gain cut-off frequency f_T=5 GHz and f_T=22 GHz before and after de-embedding the pad capacitances, respectively. The de-embedding procedure follows the well-established standard open-short method [207][119][120]. In these measurements, the back-gate, i.e. substrate, was grounded.

The substrate bias has a significant effect on the RF performance of the device. With the substrate grounded, the un-gated access regions on both the source and the drain side of the device have their Fermi energy levels located near the Dirac point (the minimum conduction point). This leads to relatively large source and drain access resistances (R_S and R_D). The resistances of these un-gated regions can be reduced through electrostatically doping them by biasing the substrate. This reduction in the resistances significantly increases the frequency performance of the device [214]. For example, Figure 4-15(b) shows that when the substrate is biased at -30 V, the current gain cut-off frequency increases to 6 GHz and 33 GHz before and after de-embedding.

The DC and RF performance of this device was also compared to a control device fabricated on a SiO$_2$ substrate and with a 16 nm Al$_2$O$_3$ gate dielectric. This control device also uses a bilayer graphene flake exfoliated from natural graphite as the channel material. The Al$_2$O$_3$ gate dielectric is formed by naturally oxidizing 3 nm of e-beam evaporated Al followed by atomic layer deposition of 13 nm Al$_2$O$_3$. The thickness of the Al$_2$O$_3$ gate dielectric was chosen to render the same top gate capacitance as in the BN/Graphene/BN FET. The Hall mobility of our bilayer graphene on SiO$_2$ is typically between 1,500 and 2,000 cm^2/V.s [219]. This low mobility is

mainly due to the scattering introduced by the SiO_2 substrate. The mobility degrades by ~30% after oxide deposition due to the additional impurities introduce to the system.

For similar device dimension and gate capacitances, the BN/Graphene/BN FET shows a peak transconductance (g_m) of 250 mS/mm, which is about 70% higher than that in the control sample that has a peak g_m of only 140 mS/mm (Figure 4-14). To further analyze and compare the two devices, the virtual source model proposed in Ref. [71] is used to fit their DC characteristics (Figure 4-14). The model extracts a field effect mobility of 6,500 cm^2/V.s in the BN/Graphene/BN FET and 1,200 cm^2/V.s in the control device, respectively. This carrier mobility, while much higher than the control device but relatively low compared to other reported mobility values of bilayer graphene on hBN, is possibly due to bubbles and ripples created during the transfer process; and the measurements being taken at high drain biases (V_{DS}=1 V) and high current density. The carrier injection velocities are estimated to be about 3.5×10^7 cm/s in the BN/Graphene/BN FET and 2.5×10^7 cm/s in the control device. This gives an indication of the significant advantage that an hBN substrate and dielectric can have over SiO_2 and Al_2O_3 in terms of preserving the high carrier mobility and carrier velocity in graphene.

Figure 4-16 compares the peak f_T of these two devices of equal gate length and gate capacitance. For V_{DS}=1 V, the BN/Graphene/BN FET has its highest f_T=33 GHz at V_{BG}=-30 V, and V_{TG}=0 V while the control sample has its highest f_T=18 GHz at V_{BG}=-10 V, and V_{TG}=1 V, demonstrating a significant improvement in peak f_T due to the change of substrate and the gate dielectric material.

Hence, we have shown here that the BN/Graphene/BN structure allows a much higher mobility and carrier velocity than in the case of SiO_2 substrates and Al_2O_3 gate dielectrics. With the same device dimensions, the BN/Graphene/BN device shows a significant improvement in f_T compared to the control device, demonstrating its great potential for applications in high frequency electronic circuits. In addition, recent developments in the synthesis of both graphene [219] and hBN [57] by chemical vapor deposition (CVD) method may allow the technology proposed in this paper to be implemented at wafer-scale in the near future.
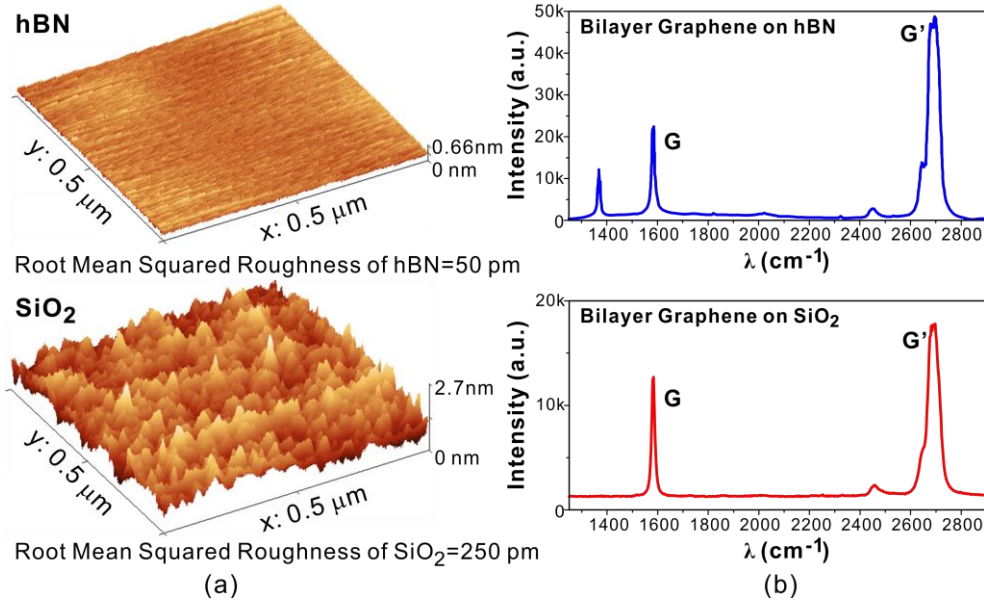
Figure 4-12 Comparison of hBN and 285 nm thermally grown SiO_2 (a) AFM images showing the surface roughness of hBN and 285 nm thermally grown SiO_2. (b) Raman spectra of bilayer graphene on hBN (the peak at $\lambda=1375$ cm^{-1} is due to hBN substrate); and bilayer graphene on SiO_2.
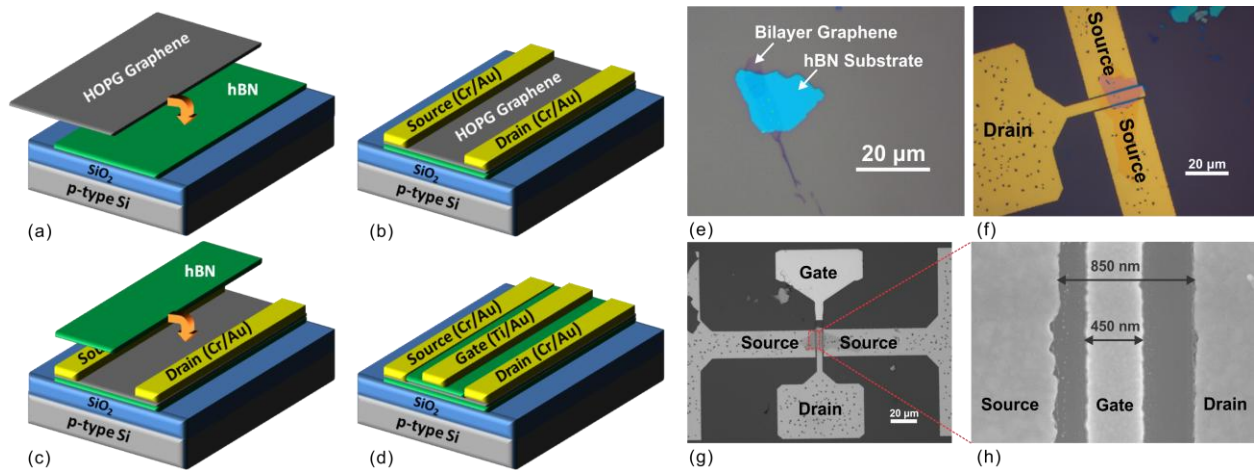
Figure 4-13 Fabrication of BN/Graphene/BN FETs (a)-(d) Fabrication process for making BN/Graphene/BN FETs. (e) optical micrograph showing a bilayer graphene flake exfoliated and transferred on top of hBN substrate. (f) optical micrograph of the device after source and drain are defined by e-beam lithography and the second (top) layer of hBN has been transferred on to graphene. (g) optical micrograph and (h) SEM image showing the final device. $L_G=450$ nm. $L_{DS}=850$ nm.
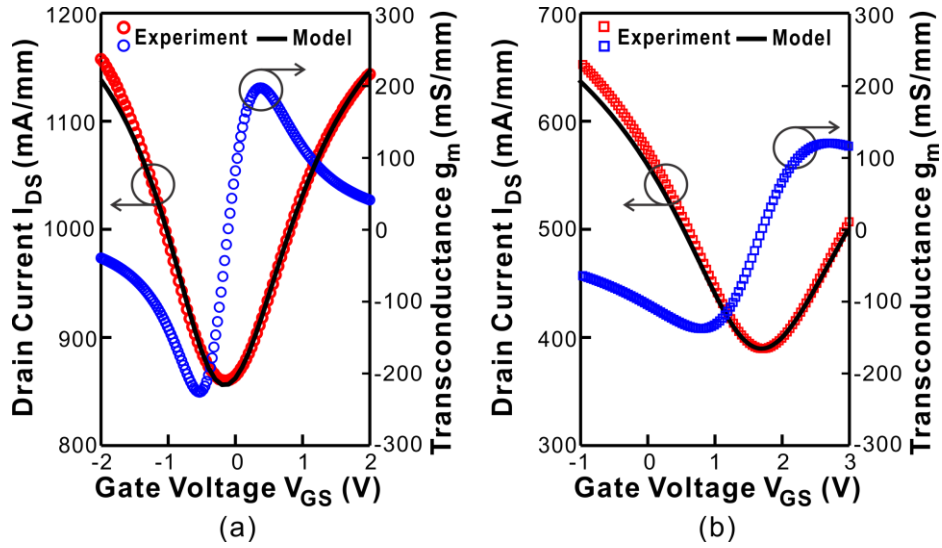
Figure 4-14 DC characteristics of the BN/Graphene/BN FETs. DC characteristics with the substrate grounded of (a) the BN/Graphene/BN device, and (b) the control device. V_{DS}=1 V in both devices. In both (a) and (b), the black solid lines show the fit by the model proposed in [207] to the device transfer characteristics.
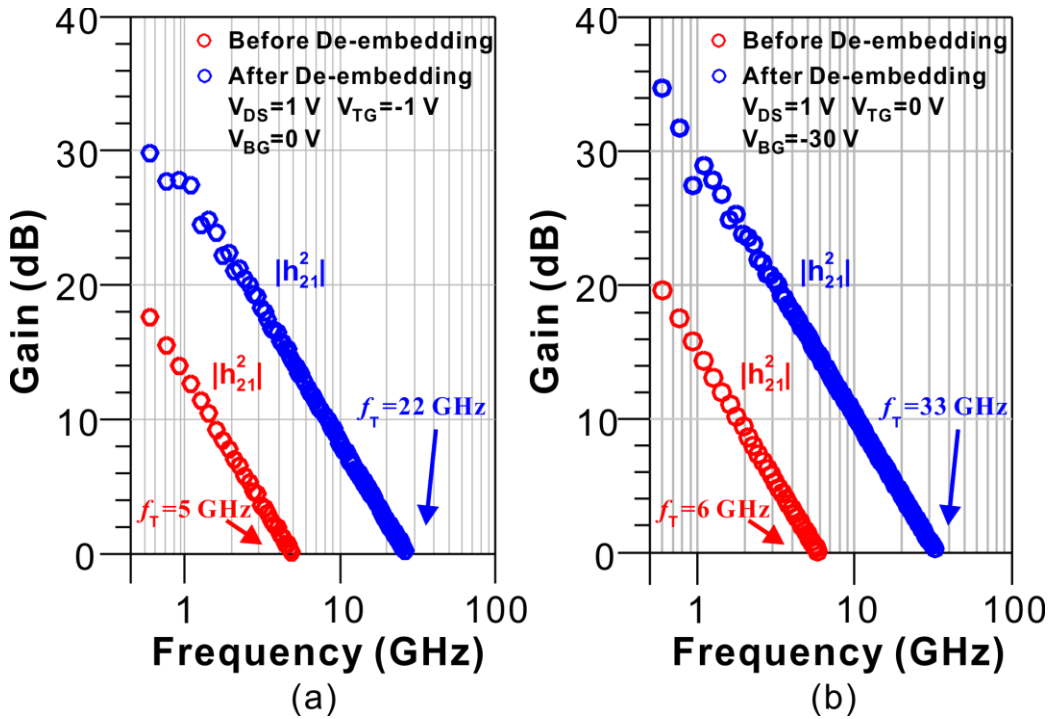
Figure 4-15 RF characteristics of the BN/Graphene/BN FETs. RF performance of the fabricated BN/Graphene/BN FET with L_G=450 nm when (a) the substrate is biased at V_{BG}=0 V, and (b) the substrate is biased at V_{BG}=-30 V. In both (a) and (b), the $|h_{21}{}^2|$ data and f_T before de-embedding are shown in red; and that after de-embedding are shown

in blue. V_{DS}=1 V. The top gate bias is V_{TG}=-1 V for (a) and V_{TG}=0 V for (b), such that the device is very close to the maximum g_m in each case.
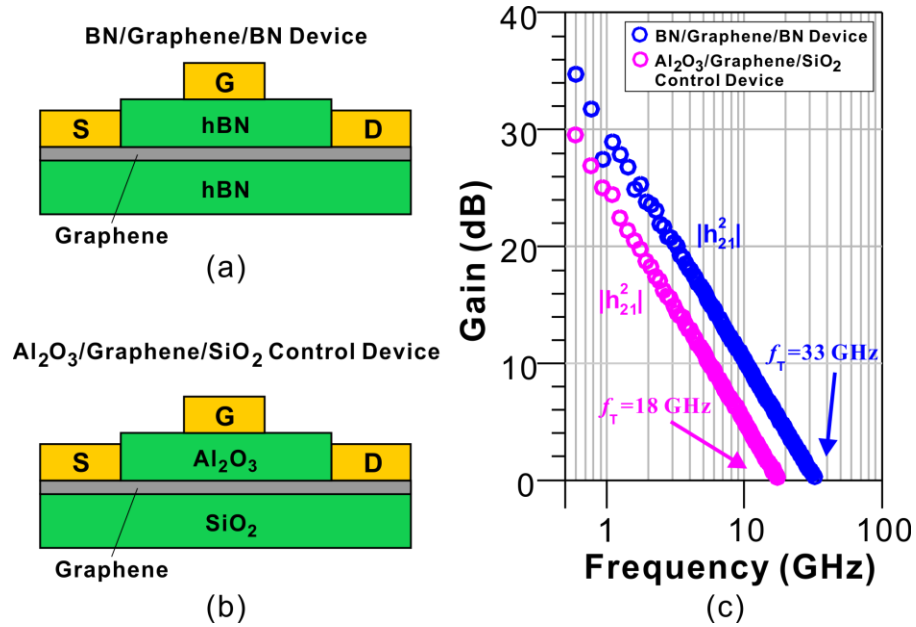
Figure 4-16 Comparison between the RF performance of hBN/Graphene/hBN device and the Al_2O_3/Graphene/SiO_2 control device. Both devices have gate length of 450 nm.

4.2.2. Sub-micrometer Graphene FETs on Sapphire Substrate and Delay Analysis

Besides extracting figures of merits such as f_T and maximum oscillation frequency (f_{max}), the high frequency performance of the GFETs can also be investigated by extracting its carrier transit delays and by understanding how the delay depends on the intrinsic and extrinsic properties of the device. Such analysis not only gives deep physical insight into the carrier transport in the channel, but also provides valuable information that can guide the device engineers in designing high performance RF GFETs. The contribution of this part of work is three-fold. First, GFETs are fabricated on an insulating substrate (sapphire) for the first time [220] to reduce the parasitics from the ground-signal-ground (GSG) probe pads. This minimizes the error in measuring the S-parameter of the device and allows small-signal capacitances to be accurately extracted. Second, we present for the first time a detailed delay analysis of high frequency graphene transistors. Lastly, the simple and robust method proposed can accurately extract the intrinsic transit delay of the GFETs - the delay purely associated with the carrier

transiting across the intrinsic gate region - and allows a new method for direct experimental extraction of the average carrier velocity in the channel. In addition, the individual contributions from the intrinsic, extrinsic and the parasitic elements to the total carrier transit delay can be estimated, which provides valuable information for optimizing the design of RF transistors.
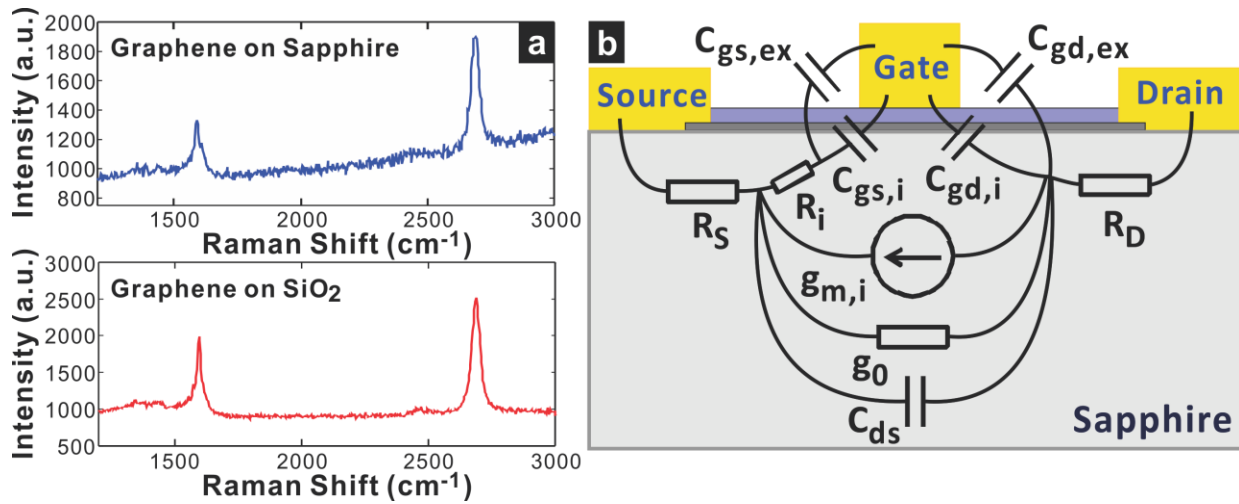
Figure 4-17 Graphene FETs on sapphire substrate (a) Raman spectra taken with a 532 nm Nd:YAG laser confirm the presence of single-layer graphene on sapphire. The Raman spectrum of graphene on SiO_2 is also shown for comparison. (b) Schematic of the GFET on sapphire with the small-signal equivalent circuit overlaid on top. R_S and R_D are the source and drain access resistances. R_i is the intrinsic resistance. $g_{m,i}$ is the intrinsic transconductance. $g_0 = 1/R_{ds}$ is the output conductance. C_{ds} is the source-drain capacitance. $C_{gs,i}$ and $C_{gd,i}$ are the internal gate-source and gate-drain capacitances. $C_{gs,ex}$ and $C_{gd,ex}$ are the external gate-source and gate-drain capacitances.

Graphene FETs on Sapphire Substrate

The proposed delay analysis relies on accurate two-port S-parameter measurements of the transistor, from which the small-signal capacitances between various electrodes of the active device can be extracted using small-signal equivalent circuit models. Unfortunately, for GFETs on a conductive substrate, such as doped silicon, the active device is embedded in the large parasitics of its GSG probe pads. The de-embedding process, hence, involves subtraction between two large numbers, which can lead to significant errors in the de-embedded S-parameters and a large ratio between these devices' f_T values before and after de-embedding

[120]. These errors in the de-embedded S-parameters will be carried over to the extraction of the capacitances and make delay analysis virtually impossible.

To reduce the GSG probe pad capacitances and improve the accuracy of the de-embedded S-parameter, we fabricate RF GFETs on a sapphire wafer (500 μm thick) with substrate resistivity above 10^{16} Ω.cm. For comparison, the resistivity of conductive Si is less than 1 Ω.cm and about 10^3 Ω.cm in high-resistivity Si. The highly resistive sapphire substrate can help eliminate most of the capacitances contributed by the coupling between the pad metals and the charge carriers in the substrate.

The graphene used in this work is grown by chemical vapor deposition (CVD) method on copper catalyst [57]. Films are then transferred to a sapphire substrate [57]. Single-layer graphene has been obtained, which uniformly covers more than 95% area of the sample. Figure 4-17(a) shows the Raman spectrum of single-layer graphene on sapphire substrate. The Raman spectrum of graphene-on-sapphire is almost identical to the Raman spectrum of graphene-on-SiO_2 except for a broad background fluorescence commonly found in sapphire due to trace impurities [221]. Room-temperature carrier mobilities were in the range of 2,234±95 cm^2/V.s (for a sheet charge density n_S= 6.0±0.4×10^{12} cm^{-2}) as measured through van der Pauw structures (B=0.3 T, I=0.1 mA). As reference, mobilities in graphene transferred on to 300 nm silicon dioxide are typically 2,220±174 cm^2/V.s (for a sheet charge density n_S= 5.5±0.6×10^{12} cm^{-2}). The ohmic contacts of the GFETs are first formed by depositing a 2.5 nm Ti/45 nm Pd/15 nm Au metal stack by e-beam evaporation using a pre-ohmic aluminum capping process [174]. The gate dielectric consists of 16 nm Al_2O_3 formed by naturally oxidizing e-beam evaporated Al and the top gate electrode is made of 60 nm-thick Al. The RF performance of the devices is measured with an N5230A Network Analyzer following short-open-load-through calibration and standard open-short de-embedding process [214]. The device with L_G=210 nm shows an f_T of 18 GHz before de-embedding and 22 GHz after de-embedding (

Figure 4-18(d)). The ratio is very close to unity, confirming that the GSG probe pad parasitics are small.

Figure 4-18(e) gives the measured (after de-embedding) and modeled S-parameters, showing excellent agreement.

Figure 4-18(f) shows the dependence of f_T on the intrinsic drain-source bias, $V'_{DS} = V_{DS} - I_{DS}(R_S + R_D)$. Since these GFETs operate in the linear regime, f_T increases with V'_{DS}, which leads to the increase in the drain current and hence higher intrinsic transconductance. This behavior is similar to conventional devices in their linear regime [222].
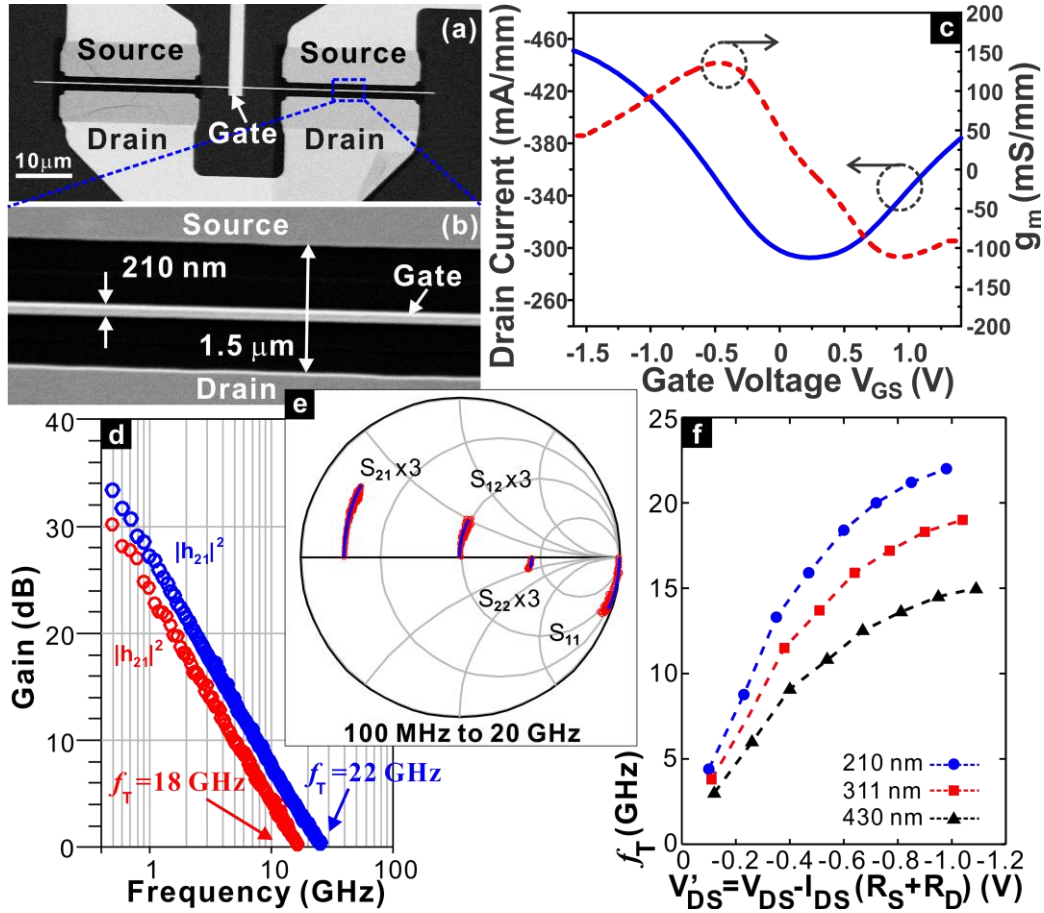
Figure 4-18 RF characteristics of graphene FETs on sapphire substrate (a) and (b) SEM images of a device with L_G=210 nm and L_{DS} =1.5 μm. (c) Transfer characteristics (I_{DS}-V_{GS}). (d) f_T of this device before (18 GHz, red circles) and after (22 GHz, blue circles) de-embedding the GSG probe pad parasitics. V_{DS}=-1.6 V. V_{GS}=-0.6 V. (e) The measured S-parameters after de-embedding (red dots) and the S-parameters predicted by the small-signal model (blue curves). (f) Dependence of f_T on drain bias with V_{GS} biased to optimum g_m. All measurements were performed in vacuum (1.4×10^{-4} Torr).

Extraction of Carrier Transit Delay in GFETs

There are several methods in the literature for extracting carrier transit delays [222]. Moll's method [222][223] is widely used for III-V HEMTs. However, the method is best used for devices operating in the saturation region, in which the dependence of the drain current on the source-drain bias is negligible. The method does not work well with graphene devices because the majority of the GFETs today operate in the linear regime. In addition, the absence of the drain depletion region in graphene transistors makes the concept of drain delay [222] irrelevant to GFETs. The method in ref. [223] requires cold-FET measurement. This is also not suitable for GFETs, which usually have a significant off-state current and never pinch off. Here, we use the method in [224][225] to extract the carrier transit delay. The f_T of a field-effect transistor is inversely proportional to the total delay (τ_{total}) of the device, which can be divided into three different components: the intrinsic delay (τ_{int}), the extrinsic delay (τ_{ext}), and the parasitic delay (τ_{par}):

$$\tau_{total} = \frac{1}{2\pi f_T} = \tau_{int} + \tau_{ext} + \tau_{par}$$

(4-27)

where τ_{int} is the time taken by the carrier to cross the intrinsic channel region (L_G); τ_{ext} is the additional delay associated with the external fringe capacitances and can be interpreted as the additional transit time due to the extended channel region (ΔL_G); and τ_{par} is the RC time constant required to charge and discharge the remaining parasitic part of the active device region. The f_T of a device is related to the small-signal circuit parameters as [213]:

$$f_T = \frac{g_{m,i}/(2 \cdot \pi)}{\left[C_{gs} + C_{gd} \right] \cdot \left[1 + \frac{R_S + R_D}{R_{ds}} \right] + C_{gd} \cdot g_{m,i} \cdot (R_S + R_D)}$$

(4-28)

Hence, the three components of the total delay are related to the small-signal circuit parameters (Figure 4-17(b)) as follows:

$$\tau_{\text{int}} = \frac{C_{\text{gs,i}} + C_{\text{gd,i}}}{g_{\text{m,i}}}$$

(4-29)

$$\tau_{\text{ext}} = \frac{C_{\text{gs,ex}} + C_{\text{gd,ex}}}{g_{\text{m,i}}}$$

(4-30)

$$\tau_{\text{par}} = C_{\text{gd}}(R_{\text{S}} + R_{\text{D}})\left[1 + \left(1 + \frac{C_{\text{gs}}}{C_{\text{gd}}}\right)\frac{g_0}{g_{\text{m,i}}}\right]$$

(4-31)

In this paper, we define the source of hole injection as the source for the GFETs. $C_{\text{gs,i}}$ and $C_{\text{gd,i}}$ are the internal capacitances. These are the components of C_{gs} and C_{gd} that directly scale with the gate length, while $C_{\text{gs,ex}}$ and $C_{\text{gd,ex}}$ are the external fringe capacitances, i.e. the components of C_{gs} and C_{gd} that do not change with the gate length. The small-signal capacitances C_{gs} and C_{gd} are first extracted from S-parameters. As shown in Figure 4-19(a), both the internal and external capacitances of the devices are then extracted from the scaling behavior of C_{gs} and C_{gd} for three GFETs with $L_{\text{G}} = 430$ nm, 311 nm and 210 nm. The effective lateral electric field in the channel $V_{\text{DS}}' = V_{\text{DS}} - I_{\text{DS}}(R_{\text{S}} + R_{\text{D}})$ and the intrinsic gate overdrive ($V_{\text{DS}}' = -1.0$ V, $V_{\text{GS}} = -0.6$ V for the 210 nm device) are kept the same in all three devices in order to achieve similar lateral and vertical electrostatic conditions in the channel for each device. The devices are within a few hundred μm from each other on the same sample and gate lengths are accurately measured by scanning electron microscopy (SEM). C_{gs} and C_{gd} have contributions from both the electrostatic capacitance of the gate dielectric and quantum capacitance of graphene. Unlike conventional devices operating in saturation regime where C_{gd} is much smaller and has a very weak dependence on the gate length due to minimum charge variation on the drain side in the saturation regime, the majority of the GFETs reported in the literature does not show current saturation and hence have C_{gd} that is a considerable fraction of C_{gs}. C_{gd} in GFETs also demonstrates significant dependence on gate length. This Miller capacitance can limit the bandwidth for amplifier applications.

Figure 4-19(b) shows that the intrinsic delay scales almost linearly with the gate length, as expected, while the extrinsic and parasitic delays both stay relatively constant as gate length changes. Hence, as the gate length reduces, the total delay in these GFETs becomes increasingly dominated by both the extrinsic and parasitic delays while the percentage of the intrinsic delay shrinks (Figure 4-19(c)). The increasing dominance of the parasitic delay in shorter channel GFETs as shown here agrees with Ref. [226], which shows that the access resistances play a key role in limiting f_T of short channel GFETs. Figure 4-19(c) shows that the extrinsic delay also becomes more significant in GFETs with shorter channels. Hence, to further improve f_T of RF GFETs, both τ_{par} and τ_{ext} need to be reduced. τ_{par} can be reduced by minimizing the source and drain access resistances, such as using a self-aligned device structure [120]. In addition, both τ_{par} and τ_{ext} can be reduced by optimizing the gate thickness and underlap to reduce fringe capacitances.

The intrinsic delay is directly related to the carrier velocity in the channel, which can be evaluated from the slope of the intrinsic delay dependence on L_G in Figure 4-19(b): $v_h = (\partial \tau_{int}/\partial L_G)^{-1} = 1.24 \times 10^7$ cm/s. While this velocity is extracted in the linear region of sample FETs, it is still much higher than saturation velocity in Si devices [227], demonstrating the great potential of graphene FETs. For a given lateral electric field in the channel, the carrier velocity in linear region is dependent on the carrier mobility. In GFETs, the mobility is mainly limited by the various scattering mechanisms, such as charge impurity scattering, optical phonon scattering, and ripple scattering. Hence, the intrinsic delay for GFETs operating in linear region can be reduced by biasing the channel at a higher lateral electric field to achieve a higher carrier velocity. For GFETs operating at a given bias condition in linear region or for operation in saturation region, the intrinsic delay can be reduced by improving the material quality and by using a better substrate such as boron nitride [87][228] to reduce scattering and improve carrier mobility and carrier velocity.

Figure 4-18(d) shows the cut-off frequencies for these devices. The measured cut-off frequencies $f_{T,meas}$ after de-embedding agree well with that calculated from the total delay $(1/2\pi\tau_{total})$. $f_{T,2}$ is the cut-off frequency if the access resistances are completely removed. $f_{T,1}$ is directly related to the carrier velocity in the intrinsic channel region and is generally hard to

reach in practical devices; but nevertheless, it highlights the great potential of these GFETs. Even with the moderate mobility in the CVD graphene used in this work, $f_{T,1}$ can reach 1 THz if the gate length can be reduced to 20 nm. This is a conservative estimate because the carrier transport may become ballistic at such gate length, which can further enhance the frequency performance.

L_G(nm)	210	311	430
$f_{T,1}=1/2\pi\tau_{int}$ (GHz)	107	80	56
$f_{T,2}=1/(2\pi\tau_{int}+2\pi\tau_{ext})$ (GHz)	40	38	31
$1/2\pi\tau_{total}$ (GHz)	23	22	19
$f_{T,meas}$ (GHz) after de-embedding	22	20	17
$f_{T,meas}$ (GHz) before de-embedding	18	17	15
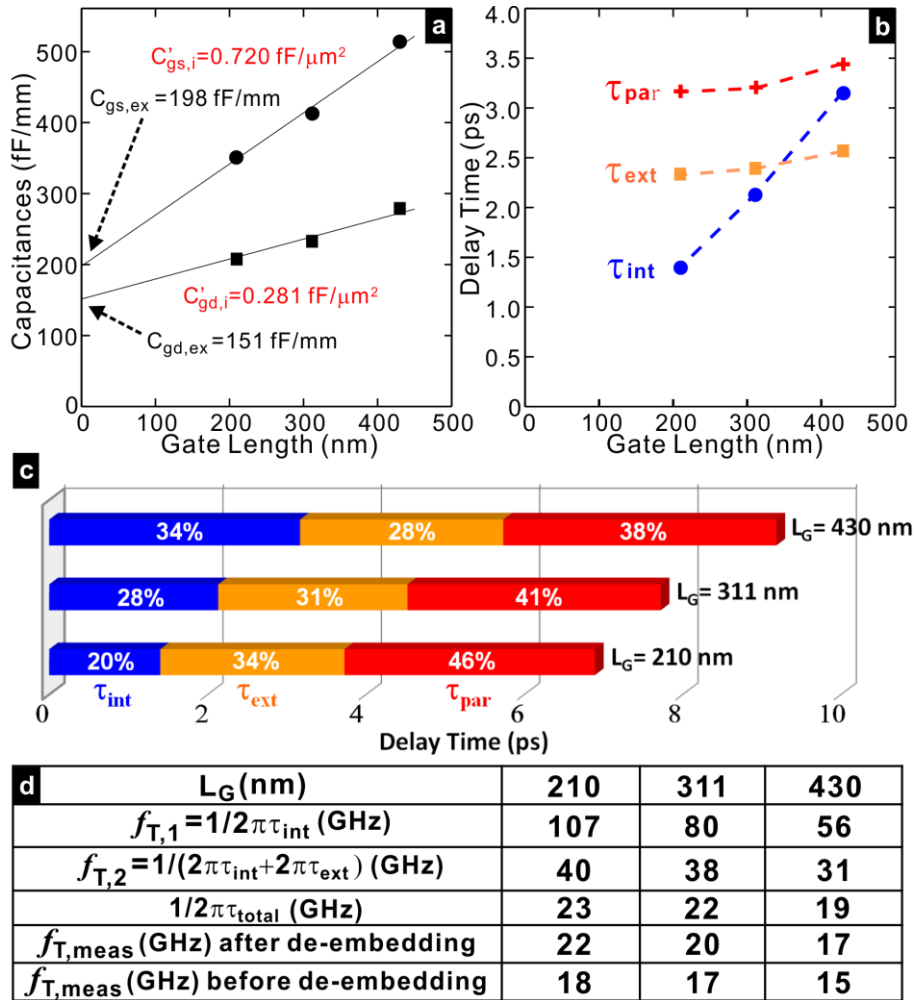
Figure 4-19 Delay analysis of the graphene FETs on sapphire substrate (a) Extraction of external gate capacitances ($C_{gs,ex}$, $C_{gd,ex}$) and internal gate capacitances ($C_{gs,i}$, $C_{gd,i}$) from the scaling behavior of C_{gs} and C_{gd}. The effective lateral electric field in the channel and the intrinsic gate overdrive $V_{GS} - I_{DS}R_S - V_{G,min}$ are kept the same for each device. (b) Intrinsic (τ_{int}), extrinsic (τ_{ext}) and parasitic delays (τ_{par}) v.s. gate length. (c) Percentage of each delay component in the total delay for each device. (d) frequency performance.

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In summary, in this section, a method for extracting the carrier transit delays in RF transistors is applied to GFETs on sapphire with sub-micrometer gate length. The extraction of intrinsic delay offers a new way to estimate the carrier velocity in the channel. By breaking down the total delay into individual components associated with intrinsic carrier velocity, fringe capacitances, and access region parasitics, this method provides insightful information for device optimization. These three delay components can also serve as figures of merit for comparing the quality of RF GFETs in terms of both the intrinsic material transport property (by using τ_{int}) and the design and quality of the external device structure (by using τ_{par} and τ_{ext}).

4.2.3. Self-aligned Graphene FETs

The results from delay analysis of graphene transistors indicate that the intrinsic delay becomes less significant as a percentage of the total delay, particularly in short channel GFETs, while the parasitic delay and extrinsic delay dominate the carrier transit time. To reduce the total delay and improve the f_T of short channel GFETs, the parasitic delay may be greatly reduced by adopting a self-aligned structure.
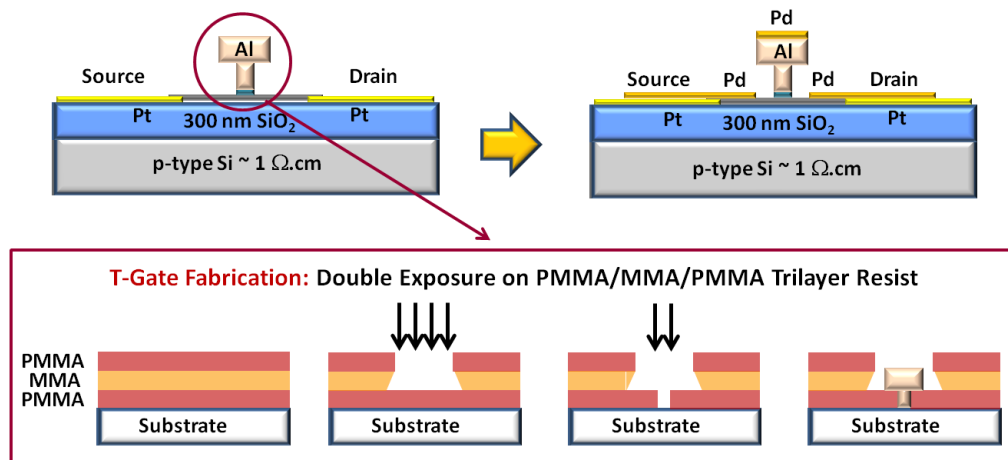
Figure 4-20 The fabrication process for creating T-gate self-aligned graphene FETs. The T-shape gate is created using a tri-layer resist double exposure method.

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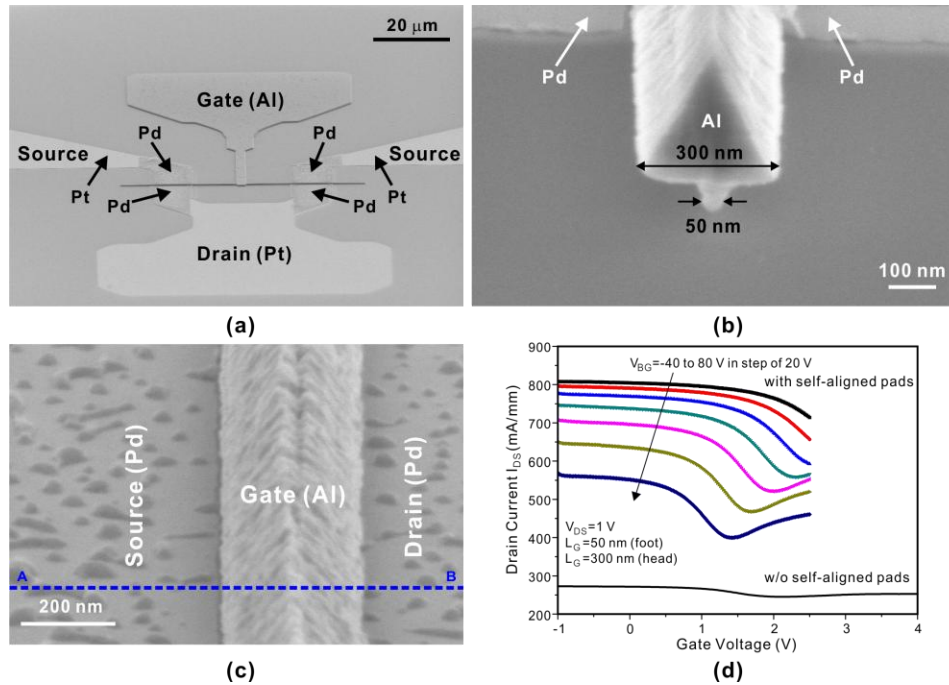
Figure 4-21 T-gate self-aligned device technology. SEM images of (a) the device. (b) the T-shape gate with 300 nm head and 50 nm foot. (c) Pd metallization self-aligned to the edge of the gate. (d) DC performance of the device with and without the final Pd metallization.

Figure 4-20 shows the process for fabricating self-aligned graphene FETs using T-gate as the mask. The fabrication process starts from CVD graphene transferred onto any arbitrary insulating substrate. After making the source/drain contacts and the gate dielectric, a T-shape gate is fabricated using a tri-layer resist double exposure method. Here, the e-beam lithography process uses a PMMA (200 nm)/MMA (400 nm)/PMMA (200 nm) tri-layer resist stack (Figure 4-20). The first e-beam exposure defines the gate head while the second exposure defines the foot region of the gate. The following recipe is used to create the T-shape resist profile using Raith150 30 keV electron-beam lithography system.

For the head write:

- EHT= 30kV

- Aperture size= 20 μm

- Step size= 6 nm

- Area dose=125 μAs/cm^2

The sample is developed for 60s in MIBK followed by developing for 20s in methanol:isopropanol = 1:1 and quenching for 60s in isopropanol.

For the foot write:

- EHT= 30kV

- Aperture size= 120 μm

- Step size= 4 nm

- Area dose=225 μAs/cm^2

The sample is developed for 90s in MIBK:isopropanol=1:3 followed by quenching for 60s in isopropanol.

It is then followed by metallization and liftoff where the T-gate is formed with Al metal. Once we have the T-gate, Pd metal is deposited everywhere in the active device region. The T-gate acts as the mask in this final metallization step where the Pd metal will stop right at the edge of the T-gate to form the self-aligned structure. With this process, we can create device structures where the access resistance of the transistor can be significantly reduced. In addition, the T-shape gate is also an ideal gate structure for high frequency transistor application since it allows a lower gate resistance to be achieved due to the increased cross-sectional area while still keeping the channel length of the device small for high speed carrier transition.

Figure 4-21(a) shows the scanning electron microscopy (SEM) image of one transistor from the first batch of devices. Figure 4-21(b) shows the fabricated T-shape metal (Al) gate with a 300 nm head and 50 nm foot. Figure 4-21(c) shows the top-view of the device where it is clear that the final Pd metallization of the source and the drain is aligned exactly to the edge of the T-gate. Figure 4-21(d) shows the DC measurements of the self-aligned GFET. The final Pd metallization, which reduces the source-drain separation from 3 μm to 300 nm, leads to a 4-5 times improvement in the transconductance of the device due to significant reduction in the access resistances. Figure 4-22 compares the current gain of the T-shape gate device with and without self-aligned structure. The self-aligned device offers f_T that almost doubles that in the non-self-aligned device extracted using both the standard and "intrinsic" de-embedding methods.
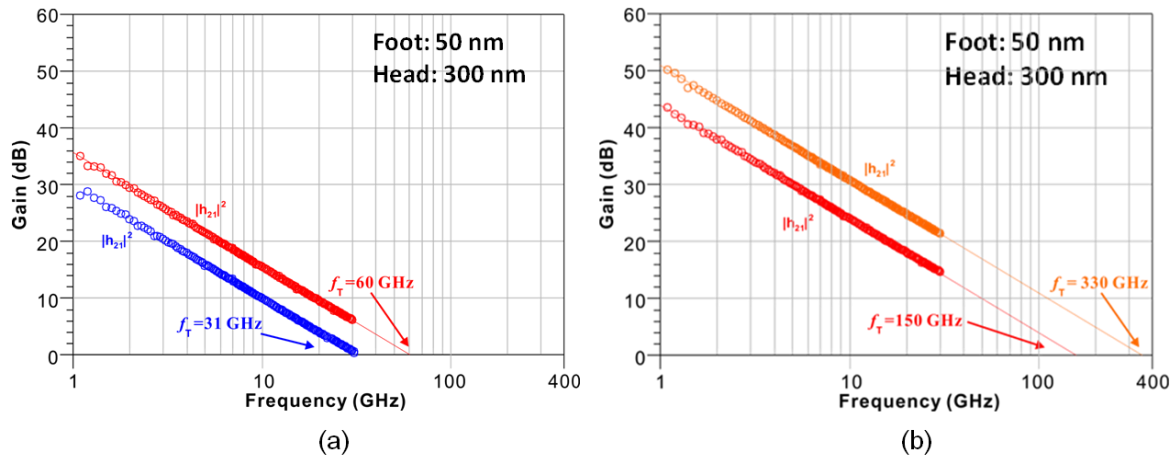
Figure 4-22 RF characteristics of GFETs with and without self-aligned structure (a) RF characteristics of GFETs with and without self-aligned structure extracted with the standard de-embedding method (b) RF characteristics of GFETs with and without self-aligned structure extracted with the "intrinsic" de-embedding method. The standard and "intrinsic" de-embedding methods are illustrated in Figure 4-10 and explained in details in Section 4.3. Both the self-aligned and non-self-aligned devices have T-gate with 300 nm gate head and 50 nm gate foot.

The carrier transit delay analysis is also performed on these self-aligned T-gate devices. Figure 4-23 compares the τ_{int}, τ_{ext}, and τ_{par} for these devices with the non-self-aligned devices previously shown in Figure 4-19. Clearly, the intrinsic delay continues to scale down linearly as the gate length reduces. There is a drastic change in the parasitic delay due to the reduction of access resistances. Although the overall parasitic delay has been greatly reduced in the self-aligned device, the extrinsic delay and parasitic delay are still the key limit for the device performance due to the scaling down of the gate length to 50 nm range.
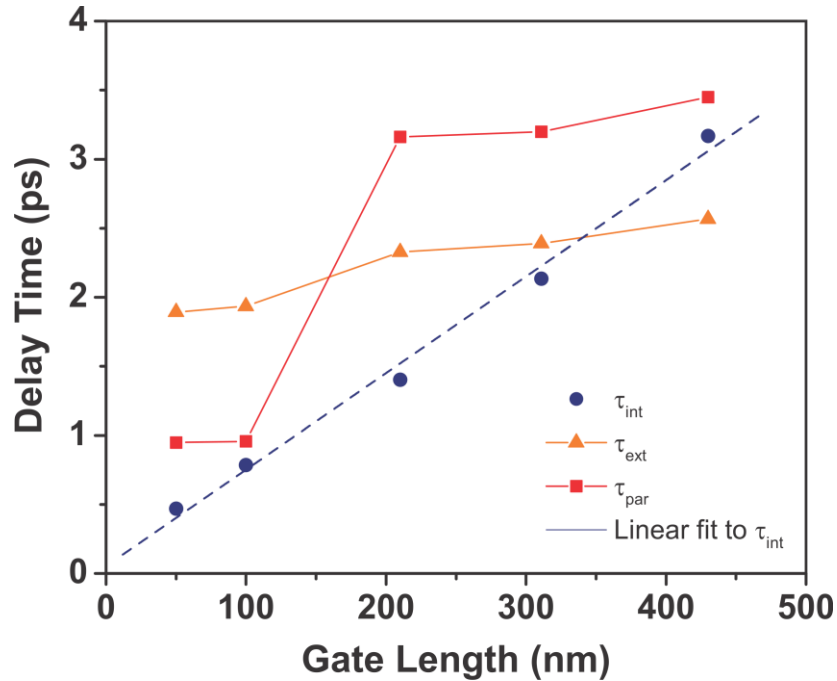
Figure 4-23 Delay time versus device channel length for self-aligned and non-self-aligned devices.

4.3 About the De-embedding Methods

The de-embedding process can affect the accuracy of RF characterization to a great extent. The open-short de-embedding technique is often used in the literature when reporting the f_T and f_{max} values of graphene FETs. However, most reports do not give the detailed design of the open and short test structures. In this section, we compare two different possible designs of the open and short test structures and illustrate the significant difference it can cause when reporting f_T values. The underlying cause for the discrepancies is studied in detail in term of carrier transit delays.

As already introduced in Section 4.1.2, the standard "open" patterns for the open-short de-embedding has the gate electrode ending outside the active device region (Figure 4-9). This design is in-line with the standard industrial method for characterizing high frequency Si MOSFETs and III-V HEMTs [214][215][216]. All RF characterization results presented in this Chapter so far were extracted using this design of "open" pad. Figure 4-25 compares f_T extracted using this method for graphene FETs with Si MOSFETs and III-V devices. The mobility of graphene available today is comparable or higher than in Si but lower than in some III-V materials. It is estimated that f_T of high quality graphene devices may exceed 1 THz at gate length around 50 nm. However, comparing the III-V and Si device technology, graphene devices

are still in their early stage of development and some of the reported f_T values may be subject to extraction errors from measurement and de-embedding steps.
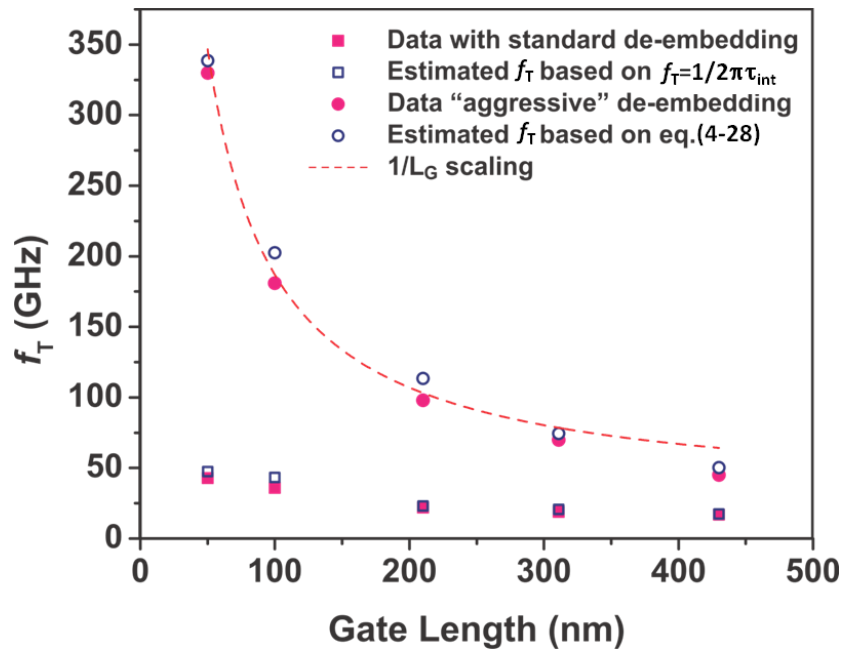
Figure 4-24 The scaling behavior of f_T for graphene transistors with gate length from 430 nm to 50 nm. The solid pink dots and squares show the values extracted using the standard and the more "intrinsic" methods, respectively, as introduced in Section 4.1.2. The blue circles and empty squares show the estimated f_T using $f_T = 1/2\pi\tau_{int}$ and eq. (4-28), respectively.
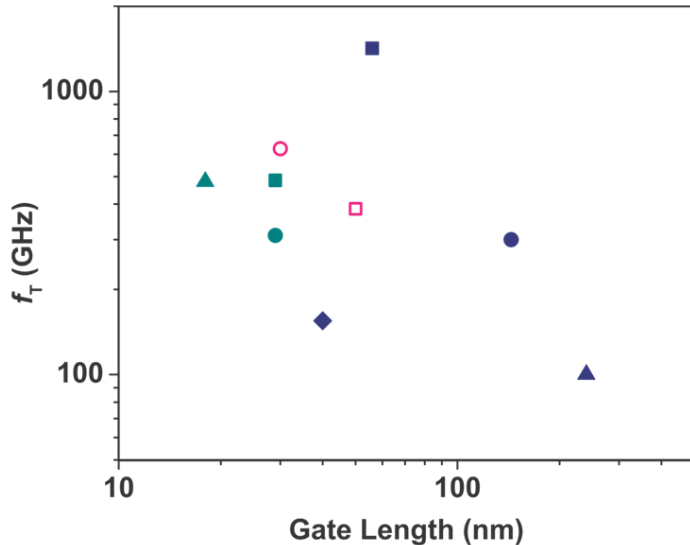
Figure 4-25 Comparison of mobility and RF performance of graphene devices with III-V and Si transistors [119][229][230][231][232][233][234]. Comparing the III-V and Si device technology, graphene devices are still in

their early stage of development and some of the reported f_T values may be subject to extraction errors from measurement and de-embedding steps.
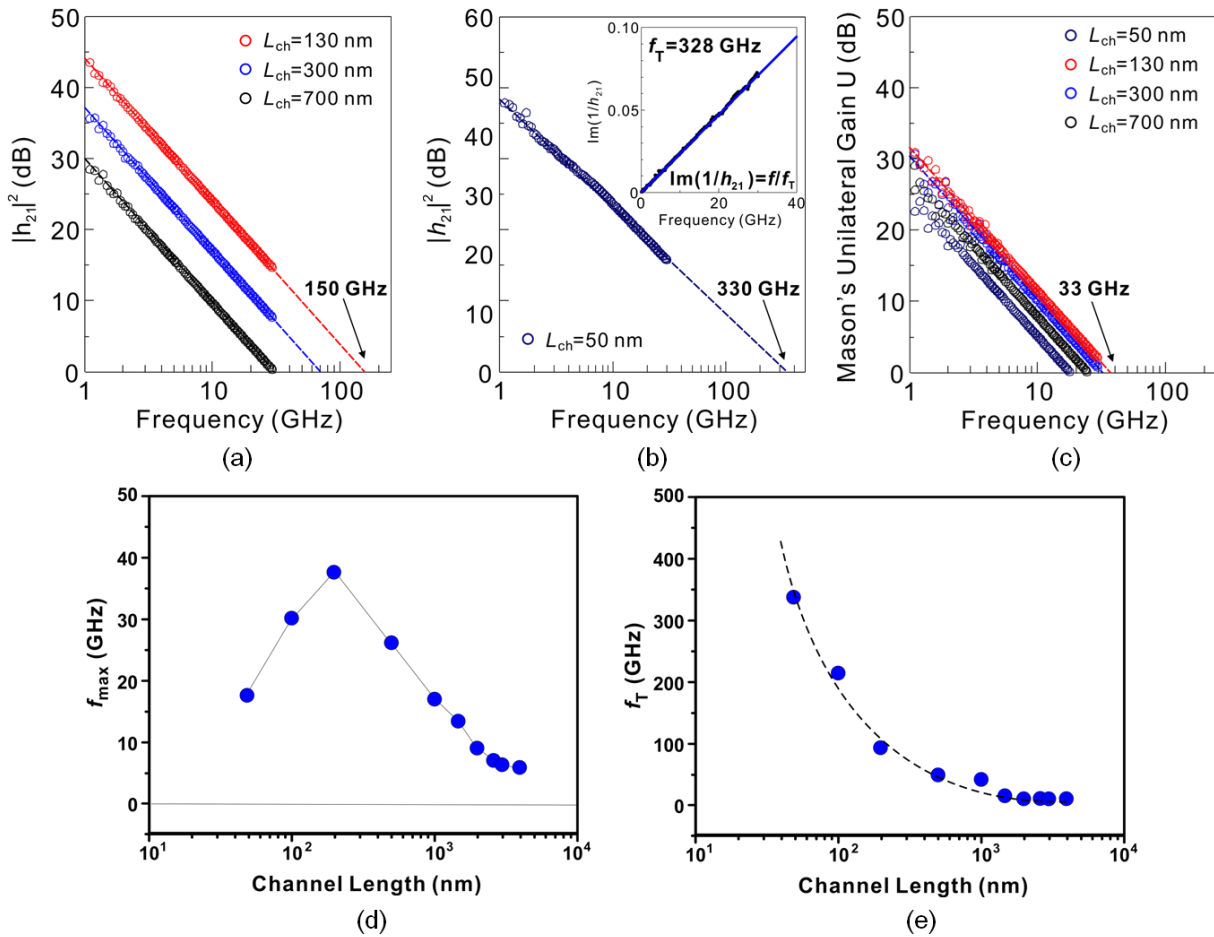
Figure 4-26 RF performance of graphene transistors extracted using the "intrinsic" de-embedding method (a) Short-circuit current gain h_{21} for graphene transistors with gate length 130 nm, 300 nm and 700 nm. (b) Short-circuit current gain h_{21} for graphene transistors with gate length 50 nm. f_T value is extracted using both the unity current gain criteria and Gummel's method [235].

There is another design of "open" pad that may be used to eliminate a large portion of the fringe capacitances that is beneficial for studying the more intrinsic performance of graphene FETs. Figure 4-10 shows the pad design for this more "intrinsic" de-embedding method. The key difference lies with the fact that the "open" pattern in this method has the gate electrode extending into the active device region while that in the standard de-embedding method does not. Although the graphene channel was etched in the "open" pattern, the de-embedding process using "open" pattern designed in this manner will remove almost all the parasitic contributions

from the fringe capacitances of the device. In terms of parameters defined in the carrier transit delay analysis in Section 4.2.2, it means that the effects of the extrinsic capacitances components $C_{gs,ext}$ and $C_{gd,par}$ will be mostly excluded and the resulting value of f_T is almost entirely due to the intrinsic delay. Figure 4-24 compares the f_T values extracted using the standard (pink solid circles) and "intrinsic" (pink solid squares) de-embedding methods. We can see that the f_T values measured with the standard de-embedding patterns are matched closely to the values estimated from eq. (4-28) (blue squares), which accounts for all the effects of intrinsic, extrinsic and parasitic delays. On the other hand, the f_T values measured using the "intrinsic" de-embedding method agree well with the values estimated using $f_T = 1/2\pi\tau_{int}$ (blue circles), which only accounts for the intrinsic delay of the device. Clearly, the f_T values extracted using the standard de-embedding and the values predicted by eq. (4-28) do not scale very well as the gate length reduces. This is because the external and parasitic delays due to fringes capacitances and the access resistances dominate the device performance and the effects of reducing the intrinsic delay by shrinking the gate length only leads to relatively small improvements in f_T of the devices. The f_T values increase from 17 GHz at L_G=413 nm to 47 GHz at L_G=50 nm. On the other hand, the intrinsic performance of the device scales very well with the $1/L_G$ curve fitted using a red dotted line in Figure 4-24. The strong gate length dependence comes from the fact that the f_T values extracted with the "intrinsic" de-embedding method and the f_T values estimated from $f_T = 1/2\pi\tau_{int}$ both excluded the effect of extrinsic and parasitic delay. The remaining intrinsic delay of the device reduces linearly with the gate length, leading to the inverse relation between f_T and the channel length of the device. The intrinsic f_T of the device increases from about 50 GHz at L_G=413 nm to 330 GHz for the 50 nm channel length device. Figure 4-26 shows the current gain and unilateral power gain of four short channel devices, characterizing its f_T and f_{max} as well as the scaling trend. From Figure 4-24, we can see that the intrinsic performance of the graphene FETs reaches above 300 GHz at gate length of 50 nm. If the scaling trend continues, it can reach 500 GHz performance at 20-30 nm gate length and THz device are possible at gate length close to 10 nm. On the other hand, the extrinsic device performance scaling is hindered by the parasitics of the devices. Further gate length scaling without proportionally reducing the access resistances and fringe capacitances will only lead to minimum additional improvements in f_T.

Chapter 5. Graphene Ambipolar Electronics

5.1. The Ambipolar Electronics Concept

The unique ambipolar transport properties of graphene provide new opportunities for radio frequency (RF) and mixed-signal applications. Unlike in conventional unipolar devices such as silicon MOSFETs whose majority carrier type in the channel is determined by the doping in the channel and cannot be changed once the device is fabricated, ambipolar devices can be switched between p-type and n-type conductions by controlling the position of the Fermi level using the gate bias. Ambipolar conduction in graphene devices has been illustrated in previous chapters. If the gate voltage V_{GS} is well below the minimum conduction point, the Fermi level in graphene is below its charge neutrality level and the conduction in the channel will be by holes. On the other hand, if V_{GS} is well above the minimum conduction point, the Fermi level in graphene is above its charge neutrality level and the conduction in the channel will be by electrons. In addition, the region at the proximity of the minimum conduction point is also called the ambipolar conduction region. In this operating region, electron and hole carriers are injected from the source and the drain respectively (assuming $V_{DS}>0$), both as majority carriers, and recombine inside the channel region.

For a long time, this ambipolar behavior of transistors based on graphene, carbon nanotube [236][237] and other ambipolar materials, such as amorphous silicon [238], organic semiconductor heterostructures [239], is considered undesirable for device operation and several techniques have been developed to suppress the ambipolar conduction [240][241]. However, I believe this property may be one of the most important strength of graphene if used in the right way. During the time span of this thesis work, I proposed for the first time a family of completely novel applications based on the ambipolar conduction properties of graphene for RF and mixed signal circuits, which are impossible to realize in traditional unipolar devices, such as silicon MOSFETs.

5.2. Graphene Frequency Multipliers

The first application I propose here is a frequency multiplier [5][242]. A graphene frequency multiplier relies on the ambipolar transport property and the highly symmetric transfer

characteristics of graphene devices to achieve excellent spectral purity at the output for frequency doubling. The frequency multiplier can be demonstrated by using the circuit shown in **Figure 5-1**(a). Under the test conditions, the gate of the GFET is biased at its minimum conduction point. As a sinusoidal signal is superimposed to the DC bias at the gate electrode, it modulates the conductivity in the channel. Due to the inductor in the bias-tee, the current through the device remains stable while the drain voltage swings in response to the change in channel conductivity. The principle of ambipolar frequency doubling is illustrated in Figure 5-1(a). Points A to E in Figure 5-1(a) are the corresponding input and output signal levels for an ambipolar frequency doubler. When the input signal swings from point A to C through B, the GFET has holes in the channel; and as the input signal swings from point C to E through D, the GFET conductivity is dominated by electrons. It is clear from **Figure 5-1**(a) that each half-cycle swing of the input signal leads to a full-cycle swing in the output signal, hence achieving frequency doubling.
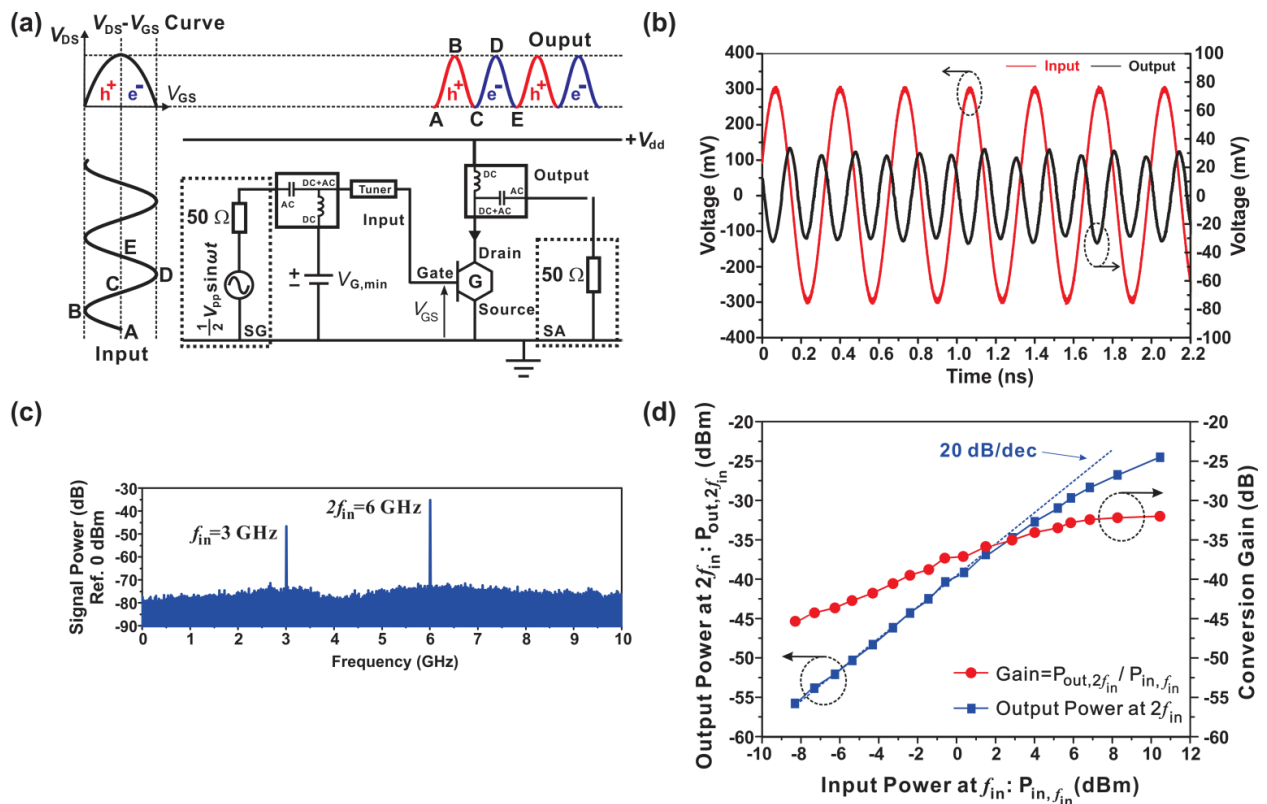
Figure 5-1 Graphene ambipolar frequency multipliers (a) Principles of ambipolar frequency doubling and schematic of the measurement circuit for the demonstration of graphene frequency multipliers. The inductor in the bias-tee at the drain isolates the DC power supply $+V_S$ from the RF power at the drain by keeping the supply current relatively constant. The capacitor in the bias-tee blocks the DC voltage component at the drain and only allows RF power to be

transmitted to the measurement equipment, which is either an oscilloscope or a spectrum analyzer. (b) Experimental demonstration of frequency doubling measured by an Agilent DSA90604A oscilloscope. The input is at 3 GHz. The output fundamental frequency is 6 GHz. DC bias: V_{DS}=2 V. The gate is biased at V_{GS}=1.33 V, slightly above the minimum conduction point (1.3 V), to compensate for the small asymmetry in the transfer characteristics and, hence, to improve the symmetry between the electron and hole conduction at the output. (c) Power spectrum of the output signal from the graphene frequency multipliers measured by an Agilent N9010A spectrum analyzer. The input is at 3 GHz. Frequency doubling is clearly visible. The signal power at frequency component $f_{out}=2f_{in}$=6 GHz is about 10 dB higher than the signal power at frequency component $f_{out}=f_{in}$=3 GHz without any filtering. (d) Output power at the doubled frequency component $f_{out}=2f_{in}$ is plotted against the input power that has a frequency of f_{in}. The output power at $2f_{in}$ increases with the input power with a slope of 2 when plotted on a logarithmic scale. Conversion Gain=$P_{out,2f_{in}}/P_{in,f_{in}}$ increases with input power up to 2 dBm.

High Performance Gigahertz Ambipolar Frequency Multipliers

To demonstrate the idea illustrated above, we use graphene devices fabricated on sapphire substrate to minimize parasitic capacitances for best high frequency performance. The graphene used in this work is grown by chemical vapor deposition (CVD) on copper catalyst. Single-layer graphene films were first grown by CVD method on copper foils [56][57] and then transferred to a sapphire substrate. More details of the device fabrication process is given in Chapter 2. The device fabrication process and basic device characterization of graphene on sapphire FETs have been discussed in Chapter 3 and 4.

Figure 5-2(a) and Figure 5-2(b) show the scanning electron microscopy (SEM) images of a device with a gate length L_G=300 nm and a drain-to-source distance L_{DS}=1.5 μm. Figure 5-2(c) shows its transfer characteristic, which has a minimum conduction point at 1.3 V. The peak transconductance for hole and electron conductions are 160 mS/mm and 140 mS/mm respectively. Figure 5-2(d) shows the drain-source voltage (V_{DS}) as a function of the gate voltage (V_{GS}) for the device. The V_{DS}-V_{GS} characteristic is measured by driving a constant current density of 250 mA/mm through the device using a current source, and then measuring the drain voltage as a function of the gate voltage. Figure 5-2(d) shows that the device has a large-signal voltage gain of about 0.2 for low-frequency voltage swings around the minimum conduction point. In this device, the current-gain cut-off frequency, f_T, is 24 GHz before de-embedding and 28 GHz after de-embedding (Figure 5-2(e)). The de-embedding ratio is about 1.2. Comparing the

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electron and hole branches, the peak current gain cut-off frequency without de-embedding measurement pad effects is $f_{T,hole} = 24$ GHz for hole conduction and $f_{T,electron} = 20$ GHz for electron conduction (Figure 5-2(f)). As it will be described in the next section, both hole and electron transport are important for frequency doubling applications since the conduction in these devices needs to alternate between electron and hole half cycles. The frequency performance will be limited by the slower of the two conduction modes.
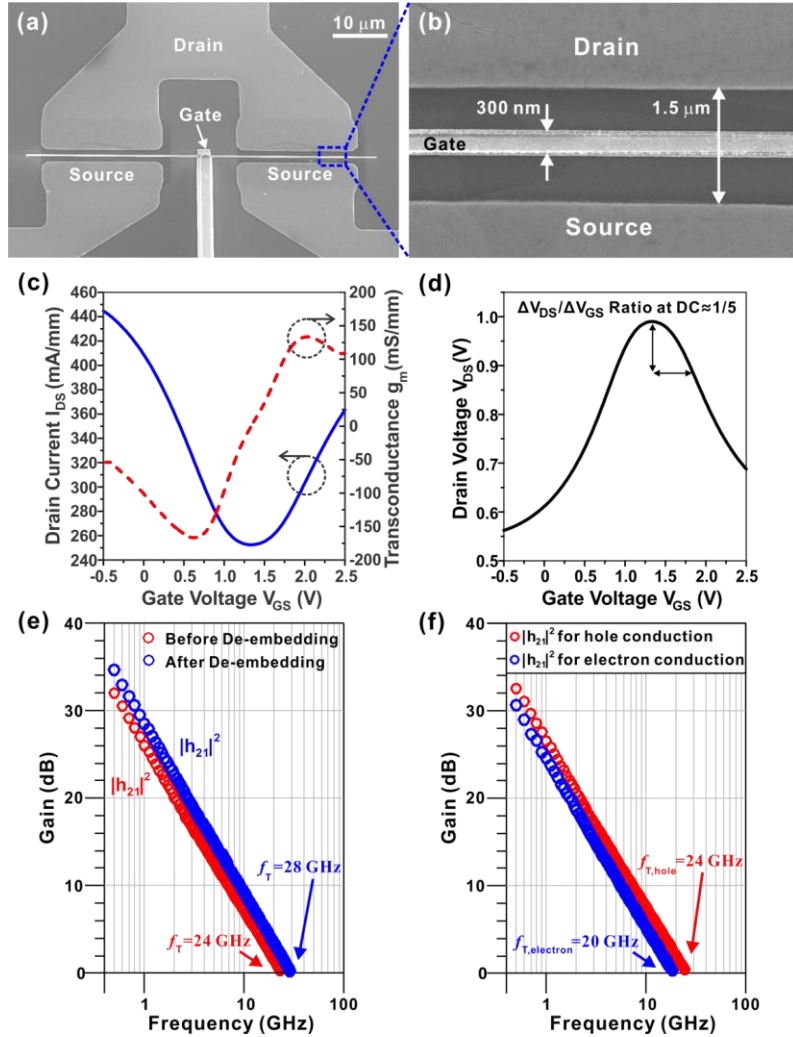
Figure 5-2 Graphene transistors on sapphire substrate (a) and (b) SEM images of a device with L_G=300 nm and L_{DS}=1.5 μm. This device is used for the frequency multiplier demonstration. (c) Transfer characteristics (I_{DS}-V_{GS}) of the device. (d) V_{DS}-V_{GS} characteristic of the device measured by keeping I_{DS} at a constant value of 250 mA/mm. (e) Peak current gain cut-off frequency f_T of the device before (f_T=24 GHz) and after (f_T=28 GHz) de-embedding the measurement pad parasitics. V_{DS}=2 V. V_{GS}=0.5 V. (f) Peak current gain cut-off frequency f_T (before de-embedding

the measurement pad parasitics) for both the electron and hole branches of the device. For the electron branch, $f_{T,electron}$=20 GHz; and for the hole branch, $f_{T,hole}$=24 GHz. The lower of $f_{T,electron}$ and $f_{T,hole}$ limits the frequency doubling performance of the device.

For reference, Figure 5-3 compares the f_T value before and after de-embedding for the state-of-the-art graphene transistors published in the literature [119][120][243][174][169][117][118], as well as the 90 nm SOI CMOS technology [244]. Firstly, the device with L_G=300 nm demonstrated in this work shows the highest before-de-embedding f_T values reported so far. In addition, the devices on sapphire substrate show a very low de-embedding ratio compared to other devices in the literature, mainly due to a highly insulating sapphire substrate that eliminates most of the measurement pad capacitances and minimizes de-embedding errors.
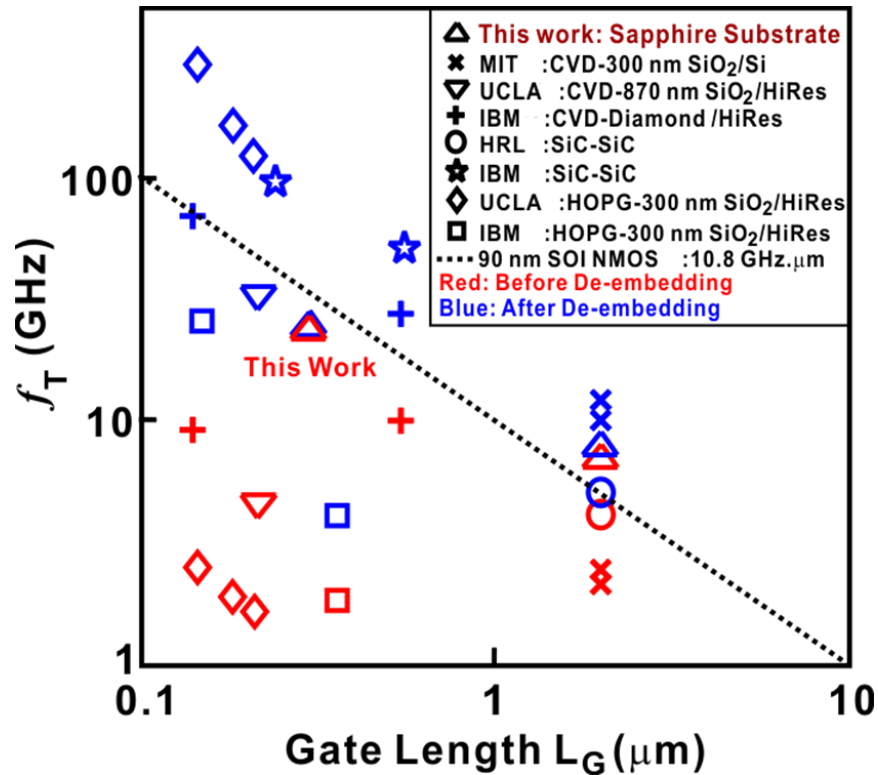
Figure 5-3 Comparison of current gain cut-off frequency f_T before and after de-embedding measurement pad capacitances for the devices fabricated in this work and other devices reported in the literature [174][120][243][118][119][120][117]. The variation in de-embedding ratios amongst various groups is dependent on measurement pad layout, substrate parameters, and device geometry.

The graphene-on-sapphire FETs (L_G=300 nm) with high extrinsic frequency performance allow the demonstration of graphene non-linear analog circuits, such as frequency multipliers, well in

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the GHz frequency range. A graphene frequency multiplier relies on the ambipolar transport property and highly symmetric transfer characteristics of graphene devices to achieve excellent spectral purity at the output for frequency doubling [5]. When the gate of the graphene device is biased at the minimum conduction point and a sinusoidal signal is applied, the device will have electron conduction in the channel for positive gate voltage swings; and hole conduction in the channel for negative gate voltage swings. Hence, the output signal at the drain conducts in alternating half cycles of electron and hole transport and has a fundamental frequency that is twice the input frequency.

Here, we test the frequency multiplier concept by using the circuit shown in Figure 5-1(a). Low-loss bias-tees are used both at the input and the output to combine DC and RF signals, and provide isolation between them. Tuners are used at the input to provide adequate impedance matching. Under the test conditions, the gate of the GFET is biased at its minimum conduction point. As a sinusoidal signal is superimposed to the DC bias at the gate, it modulates the conductivity in the channel. Due to the inductor in the bias-tee, the current through the device remains stable while the drain voltage swings in response to the change in channel conductivity. The principle of ambipolar frequency doubling is also illustrated in Figure 5-1(a). Points A to E in Figure 5-1(a) are the corresponding input and output signal levels for an ambipolar frequency doubler. When the input signal swings from point A to C through B, the GFET has hole conduction in the channel; and as the input signal swings from point C to E through D, the GFET has electron conduction in the channel. It is clear from Figure 5-1(a) that each half-cycle swing of the input signal leads to a full-cycle swing in the output signal, hence achieving frequency doubling.

We can also derive the ambipolar frequency doubling operation in a more general form. Assuming a relatively stable current I_{dd} from the DC power supply, we have:

$$V_{DS} \approx I_{dd} R_{DS} = I_{dd} f(V_{GS})$$

(5-1)

where R_{DS} is the total resistance from drain to source. R_{DS} is a function of the gate-to-source voltage V_{GS} related through the transfer characteristic of the device. The constant current

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assumption is valid because we measure the circuit performance well within the rated frequency range of the bias-tees (100k Hz-18 GHz). Within its rated frequency range, the bias-tee should provide at least 30 dB isolation between the drain and the DC supply. It does so by keeping the current from the DC power supply stable using an inductor.

If we assume that the transfer characteristics of an FET is infinitely differentiable, we can use Taylor expansion about the DC bias point to describe the drain voltage as:

$$V_{DS} = I_{dd}f(V_{GS}) = a_0 + a_1(V_{GS} - V_B) + a_2(V_{GS} - V_B)^2 + a_3(V_{GS} - V_B)^3 + \cdots$$

(5-2)

where V_B is the DC bias applied to the gate. $a_0, a_1, a_2, a_3, \ldots$ are constants whose values are determined by their respective polynomial components in the transfer characteristics of the specific device (and scaled by I_{dd}). If we apply a sinusoidal input with peak-to-peak swing of V_{pp} superimposed on a DC bias voltage $V_B = V_{G,min}$, i.e.

$$V_{in} = V_B + \frac{1}{2}V_{pp}\sin\omega t$$

(5-3)

The drain voltage at the output can be described by substituting eq. (5-3) into eq. (5-2), and we have:

$$V_{DS} = a_0 + a_1\frac{1}{2}V_{pp}\sin\omega t + a_2\left(\frac{1}{2}V_{pp}\sin\omega t\right)^2 + a_3\left(\frac{1}{2}V_{pp}\sin\omega t\right)^3 + \cdots$$

(5-4)

Eq. (5-4) can be used to describe the various analog operation modes of GFET devices. The linear term $a_1\frac{1}{2}V_{pp}\sin\omega t$ is the only component that generates an output signal at the same frequency as the input, and hence is critical for amplifier applications. In fact, the coefficient a_1 is directly related to the transconductance of the device and V_B should be at the maximum value of a_1 to achieve good signal amplification. The quadratic term, on the other hand, is crucial for both frequency doubling and mixer applications. For mixer applications, two RF input signals are applied to the gate and the quadratic term generates the sum and difference frequencies at the

output [6], such devices have important applications in almost all communication systems. Here, we focus on a single RF input and frequency doubling, where the quadratic term expands to $a_2 \left(\frac{1}{2} V_{\text{pp}} \sin\omega t\right)^2 = \frac{1}{8} a_2 V_{pp}^2 (1 - \cos 2\omega t)$, generating an output signal with a frequency that is twice the input frequency. It becomes clear that to achieve high conversion efficiency for frequency doubling, the coefficient $a_2 = \frac{1}{2!} \cdot \frac{\partial^2 V_{DS}}{\partial V_{GS}^2}$, i.e. the quadratic term in the V_{DS}-V_{GS} characteristics, needs to be as high as possible while the other components need to be suppressed. For this purpose, it becomes a natural choice to bias a GFET device at the minimum conduction point, where a_2 is at its maximum, to take advantage of its symmetric and highly quadratic transfer characteristics. When operating in this configuration, the symmetric transfer characteristics of a GFET can in principle eliminate all the odd-order terms in the output and its strong quadratic component can concentrate most of the output power at twice the input frequency, hence achieving high spectral purity.

Figure 5-1(b) shows the operation of the frequency multiplier when an input signal at 3 GHz is applied to the gate. Both the input and output signals are shown and frequency doubling is clearly demonstrated. The output signal has a fundamental frequency of 6 GHz with high spectral purity and low noise, where more than 90% of the output RF energy is at the useful frequency (6 GHz). Frequency doubling is also confirmed through measuring the power spectrum of the output signal (Figure 5-1(c)). In the output signal, the signal power at $f_{\text{out}} = 2f_{\text{in}} = 6$ GHz component is 10 dB higher than the signal power at $f_{\text{out}} = f_{\text{in}} = 3$ GHz component, which translates to a spectral purity above 90%.

Figure 5-1(d) shows the output power $P_{\text{out},2f_{\text{in}}}$ at frequency $f_{\text{out}} = 2f_{\text{in}}$, (blue square), against input power $P_{\text{in},f_{\text{in}}}$ at frequency f_{in} measured with an input signal of 3 GHz. The output power increases with the input power at a slope of 20 dB/dec. This agrees with the fact that the signal at $f_{\text{out}} = 2f_{\text{in}}$ is generated by the quadratic component in the transfer characteristics of the GFET and its power increases with a slope of 2 with respect to input power when plotted in logarithmic scale. The conversion gain (red dot), defined as: Gain=$P_{\text{out},2f_{\text{in}}}/P_{\text{in},f_{\text{in}}}$, increases with input power up to $P_{\text{in},f_{\text{in}}}$=2 dBm where the gain starts to saturate. The power gain is mainly limited by the low voltage gain in the device, which is due to a number of reasons including the lack of

current saturation in the device, the parasitic capacitances and resistances, as well as the slight asymmetry in the device transfer characteristics.

The output signal at 6 GHz has reached the frequency limit of the Agilent DSA90604A oscilloscope (frequency range DC-6 GHz), but the circuit itself can go much faster. Figure 5-5(a) shows the output signal power spectrum measured by the Agilent N9010A spectrum analyzer (frequency range: 9 kHz-26.5 GHz) when an input signal at 8 GHz is applied to the gate. The spectrum of the output signal shows a dominant peak at 16 GHz that is 11 dB higher than the peak at 8 GHz, which means that about 93% of the output power is at the doubled frequency of 16 GHz. The frequency dependence of the gain is shown in Figure 5-5(b). The -3dB cut-off point is 17 GHz, at about 80% of $f_{T,electron} = 20$ GHz. Owing to the high carrier mobility and high saturation velocity, the bandwidth is not limited by the carrier transit time, but mainly by the external RC time constant as shown below in the small-signal equivalent circuit analysis. This is the first time frequency doubling has been realized with a single transistor in the K_U-band frequency (12-18 GHz) without any filtering elements, allowing many potential applications in satellite communications, terrestrial microwave communications, and radar.

Small-signal Equivalent Circuit Analysis

Assuming the measurement pad parasitics are negligible, the high frequency small-signal equivalent circuit of the measurement setup is shown in Figure 5-4.
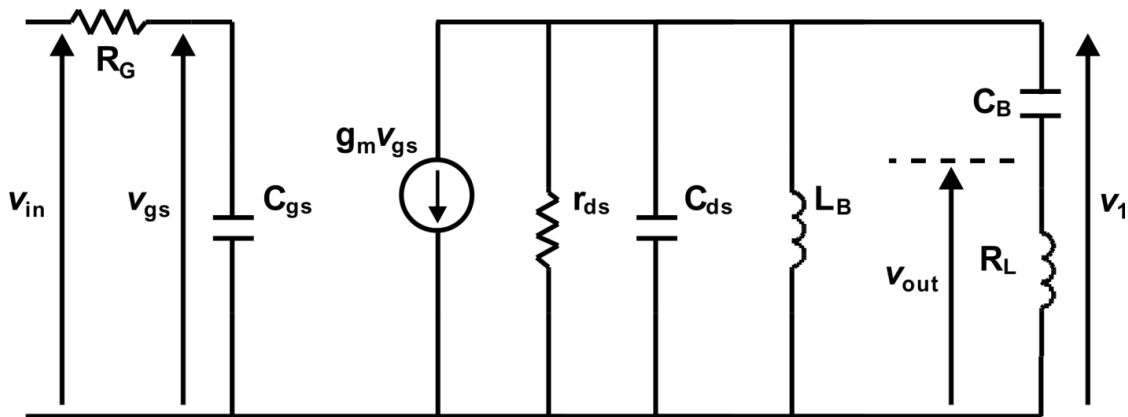
Figure 5-4 Small-signal equivalent circuit for the frequency multiplier measurement setup.

$$v_{\text{gs}} = \frac{1}{j\omega C_{\text{gs}} R_{\text{G}} + 1} v_{\text{in}}$$

(5-5)

$$v_{\text{out}} = \frac{j\omega C_{\text{B}} R_{\text{L}}}{j\omega C_{\text{B}} R_{\text{L}} + 1} v_1$$

(5-6)

$$v_1 = -g_{\text{m}} v_{\text{gs}} \left(r_{\text{ds}} \parallel \frac{1}{j\omega C_{\text{ds}}} \parallel j\omega L_B \parallel \left(\frac{1}{j\omega C_{\text{B}}} + R_{\text{L}} \right) \right)$$

(5-7)

The $\parallel$ operator represents a parallel connection between the two components. L_B and C_{B} are the inductor and capacitor in the bias-tee. C_{gs} is the gate capacitance and C_{ds} is the drain-source capacitance of the device. R_{L} is the load impedance of the measurement equipment that is either the Agilent DSA90604A oscilloscope or the Agilent N9010A spectrum analyzer. In both cases, $R_{\text{L}} = 50\Omega$. r_{ds} is the total resistance of the device channel and R_{G} is the gate resistance of the device. Hence, we have

$$\text{Voltage Gain} = \frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{j\omega C_{\text{B}} R_{\text{L}} g_{\text{m}}}{(j\omega C_{\text{B}} R_{\text{L}} + 1) \cdot (j\omega C_{\text{gs}} R_{\text{G}} + 1)} \left(r_{\text{ds}} \parallel \frac{1}{j\omega C_{\text{ds}}} \parallel j\omega L_B \parallel \left(\frac{1}{j\omega C_{\text{B}}} + R_{\text{L}} \right) \right)$$

(5-8)

The -3dB cut-off frequency of the voltage gain of the circuit can be found by setting the real and imaginary parts of the denominator in eq. (5-8) equal. If we assume L_B and C_{B} should only have small effects on $f_{\text{-3dB}}$ since the circuit operates well within the frequency range of the bias-tees, then this leads to a quadratic equation in terms of ω, which can be solved to give a closed-form solution of the -3dB cut-off frequency.

The key factors influencing the -3dB cut-off frequency include C_{gs}, C_{ds}, R_{L}, and r_{ds}, while the gate resistance R_{G} combined with C_{gs} affects the speed of the input stage. In a more simplified estimate of the RC time constant, we can consider only the two most important factors r_{ds} and

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C_{gs}. For the device with L_G=300 nm, we have $r_{ds}C_{gs}$=8.2×10^{-12} s and the -3dB cut-off frequency is $f_{-3dB} = \frac{1}{2\pi r_{ds}C_{gs}} \approx 20$ GHz.

This analysis is based on a small-signal model that assumes small changes in signal levels and linearized component values. This small signal analysis, of course, only gives a first-order estimate for the performance of the frequency multipliers, which clearly operates in large-signal modes. A more accurate analysis will have to make use of large signal models for graphene transistors and it will be for our future work.

Effect of Asymmetry in GFET Characteristics on Spectral Purity of the Output Signal

The symmetry in the device transfer characteristics plays a central role in affecting the spectral purity of the output signal. To analyze the effect of this symmetry, we revisit eq. (5-4). For frequency doubling, the useful 2f_{in} component, i.e. a second order term, is only generated by the quadratic component in the device transfer characteristics. Hence, the magnitude of a_2 with respect to the coefficients of the other polynomial components is crucial in determining the spectral purity of the output signal. In a special case, if the transfer curve is perfectly quadratic, i.e. $a_i = 0$ for all i ≠ 0 and 2, the output can in principle give a perfect sinusoidal signal with a doubled frequency [245]. For a normal graphene FET, the transfer curve may not be exactly symmetric, for example due to metal contact doping [203], and can contain linear and higher order components.

We can numerically simulate the output signal of a device, i.e. eq. (5-4), for a sinusoidal input signal described by eq. (5-3), if we know the transfer characteristic of the device; and the power in the output signal is proportional to the square of the signal voltage levels. In Figure 5-6(a), devices with transfer characteristics ranging from perfect symmetry (A) to unipolar (F) (similar to conventional Si FETs) are simulated. The hole conduction branch of these devices' transfer characteristics is taken from a typical graphene transistor fabricated at MIT. The device is assumed to be biased at the minimum conduction point. The output power levels are quoted as the square of the output signal voltage levels. This quoted power levels in each frequency component as given by the simulations are only meaningful when compared to each other in relative terms. The absolute values of the simulated power carry little significance because the

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effects of the load and the matching network are not included. Hence, we choose the simulated power level of the $f_{out} = f_{in}$ component for a perfectly symmetrical device (A) as the reference power level and set it as 0 dB. All other power values are quoted with respect to this reference power level.

Figure 5-6(b) shows the simulated relative output power at $f_{out} = f_{in}$ and $f_{out} = 2f_{in}$. As the device transfer characteristic changes from perfect symmetry to unipolar, the relative power at $f_{out} = f_{in}$ increases from 0 dB to 13.5 dB while the power at $f_{out} = 2f_{in}$ decreases from 14.1 dB to 11 dB. This result shows that, for a given input signal, as the device transfer characteristic becomes more asymmetric, the quadratic term (and other higher-order even terms) in the transfer characteristic, i.e. a_2 (and a_4, a_6, a_8 ...) in eq. (5-4), decreases while the linear term a_1 (and other higher-order odd terms a_3, a_5, a_7 ...) increases, leading to a reduction in the output power at $f_{out} = 2f_{in}$ component (and other even order harmonics) and an increase in the output power at $f_{out} = f_{in}$ component (and other odd order harmonics). Hence, the output spectral purity for frequency doubling decreases as a result. As shown in Figure 5-6(b), perfectly symmetric GFETs can achieve a spectral purity well above 95% as compared to only 33% for unipolar devices. This highlights the great advantage of ambipolar frequency multipliers in terms of output spectral purity as compared to the conventional frequency multipliers based on unipolar devices. In Si-based electronics, more complex circuits may be designed for more efficient frequency multiplication and mixing, however, the increased circuit complexity with many times more circuit components often limits the frequencies performance of the circuit due to increases amount of parasitics. Hence, the simplicity of the circuits allowed by ambipolar electronics, combined with the high mobility in graphene, is particularly promising for implementing efficient analog electronics at extremely high frequency.
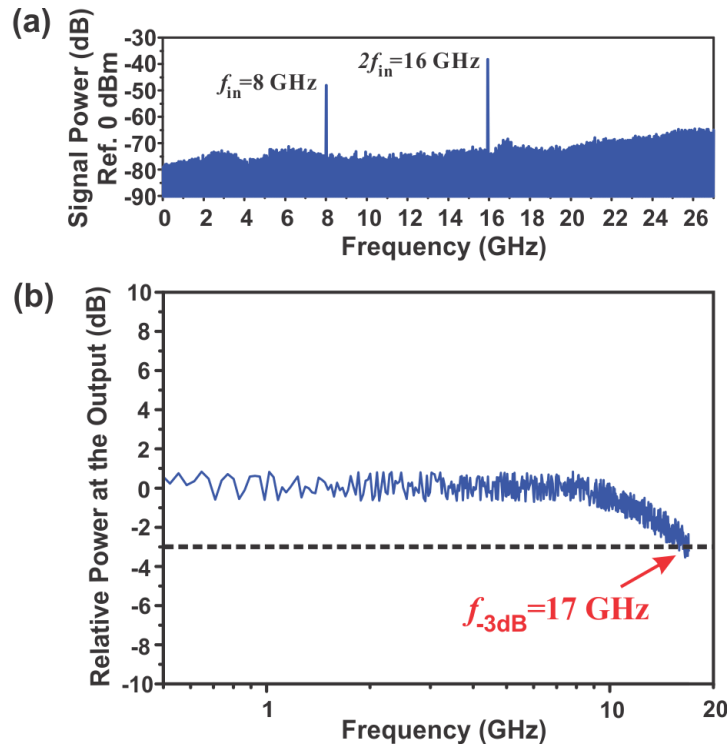
Figure 5-5 Output frequency spectrum and -3dB cut-off frequency characterization of the frequency multiplier. Output power at $f_{out}=2f_{in}$ is plotted against the input power at f_{in}. The output power at $2f_{in}$ increases with the input power with a slope of 20 dB/dec. Conversion Gain= $P_{out,2fin}/P_{in,fin}$ increases with input power up to 2 dBm.
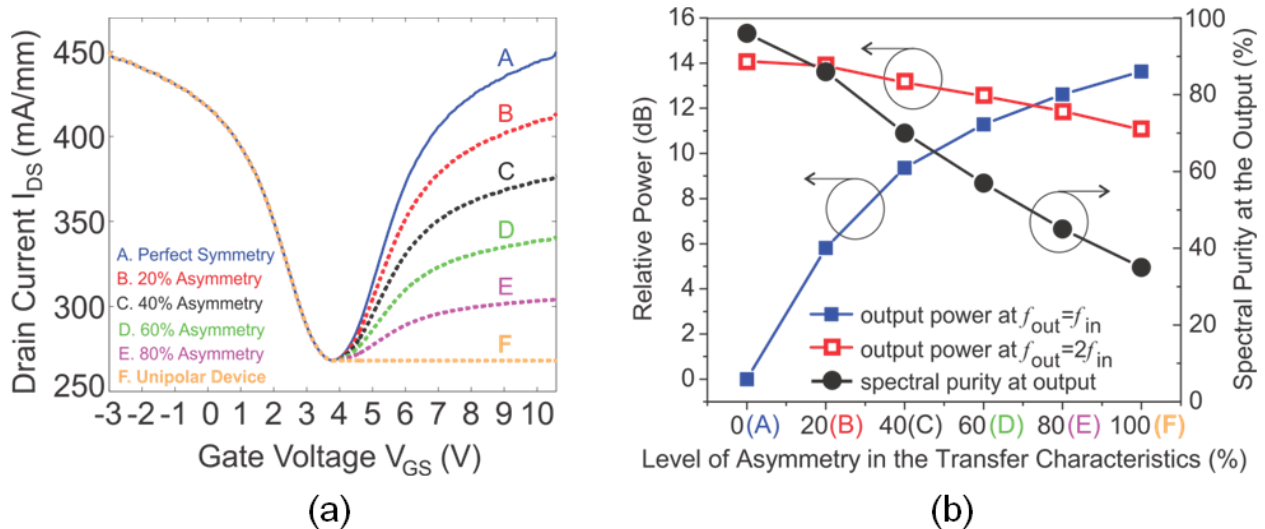
Figure 5-6 Effects of asymmetry in the transfer characteristics on relative output power at $f_{out}=f_{in}$ and $f_{out}=2f_{in}$ (a) Simulated transfer characteristics: the left half of the transfer curve is taken from typical transfer characteristics of graphene transistors fabricated at MIT. The right half is simulated from (A) perfect symmetry, to (F) unipolar (similar to conventional FET). (b) Relative output power at $f_{out}=f_{in}$ (blue squares) and $2f_{in}$ (red squares) for devices

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from 0% asymmetry (perfect symmetry) to 100% asymmetry (unipolar device), corresponding to simulated devices A to F in Figure 5-6(a). The device is assumed to be biased at the minimum conduction point. The output spectral purity (black dots) decreases as the GFET transfer characteristics becomes more asymmetrical.

5.3. Graphene Ambipolar Mixers for RF Applications

The significant quadratic component that comes with the symmetrical I_D-V_{GS} characteristics of graphene transistors also allows the device to be used as excellent RF mixers. Assuming that the transfer characteristics of the GFET are completely symmetric and infinitely differentiable, we can then describe the drain current as: $I_D = a_0 + a_2 (V_{GS} - V_{G,min})^2 + a_4(V_{GS} - V_{G,min})^4 + \dots$

where $V_{G,min}$ is gate voltage at the minimum conduction point. a_0, a_2, a_4, … are constants. From this expression, for ideal GFETs with symmetric transfer characteristics and biased at the minimum conduction point, no odd-order intermodulation distortions should appear at the output and all the output power is coupled to the difference and sum frequency, and other even-order terms. Therefore odd-order intermodulations, which are often present in conventional uni-polar mixers [246][247] and are harmful to circuit operations [247], can be significantly suppressed in GFET mixers while keeping a simple circuit. MATLAB simulations show that for given input signal power, the GFET mixer with transfer curve in Figure 5-8(a) can generate 7 dB higher useful power while having a 3rd order intermodulation that is 8 dB lower than a single transistor unipolar mixer with comparable On/Off current ratio and transconductance. This advantage can be increasingly more significant if the I-V of the GFET becomes more symmetrical. Conventional mixers with unipolar devices rely on more complicated circuits, which is a serious problem at high frequency, to achieve good intermodulation performance [248].
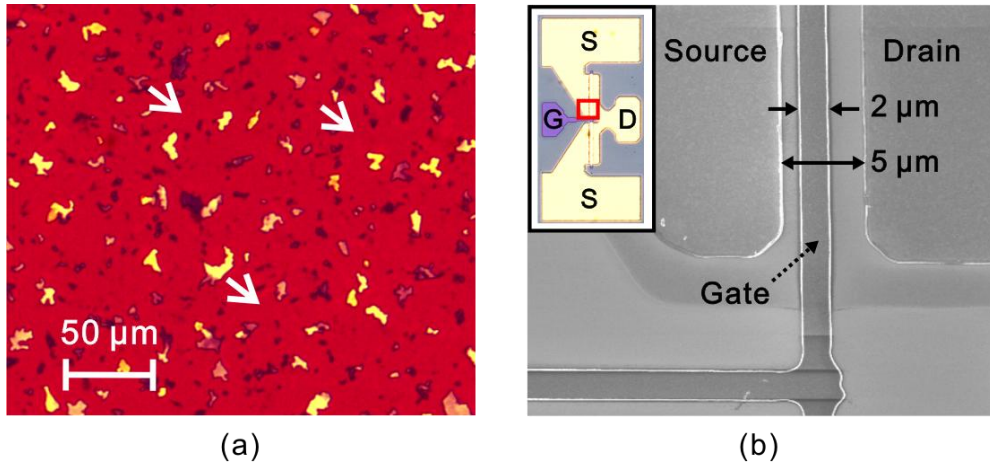
Figure 5-7 CVD graphene grown on Ni catalyst and SEM image of the graphene transistor (a) Micrograph of CVD grown graphene using Ni catalyst. The arrows indicate regions of few-layer graphene. Regions with a mix of single-layer and bi-layer graphene can be up to 20 μm in lateral size. (b) SEM image of a fabricated GFET with L_G=2 μm and L_{DS}=5 μm. The inset shows a micrograph of the device where the square indicates area of the SEM image.
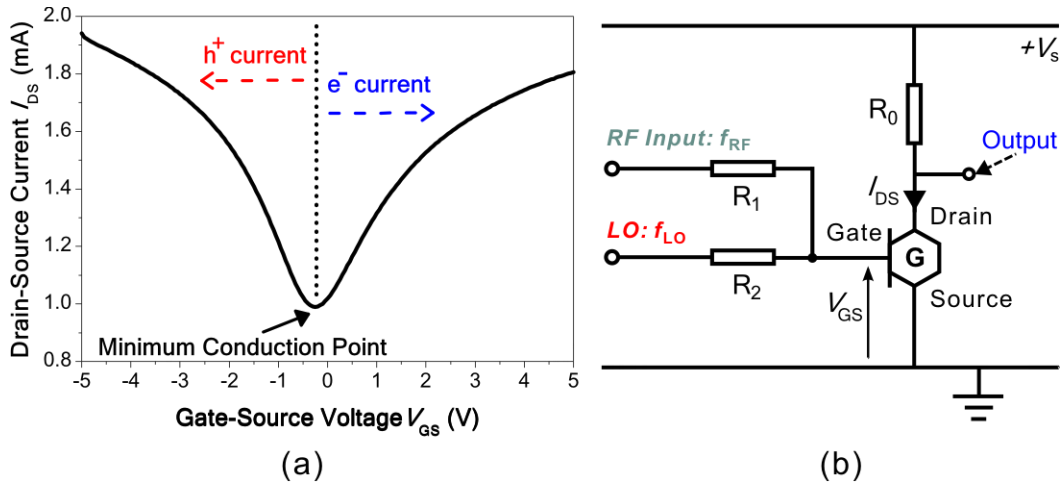
Figure 5-8 Graphene FET transfer characteristics and application circuit for ambipolar frequency mixer (a) I_D-V_{GS} characteristics of the fabricated GFETs with L_G=2 μm, W_G=2×75 μm and L_{DS}=5 μm. The minimum conduction point is very close to 0 V. (b) Proposed circuit for graphene ambipolar RF mixers. Note: no DC bias is needed at the input due to minimum conduction point close to 0 V.

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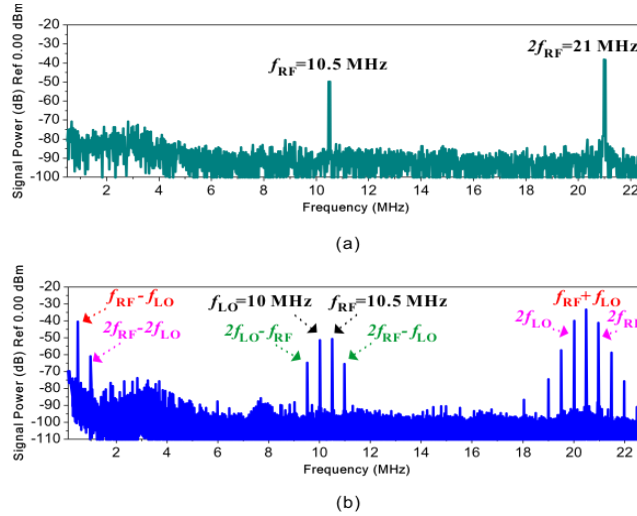
Figure 5-9 Output frequency spectrum of the ambipolar frequency mixer with one and two input signals. Spectrum Analysis: (a) Output spectrum with single RF input f_{RF}=10.5 MHz without LO signal. The frequency doubling is clearly visible. The signal power at $2f_{RF}$=21 MHz is about 10 dB higher than signal power at f_{RF}=10.5 MHz without filtering. (b) Output spectrum with RF input f_{RF}=10.5 MHz and local oscillator f_{LO}=10 MHz at equal power. The presence of strong signal power at f_{RF} - f_{LO}=500 kHz and f_{RF} + f_{LO}=21.5 MHz clearly demonstrates mixing operations. All data are obtained using Agilent N9010A spectrum analyzer and the measurements were done at room temperature in air.

Graphene Ambipolar Mixers

Figure 5-8(b) shows the proposed circuit for GFET mixers. Since the fabricated GFETs have a minimum conduction point close to zero, no DC bias is needed at the gate. This greatly simplifies the circuit and improves energy efficiency. Figure 5-9 shows the experimental demonstration of ambipolar GFET mixers. If a single RF input signal, f_{RF}=10.5 MHz, is applied to the gate, the device works as a frequency doubler. The output spectrum (Figure 5-9(a)) shows a dominant peak at $2f_{RF}$=21 MHz.

If two signals, a RF input signal and a local oscillator (LO) signal with frequencies f_{RF}=10.5 MHz and f_{LO}=10 MHz, are introduced to the gate, the GFET mixes them to generate output signals with a frequency equal to the sum (f_{RF} + f_{LO}=20.5 MHz) and difference (f_{RF} - f_{LO}=500 kHz), as shown in the output power spectrum in Figure 5-9(b). It is also interesting to note that the power at second order frequencies, f_{RF} - f_{LO} and f_{LO} + f_{RF}, is more than 10 dB higher than the power at fundamental frequencies, f_{RF} and f_{LO}; the power at fourth order frequencies, $3f_{RF}$ - f_{LO} and $3f_{LO}$ - f_{RF}, is 8 dB higher than the power at third order frequencies, $2f_{LO}$ - f_{RF} and $2f_{RF}$ - f_{LO}

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(Figure 5-9(b)). Similar trend is also observed for higher order even and odd frequencies. This is in strong contrast to mixing operation in unipolar devices [249], where odd-order frequencies are often much higher in power than the corresponding even-order frequencies. Hence, in GFET mixers, a larger proportion of the output power is at the sum and difference of the RF input frequencies, as well as other useful even-order harmonics. The power at odd-order frequencies, especially third order frequencies like $2f_{LO} - f_{RF}$ and $2f_{RF} - f_{LO}$ that are usually too close to the fundamental signals to be filtered out and are harmful to circuit operations, is significantly suppressed due to the symmetrical character of the GFET transfer characteristics. In addition, these devices have the potential to operate at very high frequencies due to the high electron mobility in graphene.

Figure 5-10(a) shows the dependence of signal power at intermediate frequency (IF), $f_{IF} = f_{RF} - f_{LO} = 500$ kHz, on the RF input power, with f_{RF}=10.5 MHz and f_{LO}=10 MHz. The fabricated GFET mixer shows good linearity. The conversion loss (CL) of the mixer is between -30 dB to -40 dB. The conversion gain can be increased by improving the device transconductance. As a first order estimate, a 0 dB gain can be achieved if the transconductance can improve from 5.5 mS/mm of the device shown in Figure 5-8 to 181 mS/mm, which can be achieved through using thinner gate dielectrics and material with higher mobility [250].

Figure 5-10(b) shows the characterization of the 3rd order intermodulation product using two-tone measurements ($f_{RF,1}$ =10.5 MHz and $f_{RF,2}$ =10.6 MHz). The local oscillator frequency f_{LO} is 10 MHz, while the intermediate frequencies are at 500 kHz and 600 kHz. The third order intermodulation frequencies are at 400 kHz and 700 kHz. The output power at intermediate frequencies and third-order intermodulation frequencies follow the theoretical 10 dB/decade and 30 dB/decade dependencies respectively. A third order intermodulation intercept (IIP3) of 13.8 dBm is achieved in these devices with a local oscillator input power (P_{LO}) of 0 dBm, resulting in a quality factor of Q_{IIP3}=IIP3/P_{LO}=13.8 dB. Conventional diode or single transistor mixers often have quality factor between 5 to 20 dB at GHz [251][252][253].

(a)

(b)
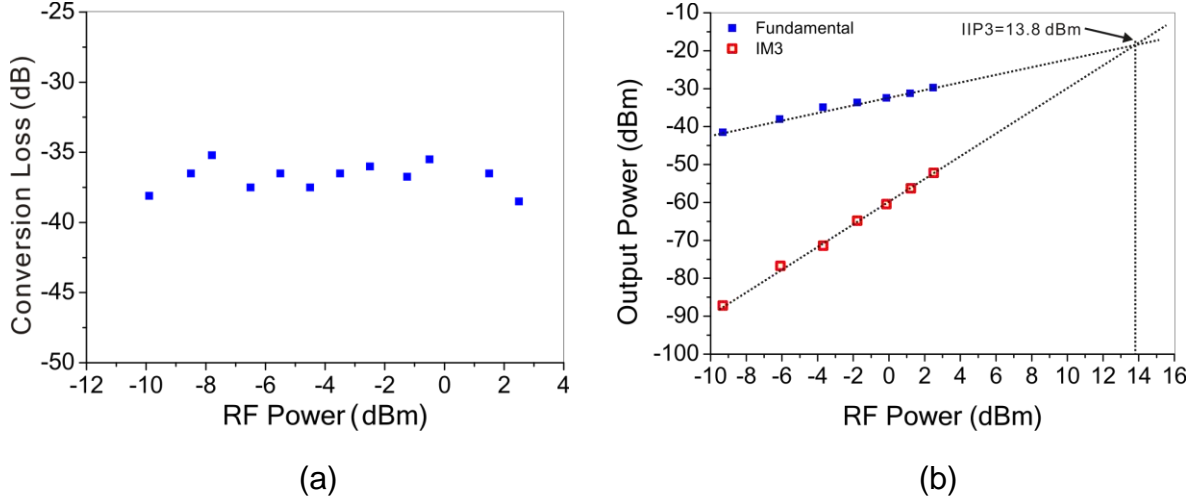
Figure 5-10 The conversion gain (loss) and the third order intermodulation point for the graphene mixer (a) Signal power at intermediate frequency vs. the RF input power at room temperature, with f_{RF}=10.5 MHz and f_{LO}=10 MHz. GFET mixer shows good linearity. (b) Two-tone test in vacuum: $f_{RF,1}$=10.5 MHz, $f_{RF,2}$=10.6 MHz and f_{LO}=10 MHz. The intermediate frequencies are $f_{IF,1}$=500 kHz, $f_{IF,2}$=600 kHz. The third order intermodulations are $f_{IM3,1}$=400 kHz, $f_{IM3,2}$=700 kHz. Local oscillator input power is 0 dBm. DC supply voltage applied is 1 V and R_0 is 1 kΩ.

The frequency performance of graphene mixers is primarily limited by the speed of the device themselves, which is limited to tens of MHz in this experiment due to the device dimensions. f_T can be calculated by using the expression, $f_T = \frac{g_m}{2\pi C_G}$. In our device, g_m=5.5 mS/mm, as obtained from the slope of the I_{ds}-V_{gs} curve. Capacitance-voltage (CV) measurements show a gate capacitance of 4.5 pF/mm in this device. This leads to a calculated f_T of about 190 MHz for these devices. At these frequencies, the mobility of the material ($\sim$1000 cm^2/Vs) should not be the limiting factor for speed. If we estimate the RC time constant of the device, we obtain a 3dB cut-off frequency f_c=$(2\pi RC)^{-1}$= 99 MHz, where we used R=2.38 kΩ for the on-state resistance and C_g=4.5pF/mm $\cdot$ 150µm =675 fF. The on-state resistance is derived from DC measurements and the gate capacitance is obtained from CV measurements.

The key limitation to f_T is the device gate length and gate capacitance. Higher frequency performance can be achieved by shrinking the gate length and gate oxide thickness. As a first order estimation using the $1/L_G^2$ dependence [117], these device from CVD graphene will have f_T in the GHz range with gate length less than 1 μm and have f_T exceeding 100 GHz with gate length of 60 nm. Much higher frequencies would be possible for devices with mobilities above

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1000 cm^2/Vs. The contact resistance and the degradation of mobility due to top gate dielectric also affect frequency performance.

The asymmetry in the transfer characteristics shown in Figure 5-8(a) may be attributed to chemical doping by adsorbants during processing and handling of the sample [254]. This asymmetry affects mixing by introducing more significant odd order intermodulations. However, the asymmetry is not significant for gate voltage within ±1V of the minimum conduction point. Hence, for small signal mixer applications where the input signal is usually less than a couple of volt peak-to-peak, the asymmetry is not of major concern to mixer performance.

Furthermore, the concept described here can also be realized in other materials that exhibit ambipolar conduction properties, such as some carbon nanotube transistors (CNT) [236]. However, the ambipolar I_{ds}-V_{gs} characteristics of GFETs are often more linear than CNT FET's, leading to less distortion and higher efficiency.

5.4. Binary Phase Shift Keying

Besides frequency multipliers and mixers, the graphene transistors can also be used to demonstrate a binary phase shift keying device for modulating digital signals onto an analog carrier signal. Figure 5-11 shows the application circuit, which is similar to the ambipolar mixer. For this application, a digital square wave (data signal) and a high frequency sinusoid (carrier wave) can be applied to the gate, which is biased at the minimum conduction point by a DC source. The digital signal switches the channel of the GFET between electron and hole conduction. Due to the negative gain on the hole branch and the positive gain on the electron branch of the device transfer characteristics, the output signal is the carrier wave modulated by the data signal with 180° phase shift between "1" and "0" (Figure 5-11).

To demonstrate this experimentally, a carrier signal with $f_{carrier}$=500 Hz (Figure 5-12(a)) and a digital data signal f_{data}=50 Hz (Figure 5-12(b)) are supplied to the gate, which is biased to the minimum conduction point. The output signal measured by an oscilloscope is shown in Figure 5-12(c). The 180° phase shift is clearly visible. Although, this demonstration is done at low frequency, the real frequency performance is only limited by the speed of the GFET. In addition,

this application, as for all analog signal processing applications, does not require a bandgap in graphene.
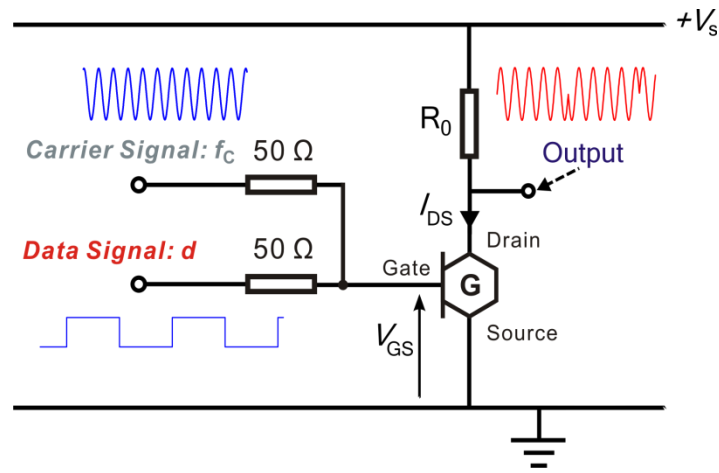
Figure 5-11 Application circuit for the graphene ambipolar binary phase shift keying device
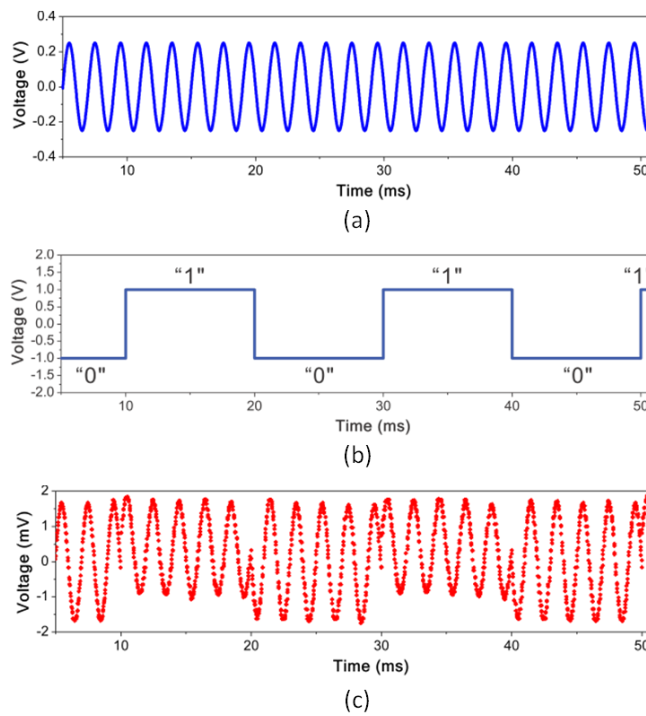
Figure 5-12 Experimental demonstration of a graphene ambipolar phase shift keying device

To end this Chapter, I would like to say that since we proposed the concept of ambipolar electronics in 2009, the idea has been very well received in the graphene research community. Many exciting work has followed in this new research direction for graphene electronics and

analog electronics design in general. With continuous improvements in the graphene material quality and the device technology, ambipolar electronics based on graphene has the great potential to change the way many conventional analog circuits are designed, especially targeting very high frequency applications, because of the extreme simplicity of the circuitry and the high mobility that graphene has to offer.

Chapter 6. MoS$_2$ Transistor Technology and Circuit Applications

In previous chapters, we have discussed the work in developing graphene as a two dimensional material targeting analog electronics application at high frequency. However, graphene suffers from the fundamental limit of zero-bandgap, low on/off ratio and the lack of current saturation, which makes graphene unsuitable for digital logic applications. In developing nano-electronic systems based on 2D materials, it is also highly desirable to have transistors suitable for logic operations because most of today's electronic systems are digital systems or at least have digital components. There have been many approaches in developing graphene for this purpose, such as inducing bandgap in graphene by patterning the material into very narrow ribbons (~5 nm), which relies on the edge states and lateral quantum confinement for opening up bandgap, or by using bi-layer graphene where a strong external electric field can lead to asymmetry in the bandstructure and the creation of bandgaps. All these studies have enabled very interesting new physics, but due to the fabrication challenges, reliability issues, controllability of the process, sample uniformity and the intrinsic limit of requiring a strong external field for the case of bi-layer graphene, it will be very challenging for these approaches to make it to industrial level applications in the near future. In this chapter, we take a different approach. Instead of trying to use graphene for logic application, we look for a new 2D material that can naturally provide the bandgap that is needed for building transistors suitable for digital electronics. It turns out that many members of the layered transition metal dichalcogenides (LTMD) family are semiconductors with the right bandgap, such as MoS$_2$, WS$_2$, MoSe$_2$ and WSe$_2$ (Table 6-1). The measured or calculated bandgap from the literature for single-layer material is shown in red. There is an important difference between the optically measured direct bandgap in single layer materials and its real electronic bandgap, primarily due to the existence of large exciton energy in these materials [163][255]. However, there are variations in the calculated exciton energy and electronic bandgap reported in the literature and the exact values are still yet to be verified through experiments.

Two-dimensional (2D) materials, such as molybdenum disulfide (MoS$_2$), have been shown to exhibit excellent electrical and optical properties. The semiconducting nature of MoS$_2$ allows it to overcome the shortcomings of zero-bandgap graphene, while still sharing many of graphene's

advantages for electronic and optoelectronic applications. Discrete electronic and optoelectronic components, such as field-effect transistors, sensors and photodetectors made from few-layer MoS_2 show promising performance as potential substitute of Si in conventional electronics and of organic and amorphous Si semiconductors in ubiquitous systems and display applications. In this section of the thesis, we address a few issues that are critical for the future applications of LTMD 2D materials: from device technology based on both exfoliated flakes and CVD grown materials to some circuit-level demonstration of the basic building blocks of both digital and analog electronics. We benchmark the device and circuits performance against other materials that have been proposed for large-area low cost electronics, such as organic semiconductors, ZnO and large-area carbon nanotube arrays. The fabrication of integrated circuits on large-area CVD grown samples demonstrate the scalability of the technology. The characterization of the basic properties, such as mobility of the material and the contact resistance of the devices, will also be presented.

Metal	- S_2	-Se_2	-Te_2
Ti	1.95(DB),0.3(IB)	1.55(DB),0.15(IB)	Semi-metal
Zr	1.68(DB),2.10(IB)	1.20(DB), 1.61(IB)	
Hf	2.7(DB),1.93(IB)	1.77(DB),1.18(IB)	Semi-metal
V	Metal	Metal	Semi-metal
Nb	Metal, superconductor	Metal, superconductor	Metal
Ta	Metal, superconductor	Metal, superconductor	Semi-metal
Mo	Bulk: 1.2(IB) Single-layer: 1.88(DB), 2.82(EB)	Bulk: 1.1(IB), Single-layer: 1.49(DB), 2.41(EB)	Bulk: Semi-metal Single-layer: 1.13(DB), 1.77(EB)
W	Bulk: 1.35(IB) Single-layer: 1.77(DB), 2.88(EB)	Bulk: 1.1(IB), Single-layer: 1.60(DB), 2.42(EB)	Semi-metal

DB: Direct Bandgap, IB: Indirect Bandgap, EB: Electronic Bandgap

Table 6-1 Bandgaps for transition metal dichalcogenides in their bulk and single-layer form. Here, a single molecular layer of LTMD consists of one layer of transition metal sandwiched between two layers of chalcogen atoms. The bandgaps for the single-layer LTMD are shown in red.

6.1. MoS$_2$ Transistor Technology based on Exfoliated Thin films

Molybdenum disulfide (MoS$_2$) [16] and other members of the transition metal dichalcogenides family offer new opportunities for developing novel applications in electronic systems with its unique 2D geometry that is very attractive for miniaturization beyond Moore's Law [17][18] and as a potential high-mobility alternative to amorphous silicon [19] and organic semiconductors
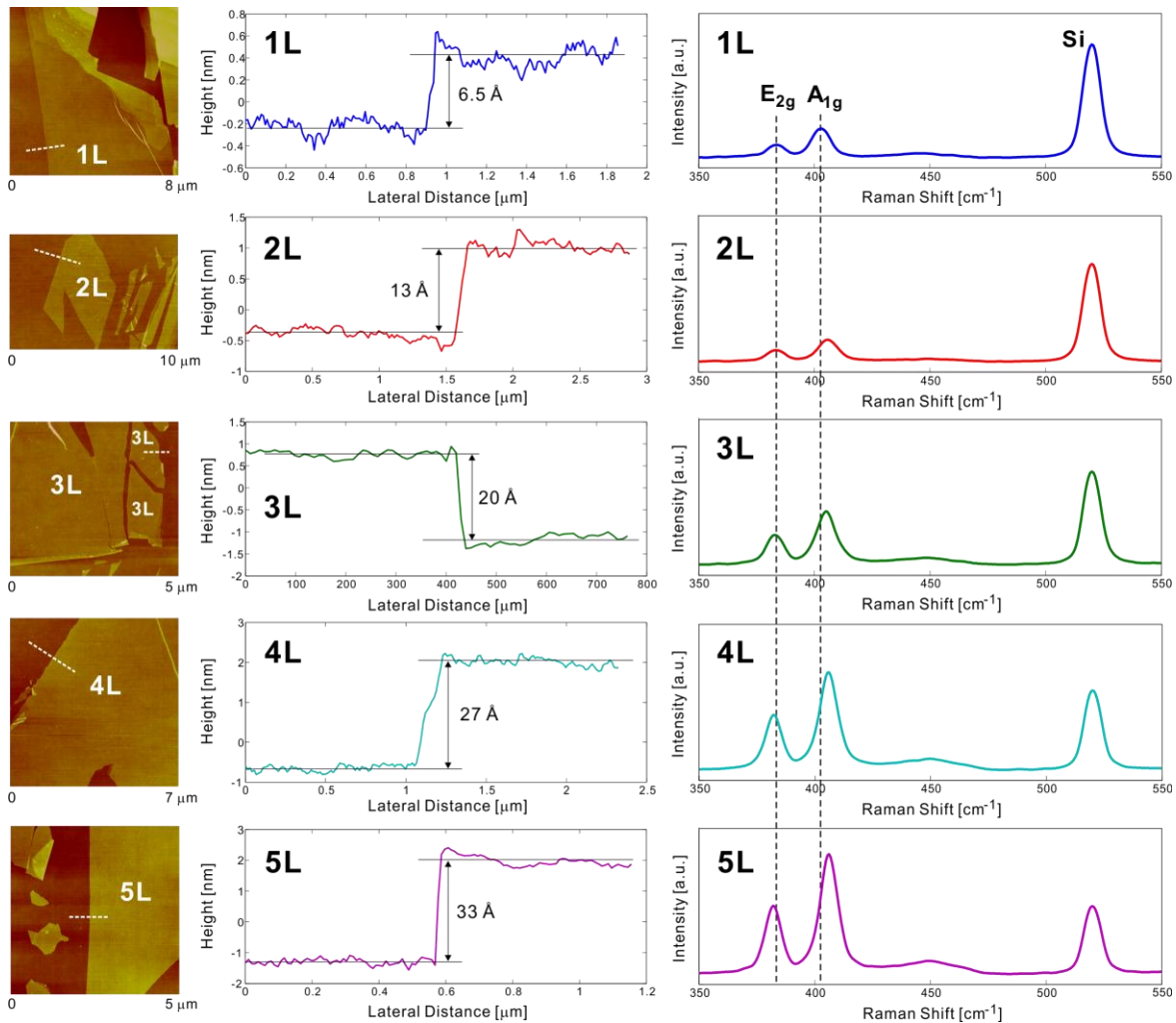
Figure 6-1 Corresponding data from AFM and Raman spectroscopy measurements for one-layer to five-layer MoS$_2$ thin films. For each MoS$_2$ flake, the height information from AFM and Raman peak spacing between E$_{2g}$ mode and A$_{1g}$ mode are cross-checked to confirm the number of layers in the MoS$_2$ thin film.

[20][21] for large-area and low-cost electronics. 2D materials with strong σ-bonds in plane and only weak Van der Waal's coupling between layers offer an ideal material structure with little out-of-plane dangling bonds, giving rise to a self-passivated surface that is very appealing for

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building electronic devices. Here, single- and few-layer MoS_2 will be used as an example for constructing transistor devices and basic building blocks for digital and analog circuits while similar techniques can also be applied to other member of the LTMD material family such as WS_2, WSe_2, $MoSe_2$.

Exfoliation and Identifying the number of layers in LTMD: For devices and circuits based on exfoliated flakes, the fabrication process starts with the exfoliation of MoS_2 thin films from commercially available bulk MoS_2 crystals (SPI Supplies) onto 285 nm SiO_2 on Si substrate, which has pre-patterned alignment grids (Cr/Au), using the micro-mechanical cleavage technique. The thickness of the SiO_2 was selected to provide the optimal optical contrast for locating MoS_2 flakes relative to the alignment grids and for identifying their number of layers [256]. The number of MoS_2 layers was then confirmed by atomic force microscopy (AFM) based on its thickness and by Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode, respectively [257]. Figure 6-1 shows the correspondence between the AFM data and Raman data for 1-layer (1L) to 5-layer (5L) MoS_2 flakes. After exfoliating the MoS_2 thin film onto 285 nm SiO_2/Si substrate, the flakes were first located using optical microscope and the number of molecular layers was estimated based on their optical contrast [256]. Then the number of layers was confirmed using both AFM and Raman spectroscopy. Bilayer MoS_2 thin films used in this report typically have a thickness around 13 Å as measured by AFM. The lateral size of the exfoliated bilayer MoS_2 thin films can reach up to 40 μm (Inset of Figure 6-2(a)).
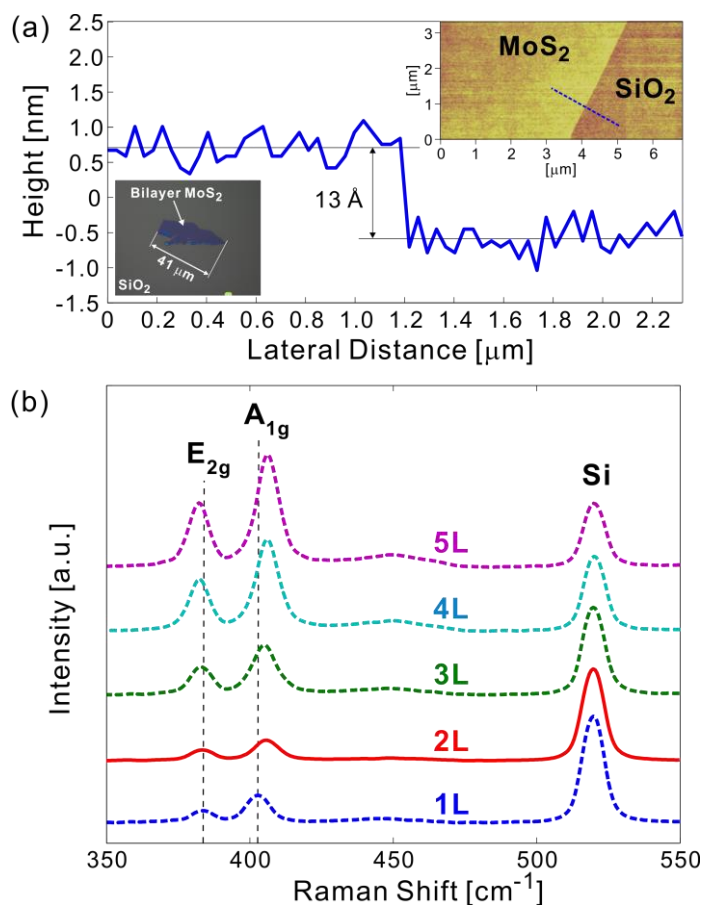
Figure 6-2 Optical micrograph, AFM and Raman spectroscopy of bilayer MoS_2. (a) Optical micrograph and AFM data of a bilayer MoS_2 thin film. The flake is 13 Å thick, which is equal to twice the thickness of single-layer MoS_2, confirming the flake being bilayer. (b) The number of layers in the MoS_2 thin film can also be confirmed from its Raman spectroscopy based on the peak spacing between the E_{2g} mode and the A_{1g} mode [257]. The red-shift of E_{2g} peak and blue-shift of A_{1g} peak lead to increasing peak spacing between E_{2g} and A_{1g} modes as the number of layers in the MoS_2 thin film increases.

In Figure 6-1 and Figure 6-2, Atomic force microscopy (AFM) for identifying the thin film thickness was performed on a Veeco Dimension^{TM} 3100 system. Raman spectroscopy was performed with a 532 nm Nd:YAG laser. All optical micrographs were taken with a Zeiss Axio Imager.A1m microscope.

Device and integrated circuit fabrication

To fabricated devices and circuits on MoS_2 thin film, the sample was first annealed at 350 C° in Ar 600 sccm/H_2 30 sccm for three hours to clean away the tape residue. The next step was to

pattern the first metal layer (M1), which are the electrodes directly in contact with MoS_2, i.e. source and drain of the devices, using electron-beam lithography (Elionix F125) based on poly(methyl methacrylate) (950k MW PMMA) resist. We then evaporated 3 nm Ti/ 50 nm Au followed by lift-off to form the contacts. Subsequently, the samples were annealed again at 350 ℃, 600 sccm Ar/30 sccm H_2 for three hours. This annealing step reduces device resistance and also removes the PMMA residue to create a clean surface for subsequent atomic layer deposition (ALD) process. The top gate dielectric consisting of 20 nm HfO_2 was then deposited by ALD. To fabricate discrete transistors, the last step of the fabrication was to pattern the top gate electrode by electron-beam lithography, which was then formed by depositing the desired gate metal. For the construction of integrated logic circuits (Figure 6-3(b)), the second and third metal layers (M2 and M3) need to be connected to the first metal layer (M1) at certain locations depending on the design. This was achieved by patterning and etching via holes through the HfO_2 dielectric using reactive ion etching (RIE) with BCl_3/Cl_2 gas chemistry. This etching step preceded the definition of the gate metal layers M2 and M3.

ALD and Via Hole Etching

The HfO_2 gate dielectric was deposited using ALD at 170 °C. The ALD deposition of HfO_2 was done on a commercial Savannah ALD system from Cambridge NanoTech using alternating cycles of H_2O and tetrakis(dimethylamido)hafnium (TDMAH) as the precursors. To fabricate the integrated circuits shown in this report, it is also necessary to etch via holes through the HfO_2 dielectric so that on-chip interconnections can be made between metal layer 1 and metal layers 2 and 3. We used a commercial Electron Cyclotron Resonance Reactive Ion Etcher (ECR/RIE) system (Plasma Quest) to perform this etch using BCl_3/Cl_2 gas chemistry. The ratio between the flow rates of BCl_3 and Cl_2 is 4:1. The etch rate of our low power recipe is around 6 nm/min.

Device and circuit characterization

Device characterization was performed using an Agilent 4155C semiconductor parameter analyzer and a Lakeshore cryogenic probe station with micromanipulation probes. The integrated circuits were characterized with an Agilent 54642A oscilloscope (1 MΩ input impedance) and the output signal power spectrum of the ring oscillator was measured with an Agilent N9010A Signal Analyzer (50 Ω input impedance). All measurements were done in vacuum (~10^{-7} Torr) at

room temperature. The high vacuum isolates the device from influences of oxygen and water vapor. The oxygen and water vapor can often attach to edges and defect sites of MoS_2, leading to possible hysteresis and additional scattering. The hysteresis can be mostly eliminated when the device is in high vacuum.

The direct-coupled FET logic (DCFL) technology is a popular architecture for constructing high-speed circuit with low power dissipation, where an excellent trade-off between speed and power loss may be achieved [258][259] and is suitable for application in low-power flexible electronics. The DCFL circuits used in this letter integrates both negative (D-mode) and positive (E-mode) threshold voltage transistors on the same chip (Figure 6-3(a) and Figure 6-3(b)). This can be achieved through engineering the gate metal work functions of the MoS_2 FETs. Figure 6-3(c) and Figure 6-3(d) show the device characteristics of two MoS_2 FETs with Al ($w_M = 4.08$ eV) and Pd ($w_M = 5.12$-5.60 eV) [260] gates, respectively, fabricated side-by-side on the same bilayer MoS_2 thin film. The difference in the work functions of these two metals effectively shifts the threshold voltages of the MoS_2 FET characteristics by about 0.76 V to form a D/E-FET pair (Figure 6-3(c) and Figure 6-3(d)). The shift in the threshold voltage is lower than the metal work function difference in vacuum (~1.04 eV) as discussed below.
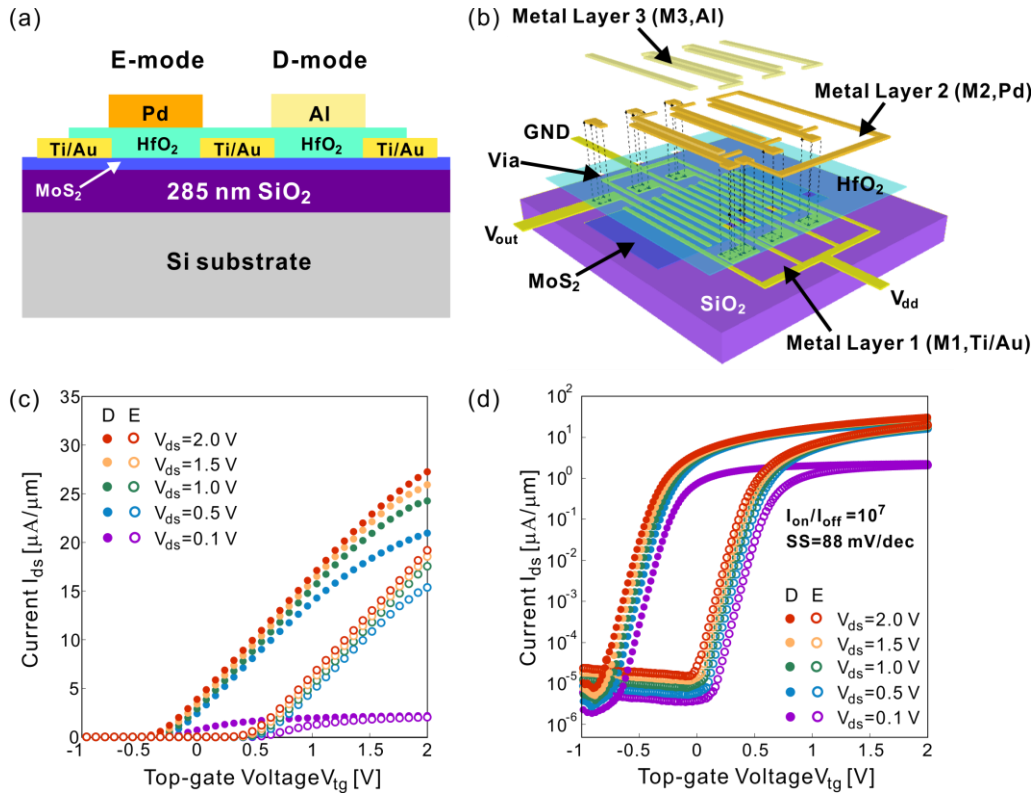
Figure 6-3 Enhancement mode and depletion mode MoS_2 transistors (a) Schematic representation of an E-mode and a D-mode device. (b) Schematic illustration of an integrated 5-stage ring oscillator circuit on MoS_2 thin films, which is constructed by integrating 12 MoS_2 FETs. Three distinct metal layers of the MoS_2 IC are represented by M1, M2, and M3. M1 is directly in contact with the bilayer MoS_2 thin film while M2 and M3 are the Pd and Al gate layers, respectively. Via holes are etched through the HfO_2 dielectric layer to allow connections from M2 and M3 to M1. The fabricated ring oscillator circuit corresponding to the design above is shown in Figure 6-7. The general aspects of the fabrication process apply to all the devices and logic circuits presented in this letter. (c) The transfer characteristics of depletion (D) mode and enhancement (E) mode bilayer MoS_2 FETs. The depletion mode FET has Al as the gate metal while the enhancement FET has Pd as the gate metal. The on-state current and transconductance of a device are its key dc performance metrics, critical for circuit application. In these bilayer MoS_2 FETs, the on-state current density exceeds 23 $\mu A/\mu m$ at V_{ds}=1 V and the transconductance is above 12 $\mu S/\mu m$, both being the highest values reported for MoS_2 FETs so far. The difference between the work functions of Al and Pd (~1.04 V in vacuum) gates results in a 0.76 V shift in the threshold voltage. The discrepancy between the work function difference in vacuum and in HfO_2 can be attributed to the dipoles at the metal/HfO_2 interface, resulting from charge transfer across this boundary [261]. (d) The transfer characteristics in logarithmic scale of depletion (D) mode and enhancement (E) mode bilayer MoS_2 FETs. The I_{on}/I_{off} ratio exceeds 10^7 for V_{ds} above 0.5 V, and is about 10^6 at V_{ds}=0.1 V. The sub-threshold slope (SS) is 88 mV/dec. Device dimension: L_g=1 μm and L_{ds}=1 μm. The substrate is grounded.

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Both the D-mode and E-mode FETs have a high on/off current ratio in excess of 10^7 (Figure 6-3(d)), which is very close to that in single-layer MoS_2 FETs [27]. On the other hand, at the on-state, these devices based on bilayer MoS_2 have much higher on-state current density (exceeding 23 μA/μm at V_{ds}=1.0 V and V_{tg}= 2.0 V for the depletion mode FET, Figure 6-3(c)) than that reported for single-layer MoS_2 FETs [27][103]. The corresponding maximum transconductance of the bilayer FETs exceeds 12 μS/μm at V_{ds}=1.0 V. These bilayer MoS_2 FETs can hence offer superior on-state performance than single-layer devices, with only a small degradation in terms of on/off current ratio. The high-field transport of both FETs shows saturation behavior (Figure 6-4(a)), a critical feature for both logic and analog circuits, for the first time in top-gate MoS_2 FETs. The excellent match between the on-set of saturation and the gate overdrive (i.e. V_{sat}=V_{tg}-V_t, where V_{sat} is the saturation voltage and V_t is the threshold voltage of the FETs) indicates that the current saturation is due to the classic channel pinch-off mechanism, as is typical for long channel MOSFETs [205]. The field-effect mobility at V_{ds}=1 V is extracted to be 10-15 $cm^2 V^{-1} s^{-1}$ before depositing the halfnium oxide (HfO_2).

Although single-layer MoS_2 FETs exhibits high on/off current ratio and low off-state current, which is important for minimizing the loss in the devices when they are turned off, it can only supply a very limited amount of current when the device is turned on (only 2.5 μA/μm at V_{ds}=0.5 V as reported in ref. [27]). Since the speed of a logic circuit is often determined by the ratio between the charge required to change the voltage across the various capacitances in the circuits and the current that can be supported by the transistors, the low on-state current in single-layer MoS_2 may limit the operation speed of any electronic systems constructed from this material. On the other hand, by increasing the number of MoS_2 layers, the on-state current of MoS_2 FETs can be increased significantly (close to 20 μA/μm at V_{ds}=0.5 V V_{tg}=2 V for bilayer MoS_2 in this work) with only small degradation in terms of on/off current ratio. For these reasons, we select bi-layer MoS_2 thin film as the material on which we demonstrate integrated logic circuits. For real electronic applications in the future, the selection of the number of layers may depend on the type of application. If better frequency performance is needed, then multi-layer MoS_2 may be used. If ultra-low power performance is necessary, then single-layer MoS_2 may be a better choice. And bi-layer and tri-layer MoS_2 thin films may offer good trade-off in between. In short, the

capability to control the number of molecular layers in the 2D crystal and the consequent control of the electronic properties enables added flexibility in this material system. In the future, it may be possible to build integrated circuits where different sections of the IC use different number of layers of MoS_2 thin films. The high performance sections (e.g. analog to digital converters, high speed oscillators) can use multilayer MoS_2 thin films while the low loss section (e.g. memory units) can use fewer layers of MoS_2 thin films.

Work function Difference between Al and Pd

To build both depletion-mode and enhancement-mode FETs on the same sheet of MoS_2, we have used metals with different work functions, w_M, as the gates to control the threshold voltages of the FETs. Figure 6-4 shows the band diagram of FETs with gate metal work function either greater than the semiconductor work function, i.e. $w_M > w_S$, or smaller than the semiconductor work function, i.e. $w_M < w_S$. A low work function metal tend to induce electrons in the channel, tuning the channel to the charge accumulation regime; while a high work function metal can induce the channel into the charge depletion regime, all at zero gate bias. For the Al-gate and Pd-gate MoS_2 FETs reported in this work, the shift in threshold voltage is around 0.76 V, which changes the threshold voltage from negative to positive and confers MoS_2 both enhancement-mode and depletion-mode FETs (Figure 6-3(c) and Figure 6-3(d)).

The difference between the work functions of two metals on a dielectric is generally different from that in vacuum. This phenomenon may be characterized quantitatively by the *S* coefficient, which accounts for dielectric screening. It can be calculated as the ratio between the effective metal work-function difference on a dielectric to that in vacuum:

$$\Phi_{M,eff} = \Phi_{CNL,d} + S \, (\Phi_{M,vac} - \Phi_{CNL,d})$$

where $\Phi_{M,eff}$ is the effective work function of the metal in a dielectric and $\Phi_{M,vac}$ is the work function of the same metal in vacuum. $\Phi_{CNL,d}$ is the charge neutrality level of the dielectric. The difference between the effective work functions of two metals can then be related to their difference in vacuum: $\Delta\Phi_{M,eff} = \Delta\Phi_{M,vac}$. Since $\Delta\Phi_{M,eff}$ and $\Delta\Phi_{M,vac}$ are about 0.76 and 1.04 eV, respectively, we have S~0.7 for the metals on HfO_2, which agrees closely with the value reported in ref. [261].

(a)

(b)
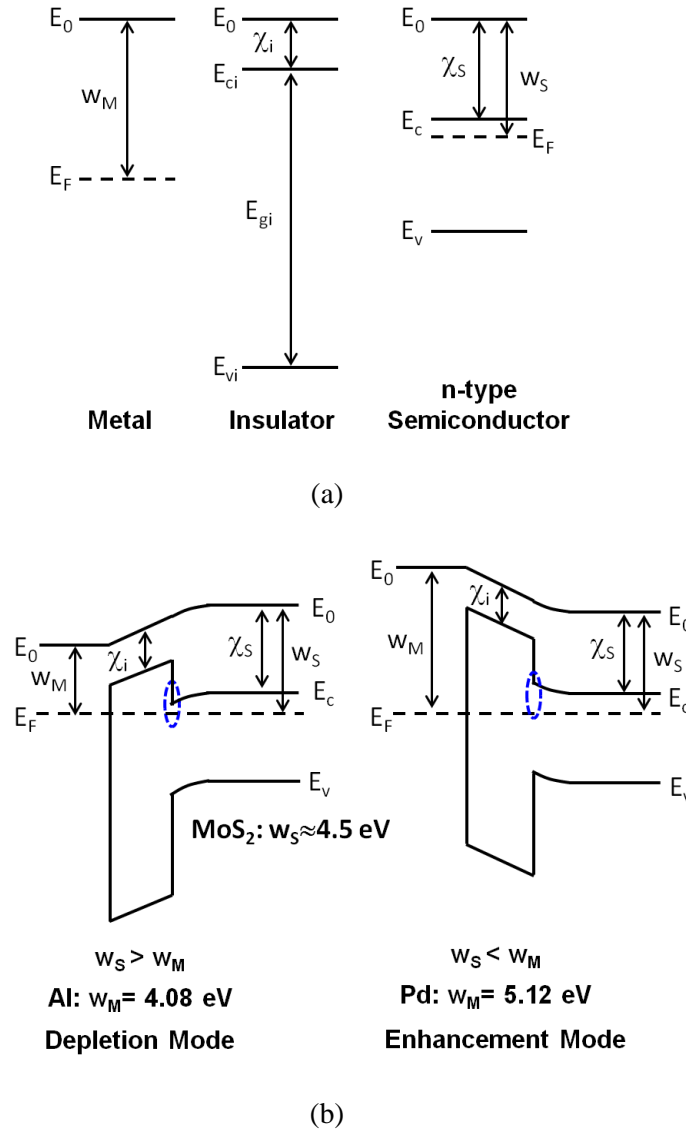
Figure 6-4 Energy band diagrams for enhancement mode and depletion mode transistors. Energy band diagrams (a) for isolated metal, insulator and semiconductor, and (b) after bringing them in intimate contact and thermal equilibrium is established. Depending on the different pairing of metal and semiconductor work functions, the metal-oxide-semiconductor (MOS) structure can induce the channel into either accumulation regime (for depletion mode FET) or depletion regime (for enhancement mode FET).

6.2. Integrated Circuits based on Exfoliated Bi-layer MoS$_2$

In this section, we address a key challenge in the development of 2D nanoelectronics by demonstrating the first fully integrated multi-stage circuits entirely assembled on few-layer MoS$_2$. These circuits are based on the development of a direct-coupled FET logic (DCFL) [262]

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in this material system, for which both enhancement-mode and depletion-mode devices with excellent pinch-off and current saturation are necessary. All the circuits were fabricated on bilayer MoS_2 obtained from micro-mechanical cleavage. Bilayer MoS_2, as discussed in the previous sub-section, offers an excellent trade-off between the off-state and on-state current levels.

Using the technology described above, we built four different integrated logic circuits entirely assembled on bilayer MoS_2: a logic inverter, a NAND gate, a static random access memory (SRAM) cell, and a 5-stage ring oscillator, all constructed with DCFL technology [100][262]. For each of the four logic circuits, all active and passive elements are integrated on the same piece of bilayer MoS_2. It is found that a supply voltage of $V_{dd}=2$ V is suitable for operating the fabricated circuits. Hence, in this letter, a voltage level close to 2 V represents the logic state 1 while a voltage level close to 0 V represents the logic state 0.
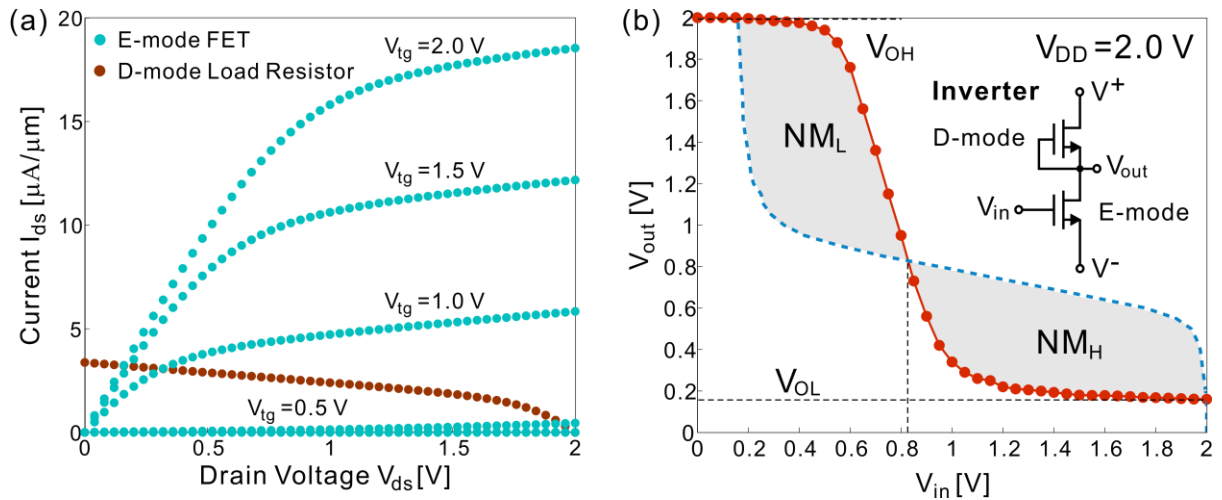
Figure 6-5 Demonstration of an integrated logic inverter on bilayer MoS_2 (a) Output characteristics (I_{ds}-V_{ds}) of the E-mode FET and D-mode load for the inverter shown in Figure 6-7(a). L_g=1 μm and L_{ds}=1 μm. For the E-mode FET, in the linear regime at small source-drain voltages, the current is proportional to V_{ds}, indicating that the source and drain electrodes made of Ti/Au metal stack forms ohmic contact with MoS_2. The current saturates at higher drain bias ($V_{ds}>V_g$-V_t) due to the formation of depletion region on the drain side of the gate, as is typical of long channel MOSFETs. (b) Output voltage as a function of the input voltage, and its mirror reflection, for a bilayer MoS_2 logic inverter. The shaded area indicates its noise margins (NM_L and NM_H) for logic operation. The gain of the inverter is close to 5. (Inset) Schematic of the electronic circuit for a logic inverter.

An inverter circuit is a basic logic element that outputs a voltage representing the opposite logic-level to its input. Our inverter was constructed from an enhancement-mode MoS_2 transistor, and a depletion-mode resistor that was formed by connecting the gate of a depletion-mode transistor directly to its source electrode (Figure 6-5(b) inset and Figure 6-7(a)). The quality of a logic inverter is often evaluated using its voltage transfer curve (Figure 6-5(b)), which is a plot of input vs. output voltage. When the input voltage is V_{in}=2 V (logic state 1), the E-mode MoS_2 FET is much more conductive than the depletion-mode FET, setting the output voltage to below 0.2 V (logic state 0). When V_{in} is 0 V (logic state 0), the MoS_2 FET is non-conducting and the output is close to 2 V (logic state 1). The slope of the transition region in the middle provides a measure of the gain - or the quality of switching. In the circuit of Figure 6-5(b), a voltage gain close to 5 is achieved. Figure 6-5(b) also shows the mirror reflection of the V_{in}-V_{out} characteristics, which highlights the robustness of the inverter towards noise for multi-stage operations. When multiple inverter stages are cascaded together, the output signal from the previous stage becomes the input signal to the next stage. Hence, the shaded area (NM_L and NM_H) represents the noise margin that can be tolerated by the inverter for multi-stage operations, which is particularly important for the demonstration of the ring oscillator.
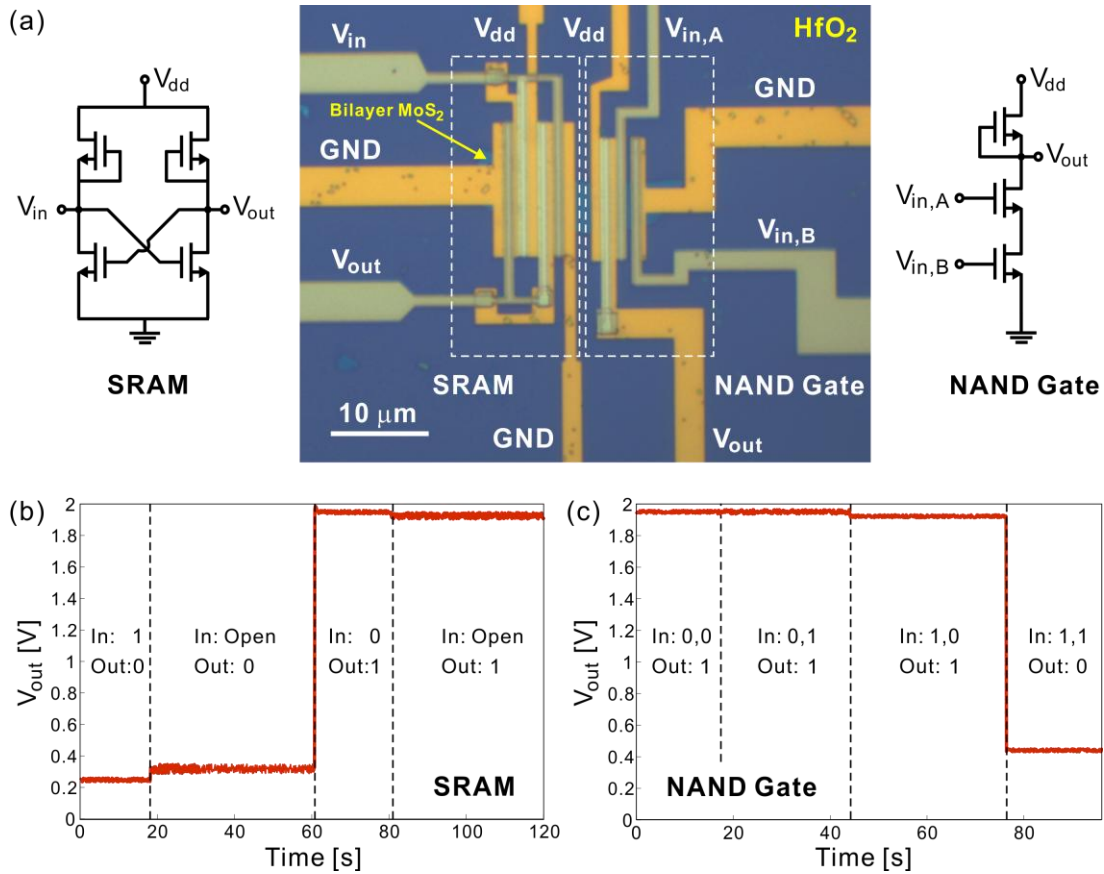
Figure 6-6 Demonstration of an integrated NAND logic gate and a static random-access memory (SRAM) cell on bilayer MoS$_2$ (a) Optical micrograph of the NAND gate and the SRAM fabricated on the same bilayer MoS$_2$ thin film. The corresponding schematics of the electronic circuits for the NAND gate and SRAM are also shown. (b) Output voltage of the flip-flop memory cell (SRAM). A logic state 1 (or 0) at the input voltage can set the output voltage to logic state 0 (or 1). In addition, the output logic state stays at 0 or 1 after the switch to the input has been opened. (c) Output voltage of the NAND gate for four different input states: (0,0), (0,1), (1,0), and (1,1). A low voltage below 0.5 V represents a logic state 0 and a voltage close to 2 V represents a logic state 1.

The schematic design and the optical micrograph of an NAND gate circuit fabricated on a sheet of bilayer MoS$_2$ are shown in Figure 6-6(a). The output of the circuit is close to 2 V (logic state 1) when either or both of the inputs are at logic state 0 (V_{in} <0.5 V). Under this state, at least one of the MoS$_2$ FETs is non-conducting and the output voltage is clamped to the supply voltage V_{dd}. The output is at logic state 0 only when both inputs are at logic state 1, so that both MoS$_2$ FETs are conducting. In Figure 6-6(c), the output voltage is measured as a function of time while the two input voltage states vary across all four possible logic combinations (0,0), (0,1), (1,0), and (1,1). This data demonstrates the stable NAND gate functions of this two-transistor

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bilayer MoS$_2$ circuit. A NAND gate is one of the two basic logic gates (the other being NOR gate) with universal functionality. Any other type of logic gates (AND, OR, NOR, XOR, etc.) can then be constructed with a combination of NAND gates. Hence, this first demonstration of a NAND gate shows that it is possible to fabricate any kind of digital integrated circuit with MoS$_2$ thin film layers.

A flip-flop memory element (SRAM) has also been constructed from a pair of cross-coupled inverters (Figure 6-6(a)). This storage cell has two stable states at the output, which are denoted as 0 and 1. The flip-flop cell can be set to logic state 1 (or 0) by applying a low (or high) voltage to the input. To verify the functionality of this flip-flop cell, a voltage source is applied to the input to set V_{in} to 2 V at time T=0 s. This drives V_{out} into logic state 0 (Figure 6-6(b)). Then at T=20 s, the switch at V_{in} is opened and the output of the SRAM cell V_{out} remains at logic state 0. At time T=60 s, we apply V_{in}=0 V at the input to write a logic state 1 into V_{out}. As the switch is opened again at T=80 s, the output of the SRAM cell remains in the logic state 1. This data demonstrates that the flip-flop SRAM circuit fabricated on the bilayer MoS$_2$ thin film indeed functions as a stable memory cell.

Finally, a 5-stage ring oscillator was constructed to assess the high frequency switching capability of MoS$_2$ and for evaluating the material's ultimate compatibility with conventional circuit architecture [262][263][264][265] (Figure 6-7(a)). The ring oscillator, which integrates 12 bilayer MoS$_2$ FETs together, was realized by cascading five inverter stages in a close loop chain (Figure 6-7(b)). An extra inverter stage was used to synthesize the output signal by isolating the oscillator operation from the measurement setup to prevent the interference between them. The output of the circuit was connected to either an oscilloscope or a spectrum analyzer for evaluation. The voltage transfer curve of the test inverter circuit fabricated side-by-side on the same piece of bilayer MoS$_2$ thin film (Figure 6-5(b) and Figure 6-7(a)) as the ring oscillator, shows that the gain in each inverter stage is close to 5. For robust ring oscillator performance, it is imperative to have stable operations in all five inverter stages throughout the oscillation cycles, and its tolerance towards noise can be determined from the noise margins for both low and high logic levels, i.e. the shaded regions in Figure 6-5(b). The positive feedback loop in the ring oscillator results in a statically unstable system, and the voltage at the output of each inverter

stage oscillates as a function of time (Figure 6-7(c)). At V_{dd}=2 V, the fundamental oscillation frequency is at 1.6 MHz, corresponding to a propagation delay of $\tau_{pd} = 1/(2nf) = 62.5$ ns per stage, where n is the number of stages and f is the fundamental oscillation frequency. The frequency performance of this ring oscillator, while operating at a much lower $V_{dd,}$ is at least an order of magnitude better than the fastest integrated organic semiconductor ring oscillators [264]. It also rivals the speed of ring oscillators constructed from the printed ribbons of single-crystalline silicon reported in the literature [266]. The output voltage swing measured by the oscilloscope (input impedance 1 MΩ) is about 1.2 V.

The output signal of the ring oscillator can also be measured in terms of its frequency power spectrum. Figure 6-7(d) shows the spectrum of the output signal from the ring oscillator as a function of the drain bias voltage V_{dd} (Figure 6-7(d)). The resonance frequency is at 0.52 MHz for V_{dd}=1.15 V. The corresponding fundamental resonance frequency reaches 1.6 MHz as V_{dd} increases to 2 V. The improvement in frequency performance with increasing V_{dd} can be attributed to the enhancement in the current driving capability of the ring oscillator due to the rise in the drain current I_{ds} in each individual MoS$_2$ FET with increasing drain and gate voltages. The fundamental frequency of oscillation is currently limited by the parasitic capacitances in various parts of the circuit rather than the intrinsic performance of the MoS$_2$ devices. The signal peaks measured by the spectrum analyzer increases from –65 dBm to -46 dBm as V_{dd} raises from 1.15 V to 2V. This is again a result of the I_{ds} dependence on V_{dd}.
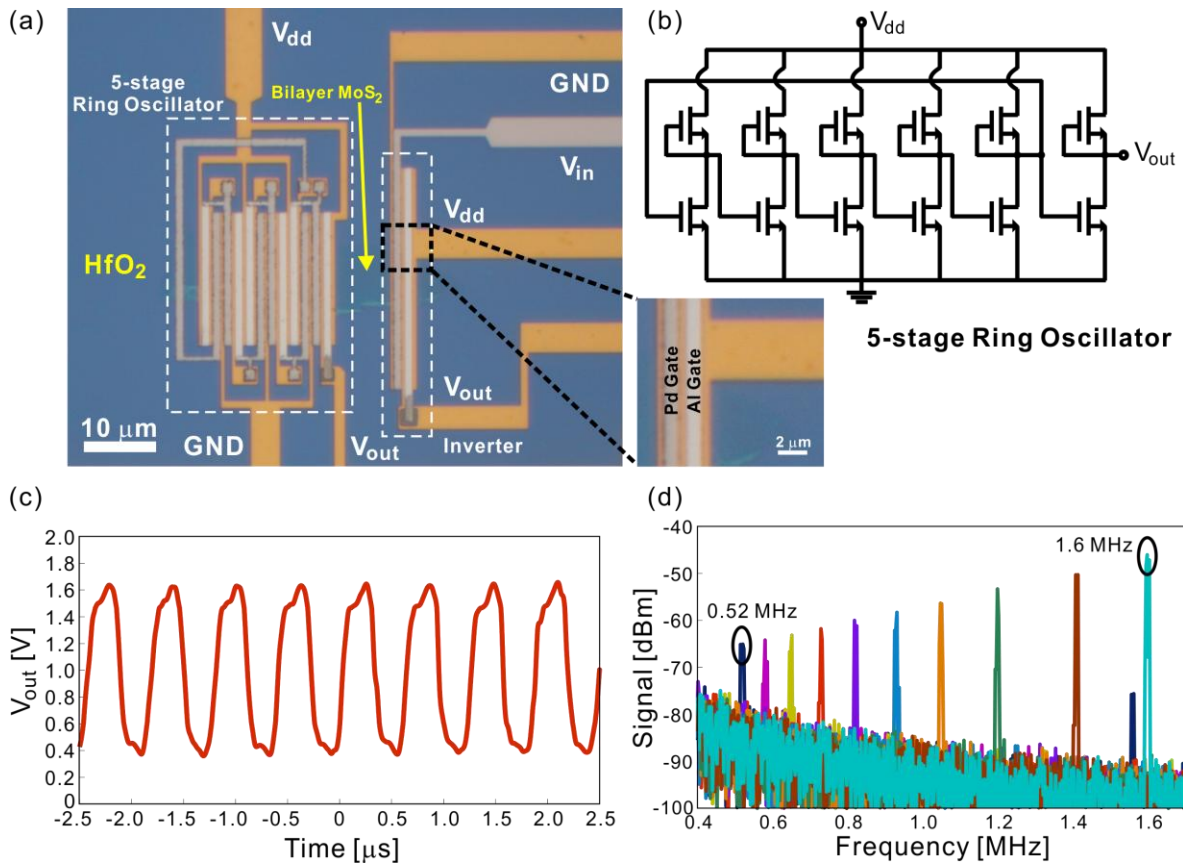
Figure 6-7 A 5-stage ring oscillator based on bilayer MoS_2. (a) Optical micrograph of the ring oscillator constructed on a bilayer MoS_2 thin film. (b) Schematic of the electronic circuit of the 5-stage ring oscillator. The first five inverter stages form the positive feedback loop, which leads to the oscillation in the circuit. The last inverter serves as the synthesis stage. (c) Output voltage as a function of time for the ring oscillator at V_{dd}=2 V. The fundamental oscillation frequency is at 1.6 MHz. The corresponding propagation delay per stage is 62.5 ns. (d) The power spectrum of the output signal as a function of V_{dd}. From left to right, V_{dd}= 1.15 V, and 1.2 to 2.0 V in step of 0.1 V. The corresponding fundamental oscillation frequency increases from 0.52 MHz to 1.6 MHz.

Estimation of the Ring Oscillator Speed

We can estimate the expected oscillation frequency for the ring oscillator at V_{dd}=2 V based on the parasitic capacitances present at various parts of the circuit and the driving current supported by the FETs as follows [262][265]:

a. The average driving current I_{ds} can be estimated from Figure 6-5(a). Each inverter stage operates along the load line defined by the depletion-mode FET. Since the width of the FETs in the ring oscillator circuit is about 11 µm, we have $I \approx 22$ µA for V_{dd}=2 V.

The parasitic capacitance in the circuit is mainly contributed by two parts:

b. capacitances due to the overlap area between the top gate layers (M2 and M3) and the source/drain layer (M1). This capacitance is mainly due to the gate capacitance of the 12 FETs in the circuit as well as the overlap between the interconnects in the gate metal layers (M2 and M3) and that in the M1 layer. The gate capacitance of the 12 FETs are estimated based on their device width (about 11 µm on average for each FET), and their gate length (1µm for each FET) with 20 nm HfO_2 (dielectric constant ~22) as the dielectric material. This leads to capacitances of 1.285 pF. The remaining overlap area between the interconnects is around 5.3 µm^2, which gives an additional 0.051 pF. The total gate overlap capacitance is hence:

$$C_{ov\_gate} = 1.336 \text{ pF}$$

c. capacitances contributed by the conductive Si substrate with 285 nm SiO_2:

$$C_{ov\_Si} = 2.138 \text{ pF}$$

Hence, the estimated total parasitic capacitances per stage is equal to:

$$C \approx (C_{ov\_gate} + C_{ov\_Si})/6 = 0.579 \text{ pF}$$

The propagation delay per stage is estimated to be: $\tau_{pd} = CV_{dd}/I = 52.6$ ns.

Thus, at V_{dd}=2 V, the expected frequency for a 5-stage ring oscillator is equal to: $f = 1/(2n\tau_{pd}) = 1.9$ MHz. This is very close to the measured value of the oscillation frequency, which is 1.6 MHz.

Figure 6-8 compares the MoS_2 ring oscillator with ring oscillators that have been demonstrated in other material systems proposed for large-area low-cost electronics. For good ring oscillator performance, it is desirable to have high oscillation frequency for performance and low operating voltage to minimize power consumption. MoS_2 based ring oscillator clearly offers significant advantages over ring oscillators demonstrated on other material systems, such as organics, large area CNT and ZnO. The MoS_2 ring oscillator also offers similar frequency performance, but with

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less than half of the operating voltage needed comparing to single crystalline Si ribbon ring oscillators. The only data point that shows better performance is a ring oscillator demonstrated on an individual piece of carbon nanotube, which however is not really a scalable technology.
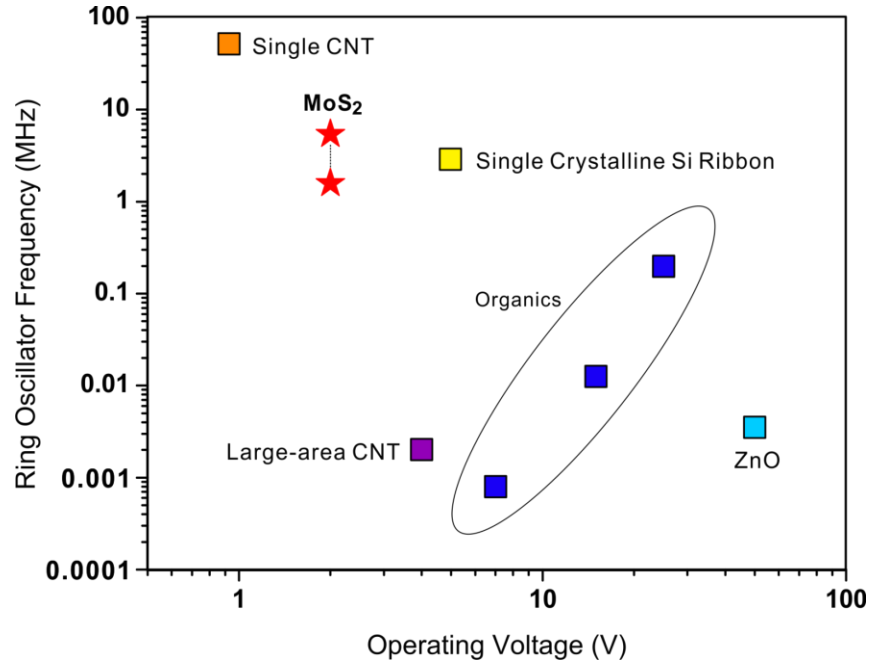
Figure 6-8 Comparison of bilayer MoS$_2$ ring oscillator performance with ring oscillators demonstrated in other material systems that have been proposed for large-area low-cost electronics.

To summarize, the realization of fully integrated multi-stage logic circuits based on few-layer MoS$_2$ DCFL represents the first demonstration of integrated multi-stage systems on any 2D materials, including graphene. It is an important step towards realizing 2D nanoelectronics for high performance low-power applications. Further optimization is underway to increase operating speed, and towards realizing complementary logic circuits to decrease the power dissipation. With the rapid progress in large-scale growth of MoS$_2$ by chemical vapor deposition [148][157], these 2D crystals are extremely promising new materials for both conventional and ubiquitous electronics.

6.3. Large-area 2D Electronics based on Single-layer CVD MoS$_2$

In the first half of this chapter, we have demonstrated the device and circuit technology based on exfoliated MoS$_2$ flakes. For 2D materials to become truly useful, it is important that the

technology should scalable, in terms of both the material availability and the device technology. The synthesis method for obtaining large-area CVD single-layer MoS_2 has already been discussed in Chapter 2. In this section, we present the device and circuit technology based on these CVD grown material to address the scalability issue of 2D electronics based on single-layer MoS_2.

6.3.1. Mobility and Metal Contacts for CVD Single-layer MoS_2

Measurements of the mobility in bulk MoS_2 dates back to the 50s and 60s of the last century where mobility up to 600 cm^2/V.s has been reported at room temperature. While the material in its bulk form is readily available in their natural minerals and is a popular option as industrial rubricant, the successful isolation of the material in its single-layer form is not reported until 2005 [37]. The earlier reports of carrier mobility in single-layer MoS_2 use the 2-probe technique that extracts the mobility from field-effect transistor device structures. The results from 2-probe measurement includes error due to the effects of contact resistances, often leading to an underestimate of the actual mobility that has been explained in Chapter 3. Figure 6-9 shows the mobility that is extracted on the same CVD single-layer MoS_2 samples where the contacts are made with various metals. The nature of the contact has a clear effect on the extracted mobility.
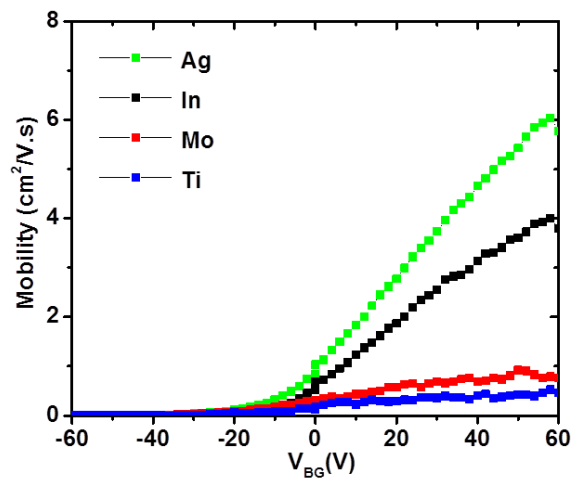
Figure 6-9 Mobility of CVD single-layer MoS_2 measured by 2-probe method using different metals for source and drain contacts

The nature of carrier injection from the metal to 2D materials depend on many different factors, including but not limited to the mismatch of work function between the two, the strain at the interface, mobility and doping of the 2D materials underneath the metal contacts, the quality of the interface. Matching the work function between the metal and MoS_2 is important for achievieng ohmic contact between the two.

Table 6-2 lists the workfunction of various metals that can be used for contacting MoS_2 and their respective work-function in vacuum. Since n-doped MoS_2 has work function around 4.7 eV, a high work function metal tend to enhance p-type carrier injection and a low work function metal tend to facilitate n-type carrier injection.

Figure 6-10 shows the normalized drain current flowing through back-gated devices with identical geometry and MoS_2 channel, but with different metal contacts including Ag, In, Mo and Ti. The four devices also show similar threshold voltages due to similar initial doping level after growth. Since the devices are otherwise identical, the only difference in conductivity is introduced by the different contacts. All the four metals provide ohmic contact to the as grown CVD single-layer MoS_2 (Figure 6-11). It is clear that Ag and In provides the best contacts to the single-layer MoS_2 while the contact resistance dominates current flow in devices with Mo and Ti contacts. There is no clear correlation between the nominal work function of these metals and the contact resistance. This may be due to the fact that the work function of the metals on MoS_2 surface can be very different from their respective nominal value in vacuum. The interface quality and possible strain at the interface may also play significant role in affecting the contact ressitance. The detailed study of the mechanism of carrier injection from the 3D lattice of the metal to the 2D lattice of the MoS_2 will be topic for future studies.

Metal	Y	Sc	In	Ti	Ag	Mo	Ni	Au	Pd	Pt
Φ_M (eV)	3.1	3.5	4.1	4.3	4.3	4.6	4.7	5.2	5.4	5.6

Table 6-2 Work function of different metals
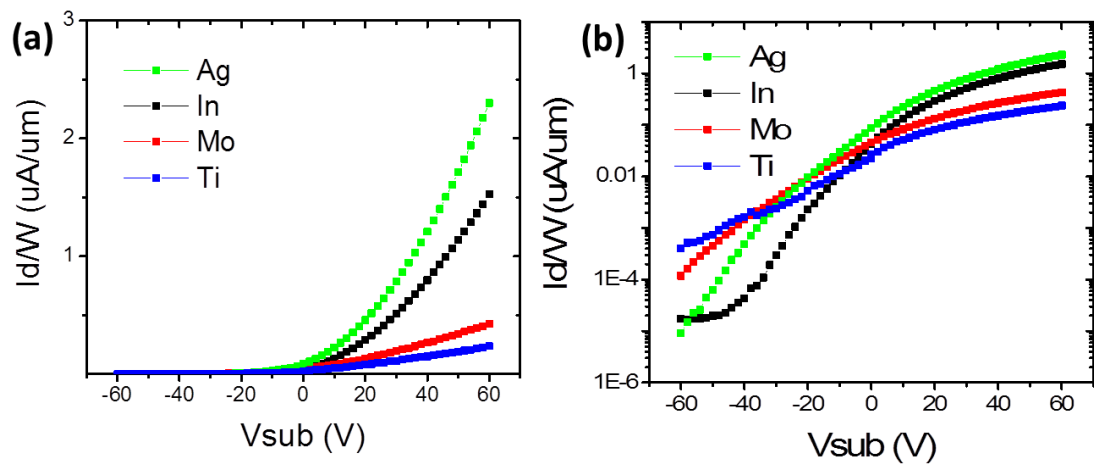
Figure 6-10 Transfer characteristics of CVD signel-layer MoS$_2$ transistors with Ag, In, Mo and Ti contacts (a) linear scale (b) logarithmic scale.
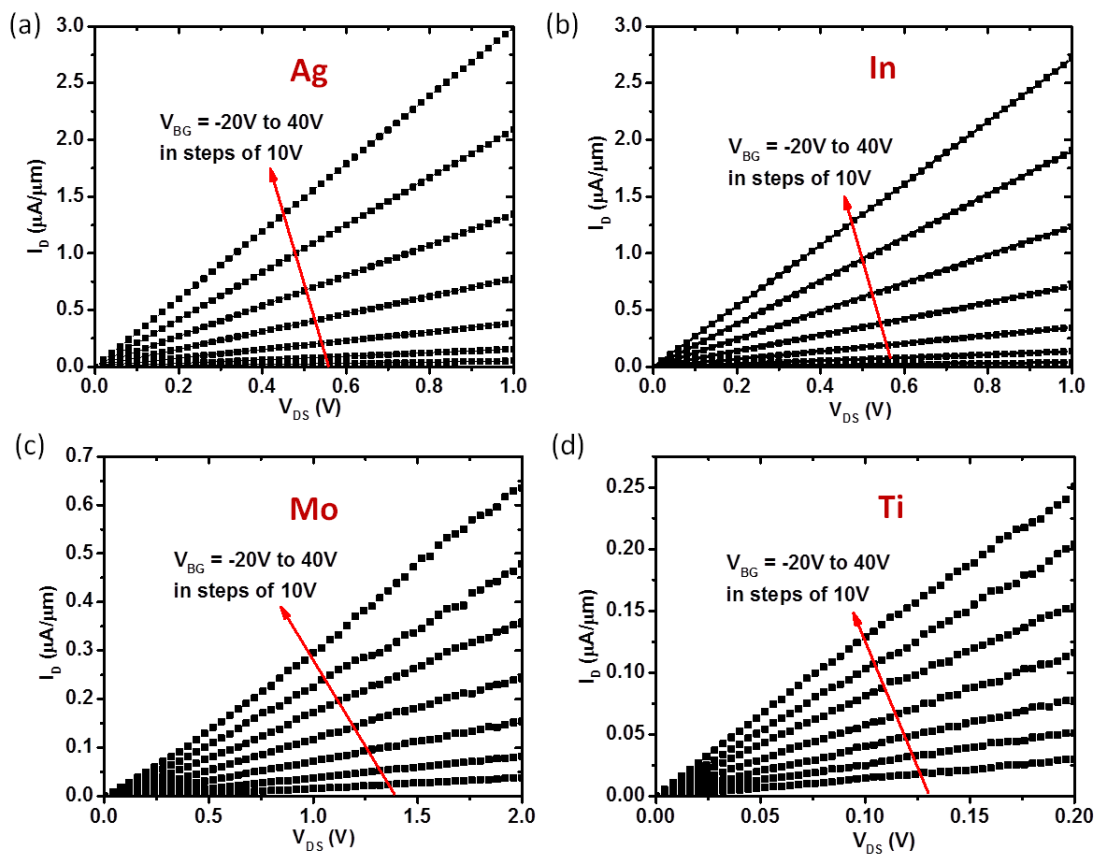
Figure 6-11 Output characteristics of CVD signel-layer MoS$_2$ transistors with Ag, In, Mo and Ti contacts (a) Ag contacts (b) In contacts (c) Mo contacts (d) Ti contacts

For metals with larger work functions such as Ni and Au, Shottkey junctions will be formed when they come in contact with MoS_2 due to the much larger work function mismatch compared to Ag, In, Mo and Ti metal introduced earlier. Figure 6-12(a) and Figure 6-12(d) show the temperature dependent conductivity measurements for two top-gated single-layer MoS_2 transistors. The current following through a Shottkey junction can be described by the following equation:

$$I_d = AT^2 \exp\left(\frac{q\Phi_B}{\kappa_B T}\right) [1 - \frac{\exp(-qV_{DS})}{\kappa_B T}]$$

where I_d and V_{DS} are the drain current and drain-source bias, Φ_B is the Shottkey barrier, T is the temperature, κ_B is the Boltzman constant and A is a constant value.

By dividing both sides by T^2 and taking logarithm, we have

$$\ln\left(\frac{I_d}{T^2}\right) = \frac{q\Phi_B}{\kappa_B T} + \ln(A) + \ln\left(1 - \exp\left(-qV_{DS}/\kappa_B T\right)\right)$$

Hence, the slope of the $\ln\left(\frac{I_d}{T^2}\right)$ versus $\frac{q\Phi_B}{\kappa_B T}$ plot will give the Shottkey barrier height (SBH), assuming φ_B does not have a temperature dependence. The Shottkey barrier limited carrier injection is dominant in the temperature range above 250 K. This is shown in Figure 6-12(b) and Figure 6-12(e). For lower temperature, the carrier injection is more dominated by tunneling processes, which shows negligible temperature dependence. From the data above 250 K in Figure 6-12(b) and Figure 6-12(e), we can extract the Shottkey barrier height. Figure 6-12(c) and Figure 6-12(f) show the extracted SBH with respect to the gate bias that modulates the single-layer MoS_2, leading to a clear trend of decreasing SBH when the bias becomes more positive. For both Ni and Au contacts, the SBH can reach close to 150 meV at V_{TG}=0 V. This technique may be insufficient, or at least not accurate enough, for extracting the SBH in Ag, In, Mo and Ti where the SBH is much lower due to better work function match and is hence much more difficult to measure accurately.
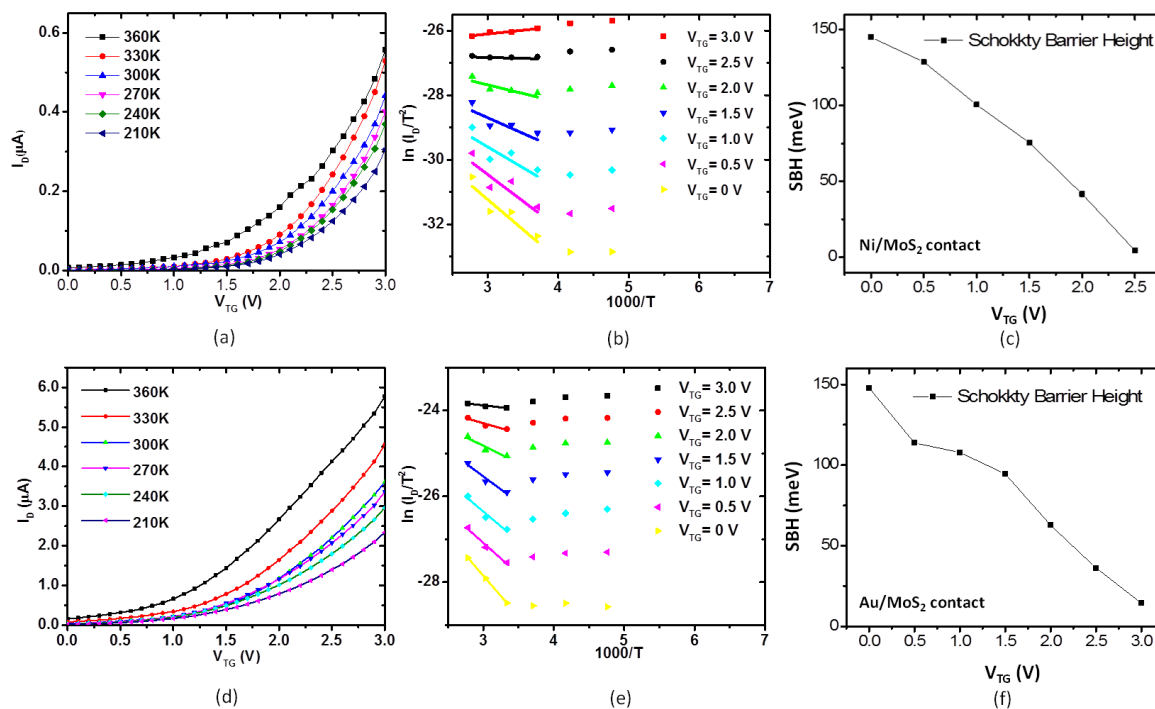
Figure 6-12 Characterization of Shottkey barrier height using temperature dependent I_D-V_{TG} measurement (a), (b), (c) Ni/MoS$_2$ contact; (d), (e), (f) Au/MoS$_2$ contact
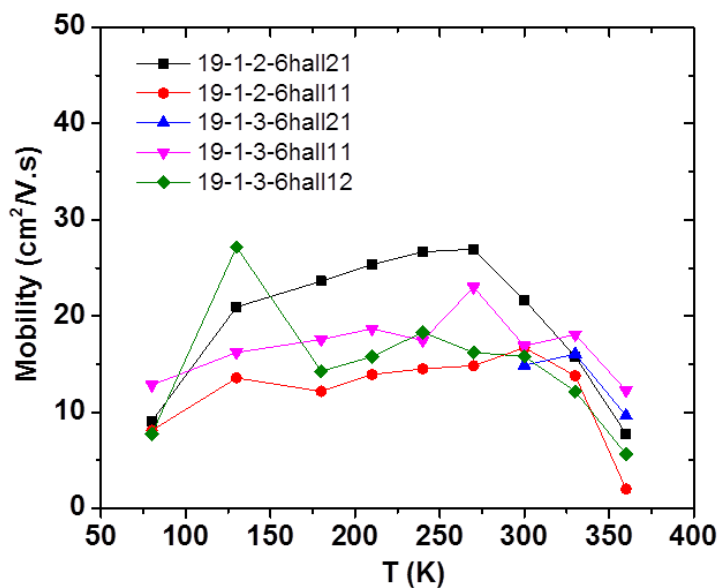
Figure 6-13 Temperature dependence of mobility in CVD polycrystalline single-layer MoS$_2$

Hence, in order to obtain a more accurate estimate of the carrier mobility in MoS_2, we need to exclude the effect of the contact resistance. 4-probe measurement offers a better technique for extracting the mobility that can exclude the effect of the contact resistances. Figure 6-13 shows the temperature dependence of the mobility measured by 4-probe method. We see two key features in the dependence of the mobility on temperature. At temperature above 250 K, the mobility is mainly limited by the optical phonon scattering [267][268][269][270]. As the temperature reduces, the phonon scattering becomes weaker and mobility increases. The mobility peaks at around 200 K before decreasing again at lower temperatures. It is believed that at lower temperature, the carrier may be attached to localized sites and the carrier transport relies on tunneling based mechanism between the localized energy minimums [268][269][270]. The room temperature mobility of these CVD grown polycrystalline single-layer MoS_2 can reach between 20 to 30 cm^2/V.s in most samples and is above 40 cm^2/V.s in the best samples.

6.3.2. FETs Based on CVD Grown Single-Layer MoS_2

Figure 6-16(a) shows the output characteristics of the fabricated single-layer MoS_2 FET with L_G=L_{DS}=1 μm. The device shows clear current saturation, which is due to the pinch-off of the channel at the drain side of the gate at high V_{DS} since the saturation voltage V_{sat} closely matches the gate overdrive V_{GS}-V_t. This is the first demonstration of current saturation in top-gated MoS_2 FETs, a crucial device characteristic that has been missing in previous reports of MoS_2 FETs [27]. The maximum on-state current reaches 16 μA/μm at V_{DS}=5 V and V_{TG}=2 V. The threshold voltage is at -2 V (Figure 6-16(b)), indicating that the material is unintentionally doped n-type during the growth and fabrication process. The peak transconductance is around 3 μS/μm. The classical drift-diffusion model [205] accurately fits the device characteristics (Figure 6-16(a) and (b)). Due to a larger bandgap than Si and excellent electrostatic control of 2D electronics, the device exhibits a remarkable on/off current ratio exceeding 10^8, giving the material great potential for ultra-low power applications such as driving circuits for flat panel display, where most of the incumbent materials - organics and amorphous Si - have mobility below 1 cm^2/V.s due to their intrinsic disorder and tunneling-based transport mechanism. In contrast, carrier mobility in this particular sample of polycrystalline CVD single-layer MoS_2 is extracted to be close to 30 cm^2/V.s at 300 K (Figure 6-13) while single-crystalline exfoliated multi-layer MoS_2

shows mobility around 150 cm^2/V.s at 300 K. Such mobility allows MoS$_2$ FETs to operate even at GHz frequency. Figure 6-16(c) shows the first RF performance characterization of MoS$_2$ FETs. This device with L$_G$=300 nm shows an f_T of 900 MHz and f_{max} of 1 GHz, giving MoS$_2$ the potential to enable high performance RF circuits on bendable substrates, such as flexible RFID tags.

6.3.3. Integrated Logic Circuits based on Single-Layer MoS$_2$

The demonstration of large-scale fabrication of integrated circuits based on CVD single-layer MoS$_2$ is described in this section. Figure 6-17 and Figure 6-18 show fully integrated inverters and NAND gates in depletion mode configuration. The inverters can operate under a wide range of V$_{dd}$ from 0.5 V to 5V with peak voltage gain close to 20 at V$_{dd}$=5 V (Figure 6-17(c)). Figure 6-18(c) shows the NAND gate performing logic function on two input signals. This demonstration of an NAND gate, one of the two types of universal logic gates (the other being NOR), shows that it is possible to realize any Boolean functions on CVD MoS$_2$ thin film.
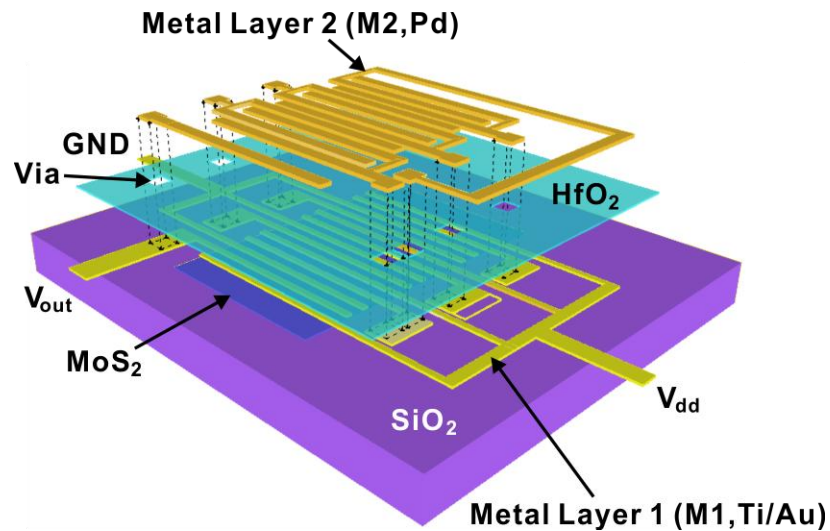
Figure 6-14 Schematic illustration of the fabrication process for building transistors and integrated circuits on MoS$_2$.

6.3.4. Integrated Mix-Signal Circuits based on Single-Layer MoS$_2$

Finally, to demonstrate the mixed-signal capability of MoS$_2$, a voltage comparator circuit is constructed (Figure 6-19(a)) based on a matched long-tail pair differential amplifier (Figure 6-

19(b)). Using the differential gain of the long-tail pair, the comparator converts a 1 kHz sinusoidal signal to a square wave, which is essentially a digital output with two logic levels. Any part of the input signal above (or below) the reference voltage V_{ref} is represented by logic level 0 (or 1) in the output signal V_1-V_2 (Figure 6-19(c)). The successful operation of the ADC also demonstrates the excellent matching between the characteristics of the various transistors used in the circuit, necessary for a successful differential amplifier.

Integrated devices and circuits based on large-scale single-layer MoS_2 grown by CVD are presented for the first time. The transistors fabricated on this material demonstrate excellent characteristics such as record mobility for CVD MoS_2, ultra-high on/off current ratio, record current density and GHz RF performance. The demonstration of both digital and analog circuits shows the remarkable capability of this single-molecular-layer thick material for mixed-signal applications, offering scalable new materials that can combine silicon-like performance with the mechanical flexibility and integration versatility of organic semiconductors.
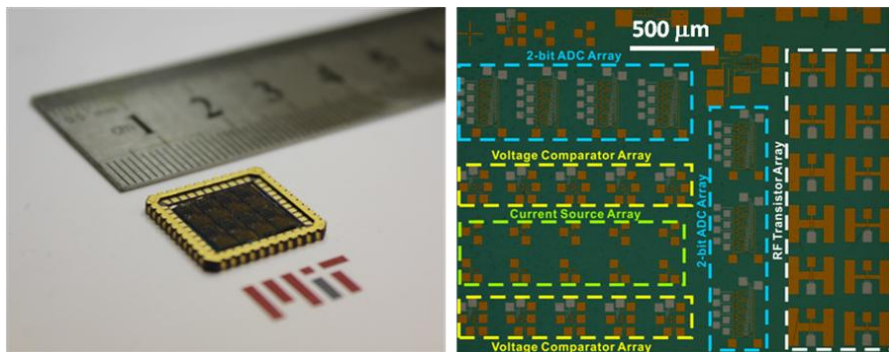
Figure 6-15 Large-scale single-layer MoS_2 chips (a) Transistors and integrated circuits fabricated at the wafer scale for the first time using single-layer MoS_2 grown directly on SiO_2/Si substrate by CVD methods. (b) Optical micrograph of the chip fabricated using CVD single-layer MoS_2 grown on SiO_2/Si substrate, showing arrays of RF transistors, currents sources, 1-bit and 2-bit analog-to-digital converters (ADC).
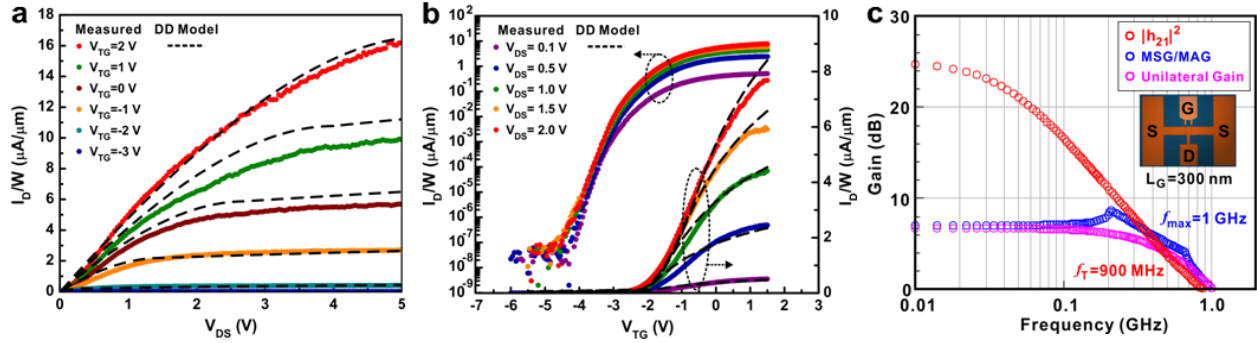
Figure 6-16 DC and RF characteristics of CVD single-layer MoS$_2$ FETs (a) Output characteristics of the FET fabricated on CVD single-layer MoS$_2$. The device shows excellent current saturation. L$_G$=L$_{DS}$=1 μm. V$_{BG}$=0 V. (b) Transfer characteristics in linear scale (right y-axis) and log scale (left y-axis). The on/off current ratio of the device exceeds 10^8, making these devices ideal for ultra-low power applications. The subthreshold swing is 110 mV/dec. V$_{BG}$=0 V. The classical drift-diffusion (DD) model (black dotted lines) [7] gives an excellent fit to the data in (a) and (b), indicating that the carrier transport in these devices are dominated by drift-diffusion and current saturation in (a) is due to channel pinch-off at the drain side of the gate, i.e. V$_{sat}$=V$_{TG}$-V$_t$, all similar to conventional long channel MOSFETs. (c) First RF characteristization of a MoS$_2$ FET. The measured device has L$_G$=300 nm. f_T=900 MHz and f_{max}=1 GHz. This demonstrates the high frequency potential of MoS$_2$ 2D-electronics compared to organic semiconductors and amorphous Si, opening doors for applications such as high performance RFID tags on flexible substrates. It should be noted that this measurement is performed in high vacuum (~10^{-6} Torr) to reduce hysteresis.
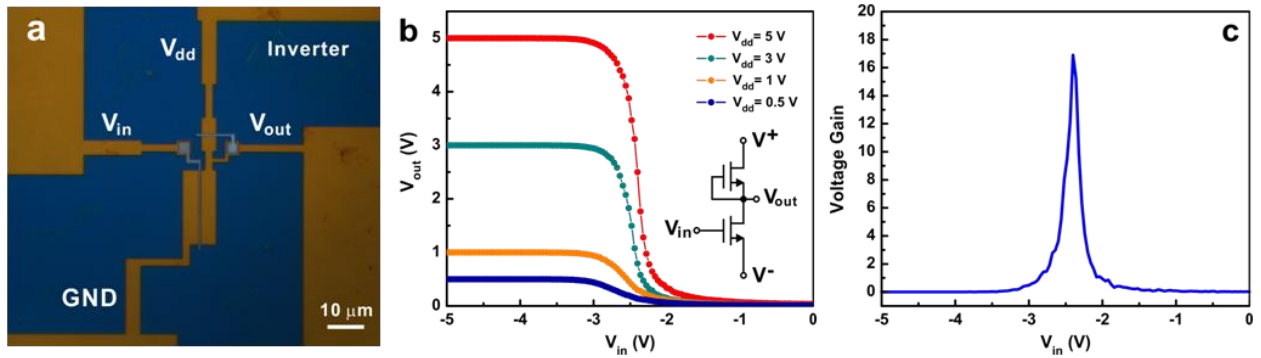
Figure 6-17 An inverter based on CVD single-layer MoS$_2$ (a) Optical micrograph of a fully integrated inverter constructed on single-layer MoS$_2$ (b) Input-output characteristics of the inverter as a function of supply voltage V$_{dd}$. The inverter operates on a wide range of V$_{dd}$ from 0.5 V to 5V. (c) Voltage gain of the inverter. At V$_{dd}$=5 V, the peak voltage gain of the inverter is close to 20.
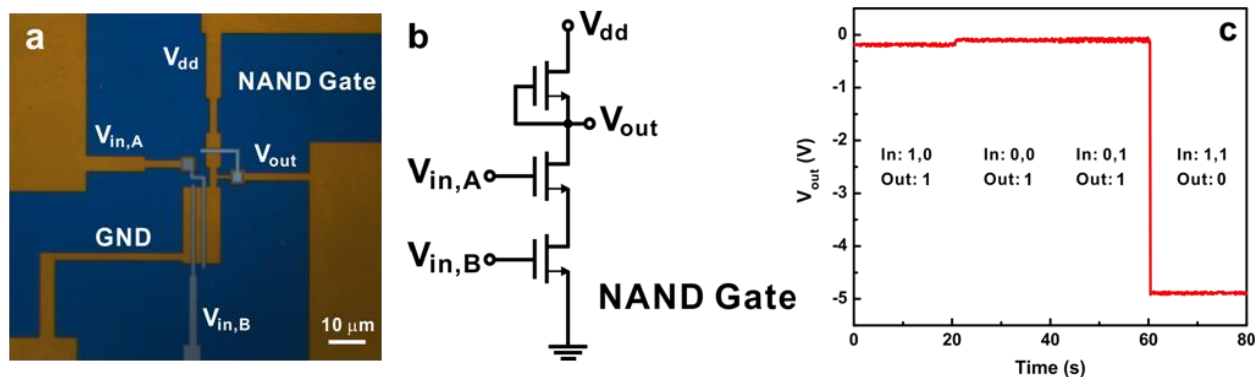
Figure 6-18 A NAND gate based on CVD single-layer MoS_2 (a) Optical micrograph of a fully integrated NAND gate constructed on single-layer MoS_2. (b) Schematic circuit for the NAND gate. (c) Output voltage of the NAND gate for four different input states: (1,0), (0,0), (0,1), and (1,1). A low voltage of -5 V represents a logic state 0 and a voltage close to 0 V represents logic state 1. This data demonstrates the stable NAND gate operation of this single-layer MoS_2 circuit. A NAND gate is one of the two basic logic gates (the other being NOR gate) with universal functionality. Any other type of logic gates (AND, OR, NOR, XOR, etc.) can then be constructed with a combination of NAND gates. Hence, this first demonstration of a NAND gate on CVD MoS_2 shows that it is possible to fabricate any kind of digital integrated circuit with MoS_2 thin film.
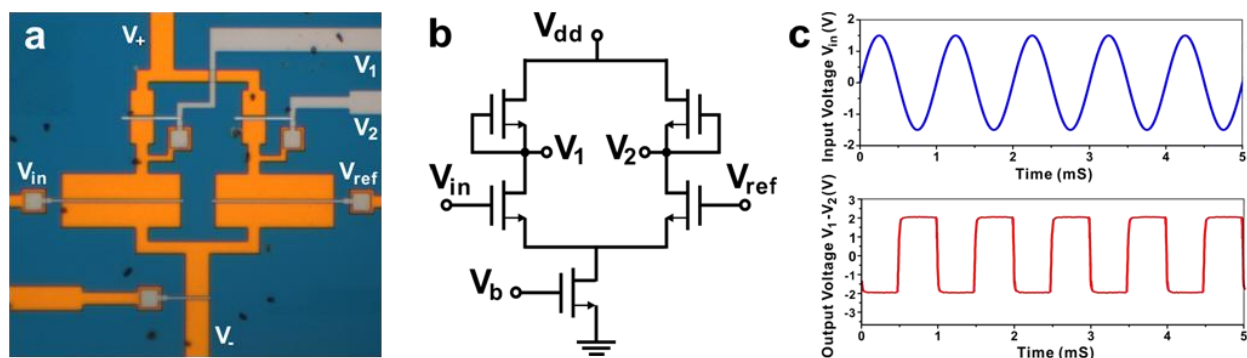
Figure 6-19 A voltage comparator based on CVD single-layer MoS_2 (a) Optical micrograph of a fully integrated voltage comparator, which is a key building block for analog to digital converters (ADC), constructed on single-layer MoS_2. (b) Schematic circuit for the voltage comparator. (c) AC coupled oscilloscope reading of the input and output signals (1 kHz) of the ADC. The ADC is essentially a voltage comparator based on a differential amplifier with matched long-tail pair configuration, which requires well-matched characteristics in the transistors involved. When the input voltage V_{in} is above (or below) the reference voltage V_{ref}, the output voltage is at logic level 0 (or logic level 1). The high differential gain converts the analog input to a digital square wave. This circuit demonstrates for the first time the mixed-signal capability in circuits based on MoS_2, or any 2D material in general including graphene. The measurement is done at room temperature under high vacuum (~10^{-7} Torr).

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In this chapter, layered transition metal dichalcogenides in their single- and few-layer forms have been proposed for application in electronic systems. These materials offer significant advantages of possessing a sizable bandgap for logic applications while preserving many of graphene's benefits as an electronic material that come with their ultra-thin 2D geometry and electronic properties. Following the discussion of creating the 2D thin film by mechanical exfoliation and the CVD synthesis technique in Chapter 2, we demonstrated devices and circuit technology in this Chapter, addressing issues including the scalability of the technology. The results show that the material even in its current quality is already feasible for system level applications. Comparison of the device performance with transistors that have been demonstrated in other material systems also highlights the great potential of these new class of materials for application in high performance flexible electronics. Finally, it should be highlighted that the work on LTMD presented in this Chapter is really just a first step towards future applications. The technology is still in its infant stage while many exciting opportunities lie ahead.

Chapter 7. Conclusion, Challenges, and Future Work

7.1 Summary

In this thesis, we have addressed several key issues that are critical for the future application of two-dimensional materials in electronic and optoelectronic systems. First, we have studied the basic transport properties of graphene by characterizing its carrier mobility using various electrical and optical measurement techniques. We have developed the process for fabricating a wide range of electronic device structures based on graphene and analyzed its device level performance. A virtual source injection velocity model was also developed to describe the behavior of graphene transistors. Issues, such as current saturation in graphene transistors, are discussed. Second, a significant part of this thesis work focuses on the design, fabrication, characterization, and simulation of the graphene transistors targeting application at microwave frequency range. Here, we focus on improving the f_T, one of the most important figures of merit in high frequency performance and investigated them analytically and experimentally. Based on improved physical understanding and advanced process technologies, we have demonstrated state-of-the-art f_T above 60 GHz in graphene transistors. hBN/Graphene/hBN sandwich structures and T-gate self-aligned device structure are proposed to reduce the scattering and minimize the parasitics, leading to significant improvement in RF performance in the devices. A new method for analyzing the carrier transit delay in graphene RF FETs are proposed to understand the individual contributions from the parasitic, external and intrinsic part of the device to the total carrier transit delay, which provides valuable information for optimizing the device structure and understanding the intrinsic carrier dynamics in the GFETs. Third, during the course of this thesis, we have proposed for the first time an entirely new concept of *Ambipolar Electronics*. The novel concept allows many basic building blocks of analog systems, such as frequency multipliers, mixers and phase shift keying circuits, to be realized with much simpler circuitry than the conventional design using unipolar Si MOSFET devices. Finally, we also explored the electronic applications of new two-dimensional materials beyond graphene. In particular, the performance of electronic devices and basic circuits for logic and mixed-signal electronics based on MoS_2 are accessed. The MoS_2 monolayers are created both from exfoliation and chemical vapor deposition techniques. The later method also addressed the scalability issue

of this new material. This new class of transition metal dichalcogenides offers many exciting opportunities for constructing high performance flexible electronic systems with potential applications in wireless sensor networks and ubiquitous electronics.

7.1.1. Graphene Transistor Device Technology

In this part of the thesis, key technology challenges in fabricating graphene transistor devices are addressed, including the mobility, metal contacts and dielectric deposition. The key advantages of graphene as an electronic material lie in its extremely high carrier mobility. This critical property of graphene varies significantly depending on the graphene quality and the environment that encapsulates the material. As an important step towards developing successful device technology, the carrier mobility in CVD grown graphene is characterized in details using various techniques including Hall Effect measurements, field effect measurements and FT-IR characterization of the dynamic Drude conductivity. The carrier transport is dominated by optical phonon scattering at high temperature, and by charge impurity and short range scattering at low temperature.

The contact resistances of graphene transistors are characterized and optimized, achieving contact resistance below 200 $\Omega.\mu m$ at high graphene carrier density. To achieve the low contact resistance, an inorganic sacrificial layer based process has been developed in this thesis, which allows significant reduction of resist contamination. Graphene surfaces immediately following the process demonstrate reduced roughness with arithmetic and root-mean-square roughness, R_a and R_q, being 1.18 and 1.00 nm, respectively, in contrast to $R_a = 0.218$ nm and $R_q = 0.2$ nm using a conventional process. It is also found that keeping a clean surface for metal deposition and maintaining high conductivity in graphene underneath the metal is critical to achieving low contact resistances.

A virtual source carrier injection model is developed for understanding the behavior of ambipoalr graphene FETs, which can also be implemented in Verilog for circuit level simulations. The work is based on a model previously developed for short channel Si and III-V transistors. In this thesis, the original model was extended to handle ambipolar conduction in graphene. The resulting model can describe very well the GFETs characteristics with both top-

and bottom-gates. The model also allows the extraction of source carrier injection velocity, a critical parameter that is important for short channel devices.

7.1.2. High Speed Graphene Transistors for RF Applications

A key application of graphene explored in this thesis is transistor devices for electronic systems operating at microwave frequency. One of the important challenges to produce a RF electronics using graphene FETs is to increase their short circuit current gain cutoff frequency (f_T). Despite the fact that f_T is largely affected by several parasitic elements in the device such as R_i, R_s, R_d, C_{gs}, C_{gd}, and g_0, systematic study of these parasitic elements has seldom been done in the literature to improve f_T. Conventional wisdom for improving f_T was to reduce the channel length and most of the research efforts were focused on the device scaling. Contrary to the conventional approach, we first explore a new hBN/Graphene/hBN sandwich structure for RF applications. The new device structure uses two layers of hBN as both the dielectric and substrate for the graphene FETs. By sandwiching the grapheen between hBN layers, it help to preserve the high mobility of graphene by providing an ultra-flat surface in touch with graphene that is also free of dangling bonds. Comparing to a control device on SiO_2/Si substrate with Al_2O_3 as the gate dielectric, which has identical geometry, the hBN/Graphene/hBN device offers 90% improvement in transconductance due to higher channel mobility (6,500 cm^2/V.s extracted for the BN/Graphene/BN FET v.s. 1,200 cm^2/V.s in the control device). The carrier injection velocities are estimated to be about 3.5×10^7 cm/s in the BN/Graphene/BN FET comparing to only 2.5×10^7 cm/s in the control device.

The effects of parasitics on the RF performance of graphene FETs are also systematically studied in this thesis. In particular, a new method for extracting the contributions from intrinsic and parasitic parts of the device to the total carrier transit delay is developed. In this method, the S-parameters of the graphene FETs are first measured. Small signal circuit simulation is then done using Agilent Advanced Design System to extract the key components in the small signal circuit. The method then uses the scaling behavior of the gate capacitances to extract intrinsic and extrinsic capacitive parasitics of the device, from which the three delay components τ_{par}, τ_{ext} and τ_{int} can be obtained. We studied devices with gate length ranging from micrometers to 200 nm. The analysis reveals the parasitic components to be the key limitation of frequency

performance in non-self-aligned graphene FETs. It is also observed that the scaling trend of the delay time indicates the parasitic and external delays, τ_{par} and τ_{ext}, which accounts for larger proportions of the total delay especially at shorter gate length. The result points to the importance of reducing the parasitic effects for sub-100 nm GFETs.

With the understanding developed in the delay analysis, we tried to maximize f_T of graphene FETs by minimizing the detrimental effects from the parasitic elements. The combination of T-shape gate and self-aligned device structure produced a very low access resistance mostly dominated by the contacts. Also, a reliable deep-submicron T-gate ($L_g = 50$ nm, $H_g = 300$ nm) was fabricated to minimize both the gate resistance R_g. The T-gate also acts as the mask in the final metallization step for creating a self-aligned structure to reduce the access resistances of the device. As a result, we have obtained a state-of-the-art f_T of 60 GHz in a graphene FET with $L_g = 50$ nm.

Finally, we also clarified in detail the open-short de-embedding method for f_T extraction where a uniform standard needs to be established in literature. Here, two different designs of "open" pattern are compared. In the more "intrinsic" de-embedding method, the "open" pattern have its gate finger extending into the region between the source and drain electrodes while in the standard de-embedding method, the gate finger in the "open" pattern stops before reaching that region. This subtle difference can lead to substantial difference in the values of f_T extracted using open-short methods, primarily due to the exclusion of fringe capacitances when using the "intrinsic" method. For example, in the device with $L_g = 50$ nm shown in Figure 4-22, the standard de-embedding yields f_T=60 GHz while the "intrinsic" de-embedding method gives f_T=330 GHz. Although the "intrinsic" de-embedding method may provide a way to access the frequency performance of the "intrinsic" device region, it must be noted that this definition of "intrinsic device" deviates from our usual notion of intrinsic device region conventionally used in the study of Si and III-V transistors. The f_T value reported by the "intrinsic" method is close to the estimated values using $f_T = 1/2\pi\tau_{int}$. Clearly, both the parasitic delay τ_{par} and the external delay τ_{ext} are not accounted for when reporting the f_T value using this method. The discrepancy in f_T caused is particularly serious in short channel self-aligned FETs where the fringe capacitances can account for the major portion of the gate capacitances and potentially

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dominates the overall intrinsic gate capacitances. Hence, we must also be very careful when benchmarking the f_T values in graphene devices (60 GHz for L_g=50 nm) with those demonstrated in Si MOSFETs and III-V HEMTs [214][215][216], where the device research community only use the standard open-short de-embedding method as introduced in Chapter 4, or its equivalent, when reporting f_T values for these devices, not the "intrinsic" one in the way this term is used here.

7.1.3. Ambipolar Electronics based on Graphene

Another key contribution of this thesis comes from the first proposal of the new *Ambipolar Electronics* concept. For a long time, many people have seen the ambipolar conduction in carbon nanotube or graphene devices as a drawback for application in electronic systems. In contrast to the conventional wisdom, we proposed and demonstrated in this thesis how this unique property combined with the high mobility of graphene can benefit analog circuits in providing new opportunities for re-designing its many basic building blocks with greater simplicity, such as ambipolar frequency multipliers, mixers and phase shift keying circuits. Using graphene on sapphire RF FETs, a single-transistor ambipolar frequency multiplier has been demonstrated in this thesis, showing -3dB cut-off frequency at 17 GHz. The output is low in noise and harmonics where more than 93% of the RF output power is concentrated on the useful frequency. These new circuit designs can potentially work well at very high frequency due to the simplicity of the circuits allowed by the new concept and the high mobility graphene is able to offer. The frequency performance, the power gain and the effects of symmetry in GFET characteristics on the output power spectrum are also analyzed.

The ambipolar electronics concept is not limited to just the frequency multipliers, but can also be used to enable a wide range of other analog applications. Here, we also demonstrated a frequency mixer where the symmetrical quadratic nature of the graphene FET transfer characteristics can be used to improve the efficiency of second order harmonic generation at which the useful sum and difference frequencies lie, and reduce undesired odd order harmonics. The mixer shows an IIP3 point at 13.8 dBm with input at f_{RF}=10.5 MHz and f_{LO}=10 MHz. The conversion gain (loss) are between -40 and -35 dB. An ambipolar GFETs based binary phase shift keying device is also demonstrated in this work where the negative gain on the hole

conduction branch and the positive gain on the electron branch were used to introduce the 180° phase shift for modulating the digital information onto an analog carrier wave.

The key advantage offered by these circuits based on ambipolar devices derives mainly from its simplicity, which is extremely appealing for applications at very high frequency. While combining with the high mobility of graphene, they have great potential for application in high speed analog systems.

7.1.4. Single- and Few-layer MoS$_2$ Devices and Circuits

In the final part of this thesis, we investigated the device and circuit technology based on other two-dimensional materials, such as MoS$_2$. While graphene may be an excellent material for high frequency RF application, the lack of bandgap in graphene has led to several undesired features in the device characteristics, making GFETs unsuitable for logic applications. This includes the difficulty in switching off the device at room temperature and the lack current saturation in the devices. On the other hand, many members of the transition metal dichalcogenides family possess the bandgap that is suitable for logic applications. In this part of the thesis, we developed the basic technologies for fabricating single- and few-layer MoS$_2$ devices, including using exfoliation methods to obtain MoS$_2$ flakes, the contact technology using various metals and the ALD deposition of high-k dielectric. Bilayer MoS$_2$ FETs with on/off ratio exceeding 10^7, current saturation and on-state current density exceeding 20 µA/µm have been demonstrated. We also demonstrated the basic building blocks of logic circuits based on this material, including inverters, NAND gates, static random access memory devices and a 5-stage ring oscillator operating at 1.6 MHz with each MoS$_2$ transistor in the circuit having L_g=1 µm. The results show that LTMD based electronics can achieve superior performance over other material systems that have been proposed for ubiquitous applications, such as organic semiconductors, ZnO and large area carbon nanotube arrays. It also offers similar mobility, but superior on/off ratio when compared to Si thin film transistors.

A key challenge in the application of LTMD systems is its scalability. In this thesis, we addressed this issue by developing the device technology and understanding the device characteristics based on single-layer MoS$_2$ grown by chemical vapor deposition techniques. The mobility of the CVD material is characterized for the first time. This polycrystalline material

shows carrier mobility close to 30 cm^2/V.s at room temperature with mobility decreasing at both low and high temperatures. In our hypothesis, which is in line with explanation proposed in the literature, the decrease of mobility at high temperature is attributed to increased optical phonon scattering while the mobility degradation at low temperature is attributed to carriers being trapped at local energy minimum and the carrier movement transiting from band-like behavior to "hopping" based transport. The quality of the metal/MoS$_2$ contacts, including Ag, In, Mo and Ti, are also characterized. Conductivity measurements at room temperature show linear I-V characteristics using these all four metals while Ag gives the lowest contact resistances. Temperature dependent conductivity measurement reveals the Shottkey barrier heights in Ni/MoS$_2$ and Ag/MoS$_2$ contacts where the work function between these two metals and the single-layer MoS$_2$ are higher. The single-layer CVD MoS$_2$ devices show on/off current ratio exceeding 10^8, current saturation and on-state current density at 16 µA/µm. Inverters, NAND gates and voltage comparators have been demonstrated for the first time on CVD single-layer MoS$_2$. These circuit demonstrations show the scalability of both the material and the fabrication technology, and more importantly that the CVD single-layer MoS$_2$ material with its current quality is ready for advanced system level applications where many opportunities exist in ubiquitous electronics, optoelectronics and their interface with biological systems.

7.2 Challenges in the Applications of 2D Materials and Future Work

2D materials have the potential to change future electronics for several reasons. Firstly, the 2D material family offers a new class of materials characterized by strong covalent bonds in-plane but only very weak Van der Waal's coupling between the layers, leading to a material system with almost ideally self-passivated structures. Materials with such atomic structures are particularly attractive for heterogeneous integration, potentially free of the lattice mismatch problems that currently limit the integration of various materials system together on the same wafer to allow the utilization of the best material for each function. For example, it is because of the lattice mismatch problem, that it has been very difficult to integrate GaN power devices or InGaP LEDs onto Si substrate. 2D materials present new opportunities for realizing heterogeneous integration of electronic materials without suffering from lattice mismatch. In fact, the hBN/Graphene/hBN RF FETs demonstrated in this thesis work is a perfect example where

the lack of interaction between the hBN layers and the graphene layer due to absence of dangling bonds allows the high mobility of graphene to be preserved. This is in direct contrast to the traditional approach of achieving high quality heterogeneous materials by matching the lattice constants between the layers in a 3D lattice. In the future, we may be able to utilize lateral, vertical and 3D heterostructures of 2D materials for electronics and optoelectronics applications where many opportunities for designing novel devices and circuit architectures exist.

Developing 2D materials for electronic applications also have other far-reaching significance. The scaling of Si electronics has been very successful for the past six decades, which has played a pivotal role in driving the information revolution that has shaped and is still shaping the world we see today. However, despite of our capability today to produce transistor devices at sub-20 nm scale, the control of the electronic materials and the associated fabrication process has seldom reached atomic level. The successful synthesis of single-atomic layer materials and its utilization for electronic applications may be the first time we are able to achieve atomic level control of the electronic material thickness in the transistor channel. In the future, we would like to achieve atomic level control of both the electronic materials and the fabrication processes in all three dimensions. Synthesizing 2D materials is the first step towards the goal on the material side while fabrication techniques such as atomic layer deposition offers opportunities on the process control. This ultimate thickness control in the vertical direction is not just attractive for device scaling, more importantly it opens the door to unlimited opportunities for new applications. Atomic-scale materials also go beyond just 2D crystals. Single-layer materials can be patterned into 1-D quantum wires and 0-D quantum dots where quantum confinements can lead to geometrically tunable bandgaps and enhanced light emission.

The most promising applications of 2D materials must be developed based on the unique properties of this material system that are not often found in other materials. 2D materials offer three key properties that are particularly attractive for future applications: the flexibility and transparency, the ease for heterogeneous integration without lattice mismatch problem, and extraordinary sensing capability due to high surface-to-volume ratio and high mobility. There are three general areas of applications, which I believe are particularly promising for 2D materials. The first area is to develop 2D materials for GHz frequency ubiquitous electronics applications.

Existing technology for ubiquitous electronics are primarily based on organic semiconductors, which are flexible, but extremely slow. Flexible organic semiconductor circuits can typically operate only in the kHz frequency range due to the low mobility of these materials (normally < 1 cm^2/V.s). Hence, the organic flexible electronics technology are currently limited mostly to display applications while many important functionalities of radio frequency electronics, such as GPS, Wifi and Bluetooth, require circuit operations at GHz frequency. 2D materials present many new opportunities in this emerging field. A second promising application of 2D materials lies in their outstanding optical properties. Optoelectronics devices, such as photodetectors, LEDs and even lasers, based on 2D materials can be envisioned to emerge where they can be placed on to arbitrary surfaces including flexible and transparent ones. New opportunities can arise in developing THz and infrared sensors based on graphene either based on conventional device structure or novel plasmonic devices. Low cost solar cells to be placed on any type of substrates can also be developed where many potential applications exist, for example as the energy harvesting units in self-powered sensors or sensor networks. Finally, many unexplored opportunities exist in developing 2D materials for application in biological systems. 2D materials like graphene are very attractive bio-compatible options of flexible and semitransparent electrodes for interfacing with the brain neurons. 2D materials can also be used to build low-cost biosensors with many potential applications, such as glucose detection, moisture sensing, and body temperature monitoring. It should also be emphasized that these applications mentioned above are some promising possibilities of 2D materials that can be identified with today's perspective while many novel ideas are waiting to be explored and discovered for the years to come.

On the other hand, many challenges remain in developing 2D materials for electronics and optoelectronics applications, from material synthesis to device technology and to some application specific challenges. The most significant obstacle probably lies with the material synthesis. The quality of the material underlies any potential applications and today's technology for synthesizing 2D materials is still immature. The ultimate goal of 2D material synthesis is to achieve large-area, high-quality, single-crystalline, single-layer material that are also free of defects and can be easily placed on any type of surfaces. Some issues facing the various synthesis approaches have been discussed in Chapter 2. At this point, the CVD technique offers

materials that can meet some, but not all, of these requirements. Issues still remain in obtaining large-area 2D materials in its single crystalline form and in avoiding the creation of defects during the transfer process. Greater challenges and opportunities co-exist in synthesizing 2D material heterostructures. By far, most of the device applications of 2D heterostructures are demonstrated on exfoliated flakes stacked together by the tedious aligned transfer techniques, for example using flip-chip bonder. But to potentially industrialize the production of 2D material heterostructures, they need to be synthesized in an integrated manner at wafer-scale. The growth process and the quality of the materials may also need to reach similar levels with respect to the III-V materials we have today. On the other hand, the requirements for the quality of the materials are also application specific. For example, the requirements on the quality of graphene for touch screen applications are less stringent than for applications in RF electronics. The requirement on the material durability, performance uniformity, device reliability and production yield are generally more relaxed for certain applications, such as plasmonic modulators and detectors, than others, such as high performance electronics.

Compared to conventional silicon and III-V electronics, graphene electronics offer numerous advantages. First, the ambipolar conduction allows the creation of a new family of device concepts that rely on the symmetry in the GFET transfer characteristic to realize certain RF circuit functions. These new devices enable simpler circuits, with fewer devices than in conventional electronics. In circuit design, simpler circuits often mean less power consumption, smaller chip areas, and reduced parasitic components. Second, the excellent electrostatic control in graphene devices, where the charges are confined within a single atomic layer, is very attractive for device scaling and for high-frequency applications. In addition, the versatile transfer technology developed for CVD grown graphene allows the integration of graphene devices on arbitrary substrates with minimal mobility degradation. This special feature of CVD graphene makes the integration between graphene and silicon electronics straight forward [271]. The silicon circuits can be fabricated on silicon wafer first and then a layer of graphene can be transferred onto the silicon wafer where graphene devices are fabricated and linked to the silicon electronics underneath through vias. Furthermore, graphene grown by CVD can also be transferred to transparent and elastic materials to enable transparent and flexible electronics. On top of all these advantages, graphene is a material with very high mobility and carrier velocity,

which makes many of the applications introduced in this article potentially realizable at very high frequencies. Finally, its 2D geometry, in combination with the excellent chemical and thermal stability of graphene, makes the fabrication of graphene circuits fully compatible and integrable with silicon-based fabrication technology, which is the mainstream of the semiconductor industry.

At the same time, significant challenges still remain before graphene applications can be used at an industrial scale. A multi-pronged approach is needed to overcome them and to develop the strength of graphene electronics technology to its full potential. First, there is great room for improving material quality in terms of uniformity, sheet size, and carrier mobility, among others. Second, the choice of substrate is crucial for graphene device and circuit performance. An ideal substrate needs to preserve the high mobility in graphene, enhance heat dissipation, be scalable to large areas, minimize parasitic capacitances, and have low cost. Furthermore, research on improving device reliability and performance uniformity across devices is still in its infancy.

Despite these challenges, the rapid development in graphene devices and circuit technology in the past few years has shown promising signs for future applications. We believe that with the continuous improvements in material synthesis and device fabrication technology, graphene electronics will have a great impact on future generations of RF circuits.

List of Publications Related to This Thesis Work

Journal Publications

A. Hsu, H. Wang, B. Mailly, X. Zhang, L. Yu, K. K. Kim, Y. Shi, Y. H. Lee, Y. C. Shin, M. Dubey, J. Kong, and T. Palacios "Large Area Two-Dimensional Electronics: Materials, Technology and Devices" *Proceedings of the IEEE*, 101, 7, 1638-1652, 2013. (Invited Review Paper)

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H. Wang, L. Yu, Y.-H. Lee, Y. Shi, M. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios "Integrated Circuits Based on Bilayer MoS_2 Transistors", *Nano Lett.*, 12, 9, pp. 4674-4680, 2012.

Y.-H. Lee, L. Yu, H. Wang, W. Fang, X. Ling, Y. Shi, C.-T. Lin, J.-K. Hwang, M.-T. Chang, C.-S. Chang, M. Dresselhaus, T. Palacios, L.-J. Li, J. Kong "Synthesis and Transfer of Single Layer Transition Metal Disulfides on Diverse Surfaces" *Nano Lett.*, 13, 4, pp. 1852-1857, 2013.

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H. Wang, A. Hsu, D. S. Lee, K. K. Kim, J. Kong, and T. Palacios "Delay Analysis of Graphene Field Effect Transistors" *IEEE Electron Dev. Lett.*, vol. 33, no. 3, 2012.

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<u>H. Wang</u>, A. Hsu, J. Wu, J. Kong, and T. Palacios "Graphene-Based Ambipolar RF Mixers" *IEEE Electron Dev. Lett.*, vol. 31, no. 9, pp. 906-908, September 2010.

T. Palacios, A. Hsu, and <u>H. Wang</u> "Applications of Graphene Devices in RF Communications" *IEEE Communications Magazine*, vol. 48, no. 6, pp. 122-128, June 2010. (Invited Review Paper)

<u>H. Wang</u>, D. Nezich, J. Kong and T. Palacios "Graphene Frequency Multipliers" *IEEE Electron Dev. Lett.*, vol. 30, no. 5, pp. 547-549, May 2009.

Conference Publications

S. Rakheja, <u>H. Wang</u>, T. Palacios, I. Meric, K. Shepard, and D. Antoniadis "A unified charge-current compact model for ambipolar operation in quasi-ballistic graphene transistors: Experimental verification and circuit-analysis demonstration" *International Electron Devices Meeting* (**IEDM**), 2013, accepted for publication.

<u>H. Wang</u>, L. Yu, Y.-H. Li, W. Fang, A. Hsu, P. Herring, M. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios "Large-scale 2D Electronics based on Single-layer MoS$_2$" *APS March Meeting,* 2013, Baltimore, MD.

Y.-H. Lee, <u>H. Wang</u>, L. Yu, W. Fang, T. Palacios, L.-J. Li, J. Kong "Synthesis of Single Layer Transition Metal Dichalcogenides with Chemical Vapor Deposition" *APS March Meeting,* 2013, Baltimore, MD.

A. G. Birdwell, F. J. Crowne, L. Yu, <u>H. Wang</u>, T. P. O'Regan, P. B. Shah, T. Palacios and M. Dubey "Temperature Dependence of the Raman Spectra of Mechanically Exfoliated Monolayer MoS$_2$" *APS March Meeting,* 2013, Baltimore.

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<u>H. Wang</u>, A. Hsu, B. Mailly, K. K. Kim, J. Kong, and T. Palacios "Towards Ubiquitous RF Electronics based on Graphene" *IEEE MTT-S International Microwave Symposium (IMS) Digest*, WE3A-1, 2012. (Invited Paper)

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Applications" *IEEE MTT-S International Microwave Symposium (IMS) Digest*, TH2D-3, 2011. (Invited Paper)

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A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios "Large Area Chemical Vapor Deposition Graphene Photodetectors" *APS March Meeting,* 2011, Dallas, TX.

B. Mailly-Giacchetti, A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios "Solution-gated Field Effect Transistors based on CVD grown Graphene for chemical and bio sensing applications" *APS March Meeting,* 2011, Dallas, TX.

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