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Spatial distribution of structural degradation under high-power stress in AlGaN/GaN high electron mobility transistors

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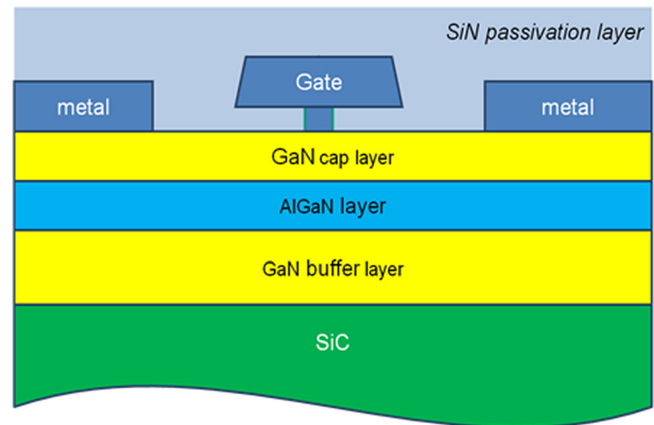
The two-dimensional spatial distribution of structural degradation of AlGaN/GaN high electron mobility transistors was investigated under high-power electrical stressing using atomic force and scanning electron microscopy. It was found that pits form on the surface of the GaN cap layer at the edges of the gate fingers in the middle of the device. The average pit area and density increase gradually from the edge to the center of the fingers and are more common along inner fingers than fingers. It was also found that pit formation and growth are thermally activated. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4707163]

GaN's high electron mobility, large band gap, and capacity for high temperature operation make it ideal for use in high electron mobility transistors (HEMTs) for high-power and high-frequency applications.[1–3] Despite having demonstrated outstanding performance,[4,5] the limited electrical reliability of GaN-based HEMTs remains a challenge to their widespread use.[6,7] To overcome this, it is essential to understand and identify the physical mechanisms responsible for degradation. While degradation of GaN HEMTs has been studied extensively,[6–10] the current understanding of the dominant degradation mechanisms is still limited. Our previous studies identified electrical degradation that was mostly driven by an electric field across the AlGaN barrier. Under high-voltage OFF-state stress, due to the piezoelectric nature of GaN and AlGaN, a very high mechanical stress develops under the drain-edge of the gate, contributing to structural damage to the GaN cap and AlGaN layer.[11,12]

TEM analysis has revealed the formation of trenches and pits after ON-state and OFF-state stressing of GaN HEMTs.[10,13] Atomic force microscopy (AFM) and scanning electron microscopy (SEM) studies of the surface of degraded devices have provided a planar view of these defects.[11,14] Temperature has been found to speed up the formation of these defects.[14] Understanding structural degradation during high-power stressing is particularly important because of the simultaneous presence of high current, high voltage and high temperature, the latter being a result of device self-heating. A complicating factor is that under high-power stress, the junction temperature can be non-uniform and depend on various factors such as device layout and the details of the epitaxial heterostructure.[15,16] Typically, the center of the device is much hotter than its periphery.[17] A consequence of this is that the current density is lower at the center. The implications of this on the structural degradation of the devices are unknown. In this paper, we investigate the spatial distribution of electrical and structural degradation of multifinger AlGaN/GaN HEMTs under high-power stressing. This is a regime in which pit formation has not been studied before. Furthermore, we study the two-dimensional distribution of pits on a device-wide scale, something that has not been carried out before in any stress regime. Our study reveals a prominent pattern of structural degradation that correlates well with the modeled temperature distribution. This work strongly suggests that proper attention to device thermal design is essential to achieve long term reliability of GaN HEMTs.

Figure 1 shows the device structure. An AlGaN/GaN heterostructure was grown on a SiC substrate using metal-organic chemical vapor deposition. The heterostructure includes a thin GaN capping layer that protects the AlGaN barrier layer and reduces the chance of oxidation or crack formation caused by



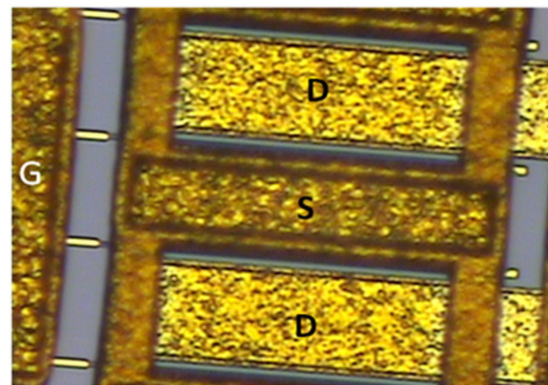


FIG. 1. Cross section of the device (top). Top-view, optical micrograph of the tested device with four 100 μm wide gate fingers, before etching (bottom).

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the inverse piezoelectric effect. The tested device has four 100 μm-wide fingers (Fig. 1, right). Further details of the device structure are given in Ref. 18. Due to the symmetric nature of the device geometry, we have analyzed one half each of one of the inner and outer fingers. Two different devices were studied yielding essentially identical results.

The devices were stressed in the high-power state with drain to source voltage $V_{DS} = 40$ V and quiescent drain current $I_{DQ} = 250$ mA/mm at a base-plate temperature of 120 °C. The stress time was 523 h. The maximum channel temperature under this stress condition was estimated to be around 354 °C from thermal simulations. These stress conditions are very harsh and far beyond the designed operational range of this device. They were selected to induce significant device degradation in a short span of time. This pit-related degradation mode has been observed in many devices stressed under a variety of conditions, including different bias conditions and temperatures.[11,19] The maximum current was recorded during the test by periodically interrupting the stress as shown in Figure 2.

After the stress test, the SiN passivation layer and surface metal were removed so as to enable characterization of the semiconductor surface underneath the gate metal[11] by an AFM-Nanoscope IIIa scanned probe microscope, a Zeiss supra 55vp SEM and an FEI Helios600.

Figure 3 shows that pits formed along the drain-side edge of the inner finger, which is in agreement with our previous OFF-state studies.[11] Along the length of the finger, pits were found to be more likely to merge together (Figure 3(b)) near the center than towards the end (Figure 3(a)). The AFM images show that the pits merge and form trenches along the edge of the gate (Figure 3(c)), a typical width and depth of the trench is roughly 50 nm and 8 nm, respectively. The pit distribution along the finger suggests a thermal enhancement of the pit formation process. During electrical stressing, the temperature at the center is expected to be higher than in the periphery. Mechanical stress[20] and the high electric field at the drain side near the gate edge probably also play roles in driving the formation and growth of these pits. In the presence of an electric field, the pits grow through a process involving thermally activated atomic diffusion, so that elevated temperatures in the center of the device accelerate the rate of physical degradation.

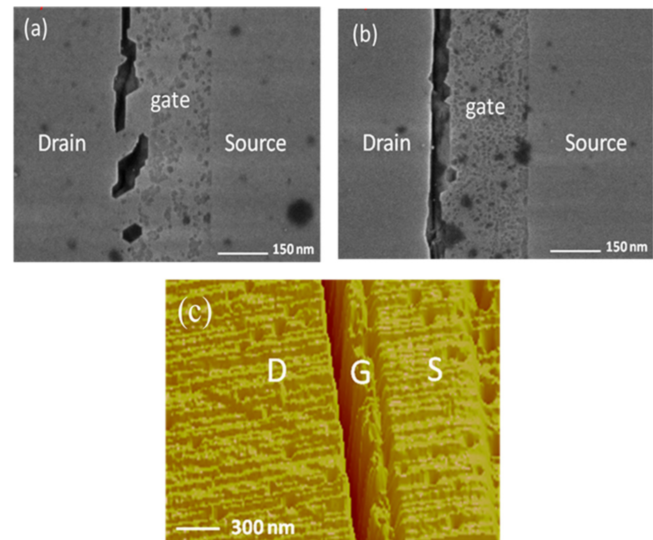

FIG. 3. SEM [(a), (b)] and AFM (c) images of different locations along a inner finger after stressing; (a) close to the end of the finger, (b) near the central part of the finger, (c) a closer view from an oblique angle showing a deep trench in the GaN cap layer. Prominent pits are apparent under the drain side edge of the gate.

The average cross-sectional pit area and pit linear density along the inner and outer fingers, as observed using AFM, are plotted in Figure 4. The average pit area was evaluated along a 10 μm segment of the gate finger. The pit density was defined as the fraction of the gate edge occupied by pits that were deeper than 7.5 nm in each 10 μm long segment. The largest cross-sectional area of a single merged pit, as observed by AFM, was about 1700 nm^2 (not shown on the figure). It should be noted that the defects present at the surface before stressing do not contribute to the measured pit area or density, due to their low depth and areal density. As Figure 4 shows, both the area and density of stress-induced pits markedly decrease from the center to the edge of the gate fingers and from the inner to the outer finger.

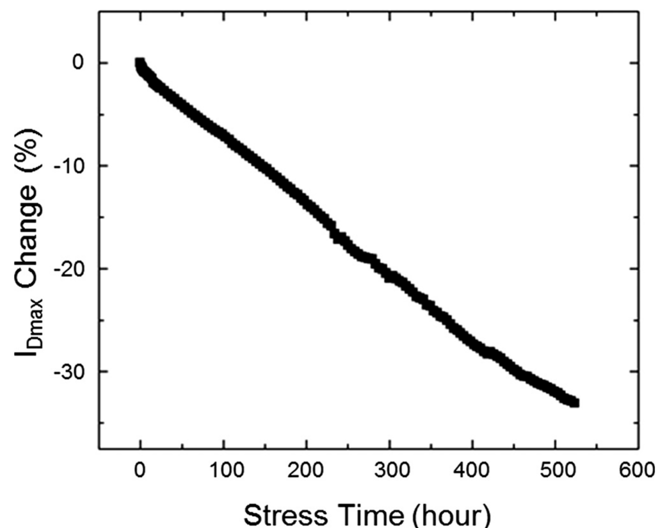

FIG. 2. Change in maximum drain current I_{Dmax} as a function of stress time (stress conditions: $I_{DQ} = 250$ mA/mm, $V_{DS} = 40$ V, $T_a = 120$ °C). A decrease of 33% in I_{Dmax} was found after stressing for 523 h.

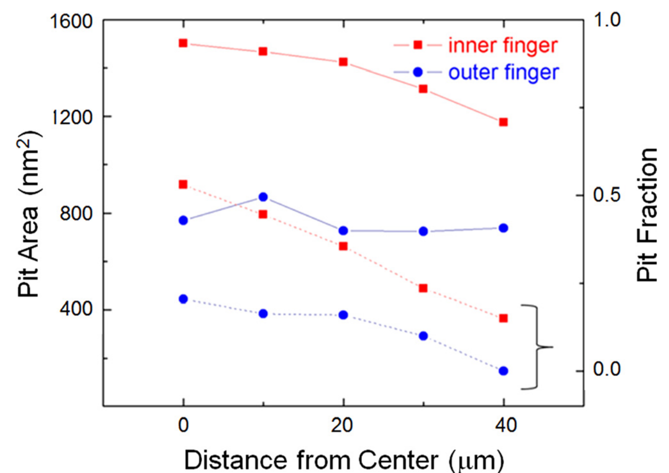

FIG. 4. Pit cross-sectional area and linear density as a function of location along the edge of the innercenter and outer fingers. The pit area and linear density decrease from the center to the end of the finger and are lower for the outer finger than the inner finger.

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The inset of Figure 5 shows simulated thermal profiles of the device under stress conditions. These simulations were carried out using the ANSYS thermal analysis system (TAS), as described in Ref. 21. The lowest temperature of the inner finger was very close to the highest temperature of the outer finger. This is due to better heat dissipation in these locations. Correlation of the data of Figure 4 and the simulated temperature profiles supports the conclusion that the pit formation process is accelerated at higher temperatures.

Figure 5 shows the pit area to the 3/2 power versus the calculated temperature, in the form of an Arrhenius plot. If the pits are assumed to all have the same shape (e.g., right circular cones with fixed ratios of the radius to depth), $A_{pit}^{3/2}$ scales with the pit volume. If the rate limiting mechanism for growth of the pits is field-induced diffusion away from the gate edges, the steady state flux away from the pit will scale with the diffusivity, and therefore with $\exp(-Q/kT)$, where Q is the activation energy for the rate-limiting diffusive process. The volume will also decrease at a constant rate, so that the data in Figure 5 should fall on a straight line. The reasonable fit of the data to this model supports the models underlying assumptions. The calculated activation energy in Figure 5, 0.32 eV, corresponds to the activation energy for the diffusive process involved. This is a reasonable value for surface diffusion.

The observations discussed above confirm that the physical damage is accelerated at high temperatures caused by self-heating, and that the location of damage and heating vary in a correlated way. The larger degradation seen at the center suggests that structural degradation is not driven by current or hot carrier effects because the current density and hot electron density at the center should be lower than at the periphery due to the higher channel temperature. This is consistent with separate experiments on similar devices previously tested in our lab.[6]

We have investigated the two-dimensional spatial distribution of structural damage caused by high-power electrical stressing of AlGaN/GaN HEMTs using AFM and SEM. It was found that pits and trenches formed along the drain side edge of the gate due to the high electric field and heating. The pit distribution is highly non-uniform along the finger length and depends on the finger location. The center of the middle gate finger is more degraded than the periphery and the inner finger shows more degradation than the outer finger. The distribution of pits correlates well with two-dimensional estimations of device junction temperature at the stress bias point suggesting that the degradation is thermally activated. Our work suggests that proper thermal design is essential to achieving long lifetimes in GaN HEMTs.

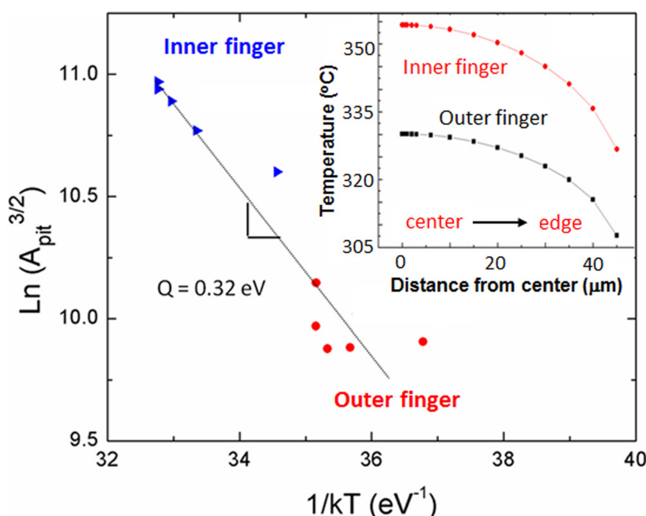

FIG. 5. Pit area to the 3/2 power as a function of temperature. The data exhibit a thermally activated behavior with an activation energy of 0.32 eV. The inset is the estimated temperature as a function of position during electrical stressing. The temperature decreases gradually from the center to the edge. The temperature of the outer finger was significantly lower than that of the innercenter finger.

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[1]U. K. Mishra, P. Parikh, and Y. F. Wu, Proc. IEEE **90**, 1022 (2002).
[2]T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, IEEE Electron Device Lett. **26**, 781 (2005).
[3]W. L. Pribble, J. W. Palmour, S. T. Sheppard, R. P. Smith, S. T. Allen, T. J. Smith, Z. Ring, J. J. Sumakeris, A. W. Saxler, and J. W. Milligan, IEEE MTT-S Int. Microwave Symp. Dig. **3**, 1819 (2002).
[4]B. M. Green, V. Tilak, S. Lee, H. Kim, J. A. Smart, K. J. Webb, J. R. Shealy, and L. F. Eastman, IEEE Trans. Microwave Theory Tech. **49**, 2486 (2001).
[5]Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **48**, 586 (2001).
[6]J. A. del Alamo and J. Joh, Microelectron. Reliab. **49**, 1200 (2009).
[7]C. Lee, L. Witkowski, Q. H. Tserng, P. Saunier, R. Birkhahn, D. Olson, G. Munns, S. Guo, and B. Albert, Electron. Lett. **41**, 155 (2005).
[8]D. W. Gotthold, S. P. Guo, R. Birkhahn, B. Albert, D. Florescu, and B. Peres, J. Electron. Mater. **33**, 408 (2004).
[9]T. Roy, Y. S. Puzyrev, B. R. Tuttle, D. M. Fleetwood, R. D. Schrimpf, D. F. Brown, U. K. Mishra, and S. T. Pantelides, Appl. Phys. Letts. **96**, 133503 (2010).
[10]S. Y. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, and M. J. Kim, Microelectron. Reliab. **49**, 478 (2009).
[11]P. Makaram, J. Joh, J. A. del Alamo, T. Palacios, and C. V. Thompson, Appl. Phys. Lett. **96**, 233509 (2010).
[12]J. Joh and J. A. del Alamo, in *Proceedings of IEEE International Electron Devices Meeting* (IEEE, Washington D.C., 2006).
[13]U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, S. Y. Park, T. Lee, J. Wang, M. J. Kim, J. Joh, and J. A. del Alamo, IEEE Electron Device Lett. **29**, 1098 (2008).
[14]J. Joh, P. Makaram, C. V. Thompson, and J. A. del Alamo, Proc. Int.'l. Workshop on Nitride Semiconductors, edited by Martin Stutzmann and S. Hildebrandt (Wiley-VCH, Tampa, Florida, USA, 2010).
[15]J. Kuzmik, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, IEEE Trans. Electron Devices **49**, 1496 (2002).
[16]K. Filippov and A. Balandin, in *Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show* (Nano Science and Technology Institute, 2003), Vol. 3, Chap. 7, p. 333.
[17]A. Sarua, H. F. Ji, M. Kuball, M. J. Uren, T. Martin, K. P. Hilton, and R. S. Balmer, IEEE Trans. Electron Devices **53**, 2438 (2006).
[18]J. L. Jimenez and U. Chowdhury, in *Proceeding of Reliability of Compound Semiconductors* (JEDEC, 2009), p. 57.
[19]J. Joh, P. Makaram, C. V. Thompson, and J. A. del Alamo, paper presented at the International Workshop on Nitride Semiconductors (IWNS 2010) on Planar View of Structural Degradation in GaN High Electron Mobility Transistors: Time and Temperature Dependence, Tampa, FL, 19–24 September 2010.
[20]S. Y. Park, T. Lee, and M. J. Kim, Trans. Electr. Electron. Mater. **11**, 49 (2010).
[21]J. Joh, J. A. del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, IEEE Trans. Electron Devices **56**, 2895 (2009).

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