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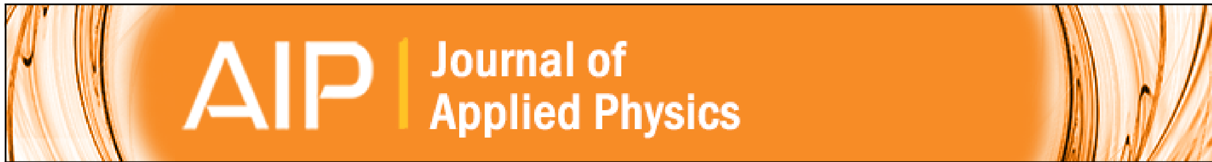

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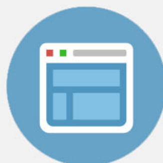

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Current on/off ratio enhancement of field effect transistors with bundled carbon nanotubes

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This work examines the enhancement of current on/off ratio in field effect transistor devices with bundled single-walled carbon nanotubes (CNTs) by incorporating a substrate etching step before the electrical cutting for metallic CNT elimination. The etching step prevents the damaging of the semiconducting CNTs while burning off the metallic ones by electrical current. By further incorporating a repeated gate voltage sweeping step, devices with low I_{off} (less than 2 nA) and high I_{on}/I_{off}, which is one to five orders of magnitude larger than before etching/cutting combination process, can be obtained. © *2009 American Institute of Physics*. [doi:10.1063/1.3253737]

I. INTRODUCTION

Carbon-nanotube (CNT) field effect transistors (FETs) have been highly pursued as a viable Si extension. While early work has shown great promise,[1–3] for most practical applications, a large number of CNTs are necessary to achieve sufficient current drive. Carrier mobility and current on/off ratio are important parameters that demonstrate the switching speed of CNT transistors. State-of-the-art growth methods do not yield purely semiconducting CNTs, and even small mixtures of metallic CNTs are detrimental and significantly increases the off-state current and degrades the current on/off ratio. Although high-density growth of aligned CNTs have been demonstrated,[4] finding an effective means of eliminating only metallic CNTs in a CNT bundle has proven to be a challenge.[5–7] In this work we fabricated FETs using CNTs grown by chemical vapor deposition (CVD). By incorporating a substrate etching step before the electrical cutting step, the metallic CNTs are more effectively burnt off, whereas the damage to the semiconducting CNTs are significantly reduced. As a result, the current on/off ratio in many devices was enhanced by one to five orders of magnitude. By combining a repeated gate voltage sweeping step, more devices were observed to have a current on/off ratio enhancement.

II. DEVICE FABRICATION

Long, aligned CNTs were directly grown on a SiO_2/Si substrate in an ethanol-based CVD system using an emulsion of $FeCl_3$ and hexane stabilized with sodium dodecylsulfate as the catalyst [Fig. 1(a)].[8] While the CNT density (0.05–0.2 CNTs/μm) is an order of magnitude smaller than the samples reported in Ref. 4, this method does not require a special substrate. The CVD growth tends to produce single isolated CNTs as well as small bundles. Photolithography was used and Cr/Au (~10 nm/~100 nm thick, by thermal evaporation methods) metal electrodes were deposited to form contacts to the CNTs. FETs having channels of varying lengths (L=5, 15, 25, 35 μm) but with a fixed width (W=300 μm) are obtained [Fig. 1(b)]. Buffered oxide etching (BOE) was used to etch approximately 60 nm of the original 100 nm SiO_2 layer before subsequent electrical cutting steps.

III. RESULTS AND DISCUSSIONS

Figure 2 (dotted line) and Fig. 3(a) are typical $I_{ds}-V_{gs}$ curves of the fabricated devices. Due to the presence of me-

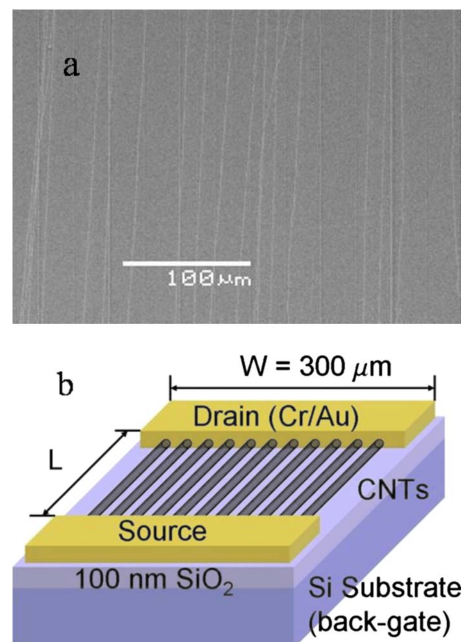

FIG. 1. (Color online) (a) SEM image of gas flow aligned long CNTs formed by CVD growth on a SiO_2/Si substrate. (b) Schematic of back-gated CNT-FET.

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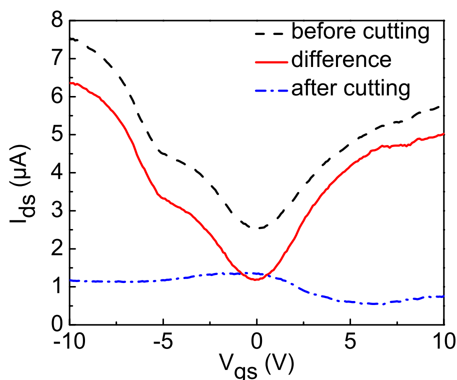

FIG. 2. (Color online) Current vs gate voltage sweep before and after electrical cutting for CNT-FETs (without etching the underlying SiO_2), showing that mostly semiconducting nanotubes are cut.

tallic CNTs in the channel (except for only a few devices), the as-fabricated FETs mostly exhibit I_{on}/I_{off} ratios less than 10.

An electrical cutting method similar to Ref. 5 was carried out in ambient on these devices to eliminate the metallic CNTs. In brief, a voltage was applied to the back gate (either +10 V or a gate voltage close to the minimum conductance point) to deplete the semiconducting CNTs in the channel. A bias voltage between the source drain was applied, which was kept increasing until the source drain current suddenly dropped, indicating that some CNTs within the channel became broken.[5] It was found that direct application of the electrical cutting method similar to Ref. 5 could not reliably cut metallic CNTs for our bundled samples. It is likely that the close contact of the semiconducting CNTs with the metallic ones in a bundle resulted in many semiconducting CNTs also being heated up and burnt off along with the metallic CNTs. Figure 2 is a typical example of the current versus gate voltage ($I_{ds}-V_{gs}$) before and after the electrical cutting. The difference between the two is also plotted in

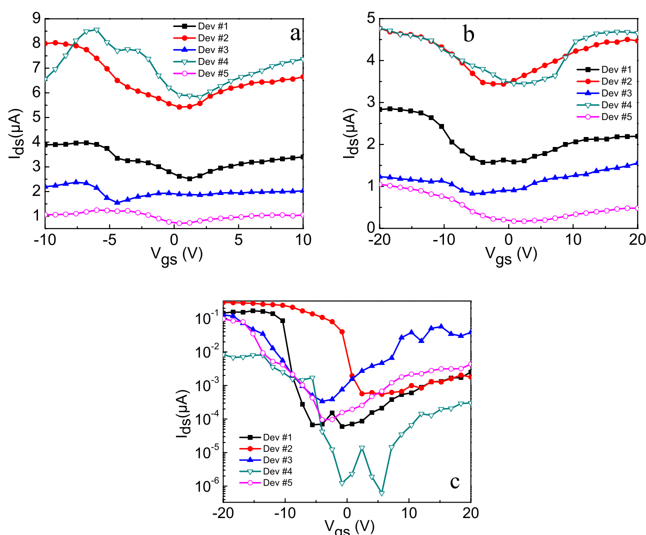

FIG. 3. (Color online) $I_{ds}-V_{gs}$ sweep of five samples, with each plot showing improvement in the I_{on}/I_{off} ratio after each processing step. (a) As-fabricated sample, with fixed channel length 5 μm. (b) After etching the SiO_2. (c) After electrical cutting. The current on/off ratio improved two to four orders of magnitude after etching the SiO_2 and electrical cutting.

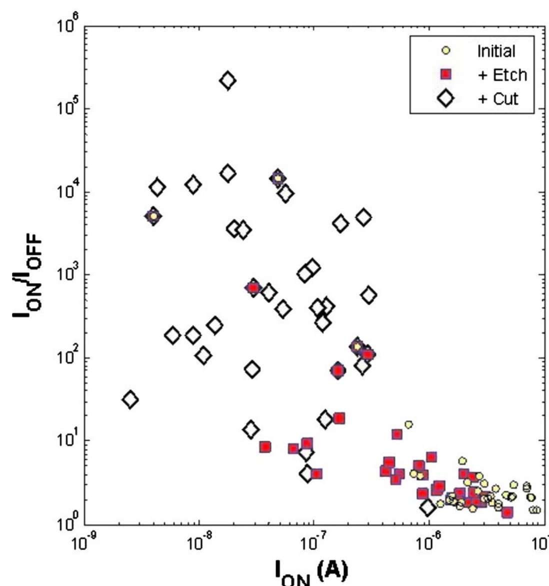

FIG. 4. (Color online) I_{on}/I_{off} vs I_{on} after each process step. Initially, devices tend to have high on currents but on/off ratios less than 10. After SiO_2 etching and cutting, the I_{on} decreases and the I_{on}/I_{off} ratio significantly increases.

solid line curve, which follows the overall variation of the original $I_{ds}-V_{gs}$ curve closely. This indicates that within the cut CNTs a large portion of them are likely semiconducting CNTs. On the other hand, for the remaining CNTs, metallic ones still compose a significant portion, as can be seen from the $I_{ds}-V_{gs}$ curve after cutting.

In order to eliminate only the metallic CNTs and enhance the current on/off ratio, two additional steps were introduced into the electrical cutting procedure. First, a BOE step was introduced before the electrical cutting. After the BOE, a few devices showed an improvement in the I_{on}/I_{off}, by one to two orders of magnitude. Most of the devices, on the other hand, only showed a slight reduction in I_{on} [compare Figs. 3(a) and 3(b)]. However, a dramatic improvement of I_{on}/I_{off} ratio was obtained with these devices after the electrical cutting step. Figure 3 shows five samples that were taken as an example to demonstrate the dramatic change. As metallic CNTs are burnt off, the increase in the I_{on}/I_{off} ratio is countered by a decrease in on-state current density. For 5 μm channel devices, after SiO_2 etching and electrical cutting steps, the average I_{on} decreased by 42.5×, but the I_{on}/I_{off} ratio improved significantly by one to five orders of magnitude (Fig. 4).

We used atomic force microscope (AFM) imaging and Raman analysis to investigate the possible reasons for the effective cutting. Figure 5 shows representative AFM images of two types of CNT behaviors before and after the SiO_2 etching. The CNTs can still be imaged well by the AFM after removing the underlying oxide by 60 nm, indicating the main part of each CNT is still in contact with the surface (instead of suspending across the electrode gap). As a result, there will be tension in most of the CNTs, as they are being stretched for up to 2×60 nm=120 nm in length. In Figs. 5(a) and 5(b), one of the CNTs in the nanotube bundle CNT A is being broken. This may explain the observation that

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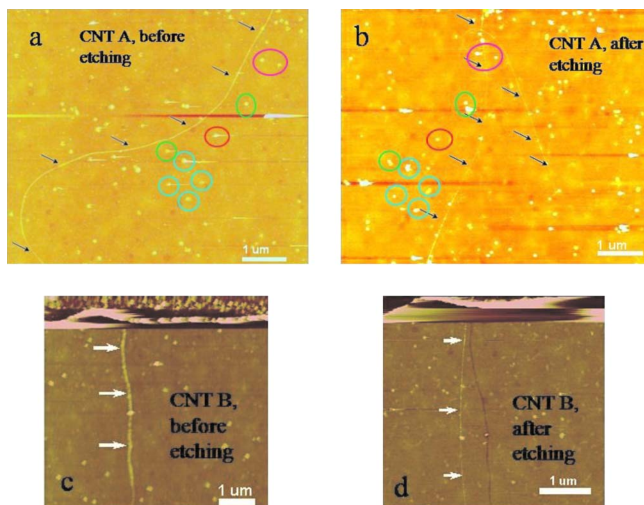

FIG. 5. (Color online) AFM images of two CNTs before and after etching. The arrows are pointed along the CNTs to guide the eyes. Particles on the surface are used to compare the location in the images. The original CNT location in the postetched image of CNT B is also visible in (d).

some of the CNT devices have a reduction in I_{on} after the SiO_2 etching. On the other hand, many other CNTs are like CNT B in Figs. 5(c) and 5(d), where the CNT is just stretched (much straighter after the SiO_2 etching than before) without being broken. The original CNT location can be seen in the postetched surface, as shown in Fig. 5(d). The tension within the CNTs is further confirmed by the Raman measurement. Figure 6 shows the Raman spectrum of a CNT before the SiO_2 etching and the spectra at the same location after the etching step. The downshifting of the G band for the entire spectra after etching is consistent with the presence of axial strain in the CNTs.[9,10] By measuring the Raman spectra from approximately ten devices, we estimate that the strain in the CNTs is 0.05%–0.05% (the amount of downshift in the G band is $\sim 1.6-13\ \text{cm}^{-1}$; direct calculation of elongation of 120 nm gives a maximum of 2.4%). Theoretical calculations have shown that axial strains in CNTs will introduce bandgaps in metallic CNTs and alter the bandgaps in semiconducting CNTs.[11] However, it is not very clear to us whether the presence of a small bandgap in metallic CNTs will make it easier to be damaged by high electrical current in air. Although the main part of the CNTs still lies on the substrate, it is likely at the two ends of the CNT a very small section is being suspended, as illustrated in Fig. 7(a). When a large electrical current goes through a CNT, the suspended part of the CNT will heat up much more quickly than the on-substrate part due to insufficient heat removal.[12] This may

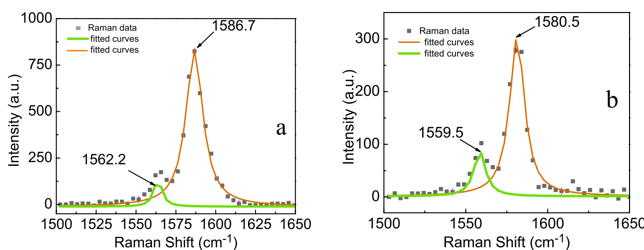

FIG. 6. (Color online) Raman spectra of a CNT before (a) and after (b) etching the SiO_2.

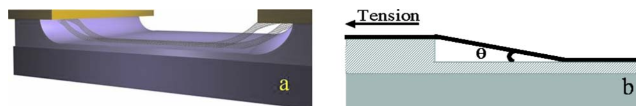

FIG. 7. (Color online) (a) Schematic of two CNTs being stretched due to substrate etching. The CNTs become suspended around the contact area. Based on their original lengths, they may become stretched to different degrees, thus may become separated. (b) Schematic of the tension and suspending angle of a CNT at the trench edge.

lead to more effective electrical cutting of the CNTs. In addition, since different CNTs in a bundle may originally have different lengths, once the substrate is removed by 60 nm and the CNTs are stretched, the substrate etching could result in different amount of tension within each CNT. Figure 7(b) illustrates a CNT being stretched at the edge of a trench. From our previous study, the tension within the CNT has the relationship with the suspending angle θ as $T=E_B[1/(1-\cos\theta)]$, where E_B is the binding energy of the CNT with the surface per unit length.[10] Thus different amounts of tension in different CNTs will give rise to different suspending angles θ, which will possibly separate the CNTs within one bundle spatially [Fig. 7(a)]. This separation between the CNTs could then result in much easier electrical cutting of the metallic CNTs, because the heating are mainly occurring at these suspended regions now.

As the etch depth is only 60 nm, it is very challenging to image the contact area to verify such a hypothesis. Nevertheless, the data in Fig. 8 present some indirect evidences for our explanation in Fig. 7(a): Fig. 8 shows the $I_{ds}-V_{ds}$ curve for a CNT device before and after etching the SiO_2. The low bias resistance does not change much, suggesting minimal damage to the CNTs by the substrate etching. But the high bias saturation current of the device after etching is much lower than before, indicating part of the CNT is suspended after etching the SiO_2.[12] When a large current goes through the CNTs, the suspended part will heat up the most due to less effective heat conduction between CNTs and air than CNTs and substrates,[12] and if at this part the CNTs within a bundle are separated, the burning off for metallic CNTs will be much more effective because of less effective heat conduction between or within bundles.

The SiO_2 etching and electrical cutting treatment were successful with about 50% of the devices. After the electrical

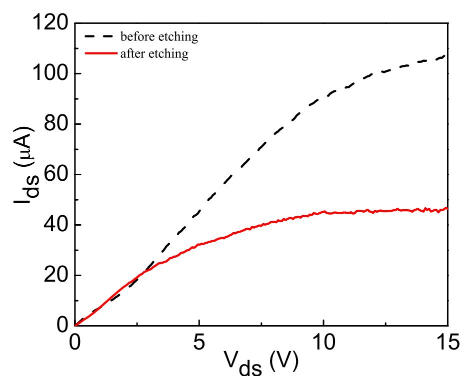

FIG. 8. (Color online) $I_{ds}-V_{ds}$ curve before and after etching SiO_2 ($W/L=300\ \mu\text{m}/5\ \mu\text{m}$, $Vg=0\ V$) for a CNT device.

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TABLE I. I_{on}/I_{off} improvement by extensive gate sweeping (the bias voltages are 0.1 V and the unit for the current is nA).

Sample	I_{on} (Before)	I_{on} (After)	I_{off} (Before)	I_{off} (After)	I_{on}/I_{off} (Before)	I_{on}/I_{off} (After)
1	708.36	66.42	109.92	0.94	6.44	70.66
2	248.34	118.53	124.99	0.0036	1.99	32916.67
3	353.47	63.29	172.02	0.49	2.05	128.98
4	344.45	104.54	61.427	0.54	5.61	193.59
5	83.73	77.23	11.43	1.27	7.33	60.81
6	177.54	133.24	13.2	1.61	13.45	82.76
7	124.39	28.04	6.79	0.11	18.32	254.91
8	288.33	284.76	14.23	1.97	20.26	144.55
9	203.11	202.69	5.93	1.58	34.25	128.28
10	967.62	15.35	597.17	0.01	1.62	15.35

cutting step, the rest devices still maintain a fairly large I_{off}. This is possibly due to the presence of large diameter metallic CNTs, because large diameter tubes have less curvature strain energy and are thus more stable.[7] This has been observed in previous methods for removing metallic CNTs as well; for example, methane plasma was used as an effective treatment to selectively eliminate isolated metallic CNTs with diameter <2 nm, but larger diameter metallic CNTs cannot be damaged easily.[7] In order to turn off most of the devices, an additional step was used after the electrical cutting. First the bias voltage was swept to +40 V. Afterwards the gate voltage was repetitively swept from -20 to 20 V under a constant applied bias voltage (0.1 V). In normal operation, a single gate sweep generally does not affect the behavior of the CNT devices. However, we have found that repeated sweeping for multiple times after large electrical stress (high bias voltage) can induce further modification to the CNT behavior. Both I_{on} and I_{off} will reduce, indicating that defects are likely induced in the lattice, but since the reduction in I_{off} is often more than I_{on}, it significantly increases the I_{on}/I_{off} ratio. Table I lists the I_{on}, I_{off}, and the I_{on}/I_{off} ratio of ten devices before and after the intensive gate sweep. It can be seen that the I_{on}/I_{off} ratio can increase one to four orders of magnitude. Afterwards, it was found that the samples can sit in air for overnight without any change to its $I_{ds}-V_{ds}$, $I_{ds}-V_{gs}$ characteristics. In addition, a single gate sweep (same voltage range) will not alter the device performance. Thus the I_{on}/I_{off} ratio improvement occurs under intensive gate sweeping following the high bias electrical stress. At present the exact mechanism is not clear to us, though it is possible that defects are introduced in the lattice of large diameter metallic tubes, similar to the chemical modification of graphene under a large applied gate voltage.[13]

Figure 9 shows the overall effects of our processing by comparing the behavior of the original devices before and after all the process steps. In total 66 devices are presented here. Devices of different channel lengths do not show noticeable differences in response to the treatments. Figure 9(a) shows the histogram of the current on/off ratio. The original as-grown devices show a narrow distribution concentrated below 10, while the processed devices show a higher I_{on}/I_{off} ratio that is more spread out. Figures 9(b) and 9(c) compare the I_{off} versus I_{on} for these devices. The various processing steps reduce I_{on} by one to two orders of magnitude. Nevertheless, the I_{off} of the devices are all below 2 nA after the processing steps.

Lastly, we point out that the 66 devices discussed here do not include the ones that are damaged during the process. If there are only a few CNTs in between the electrodes, the processing steps may damage all the CNTs in the channel, thus resulting in dead devices. It is possible to overcome this by starting with very high-density parallel aligned CNT

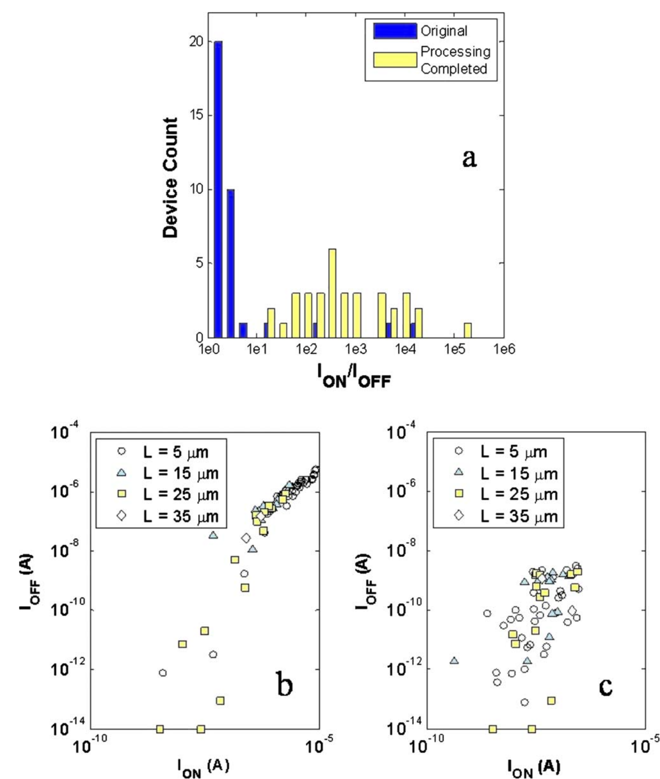

FIG. 9. (Color online) (a) Histogram of I_{on}/I_{off} ratio. Originally, most devices have an on/off ratio less than 10. After processing, devices have higher I_{on}/I_{off} ratios across a broader range. (b) I_{off} vs I_{on} before processing ($W=300$ μm, L is the channel length, and $V_{ds}=0.1$ V) Original devices have high I_{on} and high I_{off}. (c) After SiO_2 etching, cutting, and sweeping, most devices have significantly lower I_{off}.

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arrays[14] for the initial devices to counteract the reduction in I_{on} and by preventing the overall failure of the devices.

IV. CONCLUSION

In summary, this work has developed strategies of etching/cutting combination process to improve the electrical cutting method so that the current on/off ratio of CNT-FETs can be effectively enhanced. Devices with low I_{off} (less than 2 nA) and high I_{on}/I_{off}, which is one to five orders of magnitude larger than before etching/cutting combination process, were obtained. This method may be applicable for FETs made of high-density, parallel arrays of CNTs.

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