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21.4 90.6% Efficient 11MHz 22W LED Driver Using GaN FETs and Burst-Mode Controller with 0.96 Power Factor

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With the advent of reliable, high brightness and high efficacy LEDs, the lighting industry is expected to see a significant growth in the near future. However, for LEDs to completely replace the traditional incandescent and CFL bulbs, the power converters within the LED drivers need to be miniaturized. Superior figure of merit ($R_{ds,ON} \times Q_g$) of Gallium Nitride (GaN) FETs over Silicon FETs [1] can enable both high efficiency and high frequency operation, thereby making power converters smaller, more efficient and reliable. By using integrated controllers and drivers, the number of components on the driver PCB can be reduced, further miniaturizing the driver. This work focuses on demonstrating a small form factor, high efficiency offline LED driver using GaN FETs with an integrated gate driver and controller circuit implemented on a 0.35μm CMOS process with 3.3V/15V voltage handling capability.

Figure 21.4.1 shows the architecture of the LED driver implemented. An inverted buck converter [2,3] is used to drive a string of 20 LEDs. In order to operate the converter efficiently at high frequencies, a Quasi-Resonant topology [4] is employed. The resonant circuit, formed by L_{RESO} and $C_{OUT,GaN}$, helps achieve Zero Voltage Switching (ZVS). L_{BUCK} and C_{BUCK} form the LC filter of the inverted buck converter. A full bridge rectifier and an EMI filter are used to interface with the AC input voltage. An on-chip integrated burst-mode controller is implemented to control the LED current and drive the gate terminal of the GaN FET. In LED drivers, a sense resistor (R_{SENSE}) is generally usedμ to estimate the current through the FET. However, this leads to additional conduction losses that adversely affect the efficiency. In this work, the efficiency degradation due to R_{SENSE} (1Ω) is minimized by allowing the current to flow through R_{SENSE} only once in 16 system (or burst) cycles. A low breakdown-voltage (hence low $R_{ds,ON}$) silicon device (LV Si FET) is used to bypass R_{SENSE} for the other 15 system cycles. By peak-detection and low-pass filtering the voltage across R_{SENSE}, the FET current is estimated from $V_{SENSE,AVG}$.

Figure 21.4.2 shows the Quasi-Resonant inverted buck converter's ZVS operation. In this circuit, L_{RESO} and $C_{OUT,GaN}$ are made to resonate such that just prior to turning on the GaN FET, the voltage at the drain terminal comes close to ground. This minimizes the switching loss due to $C_{OUT,GaN}$ and enables the converter to operate at 11MHz. However, at such high switching frequencies and power levels, commercial inductors usually have significant core and conduction losses [5]. In this work, low permeability, low loss magnetic cores described in [5] have been used to make custom inductors L_{RESO} (850nH at 11MHz) and L_{BUCK} (12μH at 11MHz). Efforts have been made to minimize inter-winding capacitance and high frequency resistance due to skin effect. The gate of the GaN FET is driven with an 11MHz pulse having a fixed duty ratio, governed by the resonance between L_{RESO} and $C_{OUT,GaN}$. In order to reliably control the LED current, the 11MHz pulses are sent to the GaN FET at a bursts frequency of 67KHz [6]. Therefore, the gate drive signal to the GaN FET is an 11MHz pulse having a 67KHz envelope. The LED current can be adjusted by varying the on-time of the envelope (or burst). At full load (maximum LED current), the converter operates with a burst on-time of close to 5.3μs.

The block diagram of controller and gate driver IC implemented for the LED driver has been shown in Fig. 21.4.3. RC relaxation oscillators generate the required 11MHz (fixed duty ratio of 0.65) and 67KHz pulses (*hf_clk* and *lf_clk*). A one-bit feedback loop is implemented consisting of a Dimming Comparator, Increment/Decrement Block and a Burst Width Adjustment Block. The Dimming Comparator compares $V_{SENSE,AVG}$ (in Fig. 21.4.1) with a tunable reference, *dimming_ref* and sends an *inc_dec* signal to the Increment/Decrement Block to generate a 5-bit digital code for the Burst Width Adjustment Block. Power factor correction is incorporated into this controller by ensuring that *dimming_ref* has a similar sinusoidal nature as V_{RECT} (with the voltage divider in Fig. 21.4.1). The

dimming level is adjusted by varying the division ratio of the voltage divider. The Line Voltage Sense Comparator sends a *hold* signal to the Increment/Decrement logic when the line voltage is below a threshold (say 60V in case of 20 LEDs in series) during the AC cycle. Since no power is supplied to the LEDs below this threshold, the Increment/Decrement operation is then disabled. This ensures that the feedback loop does not increase the burst on-time unnecessarily when no power is supplied to the LEDs. In order to ensure that the feedback loop is stable, the burst on-time has been made monotonic with the input digital code. This is done by using a 5-bit Counter and a binary comparator shown in Fig. 21.4.3. An *envp* signal with the required burst width is obtained using *lf_clk_sync* (*lf_clk* synchronized with *hf_by2*) and the binary comparator output. The *envp* signal along with the *hf_clk* generate the required gate drive signal for the GaN FET. The LV FET is driven with a pulse which is "high" for 15 bursts and "low" for one burst. This pulse is generated by using a 4-bit Counter clocked with *lf_clk_sync* as shown in Fig. 21.4.3. Level shifters and Gate Drivers operating at 8V have been implemented to drive the gates of both the GaN and LV Si FET. It must be noted that in this work, the power for the on-chip control circuits and the gate drivers has been supplied externally from 3V and 8V supplies. Prior works [2,3] report auxiliary power converters that supply power to these circuits from the AC input to the system.

In order to quantify the efficiency advantage provided by the GaN FET for this converter, two versions of the Quasi-Resonant inverted buck converter were implemented, one with a commercial high voltage Silicon FET (HV Si FET) and the other with the GaN FET with similar input and output capacitances. All other components have been kept the same. Figure 21.4.4 shows the measured efficiencies of the power trains of the two converters with DC inputs ranging from 100V to 157V. For 133V and 157V, the efficiency improvements are 6.3% and 9.5% respectively. These improvements can be attributed to the lower $R_{ds,ON}$ of the GaN FET as compared to the HV Si FET. The voltage of the LED string varies from 61 to 65V and the output power (power to LEDs) ranges from 7W to 21W for these measurements.

The system has been tested with a string of 20 LEDs (each of 3.2V diode voltage) in parallel with a 15μF capacitor using the custom inductors described before. Figure 21.4.5 shows the efficiency and power factor plots of the system for different current levels. The power converter has been tested for AC inputs varying from 100 to 120V rms. A peak efficiency of 90.6% is obtained with a power factor of 0.96 at 400mA LED current (without gate driver losses). At 110V and 120V, the peak efficiencies are 89.5% and 86.7% for LED current of 400mA. The gate driver losses amount to 1 to 1.7% of the input power to the converter for these measurements. Figure 21.4.6 shows the transient waveforms showing the AC input voltage and current along with the design summary.

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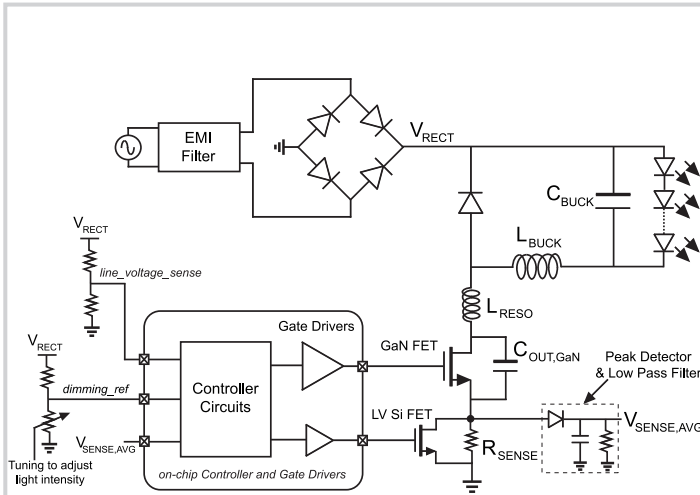
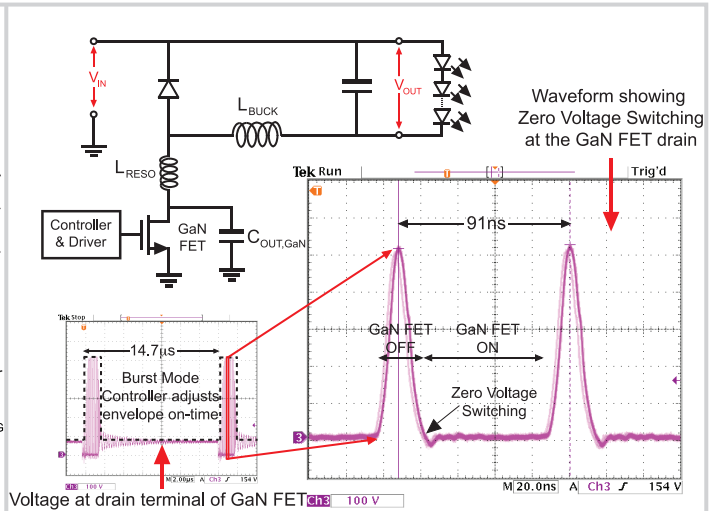Figure 21.4.1: Architecture of the LED Driver.

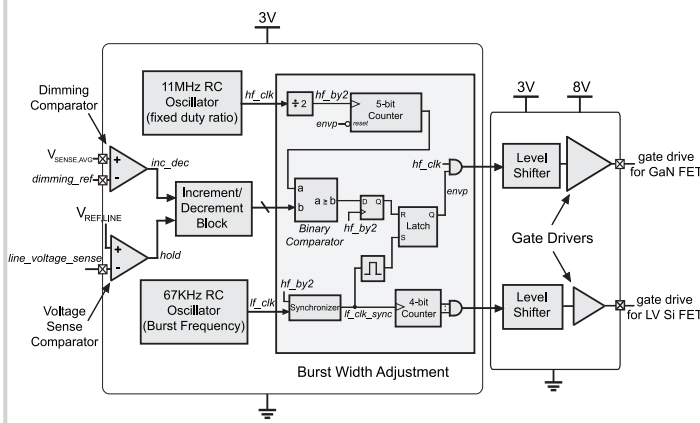Figure 21.4.2: Quasi-Resonant Inverted Buck with Zero Voltage Switching (LV Si FET not shown).

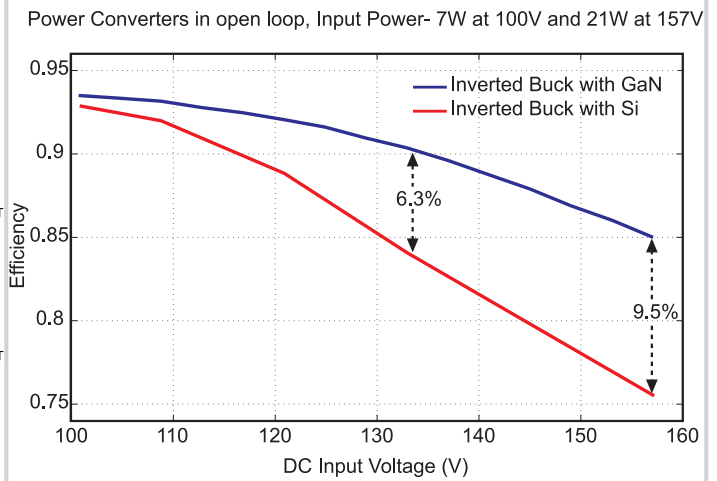Figure 21.4.3: Block diagram of circuits for dimming control and gate drivers.

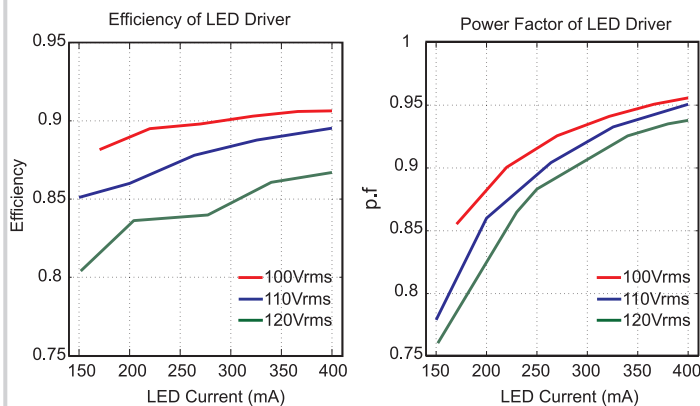Figure 21.4.4: Efficiency of LED driver with DC input voltage for GaN and Silicon FETs.

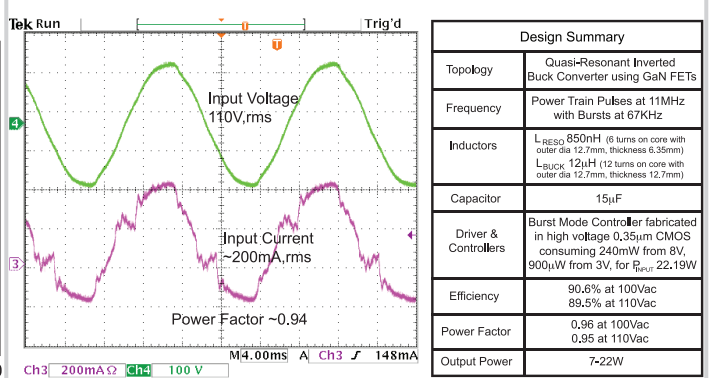Figure 21.4.5: Efficiency and power factor of LED driver with AC inputs.

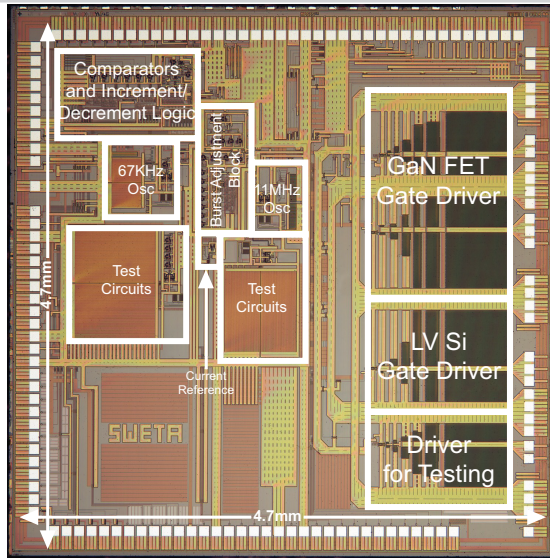Figure 21.4.6: Transient waveforms showing input voltage and current with summary table.

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Figure 21.4.7: Die micrograph of the controller and gate driver IC..