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Electrical and structural degradation of GaN high electron mobility transistors under high-power and high-temperature Direct Current stress

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We have stressed AlGaN/GaN HEMTs (High Electron Mobility Transistors) under high-power and high-temperature DC conditions that resulted in various levels of device degradation. Following electrical stress, we conducted a well-established three-step wet etching process to remove passivation, gate and ohmic contacts so that the device surface can be examined by SEM and AFM. We have found prominent pits and trenches that have formed under the gate edge on the drain side of the device. The width and depth of the pits under the gate edge correlate with the degree of drain current degradation. In addition, we also found visible erosion under the full extent of the gate. The depth of the eroded region averaged along the gate width under the gate correlated with channel resistance degradation. Both electrical and structural analysis results indicate that device degradation under high-power DC conditions is of a similar nature as in better understood high-voltage OFF-state conditions. The recognition of a unified degradation mechanism provides impetus to the development of a degradation model with lifetime predictive capabilities for a broad range of operating conditions spanning from OFF-state to ON-state. © *2015 AIP Publishing LLC*.
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I. INTRODUCTION

In the last few years, high-voltage GaN HEMT technology has burst into the scene promising to revolutionize high-power and high-frequency amplifiers. A critical concern with this new technology is reliability. An extensive amount of research has been devoted to studying the reliability of GaN HEMTs under various stress regimes such as ON-state, OFF-state, and $V_{DS} = 0$ V state.[1–9] Several mechanisms have been postulated to explain the various degradation patterns that have been observed.[8–18] Several studies [19–25] have shown the appearance of prominent physical damage (dimples, grooves, pits, trenches, and cracks) on the semiconductor surface under the edge of the gate after prolonged OFF-state stress. The damage extends through the GaN cap and the AlGaN barrier layer and in some extreme cases reaches into the GaN buffer layer.[26] It has also been found that the damage is accelerated with stress voltage and temperature and correlates with the drain current degradation suffered by the device.[19,20,26–28]

In power amplifier applications, the device is typically biased in the ON state. In spite of its importance, there has been very little research on the impact of prolonged high-power stress on the structural degradation of the device. This is partly due to the difficulty in controlling junction temperature. Marcon *et al.*[29] found evidence of structural degradation of devices subject to high-power and high-temperature stress. Cracks at the gate edge were identified where a strong reduction of gallium and nitrogen inside the crack was suggested by chemical analysis. Li *et al.*[27] also found evidence of structural degradation of devices subject to high-power electrical stress. Pits and trenches similar to those observed under OFF-state conditions were identified. The spatial distribution of the damage along the finger width suggested a thermally activated process. Nevertheless, no correlation between drain current degradation and structural degradation was established.

In this paper, we investigate the structural degradation of GaN HEMTs biased in the high-power regime at high temperature. We use both Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) to study the semiconductor surface after stress. We find similar pit and trench formation under the gate edge on the drain side as observed by other authors after stress in the OFF-state regime.[19,20] In a new finding, this damage strongly correlates with the degree of drain current degradation suffered by the device. Channel temperature was found to be an accelerating factor of this type of structural degradation. In addition, we have observed prominent erosion under the entire gate region. This was found to correlate with channel resistance degradation and appears to be much less temperature activated.

II. EXPERIMENTAL

The devices used in this study are prototype packaged S-band GaN-on-SiC MMICs from industry. The heterostructure includes a 5 nm GaN cap layer on top of a 16 nm AlGaN barrier layer which is in turn on a Fe-doped GaN buffer. The transistor features a gate with dimensions $L_g = 0.25\,\mu$m and $W_g = 2 \times 280\,\mu$m. The gate-source spacing is $2\,\mu$m and the gate-drain spacing is $4\,\mu$m.

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Testing took place in an Accel-RF life-test system equipped with a switching matrix that allows device characterization through external test equipment.[30] The devices were *step-temperature stressed* at $V_{DS} = 40$ or 50 V with $I_{DQ} = 100$ mA/mm. The base plate temperature was raised in steps from 50 °C to above 200 °C. The electrical stress was periodically stopped and the base plate temperature was lowered to 50 °C to enable device characterization under standardized conditions. Before the base plate temperature was raised to the next level, the device was completely detrapped by baking at 250 °C for 7.5 h. This is essential in order to separate *apparent device degradation* due to trapping from *permanent device degradation* due to structural damage or other causes. More details on these experiments are given in Ref. 31.

The parameters of the detrapping step were selected based on experiments where we intentionally introduced some trapping through benign stress, characterized the device through a set of FOMs, then baked the device and finally measured the same set of FOMs. By repeating this procedure several times and comparing the FOMs before and after baking, we can isolate the effect of baking on device recovery. Our selected detrapping step (250 °C for 7.5 h) yielded complete recovery of the device characteristics.

Fig. 1 shows a typical result. The figure graphs the maximum drain current (defined at $V_{DS} = 5$ V and $V_{GS} = 2$ V) normalized to its initial value and the off-state gate current (defined at $V_{DS} = 0.1$ V and $V_{GS} = -5$ V) as a function of stress time. These measurements are all made at 50 °C. The base plate temperatures as the experiment evolves are indicated in the figure. The actual junction temperature T_j's are also evaluated using a thermal model provided by our industrial collaborator and is also indicated in Fig. 1. The points sticking out in Fig. 1 correspond to measurements conducted at the transitions when the base plate temperature is increased. These points are taken right after the detrapping step and reflect device degradation in the absence of trapping. It is well known that in GaN HEMTs, carrier trapping

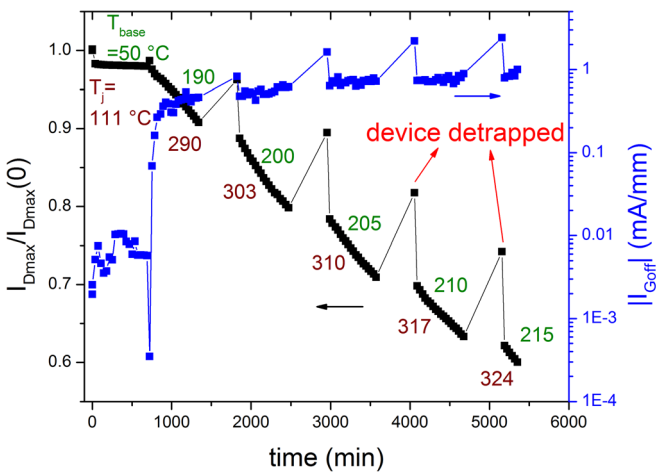

FIG. 1. Evolution of normalized I_{Dmax} (defined @ $V_{DS} = 5$ V, $V_{GS} = 2$ V) and $|I_{Goff}|$ (defined @ $V_{DS} = 0.1$ V, $V_{GS} = -5$ V) in the course of typical step-temperature stress under high power conditions. $I_{Dmax}(0)$ is 742 mA/mm. The bias point during stress is $V_{DS} = 40$ V and $I_{DQ} = 100$ mA/mm. Base temperature was raised from 50 °C up to 215 °C where the device blew up.

results in lower gate current as well as drain current.[4,32,33] The experiment proceeds until the device finally blew up.

The device shown in Fig. 1 degraded rather fast when compared with published data from isothermally treated devices. This is a result of our attempt to expedite the experiment by stressing the device under very harsh conditions. Looking at the junction temperatures in Fig. 1, we can notice that for T_{stress} exceeding 190 °C, the actual T_j is above 300 °C which is much higher than the specified maximum operating temperature for these devices (200 °C). In Ref. 31, we demonstrated that our stress methodology accelerates relevant degradation modes. Our step-temperature approach allows us to extract activation energies for device degradation rate. Our results agree quite well with those obtained using traditional long term life test experiments on similar device technology. This indicates that our experiments reflect device degradation under high power stress conditions rather accurately.

Detrapped output and gate characteristics of the device of Fig. 1 in its virgin state and right after stress at $T_{stress} = 210$ °C are shown in Fig. 2. These characteristics reflect permanent (non-trapping related) degradation. A noticeable reduction in the saturated current and the ON resistance can be seen. An increase of the gate current of more than two orders of magnitude is also observed.

One concern regarding our stress and characterization methodology is the fact that temperature ramping up and down is repeated for many times during our experiment which might itself impose considerable stress on the device. To prove that this temperature cycling alone does not appreciably degrade the device, we have carried out an experiment where a virgin device is first stressed at $T_{base} = 180$ °C under high-power DC conditions after which we conduct stress experiments at T_{base} of 50, 90, and 120 °C. The results shown in Fig. 3 indicate a much faster and severe drain current degradation during $T_{stress} = 180$ °C period than in the following lower temperature stress periods. This confirms that it is the high temperature that accelerates device degradation instead of the stress imposed by frequent temperature ramping.

Following the electrical stress experiment, a three-step process[9,19] was followed to remove the passivation and metal contacts from the surface of the devices. Our chemical techniques are rather benign on GaN. HF was used to remove passivation layer and aqua regia was adopted for removal of gate metal contact. Following these two steps, piranha was applied briefly to remove all organic contaminants and ensure a clean surface for structural analysis. None of these chemicals should attack the GaN cap layer. A Zeiss Supra 40 SEM and an AFM-Nanoscope IV Scanned Probe Microscope were used to analyze the exposed semiconductor surface.

III. ELECTRICAL AND STRUCTURAL DEGRADATION

A typical pattern of degradation is shown in Fig. 1. In all cases, off-state gate leakage current (I_{Goff}) degradation happens first and eventually saturates. On the other hand, degradation of the maximum drain current (I_{Dmax}) starts at a higher temperature and exhibits a thermally activated

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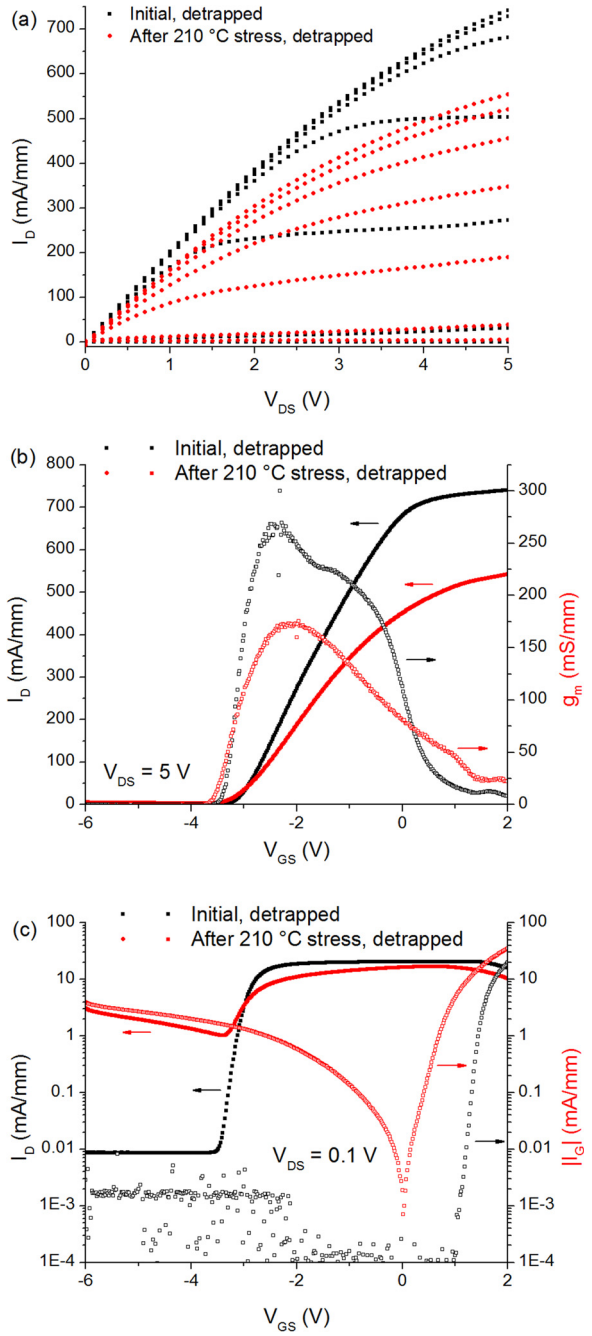

FIG. 2. (a) Output characteristics (V_{GS} from −4 V to 2 V in 1 V step), (b) transfer and transconductance characteristics for V_{DS} = 5 V, and (c) subthreshold and gate characteristics at V_{DS} = 0.1 V for the device of Fig. 1 before stress and after T_{stress} = 210 °C stress. All measurements are under detrapped conditions.

character. This behavior is similar to that observed in constant-voltage OFF-state experiments in similar devices.[34]

Fig. 4 shows SEM pictures obtained towards the center of one of the two gate fingers in six different devices. These six samples were stressed under various conditions (different V_{DS}) and ended up with different levels of I_{Dmax} degradation by the time they blew up. The purpose of using different stress conditions was to reach different levels of degradation. The sample size was limited and we did not attempt to carry out a detailed correlation study between $V_{DS,stress}$ and degree of electrical degradation.

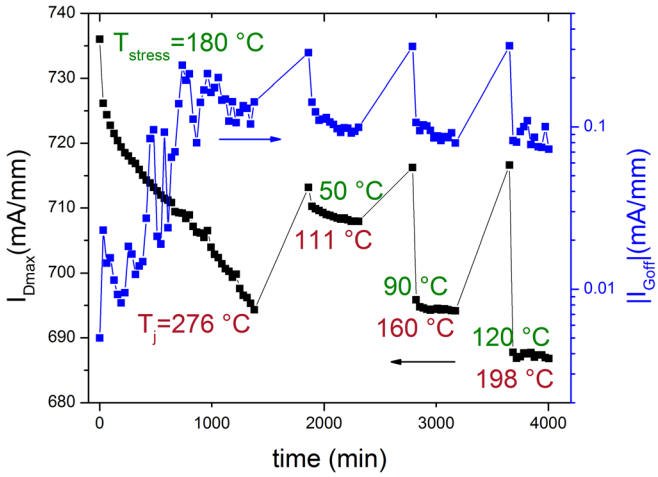

FIG. 3. Evolution of I_{Dmax} and $|I_{Goff}|$ for a device stressed first at high temperature and then at lower temperatures.

As seen in Fig. 4, in devices with relatively small I_{Dmax} degradation, a shallow groove appears along the gate finger on the drain side of the device. For devices with prominent I_{Dmax} degradation, deep pits are formed that tend to merge and form continuous trenches. When the overall drain current degradation increases from 0.2% (top left picture) up to 25.8% (bottom right picture), pits at the gate edge become more prominent and both their width and length increase with the increase in drain current degradation. The relative I_{Dmax} degradation indicated in the figure are obtained with

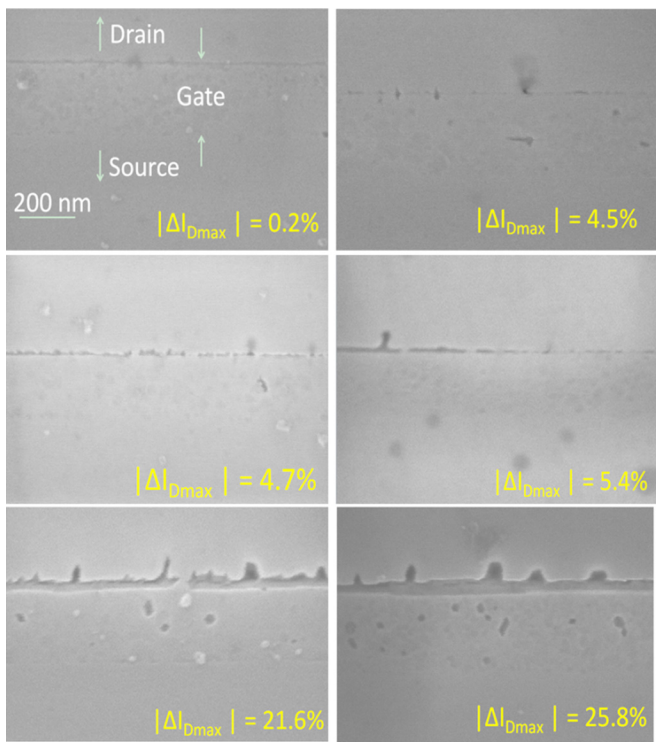

FIG. 4. SEM pictures of six delaminated devices that have been stressed under V_{DS} = 40 or 50 V and I_{DQ} = 100 mA/mm. From top left to bottom right picture, overall I_{Dmax} degradation increases. In all pictures, the drain is towards the top and the source towards the bottom. Prominent structural degradation appears in all cases under the gate edge on the drain side of the device.

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devices detrapped, thus reflecting permanent non-recoverable degradation.

To get more insight on the correlation between current degradation and structural degradation at the gate edge, a quantitative analysis was conducted using AFM. Fig. 5 shows a 3-D view of the gate area for the same six samples of Fig. 4. The vertical scales are the same for all six AFM pictures. From the top left to the bottom right pictures shown in the figure, as I_{Dmax} degradation increases, the structural damage formed at the gate edge evolves from a shallow groove to very prominent trenches which are deep enough to penetrate into the GaN buffer layer.

Fig. 6 shows a cross-sectional view of the device gate region from a single AFM line scan at the center of the gate finger for a device that suffered 25.8% degradation in I_{Dmax}. AFM provides a measurement of the actual width of the defects although the depth is likely to be underestimated. In this device, we clearly see that the trench under the gate edge on the drain side penetrates all the way through the GaN cap and AlGaN barrier layer.

Fig. 7 shows the correlation between permanent I_{Dmax} degradation and the geometry of the pits and trenches formed under the drain side edge of the gate. Each point in the graph represents a different device and the value was averaged across five 1 μm $\times$ 1 μm scans taken at the center of the gate finger. From the graph, it is clear that there is a strong correlation between I_{Dmax} degradation and both the depth and width of the pits and trenches. This is the first such observation under ON-state stress and is similar to what has been observed in GaN HEMTs under OFF-state stress.[19,20,26]

Besides the damage formed at the gate edge, there is an unusual finding of our structural studies in all stressed devices. Both SEM and AFM analyses reveal visible erosion under the entire gate of the device. This is more clearly seen in the cross section of Fig. 6 where the region under the gate shows clear erosion to a depth of about 1 to 3 nm. To our knowledge, damage of this kind has not been reported in the literature. Since devices from similar technologies were deprocessed using the same three-step wet etching process as no under-gate erosion was observed,[9,19] the observed damage is not likely to be an artifact of the wet etching process.

Of all the figures of merit that we measure in the course of our experiments, the average depth of this eroded region was found to only correlate with the channel resistance measured with the device completely detrapped. The channel resistance is derived from measurements of the ON resistance, R_{on}, which is the total resistance between drain and source with the gate floating, and source and drain resistances that are obtained through the drain-current injection technique.[35] The close correlation between the under-gate erosion depth and R_{CH} is shown in Fig. 8 for the same six devices discussed earlier in this paper. This figure also includes an analysis of a virgin device. The finite erosion depth that we observe in the virgin device indicates that the structural damage originates in the fabrication process and seems to be enhanced as a result of electrical stress.

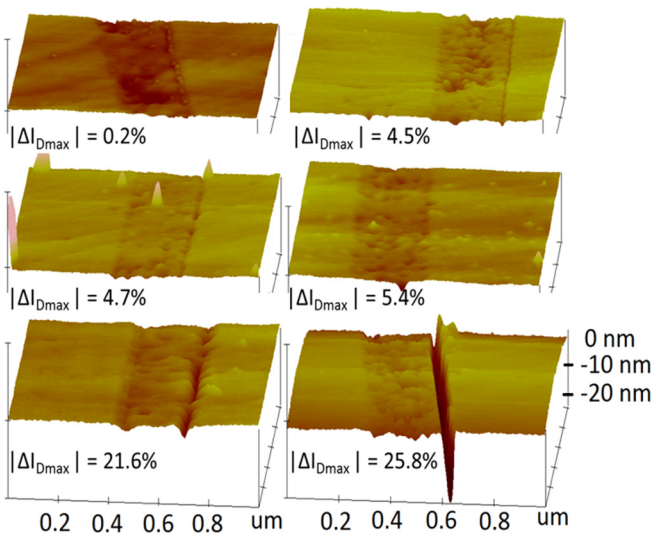

FIG. 5. AFM pictures of six delaminated devices that have been stressed under $V_{DS} = 40$ or 50 V and $I_{DQ} = 100$ mA/mm. From top left to bottom right picture, overall I_{Dmax} degradation increases. In all pictures, the source is towards the left and the drain is towards the right.

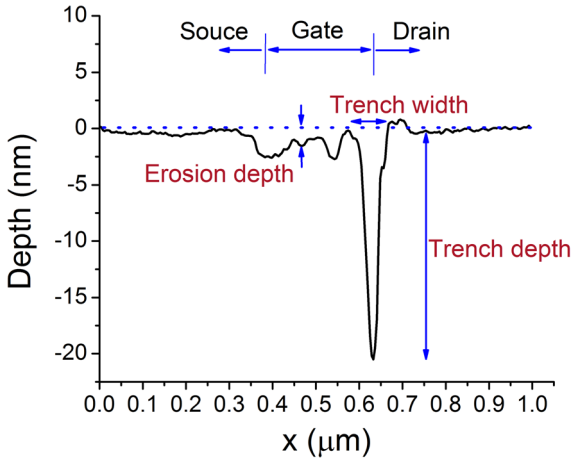

FIG. 6. Cross-sectional topographical view of a delaminated device from a single AFM line scan. I_{Dmax} degradation is 25.8% for this device. A prominent trench is visible under the gate edge on the drain side of the device. Visible erosion is also evident under the entire gate. The terms "trench width," "trench depth," and "erosion depth" are defined as shown in the picture.

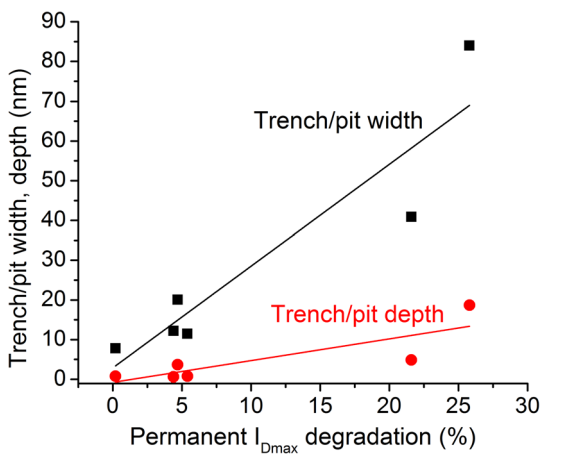

FIG. 7. Correlation between permanent I_{Dmax} degradation and the geometry of structural degradation under the gate edge on the drain side of the device for the six devices biased in the high-power stress regime. A clear correlation between I_{Dmax} degradation and trench/pit width and depth are observed.

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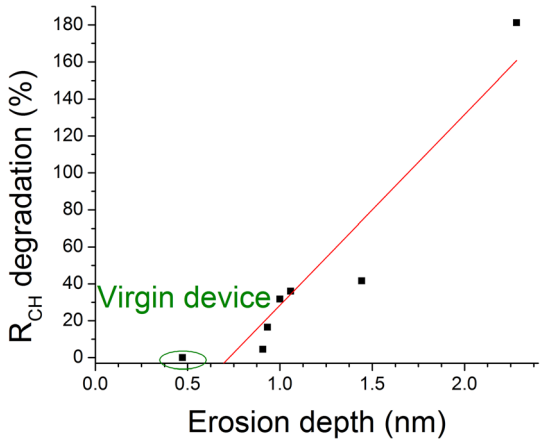

FIG. 8. Correlation between permanent channel resistance degradation (measured under detrapped conditions) and structural erosion under the gate.

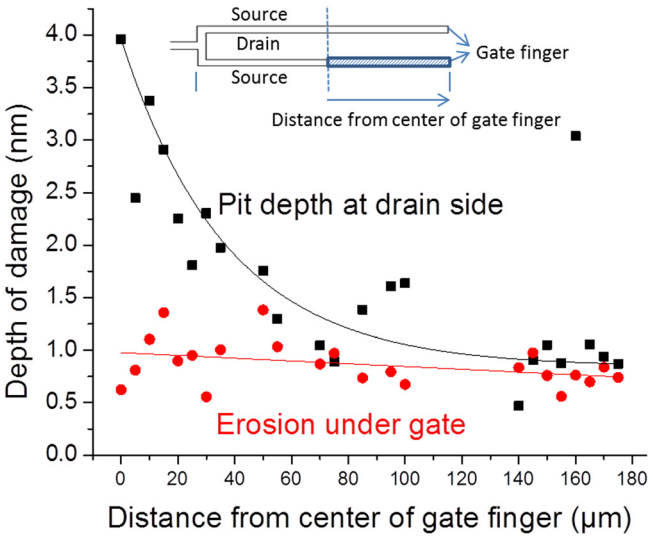

FIG. 9. Distribution of pit/trench depth and under-gate erosion depth along half of the gate width for the device with I_{Dmax} degradation of 21.6%. Each point in the graph represents an average value across a 5 μm scan.

IV. DISCUSSION

Our high-power stress experiments reveal pit and trench formation under the gate edge on the drain side of GaN HEMTs that is of a similar nature as produced under OFF-state stress.[9,19,20,27] We show for the first time that structural degradation correlates strongly with drain current degradation produced under high-power stress conditions. This has been observed in the OFF state but not under high-power stress. We also report for the first time prominent erosion of the semiconductor under the gate which correlates with channel resistance degradation.

The nature of our study precludes us from identifying the detailed origin of the observed degradation. Nevertheless, according to Ref. 9, a possible reason for pit and trench formation under the gate edge is electrochemical reactions of $Al_xGa_{1-x}N$ with water. Since the devices used for this study are encapsulated but not in hermetic packages, humidity could have crept in and contributed to the structural damage that is observed at the gate edge.

Following the approach of Li,[27] we can evaluate the stress temperature dependence of the observed degradation phenomena by studying the evolution of the geometry of these features across the width of the device. Towards this end, multiple 5 μm $\times$ 5 μm AFM scans have been taken across the entire half of one gate finger. The pit/trench and under gate erosion depth obtained from all traces (about 23) in each scan were averaged. Fig. 9 shows the average pit depth and under gate erosion depth as a function of gate finger location starting from the center of the gate, in steps of 5 μm. Pit depth is the largest at the center of the gate finger and it decreases towards its end. This is consistent with a thermally accelerated degradation process, as was found in Ref. 27. Temperature accelerated degradation of the drain current is also evident in Fig. 1. Furthermore, as described in Ref. 31, the activation energies obtained from the degradation of these devices under high-power DC stress range from 0.84 eV to 1.04 eV. In experiments carried out on similar technologies where devices are stressed under OFF state conditions, activation energies of 1.05 eV (Ref. 36) and 1.12 eV (Ref. 34) have been reported. The close values of our obtained activation energies with those under OFF-state stress conditions suggest a common physical origin for degradation. The erosion under the gate, on the other hand, does not show an obvious position spatial dependence indicating that this degradation mechanism is relatively temperature independent. Understanding the origin of this will require further studies.

We have also studied the relative degradation of the two gate fingers of each transistor. For all our tested devices, we find that one finger always suffers greater structural damage than the other finger. We suspect this to be due to misalignment during the fabrication process which leads to an asymmetric electric field or self-heating distribution. In fact, in all devices we have studied, we find that the gate finger that is closest to its neighboring drain contact, as measured by SEM, suffers the greatest damage.

Two physical processes could be responsible for this. One is an electric field driven mechanism which is known to strongly enhance pit formation in the OFF state.[20] The shorter the gate-drain gap, the greater the electric field although only at high enough voltage. Another possibility is device self-heating. It might well be the case that the closer the drain contact is to the gate, the hotter this region becomes with the consequence of accelerating degradation.[37]

V. CONCLUSIONS

We have stressed AlGaN/GaN HEMTs under high-power DC and high-temperature condition and observed the delaminated device surface under SEM and AFM. The stressed samples developed pits and trenches under the gate edge on the drain side of the device similar to those observed under OFF-state stress conditions. For the first time, we demonstrate a direct correlation between electrical degradation and structural degradation under high-power stress. The structural degradation is also found to be thermally activated which agrees well with the thermally activated I_{Dmax} degradation. In addition, we have also observed erosion under the entire gate region,

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something that has not been reported before. This is shown to correlate with the degree of degradation of the channel resistance. The recognition of a unified degradation mechanism under high-power stress and OFF-state stress suggests the possibility of developing a lifetime model with predictive capabilities under a broad range of operating conditions.

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