A 0.68V 0.68mW 2.4GHz PLL for ultra-low power RF systems

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***Abstract*— A 2.4GHz PLL consuming 0.68mW has been implemented in 65nm LPCMOS for use in ultra-low power Bluetooth Low Energy (BLE) applications. VCO, charge pump and dynamic flip-flop design optimization allow low voltage operation at 0.68V, bringing down dynamic power. The integer-N PLL covers all BLE channels and has a phase noise of −110dBc/Hz at 1MHz offset. To extend operation to extremely low duty cycles, extensive power gating is applied to bring the leakage power down to 170pW.**

***Index Terms*— PLL, 2.4GHz, RF, sub-0.7V, low power, low voltage, Bluetooth Low Energy, BLE, leakage, low duty cycle**

I. Introduction

Narrowband RF systems rely on stable, accurate LO generation to function reliably. PLLs operating from a crystal reference provide these stable LOs, but typically consume a large amount of power and set limits to the overall RF power. However, since communication costs dominate wireless sensor systems' power budgets, schemes to reduce PLL power can lead to significant battery life improvements. One approach has been to eliminate the PLL and use RF resonators such as FBARs [1]. Significant power reduction is feasible, but compatibility with standards such as Bluetooth Low Energy (BLE) is compromised because of insufficient frequency coverage.

In this work, we aim to address LO power generation, in the 2.4GHz ISM band, through a low-voltage PLL optimized for power consumption. Previous low-voltage PLLs such as [2] and [3] have shown operation down to as low as 0.5V, but the implementations still consume significant power ($>$ 2mW). On the other hand, works such as [4] and [5] demonstrate low power PLLs operating at nominal voltages such as 1V, leaving room for further reduction through voltage scaling. For example, a recent work presented a 0.3V PLL architecture that also has ultra-low 780μW power consumption [6].

The PLL in this work is part of a complete BLE transmitter, optimized for leakage in addition to active performance [7], for use in extremely energy constrained low duty cycle systems. The PLL is designed in 65nm LPCMOS to co-optimize RF and leakage performance. The PLL functions down to 0.68V and has a power consumption of 680μW. The following sections discuss the PLL architecture and circuit optimizations along with measurements from a testchip.

II. PLL Architecture and Circuit Blocks

Figure 1 shows the architecture of the integer-N PLL. A 12MHz crystal oscillator is divided down to 1MHz, allowing the PLL to provide 2MHz channel spacings, as required by BLE. The 12MHz crystal output is also used by the digital baseband in the full system. The divider in the feedback path includes a fixed divide-by-2 operating at 2.4GHz and a 32/33 dual-modulus prescaler [8] running at 1.2GHz, followed by a programmable divider. True Single Phase Clock (TSPC) flip-flops are used to enable low-voltage operation. The 32/33 prescaler is the largest value feasible to achieve complete channel coverage in the integer-N architecture. This minimizes the operating frequency of the programmable divider to 37MHz which is easily achieved at 0.68V using standard static logic-based synthesis. It should be noted that all 802.15.4 channels (with 5MHz spacing) can also be produced by simply replacing the crystal with a 15MHz one (making the PLL reference 1.25MHz). The feedback loop is designed for a phase margin of 40° and a bandwidth of 50kHz. Values of $R_1 = 400\text{k}\Omega$, $C_1 = 14\text{pF}$, $C_2 = 1.2\text{pF}$, $R_3 = 250\text{k}\Omega$ and $C_3 = 2\text{pF}$ are used in the third-order loop filter.

A. Charge Pump

Low voltage operation of the Charge Pump gives a linear reduction in power consumption, but limited output voltage range is a significant challenge at low supply voltages [6]. For example, even with subthreshold operation, at a supply of 0.68V, the linear output range is only 380mV (assuming 150mV saturation). Since some of this linear range is required to accommodate overshoot in the transients, the usable output range is only about $0.2 - 0.3\text{V}$.

A second challenge for low power operation of the charge pump is filtering of reference spurs arising from charge sharing. This is typically mitigated by analog voltage buffers that, when $\overline{\text{UP}} = 1$ or $\overline{\text{DN}} = 1$, bias the current mirror at the charge pump output voltage. To avoid significant energy overhead of an analog buffer, [4] proposed a biasing scheme using diodes. This is shown in Fig. 1 with transistors MN_1 and MP_1. The current mirrors are now biased at fixed voltages set by the diode-connected transistors. At low supply voltages, with the low inherent output voltage range of the charge pump, this fixed-voltage biasing reduces reference spurs by 15dB.

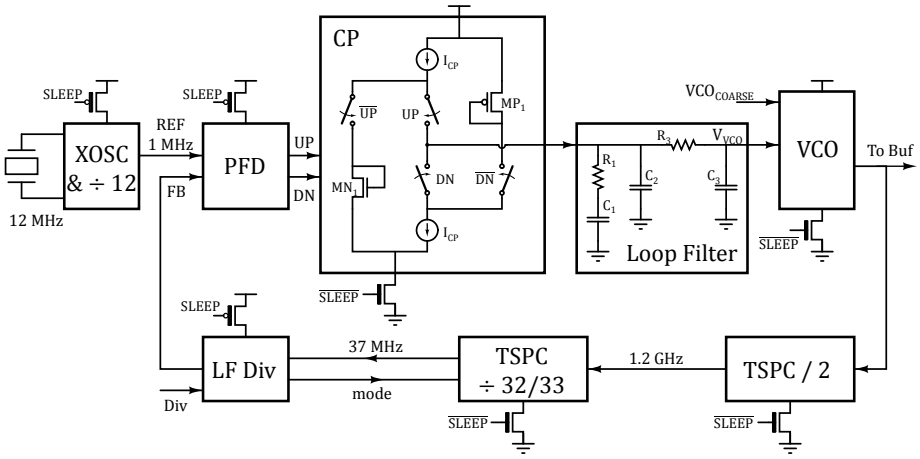


Fig. 1. Top level block diagram of the low-voltage PLL including the charge pump implementation and power gating switches.

B. VCO

The small voltage range of the Charge Pump imposes design constraints on the VCO. For a 300mV range, simulated $C_{\mathrm{Max}}/C_{\mathrm{Min}}$ of the varactors is only $1.2\times$. Hence, using a single varactor to cover the entire 2.4GHz band would lead to a large fixed capacitance, which would reduce the inductance required for resonance, thereby increasing power. In addition, the VCO gain would be $>$ 300MHz/V and lead to degraded output spectrum due to noise and coupling onto the VCO control voltage. We mitigate this problem by including a closely-spaced digitally tuned coarse capacitor bank (Fig. 2) that centers the VCO close to the required frequency and lets the PLL settle around that. Figure 3 shows the measured VCO response. With a 14.4MHz coarse frequency step and an 87MHz/V varactor gain, 200mV of the charge pump linear output range is utilized, satisfying the constraints.

A cross-coupled inverter architecture is chosen for the low-voltage VCO to minimize power. The oscillator swings rail-to-rail and power consumption is lower than a NMOS-only architecture and does not suffer adversely from shoot-through current due to the low supply voltage. However, one challenge of operating this at 0.68V is that the transistors are biased in subthreshold, leading to large sizes and associated parasitic capacitance. In order to mitigate this, body-biasing is applied to the transistors to increase current for the same transistor size, thus leading to smaller transistors. But, providing the bias voltages for the NMOS and PMOS separately is a challenge with a limited power budget. We propose a self-body-biasing scheme (Fig. 2) where bodies of the NMOS and PMOS are tied together. The body diodes self-bias at $V_{\mathrm{BODY}} \approx V_{\mathrm{DD}}/2$ (<20mV variation across corners). Since V_{DD} is low, the forward current in the body diodes is negligible. Simulations show a $1.5\times$ reduction in the transistor sizes, thereby significantly reducing parasitic capacitance.

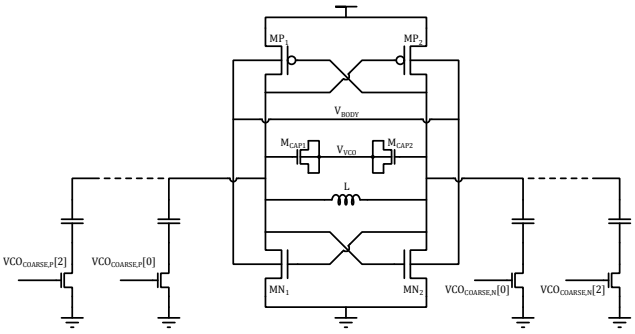


Fig. 2. Implementation of the low-voltage VCO with self-body-biasing and coarse frequency tuning.

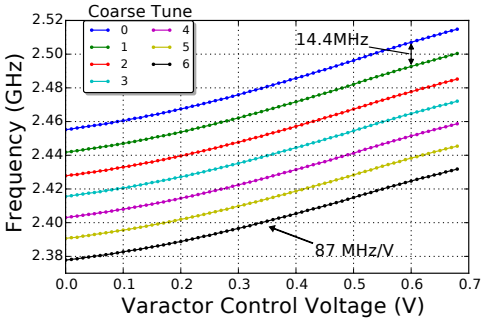


Fig. 3. Measured VCO tuning characteristics show coverage of the 2.4GHz ISM band.

C. Divider

Low voltage dividers require careful design to achieve functionality at RF. To achieve the best programmability, a

flip-flop-based architecture such as a dual-modulus divider is necessary, as opposed to an injection-locked divider such as in [6]. Since static flip-flops in our process do now work at 2.5GHz below 0.9V, we apply a dynamic TSPC logic style [8]. Power savings are achieved through both voltage scaling and lower switching capacitance in the smaller dynamic flip-flops. Figure 4 shows the 2.5GHz divide-by-2 circuit with the TSPC flip-flop and the relative sizing of the devices used to achieve functionality at 2.5GHz across corners. The same flip-flop is used in the 32/33 prescaler. An alternative is to use CML logic styles, which have been shown to achieve even lower voltage operation [2], [3], but could have higher power consumption.

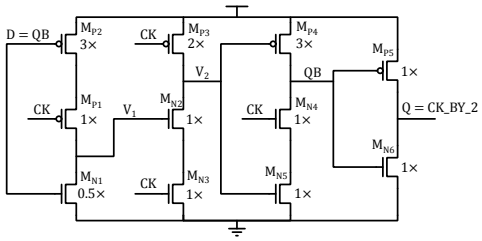


Fig. 4. Implementation of the True Single Phase Clock (TSPC) flip-flop used in the low-voltage 2.5GHz frequency divider.

D. Leakage Management

As indicated in Sec. I, this PLL has been designed for an ultra-low-leakage transmitter. Power gating has been applied to all blocks, as shown in Fig. 1. Thick oxide NMOS switches are used in most cases, with PMOS switches used to gate standard cell-based circuits. The resulting leakage power of the PLL is 170pW. The transmitter system in [7] that uses this PLL also provides a negative bias voltage around -0.2V in sleep. When this is used to strongly cutoff the NMOS switches, the total PLL leakage reduces to 27pW.

III. Measurements

The PLL was fabricated in 65nm LPCMOS. Figure 5 shows the die photo with the PLL blocks identified. The PLL occupies a core area of 0.2mm^2.

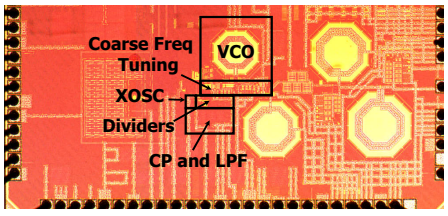


Fig. 5. Die photo of the PLL designed in 65nm LPCMOS.

All core circuits operate at 0.68V. A 1.2V rail, generated by a charge pump running from the crystal, powers various switches in the design, including the power gating switches. This 1.2V rail consumes $< 2\mu$W in active mode. The total power consumption of the PLL is 680μW. The distribution of power in the various blocks is shown in Fig. 6. A majority of the power is consumed by the VCO.

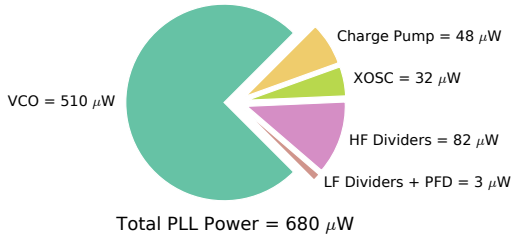


Fig. 6. Distribution of power in the various blocks of the PLL.

A 10MHz wide spectrum of the PLL output is plotted in Fig. 7. The spurs from the 1MHz reference are lower than -50dBc. There is also a -55dBc spur at 12MHz offset (not shown) due to coupling from the XOSC. Figure 7 also shows a 15dB reduction of spurs at 1MHz and 2MHz when enabling the Charge Pump spur reduction technique.

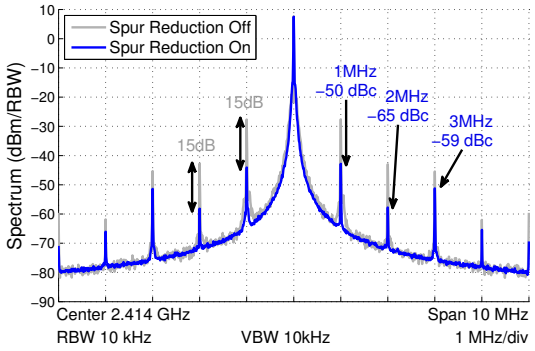


Fig. 7. Measured spectrum of the PLL output showing that spurs are lower than -50dBc and that spurs are reduced by 15dB by the charge pump bypass circuit

The phase noise of the PLL is plotted in Fig. 8. It shows a phase noise of -110dBc/Hz at 1MHz offset and -120dBc/Hz at 3MHz offset. This gives a VCO phase noise FOM of -182dB. This phase noise data was shown in the presentation of [7].

Figure 9 shows the transient response of the PLL. The startup time is 130μs for 20ppm settling. This reduces to 70μs for a step-frequency change of $+2$MHz. Both are below the requirements for BLE and 802.15.4. Figure 10 shows how the settling time can be reduced further by up to $2\times$ with higher charge pump current (and correspondingly higher total power). Similarly, the startup time of the PLL can be reduced down to 90μs.

Table I compares this work to recent PLLs in both the low voltage and low power spaces.

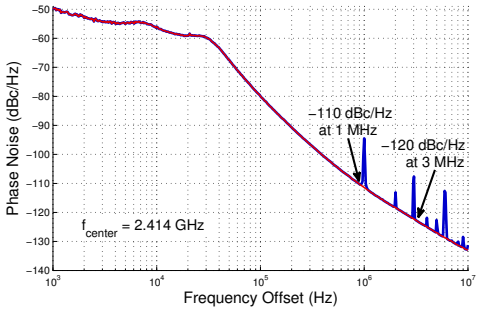
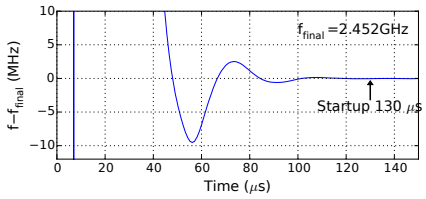
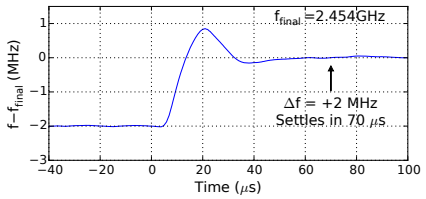


Fig. 8. Measured phase noise of the PLL at 2.414GHz.



(a)



(b)

Fig. 9. Measured 20ppm settling time of the PLL in a) Startup at 2.452GHz and b) Frequency step from 2.452GHz to 2.454GHz

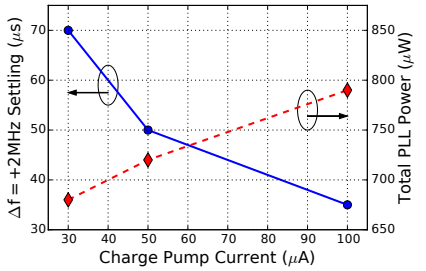


Fig. 10. Effect of increased I_{CP} on settling time.

IV. Conclusions

An integer-N PLL has been presented with ultra-low power operation at 680μW. It operates at a low voltage of 0.68V in a 65nm LPCMOS process. The VCO, charge pump and a TSPC dynamic flip-flop-based frequency divider were all optimized for the low voltage low power regime. The PLL achieves a phase noise of -110dBc/Hz at 1MHz offset and has a startup time of 130μs. Extensive power gating bring down the leakage power of the PLL to 170pW allowing operation in extremely low duty cycle applications. Overall, this PLL, if combined with a low power -10dBm PA such as in [1], could result in a sub-mW Bluetooth Low Energy (BLE) transmitter.

TABLE I
Comparison to recent PLLs

	This Work	[6]	[2]	[3]	[4]	[5]
Technology	65nm	65nm	180nm	90nm	90nm	40nm
Freq. (GHz)	2.4	2.0	1.9	2.4	2.4	2.4
PLL Type	Ana. Int-N	Dig. Int-N	Ana. Int-N	Ana. Frac-N	Ana. Frac-N	Dig. Frac-N
Supply (V)	**0.68**	0.3	0.5	0.65	1.2	1.0
Power (mW)	**0.68**	0.78	4.5	6	1.24	0.86
Ref Spur (dBc)	-50	-50^*	-44	-52	-63	-70
PN (dBc/Hz at 1MHz)	-110	-102	-121	-113	-113	-109
Lock Time (μs)	130	/	/	/	40	/
Leakage (pW)	**170**	/	/	/	/	/

$*$ Value read from Fig. 5

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