Broadband mm-Wave Signal Generation and Amplification in CMOS Using Synthetic Impedance

by

Pranav R Kaundinya

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Abstract

This thesis explores the concept of synthesizing tunable impedances by establishing the appropriate phase relationship between the drain voltage and drain current of a MOS transistor. A high frequency, wide tuning range 105-121GHz oscillator and a small-footprint 20-40GHz oscillator using synthetic resonance are presented. The concept of impedance synthesis is also used to generate a novel frequency-adaptive loss compensation scheme for distributed amplifiers which is shown to improve the bandwidth by 30%. The performance of these circuits was analyzed and simulated on a TSMC 65nm bulk CMOS process.

Thesis Supervisor: Ruonan Han
Title: Assistant Professor

Acknowledgments

Firstly, I would like to thank my advisor Professor Ruonan Han for giving me an interesting research area to explore and encouraging me throughout. I have learned a lot about how to do research and think about open-ended problems through my interactions with him. I really enjoyed the long hours that we spent discussing research and I am truly grateful for his mentorship. This thesis would not have been possible without the hours he spent with me brainstorming and refining ideas. I would also like to thank the other professors I had a chance to interact closely with during my time at MIT.

I would like to thank all the amazing friends I have made during my 4 years at MIT. These are people who are a constant source of inspiration and have supported me throughout my time here. I have learned a great deal from working with many of these friends. I am truly going to miss the late night discussions, dining hall conversations, and the student activities that I was a part of during my time here. Needless to say, my experience at MIT wouldn't have been the same without all of you.

Last but not least, my sincere thanks to my parents and my brother for supporting me in all my endeavours and making me who I am.

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Chapter 1

Introduction

The advancement of process technology has led to increasing interest in mm-wave applications in recent years. With modern CMOS processes boasting of f_T values of hundreds of GHz, mm-wave frequency sources and signal processing circuits have become more feasible.

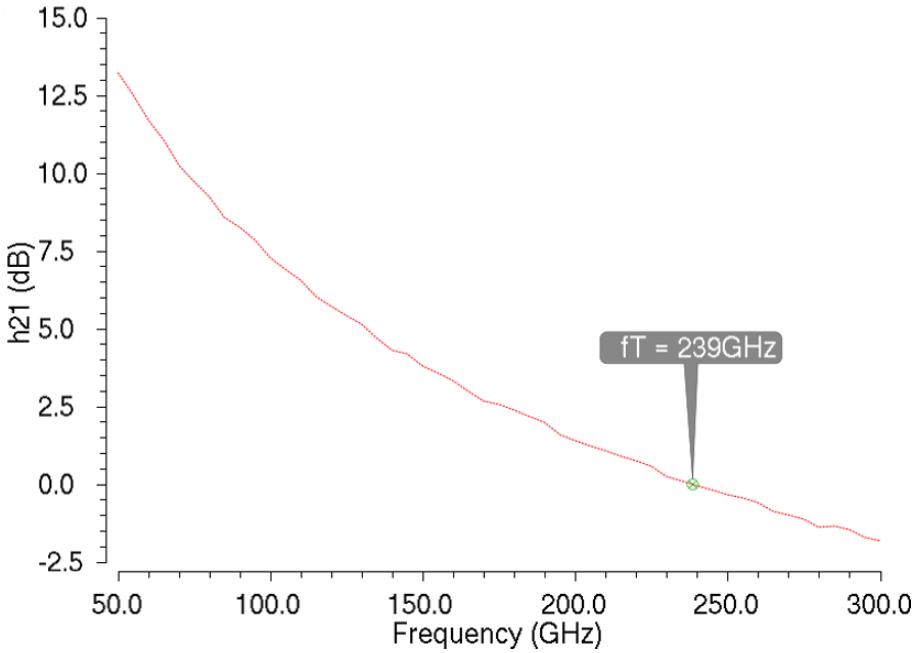


Figure 1-1: f_T of the 65nm bulk CMOS process used for simulations is roughly 240GHz

These mm-wave circuits have a variety of applications ranging from communication to imaging. 60 GHz wireless has been gaining traction in recent years and offers

potential for short range high-capacity data transmission [1]. Due to the fact that mm-Wave radiation can pass through clothing but is non-ionizing radiation (safe for use on humans), mm-Wave scanning systems [17] are already being used at airport security checkpoints. Automobile collision avoidance systems use mm-wave radar systems such as FMCW (frequency-modulated continuous wave radar) in which a transmitter centered around 80-90GHz sweeps the transmitted frequency and the beat frequency between the transmitted and reflected waves is used to obtain ranging information [19].

Figure 1-2: Potential applications for the mm-wave solutions developed in this thesis

Despite advancements in high-frequency CMOS, there are still several challenges of high frequency oscillator and amplifier design. The work described in this thesis targets the following challenges:

1. **Tunability:**

   Most of the applications mentioned above require broadband frequency sources and signal processing circuits. The most common approach to tuning at low

frequencies is to use varactors. However at higher frequencies, the tank capacitance is so small that it is often just composed of the parasitic capacitances of the active devices. Therefore, using a varactor is often not an option. Even in cases where a varactor may be used, the tuning range is very limited because the fraction of the tank capacitance that comes from the varactor is quite small.

2. **Footprint:**

   The development of on-chip inductors revolutionized RFIC design and enabled fully integrated solutions. However, inductors are very large and often occupy a majority of the die area. With the growth of portable devices, wearables, and IoT (Internet of Things) products, there is an increased demand for low-cost and small-footprint solutions (cost is closely related to die area).

3. **Loss:**

   Undesired sources of loss such as substrate loss, skin effect, and MOS gate resistance scale with frequency. The increased loss is an issue especially for distributed topologies that are often used to generate and amplify high frequency signals.

4. **Use of special process technologies:**

   Special process technologies such as SiGe are often used for high frequency applications. These process may provide higher f_T or larger breakdown voltage. Sometimes, these processes are used to provide special components such as varactors or diodes. The use of these special processes impedes the adoption and integration of high-frequency solutions into practical applications. In this work, only the components available in a standard CMOS process were used. All designs were developed using a TSMC 65nm PDK.

In this work, a new approach to generating tunable impedances by establishing the appropriate phase condition between the drain voltage and drain current of a MOS transistor is presented. While conceptually straightforward, this new framework can be used to design oscillators and amplifiers that overcome some of the challenges

described. It is important to note that the methods presented in this thesis are not limited to high-frequency applications. The designs that were implemented to demonstrate this concept were targeted towards frequencies ranging from 25GHz-125GHz because the benefits are more evident in this frequency range.

This thesis is organized as follows. Chapter 2 presents the concept of synthetic impedance generation. It discusses ways of establishing the required phase condition to synthesize a desired impedance and methods of tuning the synthesized impedance. The advantages and disadvantages of each of these approaches are also discussed. Chapters 3 and 4 describe specific examples of how synthetic impedance generation can be used to tackle some of the challenges of mm-Wave oscillator and amplifier design. Chapter 3 focuses on mm-wave oscillator design. The concept of synthetic resonance and various approaches to achieving synthetic resonance are explored in detail. Small-footprint and wide-tuning range oscillator designs using synthetic resonance are presented. Chapter 4 focuses on applications in high-frequency amplifier design. Distributed amplifiers (also known as travelling-wave amplifiers) are commonly used for ultra-broadband applications and have gain-bandwidth products in the hundreds of gigahertz. The factors that limit the bandwidth of such amplifiers are discussed. A novel frequency-adaptive loss compensation using synthetic impedance generation is presented. A distributed amplifier design incorporating this scheme is presented and the proposed compensation is shown to extend the bandwidth of the amplifier. Chapter 5 summarizes the contributions of this work.

Chapter 2

Synthesizing Impedances Using MOSFETS

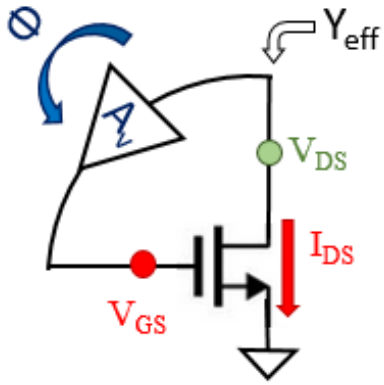
Active devices have long been used to emulate the behavior of passive components. The MOS transistor in triode is often used as a variable resistor in which the control terminal is the gate. The MOS transistor in saturation is often used as an active load due to its high output small-signal resistance r_o. The fact that this large small signal resistance is obtained with a very small DC voltage-drop is used to build high-gain amplifiers with low supply voltages. Tunable active inductors [15] developed through gyrator-C circuits are often used as substitutes for on-chip inductors [21].

In this chapter, a new approach to emulating passive components is presented in which the aim is to obtain a desired impedance by establishing the appropriate phase condition between the terminals of a MOSFET.

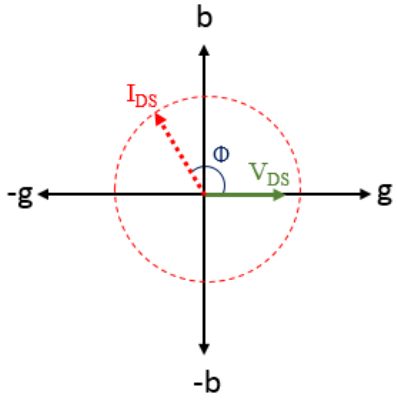
2.1 Concept

The basic idea behind synthesizing impedances is to establish a phase relationship between the V_{DS} and I_{DS} of a MOS transistor to obtain the desired impedance looking into the drain terminal of the transistor. At frequencies sufficiently below f_T, the gate voltage and drain current of the transistor are in phase. Therefore, this is can be achieved by enforcing the appropriate phase difference between V_{GS} and V_{DS} as

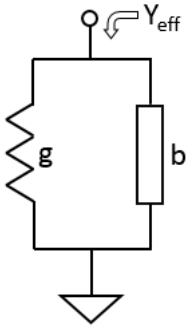
shown in figure 2-1a. If the large signal transconductance of the transistor is G_m and the voltage and current phasors are as shown in figure 2-1b, then the effective admittance as seen from the drain can be expressed as



(a) Synthetic impedance generation



(b) Admittance plane phasor diagram



(c) Equivalent circuit

$$
\begin{aligned}
Y_{eff} &= \frac{|I_{DS}|}{|V_{DS}|} e^{j\Phi} \\
&= A_v \frac{|I_{DS}|}{|V_{GS}|} e^{j\Phi} \\
&= A_v G_m e^{j\Phi}
\end{aligned} \tag{2.1}
$$

From equation 2.1, it is evident that by changing the transconductance of the transistor and the phase difference between V_{DS} and I_{DS}, it is possible to obtain any desired admittance. If A_v and Φ are frequency independent and $Im\{Y_{eff}\} \neq 0$, then Y_{eff} contains a parallel reactance that doesn't change with frequency. This scenario

is illustrated in figure 2-2. This results in an inductance or capacitance that decreases with increase in frequency (since ωL or ωC needs to remain constant, as ω increases, L or C need to decrease).

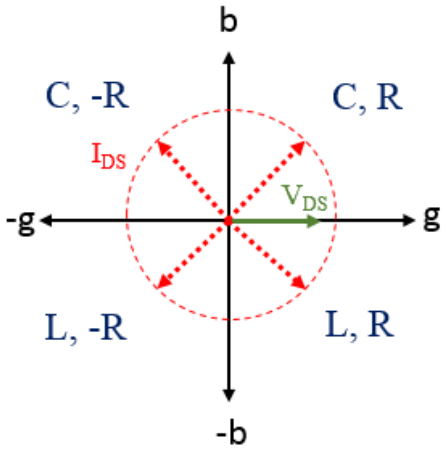


Figure 2-2: Constant reactance phasor

In order to emulate a frequency independent inductor or capacitor, $Im\{Y_{eff}\}$ needs to scale with frequency. From equation 2.1, one approach to making $Im\{Y_{eff}\}$ scale with frequency would be to exploit frequency variation in A_v and Φ. This can usually be implemented by the phase delay block in figure 2-1a. For example, if the phase delay block has a pole, as frequency increases, Φ will decrease by $\frac{\pi}{2}$ around the pole frequency and $Im\{Y_{eff}\}$ will vary correspondingly. Assuming that A_v remains same, the Y_{eff} vector rotates in the admittance plane as shown in figure 2-3. If the vector rotates towards the real axis, $Im\{Y_{eff}\}$ decreases with frequency, the network emulates an inductor (positive inductance if $Im\{Y_{eff}\} < 0$ and negative inductance otherwise). If the vector rotates towards the imaginary axis, $Im\{Y_{eff}\}$ increases with frequency, the network emulates a capacitor (positive capacitance if $Im\{Y_{eff}\} > 0$ and negative capacitance otherwise). Note that if a pole was used to obtain the frequency dependent reactance, A_v would also decrease as the frequency increases due to the impact of the pole on the magnitude response of the phase delay block.

Another application of frequency dependent impedance generation is discussed in chapter 4 in the context of frequency adaptive loss compensation.

From the discussion above, it is evident that the designer can only control Y_{eff} as a

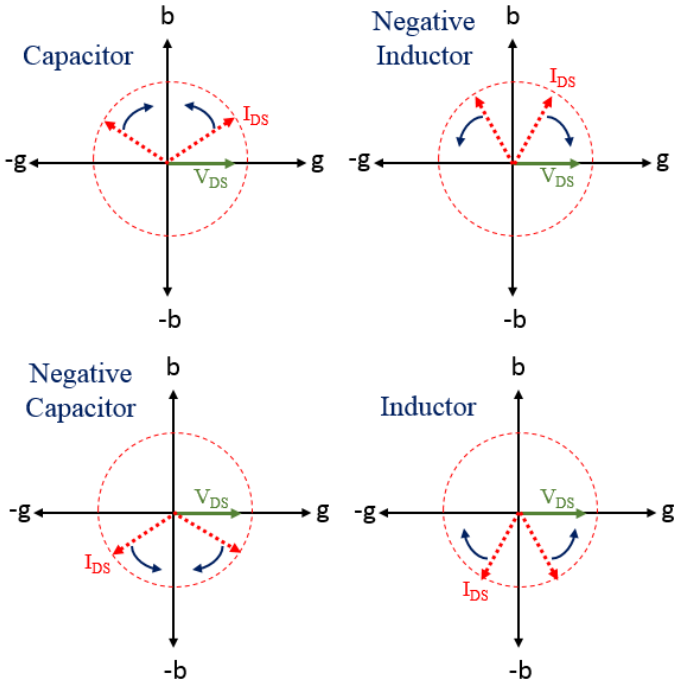


Figure 2-3: Frequency dependent reactance phasors

combined quantity and cannot separately manipulate the real and imaginary components. If the target impedance is an inductor, then the associated parallel conductance increases with frequency. This results in increased loss at higher frequencies (due to higher equivalent series resistance). While this could be an undesirable characteristic, this is true of ordinary inductors due to phenomena such as skin effect (discussed in section 4.1) that scale with frequency. On-chip components also typically have a peak Q frequency away from which the quality factor decreases.

2.2 Establishing Phase Condition

The primary component of a synthetic impedance generator is the phase delay block. The phase delay block can be implemented in a few different ways depending on the desired characteristics of the synthesized impedance. For example, in section 2.1, it was shown that in order to emulate a frequency-independent inductor or capacitor, the phase delay had to vary with frequency. Sometimes, the circuit in which the impedance is embedded can also dictate the type of implementation.

In this section, we discuss 3 distinct ways of implementing the phase delay block - using symmetry, using a passive network and using delay lines.

2.2.1 Symmetry

This approach is limited to circuits which naturally provide multi-phase signals. The idea is to sample two signals with a phase difference determined by the symmetry of the circuit as shown in figure 2-4. One of the signals is connected to the drain of the emulating transistor and the other signal is used to generate the out-of-phase drain current by connecting it to the gate of the transistor. Since the phase difference between the drain voltage and the drain current is fixed by the external circuit, this kind of implementation does not allow for frequency dependent impedance generation.

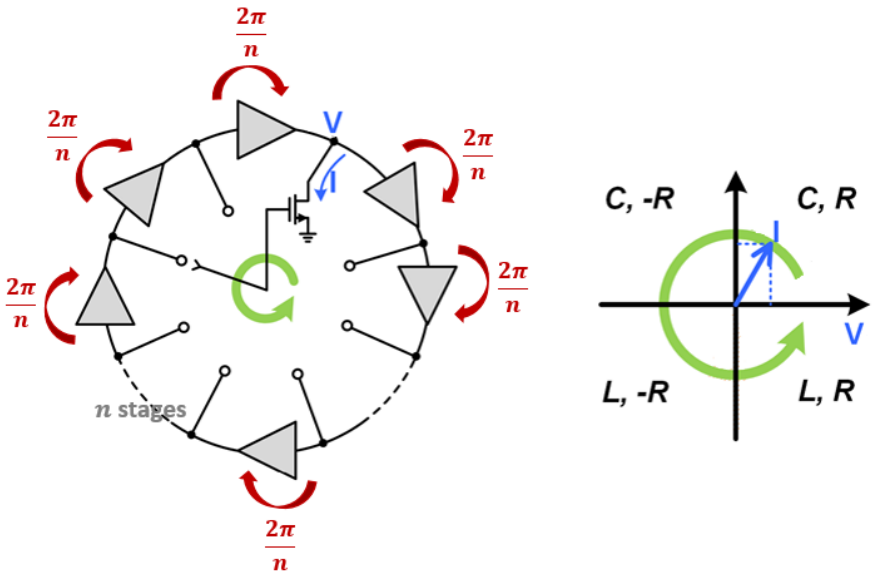


Figure 2-4: Establishing phase condition using symmetry

Oscillators are well suited for this kind of implementation because multi-phase signals are often easy to generate (for example in a ring oscillator). In chapter 3, this approach is used to implement a synthetic inductor in an oscillator.

2.2.2 Passive Network

This is the most general way to implement the phase delay block and is quite independent of the network in which the synthetic impedance is embedded. The idea is to introduce a passive network with poles and/or zeros that can shift the phase of the signal at the drain and feed it into the gate of the transistor. In section 3.3, a synthetic resonance oscillator using a passive network as the phase delay block is presented.

A simple network such as an RC low-pass filter can actually act as a phase shifter. The single-pole system results in the output voltage lagging the input voltage by $\frac{\pi}{2}$. This simple example can highlight some of the salient features and drawbacks of using a passive network to establish the phase condition. If the phase shift produced by the network is frequency-dependent, then the impedance generated is also frequency dependent, which could be a valuable feature as discussed in section 2.1. However, such a phase shifting network usually has a amplitude response that also varies with frequency. This could be undesirable, especially when the amplitude degrades severely at high frequencies. Further, the phase shifting network loads the input of the impedance generator and affects the effective impedance seen by the external circuit. Finally, the use of additional passive components could degrade performance. If inductors are used, it could lead to a large area overhead. If resistors are used, the noise performance could be severely degraded due to the added thermal noise. Some of these drawbacks can be overcome by carefully designing the phase shifting network.

2.2.3 Delay Lines

This approach is limited to travelling-wave oscillators and amplifiers. The phase delay block is implemented as an artificial transmission line segment. Since the phase delay of a transmission line segment increases with frequency, this type of implementation allows for frequency dependent impedance generation. The use of delay lines to manipulate the phase is described in section 4.2.

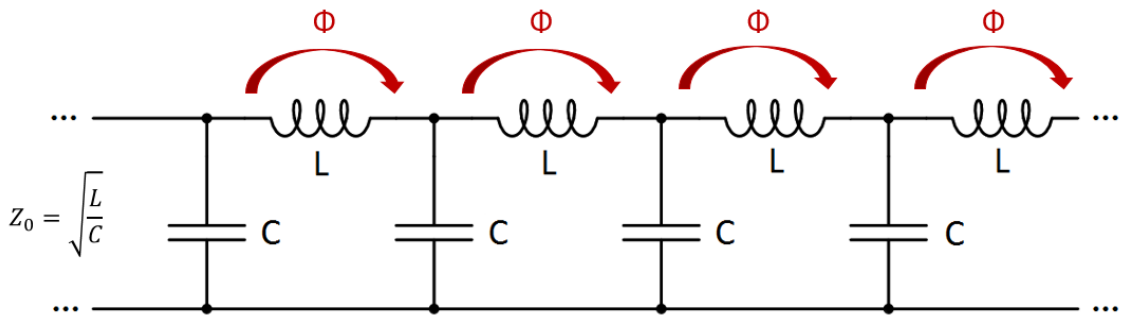


Figure 2-5: Establishing phase condition using delay lines

2.3 Tuning

One of the primary advantages of synthetic impedance generation is that the the impedance generated can be dynamically tuned. From equation 2.1, the two ways to tune the impedance are to change the transconductance G_m of the emulating device and changing the phase delay Φ of the delay block.

2.3.1 Transconductance Tuning

As the name implies, transconductance tuning involves changing Y_{eff} by varying G_m. This can be done by simply varying the DC bias of the emulating transistor. Since G_m is proportional to the overdrive voltage, it increases linearly with increase in the DC bias voltage. In section 3.2, transconductance tuning is used to tune a quadrature cross-coupled oscillator.

This tuning method has a few limitations. In a long-channel transistor, the carrier velocity is proportional to the applied electric field. However, for the large electric fields ($> 10^5 V/cm$) found in short-channel transistors, the carrier velocity saturates at about $\nu_{sat} = 10^7 cm/s$. Therefore, the transistor enters saturation at a lower value of V_{DS} and the saturation current is lower than expected. This phenomenon in short-channel MOSFETs is known as velocity saturation and it results in a smaller saturation current for a given overdrive voltage. Moreover, the current increases linearly with the overdrive voltage instead of increasing quadratically. This causes the transconductance to become independent of the overdrive voltage.

$$g_m = \begin{cases} \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) & V_{DS} < V_{DSAT} \\ W C_{ox} \nu_{sat} & V_{DS} > V_{DSAT} \end{cases} \tag{2.2}$$

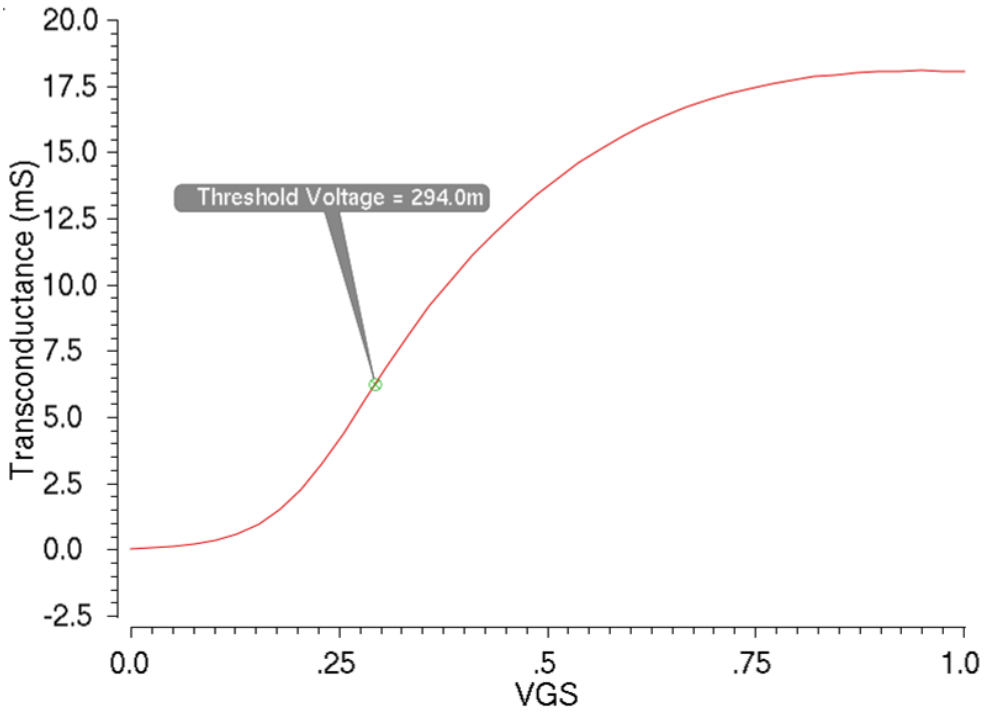


Figure 2-6: g_m saturation due to velocity saturation

For a transistor with 10 fingers with finger width $1\mu m$ and minimum length, the transconductance can be tuned from as $7mS$ to $18mS$ shown in figure 2-6. Beyond $0.8V$, the transconductance saturates with increase in V_{GS}. The only way to increase the transconductance tuning range is to increase the effective W/L of the device, but this results in increased parasitic capacitance that loads the circuit in which the impedance is embedded.

2.3.2 Phase Tuning

An alternative approach to tuning involves varying the phase delay Φ of the delay block. By rotating the current phasor in the admittance plane, the real and imaginary components can be varied such that the magnitude of the admittance remains

constant. This allows the susceptance or conductance to be varied over a large range - from 0 to $A_v G_m$ (magnitude of Y_{eff}). This tuning approach works for topologies that use a passive network or delay lines to establish the phase condition for generating the desired impedance. Phase tuning is used to tune oscillators in section 3.3. Note that topologies that use symmetry are restricted to using transconductance tuning.

A simple implementation of phase tuning consisting of an RC low-pass filter as the phase delay block is illustrated in figure 2-7. As the resistance of the RC phase delay block is increased, the pole $\frac{1}{RC}$ moves to a lower frequency. (figure 2-8) Therefore, at a given frequency, there is increased phase delay from the input of the phase delay block to the output.

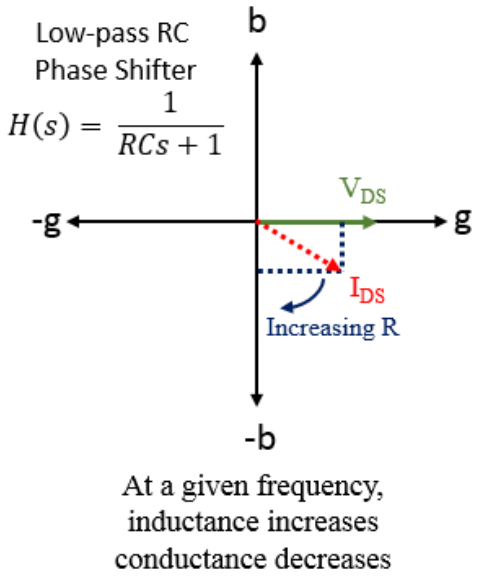


Figure 2-7: Admittance plane phasor diagram for phase tuning

Phase tuning has a few limitations. The phase difference between between the current and voltage phasors is typically not as well controlled as the transconductance of the transistor. Phase tuning is typically implemented by introducing poles and zeros using passive components, and varying the locations of these poles and zeros. However, this control system is non-linear (the phase doesn't vary linearly about poles and zeros). Further, the fact that additional passive components are required could be a disadvantage as discussed in section 2.2.2.

Another limitation is that it is not possible to use this approach to tune pure

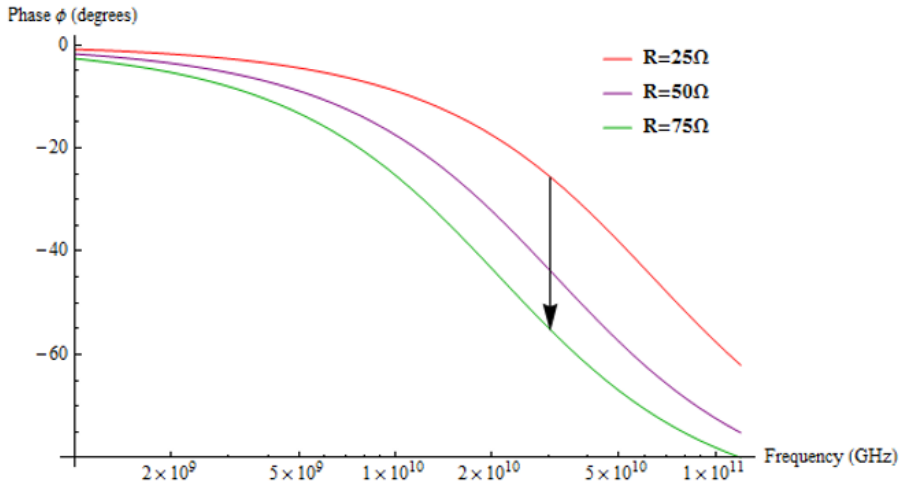


Figure 2-8: Bode plot for phase tuning

resistances or reactances because the tuning works by increasing one component while decreasing the other. Since transconductance tuning simply varies the magnitude, it can be used for this purpose.

Chapter 3

mm-Wave VCOs using Synthetic Resonance

The concept of synthetic impedance generation can be used to emulate passive components and achieve synthetic resonance. This chapter shows how tunable synthetic inductors can be used for developing wide-tuning range oscillators. It also demonstrates that synthetic inductors can potentially entirely replace physical on-chip inductors, significantly reducing the die area of VCOs.

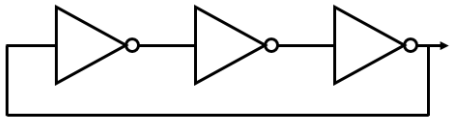
A survey of common mm-Wave oscillator topologies is presented followed by a description of synthetic resonance based oscillators.

3.1 mm-Wave Oscillator Topologies

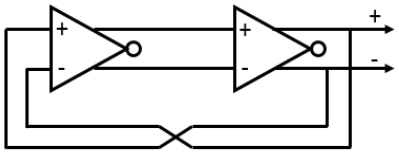
3.1.1 Ring Oscillators

Ring oscillators are widely used for applications requiring a small footprint and a wide-tuning range. A ring oscillator basically consists of a set of inverters connected in the configuration shown in figures 3-1a and 3-1b. If single-ended inverters are used, then the number of inverters in the ring must be odd. The phase difference across each inverter is $\frac{2k\pi}{n}$ where the number of inverter stages in n. The frequency of the oscillator is given by $\frac{1}{2nT}$ where T is the propagation delay of each inverter. Ring oscillators

can achieve moderately high oscillation frequencies - in a 65nm bulk CMOS process, the maximum oscillation frequency of a ring oscillator is about 16GHz. However, this is too low for mm-Wave applications such as 60GHz wireless, automotive radar, spectroscopy, etc.



(a) Ring oscillator



(b) Differential ring oscillator

One of the major drawbacks of ring oscillators is the poor phase noise performance. One of the reasons for high phase noise is the lack of passive components to filter out some of the noise. The effective Q of a 3-stage ring oscillator is 1.3 [14] which is far lower than the Q of an on-chip LC tank. [1] Another fundamental reason for high phase noise arises from an analysis of the ring oscillator ISF [6]. Intuitively, the oscillator is most vulnerable to jitter around the zero-crossing transitions. This is also when both the NMOS and PMOS transistors are on and injecting current into the output node. A 3-stage ring oscillator in 65nm bulk CMOS oscillating at 16GHz has a phase noise of -69dBc/Hz at a 1MHz offset. Due to the low power consumption, the figure of merit (FoM) [2] of the ring oscillator is respectable at 152dBc/Hz.

However, ring oscillators have a very large tuning range. By controlling the amount current through the inverters, the propagation delay can be varied, thereby changing the frequency of the ring oscillator. Additionally, because ring oscillators

[1] According to Leeson's phase noise model, the phase noise is a strong function of Q

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3.1}$$

where F and ω_{1/f^3} (sometimes approximated as the flicker noise corner frequency) are empirical fitting parameters.

[2] The figure of merit used for comparing oscillators in this work is defined as

$$FOM_{VCO} = 20\log\left(\frac{f_{VCO}}{\Delta f}\right) - \mathcal{L}_{VCO}(\Delta f) - 10log(P_{VCO|mW})$$

where f_{VCO} is the oscillation frequency of the VCO, $\mathcal{L}_{VCO}(\Delta f)$ is the phase noise in dbc/Hz, and $P_{VCO|mW}$ is the power dissipated in mW

don't have inductors, they occupy a very small area. Due to their low power consumption and small footprint, they are a popular choice for digital applications.

3.1.2 LC Oscillators

LC oscillators are more commonly used for high frequency applications. A generic LC oscillator can be modeled as an lossy parallel LC tank with a negative resistance cell in parallel to compensate the loss. Due to the presence of passive tuning components, LC oscillators produce high-Q outputs with a good phase noise performance. These working of these oscillators is explored in more detail in section 3.2

3.1.3 Standing Wave and Traveling Wave Oscillators

These oscillators are constructed by establishing standing or traveling waves along a transmission line and compensating loss to sustain oscillation by using some negative resistance. These are commonly used for high-frequency applications and are in fact limited to such applications due to the area cost (the area scales with operation frequency since the transmission line lengths are proportional to the wavelength). For example, a quarter wavelength standing-wave oscillator at 30GHz requires a transmission line of length 2.5mm. Since these oscillators don't use passive components and don't offer opportunities for synthetic impedance generation, they will not be discussed in further detail.

3.2 Quadrature LC Oscillator Using Synthetic Resonance

Chapter 2 discussed how various impedances can be synthesized by establishing the appropriate phase condition. This section explores how an inductance can be synthesized using the approaches described in Chapter 2. Being able to synthesize an inductance offers the following opportunities:

1. **Tunability:** The effective inductance of the synthesized impedance is tunable, so the frequency of the oscillator can be tuned using transconductance tuning. This eliminates the need for varactors, which enables the design of wide-tuning range oscillators at high frequencies. Current solutions to tuning high frequency oscillators such as resonant mode switching [9] or switching between LC tanks of different resonant frequencies involve large area overhead and suffer from non-idealities such as switching losses. Varactors also often require special processes and negative supply voltages, which impose additional constraints on the system.

2. **Reducing Footprint:** Since the synthesized inductance can resonate, it is possible to completely eliminate the on-chip inductors. This reduces the oscillator footprint enormously. A 1nH inductor in a 65nm bulk CMOS process occupies $0.04mm^2$ (figure 3-2), several times larger than the area of the rest of the oscillator.

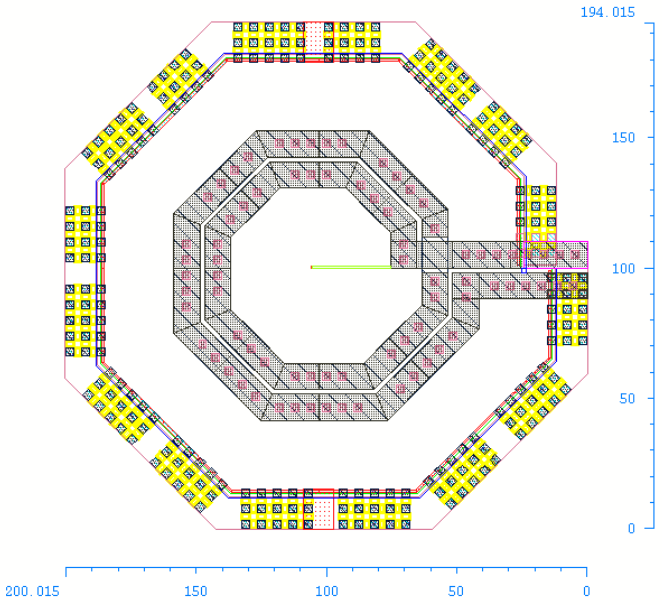


Figure 3-2: Footprint of 1nH spiral inductor

Modern RF receivers require accurate quadrature signals for modulation. Many efficient modulation schemes involve parallel mixing with quadrature LO outputs. One approach to obtaining quadrature signals is to post-process a given signal us-

ing a passive phase-shifting network to obtain quadrature outputs. Obtaining very accurate high-frequency quadrature outputs over the entire tuning range with minimal noise from the phase shifting network is hard. Alternately, a frequency divider can be used, but this significantly limits the output frequency and consumes a lot of power. A common approach to obtaining quadrature signals is to synthesize them simultaneously using a multi-phase oscillator such as a ring oscillator or multi-stage cross-coupled oscillator.

3.2.1 Synthetic Resonance in Multi-phase Oscillators

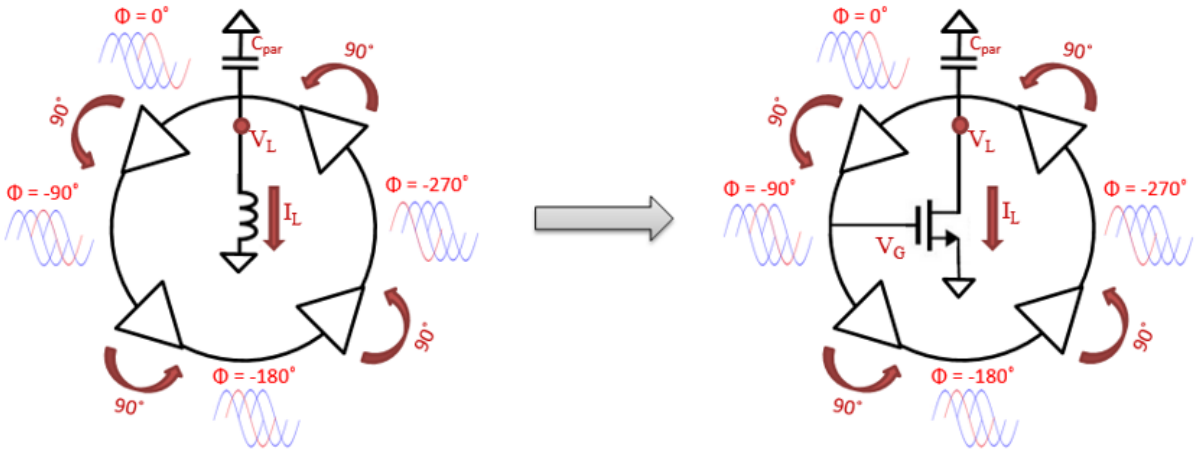


Figure 3-3: Synthetic resonance

Consider the circuit illustrated in figure 3-3. If the phase condition is setup so that the drain current lags the drain voltage by $\frac{\pi}{2}$, the synthesized impedance is inductive and can potentially resonate with the LC tank. The effective inductance as seen from the drain of the emulating transistor can be calculated as

$$Y_{eff} = -jG_m \tag{3.2}$$

$$L_{eff} = \frac{1}{\omega G_m} \tag{3.3}$$

Note that since symmetry was used to establish the phase condition, the effective

inductance is frequency dependent as discussed in section 2.1. However, at a certain frequency, the real and imaginary impedances of the virtual LC tank will resonate.

$$\left|\frac{1}{-jG_m}\right| = \left|\frac{1}{j\omega C}\right| \tag{3.4}$$

$$\omega = \frac{G_m}{C} \tag{3.5}$$

If most of the tank capacitance comes from the C_{GS} and C_{GD} of the coupling transistor,

$$\omega \approx \frac{G_m}{C_{GS} + C_{GD}} = \omega_T \tag{3.6}$$

Therefore, the transistor can theoretically oscillate at frequencies up to the cutoff frequency of the device f_T - the impedance generation itself doesn't limit the maximum oscillation frequency. In reality, due the parasitic capacitance at the drain node, the oscillation frequency is significantly below f_T.

Since the synthesized inductance is frequency dependent, the tank impedance around the resonant frequency behaves differently from the tank impedance of a conventional RLC tank. For a given tank parallel resistance R_P,

$$Z_{eff} = \frac{1}{j(\omega C - G_m) + \frac{1}{R_P}} \tag{3.7}$$

$$|Z_{eff}| = \begin{cases} \frac{1}{\sqrt{G_m^2 + (\frac{1}{R_P})^2}} & \omega << \omega_0 \\ R_P & \omega = \omega_0 \\ \frac{1}{\sqrt{(\omega C)^2 + (\frac{1}{R_P})^2}} & \omega >> \omega_0 \end{cases} \tag{3.8}$$

To find the 3dB bandwidth of the synthetic resonance oscillator,

$$|Z_{eff}(j\omega_{3dB})| = \frac{1}{\sqrt{2}} \times R_P \tag{3.9}$$

$$\omega_{3dB} = \frac{G_m \pm \frac{1}{R_P}}{C} \tag{3.10}$$

$$\Delta\omega_{3dB} = \frac{2}{R_P C} \tag{3.11}$$

Using the definition of quality factor that relates it to the bandwidth, we can compute an effective quality factor

$$Q = \frac{\omega_0}{\Delta\omega_{3dB}} \tag{3.12}$$

$$= \frac{\omega R_P C}{2} \tag{3.13}$$

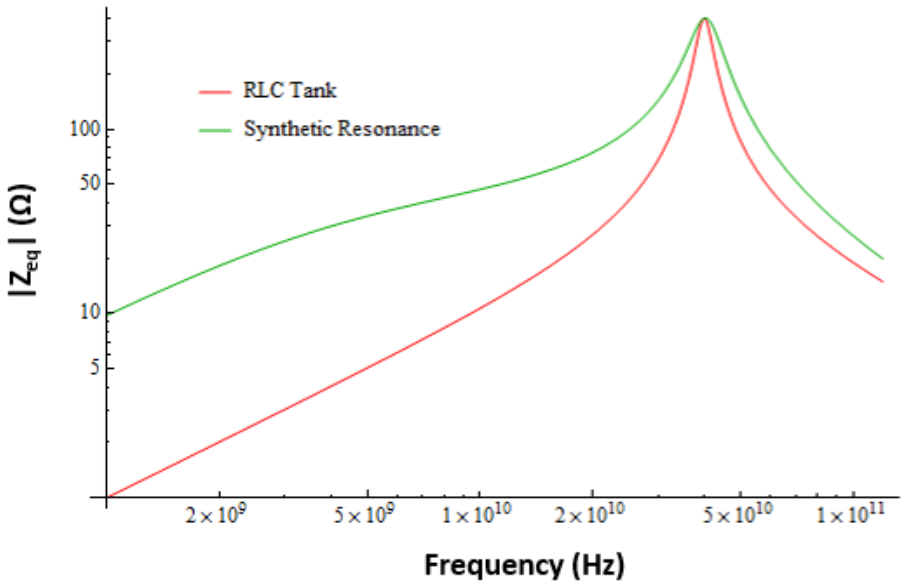


Figure 3-4: Synthetic resonance tank impedance

Therefore, for a given tank resistance R_P, the synthetic resonance oscillator has half the quality factor as a conventional LC oscillator. The tank admittance of a

synthetic resonance oscillator and conventional LC oscillator are plotted in figure 3-4. The diminished Q hurts the phase noise performance of synthetic resonance oscillators, but also allows them to operate at a wide range of frequencies.

3.2.2 Quadrature Cross-coupled Oscillator

The quadrature cross-coupled oscillator is a common quadrature oscillator topology. It consists of two cross-coupled oscillators that are coupled as shown in figure 3-5.

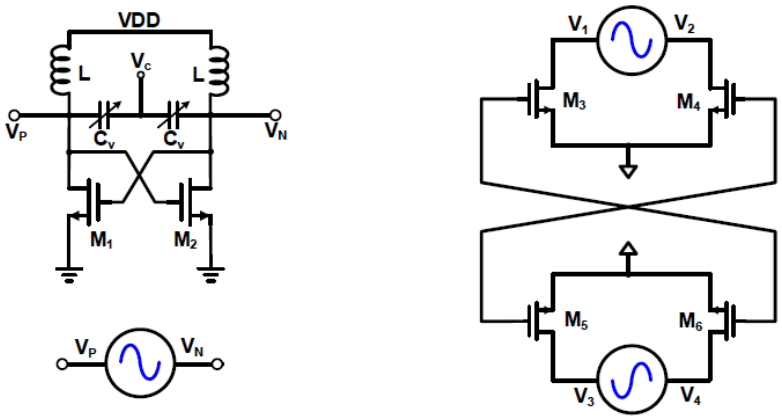


Figure 3-5: Quadrature cross-coupled oscillator

Using symmetry and applying the Barkhausen criteria for phase, the viable oscillation modes are those in which successive outputs have a phase difference of $\frac{2k\pi}{4}$. While this indicates that there are multiple viable modes, only the mode for which the startup condition is satisfied is actually sustainable. Usually, the mode corresponding to $k = 1$ is the dominant mode and the other oscillation modes are suppressed. However, if alternate lower frequency modes are present, they can be suppressed by adding an RC high-pass filter at the coupling nodes.

While the quadrature cross-coupled oscillator looks very similar to the conventional cross-coupled oscillator, the oscillation frequency of the quadrature oscillator is shifted from the natural oscillation frequency. This is a result of synthetic resonance and can be exploited to develop wide-tuning range and small footprint oscillators.

3.2.3 Synthetic Resonance in a Quadrature Cross-coupled Oscillator

A quadrature cross-coupled oscillator provides outputs that are phase shifted by $\frac{\pi}{2}$ using symmetry. Following the discussion in section 2.2.1, it seems like this circuit provides an opportunity for impedance synthesis. Further, since the signals are shifted in phase exactly by $\frac{\pi}{2}$ at all frequencies, there is a potential to produce purely reactive or resistive impedances.

A closer look at the circuit reveals that the coupling transistors are in fact acting as synthetic impedance generators. The drain of each coupling transistor is connected to one output of the quadrature cross-coupled oscillator, while the gate is connected to another output that is phase shifted by $\frac{\pi}{2}$. This means that the synthesized impedance appears either purely capacitive or purely inductive. If the gate voltage of the coupling transistor lags the drain voltage, then the coupling transistor appears as a synthesized inductor in parallel with the tank inductance.

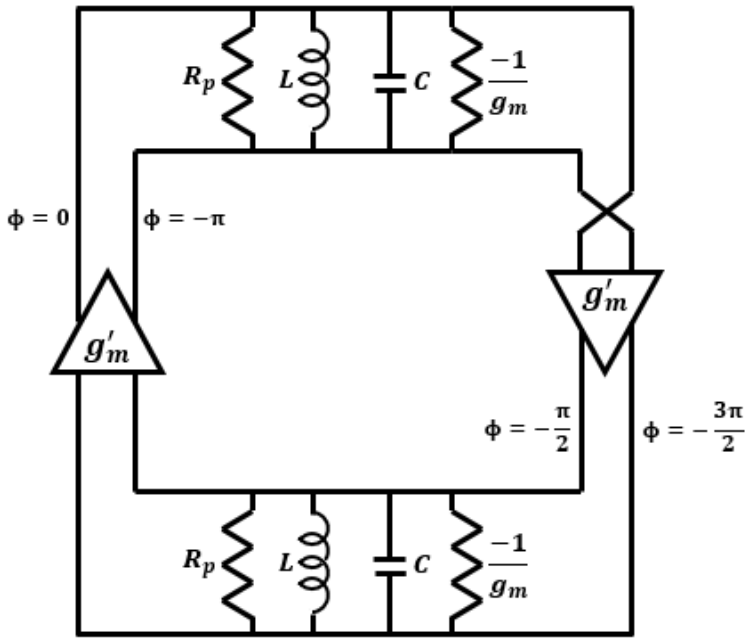


Figure 3-6: Linear model of quadrature cross-coupled oscillator

A calculation of the oscillation frequency of the quadrature cross-coupled oscillator reveals that the coupling transistors shift the oscillation frequency from the natural

oscillation frequency of the LC tank $\frac{1}{\sqrt{LC}}$. A linearized model of the circuit is shown in figure 3-6. The equivalent impedance of each RLC tank is given by

$$Z_{eq}(s) = sL||\frac{1}{sC}|| - \frac{1}{g_m}||R_P \tag{3.14}$$

$$= \frac{sL}{s^2LC + sL(\frac{1}{R_P} - g_m) + 1} \tag{3.15}$$

Assuming that the negative resistance compensates the tank loss,

$$G(s) = -g_m'^2\left(\frac{sL}{s^2LC + sL(\frac{1}{R_P} - g_m) + 1}\right)^2 \tag{3.16}$$

Then the loop gain can be calculated as

$$G(s) = -g_m'^2\left(\frac{sL}{s^2LC + 1}\right)^2 \tag{3.17}$$

Applying the Barkhausen criteria for oscillation, $|G(j\omega)| = 1$ and $\angle G(j\omega) = 2k\pi$

$$-g_m'^2\left(\frac{sL}{s^2LC + 1}\right)^2 = 1 \implies \frac{g_m' sL}{s^2LC + 1} = \pm j \tag{3.18}$$

$$s = j\omega \implies \frac{g_m' \omega L}{\omega^2 LC + 1} = 1 \tag{3.19}$$

$$\omega^2 \pm \frac{g_m'}{C}\omega L - \omega_0^2 = 0 \tag{3.20}$$

which results in two solutions

$$\omega_1 = \frac{g_m'}{2C} + \omega_0\sqrt{\left(1 + \frac{g_m'^2 L}{4C}\right)} \tag{3.21}$$

$$\omega_2 = -\frac{g_m'}{2C} + \omega_0\sqrt{\left(1 + \frac{g_m'^2 L}{4C}\right)} \tag{3.22}$$

Intuitively, as g'_m increases, the synthesized inductance $\frac{1}{\omega_0 g'_m}$ decreases and the oscillation frequency increases. This indicates that the correct solution is ω_1 as simulations also confirm. For practical values of g'_m, L and C,

$$\frac{g'^2_m L}{4C} << 1 \implies \omega_1 \approx \frac{g'_m}{2C} + \omega_0 \tag{3.23}$$

As expected, ω_1 converges to the natural oscillation frequency of the LC tank ω_0 as the coupling g'_m weakens. By varying the transconductance of the coupling transistors, the oscillation frequency can be varied.

In the following sections, designs of wide-tuning range and small-footprint oscillators using this concept are presented.

3.2.4 105GHz-121GHz Quadrature VCO

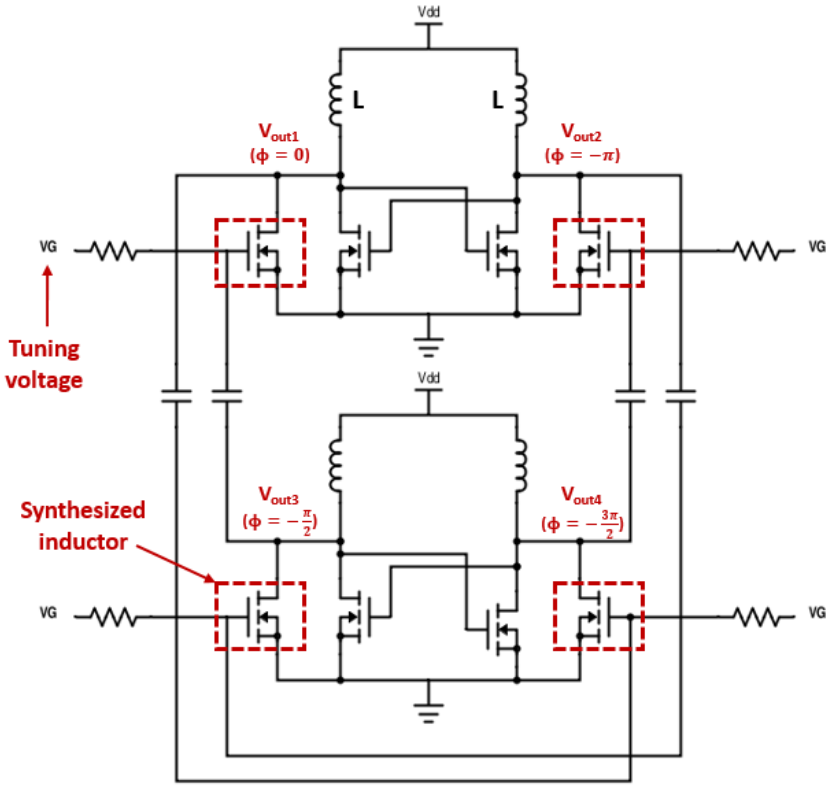


Figure 3-7: 105GHz-121GHz Quadrature VCO

Using the concept described in the previous section, a high frequency, wide-tuning range quadrature cross-coupled oscillator was designed and simulated. The design is shown in figure 3-7 and looks similar to a conventional quadrature cross-coupled oscillator. By varying the DC bias of the gate of the inductor emulating transistor, the oscillation frequency can be tuned. The cross-coupled transistors were sized to be as small as possible to meet the startup condition

$$g_m R_p > 1 \tag{3.24}$$

and obtain a respectable swing. This was done to minimize the contribution of the cross-coupled pair to the total tank capacitance and therefore maximize the oscillation frequency and the tuning range. The tank inductances were $170pH$ and had a quality factor of 15.

Analysis of the relationship between the coupling strength and the tuning range yields insight on the sizing of the coupling transistors. From the linear model developed in section 3.2,

$$\text{Tuning Range} = \frac{\Delta g'_m}{2C} \tag{3.25}$$

$$= \frac{\frac{W'}{L}\mu C_{ox}\Delta V_{ov}}{2(\alpha W' L C_{ox} + C')} \tag{3.26}$$

where

$$C' = C_{cross\_coupled} + C_{inductor} \tag{3.27}$$

$$\alpha W' L C_{ox} = C_{coupling} \tag{3.28}$$

$$\frac{2}{3} < \alpha < 1 \tag{3.29}$$

C_{ox} is the oxide capacitance per unit area $\frac{\epsilon_{ox}}{t_{ox}}$, α is a constant, and ΔV_{ov} is the

range of overdrive voltage over which the transconductance can be tuned (limited by velocity saturation as described in section 2.3.1). When the coupling transistor is small ($\alpha W'LC_{ox} << C_{cross\_coupled} + C_{inductor}$), the tuning range is given by

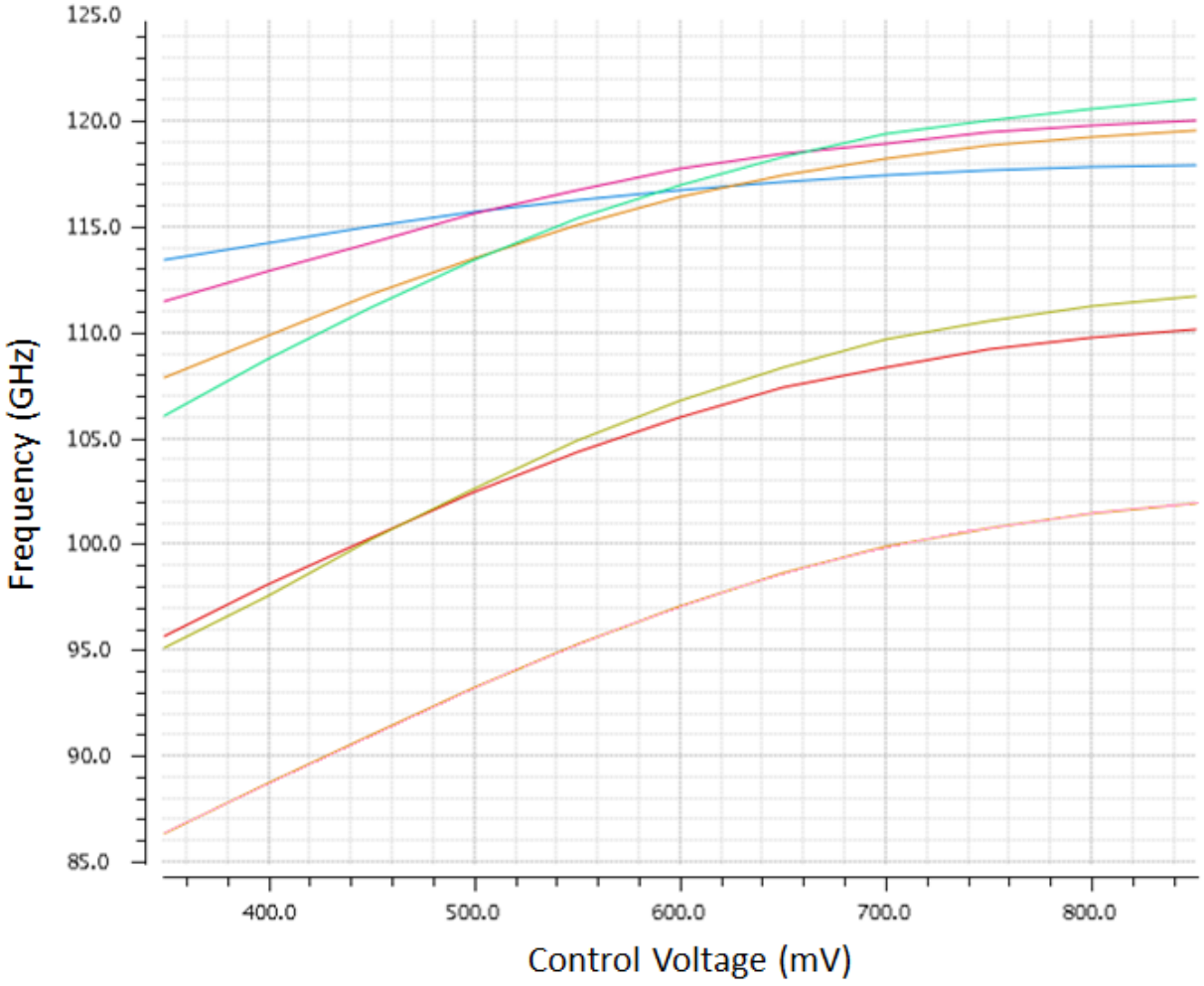
$$\text{Tuning Range} \approx \frac{W'}{L}\mu\frac{C_{ox}}{2C'}\Delta V_{ov} \tag{3.30}$$

On increasing the width of the coupling transistor, the tuning range improves until the capacitance from the coupling transistors dominates the total tank capacitance ($\alpha W'LC_{ox} >> C_{cross\_coupled} + C_{inductor}$) after which the tuning range saturates.

$$\text{Tuning Range} \approx \frac{\mu\Delta V_{ov}}{2\alpha L^2} \tag{3.31}$$

Beyond this point, there are diminishing returns to increasing the widths of the coupling transistors. The increased capacitance would lower the center oscillation frequency. Also, as the coupling transistor is made larger, the tank loss increases due to the gate resistance of the coupling transistor, requiring larger cross-coupled devices for increased compensation. This further increases the tank capacitance and reduces the oscillation frequency.

This design was simulated for different sizes of the coupling transistor (and different corresponding sizes of the cross-coupled transistors) and the results are shown in figure 3-8. The optimal size for the coupling transistors was found to be 4μm and the corresponding minimum size for the cross-coupled transistors was 3μm. For these device sizes, the maximum oscillation frequency was 121GHz with a 16% tuning range. The natural oscillation frequency of the oscillator indicates a tank capacitance of only 13.5fF. The minimum sized varactor in the PDK used for simulation had tuning range from 12.4fF-22.1fF with a capacitance of 18.7fF at a control voltage of 0V. Therefore, adding a varactor would reduce the natural oscillation frequency of the tank by over 50%. Further, the varactor would need a negative control voltage to obtain a respectable tuning range.



Color	Number of Fingers Coupling Transistor	Number of Fingers Cross-coupled Transistor
	1	3
	2	3
	3	3
	4	3
	5	4
	6	4
	7	5

Figure 3-8: Tuning range of quadrature cross-coupled oscillator with synthetic resonance

The tuning range of this synthetic resonance based oscillator is limited by the saturation of g'_m with increase in overdrive voltage (see section 2.3.1) and width(equation 3.31). This is an inherent limitation of transconductance tuning and serves as a motivation to explore alternative tuning mechanisms.

Another limitation is that the increased capacitance from the coupling transistor and the now larger cross-coupled transistors reduces the oscillation frequency. One approach to canceling the effect of the increased tank capacitance is to add some negative capacitance. The constraint here is that the implementation needs to provide broadband negative capacitance at high frequencies without reducing the negative resistance or introducing additional loss elements. The most common way of implementing negative capacitance is to use an active negative impedance converter. However, this approach results in increased loss and the parasitics of the added circuit limit the range of frequencies over which it provides stable negative capacitance. One simple implementation [2] that only involves adding passive components and doesn't contribute additional loss or parasitic capacitance uses capacitive degeneration as shown in figure 3-9.

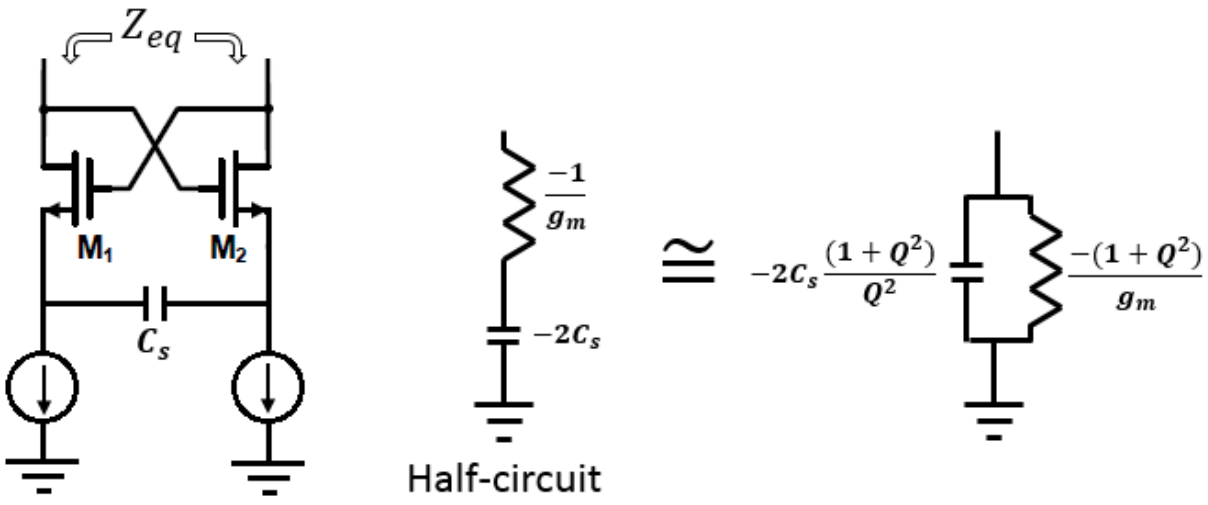


Figure 3-9: Negative capacitance using capacitive degeneration

The equivalent impedance as seen from the drain of the cross-coupled pair is given by

$$Z_{eq} = \frac{-2}{g_m} - \frac{1}{sC_s} \tag{3.32}$$

However, a closer examination shows that this scheme actually degrades the negative resistance. Consider the equivalent circuit shown in figure 3-9. A conversion from the series equivalent to the parallel equivalent results in a modified oscillation frequency and startup condition

$$\omega_0 = \frac{1}{L\left(C - 2C_s\frac{Q^2}{1+Q^2}\right)} \tag{3.33}$$

$$g_m \geq \frac{1+Q^2}{R} \tag{3.34}$$

The natural oscillation frequency of the tank is increased as expected, but the startup condition now requires a significantly larger g_m. For a Q of 3, the circuit needs a transconductance 10 times larger than before. The benefit of the negative capacitance is dwarfed by the increased capacitance from the larger cross-coupled transistors.

While adding negative capacitance to boost the oscillation frequency may not be feasible, some other approaches such as capacitance-splitting [10] could be used to improve the g_m generation efficiency. In addition, this topology offers opportunities for second-harmonic extraction [18].

With a phase noise of -70dBc/Hz at 1MHz offset, the designed oscillator has decent phase noise performance considering the operation frequency. Theoretically, the quadrature cross-coupled oscillator should have nearly 2× better Q because the Q of an $n-$stage LC oscillator scales with n [20]. The shift in oscillation frequency from the resonant frequency of the tank (due to synthetic resonance) diminishes the effect of improved Q. Moreover, the coupling transistors severely degrade the phase noise performance of the quadrature cross-coupled oscillator.

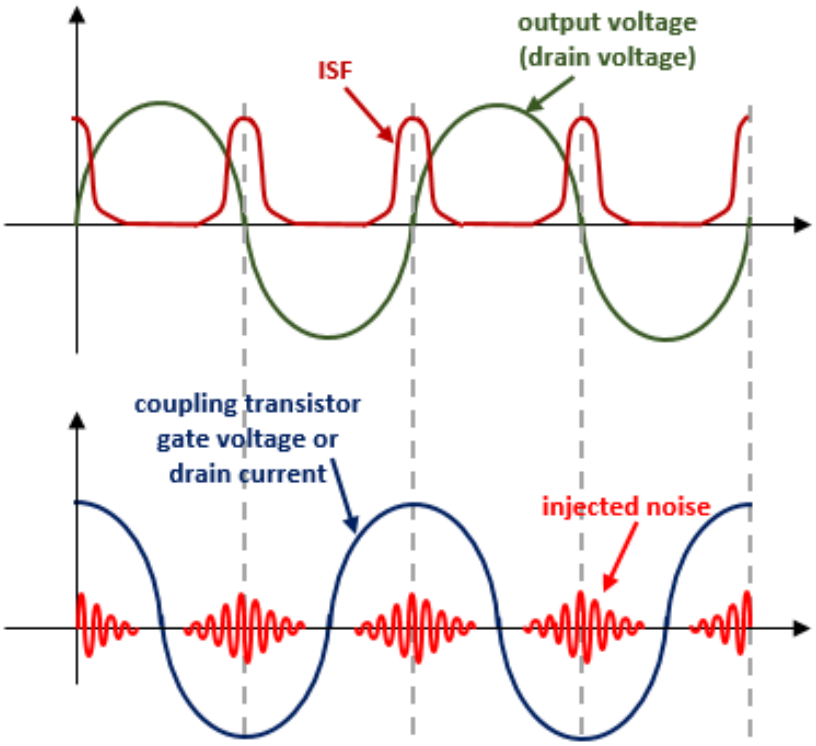


Figure 3-10: ISF of Quadrature cross-coupled oscillator

The main reason for poor phase noise performance is illustrated in figure 3-10 and similar to the reason why a ring oscillator has poor phase noise. This is expected because the quadrature oscillator can also be seen as a 2-stage differential LC ring oscillator. Noise injected when the output is at the maximum might result in a small change in magnitude, but assuming that the output swing is large, it doesn't result in jitter. The output waveform is most vulnerable to noise injection around the zero-crossing because any change in magnitude in this region directly shifts the phase. Therefore, the ISF has peaks corresponding to the zero crossing. Since the current through the coupling transistor is phase shifted by $\frac{\pi}{2}$ from the drain voltage, the peaks in the injected current line up with the zero crossings in the output voltage and the peaks in the ISF. Therefore the coupling transistors significantly degrade the phase noise performance of the oscillator.

The performance of the designed oscillator in comparison with an ordinary LC cross-coupled oscillator and 3-stage ring oscillator is shown in table 3.1.

Topology	Frequency	Phase Noise @1MHz	Power	FOM
Tunable Quadrature Cross-coupled LC	105-121 GHz	-70 dBc/Hz	56 mW	154 dBc/Hz
Differential Cross-coupled LC	148 GHz	-65 dBc/Hz	19 mW	156 dBc/Hz
3-Stage Ring	16 GHz	-69 dBc/Hz	1.5 mW	152 dBc/Hz

Table 3.1: Performance of tunable quadrature cross-coupled oscillator

3.2.5 20GHz-40GHz Small-Footprint Inductorless Quadrature VCO

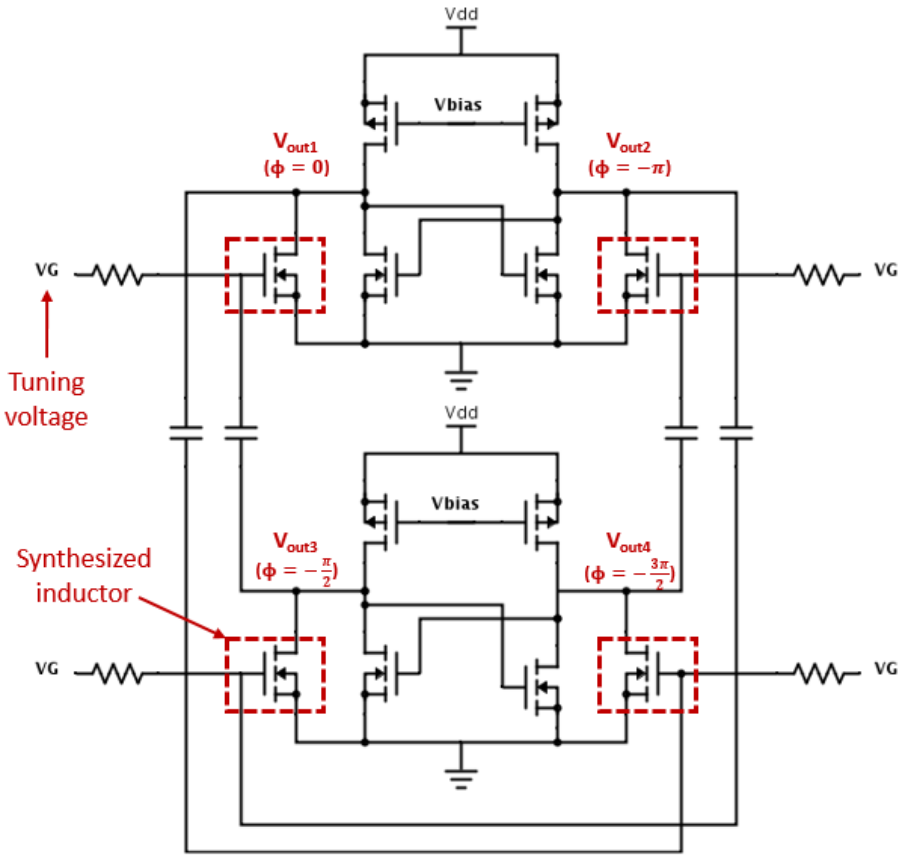


Figure 3-11: Inductorless quadrature cross-coupled oscillator

The design in section 3.2.4 proved that a synthesized inductor could indeed resonate with the tank capacitance and shift the oscillation frequency. Theoretically, the synthetic inductor should be sufficient to achieve resonance. This was demon-

strated by designing the small footprint inductorless quadrature cross-coupled oscillator shown in figure 3-11. The inductors were replaced by PMOS devices for biasing. Since there were two transistors across the rails, the supply voltage was increased to 2V to provide more headroom and allow for wider output swing.

The PMOS bias device can itself be used as a synthesized inductor by connecting its gate to a quadrature output of the oscillator. It was found that this approach didn't work well in practice due to the lower mobility of p-type silicon. In order to obtain the same transconductance as an NMOS synthesized inductor, the PMOS devices had to be made much larger, resulting in a much lower oscillation frequency.

The design methodology used was similar to that used in section 3.2.4. The biasing devices were sized to source sufficient current and properly bias the cross-coupled pair. They also contributed some additional tank capacitance. The cross-coupled devices were now larger to compensate for increased loss.

At 40GHz, the maximum oscillation frequency of the oscillator is three times the maximum oscillation frequency of a 3-stage ring oscillator in the same process. The oscillator demonstrated an octave of tuning range with a fairly linear increase in frequency with the control voltage as shown in figure 3-12. The FOM of the inductorless oscillator was poorer than that of a ring oscillator primarily because of the significantly higher power consumption. This design suffers from the same issues as the quadrature cross-coupled oscillator presented in section 3.2.4. The lack of a high Q LC tank for tuning results in an even poorer phase noise performance.

Despite the poor phase noise performance and large power consumption, the high oscillation frequency and wide tuning range of this inductorless oscillator show that this approach has a lot of potential. This kind of oscillator could be useful in mm-wave applications where a small footprint is essential and a wide tuning range is desired. For example, PLLs require small-footprint oscillators and the locking range of the PLL is a function of the tuning-range of the VCO used. Further, the maximum output oscillation frequency of the PLL is limited by the maximum oscillation frequency of the VCO used. The phase noise of the VCO at small offsets is suppressed by the low-pass nature of the feedback loop. Therefore, this type of oscillator could be a

good candidate for a high-frequency PLL.

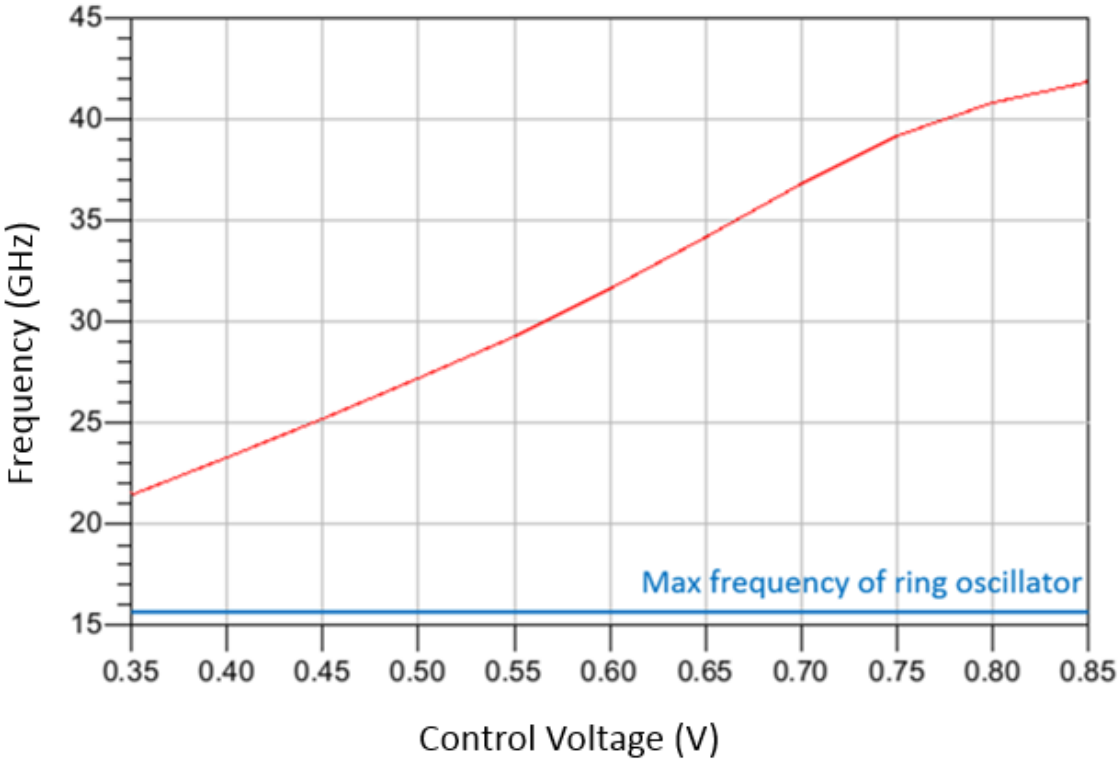


Figure 3-12: Tuning range of the inductorless quadrature cross-coupled oscillator

3.3 Passive Network Based Synthetic Resonance

As discussed in section 2.2.2, another way to establish the desired phase condition is to use a passive phase shifting network. In [7], a 23-29 GHz cross-coupled LC oscillator which operated on a similar concept was developed. This design used a tapped-inductor based RLC network to obtain a $\frac{\pi}{2}$ phase shift between the drain voltage and drain current of a MOS transistor over a certain bandwidth and used the parallel inductance synthesized to tune the oscillator. However, this work purely used transconductance tuning and due to the limitations of transconductance tuning described in section 3.2.4, the tuning range was limited.

One of the advantages of using a passive network to establish the phase condition is that phase tuning can be used. In [7], for different values of of the tank resistance,

the phase response varies resulting in different rates of phasor rotation about the $\Phi = \frac{\pi}{2}$ point. If the tank resistance is implemented as a variable resistor (for example as a MOSFET in triode), then by varying the value of this resistance, the synthesized inductance can be tuned.

The simplest phase shifting network consists of an RC filter placed between the drain and gate of the emulator device. This approach was described in section 2.2.2 and was shown to have several drawbacks, but it suffices for a proof-of-concept. Figures 2-7 and 2-8 illustrated how such a network could be used for phase tuning.

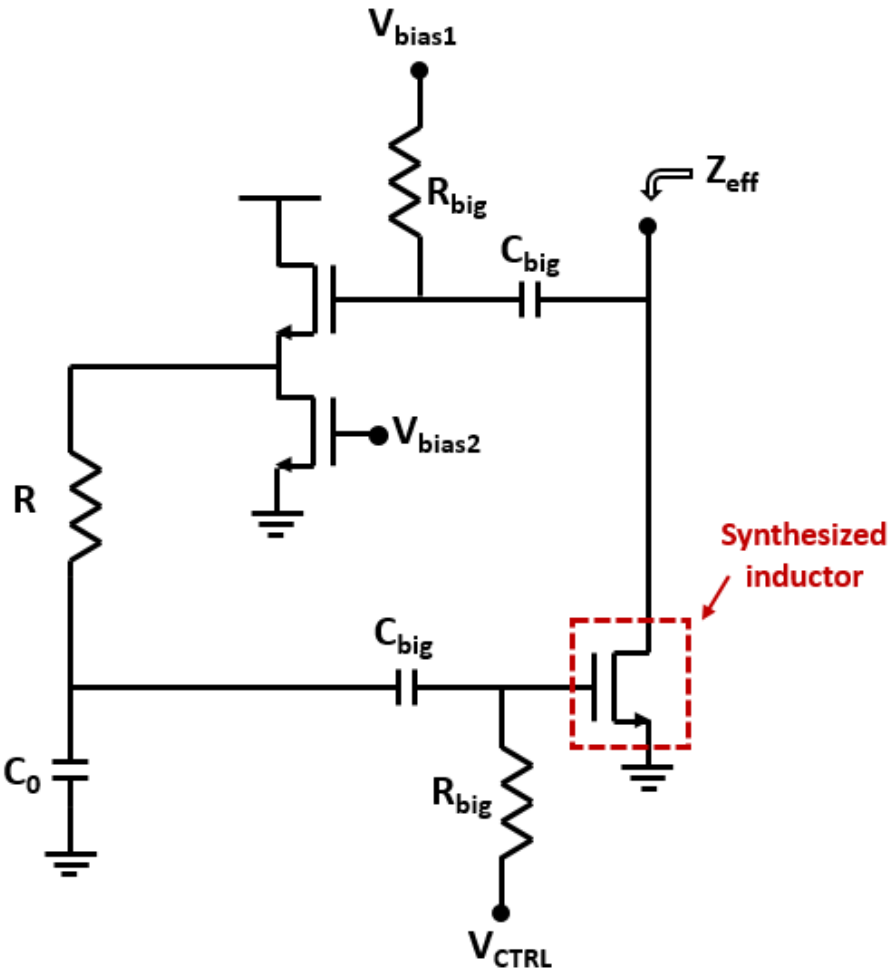


Figure 3-13: RC synthetic impedance generator

The RC synthesized inductor that was implemented is shown in figure 3-13. A source-follower buffer was used between the drain and gate of the emulator device

to isolate the drain from the phase shifting network. The input impedance was simulated for different values of the DC bias of the emulator device to demonstrate transconductance tuning (figure 3-14). As expected, the impedance has a positive imaginary component which increases with frequency; it is a synthetic inductance. Note that unlike a synthetic inductance generated through symmetry, this impedance scales with frequency so the inductance remains constant.

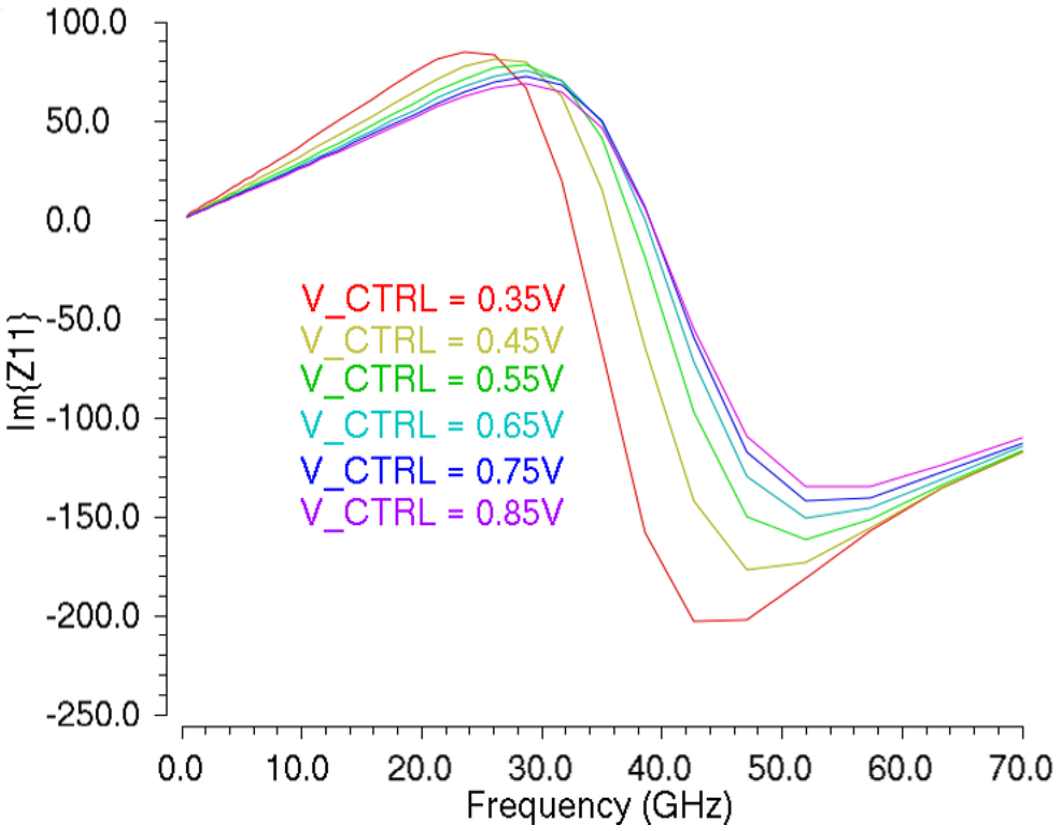


Figure 3-14: Transconductance tuning of RC synthetic impedance generator

The input impedance was also simulated for a fixed value of $C_0 = 200$fF and different values of R to demonstrate phase tuning (figure 3-15).

From figures 3-14 and 3-15, it is evident that phase tuning results in a much wider tuning range than transconductance tuning. It is also evident that beyond a certain frequency, the impedance no longer appears inductive. Depending on the value of R, this frequency could be as low as 20GHz. High frequency poles and zeros change the phase relationship between the drain voltage and drain current. This can partly be

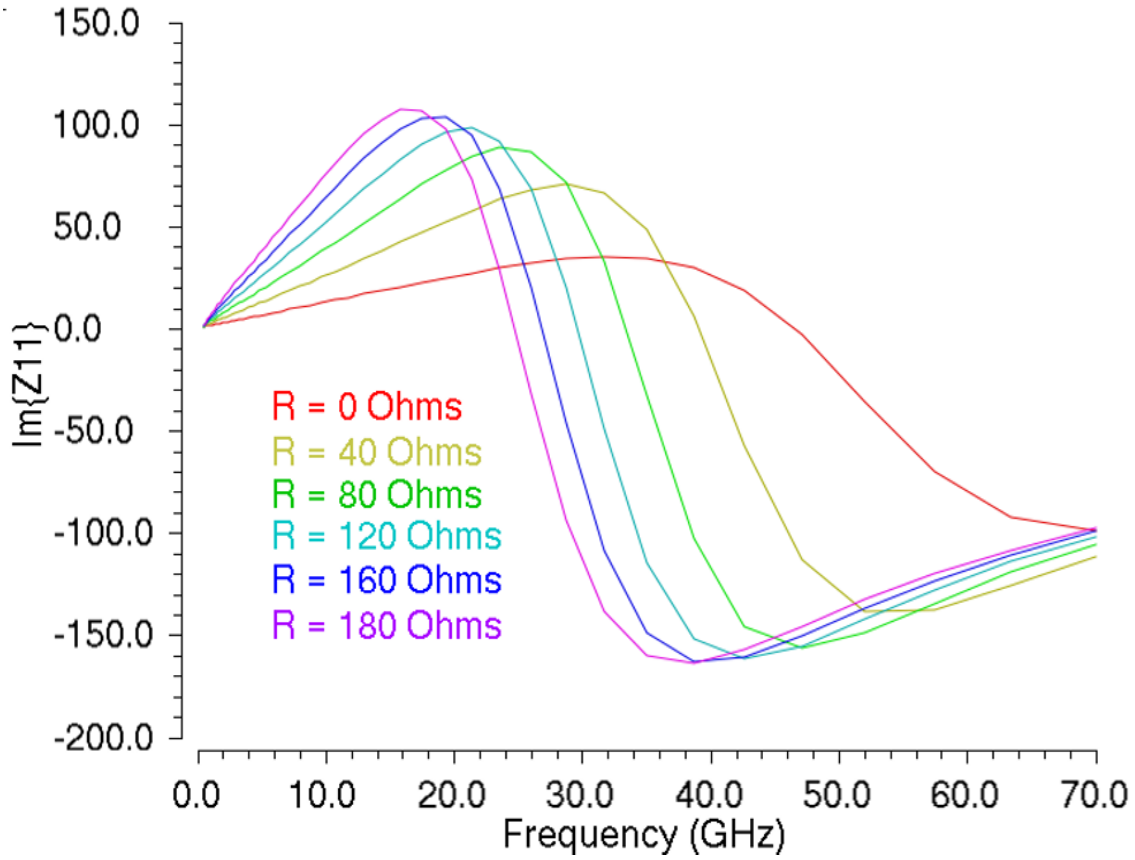


Figure 3-15: Phase tuning of RC synthetic impedance generator

overcome by designing a phase shift network that ensures that the phase difference between the drain voltage and drain current stays relatively constant even though the individual phases are affected by the higher frequency poles and zeros. One example of such a phase shifter is an RC all-pass filter comprised of a low pass filter and high pass filter with the same bandwidth connected in parallel.

Two synthetic inductors designed using the topology in figure 3-13 were attached in parallel with the 0.5nH inductors of a cross-coupled LC oscillator (figure 3-16) and were used to tune the oscillator. The resulting oscillator had a maximum tuning range of 28-32GHz as shown in figure 3-17. Due to the presence of high frequency poles around the operating frequency, phase tuning does not perform better than transconductance tuning in this implementation.

The numerous drawbacks of using passive networks to establish the desired phase relationship were discussed in section 2.2.2. Nevertheless, this design demonstrates

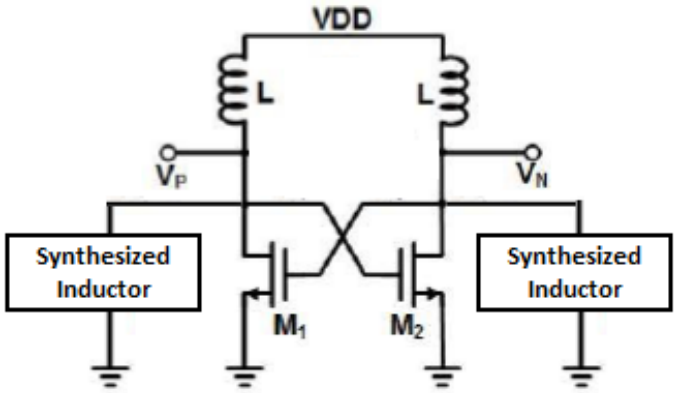


Figure 3-16: Schematic for tuning LC cross-coupled oscillator using the RC synthesized inductor

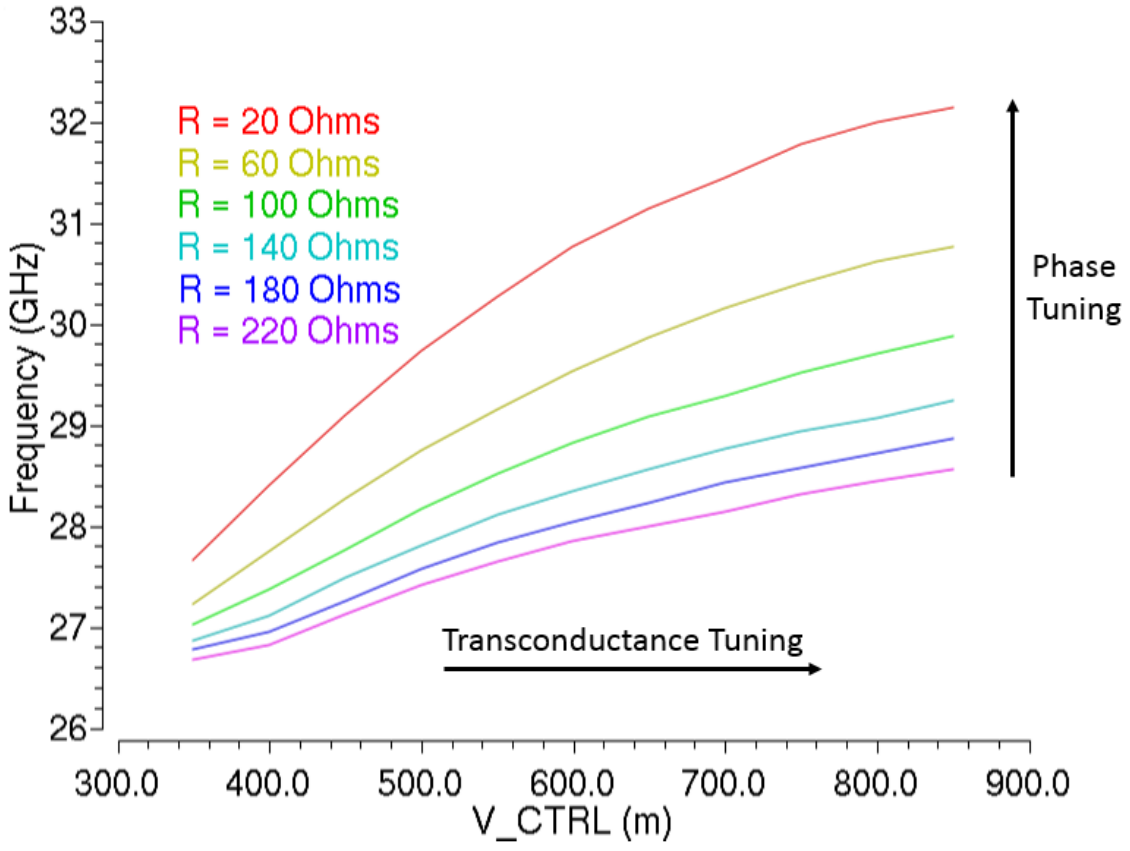


Figure 3-17: Tuning of LC cross-coupled oscillator using the RC synthesized inductor

that even the simplest passive network can work reasonably well.

3.4 Summary

Synthetic inductance was used in this chapter to tune high frequency oscillators and replace inductors to reduce footprint. A 105-121GHz quadrature cross-coupled oscillator was designed without the use of varactors. The figure of merit of the oscillator was competitive against that of a ring oscillator. Further, it was demonstrated that the synthesized inductor was sufficient to resonate with parasitic capacitance independently. This was used to design an inductorless 20-40GHz small-footprint oscillator. While this design consumes a lot of power and has phase noise performance similar to that of a ring oscillator, it serves as a proof-of-concept for synthetic resonance based circuits. Finally, the use of passive networks to establish the desired phase condition was explored. A rudimentary RC low-pass network was used to establish the phase condition. While this simple design has several drawbacks, it was was still able to produce a synthetic inductor which was used to tune a cross-coupled oscillator.

Chapter 4

Loss Compensation in mm-Wave Distributed Amplifiers

Distributed amplifiers are a well known and popular architecture for ultra-broadband applications in instrumentation, military radar and optical communication. The concept of distributed amplification was first proposed by William Percival in 1936 in the context of a broadband vacuum tube amplifier [12]. Despite the large footprint and power consumption of distributed amplifiers, increased demand from high frequency applications over the last few years has led to a renewed interest in distributed amplifier design. This chapter discusses the factors that limit the bandwidth of distributed amplifiers and presents a design that attempts to overcome some of these limitations.

In chapter 2, synthetic impedance generation was used to synthesize inductors and achieve resonance. This chapter shows how the same approach can also be used to synthesize negative resistance to compensate loss. In particular, synthetic impedance generation is used to implement a novel frequency-adaptive loss compensation scheme for distributed amplifiers that is shown to extend the bandwidth.

4.1 Distributed Amplifier Operation

A conventional distributed amplifier (figure 4-1) consists of multiple transconductance cells in parallel, configured such that the output currents from each transconductance

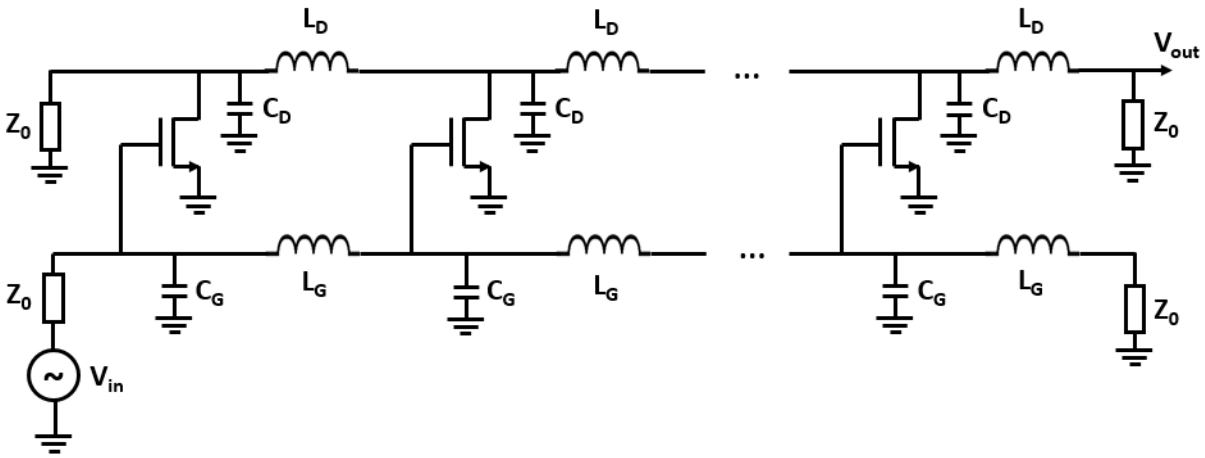


Figure 4-1: Conventional distributed amplifier

cell constructively add up to produce the output voltage. The inputs of the transconductance cells are connected using an artificial transmission line. The gate capacitance of the transistors are absorbed into the transmission line and the transmission line effectively acts as an impedance transformer that makes the input impedance looking into the amplifier real instead of looking capacitive. As a result, the bandwidth is no longer limited by the device itself, but by the frequency response of the artificial transmission line (discussed in section 4.1.1). Artificial transmission lines are usually implemented as LC ladders using transmission line segments or inductors. Assuming the artificial transmission line behaves like an ideal transmission line and the output currents from each stage constructively interfere, the gain of an n-stage distributed amplifier is

$$A_v = -ng_m\frac{Z_0}{2} \tag{4.1}$$

Ignoring the dynamics of the artificial transmission lines, the voltage at the gate of each succesive transistor is equal in magnitude but delayed with respect to that of the previous transistor. Therefore, the output current of each transistor is also equal in magnitude but delayed with respect to that of the previous transistor. Similarly, the voltage at the drain of each succesive transistor is equal in magnitude but delayed

with respect to that of the previous transistor. The forward current in the output transmission line grows towards the output as successive transistors inject current in the forward direction. To obtain maximum output power, the output currents from the transistors need to perfectly constructively interefere in the forward direction. This requires that the phase velocities of the input and output transmission lines are matched

$$\frac{1}{\sqrt{L_G C_G}} = \frac{1}{\sqrt{L_D C_D}} \tag{4.2}$$

One of the drawbacks of this architecture is that some of the power in consumed in the termination resistors. Part of the input power is delivered to the termination resistor on the input transmission line. More importantly, some of the ouput current from each transistors travels in the reverse direction along the output transmisison line and delivers power to the termination resistor. This can be mitigated by making sure that the delay between each segment is sufficient for the reverse currents to destructively interfere to a large extent. Nevertheless, most of the output power from the earlier stages is usually dissipated in the termination resistor and the later stages contribute most of the output power. Several studies have looked into ways of reclaiming this lost power [3] and tapering the transmission lines to improve efficiency [16].

4.1.1 Artificial Transmission Line

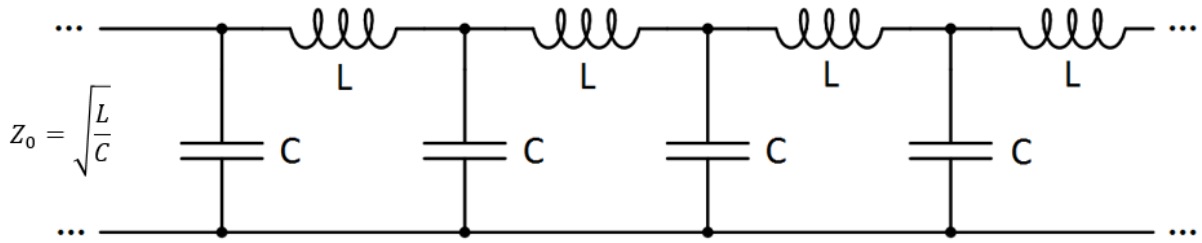


Figure 4-2: Artificial transmission line

As discussed above, the input and output lines of a distributed amplifier behave as artificial transmission lines. The key distinction between artificial and real trans-

mission lines is that an artificial transmission line is composed of a finite number of discrete L-C segments whereas a real transmission line is composed of an infinite number of such segments. As a result, unlike a real transmission line that appears as a fixed real impedance at all frequencies, the impedance of an artificial transmission line is frequency dependent. The impedance of an artificial line can be calculated by assuming that the line is terminated in its image impedance so that the line behaves as if it were infinitely long.

$$Z_{in} = sL + \left[\left(\frac{1}{sC}\right) \parallel Z_{in}\right] \tag{4.3}$$

On simplifying the expression and solving for Z_{in},

$$Z_{in} = \frac{j\omega L}{2} + \sqrt{\frac{L}{C}}\sqrt{1 - \frac{\omega^2 LC}{4}} \tag{4.4}$$

As expected, in the limit $L \to 0$, $C \to 0$, the impedance of the transmission line simplifies to $Z_0 = \sqrt{\frac{L}{C}}$ which is the characteristic impedance of a real transmission line. An important observation is that beyond a certain frequency, the impedance of the line no longer has a real component. This means that beyond this frequency, the transmission line cannot transfer energy. This frequency beyond which a signal cannot propagate beyond the line is called the cutoff frequency of the transmission line.

$$\sqrt{1 - \frac{\omega_c^2 LC}{4}} = 0 \implies \omega_c = \frac{2}{\sqrt{LC}} \tag{4.5}$$

The derivation above assumed that the line was terminated with impedance Z_{in}. In the case of a real transmission line, $Z_{in} = Z_0$ at all frequencies and there is no cutoff frequency. Therefore it is possible to terminate a real transmission line such that there is no signal reflection due to impedance mismatch at the terminations. In the case

of an artificial transmission line, the input impedance is frequency dependent. This leads to a discrepancy between the Z_{in} predicted by equation 4.4 and the actual input impedance of a 5-stage artificial transmission line terminated with a fixed resistor Z_0. Figure 4-3 shows the discrepancy between these two quantities for the artificial transmission line used in this design.

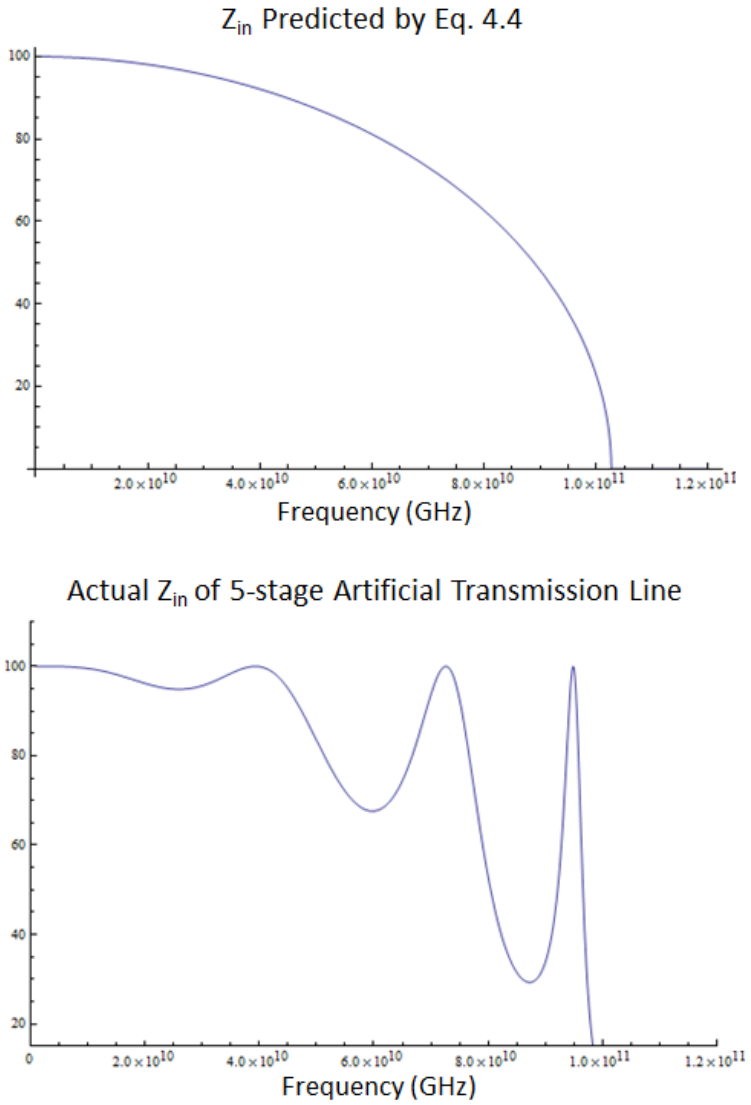


Figure 4-3: Predicted Z_{in} versus actual Z_{in} for the artificial transmission line used

The two key observations here are that there is a finite cutoff frequency and that the input and output matching degrades significantly below the cutoff frequency. In the next section, a matching network is added to the terminations of the artificial transmission to provide a good impedance match in the pass band.

4.1.2 Matching Network

An artificial transmission line is actually a constant-k low pass filter. In order to achieve broadband amplification, the input and output transmission lines need to be terminated on either end by the image impedance of the constant-k network. Therefore, the lines require matching networks on the terminations to transform the a fixed resistor of value Z_0 to the image impedance of a constant-k network.

In this design, an m-derived π half section was used as a matching network as shown in figure 4-4.

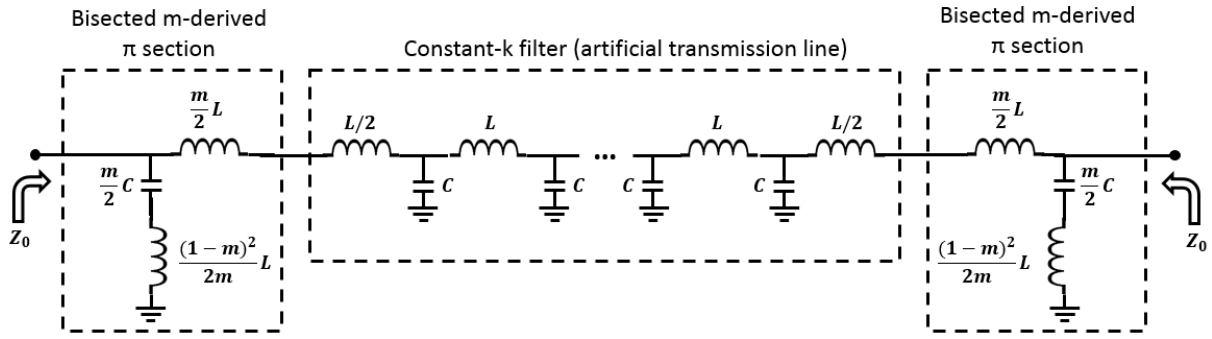


Figure 4-4: Matching network used to match transmission lines to termination resistors

There are two implementations of an m-derived section - a T configuration and a π configuration [13]. Note that a constant-k filter is composed of m-derived sections in a T configuration with $m = 1$. The image impedances of a bisected m-derived π section can be shown to be [13]

$$Z_{i1} = Z_0\sqrt{1 - \frac{\omega^2 LC}{4}} \tag{4.6}$$

$$Z_{i2} = Z_0\frac{1 - (1 - m^2)\left(\frac{\omega^2 LC}{4}\right)}{\sqrt{1 - \frac{\omega^2 LC}{4}}} \tag{4.7}$$

$$\text{where } 0 < m < 1 \tag{4.8}$$

From equation 4.4, Z_{i1} is equal to the image impedance of the constant-k filter.

In order to match Z_{i2} to the termination resistor Z_0, the value of m was chosen to minimize the variation of Z_{i2} over the passband of the matching network ($\omega < \omega_c$). According to [13], $m = 0.6$ usually results in the best match. The calculated improvement in matching for the 5-stage artificial transmission line used in this design is shown in 4-5. The matching was significantly improved across the bandwidth of operation by using this matching network.

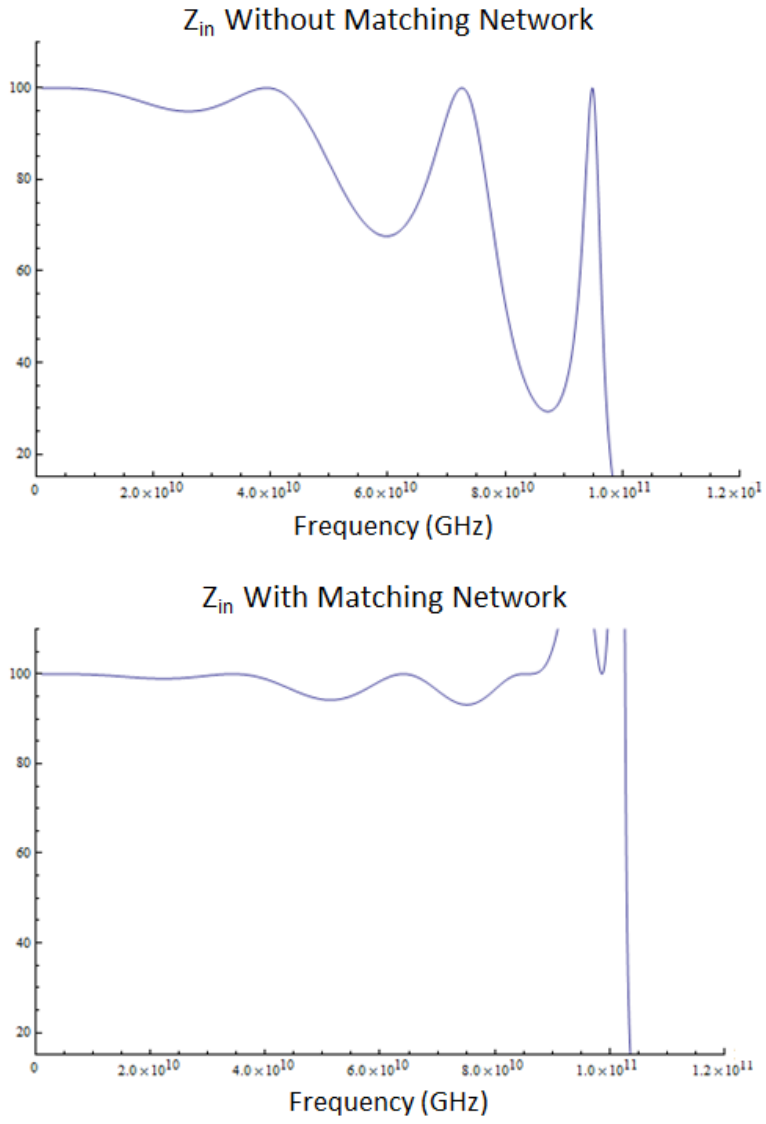


Figure 4-5: Predicted improvement in matching

4.1.3 Bandwidth-limiting Factors

There are three main factors that limit the bandwidth of distributed amplifiers.

1. **Cutoff Frequency and Impedance Mismatch:** From the discussion above, it is clear that the cutoff frequency of the input and output transmission lines imposes a strict limit on the maximum frequency that can be amplified by a given distrbuted amplifier. While $Re(Z_{in}) = 0$ at the cutoff frequency, the matching degrades at significantly lower frequencies especially if a matching network is not used to achieve broadband matching. Signal reflections along the transmission line due to these impedance mismatches result in attenuation of the signal as it travels down the transmission line. The extent of impedance mismatch increases as the cutoff frequency is approached.

   The cutoff frequency can be increased by reducing the capacitance, but usually this involves reducing the size of the transconductors resulting in an unchanged gain-bandwidth product. In [5], negative capacitance generated using a negative impedance converter was used to cancel some of the gate capacitance and increase the bandwidth without hurting the gain. However, this doesn't address the issue of attenuation due to signal reflections below the cutoff frequency.

2. **Transmission Line Loss:**

   The input and output signals are also attenuated as they propagate along their respective transmission lines due to various loss mechanisms. The primary sources of loss are the on-chip inductors (or transmission line segments) and the gate resistance of the transistors. Two major sources of inductor loss are skin effect and substrate loss. As shown below, all of these loss mechanisms result increased loss at higher frequencies.

   - *Skin Effect:*

     Skin effect is a phenomenon by which the magnetic field produced by a conductor carrying current cause the carriers to flow near the surface of the conductor. As a result, the effective resistance of the conductor is

increased. Consider a cross section of a conductor in which current is flowing in the z direction and the current density and magnetic field vary only in the y direction.

From Maxwell's Equations,

$$\nabla \times E = -\frac{\partial B}{\partial t} = -j\omega B \tag{4.9}$$

$$\nabla \times H = J \tag{4.10}$$

where the displacement current was neglected in the second equation.

$$E = \frac{J}{\sigma} \implies \nabla \times J = -j\omega B\sigma \tag{4.11}$$

$$H = \frac{B}{\mu} \implies \nabla \times B = \mu J \tag{4.12}$$

Since the current density and magnetic field only vary along the y direction,

$$\frac{dJ_z}{dy} = -j\omega\sigma B_x \tag{4.13}$$

$$\frac{dB_x}{dy} = \mu J_z \tag{4.14}$$

which results in the second order linear ODE

$$\frac{d^2 J_z}{dy^2} = j\omega\mu\sigma J_z \tag{4.15}$$

$$\text{which has solution } J_z(y) = J_{z1}e^{Ay} + J_{z2}e^{-Ay} \tag{4.16}$$

$$\text{where } A = \sqrt{j\omega\mu\sigma} = (1+j)\sqrt{\frac{\omega\mu\sigma}{2}} \tag{4.17}$$

$$\tag{4.18}$$

J_{z1} must be 0 to prevent exponential increase of the current density with y. Therefore the final solution can be written as

$$J_z(y) = J_z(0)e^{-\sqrt{\frac{\omega\mu\sigma}{2}}}e^{-j\sqrt{\frac{\omega\mu\sigma}{2}}} \tag{4.19}$$

The depth at which the current density drops to $\frac{1}{e}$ of the current density at the surface is defined as the skin depth δ

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{4.20}$$

The skin depth depends on the material and geometry of the conductor. For example, for copper at 1GHz, the skin depth is approximately $2\mu m$ [8]. Assuming that current primarily flows in the region between the surface and the skin depth and the radius of the conductor $r >> \delta$, an effective resistance can be approximated as

$$R = \frac{\rho l}{A} \approx \frac{\rho l}{2\pi r\delta} = \frac{\rho l}{2\pi r}\sqrt{\frac{\omega\mu\sigma}{2}} \tag{4.21}$$

Therefore the effective series resistance is approximately proportional to the square root of frequency.

- *Substrate Loss:*

  Due to the finite resistivity of silicon substrate, signals on the metal layer couple to the substrate and dissipate power. Substrate loss can be mitigated by using techniques like adding a patterned ground shield, but it is still a major source of loss. As frequency increases, substrate coupling increases and substrate resistivity decreases, leading to increased substrate loss.

- *Gate Resistance:*

  At high frequencies, there are two components to the gate resistance. One component is the resistance of the metal that makes up the gate. The second component is an effective resistance that originates from a finite gate to drain delay. This component increases with frequency.

4.2 Loss Compensation

From the discussion above, it is clear that there are many factors that result in the attenuation of signals as they travel down the input and output transmission lines. The stages of the amplifier closer to the output provide most of the output power (see section 4.1), but the voltage at the input of these stages is the most attenuated. This reduces the maximum gain-bandwidth product that can be achieved by a given distributed amplifier. On the output transmission line, the signal from the earlier stages get more attenuated than the signal from later stages. However, the later stages contribute most of the output power so output transmission line loss is a smaller issue. Therefore this work targeted compensating loss on the input transmission line.

It is also clear that any viable loss compensation scheme needs to scale with frequency because the major loss mechanisms at high frequencies increase with frequency. Overcompensation at low frequencies can cause instability which is highly undesirable. Further, introducing negative resistance at lower frequencies also changes

the characteristic impedance of the transmission line, degrading the terminal matching. If the series resistance is R and the shunt negative conductance is $-G$, the characteristic impedance is given by

$$Z_0 = \sqrt{\frac{R + j\omega L}{-G + j\omega C}} \tag{4.22}$$

which at high frequencies reduces to $\sqrt{\frac{L}{C}}$. However at low frequencies, a large value of negative conductance changes the characteristic impedance.

There are several ways to generate the negative resistance to compensate loss. Perhaps the most common way to generate negative resistance is to use a pair of cross-coupled transistors. This doesn't meet the basic criteria that the negative resistance needs to scale with frequency. It also requires a differential implementation of the distributed amplifier, which results in a large area and power overhead. In [4], a loss compensation scheme that showed significant bandwidth improvement was presented. While the authors used techniques to improve the flatness of the gain, the loss compensation itself was not frequency-adaptive. More recently, the authors in [11] demonstrated a bandwidth improvement using capacitively degenerated common-source compensation cells. This loss compensation scheme is frequency adaptive. The scheme presented in this thesis is likely to add a smaller capacitive load on the input and output transmission lines as discussed in the following sections.

4.2.1 Synthetic Impedance Generation

In section 2.2, it was shown that if passive components and delay lines are used to establish the phase condition, then it is possible to synthesize impedances that vary with frequency. For loss compensation, a desirable admittance would consist of a negative conductance that was 0 at DC and increased in magnitude with increase in frequency. Since the magnitude of the admittance is fixed by the transconductance of the compensating device, this would basically involve a rotation of the current

phasor on the admittance plane from the imaginary axis towards the real axis. Since the magnitude of the conductance increases with frequency, the magnitude of susceptance needs to decrease to keep the admittance magnitude constant. Therefore, the susceptance will be a positive or negative inductance. The admittance plane phasors are illustrated for the positive inductance case in figure 4-6.

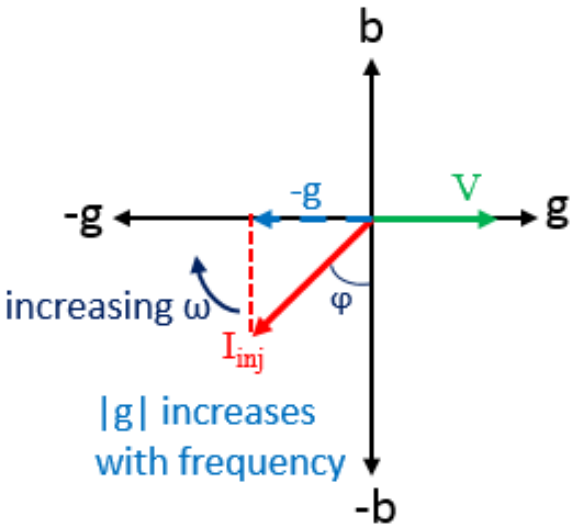


Figure 4-6: Desired admittance plane phasors for loss compensation

The proposed compensation scheme involves placing negative resistance cells between each stage of the distributed amplifier to locally compensate loss. The negative resistance cell works by feeding a small part of the output power back into the input to compensate loss. The gate of the compensating transconductor samples the voltage from the output transmission line and injects the resulting current into the input transmission line. The synthesized impedance depends on the phase difference between the voltage of the input transmission line and the injected current. For a given stage of the distributed amplifier, the amplification device produces a phase shift of π between the input and output voltage. Consider the low frequency operation of the distributed amplifier. At low frequencies, the ouput voltages of all stages and input voltages of all stages are equal. Since the gate of the compensating transistor samples the voltage of the output line and the drain of the compensating transistor is connected to the input line, there is a π phase difference between the gate and

drain voltages of the compensating transistor. Since the drain current is in phase with the gate voltage, the drain current and drain voltage of the transistor have a phase difference of π. This results in a fixed negative conductance

$$G = A_v g'_m = -n g_m g'_m \frac{Z_0}{2} \tag{4.23}$$

where g_m is the transconductance of the amplification transistors and g'_m is the transconductance of the compensation transistors. In order to have 0 conductance at DC, it is necessary to introduce a pole or zero at DC that can rotate the current phasor by $\frac{\pi}{2}$. In this design, a zero was introduced into the transfer function by adding a source degenerating capacitor and providing a separate path for DC current as shown in figure 4-7.

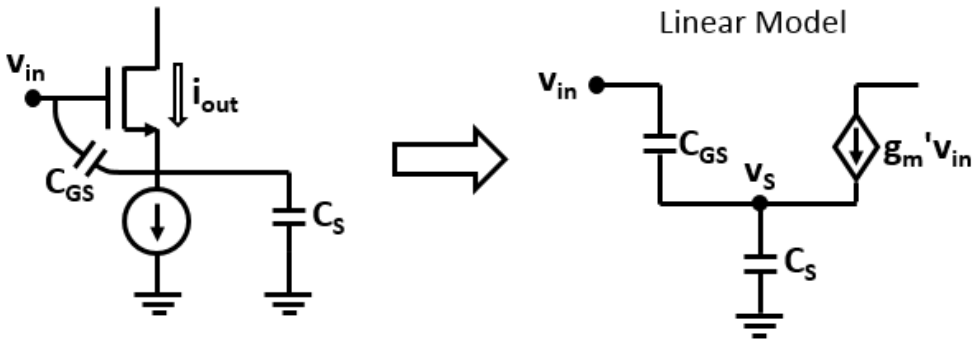


Figure 4-7: Capacitively degenerated configuration to obtain desired phase relationship

Consider the linear model shown in figure 4-7.

$$v_S = \frac{sC_{GS}(v_{in} - v_S) + g'_m(v_{in} - v_S)}{sC_S} \tag{4.24}$$

$$i_{out} = g'_m(v_{in} - V_S) = g'_m v_{in} \frac{sC_S}{g'_m + s(C_S + C_{GS})} \tag{4.25}$$

$$g'_{m,eq} = \frac{i_{out}}{v_{in}} = g'_m \frac{sC_S}{g'_m + s(C_S + C_{GS})} \tag{4.26}$$

Therefore the transfer function of the modified transconductance cell has a zero at the origin and a pole at $\frac{g_m}{C_S+C_{GS}}$. As the frequency increases and the pole is approached, the phase of the transfer function decreases from $\frac{\pi}{2}$ to π and the phasor rotates towards the real axis. The modified transconductance cell results in the admittance plane phasor shown in figure 4-6. By varying the value of the source degenerating capacitor, the frequency at which the compensation becomes significant can be changed. This is an example of using passive components (in this case a capacitor) to establish the desired phase condition.

The delay lines can also be used to control the change in negative conductance with frequency. The phase delay across each inductor increases with frequency as shown in figure 4-8. Since the voltage amplitude doesn't vary much between adjacent stages along the input and output transmission lines, the loss compensation cell can be connected across different stages of the amplifier. By sampling the output voltage of one stage of the amplifier and injecting current into input of the succeeding stage, the phasor can be made to rotate towards the real axis at a faster rate. Similarly, by injecting current into the input of the preceding stage, the phasor can be made to rotate at a slower rate. The rate variation can be modified by changing the value of the inductance. At a given frequency, a larger inductor in the transmission line results in a greater phase shift. This is an example of how delay lines can be used to establish the desired phase condition for impedance generation.

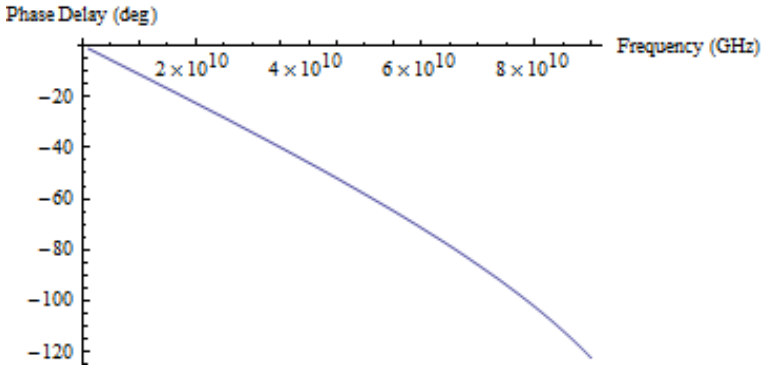


Figure 4-8: Phase delay between the input of each stage for the inductance value used in the design

4.2.2 Implementation

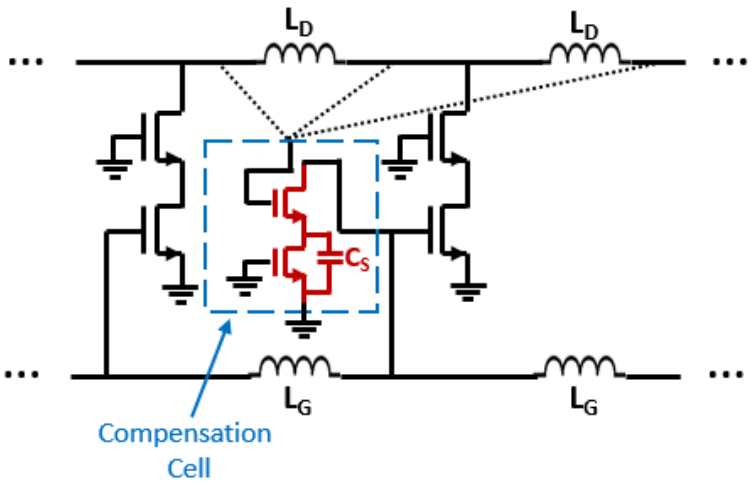


Figure 4-9: Implementation of the loss compensation scheme (AC model)

A distributed amplifier was implemented in order to evaluate the proposed loss compensation scheme. Most distributed amplifiers have between 4-8 stages and the optimal number of stages for a conventional distributed amplifier can be calculated as shown in [13]. One of the drawbacks of having larger number of stages in the traditional architecture is that the input voltage gets attenuated by the time it reaches the later stages of the amplifier. This would be remedied by a loss compensation scheme so a distributed amplifier with larger number of stages might be more optimal when loss compensation has been implemented. In this design, 5-stages were used.

The transconductance cell was implemented in a cascode configuration to obtain good reverse isolation. This also allowed the output capacitance to be controlled to match the phase velocities by appropriately sizing the cascode device instead of adding a separate capacitor at the output of each stage. The delay lines were implemented using inductors. The inductors were sized so that they are large enough to result in significant cancellation of the reverse travelling wave on the output line (see section4.1). The characteristic impedance of the input and output transmission lines is 100Ω. The same inductance values (310pH) were used on the input and output transmission lines so the capacitances of the two lines (32fF) were made the same. In order to model frequency dependent loss, inductors of quality factor 15 were used in

simulation. The gate capacitance of the amplification transistors was the capacitance limiting factor since C_{GS} is typically larger than C_{GD} and the size of the amplification device is closely tied to the gain (unlike the size of the cascode device). As a result, the cascode devices had to be made significantly larger than the amplification devices. The cutoff frequency of the resulting transmission lines was about 105GHz (figure 4-5). The appropriate values for a bisected m-derived π section with $m = 0.6$ were calculated and the resulting matching network was added at the terminations.

The loss compensation cell shown in figure 4-7 was implemented. Using the delay lines to control the rate of rotation of the phasor was explored, but it was found that connecting the cell across a single stage yielded the best results. The current source was implemented as an NMOS transistor sized so that the compensating transistor had maximum transconductance for a given size. Due to velocity saturation, increasing the current through the transistor beyond a certain point doesn't result in higher transconductance. The parasitic capacitance of this transistor (C_{GD}) is absorbed into the degeneration capacitor.

The sizing of the compensation transistor (W/L = 2μm/100nm) results in a tradeoff with the cutoff frequency. If the additional capacitance introduced by the loss compensation is too large, it can significantly reduce the cutoff frequency and degrade the bandwidth. However, it turns out it is not very useful to make the compensating transistor large anyway. Increasing the size of the compensating transistor increases its transconductance, which changes the magnitude of the phasor and the pole location. This is not very useful because the pole location can easily be changed by changing the degenerating capacitance. The other reason to increase the transconductance would be to increase the gain, but the voltage swing of the gate is quite large because the gate is sampling the amplifier output so there isn't need for much gain from the compensating transistor. By leveraging the gain of the amplifier, this scheme is able to compensate the amplifier without significantly loading the input and output transmission lines.

Another advantage of this scheme is that the loss compensation cell adds more capacitance to the output line than the input line since the output line is connected to

the gate of the compensating transistor and C_{GS} is typically larger than C_{GD}. Since the capacitance of the output line had to anyway be artificially boosted to match that of the input line, the effect of the added capacitance is less significant than in a scheme where the input line is connected to the gate of a transistor in the compensation cell as in [11].

4.2.3 Simulation Results

The proposed compensation scheme resulted in a 30% bandwidth improvement over the uncompensated amplifier. The gain plots of the compensated and uncompensated amplifier are shown in figure 4-10.

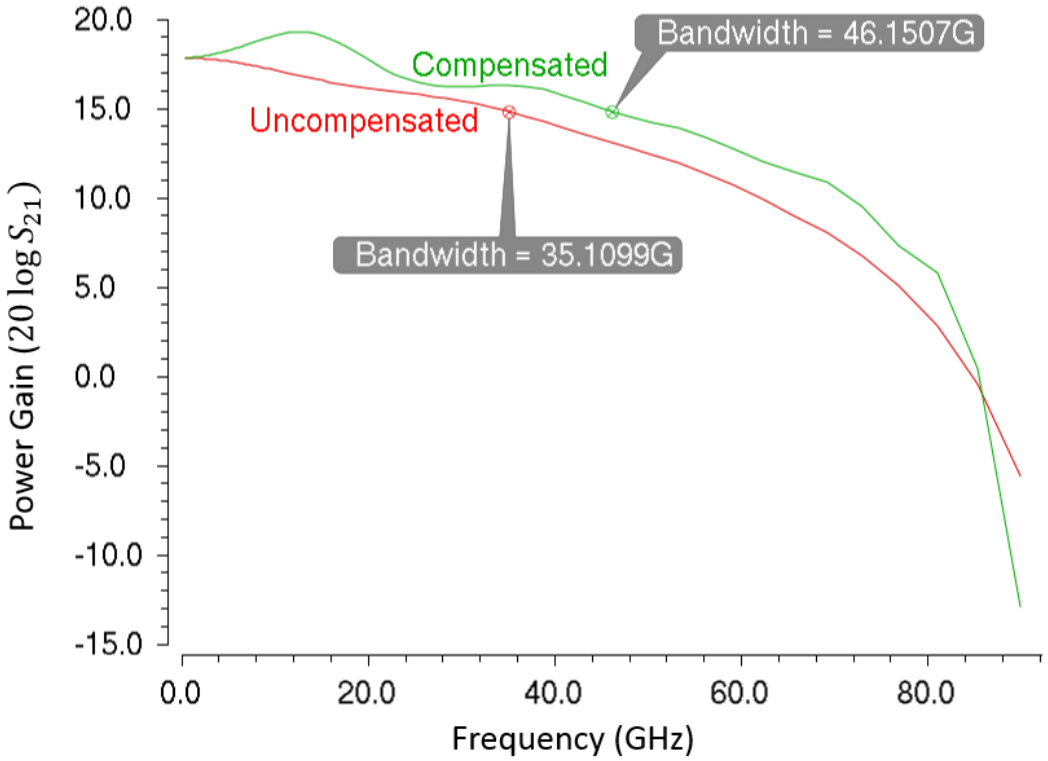


Figure 4-10: Gain of compensated and uncompensated distributed amplifiers

The gain plot of the compensated amplifier shows some peaking at low frequencies, but the stability factor is greater than 1 at all frequencies as shown in figure 4-11.

The input match, output match and reverse isolation of the compensated amplifier are shown in figure 4-12. Note that S_{11}, S_{12} and S_{22} are below -10dB for all frequencies

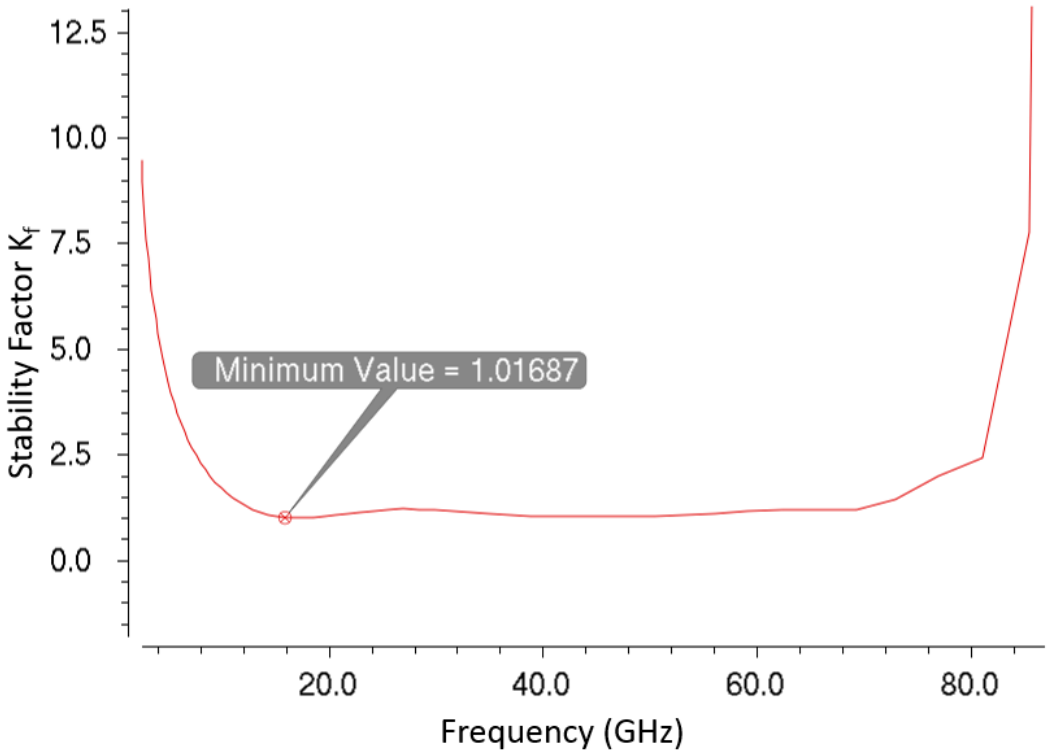


Figure 4-11: Stability factor of compensated distributed amplifier

below the cutoff frequency indicating good matching and reverse isolation.

The amplifier consumed 120mW of power and each compensation cell consumed an additional 5.1mW. The performance is summarized in table 4.1.

	Uncompensated DA	**Compensated DA**	**[11] (ISSCC 2007)**
Stages	5	5	8
Process	65nm CMOS	65nm CMOS	130nm CMOS
DC Gain	17.8 dB	17.8 dB	9.8 dB
Bandwidth	35GHz	46GHz	44GHz
Power	120mW	145mW	103mW

Table 4.1: Performance of the loss compensated distributed amplifier

4.3 Summary

A novel frequency-adaptive loss compensation scheme was demonstrated to improve the bandwidth of a distributed amplifier by 30%. The compensation scheme has the

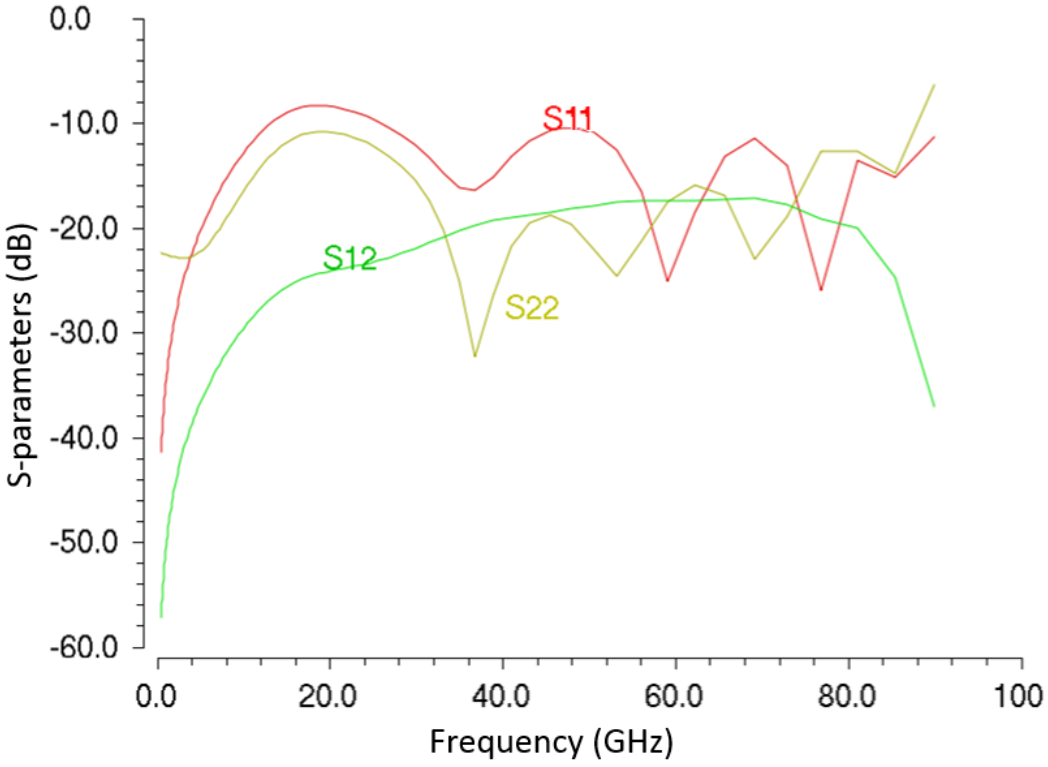


Figure 4-12: S-Parameters of compensated distributed amplifier

following salient features:

- The compensation scales with frequency, preventing overcompensation and instability at low frequencies. It also prevents the characteristic impedance from being affected at low frequencies.

- The compensation network adds minimal additional capacitance to the input and output lines by leveraging the gain of the amplifier. In addition, while the capacitance on the gate line is the bottleneck with respect to the cutoff frequency, most of the added capacitance is on the drain line.

- The resulting amplifier has good input matching, ouput matching and reverse isolation. The additional power consumed by the compensation network is minimal.

Chapter 5

Conclusion

A new framework for designing impedances in which a tunable impedance is obtained by establishing the appropriate phase relationship between the drain voltage and drain current of a MOS transistor was presented. Different methods of establishing the desired phase condition were explored.

This concept was used to synthesize inductors for broadband high frequency oscillators. The concept of synthetic resonance was explored and a high frequency, wide tuning range (105-123GHz) quadrature oscillator was presented. It was demonstrated that the synthesized inductors themselves are in fact sufficient to produce resonance by designing a wide tuning range (20-40GHz) inductorless oscillator. By eliminting the need for inductors, this design drastically reduced the footprint of the oscillator.

The concept of impedance synthesis was also used to synthesize negative resistance for a novel frequency adaptive loss compensation scheme for distributed amplifiers. The compensation scheme was demonstrated to improve the bandwidth of a distributed amplifier by 30%. The resulting distributed amplifier had a gain of 17.8dB, bandwidth of 46GHz and good input and output matching.

While the loss compensation scheme was demonstrated to improve the bandwidth significantly, there are several parameters (such as the number of stages) that could potentially be optimized to obtain better performance. This technique could also be combined with other techniques such as using negative capacitance to further extend the bandwidth. More accurate modeling of the inductors and measurement results

are required to fully validate the performance of the proposed scheme.

Bibliography

[1] I. Chant. Samsung Demos Multi-Gbps Speeds Using 60 GHz Wi-Fi. *IEEE Spectrum*, 2014.

[2] J. Covington et al. A cross-coupled CMOS negative capacitor for wideband metamaterial applications. In *IEEE SOUTHEASTCON*, March 2014.

[3] K. Eccleston et al. Analysis of the dual-fed distributed power amplifier. In *Asia Pacific Microwave Conference*, December 1999.

[4] S. Kimura et al. Loss-compensated distributed baseband amplifier IC's for optical transmission systems. *IEEE Transactions on Microwave Theory and Techniques*, 44(10), October 1996.

[5] A. Ghadiri and K. Moez. Gain-Enhanced Distributed Amplifier Using Negative Capacitance. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(11), August 2010.

[6] A. Hajimiri, S. Limotyrakis, and T. Lee. Phase noise in multi-gigahertz CMOS ring oscillators. In *Proceedings of the IEEE Custom Integrated Circuits Conference*, May 1998.

[7] K. Kwok and J. Long. A 23-to-29 GHz Transconductor-Tuned VCO MMIC in 0.13um CMOS. *IEEE Journal of Solid State Circuits*, 42(12), December 2007.

[8] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*, chapter 4.2. Cambridge University Press, second edition, 2004.

[9] G. Li, Y. Tang, and E. Afshari. A Low-Phase-Noise Wide-Tuning-Range Oscillator Based on Resonant Mode Switching. *IEEE Journal of Solid State Circuits*, 47(6), June 2012.

[10] L. Li, P. Reynaert, and M. Steyaert. A 60-GHz CMOS VCO Using Capacitance-Splitting and Gate Drain Impedance Balancing Techniques. *IEEE Transactions on Microwave Theory and Techniques*, 59(2), February 2011.

[11] K. Moez and M. Elmasry. A 10dB 44GHz Loss-Compensated CMOS Distributed Amplifier. In *IEEE International Solid-State Circuits Conference*, February 2007.

[12] W. Percival. Thermionic Valve Circuits. British Patent Specification no. 460562, filed July 1936, granted January 1937.

[13] David M. Pozar. *Microwave Engineering*. John Wiley & Sons, Inc., fourth edition, 2012.

[14] B. Razavi. A Study of Phase Noise in CMOS Oscillators. *IEEE Journal of Solid State Circuits*, 31(3), March 1996.

[15] R. Sharman, Abu Khari A'ain, M. Azmi, and Huang Min Zhe. Design approach for tunable CMOS active inductor". In *IEEE International Conference on Semiconductor Electronics*, December 2004.

[16] P.N. Shastry and A.S. Ibrahim. Design Guidelines for a Novel Tapered Drain Line Distributed Power Amplifier. In *European Microwave Conference, 2006*, September 2006.

[17] D. Sheen, D. McMakin, and T. Hall. Three-dimensional millimeter-wave imaging for concealed weapon detection. *IEEE Transactions on Microwave Theory and Techniques*, 49(9), September 2001.

[18] H. Shin and H. Kim. Extraction Technique of Differential Second Harmonic Output in CMOS LC VCO. *IEEE Microwave and Wireless Components Letters*, 17(5), May 2007.

[19] A.G. Stove. Linear FMCW Radar Techniques. *IEE Processing-F Radar and Signal Processing*, 139(5), October 1992.

[20] J. Tang, P. Ven, D. Kasperkovitz, and A. Roermund. Analysis and Design of an Optimally Coupled 5-GHz Quadrature LC Oscillator. *IEEE Journal of Solid State Circuits*, 37(5), May 2002.

[21] Y. Wue, X. Ding, M. Ismail, and H. Olsson. CMOS Active Inductor and its Application in RF Bandpass filter. In *Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2004.