Monolithic silicon photonics in a sub-100nm SOI CMOS microprocessor foundry: progress from devices to systems

Monolithic Silicon Photonics in a Sub-100nm SOI CMOS Microprocessor Foundry: Progress from Devices to Systems

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ABSTRACT

We review recent progress of an effort led by the Stojanović (UC Berkeley), Ram (MIT) and Popović (CU Boulder) research groups to enable the design of photonic devices, and complete on-chip electro-optic systems and interfaces, directly in standard microelectronics CMOS processes in a microprocessor foundry, with no in-foundry process modifications. This approach allows tight and large-scale monolithic integration of silicon photonics with state-of-the-art (sub-100nm-node) microelectronics, here a 45nm SOI CMOS process. It enables natural scale-up to manufacturing, and rapid advances in device design due to process repeatability. The initial driver application was addressing the processor-to-memory communication energy bottleneck. Device results include 5Gbps modulators based on an interleaved junction that take advantage of the high resolution of the sub-100nm CMOS process. We demonstrate operation at 5fJ/bit with 1.5dB insertion loss and 8dB extinction ratio. We also demonstrate the first infrared detectors in a zero-change CMOS process, using absorption in transistor source/drain SiGe stressors. Subsystems described include the first monolithically integrated electronic-photonic transmitter on chip (modulator+driver) with 20-70fJ/bit wall plug energy/bit (2-3.5Gbps), to our knowledge the lowest transmitter energy demonstrated to date. We also demonstrate native-process infrared receivers at 220fJ/bit (5Gbps). These are encouraging signs for the prospects of monolithic electronics-photonics integration. Beyond processor-to-memory interconnects, our approach to photonics as a "More-than-Moore" technology inside advanced CMOS promises to enable VLSI electronic-photonic chip platforms tailored to a vast array of emerging applications, from optical and acoustic sensing, high-speed signal processing, RF and optical metrology and clocks, through to analog computation and quantum technology.

Keywords: Electronic-photonic integrated circuits, monolithic integration, zero-change CMOS photonics, 45nm SOI CMOS, on-chip interconnects, on-chip photonic links, modulators, detectors.

1. INTRODUCTION

Integrated photonics is at a transition point from individual devices [1-4] to densely integrated electronic-photonic systems on chip [5]. Driver applications such as processor to memory interconnects [5], ultrahigh bandwidth RF signal processing, photonic A/D conversion [6], and others demand very large scale (VLSI) integration of electronics and photonics. To scale electronic-photonic systems requires a design paradigm shift toward manufacturability and achieving high yield of a complete system-on-chip. For photonics to become a viable technology, it must also scale to complex systems on chip at low cost. Since 2006, we have invested a major effort into exploring the viability of realizing photonics monolithically integrated with electronics in commercial, microelectronics CMOS foundries, which meets both of these objectives, and allows photonics to tightly integrate with advanced microelectronics, something that is not possible in custom photonics fabrication due to the large costs of realizing state of the art transistors. By

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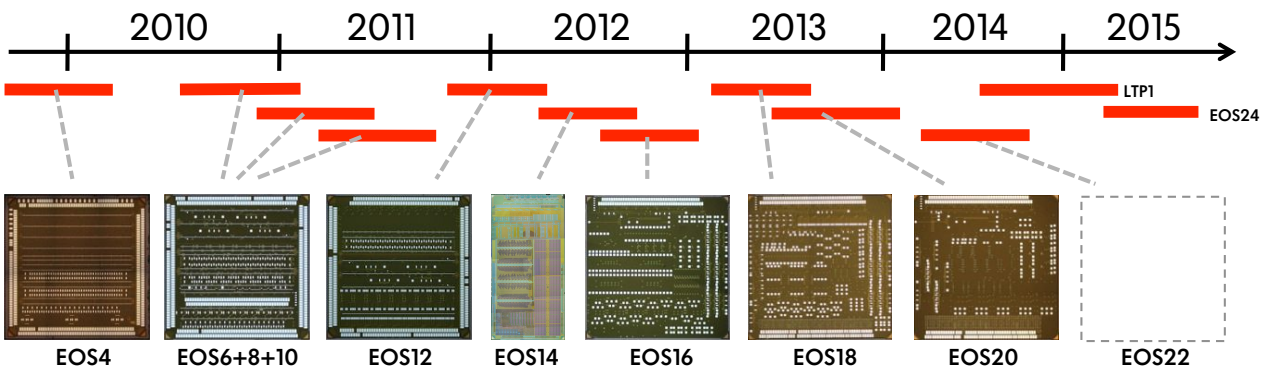

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Fig. 1. Zero-change CMOS monolithic electronics-photonics integration paradigm. Electronic-photonic chips in a commercial, microelectronics 45nm SOI CMOS technology: over ten chip designs have been designed by our university team, within a microelectronics design flow and environment, and taped out via the Trusted Foundry program [24] to a commercial IBM foundry running the 45nm SOI CMOS (12S) process [13], yielding chips with thousands of photonic devices integrated alongside circuits comprising tens of millions of transistors.

introducing a photonics design capability directly into standard microelectronics design flows and infrastructure (in our case within the Cadence Virtuoso design environment), we have enabled large-scale system-on-chip design, including layout of photonic components, full chip design rule checking (DRC) including electronics and photonics, as well as some functional verification, i.e. layer-vs-schematic (LVS), etc. The challenges have been manifold, but they include the need to design working photonic devices within the fixed material layer stackup of a CMOS process, and subject to design rules that are written to ensure manufacturability and yield of transistors in a CMOS process, efficient layout of photonics jointly with electronics, and circuit design for efficient drive and control of photonics.

Using this approach, we have demonstrated photonic platforms in both bulk and silicon-on-insulator microelectronics CMOS technology. In bulk CMOS platforms, we demonstrated photonics in unmodified 65nm [7] and 28nm [8] bulk CMOS processes, and a customized memory process in collaboration with Micron Technology [9] for the purposes of enabling photonically interfaced dynamic random access memory (DRAM). These efforts led to the first demonstration of an optical link between two bulk CMOS chips [10]. In silicon-on-insulator (SOI) technology, we have demonstrated photonic devices and systems in the 45nm and 32nm nodes [11-12]. SOI CMOS allows lower loss optical waveguides due to presence of a crystalline silicon device layer, but is a higher cost technology than bulk CMOS.

In this paper, we review our progress over the past several years on integration of electronics and photonics in unmodified (so-called "zero-change") 45nm SOI CMOS, using the commercial 12SOI process run by IBM [13], and provide references herein that can help the reader track down greater detail on each result. The summary provided here covers the basic idea of zero-change integration of photonics in CMOS, device technology demonstrations, and some of the first subsystem demonstrations.

2. ZERO-CHANGE CMOS MONOLITHIC INTEGRATION OF ELECTRONICS & PHOTONICS

The challenges in enabling photonics in an unmodified advanced CMOS process included design of photonics within the electronics design environment, to enable co-design of electronics and photonics, design of low loss waveguides and fiber-to-chip coupling interfaces, passive devices, and actives including modulators and detectors. In some cases, tight integration allows limited performance devices to enable efficient systems. Our team of students and postdocs has to date designed over 10 chips in the 45nm SOI CMOS platform, as illustrated in Fig. 1.

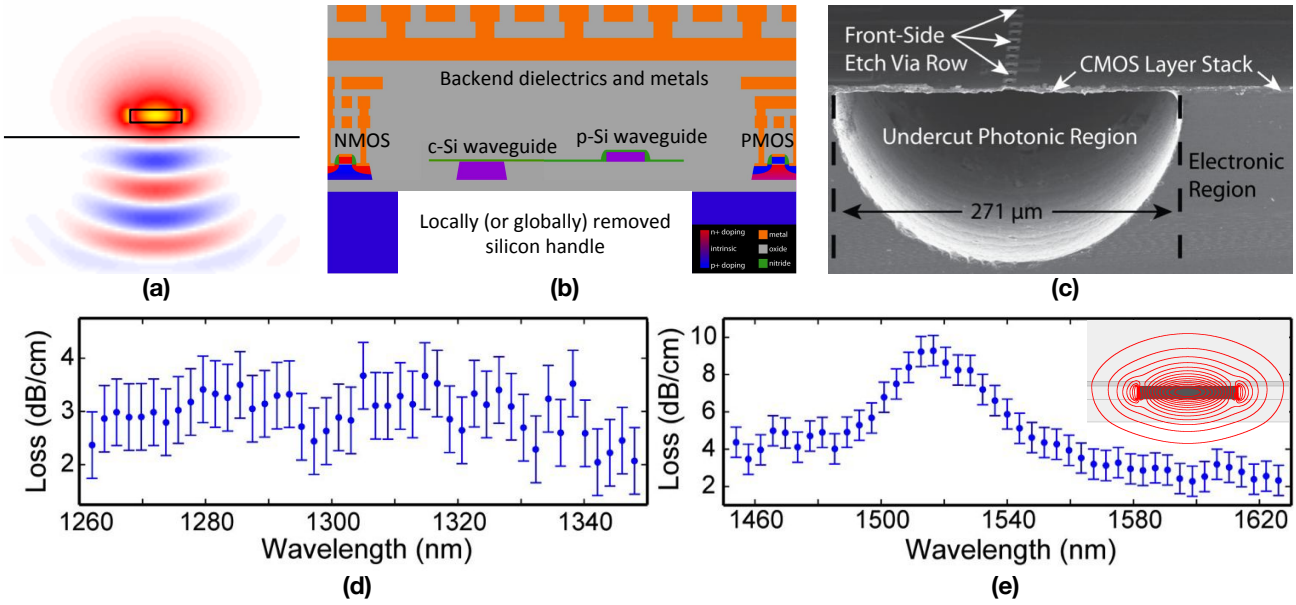

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Fig. 2. Enabling low-loss waveguides in microelectronics SOI CMOS [11]: (a) microelectronics SOI processes use thin SOI wafers (less than 200nm thick oxide), leading to substrate leakage radiation loss in waveguides; (b) we globally or locally remove the substrate wafer in a post-processing step to enable photonics; low doping and clearing out of the first few backend metal levels is compatible in design with electronics design rules; (c) example of localized substrate removal from the front side [14]; (d-e) we have demonstrated waveguide loss on the order of 2-3 dB/cm in both the O and C-L bands [inset: waveguide mode], competitive with the best custom photonics results.

The first challenges in integrating waveguides in CMOS were enabling low-loss guiding in the device layers of the process. The crystalline silicon transistor body device layer can be obtained undoped in the process, to allow low-loss waveguide propagation (Fig. 2). However, the buried oxide (BOX) in a SOI wafer used in advanced CMOS microelectronics processes is less than 200nm thick, to provide electrical isolation but good thermal contact for heat sinking, to ensure proper transistor performance across the wafer, unlike custom photonics SOI wafers that have a 2 to 3 micron thick BOX. The thin BOX is insufficient to confine light and would lead to large substrate radiation leakage loss [Fig. 2(a)]. Therefore, we have developed both partial (Fig. 2(c), Ref. [14]) and full [11] substrate removal processes that are carried out post-foundry, and enable low loss waveguiding. Metal levels near the waveguide can be cleared in the region of the optical mode without breaking density design rules [Fig. 2(b)], allowing low loss optical guiding. The waveguide is then formed in the same device layer as the transistors [Fig. 2(b)], and waveguide losses have been measured at the 2-3 dB/cm level in both the O band and the C-L band wavelength ranges [Fig. 2(d-e)] (the C-L band shows a N-H bond overtone absorption peak typical of silicon nitride, at 1515nm, due to the nitride stressor films that are part of the sub-100nm transistor process, and are part of the waveguide cross-section). Microring cavity unloaded Q factors in the 100,000 to 250,000 have been demonstrated [11].

3. PHOTONIC DEVICE TECHNOLOGY

Efficient fiber-to-chip coupling has been demonstrated using grating couplers. Basic designs provide about 3dB coupling loss [11]. Advanced designs that employ two independently patternable silicon layers that are available in SOI CMOS provide 1dB demonstrated coupling loss with record bandwidth [15-16]. They are based on an array nanoantenna design that employs both the polysilicon gate and the crystalline silicon transistor body layers. The devices are uniform, and simulations of new apodized designs not yet experimentally measured show 0.2dB coupling loss is achievable in an unmodified platform [17]. This device is one example where the very high resolution, process repeatability, and unique properties (two independently patternable silicon layers) provide an advantage in photonic device design in comparison to custom platforms – at no increase in cost, since we are reusing transistor masks.

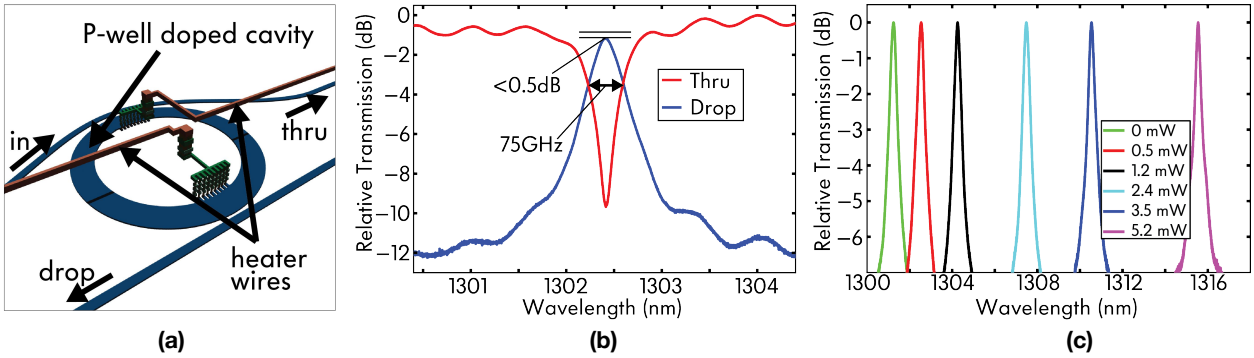

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Fig. 3. Efficient thermal tuning: (a) by light doping of a spoked-ring microcavity and direct heating of the dual "resistor-optical resonator", (b) we demonstrate efficient add-drop filters (less than 0.5dB drop loss), with (c) record thermal tuning efficiency of 2 uW/GHz [21].

Efficient active devices including tunable filters and modulators required a way to provide strong optical confinement as well as electrical contact to the structure without incurring large optical losses. The classic approach employs a partially etched, rib waveguide [1], where the rib provides lateral optical confinement but still enables electrical contact to a p-n junction formed in the waveguide to enable depletion region modulation. The contacts can be far from the waveguide and minimally impact Q. In CMOS processes, including the IBM 12SOI 45nm process, no partial etch step is available. Watts *et al.* have demonstrated use of vertical junctions in modulators, which permit fully etched through microdisks, and contact is made in the middle of the disk cavity for both terminals [18]. However, sub-65nm (transistor gate length) SOI CMOS node platforms employ a thin, sub-100nm crystalline silicon layer, making vertical junctions difficult to realize efficiently.

Our best solution to date is the "spoked-ring" microcavity design, where we employ a wide microring cavity with radially extending lateral junctions [19-21]. The cavity has contacts along the inner radius wall to both the p and n regioins. It supports a disk-like fundamental mode that does not have substantial optical field intensity at the inner sidewall and hence the contact have no impact on cavity Q. Unloaded Q's, including mid-level dopings, above 30,000 were demonstrated. A uniformly lightly doped cavity (Fig. 3) was used as both an optical filter and a resistor, allowing efficient thermal tuning by directly heating the mode. The device demonstrated 2 uW/GHz thermal tuning efficiency [21] (record efficiency at the time of publication). A tunable filter with 75GHz bandwidth and under 0.5dB insertion loss was demonstrated, tuning across 16nm (in the O band) with 5 mW of electrical power [21].

The spoked-ring cavity as a modulator is shown in Fig. 4. Fig. 4(a) shows a schematic of the concept, with p and n mid-level doped regions. The p and n doped regions could be made as narrow as on the order of 200nm wide [15], owing to the high resolution and mask alignment precision of the 45nm process. The layout of the actual device is shown in Fig. 4(b) as a 3D rendering of the mask level patterns in the layout data file. The curved bus waveguide enables phase matched coupling to the fundamental resonance of the spoked ring cavity, and rejects higher order modes of the cavity. Hence, despite the fact that the cavity supports multiple transverse spatial modes, it shows a clean, single-mode transmission spectrum [Fig. 4(c)], enabling cascading to construct a WDM transmitter. In reverse bias, each of the 84 junctions around the spoked ring structure increase the depletion width, the carrier density is reduced, the index increases, and the resonant wavelength red shifts enabling modulation. Fig. 4(d) shows that the cavity can be sufficiently shifted by less than a volt of drive, enabling a simple inverter to drive the modulator. The device level testing (GSG probes) demonstrated 5 Gbps modulator operation with an estimated 5 fJ/bit energy efficiency. A tradeoff of speed and energy can be made through control of the geometry (density) of the p-n junctions and their contacts, but processor-to-memory interconnects optimally call for around 8 Gbps data rate [22] and minimizing energy at that point.

Infrared detectors were also realized in this unmodified CMOS platform, by making use of the silicon germanium implants in the source and drain regions, whose primary use in CMOS is as a stressor to the transistor channel, to increase carrier mobility. The low mole-fraction SiGe (around 20% Ge) does not absorb at 1550nm, but does at 1200nm wavelength, suitable to our processor-to-memory application. Working SiGe detectors were demonstrated, though with

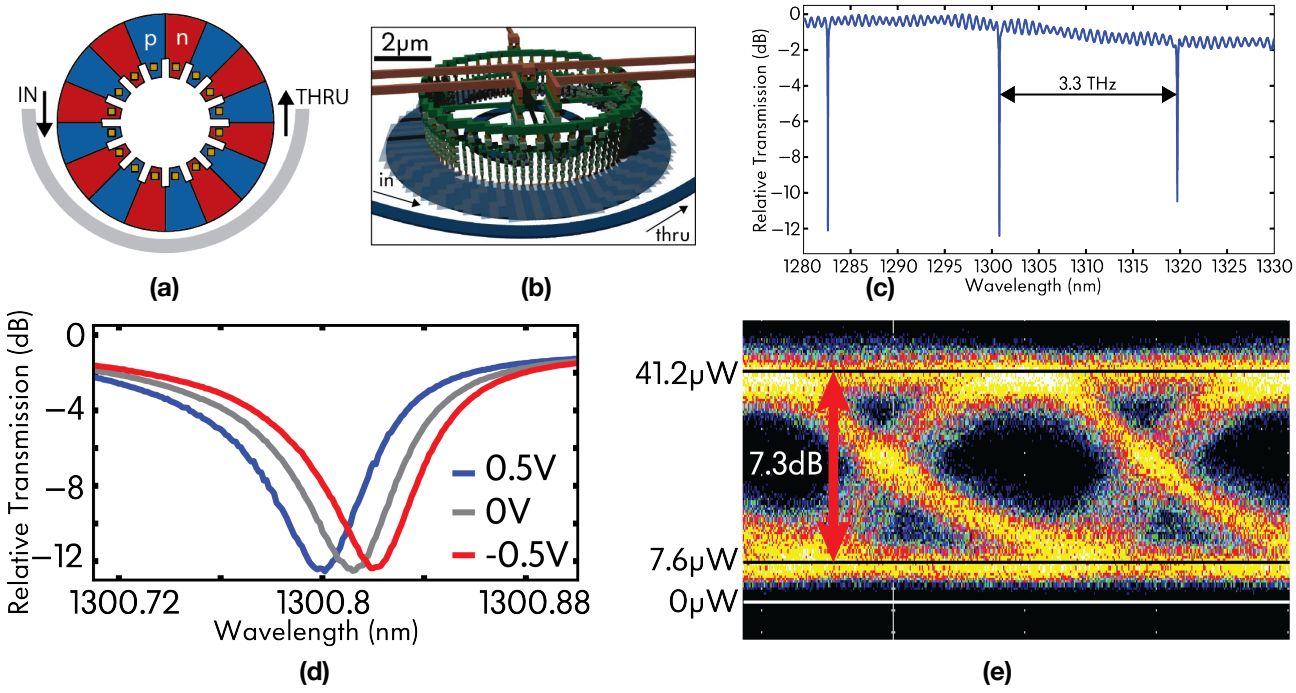

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Fig. 4. Energy efficient modulators [19-21]: (a) the spoked-ring microcavity design permits the implementation of a high-Q optical cavity in the (transistor) device body layer of the SOI CMOS platform, which admits only full etch-through of the silicon, while allowing efficient electrical contact at the inner radius by leveraging an array of radially oriented p-n junctions; (b) 3D visualization of the actual device layout (GDS file comprising many mask levels) showing coarse-grid implant masks required by the process design rules, and the back-end metal connections to the device; (c) a curved, phase-matching coupler excites only the fundamental resonance of the disk-like, multimode cavity, thereby allowing a clean, single-mode-like spectral response [20]; (d) DC shift vs. bias voltage showing that the device can in principle be driven by a logic transistor; (e) 5Gbps eye diagram of the device (driven by GSG probes), estimated efficiency: 5fJ/bit [21].

low quantum efficiencies of around 2% [23]. Nevertheless, tight integration with receiver circuits has enabled sensitive receivers, as described in the next section.

4. INTEGRATED ELECTRONIC-PHOTONIC SUBSYSTEMS ON CHIP

With a full suite of photonic devices enabled, a number of electronic-photonic integrated subsystem on chip demonstrations were pursued, to demonstrate the potential of this platform. The specific goal of the research program is to demonstrate a complete microprocessor-to-memory interface, including an optically enabled modern microprocessor, but the technology and approach are broadly applicable.

Fig. 5(a) shows a snapshot from the Cadence Virtuoso design environment where complete electronic-photonic systems are designed in an integrated environment. The example shown in the figure is an 11-wavelength monolithic optical transmitter, comprising an array of spoked-ring optical modulators, analog drive electronics, and a digital logic backend. Two transmitters are shown. Fig. 5(b) shows a close-up of the layout of the modulator with an integrated heater, including a tap photodiode for thermal tracking and locking, and a grating coupler for direct optical access for debugging purposes. All of the photonic components are represented as parametrized cells (p-cells), coded within the SKILL scripting language, and added to a photonic component library within Cadence. Design rule check (DRC) files have been designed to automate design rule checking of complex photonic components, as well as layer-vs-schematic (LVS) checking of circuit connections, including between electronics and photonics.

Fig. 6(a) shows an integrated 8-channel filter bank based on microring resonators with integrated heaters, and an integrated digital thermal tuning circuit [Fig. 6(b)] [11]. Fig. 6(c) shows the filter bank through and drop port responses

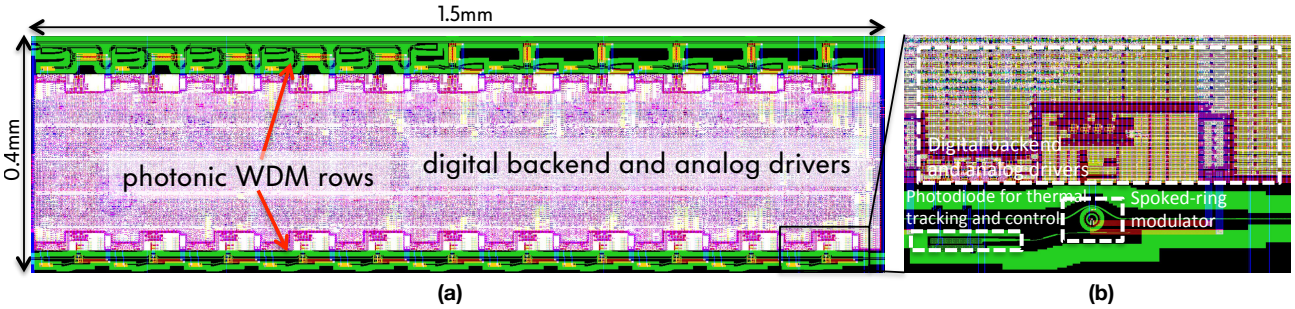

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Fig. 5. Integrated electronics-photonics design in standard microelectronics design flow: (a) snapshots from Cadence Virtuoso layout environment showing wavelength-division multiplexed (WDM) transmitter rows comprising 11 cascaded optical transmitters based on the spoked-ring modulator, alongside analog circuit drivers and a complete digital backend; (b) zoom-in view showing the modulator, a tap-port photodiode for thermal tracking and control, and an auxiliary grating coupler for debugging, alongside part of the digital backend and analog driver for the device.

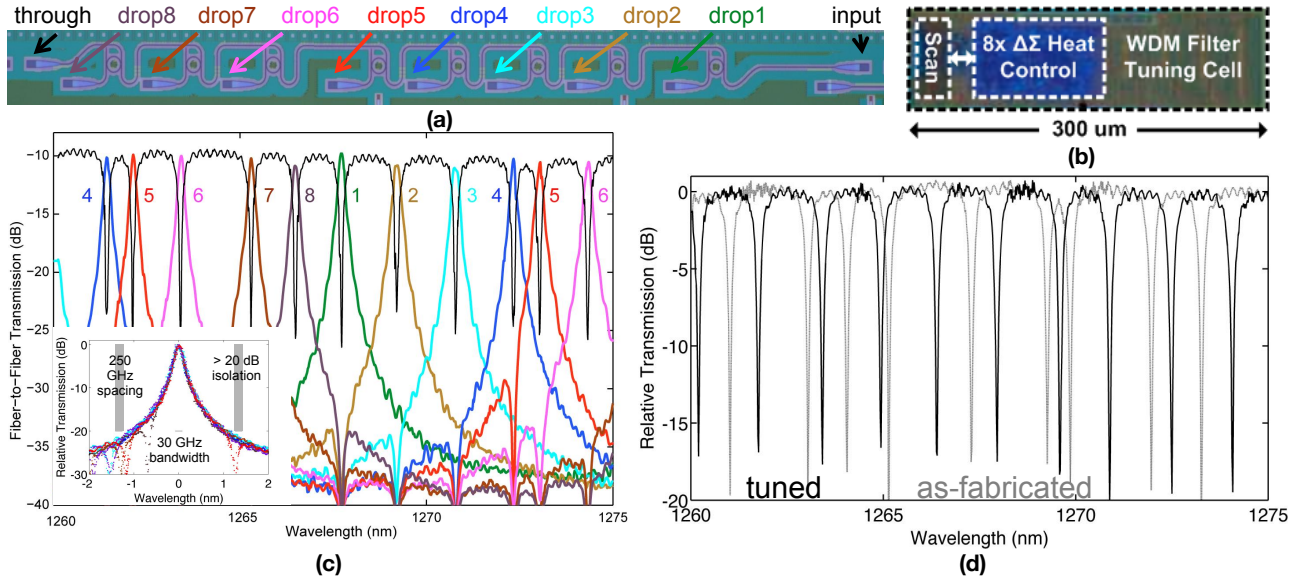

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Fig. 6. Thermally-tuned optical filter bank electronic-photonic subsystem [11]: (a) 8-channel filter bank comprising microring resonator filters with integrated microheaters; (b) digital heater controller next to the filter bank; (c) filter bank response without tuning showing unevenly spaced channels due to fabrication variations. The fabrication variations are small in this advanced process, as evidenced by the fat that the channels are in order as designed (detunings are small) and the passbands all match [inset: all passbands overlapped for comparison]. (d) Tuning controller produces equispaced channels.

with no tuning. The relatively even channel spacing, in intended order (i.e. much less than one channel spacing of fabrication error induced detuning), as well as the indentical passband shapes [Fig. 6(c), inset], indicate a high quality and repeatable process – an intrinsic advantage of using an advanced foundry CMOS process. The detuning present due to fabrication variations is compensated using the on-chip thermal tuning circuit [11].

In addition to wavelength (de)multiplexers, energy efficient monolithic transmitters and receivers are needed to enable silicon photonics based electronic-photonic systems. Our first demonstration of a monolithic silicon photonic transmitter employed a ring resonator based on a rib-like waveguide using poly and body silicon layers [25], showing 1.23pJ/bit energy at 2.5Gbps. The waveguide had high propagation loss due to the lossy polysilicon, limiting the cavity Q to a few thousand, and requiring a large wavelength shift to achieve reasonable extinction ratio. As a result, injection mode

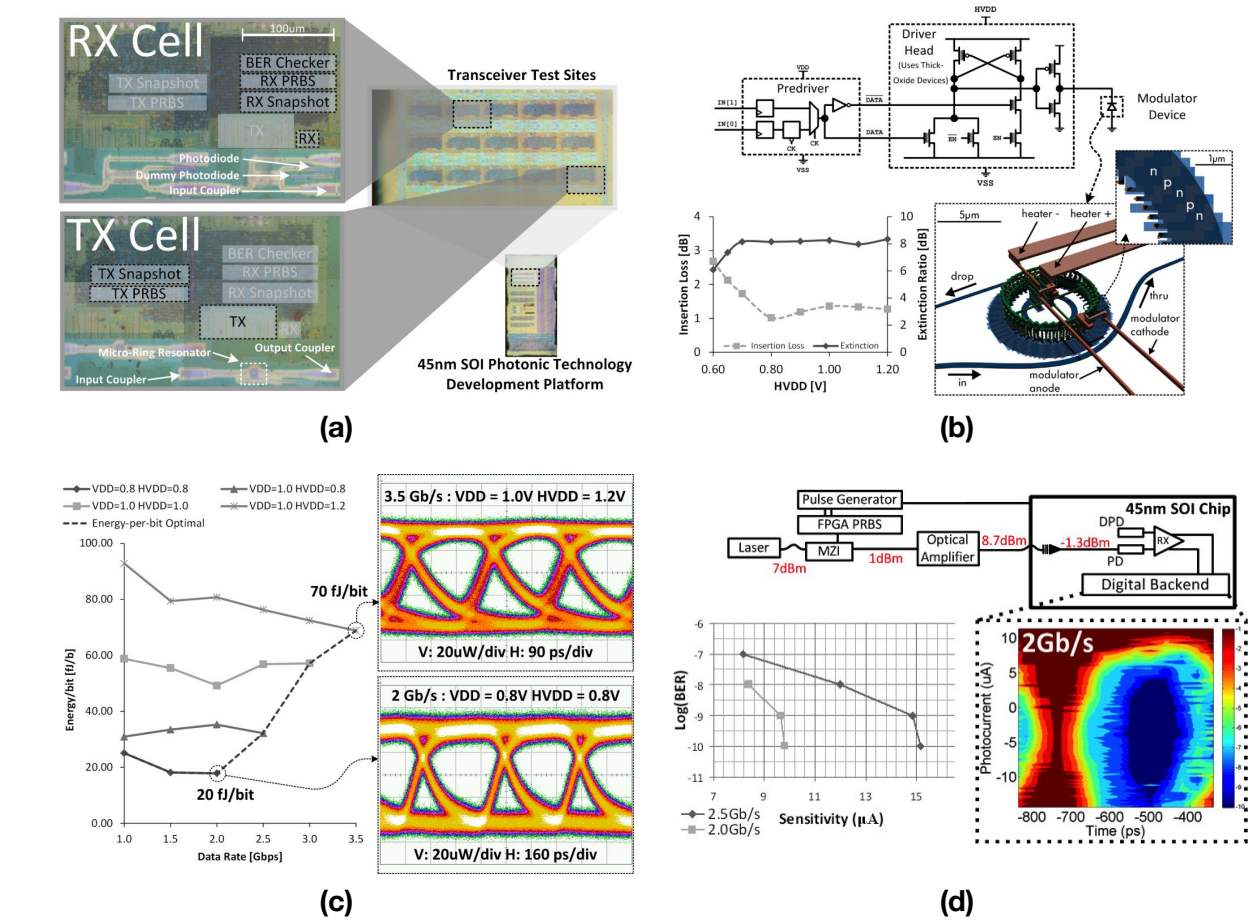

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Fig. 7. Optical transmitter and receiver electronic photonic subsystems [23]: (a) 3x6 mm chip showing monolithically integrated transmitter and receiver sites. (b) spoked ring modulator driven by on-chip circuit shows 1dB insertion loss and 3.5 dB extinction ratio with 0.8 to 1.2V rail voltages in the driver. (c) Eye-diagrams demonstrating (record) 20fJ/bit transmitter energy at 2Gbps. (d) Monolithic receiver, using to form detectors the SiGe source and drain regions normally used to increase mobility in sub-65nm transistors. Receiver energy of 220fJ/bit at 1.2 micron wavelength.

operation (using a p-i-n structure) was used, limiting the speed to 600Mbps before preemphasis and the energy of the pre-emphasized transmitter to a picojoule.

The depletion-mode spoked ring modulator in Fig. 4 was included as part of a monolithic transmitter (Fig. 7) [26]. The higher Q of around 15,000 when loaded and critically coupled (due to implementation fully in the crystalline body layer only), allowed a narrow resonance, and 3.5dB extinction with 1dB insertion loss with only a 1.2V swing. In this demonstration a higher voltage capable driver was used, to allow for worse performing modulators. The complete transmitter demonstrated a 20 fJ/bit energy at 2Gbps and 70 fJ/bit at 3.5Gbps [26]. More recent work that has replaced that driver with a logic inverter based driver showed sub-30 fJ/bit total (wall-plug) energy up to 6+ Gbps.

A receiver using SiGe photodiodes was also implemented [26], demonstrating 15 uA sensitivity at a cost of 220 fJ/bit.

5. CONCLUSIONS AND OUTLOOK

We have demonstrated that photonic devices with respectable to excellent performance can be designed within the constraints of an unmodified, sub-100nm, microelectronics SOI CMOS process. Furthermore, aspects of advanced CMOS processes provide opportunities for advanced designs, such as ultra-high efficiency nanoantenna array based

grating couplers, and finely grained dopant masks for spoked-ring microcavity modulators. Subsystems were demonstrated showing integrated on-chip tunable filter banks, record energy monolithic transmitters, and the first infrared receivers in unmodified CMOS. The work ahead will attempt to combine these components to demonstrate a viable platform for low-energy interconnects for microprocessor-to-memory communication. Current efforts are also aimed at broadening the photonic device library and platform capabilities, including advanced filters [27], photonic crystal microcavities [28-30], and four-wave mixing [31].

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