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Study of Gold Diffusion Kinetics in p/p+ Epitaxial Silicon

by
Edward C. Wu

Submitted to the Department of Materials Science & Engineering
in Partial Fulfillment of the Requirements for the
Degree of

Bachelor of Science
in
Materials Science & Engineering

at the

Massachusetts Institute of Technology

June 1998

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ABSTRACT

Boron doped, dislocation-free p/p+ epitaxial silicon was studied to determine gold diffusion behavior at the interface region.. Samples annealed at 700°C, 800°C, and 1000°C were examined under Deep Level Transient Spectroscopy and Spreading Resistance Measurement. As hypothesized, presence of the p+ region proved to be a sink for Au. Detection of enhanced solid solubility limit, by over five orders of magnitude, was evident in all three annealing temperature samples. The enhanced solubility at the interface causes a resulting gradient that drives rapid gold diffusion. Therefore, depletion of Au source prior to the epilayer is detected.. Subsequently, reduction in compensation bolsters an increase in minority carrier concentration.

Thesis Supervisor: Lionel C. Kimerling
Title: Thomas Lord Professor of Materials Science & Engineering

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1.0 Introduction

Interest in p/p+ and n/n+ epitaxial silicon has increased rapidly over the years. It has become the standard in semiconductor industries, due to its inherent advantages as starting material for small geometry CMOS devices [1]. Structural defects at the epilayer-substrate interface and within the epitaxial layer have been the subject of various previous investigations [2,3], but electrically active centers have rarely been studied. In this work, the diffusion kinetics of gold in p/p+ epitaxial silicon are investigated. Due to its ability to introduce deep electronic levels into silicon, gold is used in high-speed electronic devices to control the base minority-carrier lifetime; it is also well known that deep levels can contribute to junction leakage in MOS devices and hence affect device performance and reliability. Hence, an understanding of the diffusion mechanism of gold in silicon is highly desirable from a electrical point of view.

As empirical research have shown gold diffusion to be a function of silicon point defects (i.e. vacancies and self-interstitials), the complexity of its diffusion kinetics arises in examining how the p+ substrate region of epitaxial silicon dictates gold diffusion through the epilayer and into the bulk wafer. Point defect concentrations are expected to change at the interface, accompanied by the high boron doping concentration of $\sim 10^{18}$cm-3. The experiment conducted here focuses and compares gold diffusion in epitaxial p/p+ silicon wafer to that of plain p-silicon. Gold diffusion profile is assessed through Deep Level Transient Spectroscopy (DLTS) and Spreading Resistance measurement. Particular focus is placed on the interface regime where the heavily doped boron region is expected

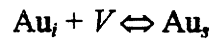
to vary the point defect concentration, and thus the solid solubility and diffusivity of gold. It is hypothesized that the p+ region will function as sinks for Au impurities.

2.0 Theory/ Background

The diffusion mechanisms of point defects in Si and their properties such as their charge stages, equilibrium concentrations, and diffusivities are technologically very important for the fabrication of semiconductor devices. Specifically, gold impurities are known to introduce deep electronic levels into the silicon energy band gap which then serves as recombination centers or traps, thereby reducing minority carrier-lifetime. Furthermore, gold is a rapid diffuser with large solid solubilities and capture cross section. As will be discussed later in more detail, the fact that Au thermodynamically situates in substitutional lattice sites and diffuses interstitially means that its diffusion is a function of point defect concentration. The utilization by industry of epitaxial p/p+ and n/n+ silicon wafers makes the profiling of gold to be of interest.

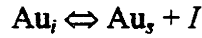
In silicon, Au atoms are known to occupy both either substitutional (Au_s) or interstitial (Au_i) sites. It is also known (Figure 1) that the solubility of Au_s is larger than that of Au_i, whereas the diffusivity of Au_i greatly exceeds that of Au_s by several orders of magnitude. [4] Clearly, an interplay governed by native point defects in Si must exist between the interstitial and substitutional sites. This gives rise to two possible relationships:

1. Dissociative Mechanism (aka. Frank-Turnbull)



$$Au_i + V \Leftrightarrow Au_s$$

2. Interstitialcy Mechanism (aka. "Kick-out")



$$Au_i \Leftrightarrow Au_s + I$$

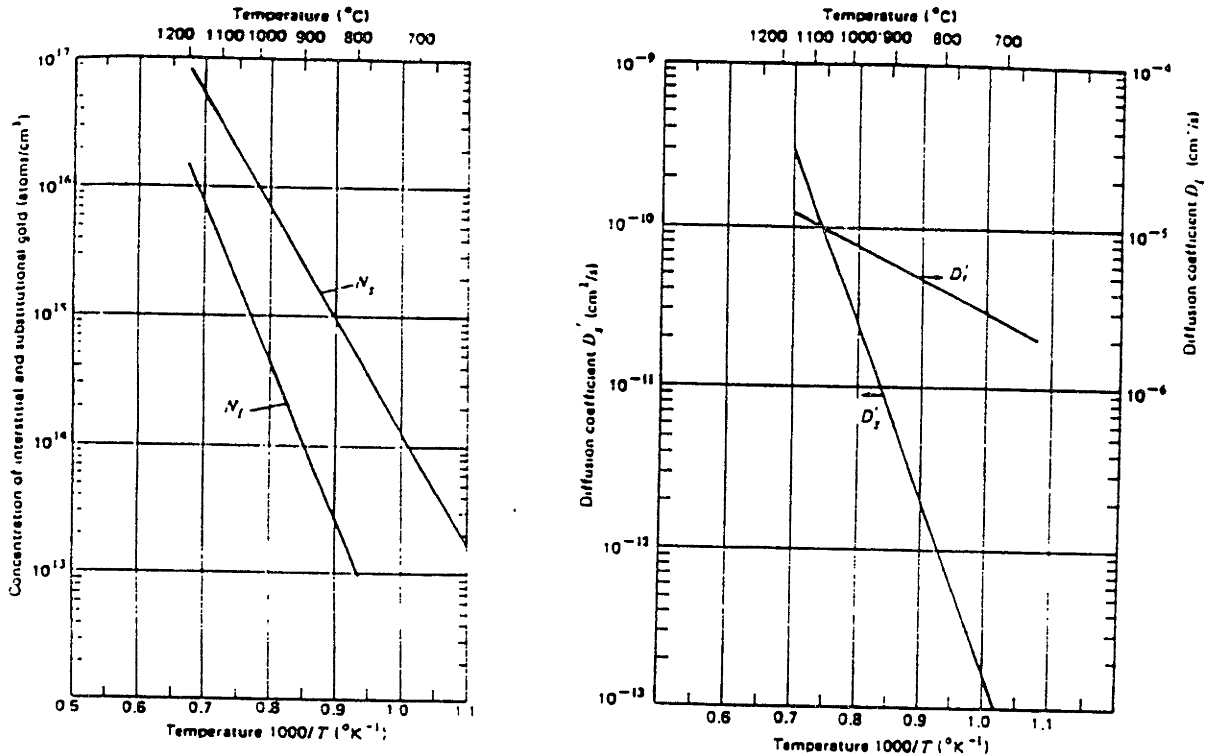


Figure 1: Solubility and Diffusivity between Au_i and Au_s

2.1 Dissociative Mechanism

The dissociative mechanism can consist of four separate steps: (1) diffusion of interstitial gold from the surface, (2) reaction of Au_{int} with Si_v, (3) diffusion of vacancies

from surfaces, and (4) production of vacancies in the bulk. Theoretically, any one of these steps can be rate limiting. The reaction of Au_{int} with Si_v is assumed to be fast so that an available Si_v will instantly react with Au_{int}. This means that the initial diffusion of gold will then deplete the bulk of Si_v. Further buildup of gold in the wafer is limited by the time required to introduce additional silicon vacancies into the bulk. This occurs either by the diffusion of silicon vacancies from the surface or by bulk generation. (Figure 2) In the dissociative mechanism, interstitial metal reacts with silicon vacancies to form substitutional metal. The rate limiting step in this process is bulk vacancy generation.

2.2 Kick-Out Mechanism

Like the dissociative mechanism, the kick-out mechanism also consists of four separate steps of which any one can be rate limiting: (1) diffusion of interstitial gold from the surface, (2) the reaction of Au_{int} to create Si_{int} and Au_{sub}, (3) diffusion of Si_{int} to surface sinks, and (4) recombination of Si_{int} in the bulk. It is assumed that the reaction of Au_{int} to create Si_{int} and Au_{sub} is fast so that local equilibrium is maintained. As Au_{sub} builds up, excess Si_{int} is created. The recombination of this excess Si_{int} is the rate limiting process. The excess Si_{int} can either diffuse to the surface or recombine in the bulk. (Figure 3)

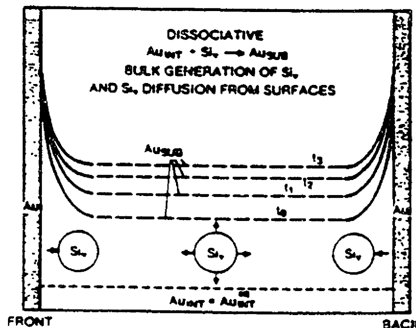


Figure 2 : Dissociative Mechanism in Si wafer

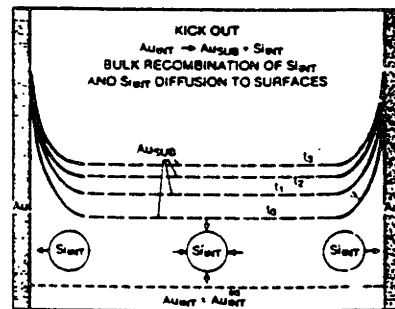


Figure 3: Kick-out Mechanism in Si Wafer

When the generation of vacancies is sufficient, the dissociative mechanism is preferred. But at higher temperatures, the solubility of substitutional gold rises and the generation rate of silicon vacancies is insufficient for gold to diffuse into silicon via the dissociative mechanism. Due to this, the kick-out mechanism dominates for the diffusion of gold into silicon at high temperatures. [5] Recent investigations have confirmed that Au diffuses predominately via the kick-out mechanism. Several important inferences and be drawn from this:

1) The movement of gold in siiicon is controlled by the reaction of gold with silicon interstitials, not by the intrinsic diffusion coefficient of gold.
2) Wafer surfaces are the only sinks at which the self-interstitials produced in supersaturation by the kick-out reaction can be removed. [6]
3) The migration of self-interstitials to the surfaces is a slow process and thus limits the transport of Au_s.

2.3 Au Diffusion in Boron-Doped Silicon

Recent research by Bracht et. al [7] detected increase Au concentration in the center of the Si sample with increasing Boron background doping. Enhanced transport capacity of both Au_i and Si self-interstitials was also seen with increased Boron concentration.

3.0 Design of Experiments

In order to effectively and accurately evaluate the gold diffusion profile of p/p+ silicon through electrical characterizations (i.e. DLTS and Spreading Resistance measurement), a series of scientific queries must first be resolved.

3.1 Rapid Thermal Annealing (RTA)

Straight deposition of Au layer onto silicon followed by annealing will produce an irregular and inconsistent Au-Si interface boundary/reference point that makes accurate profiling of gold diffusion unfeasible. Rapid thermal annealing can remedy this problem. As indicated by the phase diagram (Figure 4), the eutectic temperature of Au/Si exists at 363°C. Rapid heating of the samples at a high temperature exceeding T_{eut} will: 1) ensure melting at the interface first and 2) uniformity of melt. Rapid quenching to room temperature will then "freeze" the melting process and preserve a flat, smooth interface that is needed for annealing.

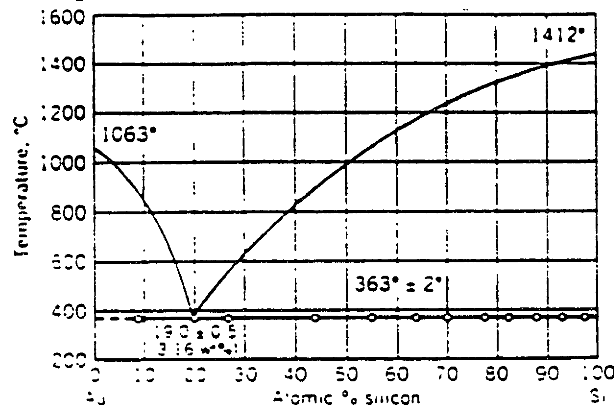


Figure 4: Phase Diagram of Au/Si

As seen in preliminarily results (Figures 5,6,7) RTA-ing at 900°C for 60 seconds ensures the flattest Au/Si interface.

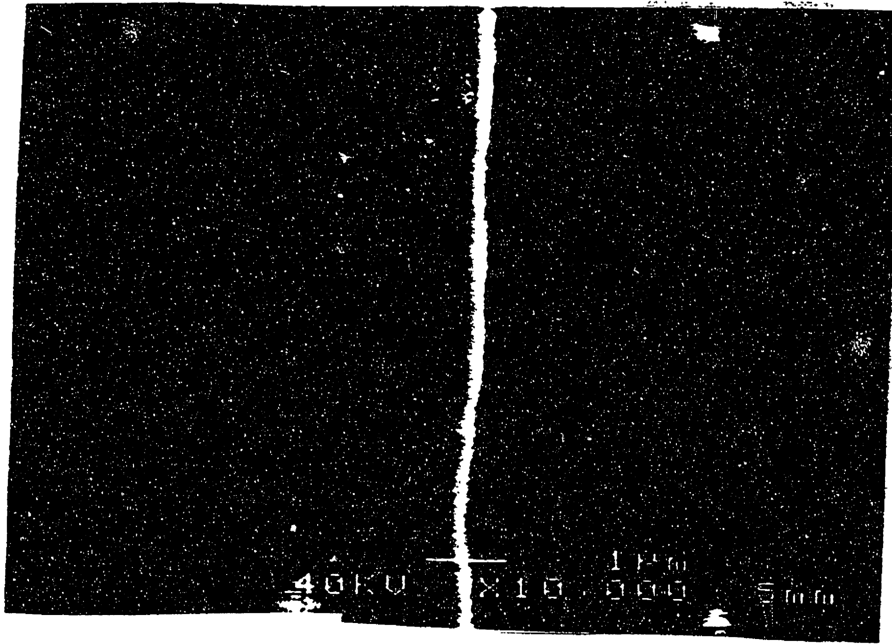


Figure 5: 600°C RTA for 60 secs

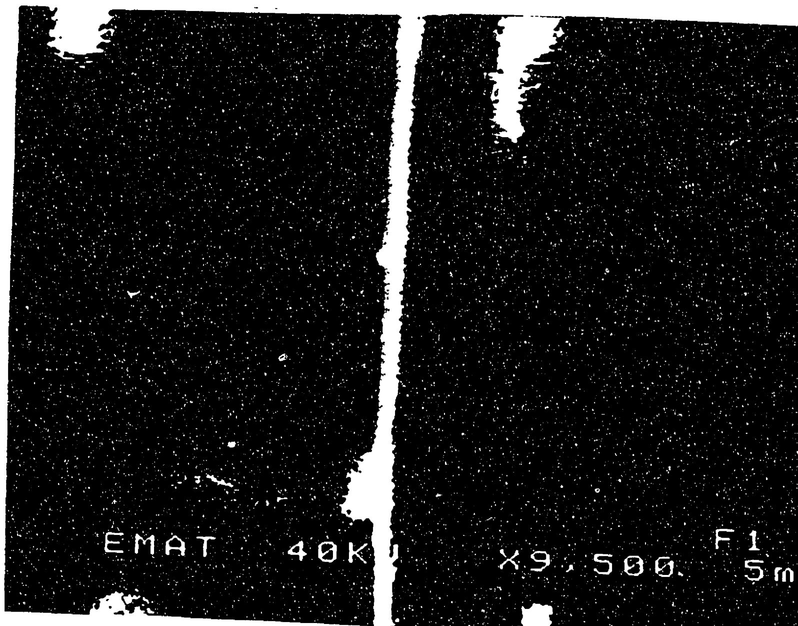


Figure 6: 900°C RTA for 60 secs

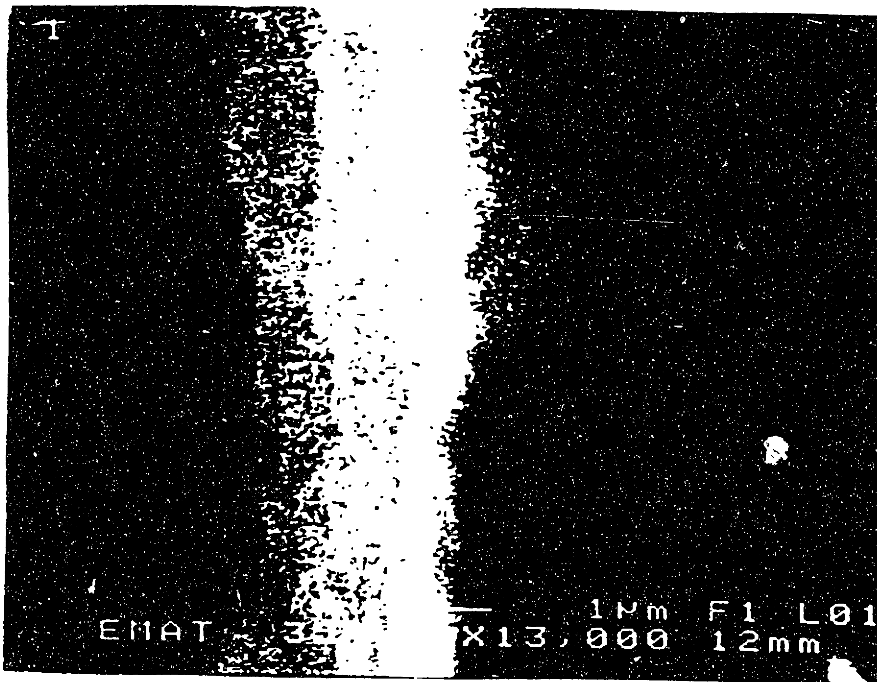


Figure 7: 900°C RTA , 600°C anneal for 1 ½ hrs

In actuality, RTA temperatures of 700°C and 800°C for 60 seconds were used on the samples. The hesitation to operate at any higher temperatures, such as 900°C, can be explained from preliminary experiments which showed Au concentration greatly exceeding that of the dopant concentration rendering accurate profiling by DLTS and Spreading Resistance measurement useless.

3.2 Annealing Temperature and Time

Both the DLTS and Spreading Resistance measurement has resolution limitations. Detection of deep level states of impurities by DLTS assumes the condition where the solubility of Au < 10% of the boron dopant concentration (5.5×10^{14}). This would occur at low temperatures where the diffusion of gold is low. Conversely, resistance measurements

are done for high temperature samples where compensation occurs because the $C_{Au} >> N_{A,Boron}$. Considering these conditions, samples were heat treated at high (800°C & 1000°C) for 10 minutes and low (700°C) for 20 minutes to qualify for both electrical tests.

3.3 Electrical Characterizations

As will be further explained in section 5.1.1, the 700°C samples, upon completion of annealing, had thicknesses of 5, 8, 11, and 14 μms polished off from the surface. Recall that the epilayer is 16 μm thick, and the DLTS spatial resolution is 1-3 μm maximum. Thus, in order to detect substantial changes in the diffusion profile at the epilayer interface, controlled polishing of varying thicknesses was necessary. Lastly, establishing good Titanium Schottky contacts with low leakage current (<10 μA) is a necessary precursor to performing any electrical characterizations (i.e. capacitance-voltage (C-V) measurements and DLTS).

4.0 Procedure

The starting materials are 4" diameter silicon wafers grown by both Float-Zone (FZ) and Czochralski (CZ) methods. The control specimen for this experiment is a dislocation-free, p-type, boron doped (~10^{15} cm-3), <100> direction silicon wafer. On the other hand, the p/p+ epitaxial samples are of similar nature, except the epitaxial layer is 16μm thick with a boron doping concentration of 10^{15}, whereas the bulk p+ region is 650 μm thick with 10^{18} boron concentration. Both plain and epitaxial silicon exhibit a resistivity of 14-24Ω.

Samples were prepared for annealing at three different temperatures: 700°C, 800°C, and 1000°C. Table 1 briefly summarizes the overall process leading up to the electrical characterizations:

Step	Process
1	Sample Clean: elimination of contaminants
2	Au Layer Deposition by Evaporative Coating
3	Rapid Thermal Annealing @ 700°C and 800°C: generation of flat Au/Si interface
4	Scanning Electron Microscope: inspection of interface
5	Anneal: in-diffusion of Au @ 700°C, 800°C, and 1000°C
6	Polish off 5, 8, 11, or 14 μm of Au layer
7	Evaporative Deposition of Ti Schottky Contacts
8	Electrical Characterization: C-V Measurements Resistance Measurement Deep Level Transient Spectroscopy

Table 1: Process Summary

4.1 Sample Clean

Prior to Au film deposition, all samples are cleaned to eliminate any sources of wafer contamination as well as to ensure a clean integrity for future processes. The cleaning procedure commences with removal of any organic residues or contaminants. Each sample is ultrasonically cleaned for 5 minutes under Tricholoroethane, Acetone, and Methanol. Next, removal of metallic contamination from surface is accomplished by immersion in Piranha (Sulfuric Acid: Hydrogen Peroxide in 3:1 ratio) for 5-7 minutes; the Piranha entraps the contaminants in oxide (SiO_2) formation. Samples are then rinsed in di-ionized water. Lastly, the oxide layer and the metallic contaminants are removed by etching in dilute HF (1%) for 30 seconds.

4.2 Au Deposition by Evaporative Coating

Metallic deposition will occur by evaporative vacuum means. The chamber is first pumped down to 10^{-7} millitorr to ensure a high mean free path for the source molecule being evaporated onto the surface, while at the same time reducing impurity arrival rate onto the silicon surface. [14] Current (~40-60 kVs) is sent through a resistive wire, which upon heating, melts the Au source metal and evaporates onto the target wafer.

4.3 Rapid Thermal Annealing (RTA)

Establishment of a flat smooth Au-Si layer interface, prior to annealing, is accomplished by RTA. Samples are rapidly heated and cooled to room temperature. To maintain a gold concentration that is less than the boron concentration, samples were RTA-ed at either 700°C or 800°C for 10 seconds.

4.4 Anneal

Drive-in diffusion of gold was carried out in sealed quartz ampoule under a nitrogen atmosphere. Samples were annealed at three different temperatures: 700°C, 800°C and 1000°C. The 700°C samples were annealed for 20 minutes while the 800°C were heat treated for 10 minutes. Temperature control was monitored by a thermocouple connected to the furnace.

4.5 Mechanical Polishing

Starting with a 30μm diamond grit-size paper, thicknesses of 5, 8, 11, or 14 μms were mechanically polished off the epitaxial p/p+ samples. Thickness control was roughly

monitored by a micrometer. Subsequent polishing with 15, 5, and 1 μm size grit paper ensured a smooth surface necessary for Schottky contact making.

4.6 Schottky contacts

Prior to titanium deposition, all samples undergo a second cleaning, similar to that described in section 4.1. The only difference is the removal of metallic contamination by a 20:1 mixture of Nitric acid and HF for 1-2 minutes, instead of a Piranha clean. A Schottky mask is placed over the samples, exposing only certain regions for metallic deposition. The vacuum evaporative deposition proceeds as described in section 4.2.

4.7 Electrical Characterization

Gold diffusion profiling (concentration vs. distance) is done by either Deep Level Transient Spectroscopy (DLTS) or Spreading Resistance Measurement. The "low" temperature (700°C) samples were characterized by DLTS, whereas the high temperature (800°C and 1000°C) samples were analyzed by a four-point resistance measurement. The surfaces of the 800°C and 1000°C samples were beveled (See Section 5.2) in order to profile at various thicknesses. The criteria for accurate DLTS measurements require Schottky contacts exhibiting low leakage current (<10 μA) before conducting any further tests. Capacitance versus voltage (C-V) measurements were also taken to see the compensation effects of gold on boron.

5.0 Experimental Apparatus

5.1 Deep Level Transient Spectroscopy (DLTS)

The detection of transition metal impurities occupying deep energy levels within the silicon band gap as recombination centers or traps requires capacitance transient spectroscopic techniques to characterize the point defects in semiconductor materials. By applying a reverse bias to the Schottky diode on the sample, electrical and optical properties of defects in semiconductors can be obtained. Furthermore, such capacitive measurements are made in a region of the semiconductor that is essentially devoid of mobile carriers, thereby providing a very convenient location for the observation of isolated electronic transitions. [8] Because deep traps have been found to greatly influence apparent free-carrier profiles determined by capacitance-voltage (C-V) measurements, use of Deep Level Transient Spectroscopy in this experiment will produce a fine resolution of gold diffusion profile in p/p+ epitaxial silicon.

5.1.1 Schottky Behavior Under Reverse Bias

In a simple p-n junction where one side is doped more heavily than the other, application of a reverse bias drives a depletion layer that almost spans the width of entire lightly doped region. The width of the depletion layer is expressed by:

$$W = [2\varepsilon(V_{bi} + V)/(qN)]^{1/2}$$

where ε is the dielectric constant, V_{bi} is the built-in voltage, V is the applied bias voltage, q is the charge of an electron, and N is the density of ionized doping centers in the lightly

doped material. This behavior holds true also for Schottky diodes, formed by metal deposition onto a semiconductor surface. (See Figure 8)

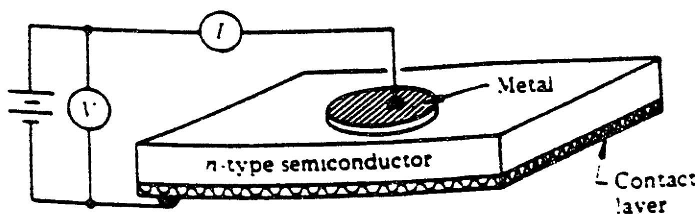


Figure 8: Example of a Schottky barrier

By comparing the Schottky diode behavior to that of a parallel plate capacitor ($C = \varepsilon A/W$) and knowing that the depletion width (W) is proportional to $V^{1/2}$, the capacitance of this voltage dependent capacitor behaves inversely with increasing bias voltage. This assertion holds true assuming uniformity of doping in the lightly doped regime.

The extrapolation of local doping density N(W) from the depletion width of the capacitance measurements formulates the basis of "junction-profiling" - the fundamental basis for junction transient capacitance measurements. [8] Worthy of note is that the spatial resolution limit by electrical junction profiling is set by the Debye length l_D:

$$l_D = [kT\varepsilon/(q^2n)]^{1/2}$$

where k is the Boltzmann's constant, T is the absolute temperature, and n is the free carrier density at the probed region. Figure 9 correlates the free carrier density as a function of Debye length at 300°K.

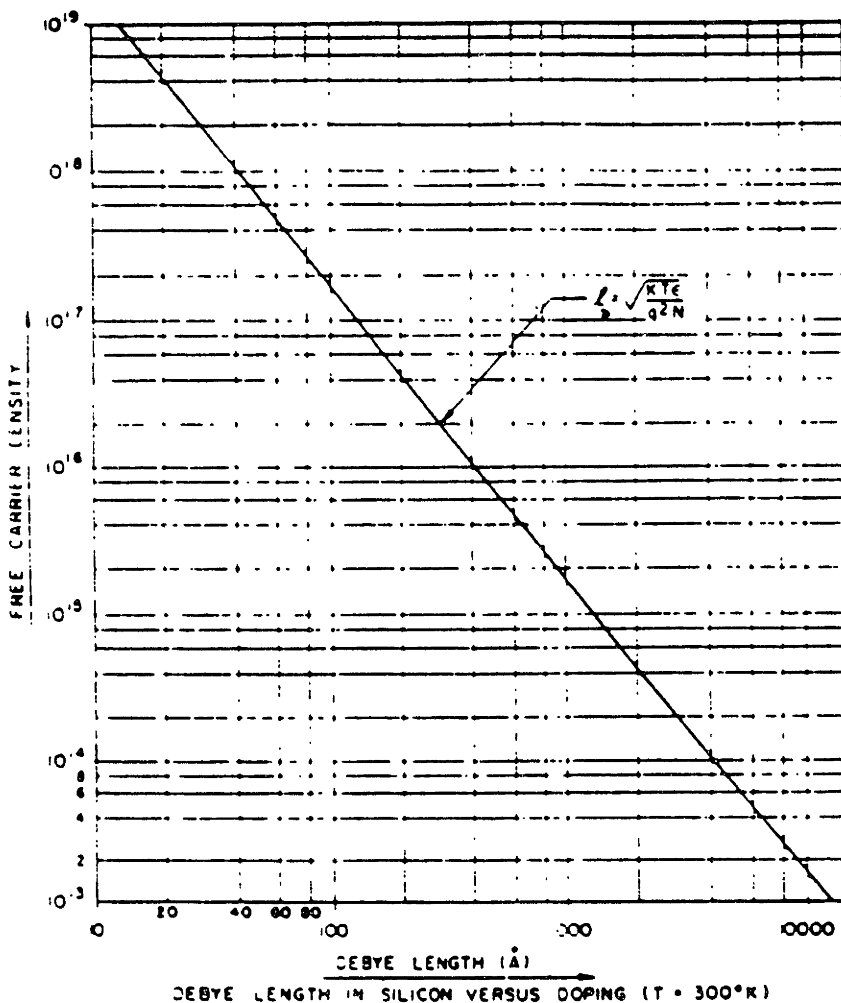


Figure 9: Free Carrier Density vs. Spatial Resolution (Debye length)

5.1.2 Defect States on Semiconductor Junction

Our formal discussion assumed no metal impurities occupying any deep level energy levels in the silicon band gap. In reality, defect states are often introduced into the band gap due to perturbation of the bonding structure of the host material by the presence of a lattice defect or impurity. [8] The presence of a defect center may function as a majority carrier trap, in which the 'capturing' and thermal emission of a majority carrier affect the junction capacitance. Capacitance spectroscopy utilizes this phenomenon (generation-recombination process) in the transition region of the p-n junction to determine the equilibrium occupation of defect states.

Because states within the depletion zone have no possibility of being filled by capture processes, emission process can only be observed by forced introduction of carriers which are to be captured. This can be accomplished by pulsing the junction bias. As illustrated in Figure 10, an initial reverse bias creates an empty space region with no available mobile carriers for capture. In Step 2, a pulse to reduce V_R will momentarily collapse the space charge region making majority carriers available for capture. When the pulse is turned off (Step 3) and V_R reestablished, the junction capacitance is reduced because compensating majority carrier charge has been trapped in the space charge region. Defect states which are filled during the pulse will return to their initial state if provided enough thermal or optical energy. (Step 4) The rate of carrier emission during this recombination-generation process is defined as:

$$e_n = \{[\sigma_n \langle v_n \rangle N_c]/g\} \exp(-\Delta E/kT)$$

where σ_n is the capture cross sections for electrons and holes, $\langle v_n \rangle$ denotes the average thermal velocity of electrons, N_c is the effective density of states, g is the degeneracy of the level, ΔE is the energy difference between the conduction band and defect state level, k is Boltzmann constant, and T is temperature. The characteristic time constant for this transience is defined as $\tau_n = e_n^{-1}$. Consequently, one can repeatedly pulse the junction with short pulses and measure the resulting capacitance change after each pulse, taking as much time as is desirable to make each capacitance measurement. [8]

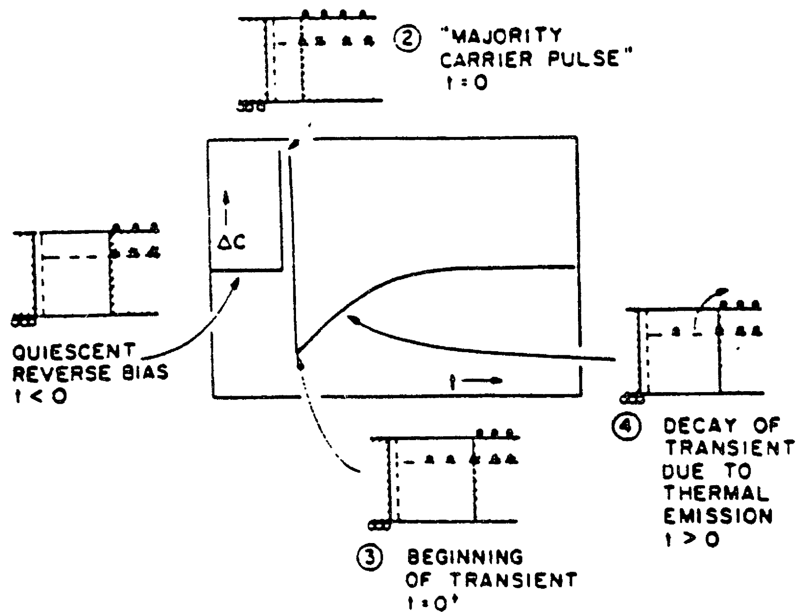


Figure 10: Transient Capacitance

The DLTS method introduces a technique for displaying the time constant of the decaying capacitance signal. The capacitance versus time information from a transient capacitance experiment is processed so that a selected decay rate produces a maximum output. [8] By observing a p-n junction repetitive capacitance transient through a designated rate window (e_n), and on slowly scanning the sample temperature (thereby changing the thermal emission rate and therefore the capacitance decay rate itself), a peak appears in the temperature versus output plot, thus generating a DLTS Spectrum. Figure 11 shows the DLTS spectra for Au. Note the peak at 150°K indicative of occupancy of Au atoms at the 0.35eV electronic defect state level; conversely, a smaller peak at 250°K indicates the presence at the 0.54eV level. The strength of the DLTS method is that each defect state may be studied independently through its unique activation energy for carrier emission, cross section for carrier capture and cross section for thermal excitation. [8]

Figure 11: DLTS Au Spectra

5.2 Resistance Measurement

At high temperature annealing, the in-diffusion of gold into the bulk silicon is expected to greatly exceed that of the Boron doping concentration ($N_{A,Boron} = 5.5x10^{14}$). From Figure 12, one realizes that Au has amphoretic properties and thus occupies 2 possible band levels: 0.54eV from the conduction band E_c and 0.35 eV above the valence band E_v. The Fermi Energy level E_f, dictated by the Boron concentration, lies 0.054eV above E_v. Because $C_{Au} >> N_{A,Boron}$ under high temperature, compensation is bound to occur.

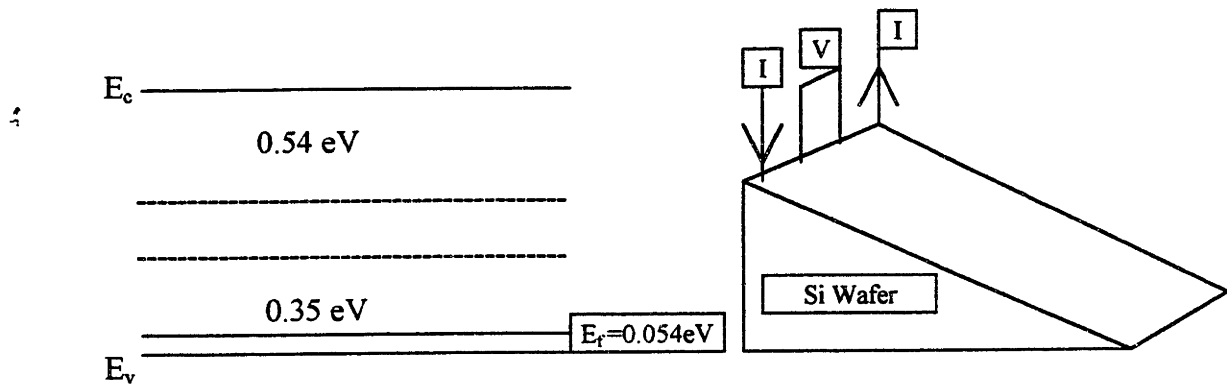


Figure 12: Au Energy Level

Figure 13: 4-Point Resistance Measurement utilizing Beveled Si surface

The high resistance expected from compensation renders the use of fine resolution DLTS inadequate. Thus, resistance measurement through the 4-point probe technique on a beveled surface will give a gold diffusion profile with respect to distance in the z-direction. (Figure 13) Current is passed through the outer two probes, and the drop in voltage detected by the inner two probes will decipher the resistance of the sample. By the relation:

$$R = V/I = (\rho L)/(wt)$$

where is ρ resistivity, L = length, w = width, and t = thickness of the measured region..

$$\rho = 1/\sigma = q\mu_n N_{net}$$

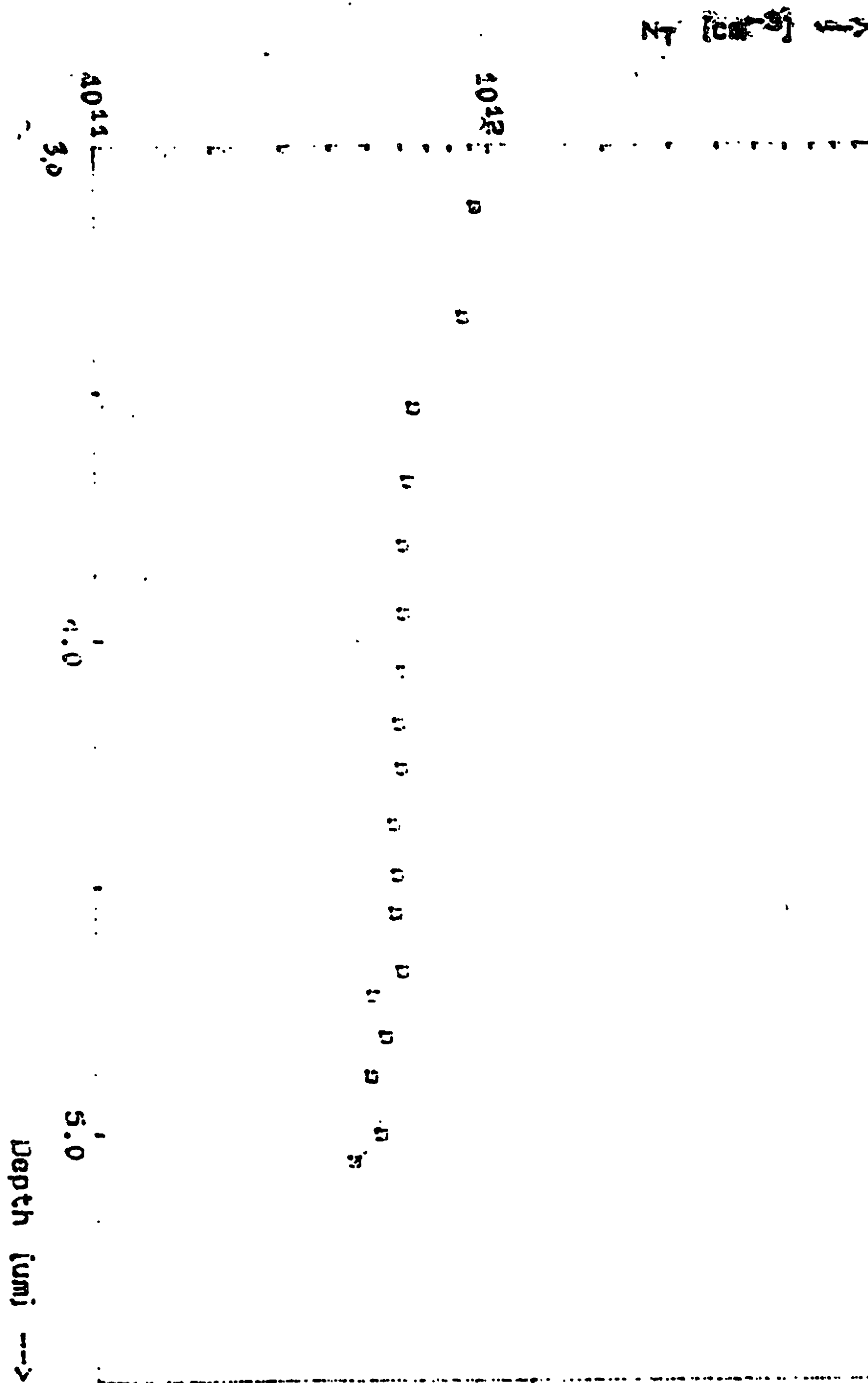
where $N_{net} = N_{boron} - N_{Au}$, one can determine the carrier concentration of gold, knowing that N_{boron} is set at 5.5×10^{14} cm-3. Measurements are taken at various height thicknesses to profile the gold diffusion.

6.0 Results and Discussions

Because of a spatial resolution of 1-3 microns, samples annealed at 700°C had 14 μms polished off the epilayer so that DLTS measurements can detect gold's diffusion behavior prior to and at the interface region. The DLTS measurements of the 700°C annealed samples showed appreciable diffusion profile differences between the p and p/p+ epitaxial samples. As seen in Figure 13, the gold diffusion in the plain p-silicon maintained at a near constant concentration of approximately 6×10^{12} cm-3. Note however, that the p/p+ sample started with roughly the same gold concentration as the control, but rapidly decreased to a concentration of 2×10^{11} cm-3 at a depth of 4.3 μm and then increased significantly after 4.4 μm (Figure 14). The apparent discontinuity that appears in the profile can be explained by the lack of resolution to detect Au concentration less than 10^{11} cm-3.

As can be expected, a drive-in diffusion at a temperature of 800°C will yield a greater gold concentration due to higher thermal activation. Figure 15 shows an increase in Au concentration (5×10^{14} cm-3 versus 6×10^{12} cm-3 of the 700°C sample). But greater significance lies in the comparison between the control and epitaxial samples. Once again,

note the depletion of gold in the p/p+ sample at a depth of 14 µm. But at the epilayer interface, the resistance measurement picked up an enormous concentration of Au (4 x 10^{18} cm-3).



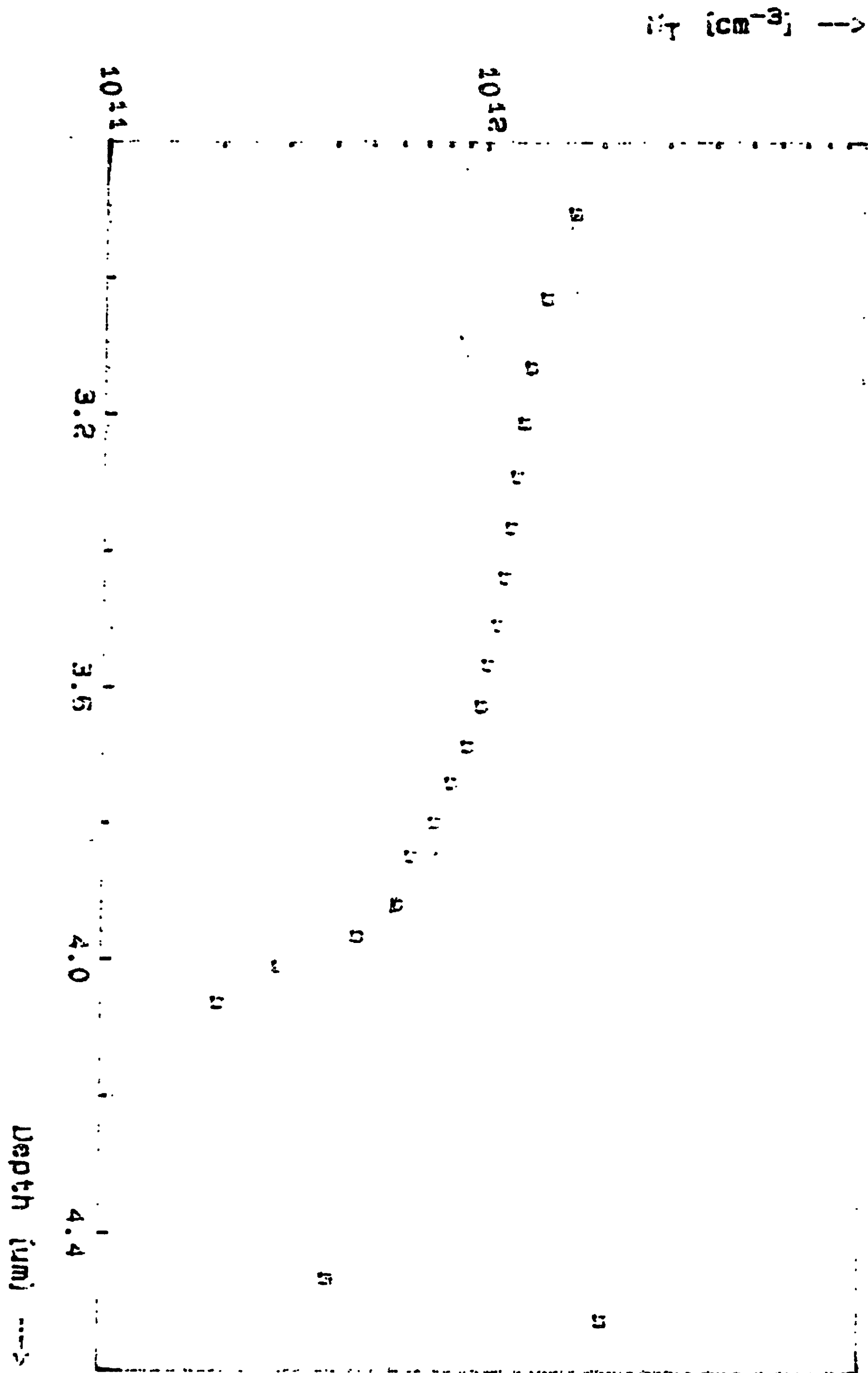


Figure 15: DLTS Result of 700°C p/p+ Silicon

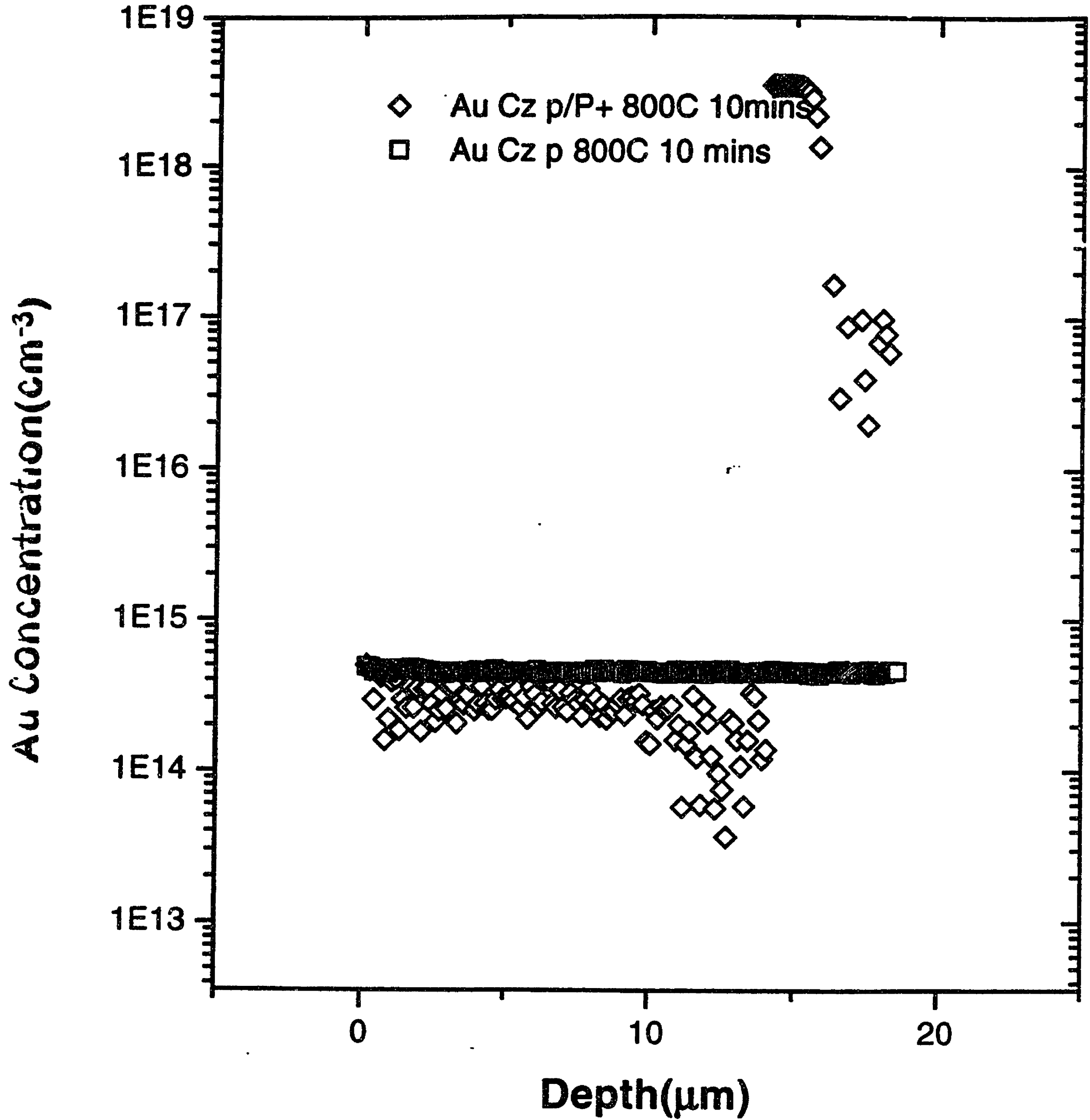
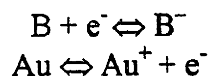


Figure 16: Spreading Resistance Measure of 800°C for p & p/p+ Silicon

Although the data would imply that there is an increase of over 5 orders of magnitude in Au concentration, this assumes no concentration gradient between the epilayer and substrate region. Such is the assumption and simplification made in these resistance measurements. The difficulty in measuring the actual boron concentration, due to a diffusion gradient at the interface region, makes it difficult to accurately estimate the precise gold concentration. Nonetheless, several inferences can be drawn from this behavior. The presence of the p+ layer has a solubility enhancement effect on gold at the interface. Consequentially, this causes a solubility gradient between the epilayer and the bulk wafer. The need to reach equilibrium between the disparity therefore drives increased gold diffusion towards the interface. This causes a depletion of the source concentration as provided by the epilayer, from $5x10^{14}$ to $2x10^{13}$ cm-3. Lastly, the steep drop in Au concentration as detected in the p+ substrate region (beyond 15 μm) can be explained by the short annealing time of 10 minutes. It can be expected that longer annealing time will drive the system towards equilibrium, at which time greater Au concentration will be detected at distances deep into the bulk wafer.

In looking at the charge neutrality chemical equations:



$$B + e^- \Leftrightarrow B^-$$
$$Au \Leftrightarrow Au^+ + e^-$$

the substantive increase in Boron concentration from the substrate would consume electrons and drive the reaction towards ionization. Subsequently, the lack of electrons to neutralize the Au^+ perpetuate continual ionization of Au atoms, thus driving to greater solubility at the epilayer. As confirmed by Figure 16, solubility enhancement has increased

by two orders of magnitude (10^{17} cm-3). Once again, the higher Au concentration "detected" above 10^{17} cm-3 is attributed to the simplified assumption that no Boron concentration gradient exists at the interface, when in actuality it is quite conceivable that interdiffusion has taken place. When compared (see Appendix) to the diffusion modeling done at 800°C (@ 30 minute time intervals) of plain silicon where diffusivity and C_S, using the semi-infinite solid solution to Fick's Second Law of Diffusion, was calculated to be 7.16×10^{-9} cm^2/s and 9×10^{14} cm-3 respectively, the experimental results reveal a contrasting solubility enhancement, which would also inadvertently hint at increase Au diffusivity.

Figure 17 also plots Au concentration versus carrier concentration as a function of depth. Of particular interest is the rapid increase of carrier concentration near the 15 μm mark. This behavior can be explained through the decrease in compensation effects as the Au concentration is depleted near the epilayer interface. Subsequently, there should be a decrease in resistivity measurements as carrier concentration increases. With samples annealed at 1000°C (Figure 18), the rapid depletion of gold concentration near the epilayer interface perfectly demonstrates an inverse growth in carrier concentration, which holds in good concurrence with the theory of reduced compensation between Au and Boron.

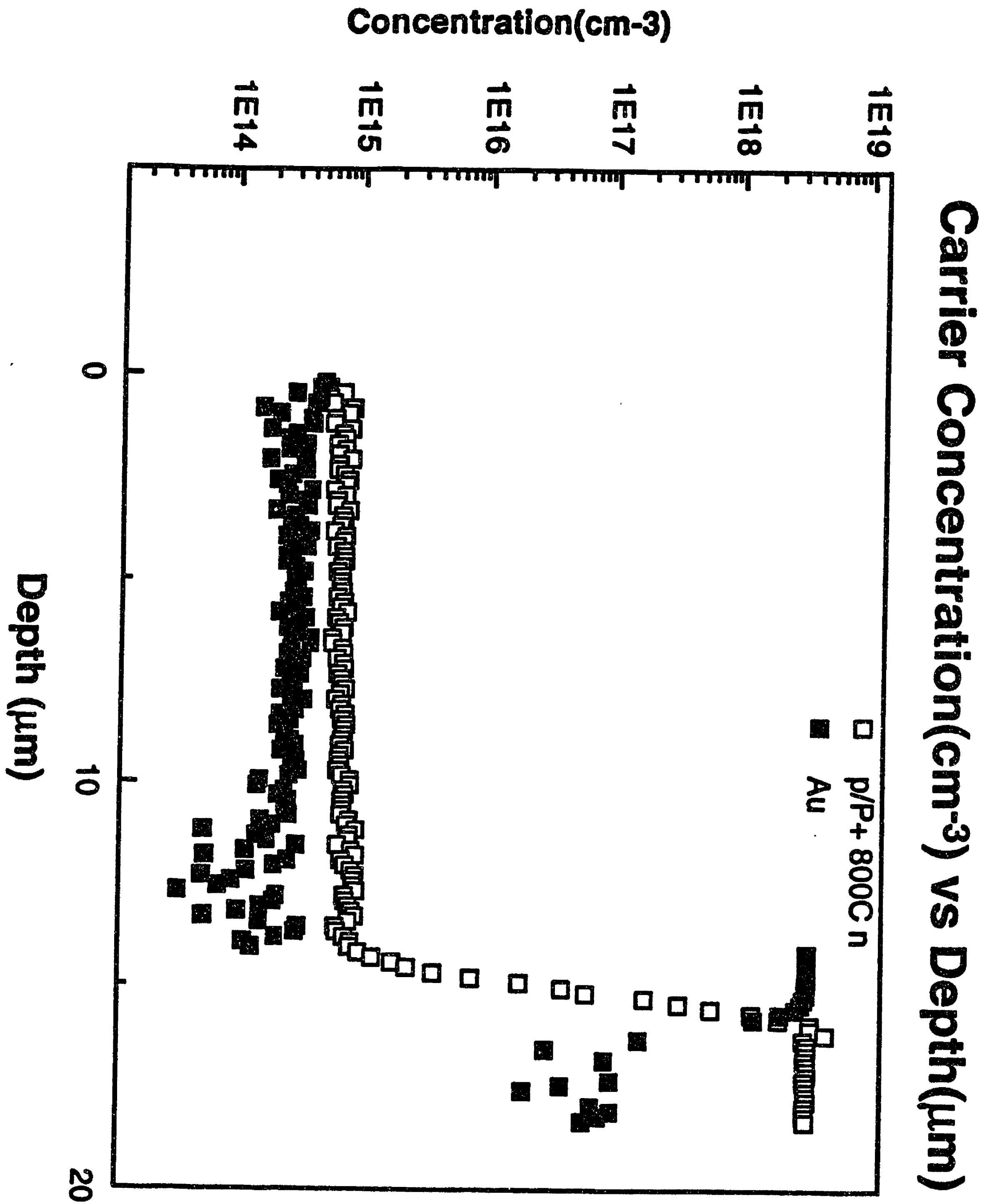


Figure 17: Carrier Concentration vs. Depth (µm) for 800°C p/p+ Silicon

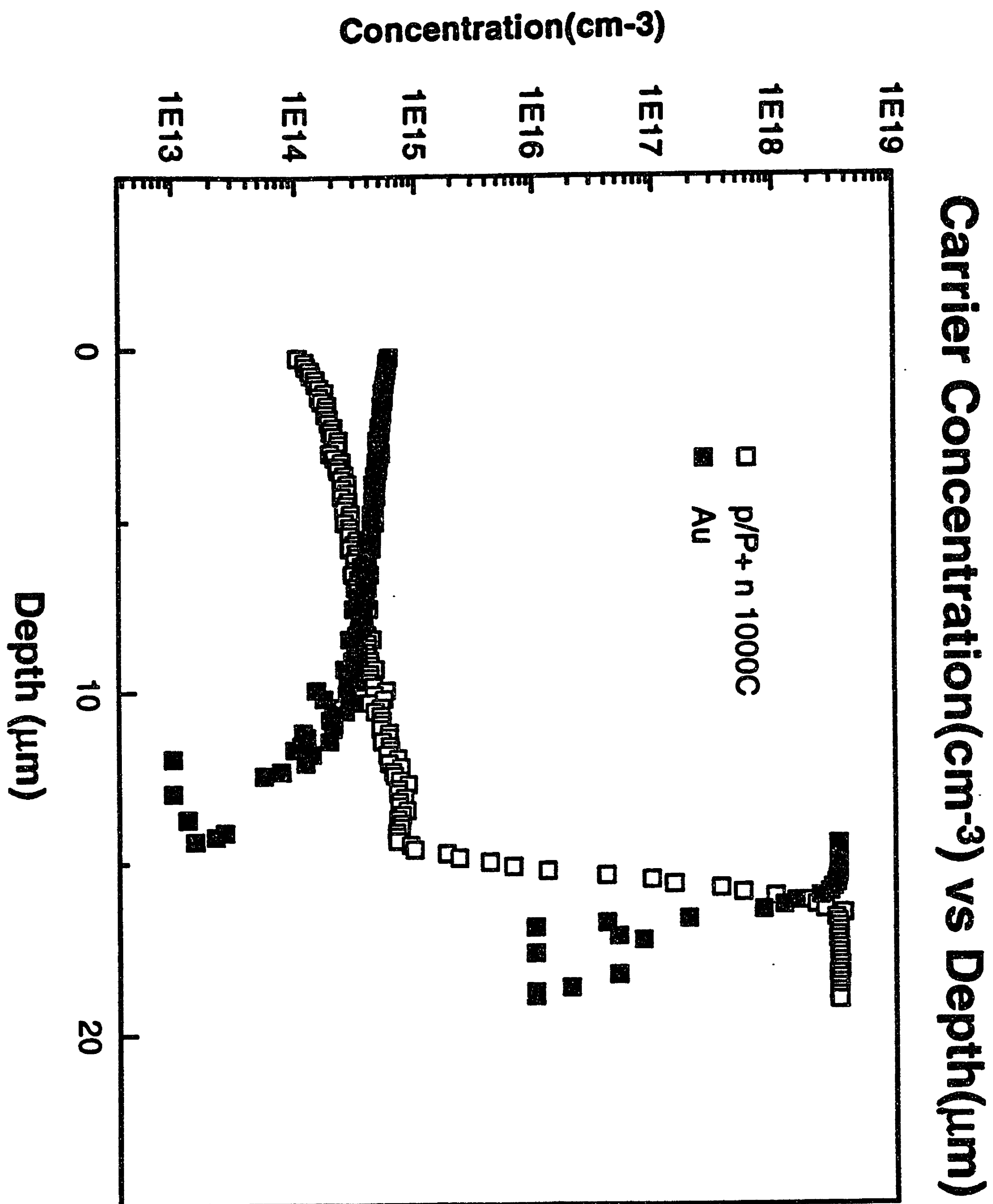


Figure 18: Carrier Concentration vs. Depth (µm) for 1000°C p/p+ Silicon

7.0 Conclusions

The presence of the p+ substrate layer in epitaxial silicon provides solubility enhancement for Au diffusion. As confirmed by samples annealed in three different temperatures (700°C, 800°C, and 1000°C) and tested by DLTS and spreading resistance measurements, a depletion of Au concentration is detected near the epilayer interface, followed by an increase in Au solubility by approximately two orders of magnitude. Concurrently, an increase in minority carrier concentration is detected due to a decrease in compensation effects. The ramification of enhanced solubility due to the mismatch of solubility limits between the p and p+ layer creates a gradient driving increased Au diffusion towards the epilayer. Once past the epilayer, diffusion immediately drops off due to limited source. This greatly contrasts with plain p samples in which the gold profile remains constant throughout

8.0 Future Considerations

What the DLTS and spreading resistance measurements provide in this project are a behavioral study of gold diffusion in epitaxial silicon. However, this experiment does not provide confident insight into the prevailing diffusion mechanism. More exploration needs to be done at the interface region. Considerations such as boron interdiffusing from the substrate into the epilayer need to be isolated from point defects influencing Au diffusion. Isolation of these different possible scenarios remain the next crucial step in this research.

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Appendix

Diffusion Approximation

Fick's 2nd Law:

$$dC/dt = D\,(d^2c/dx^2)$$

Assume case of semi-infinite solid

Solution:

$$C = C_s \,\mathrm{erfc}\,(x/2(Dt)^{1/2})$$

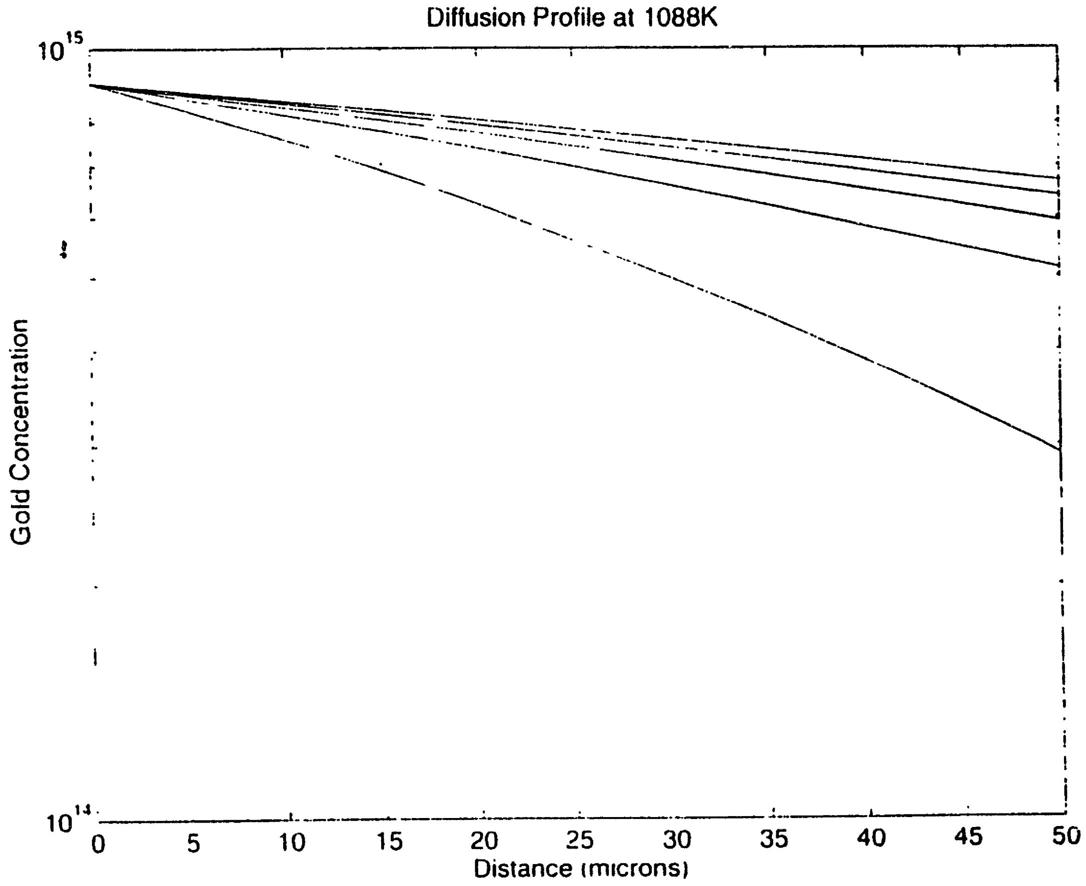
where:

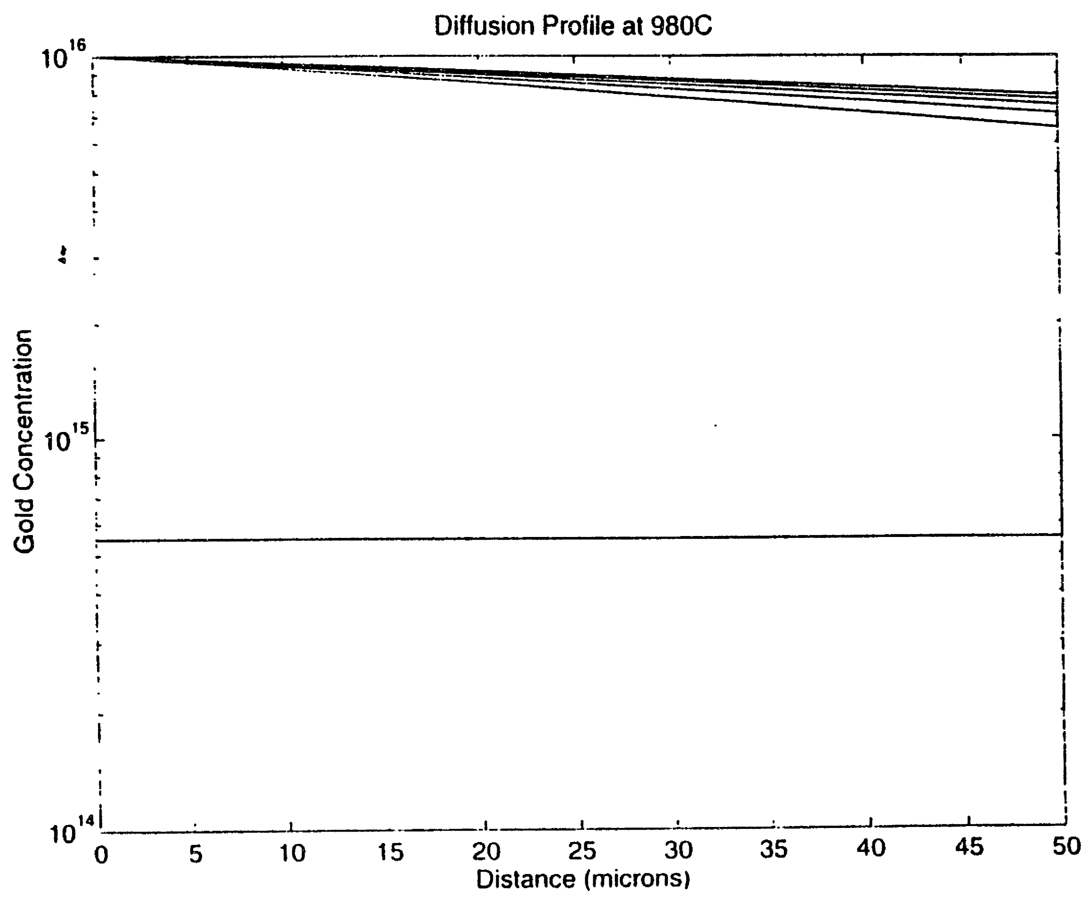
- C = concentration
- C_s = surface concentration
  - $C_{s\ T=600^oC} = 4 \times 10^{13}$
  - $C_{s\ T=1000^oC} = 1 \times 10^{16}$
  - D = Diffusivity $D_0 \exp(-E/kT)$
    - $D_0 = 1.1 \times 10^{-3}\ cm^2/s$
    - $E = 1.12\ eV$
    - k = Boltzmann Constant

x = distance = 16 μm

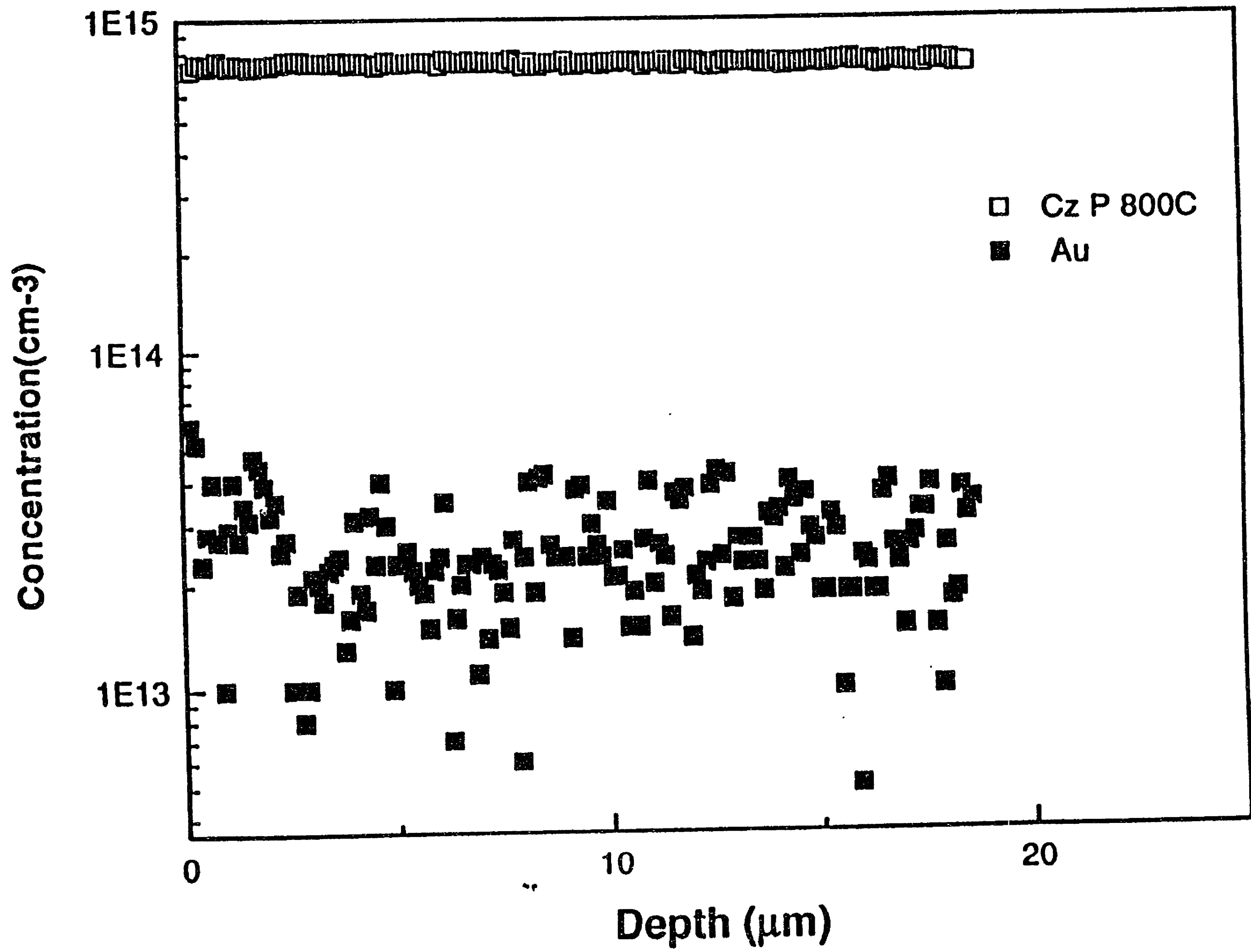
t = time = 30min intervals

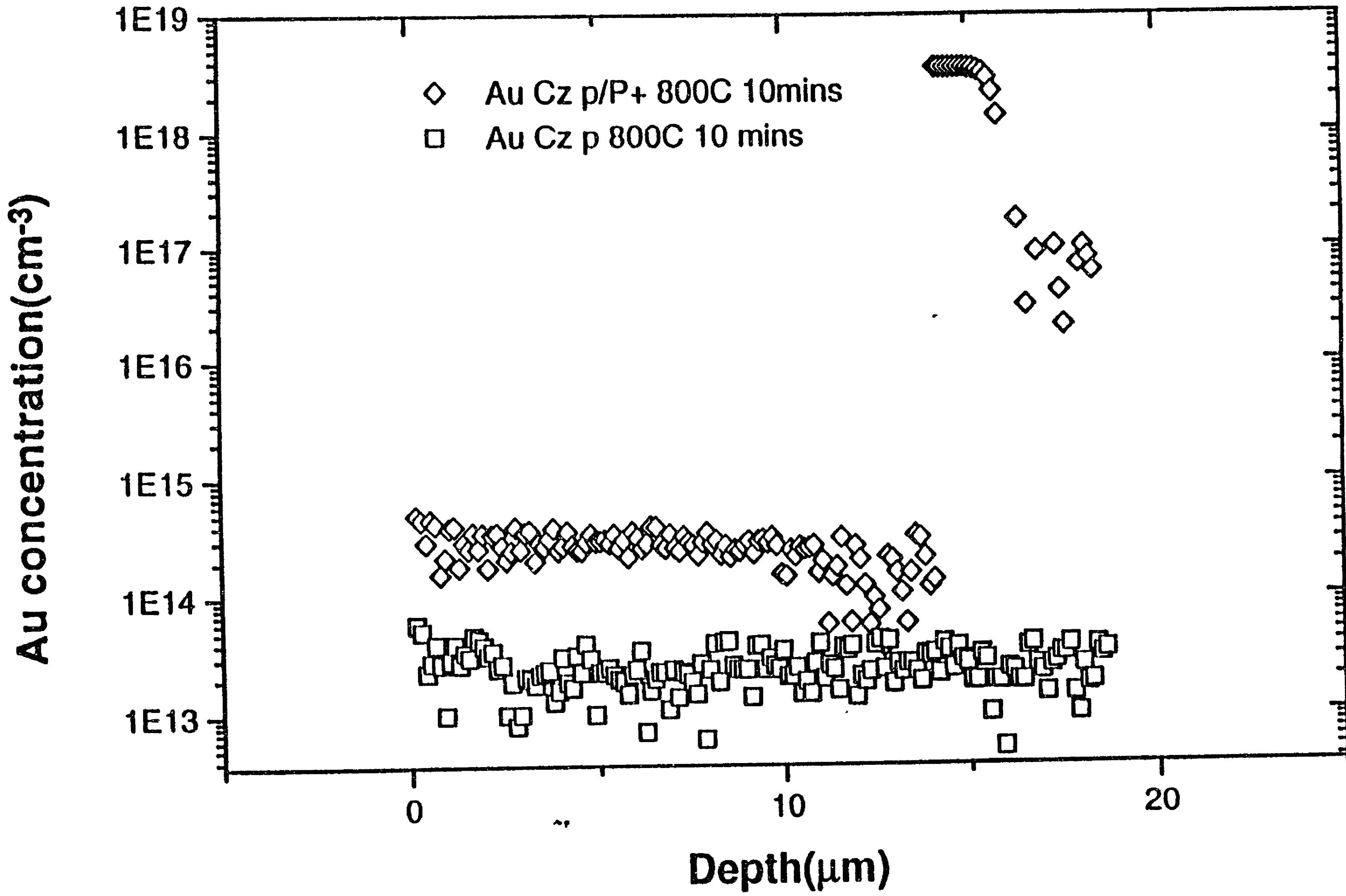
$T = 600^oC$ & 900^oC

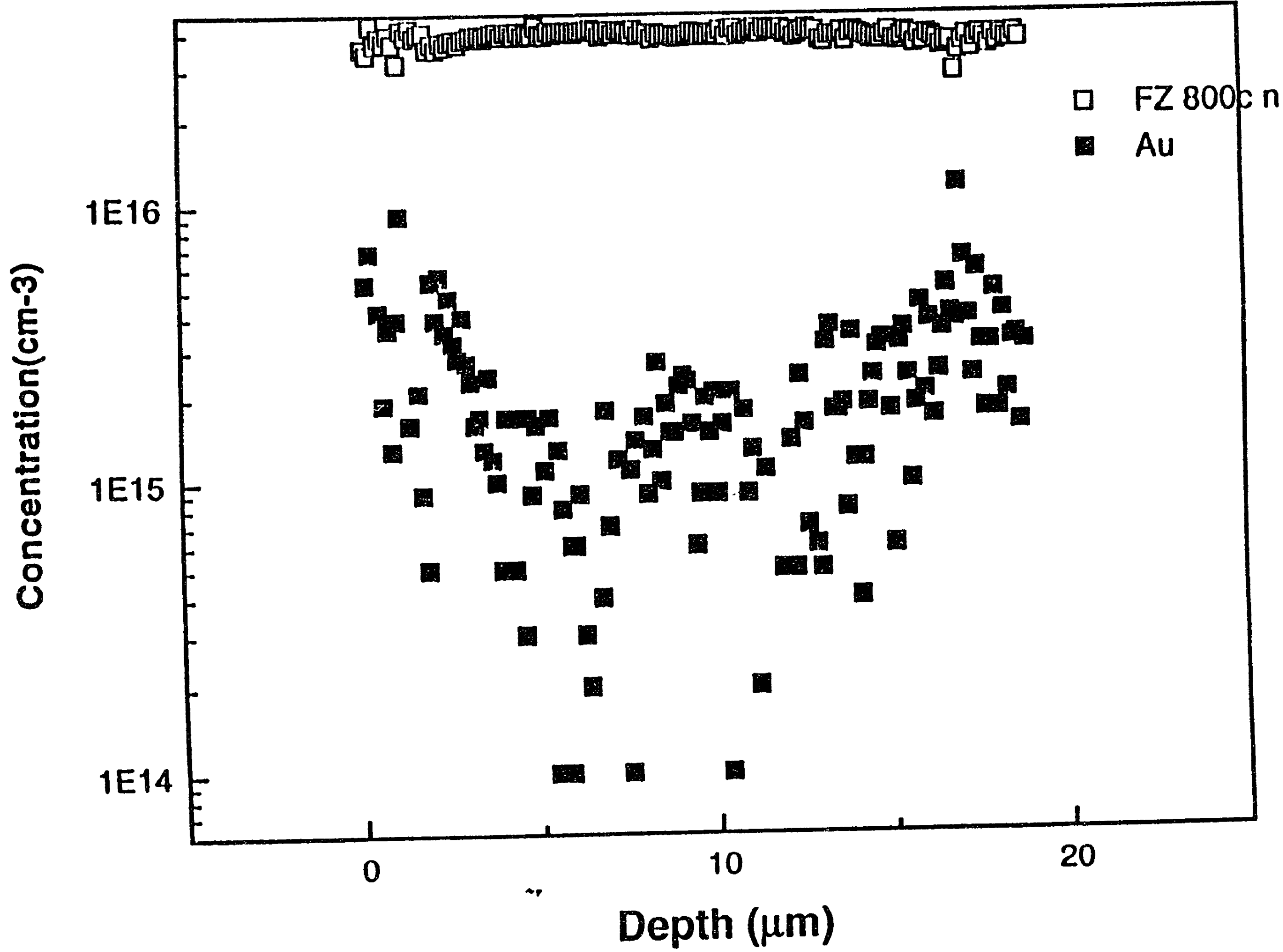

Diffusion Profile at 1088K
Gold Concentration
10^15
10^14
0
5
10
15
20
25
30
35
40
45
50
Distance (microns)



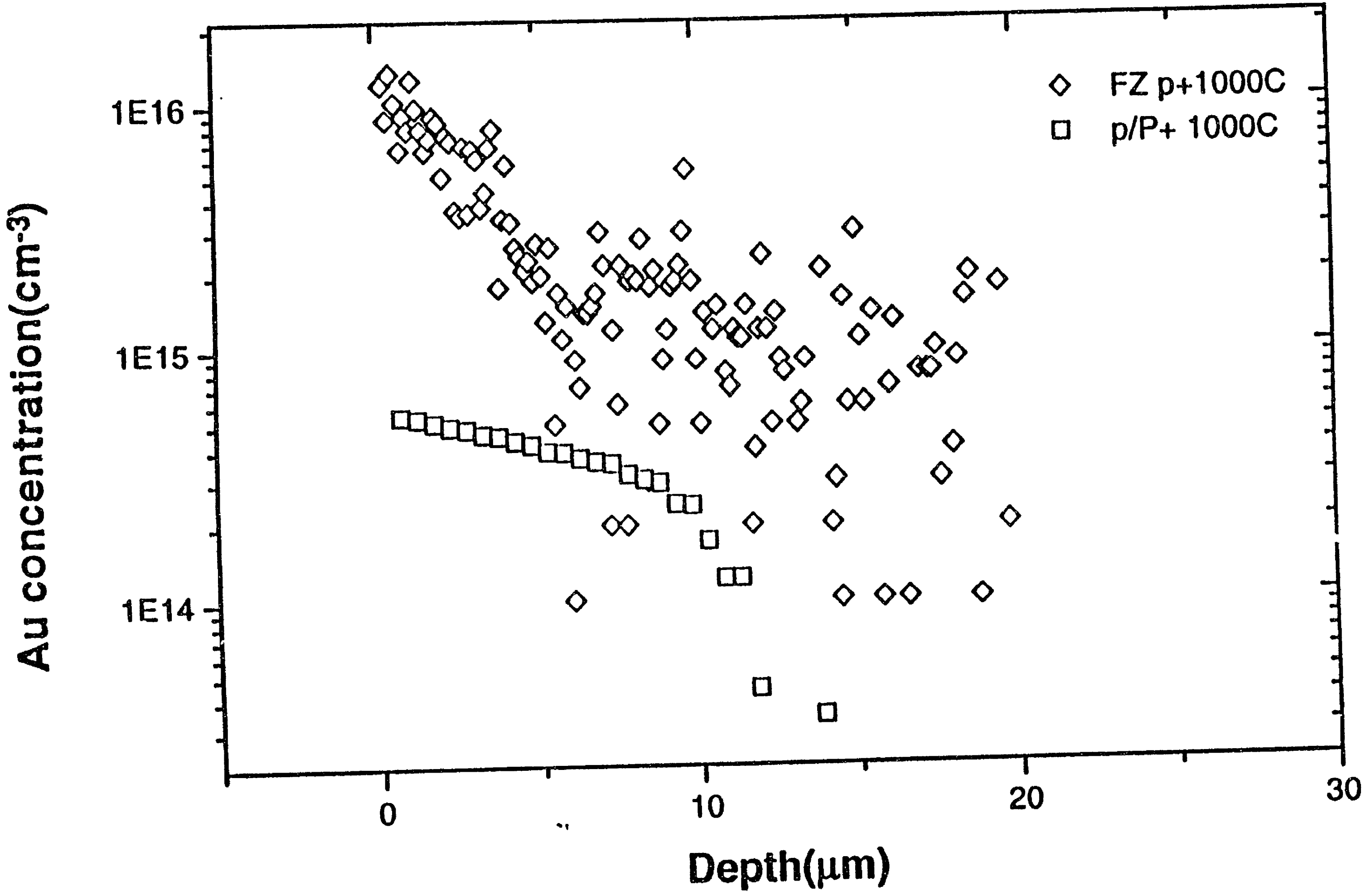
Diffusion Profile at 980C
Gold Concentration
10^16
10^15
10^14
0
5
10
15
20
25
30
35
40
45
50
Distance (microns)

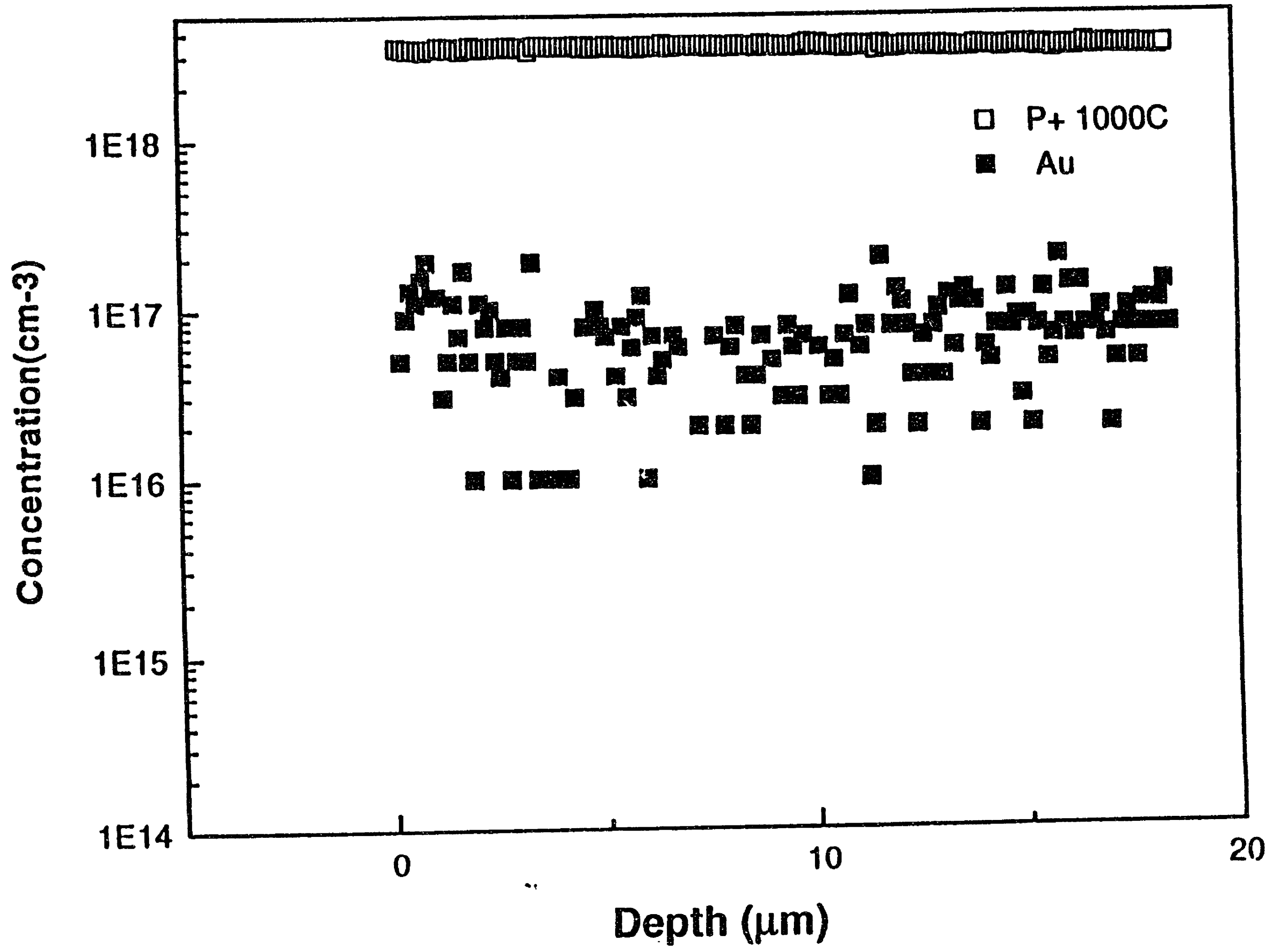

Carrier Concentration(cm-3) vs Depth(μm)
1E15
1E14
1E13
Concentration(cm-3)
Cz P 800C
Au
0
10
20
Depth (μm)

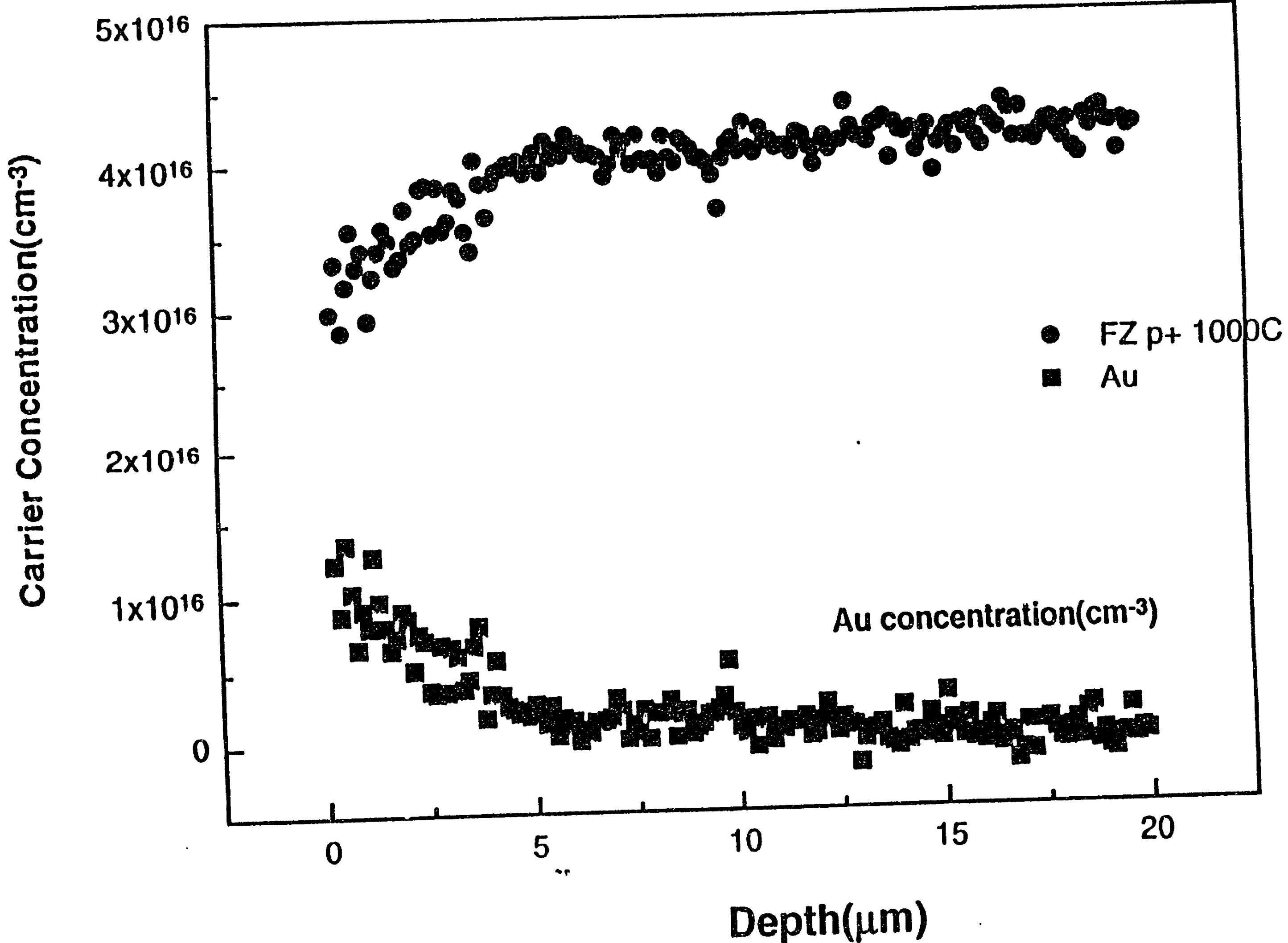

Au concentration vs Depth
Au Cz p/P+ 800C 10mins
Au Cz p 800C 10 mins
1E19
1E18
1E17
1E16
1E15
1E14
1E13
Au concentration(cm-3)
0
10
20
Depth(μm)



Carrier Concentration(cm-3) vs Depth(μm)
Concentration(cm-3)
1E16
1E15
1E14
0
10
20
Depth (μm)
FZ 800c n
Au


Au concentration vs Depth
FZ p+1000C
p/P+ 1000C
1E16
1E15
1E14
Au concentration(cm-3)
0
10
20
30
Depth(μm)


Carrier Concentration(cm-3) vs Depth(μm)
P+ 1000C
Au
Concentration(cm-3)
1E18
1E17
1E16
1E15
1E14
0
10
20
Depth (μm)


Carrier Concentration(cm-3) vs Depth(μm)
Carrier Concentration(cm-3)
5x1016
4x1016
3x1016
2x1016
1x1016
0
FZ p+ 1000C
Au
Au concentration(cm-3)
0
5
10
15
20
Depth(μm)

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