Artificial Atoms and Electron Puddles: Single and Double Barriers in a Silicon MOS System

by

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Sc.B. Mathematics/Physics
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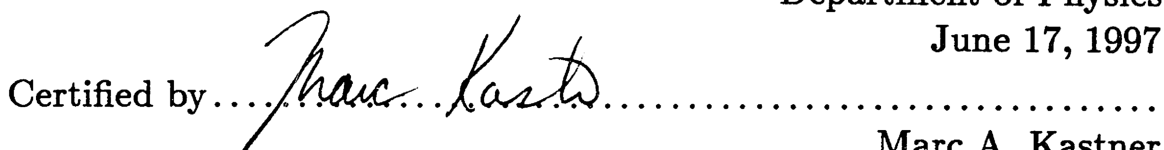

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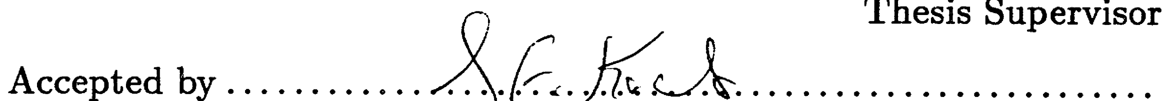

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Abstract

We have fabricated one of the first electrostatically defined double barrier artificial atoms in a Silicon Metal Oxide Semiconductor (MOS) system, and observed Coulomb blockade. Intriguingly, we have found that electrons do not simply tunnel across the individual barriers fabricated, but rather tunnel through states that exist within these barriers. Such resonances are due to the localization of electrons by fluctuations in the impurity potential in the barrier region. The separation of these resonances in gate voltage is surprisingly constant, indicating only small fluctuations in the addition energy as more electrons are trapped in the states localized in the barrier. After considering several models we conclude that we can only account for the uniform addition energy by hypothesizing that the electrons are localized in "electron puddles". With this hypothesis in mind, we interpret reports in the literature of equally spaced conductance resonances in single barriers fabricated in a variety of different material systems as evidence that these electron puddles are a general consequence of disorder. We suggest that such electron puddles form in a variety of systems near the metal-insulator transition. Using transport spectroscopy to study these electron puddles we find that some of their behavior can not be understood within a single-particle picture.

Thesis Supervisor: Marc A. Kastner
Title: Donner Professor of Physics

דְּעֶה חָכְמָה לְנַפְשֶׁךָ,
וְהִיא כֶּתֶר לְרֹאשֶׁךָ

Seek wisdom for your soul
It will be your crowning glory

Acknowledgments

The last six years have been full of exploration and discovery as well as trials and travails. I have tried to learn from all of these experiences. My many lessons have occurred in a variety of places: the lab, the cleanroom, the classroom, the office, the hallway, and at home. While this thesis focuses on the knowledge I have gathered in my studies of physics, some of the most important lessons I have learned in my time at MIT have been about myself and my relationships with others. I wish to thank all those who have helped me learn about myself and the world around me.

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Most of my time in the past years has been spent in building 13 at MIT. I have enjoyed the companionship, advice, and intellectual stimulation of many people. Among those I will miss are Tom Killian, Dale Fried, Adam Polcyn, Mike Yoo, John Perkins, Ibo Mathews, Yousef Habib, Sandra Brown, Raissa D'Souza, Mike Young, Young Lee, Barry Wells, Martin Greven, Bill Nutall, Qiang Feng, James Chen, David Berman, Ho-Ban Chan, Sven Heemeyer, Jens Siewert, and Lyndon Hicks.

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As a scientist and as a person, I see myself as one link in a chain that connects the past with the future. I would like to dedicate this thesis to those who have come before me, and those who will follow me. It is with love that I dedicate this thesis to my grandparents Sylvia Friedberg Krassner, Jerome Krassner, Morris Abusch, and Jesse Weingart Abusch, and to my uncles Lowell Krassner, Frank Talmage, and John Ebstel. I only regret that more of them could not have lived to read this dedication. It is with hope that I dedicate this thesis to my children, the first of whom just starting kicking last week.

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Chapter 1

Introduction

In the past thirty years there have been tremendous advances in the semiconductor industry resulting in the exponential growth in the complexity of modern computers. These developments have been enabled by the relentless drive to make smaller devices. The ability developed by those in the semiconductor industry to confine electrons to short length scales has enabled experimental physicists to create new structures and to explore new physical effects. In addition, new technology has allowed the fabrication of structures with unprecedented cleanliness in which electrons may travel ballistically over distances greater than $10\,\mu$ without being scattered. For example, the discovery of the fractional quantum hall effect [3] was only possible in crystals where the electrons were confined to a two-dimensional layer and in which disorder was minimized. This exciting discovery has given rise to a new subfield within condensed matter physics where theoretical and experimental developments have continued for the past fifteen years. The fractional quantum hall effect is just one example of the exciting directions in physics that have been made possible by the technological advances of the semiconductor industry.

This thesis concerns itself with two of the other subfields that have developed in tandem with semiconductor fabrication: nanostructures and mesoscopics. Mesoscopic physics is concerned with the effects that disorder has on the electronic states and on the transport properties of a system on length scales large compared with the size of atoms, but short compared with those of macroscopic samples. These effects include the localization of the electronic states in the presence of disorder and a modification of Fermi liquid theory to account for the role of electron-electron interactions in disordered systems. Mesoscopic physics is particularly interested in systems of reduced dimensionality and the behavior of electrons at short length scales; the great theoretical advances of this field even correctly predicted the surprising result that any

disorder in two dimensions will cause all the electronic states to be localized. Two very readable reviews of the development in this field can be found in reference [4] and the introduction to reference [5].

The study of nanostructures focus on the electronic states and transport properties of systems where electrons are confined spatially in one or more dimensions. The scientist can design and fabricate a device to address specific theoretical issues, for example, there ave been experimental studies of the Luttinger liquid, which describes interacting electrons in one dimension [6], the Aharonov-Bohm effect [7], the quantization of conductance [8], and the one dimensional Hubbard Hamiltonian [9]. This field is characterized by an active exchange between theory and experiment and is reviewed nicely in reference [10].

As we introduce the work in this thesis we will present the background in which our work began and the motivation for the original project. We then present the reader with a preview of what this thesis contains; as frequently happens, the most interesting results that we have found were discovered serendipitously. Finally, we give an overview of the main line of argument that will be presented in this thesis and lay down a road map to guide the reader through the document.

1.1 Background

One of the nanostructures that has been the focus of much recent study is the artificial atom [11, 12]. An artificial atom is a structure containing a fixed number of electrons that occupy quantized energy states. Artificial atoms are different from natural atoms like hydrogen and helium because their size and shape can be controlled and because they are confined in a potential that is much weaker than the $\frac{1}{r}$ potential of the nucleus. Two of the important energy scales in the artificial atom are the addition energy, U, which is required to add another electron to the atom, and the excitation energy, $\Delta\varepsilon$, which is required to excite an atom with a fixed number of particles from the ground state to an excited state. Both of these energies get larger as the device is made smaller and the electrons are confined more tightly. U grows because it is dominated by the electron-electron interaction whose magnitude increases as the electrons are forced to occupy a smaller volume, while $\Delta\varepsilon$ increases as the electronic wavefunctions are forced to occupy a smaller volume much like the energy of a particle in a box increases as the dimensions of the box decrease.

It is possible to probe artificial atoms by means of a technique known as transport spectroscopy. In this technique two leads are brought near enough to the artificial

atom so that electrons can tunnel from the leads to the states localized in the artificial atom. A voltage bias is applied between the leads and they are positioned so that direct tunneling from one lead to the other is suppressed. For a current to flow an electron must then tunnel from one lead onto the localized states in the artificial atom and then to the other lead. This will only be possible if there is a localized state on the artificial atom within $k_B T$ of the Fermi level in the leads. Thus the resolution of transport spectroscopy is limited by the temperature of the electrons in the leads.

To form an artificial atom we begin with a sheet of electrons that are confined near a semiconductor interface. By positioning gate electrodes above this sheet and biasing them negatively it is possible to expel the electrons under the gates and to confine an isolated island of electrons to a small region where there is a gap between the gates (see for example figure 2-1b). The shape and size of this artificial atom will then be determined by the shape of the gap in the gates and the separation, d, between the gates and the interface at which the electrons are trapped. As the gap in the gates is made smaller the artificial atom will be confined more tightly as long as the gap is larger than the separation d. If, on the other hand, the gap in the gate is much smaller than d the potential created by the gates will be blurred; in this case making the gap smaller will not confine the electrons more tightly. Therefore, to confine electrons to very small distances the gates must be brought as close as possible to the sheet of electrons.

The initial goal of this project was to study artificial atoms with better spectroscopic resolution. Because the resolution of transport spectroscopy is limited by the electron temperature, previous measurements were performed at the lowest accessible temperatures. We hoped to improve our *relative* spectroscopic resolution by increasing the intrinsic energy scales in an artificial atom, U and $\Delta\varepsilon$. We sought to do this by confining the electrons in an artificial atom to a smaller area; as discussed above, this required us to fabricate a device with both fine patterning of the gate that confines the electrons and a small separation, d, between the gate and the plane of the electrons.

Previous artificial atom devices had all been fabricated in GaAs/AlGaAs heterostructures [13, 14, 15] which had thick spacer layers between the gates and the sheet of electrons. Furthermore, the layer of $Al_{0.3}Ga_{0.7}As$ between the gates and the electron sheet forms a Schottky contact with the gates; therefore large leakage currents result if the gates are brought closer to the sheet of electrons so as to confine the electrons in a tighter potential. These leakages can be many orders of magnitude larger than the currents of the transport spectroscopy which we wish to study. Previ-

ous devices were fabricated with a separation of 80 nm – 100 nm, and it was believed that a large effort would be required to place the gates any closer then 35 nm [16]. Therefore, we sought to fabricate artificial atoms in a material system where a thin insulating layer is available.

The natural choice of the of a material in which to fabricate tightly confined artificial atoms is the Si/SiO_2 system.[1] SiO_2 is an excellent insulator and has very low leakage currents in layers as thin as 8 nm. Many of the early breakthrough experiments in the study of two-dimensional systems were conducted in this system [17]. Furthermore there is a whole industry that relies on making devices in the Si/SiO_2 material system from whose experience we have been able to learn. Thus it seemed natural that to make smaller devices and to improve the relative spectroscopic resolution in our studies of artificial atoms we would chose to use the Si/SiO_2 system.

In addition to the improved spectroscopic resolution, there were several other interesting physical issues which we hoped to study by fabricating artificial atoms in a Si/SiO_2 system. The band structure of electrons in this system is different from that in the more carefully studied and much simpler GaAs/AlGaAs system, with the conduction band in silicon having a two-fold valley degeneracy [18, Ch. 1]; such an additional degeneracy would certainly affect the exchange interaction among the electrons confined to an artificial atom [19]. Also the band mass of electrons is three times larger in the Si/SiO_2 system making electron-electron interaction effects more important. In addition the nature of the material systems are different which gives rise to different types and quantities of disorder.[2] The Si/SiO_2 interface is known to have lower mobilities than GaAs/AlGaAs heterostructures reflecting a higher level of disorder. While disorder is generally considered to be undesirable, it is clear from the literature dealing with mesoscopic phenomena [4] that there are many novel physical effects that can only be observed in the presence of disorder.

While there appeared to be many interesting physical questions that could be addressed by studying artificial atoms in the Si/SiO_2 system, other researchers were not actively engaged in this exploration.[3] Given this background it seemed natural

[1]The Si/SiO_2 system is also known as a silicon Metal Oxide Semiconductor (MOS) system when the device has a metallic gate, as is the case in our devices. Details of the gates and of the material system in general can be found in chapter 2.

[2]Recently a metal-insulator transition has been reported in a two-dimensional electron gas in a silicon MOS system [20]. No such observation has been reported in any other material systems. This in another example of a situation in which silicon MOS systems are different, and not just more disordered

[3]The lack of other investigations in this area in the early 1990's was due primarily the large economic expense of access to the appropriate facilities. However our collaboration with Lincoln

to undertake the fabrication and study of artificial atom at a Si/SiO_2 interface.

1.2 Preview

In this thesis we present the results of our study of nanostructures fabricated in a Si/SiO_2 system. We have successfully in accomplished our initial goal of fabricating artificial atoms, and have made the first measurements reported of electrostatically confined artificial atoms at the Si/SiO_2 interface. The devices we have made vary in size between 4 and 100 times smaller in area than the devices that have been previously fabricated using GaAs/AlGaAs heterostructures [13]. As expected, the energy scales of these devices are increased because of their smaller area. In addition to these expected results, we have found that tunneling through each of the two tunnel barriers that separates the artificial atom from its leads has unexpected structure. The textbook solution of a particle tunneling through a barrier suggests that the tunneling current should increase monotonically as the barrier is lowered. Instead we have observed that there are resonances in the tunneling conductance through a single barrier. While this structure has made it difficult to study the artificial atoms that we fabricated, its presence and properties have proven far more interesting than we could have anticipated.

This work therefore focuses on trying to understand the origin and nature of the tunneling resonances that are observed as a single electrostatically formed barrier is gradually lowered. The existence of resonances in these barriers is due to long-lived electronic states that exist within the barrier. Just as in the case of artificial atoms, we may apply the technique of transport spectroscopy to study the nature of these localized electronic states. In doing so we find that these resonances have many mysterious properties, only some of which may be understood within a simple single-particle picture. Much of this thesis is concerned with a careful study of these strange properties. Although we still do not have a complete picture of the origin of the resonances we have established that these electronic states are localized by disorder.

One of the most interesting of our findings is that the energy required to add additional electrons to the states already localized in a barrier is remarkably constant. If the localized states were due to confinement in a metallic droplet we would expect only small fluctuations in the value of U, because each additional electron is added

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Laboratory gave us the possibility to work in a leading cleanroom with the most modern equipment.

to the same metallic region. Classically the energy required to add an electron to a metal is independent of particle number and is $U = \frac{e^2}{C_\Sigma}$, where C_Σ is the total capacitance of the metallic area. The conclusion we may draw from the classical analogy is that if U does not depend on the number of confined electrons then each subsequent electron is being added to the same metallic area. Thus, the uniformity of U that we have observed brings us to the surprising conclusion that the electronic states localized by disorder consists of metallic puddles instead of individual isolated states; we term these metallic regions "electron puddles". Furthermore, by a careful review of the literature, we find evidence that these electron puddles are observed in several other material systems.

Thus we have been able to use the technique of transport spectroscopy and the tools of nanostructures to study a disordered system. In doing so we see evidence that the electronic states have an unexpected structure which greatly affects their transport characteristics.

1.3 Overview

After this introduction, this thesis begins in chapter 2 with a review of the device structure and basic physical properties of the Si/SiO_2 system. While we spent more than two years in the process of fabricating the device, the reader need not be concerned with the minutiae involved in the fabrication. However, a basic picture of the different layers and how they are patterned is essential to understanding the different experiments that are presented later in this thesis. Chapter 2 also gives the reader additional details about the properties the electrons confined at the Si/SiO_2 interface. Chapter 3 gives a detailed theoretical introduction to artificial atoms and transport spectroscopy as well as considers the behavior that would be observed in a single barrier in the absence of disorder. Finally it discusses hopping transport which has served as a longstanding model for understanding transport in disordered systems.

Having established the device structure and theoretical background, chapter 4 begins our discussion of experimental data. In this chapter we start by presenting the results of our studies of the intentionally confined artificial atoms we had originally set out to study. In presenting these data we show how the the tunneling resonances in a single barrier affect the measurements of an artificial atom. In chapter 4 we present data from a single barrier device whose behavior can be easily understood in analogy with an artificial atom. We also consider how the electronic states change as the density is increased and the states at the Fermi level become delocalized.

Chapter 5 is concerned with various models that explain the existence and properties of the electronic states localized in a barrier. It begins by presenting a review of experiments reported in the literature that have revealed resonances in single barrier devices in different material systems. It then considers the possibility that the electrons might be confined by the image charges induced in the nearby gates. After rejecting this model it considers several different ways in which the disorder potential can localize electrons. However the only model that is capable of explaining why the observed resonances have such equal values of U remains the picture of "electron puddles".

Chapter 6 is a careful experimental study of the resonances observed in a single barrier. It surveys the lineshape of the resonances, the variations in U and $\Delta\varepsilon$, and the dependence of the resonances on changes in temperature and magnetic field. Finally in chapter 7 we draw conclusions from this study. We have also included several appendices to aid anyone who wishes to reproduce or extend our experiments or analysis. Appendix A presents an outline of the detailed semiconductor fabrication process that we used to manufacture the devices. It is particularly focused on the problems we encountered in fabricating these devices, and will be valuable to anyone bold enough to attempt to repeat this fabrication process. Appendix B shows the reader the different geometries of the gates that have been used to confine electrons. It also explains the notation we have used to distinguish the various different gate patterns. Finally appendix C presents some of the mathematical formalism used in the computation of the energy of an electron in the presence of conductors discussed in chapter 5.

We have endeavored to make this thesis accessible to a variety of different readers. In particular, we have labored to present as much of the argument as possible in the figures and their captions. In addition we have limited interrupting details within the text by making extensive use of footnotes. The introduction to each chapter explains its purpose and attempts to place the material presented in that chapter in the context of the larger document. In addition, we have divided each chapter into sections and subsections that will help the reader easily understand the flow of the text. Finally we have endeavored to place a topic sentence at the beginning of each paragraph thus allowing the reader to more easily skim the material.

Chapter 2

Device Structure and Fabrication

In this chapter we describe the fabrication procedure for the devices that we have studied, and discuss their general physical properties. In describing the fabrication our purpose is not to provide as recipe, nor to describe the process in all its detail, but rather to provide the reader with the necessary information to understand the experiments that are discussed in the rest of this thesis. In section 2.1 we will present the elements of the basic structure that play key roles in our later investigations and discuss their function. In section 2.2 we focus on the physical properties of devices that we have fabricated, with particular attention to the nature of the bulk two-dimensional electron gas induced at the Si/SiO_2 interface. This discussion will furnish information essential for the interpretation of the experiments we present in later chapters.

2.1 Basic Principles and Layer Structure

The purpose of the devices that we have fabricated is to confine a small number of electrons in all three dimensions so that we can investigate how the confinement changes the nature of their electronic states. Our structure consists of a metal oxide semiconductor (MOS) structure fabricated in a silicon system. The layer structure, shown in figure 2-1a, consists of a silicon substrate, a layer of thermal oxide, lower metal gates, a second layer of oxide (CVD oxide) and an upper gate. When the one of the gates is biased above the threshold voltage, the gate attracts a layer of electrons which forms at the Si/SiO_2 interface. Stated technically, the voltage applied between the gate and the silicon substrate bends the conduction band of the silicon until it

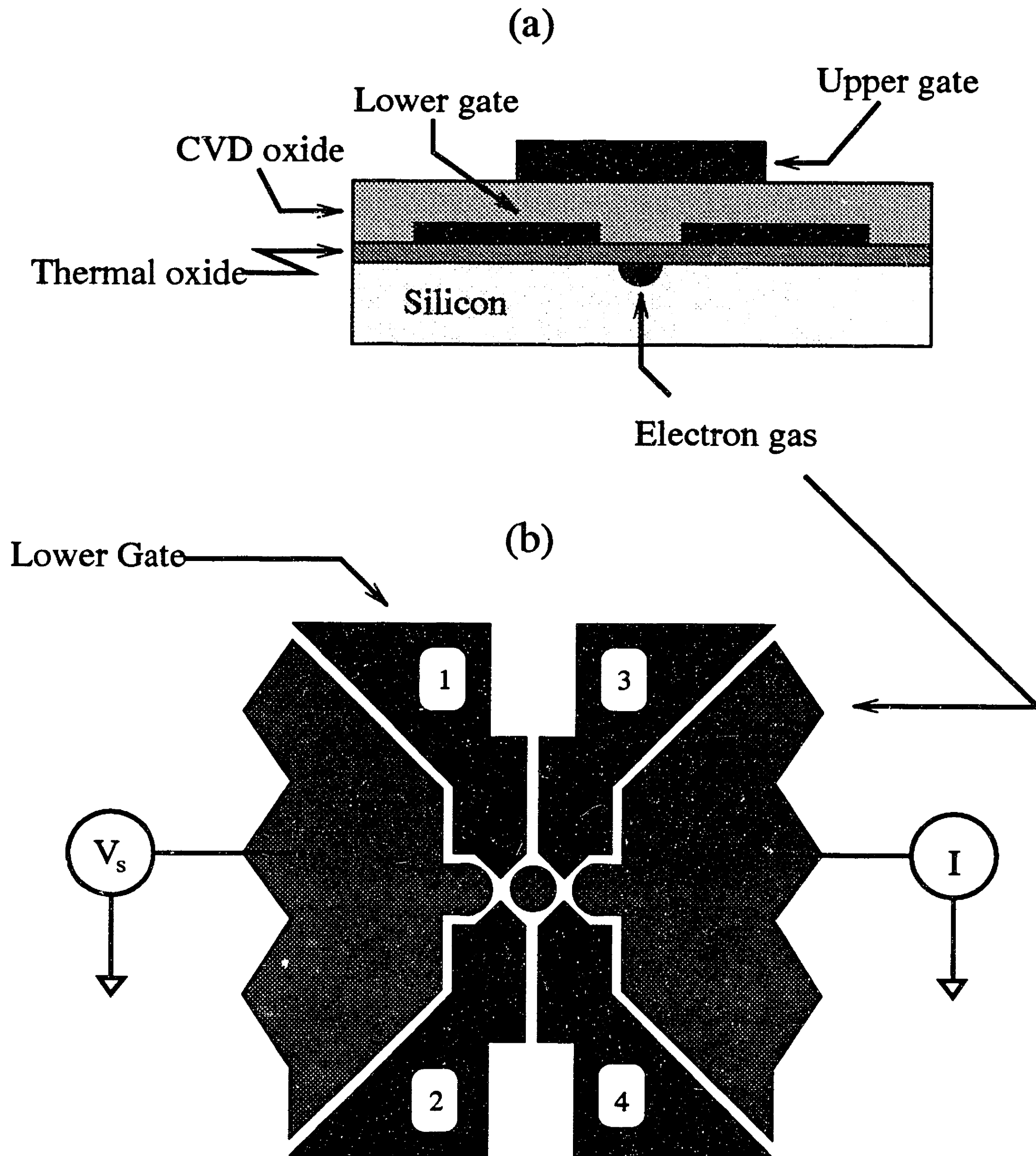

Figure 2-1: In (a) we see a schematic diagram of the layer structure in the devices that we fabricated. In a normal MOS device a two-dimensional electron gas forms at the interface between the Si/SiO_2 interface when a voltage above the inversion threshold is applied to the upper gate. In this device there is an additional gate layer known as the lower gate which is insulated from the upper gate by second layer of oxide (CVD oxide). In standard operation the upper gate is biased above the inversion threshold while a negative bias is applied to the lower gate. The regions at the Si/SiO_2 interface underneath the lower gate are depleted because of the negative voltage on the lower gate, and no electron gas forms at the interface. However in the regions where there is no lower gate the voltage applied to the upper gate is not screened, and an electron gas forms at the Si/SiO_2 surface. In this way an electron gas may be patterned. In (b) we show a top view of this device. Here the upper gate covers the whole region, and is not shown. By patterning the lower gates in the manner shown a small island of electrons may be localized and separated from the two leads. By applying a bias to the electron gas of one of the leads (the source) and measuring the current at the other (the drain) we may study the transport properties of electron island localized between the two leads. This localized island of electrons is known as an artificial atom.

crosses the Fermi level at the Si/SiO_2 surface.[1] The high density layer of electrons that forms is confined very tightly normal to the interface; while the electrons are free to move along the interface their normal motion is quantized and they can therefore be considered a two-dimensional electron gas. This electron gas in also known as an inversion layer.

The device that we have fabricated has two gate layers which allows us to pattern the two-dimensional electron gas and thereby confine electrons in all three dimensions. This is done by applying a voltage above threshold to the upper gate, while keeping the voltage on the lower metal gate below threshold. Since the voltage on the upper metal gate is screened by the lower metal gate, areas of the Si/SiO_2 interface which are covered by the lower gate will not be inverted. However, an electron gas will form in areas of the Si/SiO_2 interface which are not covered by the lower metal gate. Figure 2-1a shows a sideview of electrons being patterned in this manner. In figure 2-1b we sketch a top view of the device showing the structure of the lower gates and the electron gas (the upper gate, which is not shown, covers the whole area of this figure). In this way an island of electrons may be isolated by tunnel barriers from the bulk electron gases. Furthermore because we can independently bias each of the lower metal gates we can adjust the height of the two tunnel barriers independently. We may also chose to study each of the tunnel barriers (say that formed between gates 1 and 3) independently by biasing the other pair of gates (say 3 and 4) to a voltage above threshold; in that configuration the electron gas under the second pair of gates will allow current flow underneath as well as between this second pair of gates. This configuration is discussed in greater depth in section 4.2 (see figure 4-6 for a schematic diagram), and many of the experiments presented in this thesis are performed under these biasing conditions.

Ohmic contact are made to the two bulk electron gases shown in figure 2-1b which then serve as leads to electrically probe the isolated island of electrons. In a standard measurement a voltage is applied to one lead (the source) while the current is measured through the other lead (the drain). Since the current that can flow from source to drain depends on the electronic states of the island, studying the electronic transport properties of this system allows us to study the states of a confined electron island. This technique is called transport spectroscopy and is discussed at length in chapter 3.

We would like to confine electrons to a small area and thus require that both the

[1]For a very readable introduction to the operation of MOS devices see [21, Ch. 8].

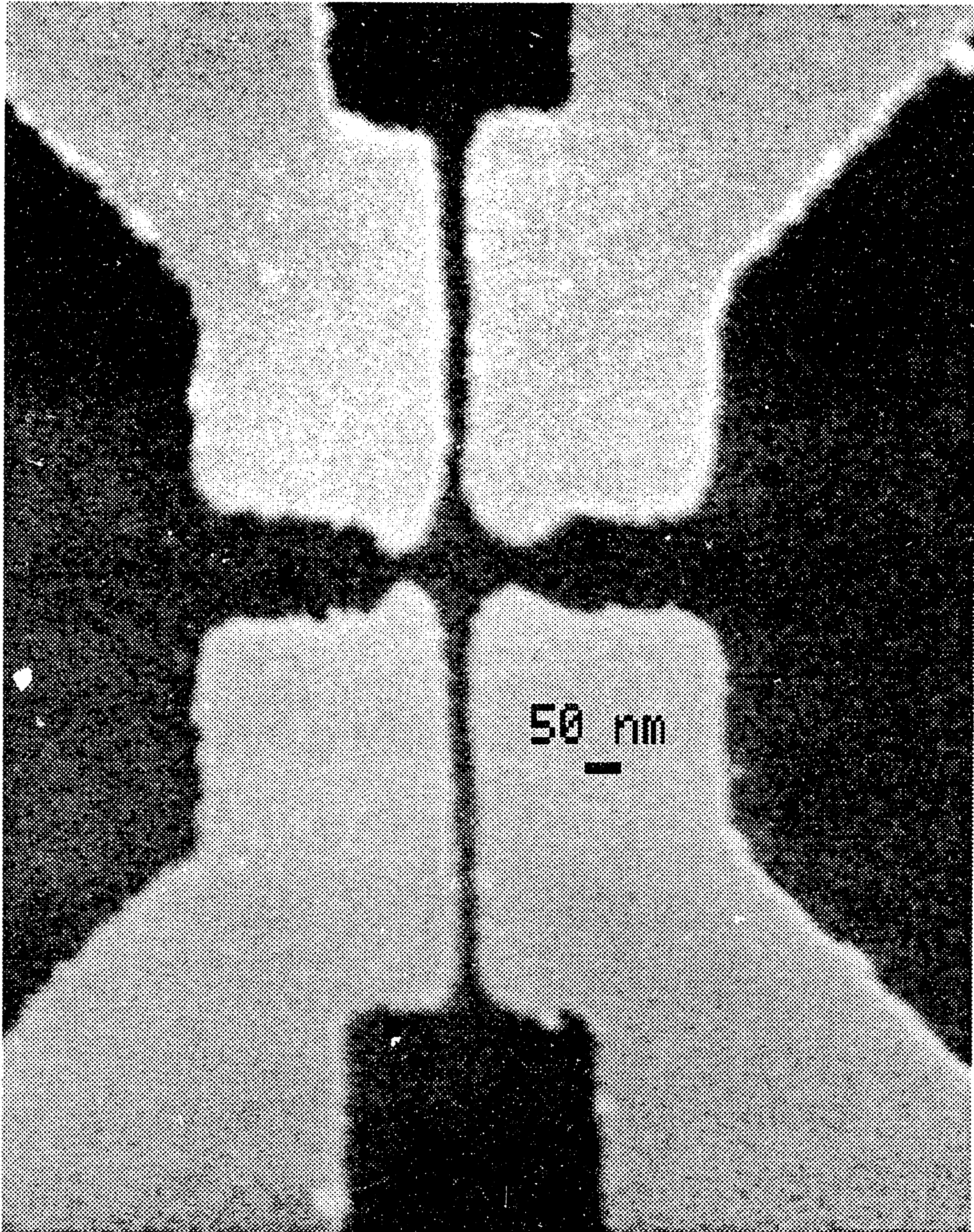

Figure 2-2: This figure shows a scanning electron micrograph of one of our lower metal gate patterns. The pattern shown here should be compared to the schematic diagram shown in figure 2-1b. The bar black bar represents a distance of 50 nm. Note that the gap between the lower metal gates is approximately 20 nm – 30 nm. Such aggressive patterning was accomplished by using electron-beam lithography.

gaps in the lower metal gate and the thermal oxide be very small. A scanning electron micrograph of a typical lower gate pattern is shown in figure 2-2. The features shown in that figure are approximately 30 nm in size and could not be patterned with optical lithography; we therefore used electron-beam lithography.[2] The size of the region of confined electrons is determined not only by the shape of the lower gates, but also by the thickness of the thermal oxide (see figure 2-1a). Since the electrons are confined by the repulsive voltage applied to the lower gates, the potential they experience will be blurred because of the separation of the lower gates from the Si/SiO_2 plane. It is because of this blurring of the potential that there are no electrons induced in the narrow regions between gates 1 and 3 or between gates 2 and 4 (figure 2-1b). For this reason it is not possible to confine the electrons to a region that is much smaller then the thickness of the thermal oxide. In previous GaAs/AlGaAs devices the spacing between the gates and the two-dimensional electron gas was 50 – 100 nm [13, 1, 2, 15] which limited previous researcher's ability to confine electrons to small areas.[3] One of the motivations for using a silicon MOS system was the excellent insulating properties of layers of SiO_2 as thin as 5 – 8 nm.

To fabricate these devices we have combined standard silicon processing with electron-beam lithography to create a unique hybrid process. We tried to minimize the time required to develop a working process by taking advantage of existing technology where possible. The main difference between the devices we fabricated and a standard MOS device was the lower gate layer; therefore most of the complications were encountered in integrating this layer into the rest of the process. In appendix A we present a detailed outline of the fabrication process with particular attention to various problems that we were forced to overcome. The reader should consult this

[2]Patterning by optical lithography is conceptually much like photography. First the surface of the wafer to be patterned is covered with a uniform coating of photoresist. Then light is passed through a "mask" which acts as the photographic negative. The exposure of the photoresist to the light induces chemical changes in the photoresist; these changes become permanent after the photoresist is developed. Then this patterned photoresist acts as a mask to transfer its pattern to the wafer below. For example, if the wafer were put in an enchant then the photoresist would protect the surface only where it was present, and the wafer would be etched in the pattern of the photoresist. A simple explanation of basic silicon processing can be found in [21, Ch. 2]. Electron-beam lithography works similarly, though no mask is required since the beam can be directed to expose any pattern desired. In our process the lower metal gates were patterned with a single layer of PMMA photoresist using a 25 KeV electron beam. The pattern was transferred to lower gate metal by a standard liftoff process. A nice discussion of electron-beam lithography and liftoff is given in Ethan Foxman's thesis [22, p. 38]. Further details of how we patterned the lower metal gates are given in appendix A.

[3]Recently advances have been made in fabricating GaAs/AsGaAs heterostructures where the electron gas is 15 – 20 nm deep [23].

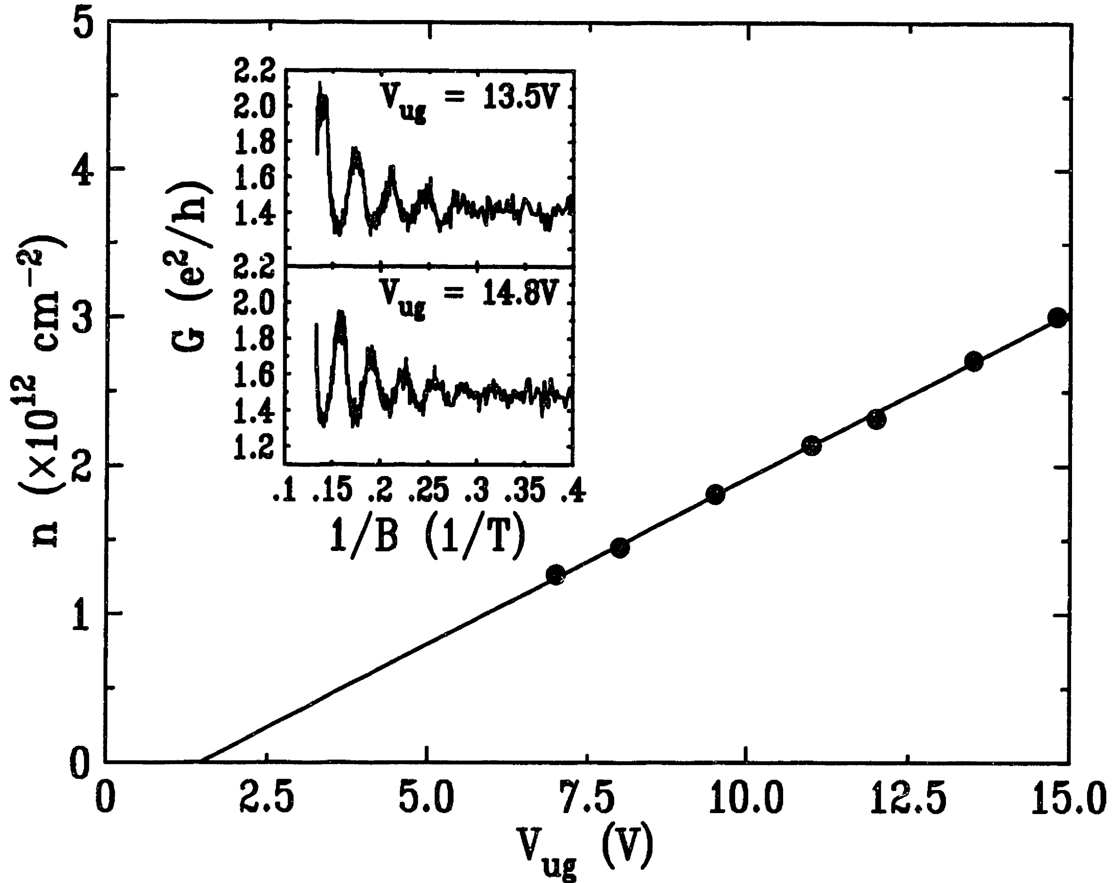

Figure 2-3: This figure plots the areal density of the two-dimensional electron gas as a function of gate voltage. The Shubnikov-de Haas oscillations are shown in the inset for two different values of gate voltage. From their period the density can be determined; this density is plotted in the black points in the main figure. The line is a fit to the points and yields $n = 2.18 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{V}^{-1} \times (V_{ug} - 1.2\,\mathrm{V})$. The values of capacitance and threshold voltage obtained from this fit agree to within 1% with the values computed from basic quantities and discussed in the text. Data taken at $T \approx .1\,\mathrm{K}$, $V_l = +2.2\,\mathrm{V}$, $V_r = +2.2\,\mathrm{V}$, device B40 and B41 wafer #13, which together consist of 14 squares.

appendix for more details.

2.2 Physical Properties of Devices

We begin our discussion of the physical properties of the MOS structures that we have fabricated by computing the threshold voltage for the formation of an electron gas underneath the gates. Using the depletion approximation we find that the Fermi level will cross the conduction band edge at the Si/SiO_2 surface[4] when a voltage

[4] In calculating the threshold voltage we follow reference [21, p. 418]. This calculation is for $T = 0$ using the depletion approximation assuming that the Fermi level in the bulk was pinned in the acceptor level .045 eV above the valence band edge. We have used a doping density of

of $V_{ug} = 1.2\,\mathrm{V}$ is applied to the Al upper gate; we call this voltage the upper gate threshold voltage, V_{ug}^{th}. Performing a similar calculation for the Cr lower gate we find[5] the lower gate threshold voltage is $V_{lg}^{th} = .7\,\mathrm{V}$. These values do not include any fixed spatial charge which may act to shift the threshold. In addition we may calculate the expected capacitance between the gates and the electron gas: for the top gate $C_{\mathrm{Al}} = 34.5 \times 10^{-9}\,\mathrm{F\,cm^{-2}}$ assuming an oxide thickness of $t_{ox}^{\mathrm{Al}} = 100\,\mathrm{nm}$, while for the lower gate $C_{\mathrm{Cr}} = 173 \times 10^{-9}\,\mathrm{F\,cm^{-2}}$ assuming an oxide thickness of $t_{ox}^{\mathrm{Al}} = 20\,\mathrm{nm}$.

To obtain the experimental values for threshold and capacitance we measure the density of the two-dimensional electron gas using the Shubnikov-de Haas oscillations of the conductivity.[6] The black points in figure 2-3 shows the electron density as a function of upper gate voltage obtained from the period of the Shubnikov-de Haas oscillations. The line in that figure is a fit to the points, while the insets show the Shubnikov-de Haas oscillations. From the slope of this line[7] we obtain $\frac{dn}{dV_{ug}} = 2.18 \times 10^{11}\,\mathrm{cm^{-2}\,V^{-1}}$, while the value of threshold obtained from the fit is $V_{th}^{\mathrm{Al}} = 1.2\,\mathrm{V}$. From $\frac{dn}{dV_{ug}}$ we obtain a value of the capacitance between the Al upper gate and electron gas of $C_{\mathrm{Al}} = 34.9 \times 10^{-9}\,\mathrm{F\,cm^{-2}}$. All of these numbers differ by less than 1% from the calculated values discussed above. In figure 2-4 we show how the magnetic field changes the conductivity as a function of gate voltage, and show weak localization corrections to the conductivity at low densities.

If we measure the conductivity of the bulk two-dimensional electron gas we find that it increases linearly with density only over a limited range of gate voltage (figure 2-5). The Drude model of conductivity [24] predicts that that the conductivity will be linearly dependent on density and therefore linearly dependent on gate voltage, $\sigma = nev = n\frac{e^2\tau}{m^*}$ and that $\mu = ev = \frac{e^2\tau}{m^*}$ where σ is the conductivity, μ is the mobility, τ is the electron scattering time, m^* is the band mass of the electron, and v is the drift velocity of the electrons. At the lowest measurement temperatures of $T \approx .1\,\mathrm{K}$ the conductivity is linear in density over a narrow range $3.5\,\mathrm{V} < V_{ug} < 5\,\mathrm{V}$.

$N_a = 2 \times 10^{15}\,\mathrm{cm^{-3}}$ which corresponds to a bulk resistivity of $\approx 8\,\Omega\,\mathrm{cm}$, and assumed that the thickness of oxide $t_{ox}^{\mathrm{Al}} = 100\,\mathrm{nm}$. For the other physical constants we have used the aluminum work function $\Phi_{\mathrm{Al}} = 4.1\,\mathrm{eV}$, the electron affinity for silicon $X_{\mathrm{Si}} = 4.05\,\mathrm{eV}$, and the Fermi energy in the bulk with respect to the conduction band edge $E_f = -1.13\,\mathrm{eV}$. We found the depletion depth to be $x_d = 1.2\,\mu$.

[5]In this calculation we used $t_{ox}^{\mathrm{Cr}} = 20\,\mathrm{nm}$ for the thickness of the oxide, and $\Phi_{\mathrm{Cr}} = 4.5\,\mathrm{eV}$.

[6]The quantization of an electron gas into Landau levels makes the density-of-states discrete and causes oscillations in the conductivity. These oscillations are known by the name Shubnikov-de Haas; their period in $\frac{1}{B}$ is proportional to the inverse of density [24].

[7]The period of the Shubnikov-de Haas oscillations is proportional to the degeneracy of the electronic wavefunctions. We have used the standard value for silicon of $g = 4$ which is due to the spin and valley degeneracies.

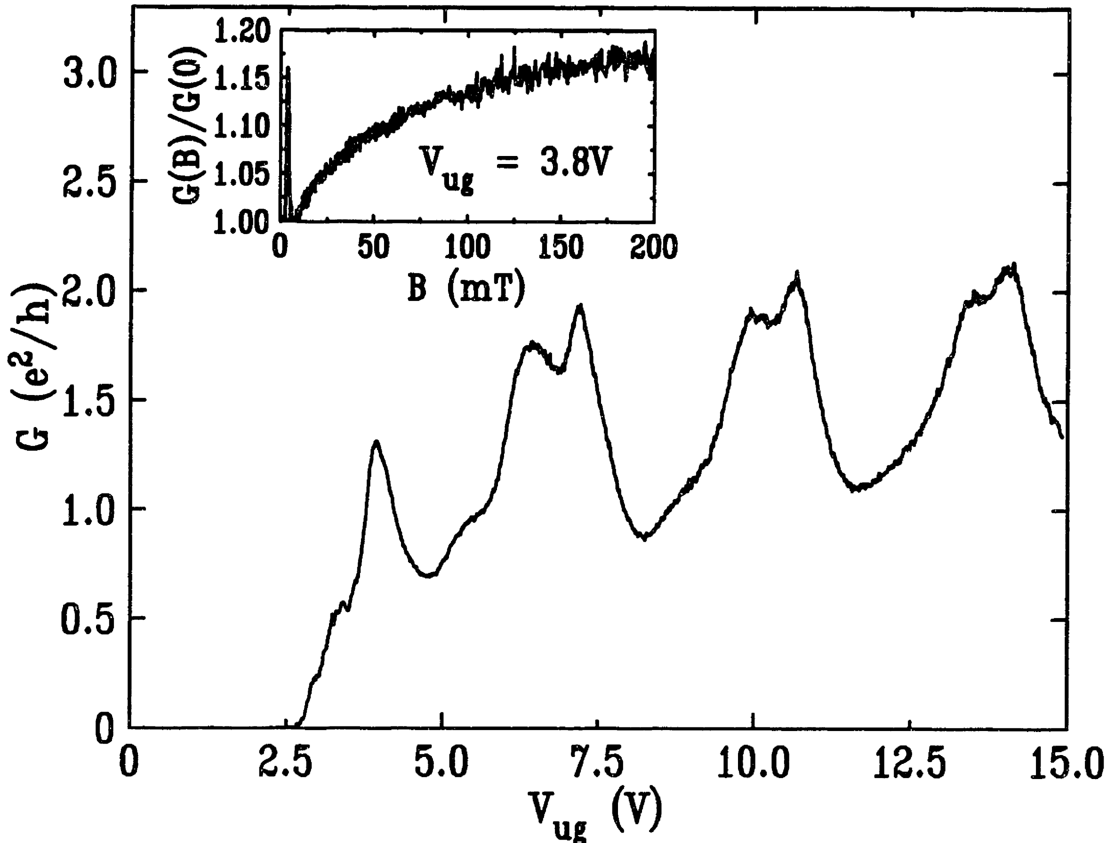

Figure 2-4: This figure shows how the conductance of the bulk two-dimensional electron gas changes in a magnetic field. The main figure shows the Shubnikov-de Haas oscillations periodic in electron density at a field of $B = 7.52\,\mathrm{T}$. The period of $V_{ug} = 3.3\,\mathrm{V}$ corresponds to the main oscillations, while at gate voltages $V_{ug} \approx 7\,\mathrm{V}$ we are able to resolve the spin splitting of the oscillations. The inset shows the conductance as a function of magnetic field in the low field regime. The positive magnetoconductance observed is due to the destruction of weak localization by the magnetic field. This trace shown was taken at $n = 5.6 \times 10^{11}\,\mathrm{cm}^{-2}$; at higher densities the weak localization feature is destroyed at a smaller magnetic field. The nature of the peak near $B = 0$ is not known. It appears in both up and down sweeps but not at higher electron density. It may be due to faulty equipment which causes sudden changes in the field near $B = 0$, and therefore electron heating. Data taken at $T \approx .1\,\mathrm{K}$, in device B40 and B41 wafer #13, which together consist of 14 squares. In the main figure $V_l = +2.2\,\mathrm{V}$, $V_r = +2.2\,\mathrm{V}$, while in the inset $V_l = +1.0\,\mathrm{V}$, $V_r = +1.0\,\mathrm{V}$, $V_{ug} = 3.8\,\mathrm{V}$.

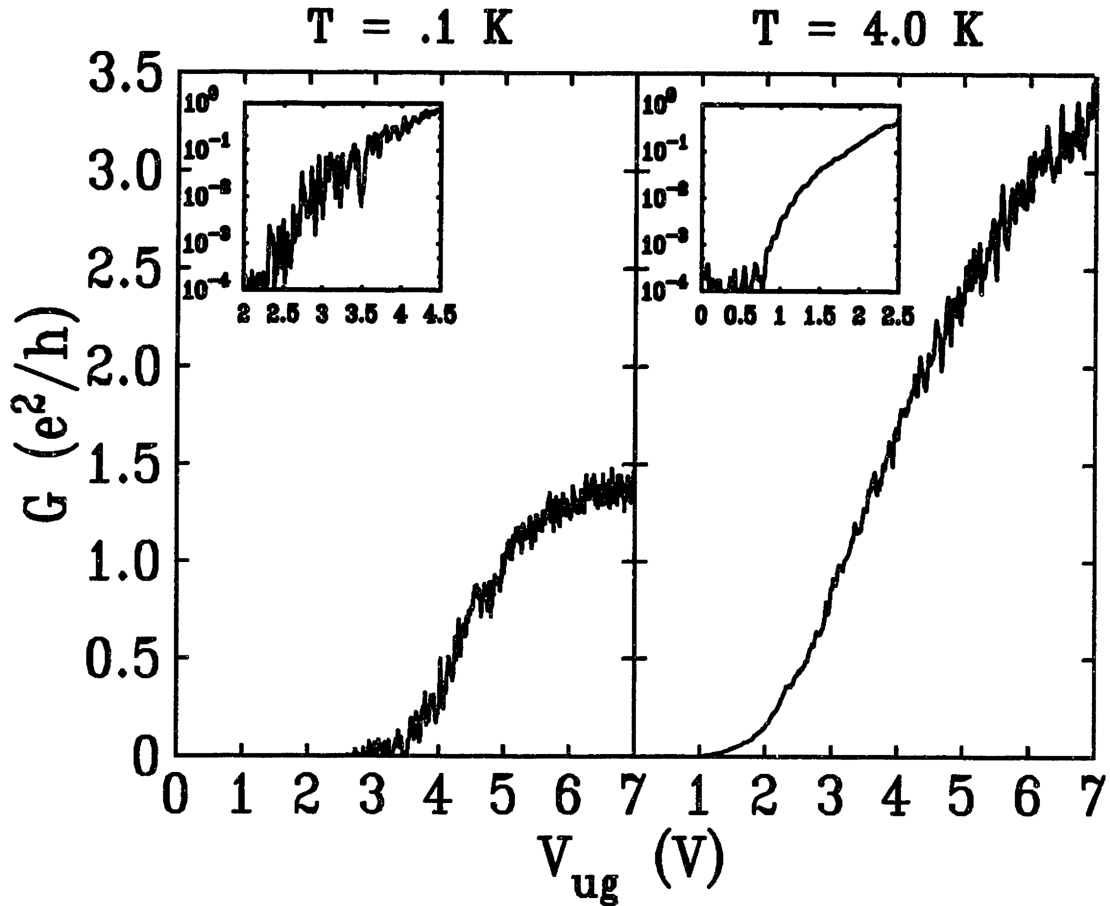

Figure 2-5: This plots shows how conductivity of the bulk two-dimensional electron gas changes with gate voltage. At $T = .1\,\mathrm{K}$ the conductivity increases linearly with gate voltage only over a narrow range of gate voltages, $3.5\,\mathrm{V} < V_{ug} < 5\,\mathrm{V}$. Below this gate voltage range the disorder prevents conduction despite a density of $n \approx 4 \times 10^{11}\,\mathrm{cm}^{-2}$, while at high gate voltages a contact resistance in series with the device limits the conductance. Both these effects are mitigated as the temperature is increased, as can be seen in the plot at $T = 4.0\,\mathrm{K}$. The inset in each plot shows the conductivity on a semilog scale. The fluctuations in the conductivity seen in the inset are repeatable. Data taken with $V_l = +3.0\,\mathrm{V}$, $V_r = +3.0\,\mathrm{V}$, device G20 wafer #7 which is consists of approximately 7 squares. The measurement temperature is noted in each panel.

Name	Symbol	quantity	units
sheet density	n	$2.18 \times 10^{11} \times (V_{ug} - V_{ug}^{th})$	$\mathrm{cm}^{-2} V^{-1}$
upper gate threshold voltage	V_{ug}^{th}	1.2	V
lower gate threshold voltage	V_{lg}^{th}	.7	V
mobility	μ	5.6×10^3	$\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{sec}^{-1}$
Fermi energy	E_f	$1.36 \times (V_{ug} - V_{ug}^{th})$	$\mathrm{meV\,V}^{-1}$
Fermi wavelength	λ_f	$\frac{76}{\sqrt{V_{ug}-V_{ug}^{th}}}$	nm
mean electron separation	r_s	$\frac{12}{\sqrt{V_{ug}-V_{ug}^{th}}}$	nm
mean free path	l	$30 \times \sqrt{V_{ug} - V_{ug}^{th}}$	nm
scattering time	τ	6×10^{-13}	sec
Fermi velocity	v_f	$5 \times 10^4 \times \sqrt{V_{ug} - V_{ug}^{th}}$	$\mathrm{m\,sec}^{-1}$
lower gate oxide thickness	t_{ox}^{Cr}	20	nm
upper gate oxide thickness	t_{ox}^{Al}	1:)0	nm
capacitance to upper gate	C_{Al}	34.9×10^{-9}	$\mathrm{F\,cm}^{-2}$
capacitance to lower gate	C_{Cr}	173×10^{-9}	$\mathrm{F\,cm}^{-2}$
breakdown field of SiO_2		$\approx 10^7$	$\mathrm{V\,sec}^{-1}$
fixed charge density in SiO_2		$\approx 5 \times 10^{10}$	cm^{-2}

Table 2.1: This table lists the important physical parameters for the devices that we have studied. It assumes that the oxide is 20 nm thick, which is the case for all the devices presented in this thesis. It is compiled using values and formula obtained from reference [10, p. 7] and [18].

As the gate voltage is decreased the conductivity vanishes despite the finite density of electrons because of the effects of disorder. In figure 2-5 the conductivity vanishes[8] at $n \approx 4 \times 10^{11}\ \mathrm{cm}^{-2}$ when $T = .1\,\mathrm{K}$, while when $T = 4.0\,\mathrm{K}$ the conductivity vanishes at $n \approx 2 \times 10^{11}$; these number are consistent with the findings of others [25]. Because the conductivity is limited by disorder, the greater the available thermal energy the lower the density at which conductivity is possible.

At higher densities the series resistance of the ohmic contacts exceeds the resistance of the electron gas, and the total conductivity saturates. This can be seen when $V_{ug} > 6\,\mathrm{V}$ in figure 2-5 at $T = .1\,\mathrm{K}$. We test this hypothesis by measuring a sample where the electron gas region is has a different aspect ratio. While the conductivity, σ, of the electron gas depends only on density, the conductance depends on the geometry of the sample, $G = \frac{W}{L}\sigma$, where W is the width of the sample and L is it length; we characterize the geometry by the number of squares $\frac{L}{W}$. When we measure a device with the same width but twice the length we find that the conductance saturates at the same value indicating that this high gate voltage saturation is due to a contact

[8]We fit $G(V_{ug})$ to a line over the region where it varies linearly. We then define the conductivity threshold as the value of density at which the linear fit predicts $G = 0$.

resistance and not to an intrinsic property of the electron gas. We also find that the contact resistance decreases with increasing temperature[9] as shown in figure 2-5.

Based on the measurements shown in figure 2-5 we may compute the mobility of electrons in the two-dimensional electron gas. We measure $\frac{dG}{dV_{ug}}$ in the region where the conductivity increases linearly with gate voltage. Since $n = C_{Al}(V_{ug} - 1.2\,\mathrm{V})$ we may write the mobility as

$$\mu = \frac{d\sigma}{dn} = \frac{L}{W}\frac{1}{C_{Al}}\frac{dG}{dV_{ug}} \tag{2.1}$$

where we have used the notation discussed above. We find that $\mu = 5.6\times10^3\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ which reasonable for this system, though lower than the value of $\mu = 20\times10^3\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ reported by Scott-Thomas [26], or by Kravchenko *et al.* [20].

We summarize the important physical information about the two dimensional electron gas and the Si/SiO_2 interface in table 2.1.

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[9]The ohmic contacts are formed by a very heavy implant of P atoms into the silicon. These dopant atoms act as impurities and provide carriers at room temperature. At lower temperatures these impurities can freeze out. However if the doping level is high enough than the impurity states form a band and there will be conduction even at $T = 0$. We believe that our doping levels and the disorder of the dopants in the ohmic contact region contribute to the contact resistance. Thus we observe a decease in the contact resistance as the temperature is increased.

Chapter 3

Physical Expectations

In this chapter we will discuss a variety of systems which have been previously studied in some depth. We review these systems because they are some of the important models we believe to be relevant to our work. While the devices we study are different from each one of the systems reviewed in this chapter, we will frequently be comparing the behavior of our devices to these model systems. Emphasis is placed on conveying a basic physical picture of each of these model systems with a focus on the properties that are relevant to the type of experiments we perform.

We begin with a review of artificial atoms and then proceed to a review of transport through an electrostatically defined barrier, and hopping transport. Many important and general concepts are presented in the section on artificial atoms; while these concepts apply to the study of artificial atoms they are more general, and thus the section on artificial atoms serves also as an introduction.

3.1 Artificial Atoms

Using modern fabrication techniques it is possible to isolate a fixed number of electrons in a small area coupled to two leads by tunnel barriers. One way in which this can be accomplished is by electrostatic depletion of a two-dimensional electron gas; the details of how this can be done in a silicon MOS system have been discussed in chapter 2 (see figure 2-1). Such an island of electrons will have a fixed number of electrons occupying quantized energy levels. We call these structures artificial atoms because the analogy with "natural" atoms is quite fruitful.

We can study the electronic states of an artificial atom by studying its transport properties. To do this we apply a voltage to one lead and measure the current through the other (see figure 3-1). Because tunneling is suppressed exponentially

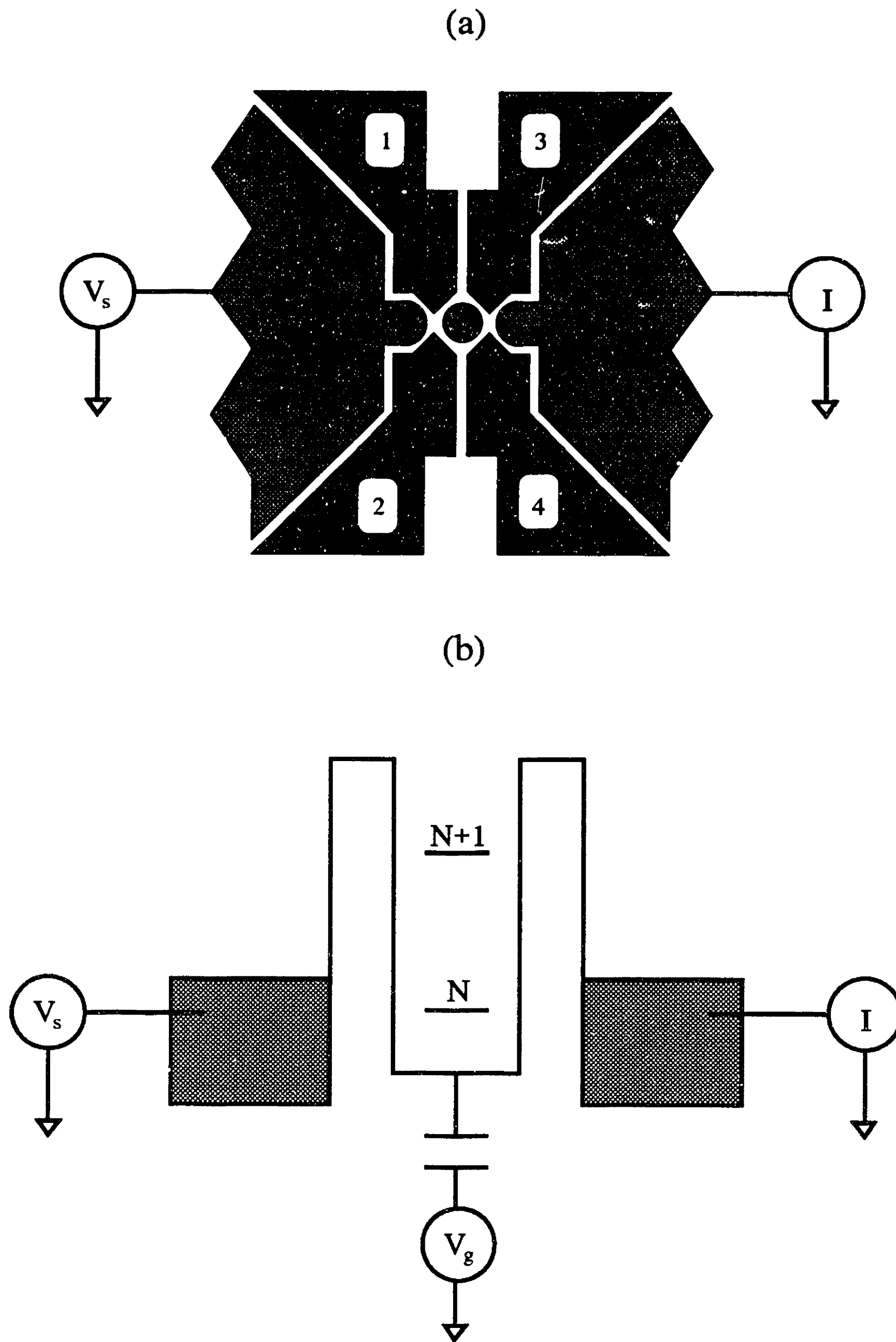

Figure 3-1: Figure (a) show the gate patterns that we have fabricated to confine electrons in an isolated region known as an artificial atom. The upper gate covers the whole region shown in (a); for details see figure 2-1. In the bottom panel (b) we see a schematic band diagram for the device structure shown in the top panel. The tunnel barriers isolate a small region of localized states from the electron gases in the source and drain. In a typical conductance measurement a small bias, V_s, is applied to the source and the current is measured at the drain. The energy of the localized states in the artificial atom can be adjusted by the capacitive coupling to a gate with voltage V_g. In our device this gate is typically the upper gate, though the states of the artificial atom are also capacitively coupled to the lower gates. We have labeled the available states on the artificial atom by the number of electrons that are localized. Figure 3-2 shows in more detail the states of the artificial atom.

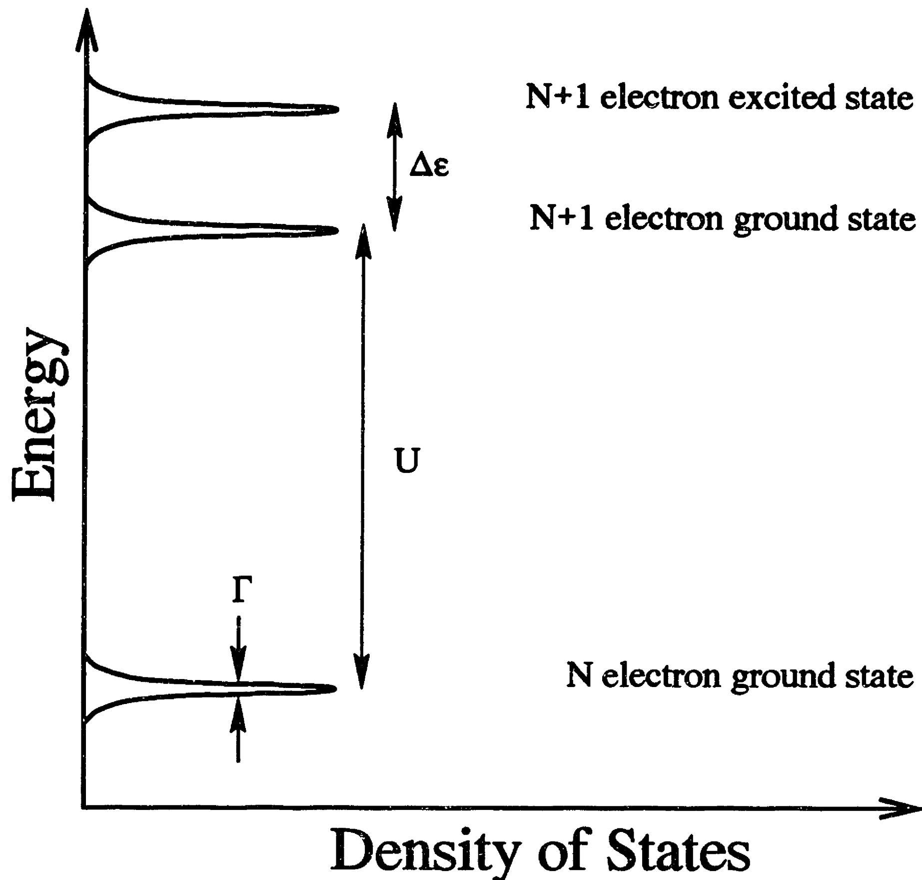

Figure 3-2: This figure shows a schematic diagram of the density of states in an artificial atom. In this plot three electronic states are shown: the ground state of N and of $N+1$ electrons, and an excited state of $N+1$ electrons. The addition energy, U, is the separation between the ground states of N and $N+1$ electrons and is frequently dominated by electron-electron interactions. The excitation energy, $\Delta\varepsilon$, is the separation between states with the same number of electrons and is dominated by the kinetic energy due to quantum confinement. The natural linewidth of a resonance, Γ, may be due to lifetime broadening.

with increasing distance the contribution to the conductance from direct tunneling across both tunnel barriers is negligible. However it is possible for an electron to tunnel from the source onto the artificial atom and to then tunnel from the artificial atom to the drain. Such processes are only possible if the artificial atom has available states near the Fermi level of the leads. Thus, the transport through such a double barrier structure can be used to probe the electronic states of the artificial atom. This process is known as transport spectroscopy. It is just one example in which a great deal of information about the electronic states of a system can be derived from the transport properties of that system.

Artificial atoms have several important energy scales, each of which can be measured by using transport spectroscopy. In figure 3-2 we show a schematic version of

the density of states of an artificial atom. The three energy scales inherent to the artificial atom are: U, known as the addition energy, is the difference in ground state energies for the system with N and $N+1$ electrons; $\Delta\varepsilon$ is the characteristic energy required to excite the atom into a higher lying quantum state without changing the particle number; Γ is the broadening of a quantum mechanical state due to its finite lifetime. The fourth important energy scale is k_BT, the temperature of the electrons in the leads. The resolution of transport spectroscopy is limited by k_BT; if the temperature is larger than any of the energy scales enumerated above we are limited in the information that we can obtain from transport spectroscopy. For artificial atoms the hierarchy of energies is $\Gamma < \Delta\varepsilon < U$.

3.1.1 Coulomb Blockade

First let us consider the conductance through an artificial atom. The conductance is defined as $I_s = GV_s$, where V_s and I_s are the bias voltage applied to the source and the current through the source, respectively. This equation, and the whole notion of conductance assumes that I_s is linear in V_s which is generally true when the voltage is vanishingly small. In general this equation is valid for an applied voltage smaller than the thermal voltage, $V_s < \frac{k_BT}{e}$. The natural units for conductance in two dimensions are $\frac{e^2}{h}$, and our conductances are usually measure in these units; later we will discuss the significance of these units (see section 4.3.3).

Since conductance through an artificial atom requires that an electron be added and subsequently removed from the artificial atom, an important energy to consider is U, the addition energy. The addition energy is a measure of the electron-electron interaction for the electrons localized in the artificial atom. Naively it can be thought of as the mutual repulsion of electrons confined in a small area, the smaller the size of the artificial atom the larger will be U. In the a simple classical approximation U is treated as the energy required to charge the capacitor whose capacitance C_Σ is determined by the size and geometry of the artificial atom, in which case $U = \frac{e^2}{C_\Sigma}$. Since the only states of the artificial atom that can be accessed are within k_BT of the Fermi level we expect that when $k_BT \ll U$ it may not be possible to add an additional electron the the artificial atom. If this is the case, there will be no conductance between source and drain; this condition is known as Coulomb blockade.[1] In the case when $k_BT \gg U$, it will not be possible to observe any traces of U in conductance; this is just one example of how the information that we can obtain from transport

[1] An excellent and very clear discussion of this issue can be found in Ethan Foxman's thesis [22].

spectroscopy is blurred by thermal smearing.

It is possible to change the energy of the electronic states on the artificial atom by changing the voltage on a nearby gate that is capacitively coupled to the artificial atom (see figure 3-1b). By simply considering the artificial atom as an island of electrons capacitively coupled to several gates we find that changing the gate voltage by ΔV_g results in a change in the energy of the electronic states by ΔE:

$$\Delta E = \Delta V_g \frac{C_g}{C_\Sigma} \quad \text{where} \quad C_\Sigma \equiv \sum_i C_i \quad . \tag{3.1}$$

C_Σ is the total capacitance of the island and C_i is the capacitance to the ith conductor. If we change the gate voltage by $\frac{e}{C_g}$ we will change the equilibrium number of charges on the artificial atom from N to $N+1$ just as we would have expected for a capacitor. Changing the gate voltage in this way effectively lowers the energy of the $N+1$ electron state until its energy is below the Fermi energy and another electron is transferred to the island.

Current can flow through an artificial atom if there is no difference in energy between the state with N or $N+1$ electrons; such a configuration is known as a charge degeneracy point. Because at such a point there is no difference between the energy of the artificial atom for the two charge states, the number of electrons is free to fluctuate. When a small bias is then applied across the leads of the system current will flow through the artificial atom. In this state charge fluctuation is allowed not because the temperature of the system is large enough to overcome the barrier to adding an electron but rather because there is no barrier to adding an electron. In our schematic band diagram (figure 3-1b) this condition is met when the energy of the $N+1$ electronic state lines up with the Fermi level. In this configuration an electron from the leads can be transferred onto the island and then off again with no energy cost, thus leading to the possibility of charge fluctuations and current.

3.1.2 Gate Voltage Sweeps

Every time the gate voltage is changed by $\Delta V_g = \frac{C_\Sigma}{C_g}\frac{U}{e}$ another electron will be added to the artificial atom. Each time an electron is added, the artificial atom passes through a charge degeneracy point and conductance through the artificial atom is possible. Therefore, we can learn a great deal about the electronic states of an artificial atom by measuring the conductance as a function of gate voltage, $G(V_g)$. For example, if the addition energy is independent of particle number we will find

periodic conductance peaks [27]. However, if there are large variations in the addition energy these will be reflected in the spacing of the conductance peaks in gate voltage.

For artificial atoms in metals and semiconductors the conductance peaks are generally periodic (see for example figure 4-1 or 4-4). This reflects the fact that each subsequent electron is being added to the same area or similarly to the same "capacitor". If, however, the addition energy varies, so too will the peak spacing. Since the energy of an electron can be divided into kinetic and potential contributions we can think of the addition energy in those term too. The potential energy is due to the electrostatic environment which consist of the attraction to the gates, repulsion form nearby electrons, and the potential from any other fixed charges that may be present in the system. The kinetic energy is due to the quantization of the wavefunction within a small area. For larger systems the potential energy contribution is generally much larger than the kinetic energy component, while for smaller systems they are of about the same size; for a hydrogen atom, for example, we know from the virial theorem that the kinetic energy is half the magnitude of the potential energy. If the the electron-electron interactions are treated as giving rise to a charging energy, and the particles are otherwise considered to be noninteracting then these two energies would be separable and we could think of the addition energy simply being $U = \frac{e^2}{C_\Sigma} + \Delta\varepsilon$. When this approximation is applied to artificial atoms it is known as the "constant interaction model".

In semiconductor artificial atoms with tens of electrons, variations in the peak spacing are typically 10%. Within the constant interaction model these irregular variations are generally thought of as arising from the variation of the kinetic energy component [28], $\Delta\varepsilon$. This picture is particularly appropriate when the confinement energy does not have a regular spectrum as is the case in the presence of disorder where theory predicts random variations in the level spectrum [29]. The picture is further supported by independent measurements of the excitation spectrum for a fixed number of particles (see section 3.1.3 for details) which finds that the magnitude of $\Delta\varepsilon$ generally agrees with the variation in peak spacing [15, 30, 31]. Regular variations of the peak spacing, on the other hand, are usually due to the a steady change in area of an artificial atom as more electrons are added and the size of the system increases [32]. There are however many examples where the details of the electron-electron interaction can not be ignored [19, 33]. This is particularly the case if the number of particles is reduced and the electrons are confined to smaller areas.

The amplitudes of the conductance peaks in a gate voltage sweep are determined by the coupling between the leads and the electronic states of the artificial atom.

This coupling is determined by the overlap of the wave function of the electronic state on the artificial atom with the wavefunction in the leads and is quantified by a coupling energy which can be found by using Fermi's Golden Rule. This coupling will determine both the amplitude and the natural linewidth of the peak. We write the coupling energy between the artificial atom and the leads as Γ_l and Γ_r for the left and right lead respectively. Since the amplitude of a peak requires tunneling onto and then off of the dot in series it will be given by the expression for barriers in series,

$$\Gamma_{amp} \propto (\frac{1}{\Gamma_l} + \frac{1}{\Gamma_r})^{-1} = \frac{\Gamma_l \Gamma_r}{\Gamma_l + \Gamma_r} \quad . \tag{3.2}$$

The natural linewidth, however, is determined by lifetime broadening of the electronic state and therefore all channels for the state's decay must be considered in parallel. If the decay is dominated by scattering into the leads then the width will be $\Gamma_{width} = \Gamma_l + \Gamma_r$. Notice that the width is dominated by the more transparent barrier while the amplitude is set primarily by the more opaque barrier; the amplitude and width need not be correlated. It is also clear that since the amplitude of the peak is determined by the overlap of the wavefunction of the artificial atom with the wavefunctions in the leads it is very sensitive to the exact shape of the wavefunction. The shape of the wavefunction depends on the exact realization of the system, and can vary dramatically due to disorder or small changes in the size of the artificial atom. This is clearly seen in the data where the amplitude of subsequent peaks can vary over several orders of magnitude. While this is also true of the natural linewidth, most data sets have peaks that are thermally broadened since $k_B T > \Gamma_{width}$ and therefore the variation in Γ_{width} is not observable (more detail is given about the peak shape below in section 3.1.4).

3.1.3 Tunneling Spectrum

By applying a finite bias to the leads it is possible to measure the tunneling spectrum of an artificial atom. A schematic band diagram is shown in figure 3-3. Typically we measure the differential conductance of the system $\frac{dI_s}{dV_s}$ as a function of bias voltage V_s applied to the source. This is done using standard lock-in techniques whereby a small signal is applied at a fixed frequency in addition to the DC bias voltage, and then the component of current at the excitation frequency is measured. In the limit of weak coupling to the leads, the differential conductance is proportional to the density-of-states on the artificial atom; the interpretation of this measurement is complicated,

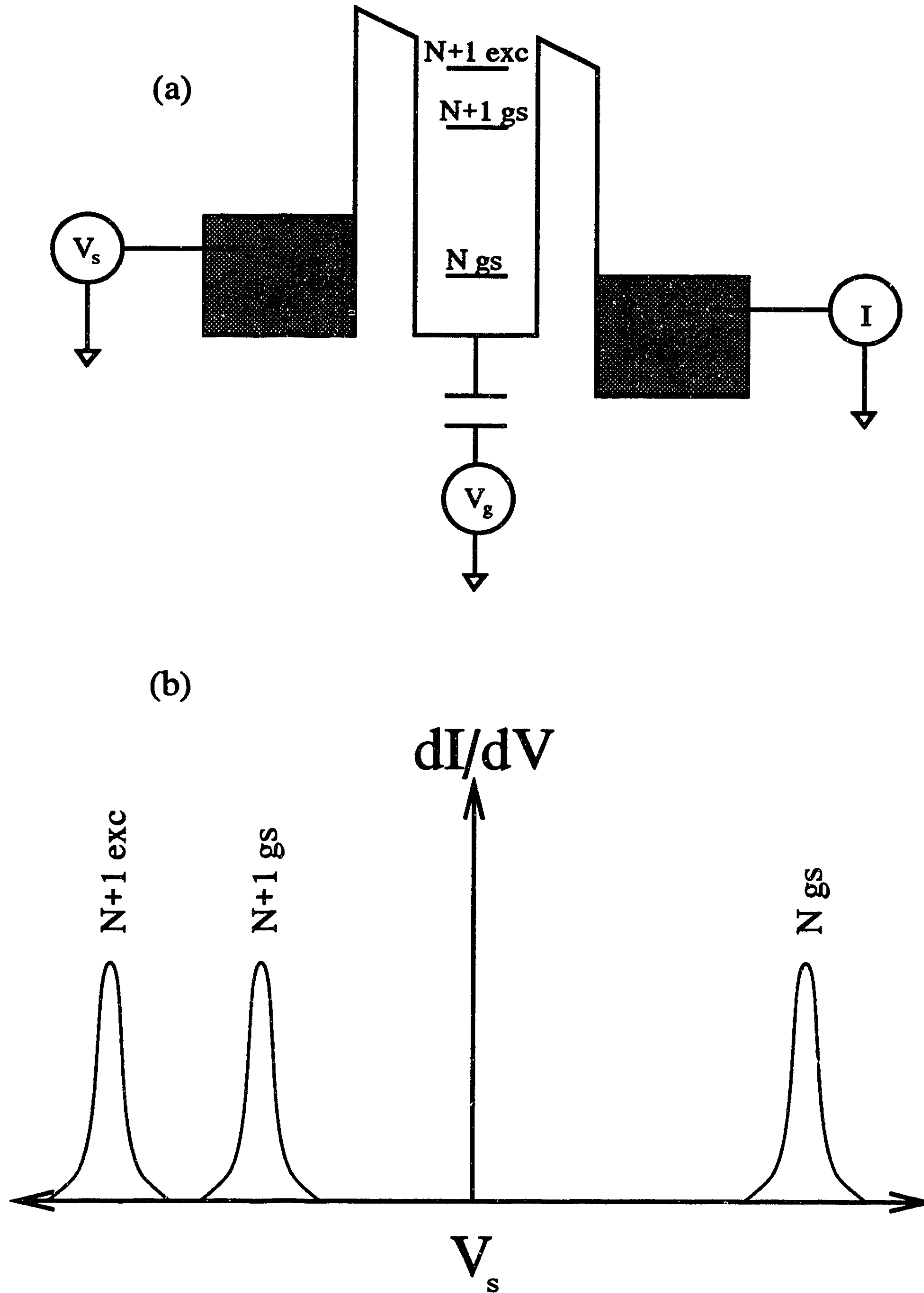

Figure 3-3: Figure (a) shows a schematic band diagram of an artificial atom when a large voltage bias, V_s, is applied between the source and the drain. In a typical measurement there is a large DC bias as well as a small AC signal applied across the device. By using lock-in techniques the AC component of current is measured thus giving the differential conductance as a function of both V_s and the gate voltage, V_g. We have labeled the available states on the artificial atom by their electron number (N or $N+1$) and noted whether the state is a ground state (gs) or an excited state (exc), following the convention of figure 3-2. In panel (b) we show a schematic tunneling spectrum for this device labeling which features in the spectrum are due to which electronic states.

however, by the sensitivity of differential conductance to the coupling between the electronic states in the leads and those on the artificial atom. For an artificial atom dominated by Coulomb blockade we expect that the tunneling spectrum will show a clear gap at zero-bias as well as features reflecting the excitation spectrum. Thus it will reveal the two energy scales U and $\Delta\varepsilon$. The expected behavior is commonly seen [15, 30, 14], and can be observed in figure 4-11.

By measuring the tunneling spectrum as a function of gate voltage it is possible to determine how the density-of-states of the artificial atom changes when the gate voltage is changed. In the simplest model, the gate voltage is capacitively coupled to each electronic state with a capacitance that is independent of the state, the gate voltage, or the number of electrons on the island; this means that changes in the gate voltage can only shift the energy of the state relative to the Fermi level, and does not otherwise change the nature of the state. In this model the location of a peak in differential conductance will then shift linearly with gate voltage. It is also important to consider the capacitive coupling that exists between the leads and the artificial atom; changing the voltage on the source changes the energy of electrons in the source and, by capacitive coupling, the energy of the localized electronic state on the island. By measuring the location of differential conductance peaks as a function of gate voltage and source voltage it is possible to extract the capacitance of the artificial atom to both the gate C_g and to the source C_s.

Peaks in the differential conductance result from additional current-carrying channels becoming available as electronic states of the artificial atom cross the quasi-Fermi level of the source or of the drain. We denote the position of a peak in the differential conductance due to an electronic state of the artificial atom crossing the quasi-Fermi level of the *source* by (V_s^s, V_g). Then after a slight change of the gate voltage δV_g the peak will be located at $(V_s^s + \delta V_s^s, V_g + \delta V_g)$. As we change the source voltage it is also possible, however, to capacitively couple to an electronic state on the artificial atom and pull it into alignment with the quasi-Fermi level in the *drain*, thus giving rise to a peak in the differential conductance. We denote such a peak in the differential conductance by (V_s^d, V_g). It is possible to distinguish these two classes of peaks[2] by their slopes, $\frac{\delta V_s^s}{\delta V_g} > 0$ while $\frac{\delta V_s^d}{\delta V_g} < 0$ as we show see below. Since the peak of the differential conductance must always occur when the Fermi level in the lead crosses

[2]In both these cases we are sweeping the source voltage and the gate voltage. In one case the peaks are due to electronic states of the artificial atom crossing the quasi-Fermi level in the swept lead (the source); in the other case, however, the electronic states are crossing the quasi-Fermi level in the lead that is not swept (the drain).

the resonance we may write the following equations employing a similar argument to that used for equation 3.1:

$$\delta V_s^d \frac{C_s}{C_\Sigma} = \delta V_g \frac{C_g}{C_\Sigma} \Longrightarrow \frac{\delta V_s^d}{\delta V_g} = -\frac{C_g}{C_s} \quad \text{and} \tag{3.3}$$

$$\delta V_s^s - \delta V_s^s \frac{C_s}{C_\Sigma} = \delta V_g \frac{C_g}{C_\Sigma} \Longrightarrow \frac{\delta V_s^s}{\delta V_g} = \frac{\frac{C_g}{C_\Sigma}}{1 - \frac{C_s}{C_\Sigma}} \quad . \tag{3.4}$$

To find C_g and C_s we solve equations 3.3 and 3.4 and obtain solutions for the capacitances ratios:

$$\frac{C_g}{C_\Sigma} = -\frac{(\frac{\delta V_s^s}{\delta V_g})(\frac{\delta V_s^d}{\delta V_g})}{\frac{\delta V_s^s}{\delta V_g} - \frac{\delta V_s^d}{\delta V_g}} \quad \text{and} \tag{3.5}$$

$$\frac{C_s}{C_\Sigma} = \frac{\frac{\delta V_s^s}{\delta V_g}}{\frac{\delta V_s^s}{\delta V_g} - \frac{\delta V_s^d}{\delta V_g}} \quad . \tag{3.6}$$

The analysis we just carried out holds for the differential conductance due to any electronic state capacitively coupled to the gates and located between the source and the drain. What distinguishes the case of an artificial atom in the Coulomb blockade regime is that the differential conductance clearly shows both a gap for addition of a particle as well as additional excited states for a fixed number of particles. However, the capacitance ratios can be extracted from equations 3.5 and 3.6 whatever the nature of the electronic states.

3.1.4 Temperature Dependence

The temperature dependence of the peaks in conductance as a function of gate voltage, $G(V_g)$, provides important information about the artificial atom. In particular the temperature dependence is the most reliable way to determine the different energy scales U, $\Delta\varepsilon$, and Γ, as well as allowing an independent measure of $\frac{C_g}{C_\Sigma}$. How the temperature, k_BT, compares with the other energy scales will determine the nature of the conductance through the artificial atom. Let us consider the different regimes: if $k_BT > U$ then thermal fluctuations will allow conductance through the artificial atom despite the energy needed to add an electron, and Coulomb blockade will not limit the conductance. However if $\Delta\varepsilon < k_BT < U$ then Coulomb blockade will limit the current flowing through the artificial atom. In this regime, however, transport will proceed through many of the excited electronic states that contain N electrons. However, when $\Gamma < k_BT < \Delta\varepsilon$ it will be possible to distinguish the individual states

through which current flows. Finally when $k_B T < \Gamma$ it is possible to study the natural lineshape of the electronic states. While this regime has not been explored, it is of great interest because the coherence of the states on the artificial atom and the states in the leads is not destroyed by thermal fluctuations. It is in this regime that the Kondo effect should be observable [34, 35].

Let us consider the explicit formula for conductance due to tunneling through electronic states between the source and the drain. This formulation of the problem is valid for an artificial atom but is more general and will also apply to a variety of other systems. To determine the conductance through this system we must sum left moving current and right moving current. $g(\varepsilon)$, the conductance contribution of an electron at an energy ε, is determined by the density-of-states of the artificial atom multiplied by the probability that the state at energy ε is unoccupied multiplied by the transition probability for tunneling into and then out of that state. Writing the Fermi-Dirac distribution in the leads as $f(\varepsilon)$, and δV_s as the bias voltage, we use Fermi's golden rule:

$$I_{right} = \frac{e}{2\pi\hbar}\int f(\varepsilon)g(\varepsilon)\,d\varepsilon \tag{3.7}$$

$$I_{left} = \frac{e}{2\pi\hbar}\int f(\varepsilon + e\delta V_s)g(\varepsilon)\,d\varepsilon \quad . \tag{3.8}$$

Since we are interested in the conductance which is the linear response of the system, we expand equation 3.8 to first order in $f(\varepsilon)$:

$$I_{left} = \frac{e}{2\pi\hbar}\int \left[f(\varepsilon) + \frac{df}{d\varepsilon}e\delta V_s\right] g(\varepsilon)\,d\varepsilon \quad . \tag{3.9}$$

Summing the left moving and the right moving current we then have:

$$I_{total} = I_{left} - I_{right} = \frac{e}{2\pi\hbar}\int \frac{df}{d\varepsilon}e\delta V_s g(\varepsilon)\,d\varepsilon \quad . \tag{3.10}$$

And thus the conductance is given by:

$$G = \frac{I_{total}}{\delta V_s} = \frac{e^2}{2\pi\hbar}\int \frac{df}{d\varepsilon}g(\varepsilon)\,d\varepsilon \quad . \tag{3.11}$$

Equation 3.11 determines the conductance for a given gate voltage configuration. To determine the conductance as a function of gate voltage it is necessary to evaluate

equation 3.11 replacing $g(\varepsilon)$ with $g(\varepsilon + \frac{C_g}{C_\Sigma}V_g)$ for each point in gate voltage:

$$G(V_g) = \frac{e^2}{h}\int \frac{df}{d\varepsilon}(\varepsilon)\, g(\varepsilon + \frac{C_g}{C_\Sigma}V_g)\, d\varepsilon \quad . \tag{3.12}$$

To show the lineshape expected for peaks with very narrow $g(\varepsilon)$, we explicitly write the form of the derivative of the Fermi-Dirac distribution:

$$-\frac{df}{d\varepsilon} = \frac{1}{k_BT}\frac{\exp(\varepsilon/k_BT)}{(\exp(\varepsilon/k_BT)+\exp(-\varepsilon/k_BT))^2} = \frac{1}{4k_BT}\left[\cosh(\frac{\varepsilon}{2k_BT})\right]^{-2} \quad . \tag{3.13}$$

From this equation we note that equation 3.13 has a maximum amplitude that decreases as $\frac{1}{4k_BT}$ and a full width at half maximum of $3.52k_BT$.

Finally, we would like to note that we expect the density-of-states on the artificial atom to be made up of discrete states, each of which has a Lorentzian lineshape. If there is a resonance at ε_0, then the conductance contribution near that resonance will be proportional to the Lorentzian density-of-states [22, 30]:

$$g(\varepsilon) \propto \frac{\Gamma/\pi}{(\varepsilon-\varepsilon_0)^2+\Gamma^2} \quad \text{where } \frac{h}{\Gamma} \text{ is lifetime of the state.} \tag{3.14}$$

The Lorentzian form is general in nature and reflects the decay process of the quantum state. If the quantum state has a lifetime τ it will decay in time as $\exp(-\frac{t}{\tau})$ and the lineshape will be a Lorentzian with a width $\Gamma = \frac{h}{\tau}$. The energy spectrum of the Lorentzian is just the fourier transform of the temporal exponential decay; since the exponential decay is general and does not depend on the decay channel, we also expect the Lorentzian lineshape to be general. For the ground-state of the artificial atom, the main decay channel that contributes to the lifetime will be due to scattering into the leads. We should, however, note that electron-electron interactions may cause deviations from the Lorentzian lineshape by changing the nature of the decay [36].

Having written the general expression for the conductance we now consider the temperature dependence in the regime pertinent to this study. We are be interested in the functional dependence of the peak amplitude, G_{max}, and of the peak width in gate voltage measured by the full width at half maximum, $FWHM$. We can approximate the width of the peak (equation 3.12) by

$$FWHM = \frac{1}{e}\frac{C_\Sigma}{C_g}(3.52k_BT + 2\Gamma) \quad \text{and thus}$$

$$\frac{d(FWHM)}{dT} = 3.52\frac{C_\Sigma}{C_g}\frac{k_B}{e} \quad \text{and} \quad FWHM\ (T{=}0) = \frac{2\Gamma}{e} \quad . \tag{3.15}$$

In the regime where $k_B T \ll \Gamma$ equation 3.12 yields a temperature independent $G_{max} \propto A$ and $FWHM = \frac{C_\Sigma}{C_g}(2\Gamma)(1+\frac{3.52k_BT}{2\Gamma}) \approx 2\frac{C_\Sigma}{C_g}\Gamma$. This is not surprising since the natural lineshape of the resonance, which is temperature independent, will determines the peak shape; finite temperature tends only to slightly broaden the peaks. In the regime where $\Gamma \ll k_BT \ll \Delta\varepsilon$ the shape of the conductance peak will be dominated by the derivative of the Fermi-Dirac function, $\frac{df}{d\epsilon}$. In the case $G_{max} \propto \frac{A}{4k_BT}$ while the width is given by $FWHM = \frac{C_\Sigma}{C_g}(3.52k_BT)(1+\frac{2\Gamma}{3.52k_BT}) \approx 3.52\frac{C_\Sigma}{C_g}k_BT$. Notice that in both cases the width of the conductance peak is scaled by the capacitive division factor $\frac{C_\Sigma}{C_g}$, as expected from equation 3.1. Examining equation 3.15, it is clear that we can determine $\frac{C_g}{C_\Sigma}$ from a measurement of $\frac{d(FWHM)}{dT} = 3.52\frac{C_\Sigma}{C_g}k_B$, and thus convert gate voltage into an energy scale. Similarly we may find Γ by taking $FWHM(T=0) = 2\Gamma$. Finally we note that the magnitude of A in these conductance formulae is determined by the two barriers in series, as discussed above on page 45, and thus $A = \frac{\Gamma_l\Gamma_r}{\Gamma_l+\Gamma_r}$.

Under certain circumstances it is possible to obtain a temperature dependence of a conductance peak that is different from that discussed above. We do not believe that either of the two cases mentioned below apply to the measurements presented in this thesis, however we review them nonetheless. In the case when $\Delta\varepsilon < k_BT < U$ the conductance peaks have a temperature independent G_{max} and have $FWHM = 4.35\frac{C_\Sigma}{C_g}k_BT$ [37]. Another possibility exists in the regime where $k_BT < \Delta\varepsilon$ when the ground state is very weekly coupled to the leads while an excited state has stronger coupling. Such a situation is considered in reference [38]. There Foxman *et al.* find that it is possible to have conductance peaks whose amplitude increases with temperature. As the temperature is increased, so too is the possibility of having an electron energetic enough to tunnel through an excited state which has higher conductance. They found that in this case the conductance can increase by as much as a factor of two before crossing over into temperature independent behavior.

3.1.5 Magnetic Field Dependence

The application of a magnetic field to the artificial atom can greatly change the nature of its electronic states and therefore its transport properties. There are two important field scales that dictate the nature of these changes. When one flux quantum $\Phi_0 = \frac{h}{ec}$ penetrates the artificial atom, at a field $B_1 = \frac{\Phi_0}{A}$, the quantum mechanical phases of the electrons are altered by approximately π. Here A is the area of the artificial atom, and c is the speed of light. At a higher field for which there is one flux quantum per

electron and $B_{\nu=1} = n\Phi_0$ then the nature of the electronic states will be fundamentally changed. For the two-dimensional electron gas the states are the Landau levels that develop in a magnetic field; these Landau levels can naively be thought of as the quantum mechanical version of electrons executing cyclotron orbits. Analogous states are expected in artificial atoms if the confinement potential is harmonic (cite Darwin/Fock and McEuen). In both field regimes the changes in the electronic states of artificial atom and of the leads change the transport properties.

When $B \approx B_1$ the phase of an electronic states of the artificial atom is effectively randomized. In other words, if we examine a single electronic state as a function of field the wavefunction is no longer correlated with that at $B = 0$ after we have changed the field by B_1. These predictions are valid in the regime where the disorder in the sample or at the sample's edge randomize the phases of the electronic states [39]; this will only be true at low fields $B \ll B_{\nu=1}$ where the states are still sensitive to the boundaries and are not dominated by the magnetic field. Thus, as we increase the field in this regime the excitation spectrum of the artificial atom, as well as the coupling between the states and the leads, will change. Experimentally this can be seen both in a measurement of $G(V_g)$ as well as in a measurement of the differential conductance. We expect that the amplitude of the conductance peaks will vary considerably as their coupling is modified [40, 41]. Since the excitation spectrum is changing as a function of field we expect to to observe these changes both in the differential conductance as well as by shifts in the position of conductance peaks in gate voltage of order $\frac{C_\Sigma}{C_g}\Delta\varepsilon$.

At higher magnetic fields $B \approx B_{\nu=1}$ and for a confining potential that is slowly varying in space the electronic states of the artificial atom are quantized into Landau levels. This is true both of the electronic states in the leads as well as the localized states in the artificial atom, though the two regions may have different filling factors $\nu \equiv \frac{n\Phi_0}{B}$ due to variations in density. The Landau level wavefunctions can be understood by recalling that electrons free to move in two dimensions in a magnetic field normal to the place of their motion are effectively confined in a parabolic well due to the field. The electronic states in this effective confining potential are Gaussian; the strength of the effective confining potential and therefore the decay of the wavefunction with radial coordinate r depends on field

$$\psi(r) \propto \exp(-\frac{\pi}{2}\frac{r^2 B}{\Phi_0}) \quad . \tag{3.16}$$

Thus, at high fields the tunneling through the barriers is suppressed exponentially with distance as $|\psi(r)|^2$. This effect is quite general and is important for any problem

involving tunneling in a magnetic field. In artificial atoms, for which the nature the confinement of the localized electronic states is well understood, there have been careful studies of how the conductance varies due to more subtle changes that the magnetic field induces in these electronic states; these changes can also be correlated to shifts in the position and amplitude of conductance peaks [19, 42, 43]. These same changes also effect the excitation spectrum of the artificial atom [44, 45].

3.1.6 Dependence on Thermal Cycle

Finally we would like to discuss how the conductance of an artificial atom changes when the device is warmed to room temperature and then cooled back down to low temperatures. The process of thermally cycling a device is important because there are processes that can affect the electronic states and transport properties of an artificial atom that are frozen out at measurement temperatures ($T \lesssim 10\,\mathrm{K}$) but change at room temperature. For example, the detailed configuration and occupation of charged impurities can change at room temperature and therefore the impurity potential in the vicinity of the artificial atom can be changed by thermal cycling. Thus, properties of the artificial atom that are dominated by the impurity potential will change while those properties that are intrinsic or are due the intentional fabrication of the device will not. While the division of properties in this way is somewhat arbitrary it is quite useful.

The size of a lithographically patterned artificial atom, and therefore the spacing of conductance peaks does not change when the impurity configuration is changed. However, the wavefunctions of the electronic states may change. Thus, we expect that while the peak spacing of conductance peaks should not change with thermal cycling the amplitudes of the conductance peaks after thermal cycling may be totally different. This type of experiment has proven to be quite revealing; for example, when periodic conductance oscillations were first found [46, 26] their period changed after a thermal cycle because the size of the region in which electrons were localized was determined by the impurity potential. However, when an artificial atom is localized using lithographically patterned gates, the peak spacing did not change after thermal cycle [13].

3.2 Single Barriers

Let us consider a barrier that separates two regions of a two-dimensional electron gas. Such a barrier consists of a region where the lowest-lying electronic states are above the Fermi level of the electron gas; equivalently we may say that the conduction band bottom is higher than the Fermi energy in the barrier region. An electron at the Fermi level is prohibited in classical mechanics from spending time in this region, however such an electron may quantum mechanically tunnel through this barrier. The barrier may be formed by electrostatic depletion of the electron gas as discussed in section 2.1, or it may be formed by a material boundary such as a Si/SiO_2 interface. In this section we will consider the transport of electrons from the electron gas on one side of the barrier to the electron gas on the other side of the barrier; the nature of the barrier will not affect our considerations. We will focus primarily on transport due to tunneling through this barrier.

3.2.1 Gate Voltage Dependence

Changing the voltage on a gate located in the vicinity of a barrier will change the conductance of the barrier. The gate will be capacitively coupled to the barrier and thus changing the gate voltage will lower the barrier whose height above the Fermi level as a function of distance we write as $E_b(x) - E_f$; this is the case in our device where the upper gate covers the depleted region where the electrostatic barrier is formed (see figure 2-1). The conductance of the barrier results from tunneling of electrons at the Fermi level plus a contribution from thermally excited electrons with energies greater than the barrier; at low temperatures $k_B T \ll (E_b^{max} - E_f)$ the tunneling term will dominate. The tunneling probability is computed by finding the quantum mechanical wave equation. Using the WKB approximation we may write transition probability

$$g(\varepsilon) \propto \exp\left(-\int \sqrt{\frac{2(E_b(x) - \varepsilon)m^*}{h^2}}\, dx\right) \tag{3.17}$$

where $E_b(x)$ is energy of the band edge as a function of distance, and m^* is the band mass of the electron. To compute the conductance at a given gate voltage we must use equation 3.17 in the conductance formula (eq. 3.12). Thus the conductance will increase dramatically and monotonically as the gate voltage is increased and $E_b(x) - E_f$ is lowered.

There are secondary effects that may further increase the conductance of the barrier as the gate voltage is increased. For example, as the density in the electron gas is raised due to increasing gate voltage, the improved screening ability of the electron gas may make the barrier narrower thus decreasing the tunneling distance as gate voltage is increased. While the change in the tunneling distance will depend on barrier shape and electron density this effect can only increase the conductance further.[3] Additionally we expect the contribution of thermal activation to increase the conductance still further as the barrier is lowered. When the barrier gets low enough the activated contribution will become dominant over tunneling; in the case of a rectangular barrier of width d, this will be when the barrier is low enough so that $(E_b - E_f) \ll \frac{(k_B T)^2}{\hbar^2/(2d^2 m^*)}$. In the activated regime, as in the tunneling regime, the conductance will rise exponentially with increase gate voltage. Whether or not these secondary effects are important our conclusion remains; the conductance through a barrier will increase exponentially as the gate voltage is increased.

3.2.2 Temperature Dependence

Increasing the temperature will tend to broaden the features of a conductance versus gate voltage plot. When in the tunneling regime this is primarily due to the broadening of the Fermi function in equation 3.12. As noted above, the conductance remains a monotonic function of gate voltage no matter which regime we are in. We will see that the behavior of the barriers formed in our devices is quite different, thus implying that they are not the simple barriers we have just been considering.

3.2.3 Magnetic Field Dependence

The magnetic field will affect the tunneling through a barrier because it changes the states of the electron gas that constitute the leads. In all cases the magnetic field suppresses the conductance of electrons through the barrier. The natural field scale for a barrier whose area is $\approx d^2$ is $B_0 = \frac{\Phi_0}{d^2}$. At high fields the suppression of the conductance will be of the form $\log\, G \;\propto\; -\frac{\pi}{2}\frac{B}{B_0}$, as seen in equation 3.16. The important point, without going into further detail, is that the magnetic field suppresses

[3] If we compare tunneling through a rectangular barrier and a parabolic barrier this effect is obvious. In a rectangular barrier the tunneling distance does not change with ε and thus $\log[g(\varepsilon)] \propto \sqrt{E_b - \varepsilon}$. While in the inverted parabolic barrier, the tunneling distance changes with ε and thus $\log[g(\varepsilon)] \propto (E_b^{max} - \varepsilon)$. The increase in tunneling distance has caused $g(\varepsilon)$ to rise more rapidly with ε.

the conductance on a field scale B_0; thus the magnetic field induced suppression of the conductance can be used to determine d, the size of t'.e barrier.

3.3 Hopping

Another important model system we wish to consider is transport through an insulator that has only localized states. Such an insulator arises from the localization induced by disorder, and is usually known as an Anderson insulator. The electronic states of an Anderson insulator are characterized by localized sites with random binding energies. Unlike a metal where the electronic states are extended over the sample an insulator has states that are localized at various points in the sample. The fact that the electronic states are localized gives rise to two important properties associated with the electrons in an insulator: screening and transport properties. Placing an extra charge in an insulator will distort the localized states giving rise to dipole moments and dielectric screening; in a metal, however, since charge is not localized and is free to rearrange, the screening is much more efficient. Obviously, the transport of charge is also encumbered by the localization of charge since electrons can no longer flow freely from one end of the sample to the other.

Charge localization does not mean that it is not possible to transport electrons through a sample. It is possible for an electron to tunnel from one localized site to another and thus traverse the sample by "hopping". Since the binding sites have random energies the electron must absorb or emit energy as it tunnels. This process is called inelastic tunneling and requires exchanging energy with other degrees of freedom in the sample, usually by absorbing or emitting a phonon. As the temperature is lowered the energy available from the thermal bath is reduced and an electron must find another site with an energy closer to its own. This will require hopping a longer distance and thus will be much less likely. For this reason the conductance will be suppressed as the temperature is lowered. Reduced conductivity as the temperature is lowered is characteristic of insulators.

Starting with the physical picture described above various detailed theories have been developed. The rich literature of this subject includes detailed studies of disorder in regular lattices due to random binding sites, disorder as found in amorphous materials, the effects of dimensionality on transport, the effects of Coulomb correlations, and higher order quantum mechanical corrections.[4] Some predictions of these

[4]For general reviews of hopping and trasport in disorded and noncrystaline systems see [47, 48],

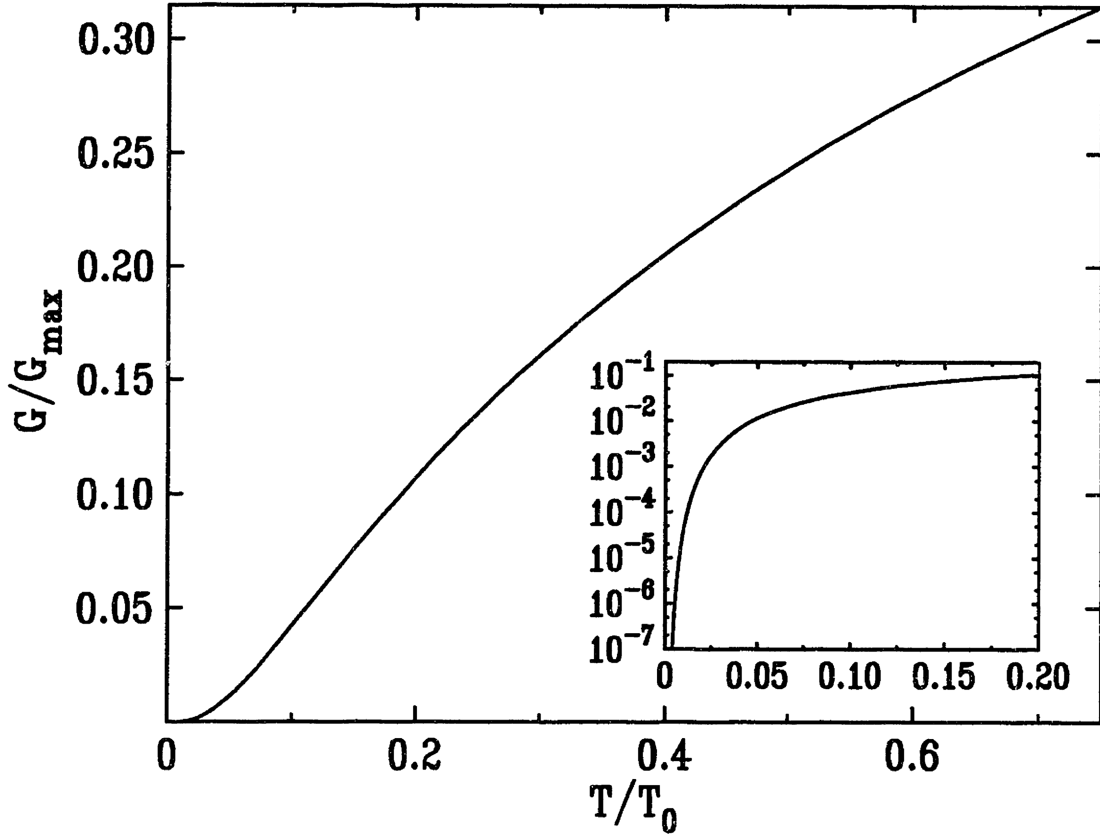

Figure 3-4: This figure shows the hopping conductivity expected from equation 3.18 for the case $\alpha = \frac{1}{2}$. The conductivity is plotted in units of $\frac{G}{G_{max}}$ while the temperature is plotted in units of $\frac{T}{T_0}$. The sigmoidal shape of this curve on a linear scale is visible, and is characteristic of equation 3.18 whatever the value of α. The inset shows the same cure on a semilog plot and emphasizes how quickly the conductivity falls to zero at low temperatures.

theories are presented below.

3.3.1 Temperature Dependence

As the temperature is lowered there is less thermal energy for an electron to absorb in an inelastic tunneling process. Since the electron must "hop" to a site within $k_B T$ of its energy and since there is no spatial correlation between the energy of sites on average the hopping distance will get longer as the temperature is lowered; this is known as variable range hopping. The predicted temperature dependence of variable

for a review of higher order corrections see [49], and for an overview of Coulomb correlations see the very readable [4].

range hopping in the absence of correlations is [47]:

$$G(T) \propto \exp\left[-\left(\frac{T_0}{T}\right)^{\alpha}\right] \tag{3.18}$$

where α and T_0 depend on the system. In most cases $\alpha = \frac{1}{1+d}$ and $k_B T_0 = N(E_f)\,\xi^d$ where d is the dimension of space, $N(E_f)$ is the density-of-states at the Fermi level, and ξ is the radius in which the electron is localized. $\xi(E)$ is also known as the localization length, and it changes as a function of energy E becoming infinite at energies where the states are delocalized. Equation 3.18 is valid for the average conductance and may vary if there is one step that limits the transport. There are corrections to this formula due to electron-electron interactions; most notably, in two dimensions it has been shown [48] that in the presence of interactions $\alpha = \frac{1}{2}$. In any case the conductance is strongly suppressed at low temperatures. A plot of this temperature dependence is shown in figure 3-4 for the case of $\alpha = \frac{1}{2}$, but the characteristic shape of the curve does not depend on α.

3.3.2 Magnetic Field Dependence

As discussed in sections 3.1.5 and 3.2.3 the conductance is suppressed as the magnetic field is increased. It was noted in those sections that the suppression of the conductance is due to the reduced decay length of the wavefunction and thus suppression of tunneling in magnetic fields. The exact nature of the suppression depends on the nature of the electronic state and on the magnitude of the magnetic field. If the field is weak $B \ll \frac{\Phi_0}{\xi^2}$ then the tunneling probability and the conductance will be suppressed by [48, eq. 7.1]

$$G \propto \exp\left(-\xi r^3 \frac{\pi^2}{3}\frac{B^2}{\Phi_0^2}\right) \quad \text{at a distance} \quad r \ll \frac{\Phi_0}{B}\frac{1}{\xi} \quad . \tag{3.19}$$

However if the field is strong or if $r \gg \frac{\Phi_0}{B}\frac{1}{\xi}$ then the suppression will be of the same form as that of an electron that is magnetically confined, and the tunneling will be suppressed according to equation 3.16. We again see that whatever the nature of the electronic state tunneling is suppressed at high fields, and that the field scale of the suppression can be used to extract a length scale over which an electron tunnels.

Chapter 4

Single and Double Barriers

In this chapter we begin our presentation of data from the study of the devices we have fabricated. We find that, as expected, we can confine electrons between two barriers, and that the conductance of this artificial atom is dominated by Coulomb blockade. In studying transport through this system we find additional structure that is due to transmission resonances through the *individual* barriers. The rest of the chapter, and much of the rest of this thesis, is devoted to the study of the transport through individual barriers. In this chapter we focus on the study of one device which shows Coulomb blockade in a single barrier, while in subsequent chapters we will review data from the study of many different single barrier devices as well as discuss how it may be possible to have conductance resonances in a single barrier.

4.1 Double Barrier

4.1.1 Periodic Conductance Oscillations

We begin by examining the conductance as a function of gate voltage of a device with two barriers as shown in figure 4-1. The first thing to note is that the peaks are periodic with a spacing of $\Delta V_{ug} = \frac{e}{C_g} = 12.5\,\mathrm{mV}$ in upper gate voltage; this is exactly what we expect for Coulomb blockade. We first analyze the peak spacing to determine the Coulomb blockade addition energy $U \approx \frac{e^2}{C_\Sigma}$. To do this we must determine the factor $\frac{C_g}{C_\Sigma}$ so that we may convert the gate voltage spacing of the conductance peaks into an energy; the width of one of the peaks is plotted in figure 4-2 and analyzed using equation 3.15. From fitting the width to a line we extract $\frac{d(FWHM)}{dT} = 2.0\,\mathrm{mV/K}$ which gives us a value of $\frac{C_g}{C_\Sigma} = .15$. Using this value we then find that $\frac{e^2}{C_\Sigma} = \frac{C_g}{C_\Sigma}\frac{e^2}{C_g} = e\frac{C_g}{C_\Sigma}\Delta V_{ug} = e \times .15 \times 12.5\,\mathrm{mV} = 1.9\,\mathrm{meV}$. Finally using

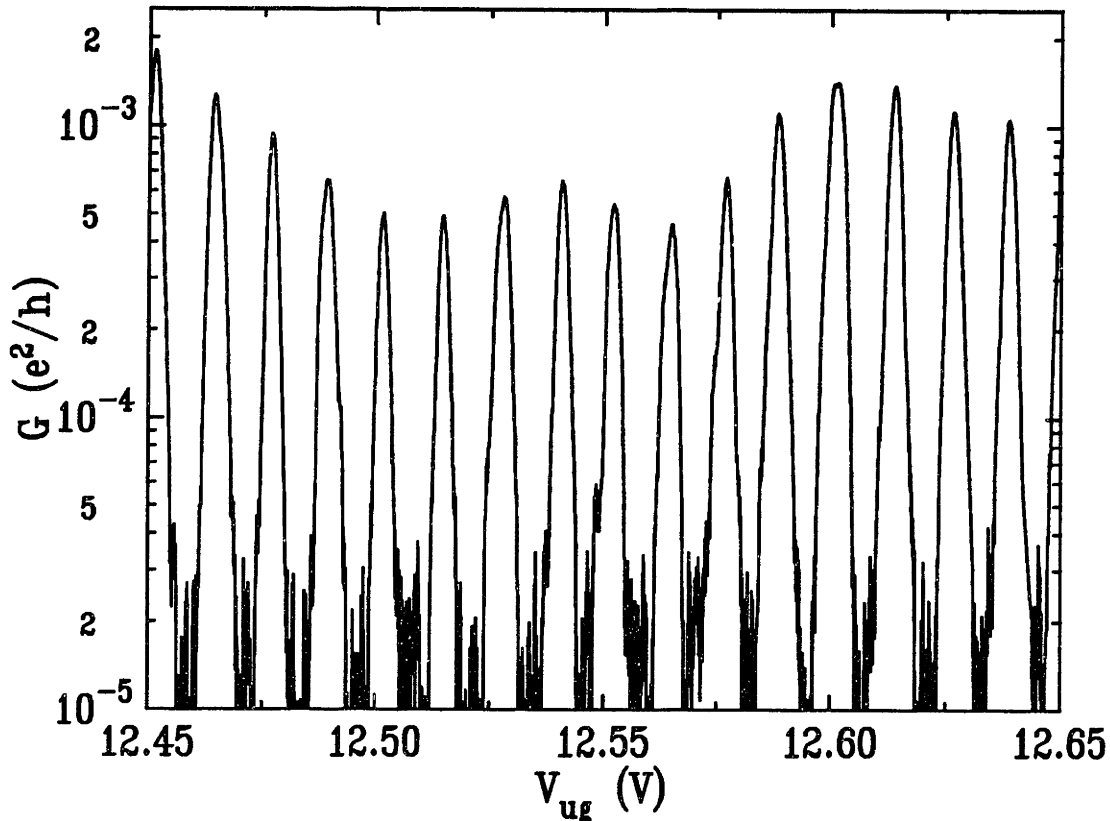

Figure 4-1: **Conductance versus gate voltage for a device with electrons isolated between two barriers. In the text we find $U = 1.9\,\text{meV}$. The approximate lithographic size of the device is $250\,\text{nm} \times 270\,\text{nm}$. Data taken at $T = .32\,\text{K}$, $V_l = -4.5$, $V_r = -8.0$ on device F30 wafer #13.**

equation 3.15 we can find the natural line width of this peak $\Gamma = 120\,\mu\text{eV} = k_B \times 1.4\,\text{K}$; this value of the natural linewidth is larger than the measurement temperature of .3 K giving $\frac{\Gamma}{k_B T} \approx 5$.

It is worth comparing the numbers that we find for this device to typical numbers for the GaAs devices that have been previously studied. For devices fabricated by Udi Meirav and measured by Ethan Foxman [22] at MIT, typical values of the charging energy were $\frac{e^2}{C_\Sigma} \approx .6\,\text{meV}$, typical excitation energies were $\Delta\varepsilon \approx 50\,\mu\text{eV}$, and the temperature was typically larger than the natural linewidth even at the lowest temperatures thus giving an upper bound of $\Gamma < 10\,\mu\text{eV}$. The smallest of the devices they studied had a lithographic dimension of $\approx 500\,\text{nm} \times 500\,\text{nm}$. The device we fabricated, whose measurements were just presented, has a lithographic dimension of about $\approx 250\,\text{nm} \times 270\,\text{nm}$ in size, one of the larger devices that we fabricated. The increase by a factor of three in the magnitude of $\frac{e^2}{C_\Sigma}$ is due to the decreased size of the device, while the increase in Γ is due to strong coupling between the leads and the artificial atom. This coupling will be discussed at length below (see section 4.3).

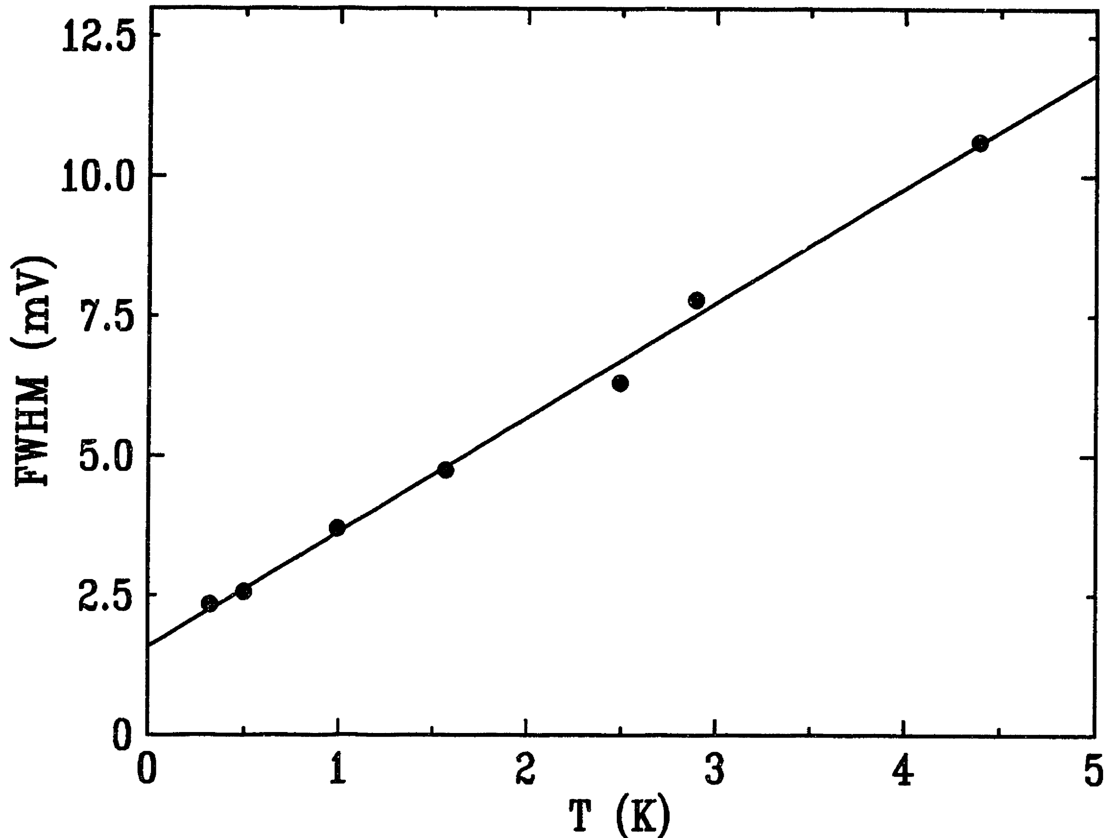

Figure 4-2: The temperature dependence of the full width at half maximum ($FWHM$) of one of the conductance peaks show in figure 4-1. From this measurement we find $\frac{C_g}{C_\Sigma} = .15$ and $\Gamma = 120\,\mu$eV.

It is also interesting to compare the strength of the electric field applied across the dielectric in these two devices. In the silicon MOS device the field has a magnitude of $\approx 2.5 \times 10^6$ V/cm, while in the GaAs device the field is $\approx 1.5 \times 10^4$ V/cm. The two order of magnitude difference between the strength of the field reflects the difference in the characteristics of the dielectric. While SiO_2 can withstand fields up to 10^7 V/cm, GaAlAs, which is the insulating layer in a GaAs/AlGaAs heterostructure, would have intolerable leakages at fields of 10^5 V/cm. The wide range of fields that a silicon MOS device can withstand allows these devices to be operated over a much broader range of parameter space.

We wish to compare the capacitance of the device that we have measured to and compare it to some model capacitor systems. We will consider two simple model systems: a parallel plate capacitor consisting of two parallel sheets of metal, and a metallic disk which is circular in two dimensions and flat in the third. In both cases we will consider the affect of the dielectric background; since our system consists of both Si and SiO_2 we take an average dielectric constant $\epsilon_{av} = \sqrt{\epsilon_{Si}\epsilon_{SiO_2}} = 6.8\,\epsilon_0$. The

capacitance of a parallel plate capacitor of area A and separation s is

$$C = \frac{\epsilon_{av}}{4\pi}\frac{A}{s} \quad \text{if } s = 100\,\text{nm then} \quad C = 6.0 \times 10^{-22} \times A\,\frac{\text{F}}{\text{nm}^2}$$
$$\text{thus giving} \quad \frac{e^2}{C} = 267\,\text{eV} \times \frac{\text{nm}^2}{\text{A}} \quad . \tag{4.1}$$

Knowing that $\frac{e^2}{C_\Sigma} = 1.9\,\text{meV}$, we can use this formula to compute the expected size of the artificial atom. We find that $A = 1.4 \times 10^5\,\text{nm}^2$, or we may assume the parallel plates are disks of radius r and then we find $r = \sqrt{\frac{A}{\pi}} = 210\,\text{nm}$; given the lithographic dimensions of $250\,\text{nm} \times 270\,\text{nm}$ we might have expected $r \approx 125\,\text{nm}$. The overestimate of the size of the device means that the capacitance of the artificial atom is larger than we would have expected from the model given its lithographic dimensions. The model, however, neglects edge effects of this capacitor which are important given its low aspect ratio $\frac{r}{s} \approx 1.3$. In addition the effect of other conductors in the vicinity of the artificial atom have been ignored; both these corrections tend to reduce the energy required to store charge in a capacitor and thus to increase the capacitance of the actual device. Given the geometry of the artificial atom it is reasonable to model it as a metallic disk. The capacitance of a disk of radius r is given by[1] :

$$C = \frac{2}{\pi}\epsilon_{av} r = \quad \text{so} \quad C = 4.8 \times 10^{-19} \times r\,\frac{\text{F}}{\text{nm}}$$
$$\text{thus giving} \quad \frac{e^2}{C} = .33\,\text{eV} \times \frac{\text{nm}}{\text{r}} \quad . \tag{4.2}$$

Substituting the charging energy into equation 4.2 we find $r = 170\,\text{nm}$. Again we find that the capacitance of the artificial atom is larger than that estimated by the model. As with the previous model, we believe that this discrepancy is due primarily to our failure to consider the presence of nearby conductors when computing the capacitance of the artificial atom. It is noteworthy that this model's estimate of the size has an error of less than 50%.

We perform two other experiments that further convince us that the Coulomb blockade observed in this device is due to the electrostatic confinement of electrons by the lithographically patterned gates. These experiments are meant to discriminate between electrons confined by the lithographic gates and electrons confined by fluctuations in the impurity potential. There have been many observations of Coulomb blockade in systems in which there is no intentional confinement [1, 2, 46, 51, 52]

[1]The capacitance of a disk, C_{disk}, is just slightly for than the capacitance of a a sphere, C_{sphere}, of the same radius: $C_{disk} = \frac{2}{\pi}C_{sphere}$. See reference [50, eq. 4.20]

(see section 5.1); additionally many of the properties of our devices are dependent on the realization of the impurity potential as will be described in detail below (see section 6.2.3. Thus it is important to distinguish the Coulomb blockade which we observe in these devices. In the first experiment, we have warmed the device to room temperature and then cooled it back down to .3 K, and it continues to show periodic conductance oscillations with the same period. As discussed in section 3.1.6 warming the device to room temperature and recooling it effectively rerandomizes the impurity potential by changing the occupation of charge traps and by allowing the motion of certain types of mobile defects. If electrons are confined by the impurity potential then the area to which they are confined will be changed and therefore the period of Coulomb blockade oscillations will be different after a thermal cycle [26]. Since in our experiments we found that the period did not change after a thermal cycle, we conclude that the electrons are not confined by disorder but rather are confined by the gate pattern. In the second experiment, we measure an artificial atom whose gates define a smaller lithographic area and in this smaller device we find a larger oscillation period; this is what would be expected with a smaller artificial atom which has a smaller C_{ug}, and thus a larger period, $\Delta V_{ug} = \frac{e}{C_{ug}}$. Thus using the two hallmark experiments of this field we can be confident that we have observed Coulomb blockade in an intentionally fabricated artificial atom.

4.1.2 Amplitude Envelope of Coulomb blockade Oscillations

An examination of the amplitude of the conductance oscillations presented above makes it clear that the system we are studying has some usual behavior worthy of further study. In figure 4-1 we plotted only a limited range in gate voltage, while in figure 4-3 we present a sweep over a larger range in gate voltage; the difference between the figures is only the range of gate voltage swept, otherwise they are the same device at same temperature with the same period of conductance oscillations. Figure 4-3 is notable because it clearly shows that the amplitude of the conductance oscillations are modulated by an envelope function. As we saw in section 3.1.4 the amplitude of the conductance oscillations is due to having two tunnel barriers in series $G \propto \frac{\Gamma_l \Gamma_r}{\Gamma_l + \Gamma_r}$, thus the natural interpretation of the changes in amplitudes is in terms of changes in Γ_l (or Γ_r), the coupling between the artificial atom and the left (or right) lead.

Typically the magnitude of the coupling between the leads and the artificial atom is determined by the overlap of the wavefunction for an electron in the lead and the

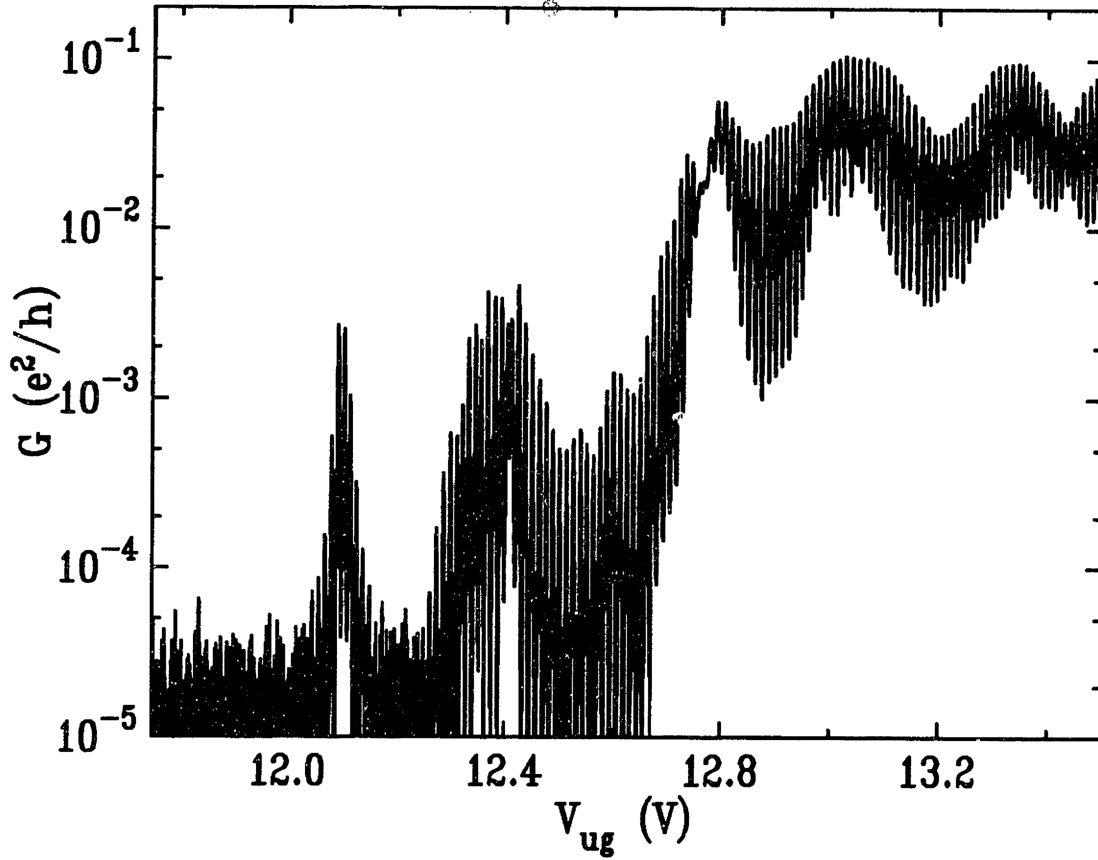

Figure 4-3: $G(V_{ug})$ which shows a larger range of the Coulomb blockade oscillations seen in figure 4-1. Here we see that the amplitude of the conductance peaks are modulated by an envelope function which varies smoothly over many periods of the Coulomb blockadeoscillations. We believe that this envelope function is due to variations of the transmission through one of the barriers as a function of gate voltage. Data taken on same device, same lower gate voltages, and same temperature as figure 4-1.

wavefunction of an electron on the artificial atom. Since this overlap is very sensitive to the amplitude and phase of the wavefunction near the barrier and since the wavefunction of electrons in the leads is not very dependent on energy, variations in the amplitude of conductance peaks is normally attributed to variations of the wavefunction of successive electrons on the artificial atom. As we discussed in section 3.1.5 if the confinement potential is not symmetric[2] the variation in the wavefunction will then give rise to random variation in the peak amplitudes from one peak to the next rather than a continuous variation of an amplitude envelope function. Data taken on an artificial atom fabricated in a GaAs material system are shown in figure 4-4; these data show random variation in peak amplitude from one peak to the next as

[2]Even if the lithography were cylindrically symmetric, any disorder or imperfections in the lithography would then break the symmetry.

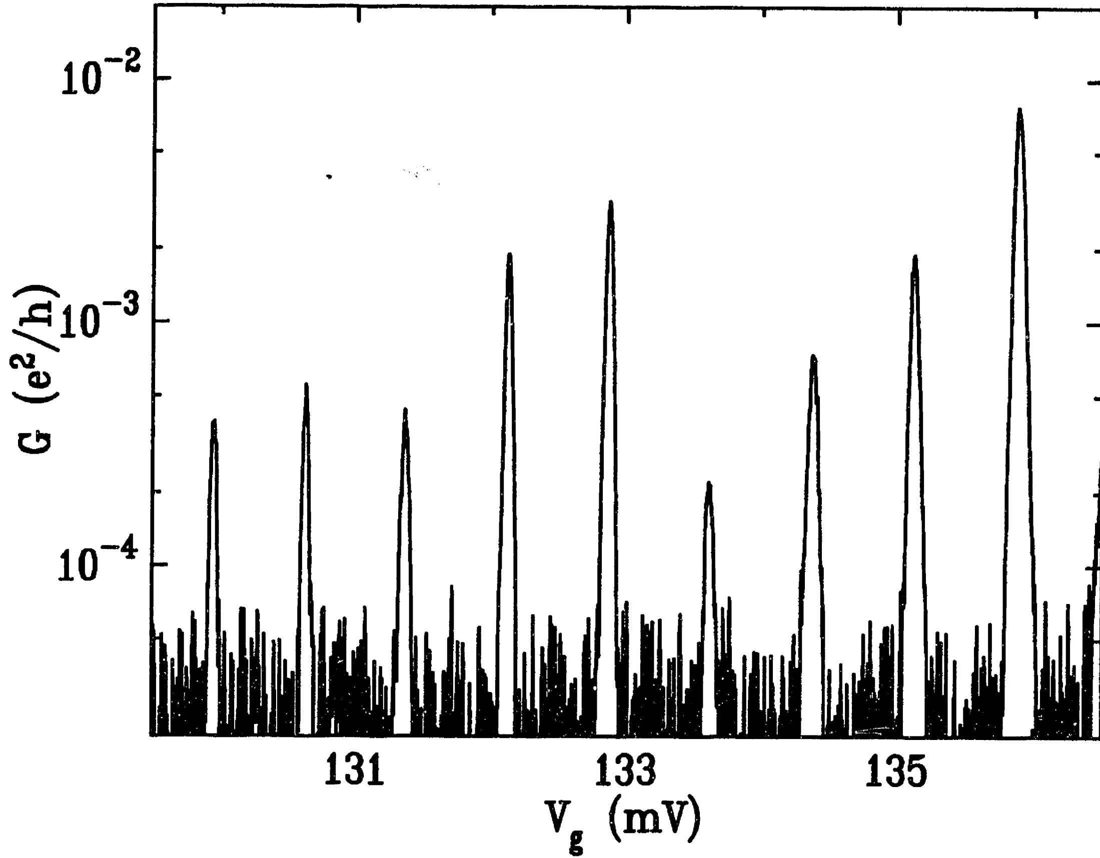

Figure 4-4: $G(V_g)$ showing Coulomb blockade for an artificial atom made in a GaAs/AlGaAs heterostructure. Here we see random variations in peak amplitudes from peak to peak as would be expected from theory [29, 39]. This random behavior should be contrasted with figure 4-3 where we saw an envelope function of the peak amplitude which varies slowly over many periods. In this device which was made by Udi Meirav and measured by David Goldhaber-Gordon and Olivier Klein, $U = .6\,\text{meV}$, and $\Delta\varepsilon = 50\,\mu\text{eV}$. Data taken at $T \approx .1\,\text{K}$, with a device of approximate lithographic size is $500\,\text{nm} \times 500\,\text{nm}$.

expected from theory [29, 39] in contrast to the data in figure 4-1.

The peak amplitudes in our data, however, have an envelope function which varies smoothly over large ranges in gate voltage which encompass many peaks. This would be explained if the conductance of one of the barriers were changing as a function of gate voltage. Since this device consists of two barriers in series we can test this idea by raising one of the barriers until the impedance of the device is dominated by that other barrier. In this way we can measure the conductance of a single barrier as a function of upper gate voltage. Such a measurement is easy to make because our devices have been fabricated with independent control over each of the barriers; by changing the voltage on the left pair of lower gates (see figure 2-1 gates 1 and 2) we can independently tune the height of the left barrier. In figure 4-5 we see a trace where the left barrier has been raised so that it now dominates the impedance through the

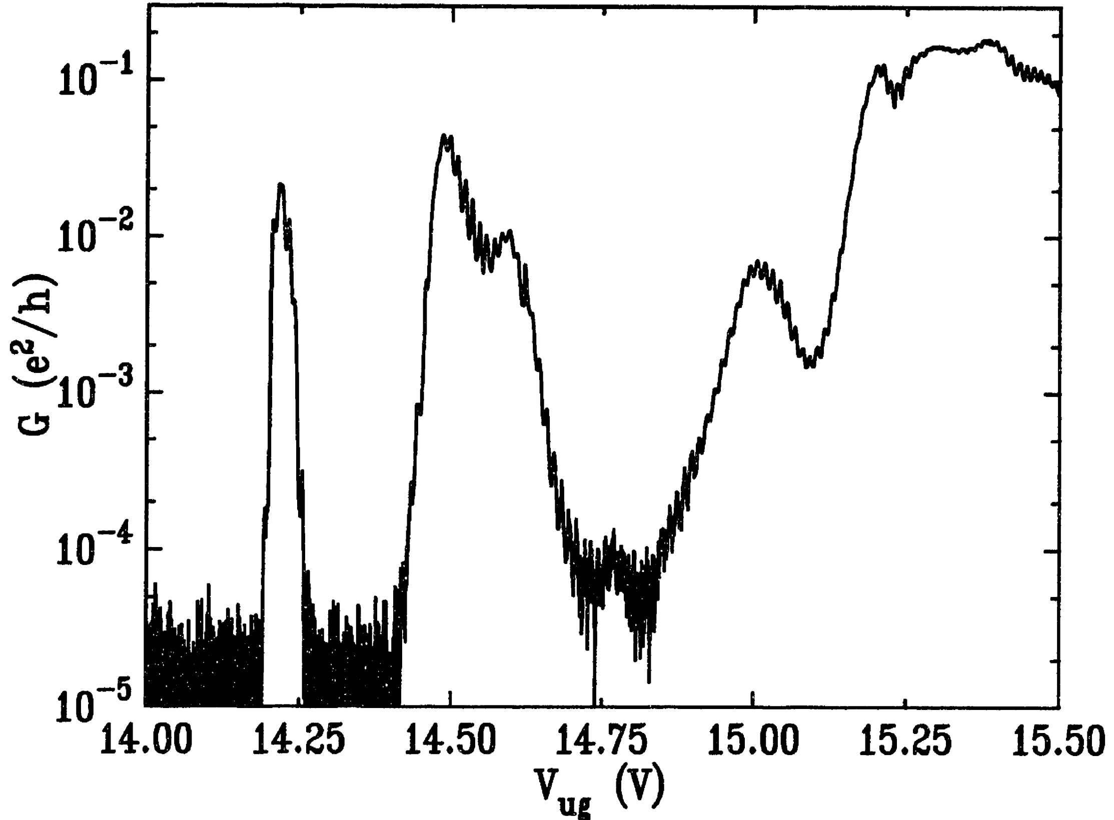

Figure 4-5: $G(V_{ug})$ for same device as shown in figure 4-1 but with the left barrier raised so that it dominates the conductance of the device. While remnants of Coulomb blockade oscillations with period $\approx 13\,\mathrm{mV}$ can still be seen the main modulation of the conductance has a spacing of $\approx 250\,\mathrm{mV}$. This modulation is due to the dependence of the conductance of the left barrier on the upper gate voltage. Data taken at $T = .32, \mathrm{K}$, $V_l = -8.0\,\mathrm{V}$, $V_r = -8.0\,\mathrm{V}$, with a V_l which is $-3.5\,\mathrm{V}$ lower than in figures 4-1 and 4-3. Device F30 wafer #13 has a gate geometry that is an isosceles triangle of height 50 nm, with 150 nm gap.

device. While there are remnants of the Coulomb blockade oscillations with a period of $\approx 13\,\mathrm{mV}$, the main modulation of the conductance has a spacing of $\approx 250\,\mathrm{mV}$. By comparing figures 4-3 and 4-5 it is clear that the envelope of conductance oscillations in figure 4-3 is due to variations of the transmission through the left barrier.

4.2 Conductance through a Single Barriers

In our device it is possible to study the transport properties through a single barrier. As discussed above this may be done by raising one barrier so that the other dominates the impedance (as that shown in figure 4-5). However it is also possible to bias one pair of lower gates so that they induce a metallic two-dimensional electron gas beneath them. In this way, the region that had been isolated into an artificial atom is now

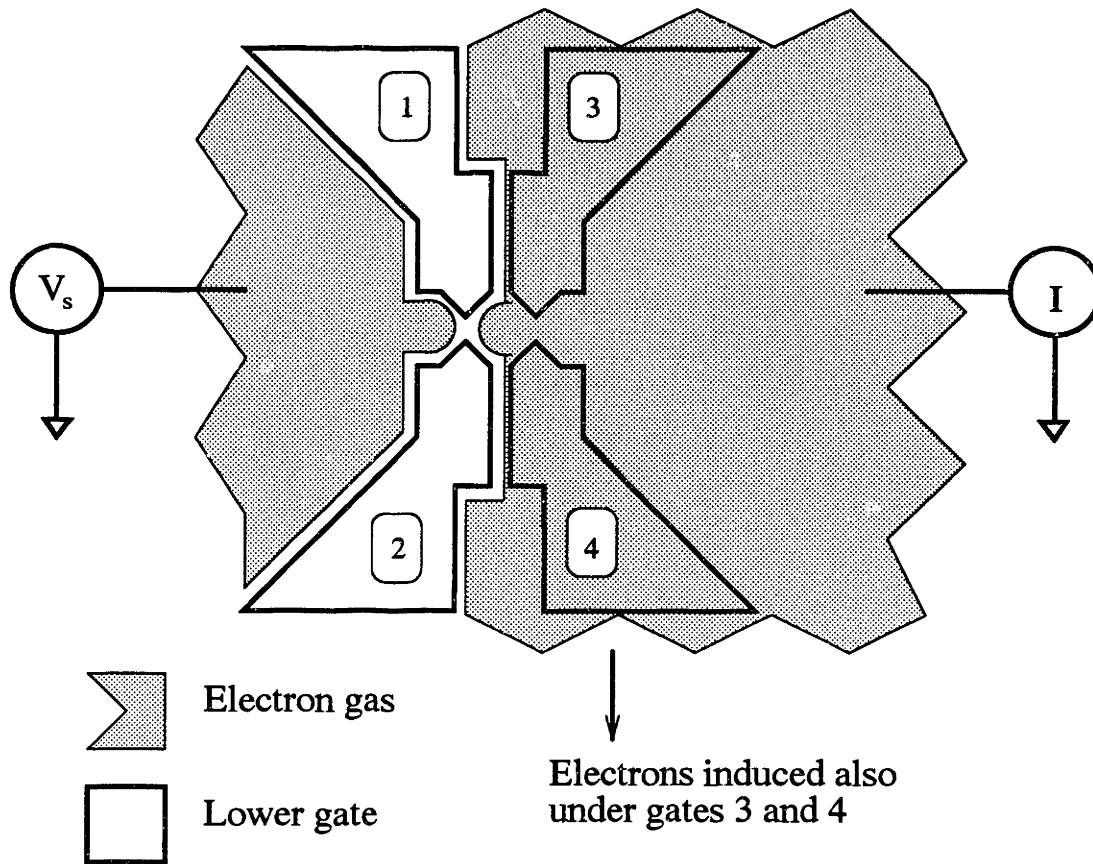

Figure 4-6: This figure shows a schematic top view of one of our devices with the lower gates biased so that we can study transport through a single barrier. In figures 2-1 and 3-1 we showed a similar schematic diagram, but there we biased the lower gates to create two barriers in series. The upper gate that induces the electron gas in the leads covers all the regions shown in this figure. In the configuration shown in this figure gates 1 and 2 are biased so that no electron gas is formed underneath them, while gates 3 and 4 are biased so that beneath them there is a metallic electron gas. Because the regions in the leads as well as under gates 3 and 4 are metallic the impedance of this device is dominated by the electrostatic barrier created by gates 1 and 2. By applying a bias across this barrier we can study its transport properties.

part of a large electron gas (see figure 4-6). Using this type of configuration we can be sure that electrons are not isolated between the two barriers. Any structure that is observed in the conductance traces can only be due to variations in the tunneling rate of the single remaining barrier. In figure 4-7 the same device we examined above is biased in this regime. The gate voltage scale of conductance changes is $> 100\,\mathrm{mV}$, confirming our notion that the the envelope of conductance oscillations observed in figure 4-3 is due to changes in the transmission through a single barrier.

The conductance trace observed in figure 4-7 is not the monotonic increase of conductance with gate voltage we had expected for a simple barrier (see section 3.2). While we claim that the conductance peaks are due to changes in the transmission

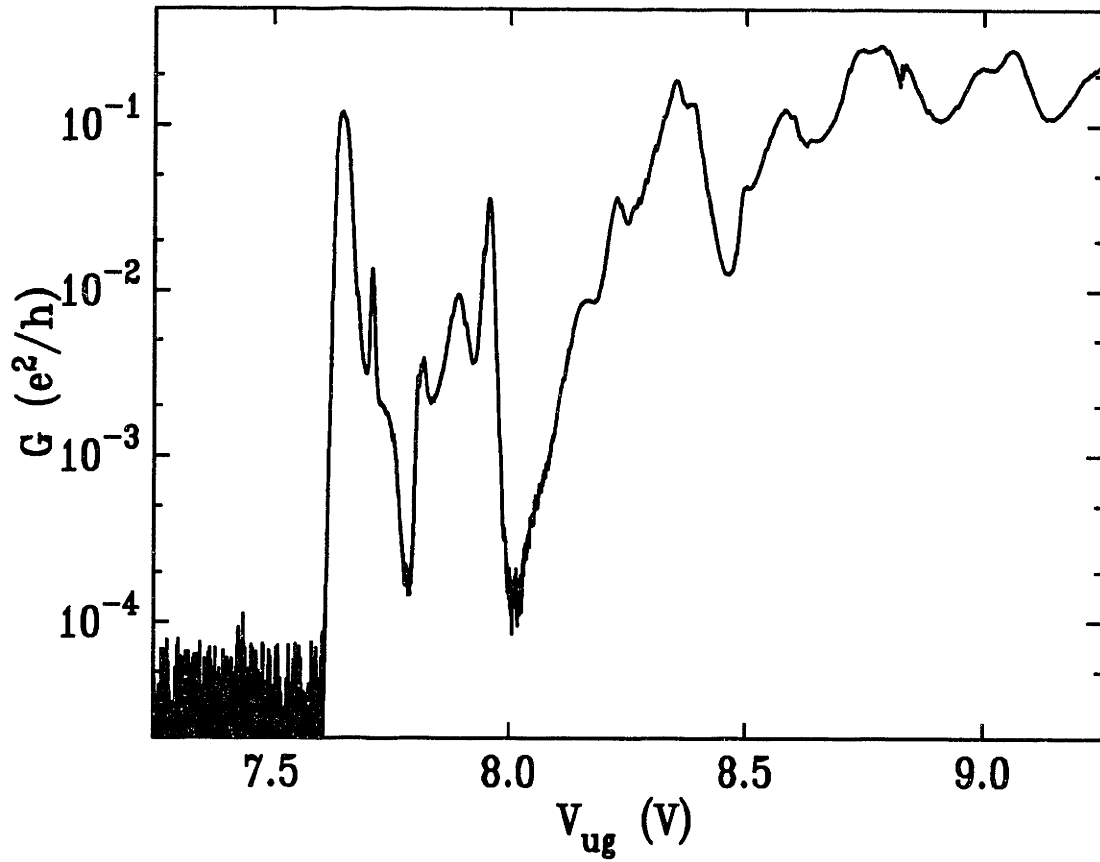

Figure 4-7: $V(V_{ug})$ for a single barrier. Here we have biased the lower gates so that the right pair of gates induces a metallic two-dimensional electron gas underneath; therefore the impedance is limited only by tunneling through the left barrier. Clearly the conductance through a single barrier has resonances. This is the same barrier as dominates 4-5. Data taken at $T = .32, \mathrm{K}$, $V_l = -1.5\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device F30 wafer #13. The gate geometry is an isosceles triangle of height 50 nm, with 150 nm gap.

through a single barrier, one may wonder whether they could be due to a parasitic conduction path under the region covered by the lower metal gates (gates 1 and 2 in figure 4-6). This worry, however, may be discounted based on two observations. The first observation is that there is a monotonic correlation between the lithographic size of the gap between the lower metal gates and the upper gate voltage at which these resonances begin. The smaller the gap in the lower gates the higher an upper gate voltage is required for the onset of the conductance resonances[3] (for more details see section 6.2.1). The second observation is that the conductance peaks have a capacitance to the confining gate that is twenty times larger than to the "open" gate

[3]This is true for a fixed lower gate voltage. Of course the onset depends strongly on lower gate voltage. A more complete statement of the observation would be: the smaller the gap in the lower metal gates the more the threshold for conductance oscillations shifts with changes in the lower gate voltage. However this observation is stated the conclusion remain the same.

which has the electron gas beneath it (see section 6.1.1). From this we may conclude that the conductance path is spatially located in the region between the lower metal gates, and that we are not seeing parasitic conductance under the lower metal gates.

It is clear from the conductance traces that the probability for an electron to tunnel through the barrier is enhanced at specific energies. While this does not occur in a conventional tunnel barrier (see section 3.2) it will occur if there are bound (or quasi-bound) states that exist within the barrier. Then transport can occur by tunneling resonantly through these states, and the conductance will be enhanced at specific energies. We believe that the states bound inside the barrier are due to fluctuations in the impurity potential in the barrier region. Our hypothesis is confirmed by the large changes in the structure of these resonances when the device is thermally cycled (see section 6.2.3); thermal cycling, as discussed above, effectively rerandomizes the impurity potential, and thus will change features that are due to potential fluctuation and to disorder. Furthermore, based on our observations in section 2.2 we expect there to be a density of localized states of $\approx 3 \times 10^{11}\,\mathrm{cm}^{-2}$. Using this density we estimate the number of localized states we would expect in a barrier of $50\,\mathrm{nm} \times 50\,\mathrm{nm}$ to be 8. Thus we expect that there should be many localized states through which we may tunnel resonantly. The rest of this thesis focuses on measuring and trying to understand the the nature of these states.

4.3 Coulomb blockade in a Single Barrier

By studying the transport properties of a single barrier we may learn a great deal about the electronic states trapped inside the barrier. In chapter 3 we developed the idea that the transport properties could be used to probe the electronic states of a variety of different systems; in particular we showed how transport spectroscopy could be used to probe the electronic states localized in an artificial atom(see section 3.1). Here we extend these techniques to the study of the localized electronic states inside a barrier. We begin by focusing on one particular barrier whose study demonstrates the fruitful nature of the analogy between the states localized in a barrier and the states of an artificial atom. After our study of this device, chapter 5 focuses on various models we can use to explain the states in a single barrier. In particular it will focus on our peculiar observation that many single barriers, including the one discussed below in this section, show equally spaced conductance resonances. Chapter 6 then focuses on the measurements of many different single barrier devices. However we have chosen to begin our discussion of conductance in a single barrier by focusing

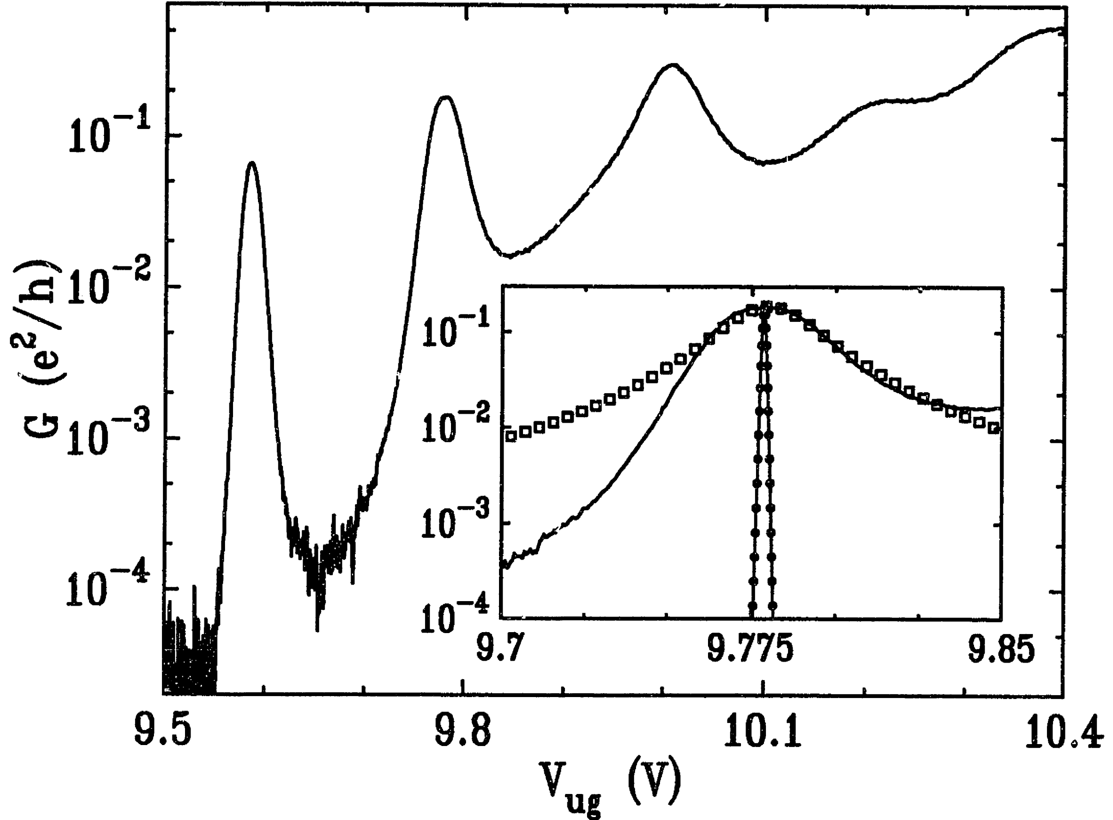

Figure 4-8: Conductance versus gate voltage for one barrier. The conductance shows equally spaced peaks reminiscent of Coulomb blockade with $U = 15\,\text{meV}$. The inset compares the second peak (solid curve) with the width of the derivative of the Fermi-Dirac function (small circles connected by line) showing that the conductance peak is not thermally broadened; rather we are measuring the natural line width. Since we are measuring the natural peak-shape we expect that the resonance will be fit by a Lorentzian. The squares are a Lorentzian, and while they fit one one side of the peak they highlight the asymmetry of the peak-shape. Data taken at $T = .32\,\text{K}$, $V_r = -2.448\,\text{V}$, $V_l = +1.0\,\text{V}$ on G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

on a specific device because it illustrates the parallels between the study of artificial atom that we have developed thus far and the study of states localized in a single barrier.

4.3.1 Conductance versus Gate Voltage

First let us discuss the measurement of the conductance versus gate voltage for a single barrier. Examining the conductance trace in figure 4-8, there are 3 clear peaks in the conductance; there are also two additional modulations in the conductance at higher gate voltages. Taking the three peaks and the two modulations of conductance as features, our first important observation is that the spacing between these five

features is uniform. While there are not enough oscillations to discuss whether these peaks are "periodic", the even spacing suggests that we might try interpreting these conductance oscillations as Coulomb blockade; we will in fact analyze these data using this picture. It is also encouraging to note that the overall conductance of both the peaks and the valleys is rising as a function of increasing gate voltage. This overall trend is what we would expect as the barrier is pulled down with increasing gate voltage.

By examining how the conductance trace depends on temperature we can learn about the nature of these conductance resonances. In addition we expect the broadening of the conductance peaks with temperature will allow us to convert the gate voltage scale into an energy scale following the analysis of section 3.1.4. In figure 4-9a we see that the width of the peak at $V_{ug} = 9.8\,\mathrm{V}$ increases linearly with increasing temperature. Using equation 3.15 we determine from these data that $\frac{C_g}{C_\Sigma} = .08$ and that $\Gamma = 1.3\,\mathrm{meV}$. Since these measurement are being made at $T = .32\,\mathrm{K}$ ($k_BT = 28\,\mu\mathrm{eV}$) it appears that we are in a regime where $\frac{\Gamma}{k_BT} \approx 50 \gg 1$; this regime has not been well explored in previous experiments and is of great interest. Our measurement of the peak amplitude versus temperature seen in figure 4-9b confirm that $\Gamma \gg k_BT$ for our lowest measurement temperatures. In that figure we see that at low temperatures the amplitude of the peak is temperature independent as would be expected when measuring the natural lineshape ($\Gamma \gg k_BT$); at high temperatures when the peak-shape is dominated by thermal broadening ($\Gamma \ll k_BT$) the amplitude decreases like $A \propto \frac{1}{T}$. The crossover of the peak amplitude's functional form occurs when $k_BT \approx .4\Gamma$ and is consistent with numerical simulations; as expected the same crossover is seen in the amplitude of the peak at $V_{ug} = 9.6\,\mathrm{V}$. It should be noted, however, that the the crossover is much more abrupt than expected from numerical calculation of the convolution of a Fermi-Dirac derivative with a Lorentzian. In any case, using the value of $\frac{C_g}{C_\Sigma}$ obtained above, we plot the derivative of the Fermi function in the inset of figure 4-8 on the same scale as the conductance peak. It is quite clear from this plot that the conductance peak is not dominated by thermal broadening but rather that we are measuring the natural lineshape of the resonance.

Since each conductance resonance is due to another bound state being occupied in the barrier, we can use the value of $\frac{C_g}{C_\Sigma}$ to convert the gate voltage spacing between peaks into an addition energy, U. Just as in the case of the artificial atom, U is a measure of the electron-electron interaction of states bound in the barrier. We find that $U = 15\,\mathrm{meV}$ which is a very large energy and corresponds to $175\,\mathrm{K}$; we would thus expect that the conductance oscillations would persist to a high temperature.

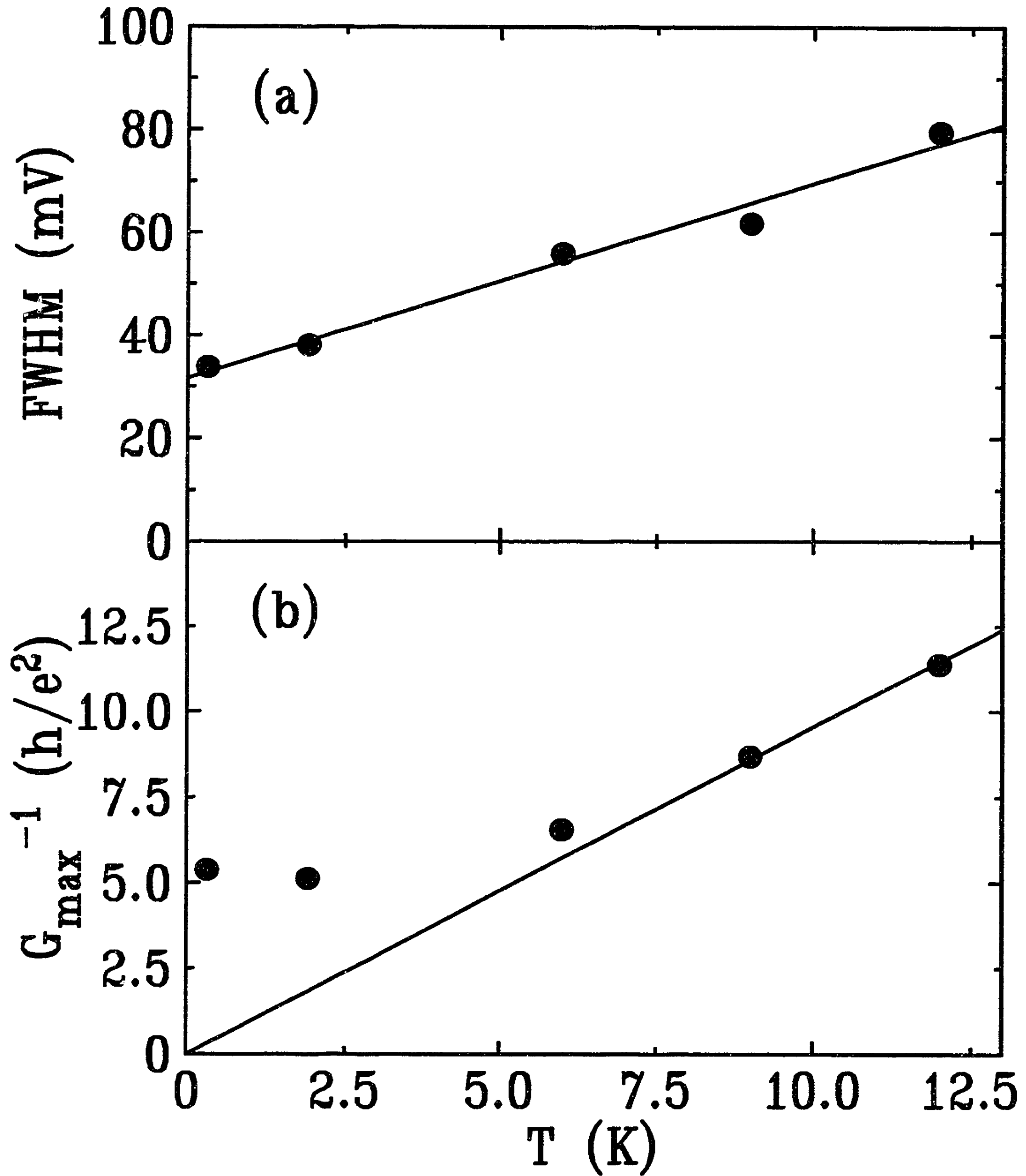

Figure 4-9: Temperature dependence of second peak at $V_{ug} = 9.8\,\mathrm{V}$) in figure 4-8. In panel (a) we see the full width at half maximum (FWHM) plotted as a function of temperature. From this measurement we find $\frac{C_g}{C_\Sigma} = .08$ and $\Gamma = 1.3\,\mathrm{meV}$. While in panel (b) we see the inverse of the peak amplitude G_{max}^{-1} as a function of temperature. The high temperature behavior is dominated by thermal broadening and is expected to follow $\propto T^{-1}$ while at low temperatures the peak is dominated by its natural lineshape and the amplitude saturates.

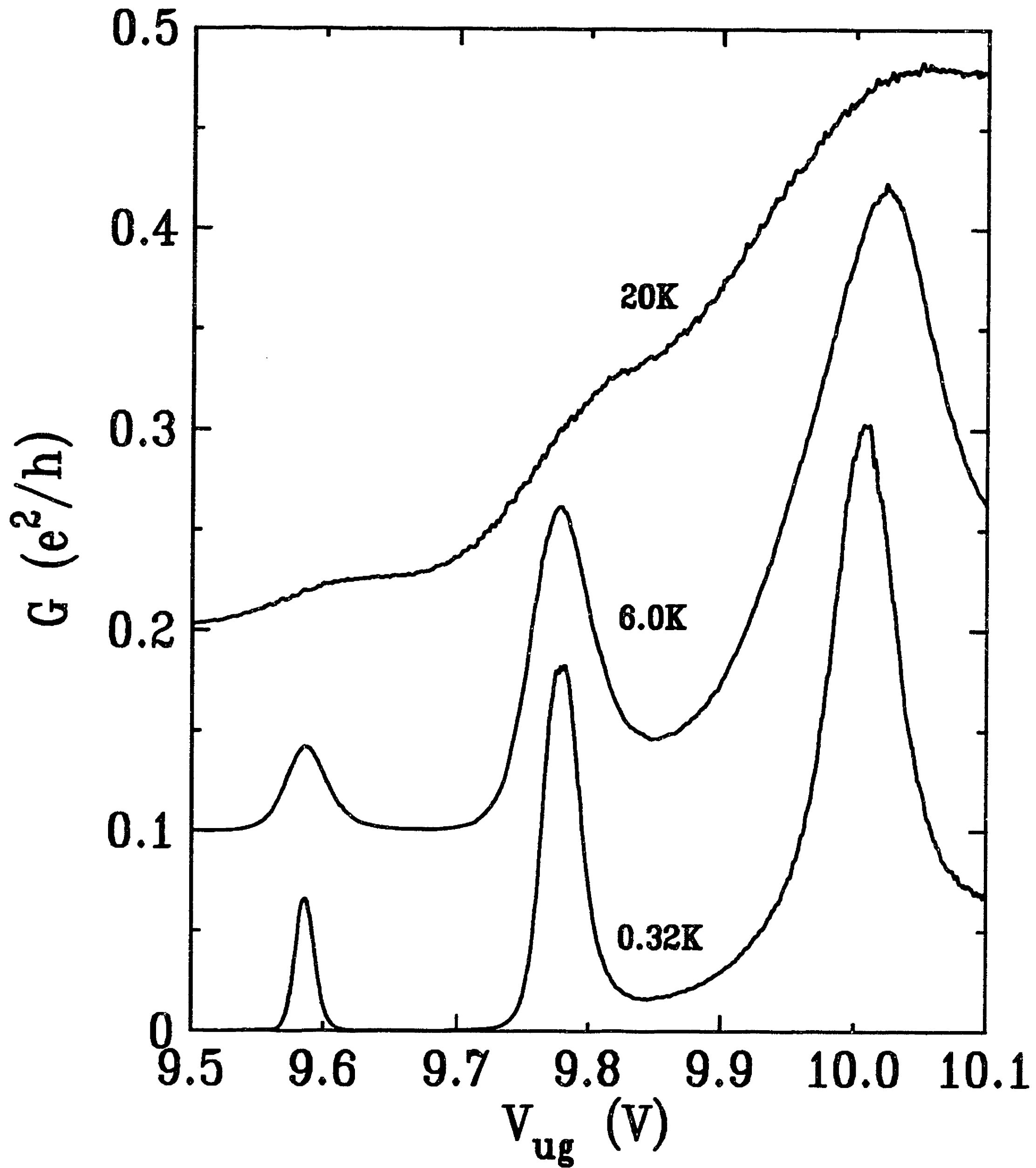

Figure 4-10: $G(V_{ug})$ at three different temperatures for single barrier shown in figure 4-8. We see that at 6 K the conductance peaks are well defined, while even at 20 K there is a remnant modulation of the conductance. This is consistent with Coulomb blockade with an addition energy of 15 meV. The curves are offset by .1 $\frac{e^2}{h}$ from each other for clarity. Data taken at temperatures noted in figure. For other details see caption of figure 4-8.

In figure 4-10 we plot the conductance versus gate voltage for $T = .32\,\mathrm{K}$, $6.0\,\mathrm{K}$, and $20\,\mathrm{K}$. The conductance oscillations are still well defined at $6\,\mathrm{K}$ and an equally spaced modulation of the conductance persists even up to $20\,\mathrm{K}$. Since the observation of Coulomb blockade peaks requires $k_B T < \frac{U}{5}$ the temperature dependence is consistent with our interpretation of these conductance peaks as being due to Coulomb blockade[4] with $\frac{U}{k_B} = 175\,\mathrm{K}$. If we now naively assume that this charging energy is due to a metallic puddle of electrons localized in the barrier, we may estimate the size of the puddle using equation 4.2. We find that $r = 22\,\mathrm{nm}$ using the average dielectric constant, $\epsilon_a v = 6.8$ or $r = 13\,\mathrm{nm}$ if we use the silicon dielectric constant $\epsilon_{Si} = 11.9$. Again, as in section 4.1.1, we expect that the size estimated using this formula will be an overestimate. While we do not understand the genesis of this metallic puddle of electrons, its size is quite reasonable to be localized within a barrier of $50 - 100\,\mathrm{nm}$ in size.

4.3.2 Tunneling Spectrum

We now turn our attention to a measurement of the tunneling spectrum from which we hope to determine the excitation energy $\Delta\varepsilon$ of the states localized in the barrier. In analogy to probing the states of an artificial atom (see section 3.1.3), the measurement of the differential conductance reveals the density-of-states of electrons localized in the barrier; the excitation energy $\Delta\varepsilon$ is then a measure of the spacing between states with a fixed number of electrons, and label them "exc" in figure 4-11. The differential conductance of the barrier is shown in figure 4-11 for $V_{ug} = 9.68\,\mathrm{V}$ which is at the minimum between the first and second conductance peaks and therefore in the middle of the Coulomb gap. We begin by observing a gap of $21\,\mathrm{mV}$ in the differential conductance around zero bias, as would be expected for Coulomb blockade. In addition there are several features in the differential conductance whose spacing is reproducible; we associate these features with tunneling through excited states with a fixed number of electrons. To convert the voltage on the source into an energy we must take into account the capacitive coupling between the source and the electronic states in the barrier as discussed in section 3.1.3; this scaling factor between source-voltage and energy will be the larger of $\frac{C_s}{C_\Sigma}$ or $1 - \frac{C_s}{C_\Sigma}$. Since we know the size of U from the measurements of $G(V_{ug})$, we find that the appropriate conversion factor is 0.75. We now find $\Delta\varepsilon = 4\,\mathrm{meV}$ by multiplying this scaling factor by the spacing of the excited states as seen in the tunneling spectrum.

[4]See for example figure on page 181 of reference [12].

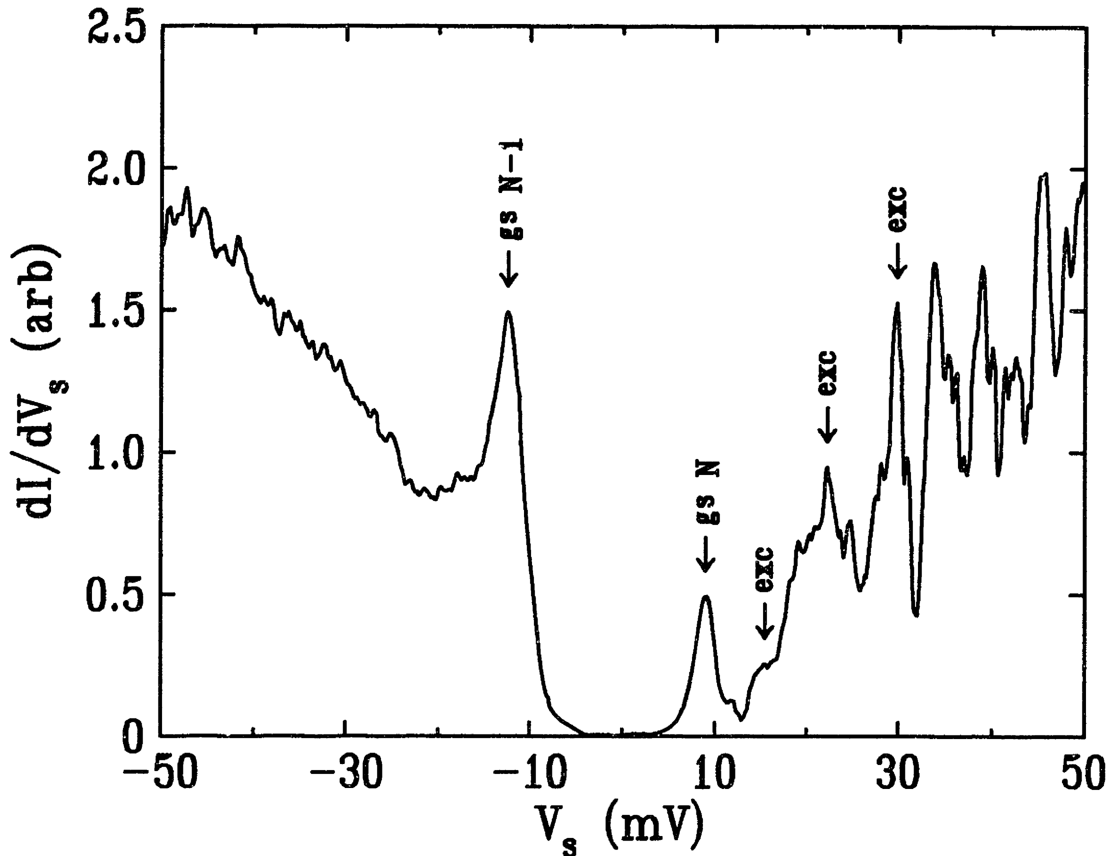

Figure 4-11: Differential conductance for the single barrier shown in figure 4-8. The differential conductance, or tunneling spectrum, is a measure of the density-of-state of the electrons trapped in the barrier. This trace is taken with $V_{ug} = 9.68\,\mathrm{V}$ which is right between the first and second conductance peaks, and thus we observe a Coulomb gap of 21 mV around zero-bias which corresponds to an energy of 15 meV. Tunneling into the ground-state of the N ($N-1$) electrons gives rise to the peak labeled "gs N" ("gs $N-1$"). The other reproducible features are ascribed to tunneling into excited states and are labeled "exc"; by converting their spacing into energy we find $\Delta\varepsilon = 4\,\mathrm{meV}$. Data taken at $T = .32\,\mathrm{K}$, for other details see caption of figure 4-8.

This value of the excitation energy is nearly two orders of magnitude larger than that measured in GaAs devices and is consistent with confinement of the electrons to a very small area within the barrier. We may estimate the area, A, to which the electrons are confined by assuming that it is determined by the density-of-states $N(E)$ and the excitation energy $A = \frac{1}{N(E)\Delta\varepsilon}$. This assumption takes advantage of the fact that the density-of-states in two dimensions is independent of the energy and the exact nature of the confining potential, and thus the kinetic energy spacing between states depends only on how tightly they are confined. we find[5] that an area $A = 160\,\mathrm{nm}^2$ or a radius of $r = 7\,nm$. The size estimated in the method is much smaller than the $r = 13 - 22\,\mathrm{nm}$ estimated from the charging energy. While we are not sure what causes this discrepancy, we know that our calculation of the size based on the charging energy is an overestimate because neglecting other conductors tends to overestimate the size of the capacitor. In addition the states localized in the barrier are very strongly coupled to the leads, a point which will be discussed in detail below. This strong coupling will increase quantum fluctuations of the charge which in turn renormalizes the capacitance [53]. This correction will also decrease the charging energy and therefore tend to overestimate the size of the artificial atom.

4.3.3 Collapse of Coulomb blockade

We now return our attention to the width of the conductance peaks in our measurements of $G(V_{ug})$. As was noted previously our measurement of the temperature dependence of the peaks showed convincingly that the peaks are not dominated by thermal broadening, and that we are therefore measuring the natural lineshape of the conductance resonances. In figure 4-12 we use dark circles to plot $\frac{\Gamma}{\Delta\varepsilon}$ as a function of upper gate voltage; Γ is taken from the width of the conductance peaks in figure 4-8, while $\Delta\varepsilon$ is assumed to be a constant and is taken from the measurement shown in figure 4-11. It is clear from figure 4-12 that the three conductance peaks have an exponentially increasing Γ. Assuming that Γ is determined by lifetime broadening then we would expect just such an exponential increase in the tunneling rate as the barrier to tunneling on and off of the artificial atom is pulled down by increasing the gate voltage.

To understand the significance of the quantity $\frac{\Gamma}{\Delta\varepsilon}$ we turn to a scaling argument

[5] Using the density-of-states for a two-dimensional electron gas, $N(E) = g\frac{m}{2\pi\hbar^2} = 1.59 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{meV}^{-1}$, where m is the band mass of the electron, and g is the degeneracy due to spin and valley quantum numbers.

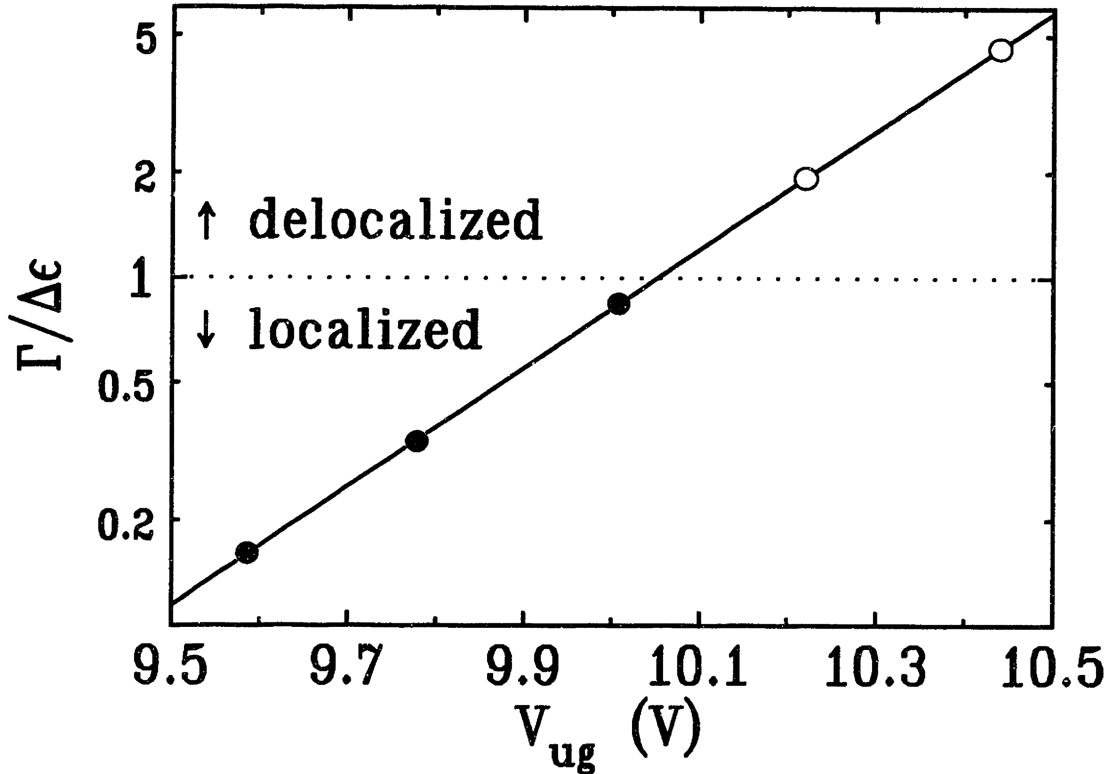

Figure 4-12: This figure shows the change in $\frac{\Gamma}{\Delta\epsilon}$ as a function of V_{ug} for the five conductance features shown in figure 4-8. The three solid points are obtained by from the width of the three peaks in figure 4-8, and show that the peaks have a width, Γ, that is increasing exponentially with gate voltage; such an exponential increase would be expected for lifetime broadening of the states of an artificial atom as the barrier is lowered. If this exponential growth were to continue then the two features at $V_{ug} = 10.2\,\mathrm{V}$ and $V_{ug} = 10.45\,\mathrm{V}$ would have a $\frac{\Gamma}{\Delta\epsilon} = 1.9$ and 4.5, respectively. The Thouless scaling argument discussed in the text argues that the states are delocalized when $\frac{\Gamma}{\Delta\epsilon} > 1$. As the states delocalize Coulomb blockade, which requires charge localization, collapses. Thus we expect the observed Coulomb blockade peaks when $\frac{\Gamma}{\Delta\epsilon} < 1$. In addition, we interpret the modulations in gate voltage at $V_{ug} = 10.2\,\mathrm{V}$ and $V_{ug} = 10.45\,\mathrm{V}$ as the remnants of Coulomb blockade in this nearly delocalized regime. Data taken at $T = .32\,\mathrm{K}$, for other details see caption of figure 4-8.

due to Thouless [54] which argues that for electrons to be localized $\frac{\Gamma}{\Delta\epsilon} < 1$. Intuitively we can understand this argument by considering a box of size L^d in which an electron may be located. Upon solving Schrödinger's equation in that box we will find a series of eigenstates whose average separation is $\Delta\varepsilon(L)$. By considering how quickly an electron in one of these eigenstates escapes from the box we can find the width of each eigenstate due to lifetime broadening; this lifetime broadening, $\Gamma(L)$, is known as the Thouless energy and can be defined even in the case of diffusive electron motion. When $\Gamma(L) > \Delta\varepsilon(L)$ then the electron escapes quickly, the electronic states are strongly mixed with the continuum, and the electron is not localized within the box. Because the electrons are not localized in the box the solutions to Schrödinger's

equation will depend on the boundaries and consequently on the arbitrary size of the box we have chosen. If however $\Gamma(L) < \Delta\varepsilon(L)$ then the electrons are localized within the box and the solutions to Schrödinger's equation will not depend on the size of the box. Thus by considering how $\Delta\varepsilon(L)$ and $\Gamma(L)$ evolve as a function of box size L^d we may define the localization length ξ such that $\Gamma(\xi) < \Delta\varepsilon(\xi)$.

We see in figure 4-12 that for the three conductance resonances that we observe we have $\frac{\Gamma}{\Delta\varepsilon} < 1$. We recall that in figure 4-8 there were two additional modulations in the conductance positioned in gate voltage where we might have expected conductance peaks if the peak spacing remained constant. If we take the position associated with the first of these conductance modulations $V_{ug} = 10.2\,\mathrm{V}$ and we assume that Γ continues to grow exponentially as a function of gate voltage then we can ask what value of $\frac{\Gamma}{\Delta\varepsilon}$ we would have expected for a resonance at $V_{ug} = 10.2\,\mathrm{V}$. We find that we might have expected a value of $\frac{\Gamma}{\Delta\varepsilon} = 1.9$, while for the feature at $V_{ug} = 10.45$ we would have $\frac{\Gamma}{\Delta\varepsilon} = 4.6$. Therefore we would not expect electrons to remain localized with such strong coupling to the extended states in the leads. Since it is the quantization of charge in a specific area that leads to the suppression of current in the Coulomb blockade we expect the blockade to collapse when $\frac{\Gamma}{\Delta\varepsilon} > 1$. Since the delocalization transition is not sharp in this small sample we interpret the modulations of the conductance that we see in figure 4-8 as the remnant of Coulomb blockade as the states become more and more delocalized. It is noteworthy that the conductance modulations at high gate voltage in figure 4-8 resembles those in the 20 K curve of figure 4-10; in both cases charge fluctuations are washing out the charge quantization that leads to the Coulomb blockade. While in one case these fluctuations are quantum mechanical in nature and in the other they are thermal in nature; the conductance curves nonetheless resemble each other.

4.3.4 Lineshape

Having determined that we are measuring the natural lineshape in figure 4-8 we would expect to find a lifetime broadened Lorentzian lineshape. The finite temperature lineshape should be given by the convolution of the derivative of the Fermi-Dirac function with the natural lineshape (equation 3.12); as noted on page 50 if the peak is lifetime broadened then we expect that the natural lineshape of the resonance $g(\varepsilon)$ to be given by the Lorentzian form (equation 3.14) which states $g(\varepsilon) \propto \frac{\Gamma/\pi}{(\varepsilon-\varepsilon_0)^2+\Gamma^2}$. While the third peak at $V_{ug} = 10.0$ is asymmetric is appears to have has Lorentzian tails, as expected. The tails of the first peak at $V_{ug} = 9.6\,\mathrm{V}$ do not appear to be

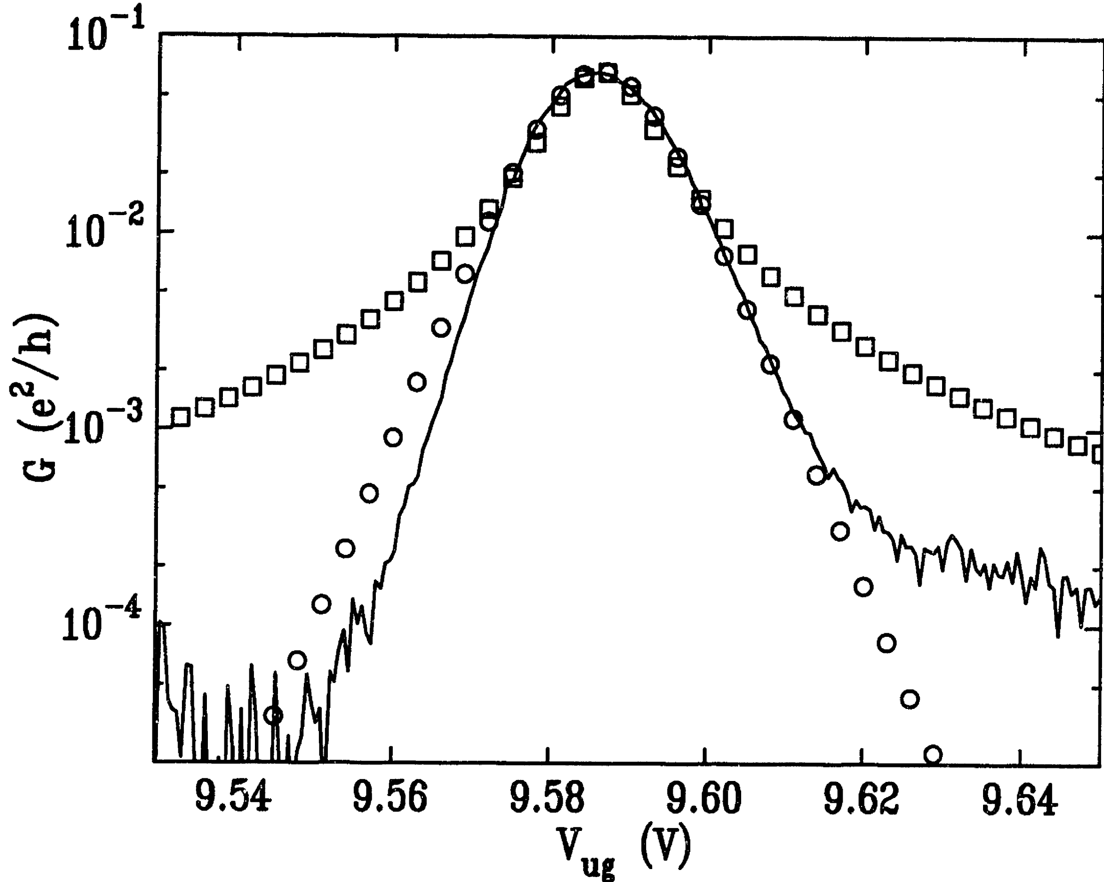

Figure 4-13: Detail of the lineshape of the first peak in figure 4-8. The solid curve is the data, while the expected lineshape, a thermally broadened Lorentzian, is plotted by squares. Based on the temperature dependence of the peak width (equation 3.15), we have set $\Gamma = 552\,\mu$eV and $k_BT = 27.5\,\mu$eV, and multiplied all values by $\frac{C_\Sigma}{C_g}$ to plot in gate voltage units. The circles, which fit the peak much better than the squares, are a fit to a Fermi-Dirac function. However the temperature obtained from the fit is 13 times larger than expected from the sample temperature and corresponds to 4.3 K. Data taken at $T = .32$ K, for other details see caption of figure 4-8.

Lorentzian, but rather appears to be like the derivative of the Fermi-Dirac function.[6]

In figure 4-13 we show a more detailed view of this peak. We have attempted to fit the peak with a thermally broadened Lorentzian and plotted this fit using open squares. In this fit we use $\Gamma = 552\,\mu$eV and $T = .32$ K which we determine from the temperature dependence of the width of the conductance peaks (see equation 3.15). Clearly this functional form does not account for the shape of the peak despite our expectation that when $\frac{\Gamma}{k_BT} = 20$ the peak would be dominated by a natural peak shape which is Lorentzian. We have also fit this peak to the derivative of a Fermi-

[6]On a semilog plot the tails of the two functions should look differently. The Lorentzian which has a power law decay $\propto E^{-2}$ should show curvature on a semilog plot. The derivative of the Fermi-Dirac, which has exponential tails, should look like a straight line on a semilog axis.

Dirac function which is plotted in open circles. This function fits the conductance well over more than two orders-of-magnitude, however the temperature obtained from the fit is 13 times higher than the temperature of the electrons. The only deviation from this fit is due to the asymmetry of the peak. It should be stressed that this fit to the Fermi-Dirac derivative has only three adjustable parameters: the height, the width, and the location of the peak; nonetheless it fits the peak very well. The peak at $V_{ug} = 9.8$ has a shape that can be fit on at least one side by a Lorentzian. In the inset of figure 4-8 we have plotted a Lorentzian with the appropriate Γ in open squares. The failure of the Lorentzian to fit on the low gate voltage part of the peak highlights the peak's asymmetry. All of the peaks in this device, and many of the ones examined in section 6.1.2, are asymmetric despite the fact that both the expected lineshapes are symmetric. As discussed above in section 4.3.3, Γ changes exponentially as a function of V_{ug}, and thus we would expect that the tunneling rate would be higher on one side of the peak than on the other leading to an asymmetry. Fitting the peaks to a series of Lorentzians whose width, $\Gamma(V_{ug})$, is growing exponentially according to the functional form we found in figure 4-12 does not account for the lineshape. Thus the nature of the asymmetry in this device remains a mystery.

In summary, while it is clear from our analysis that we are measuring the natural lineshape of these conductance resonances, we do not understand the shape of the peaks. We have tried but failed to account for the asymmetry by simply assuming it is due to a coupling that is gate voltage dependent. Our most surprising finding is that the first peak has the shape of a thermally broadened peak but with an apparent electron temperature 13 times higher than the actual temperature of the electrons. These deviations from a Lorentzian lineshape indicate that the decay channels can not be characterized by a simple lifetime decay of the quantum state. It is possible that the role of interactions in tunneling has changed the natural lineshape [36]. Whatever their genesis, the lineshapes of the conductance resonances remains a mystery.

4.4 Other Single Barriers

We wish to conclude this chapter by reviewing the observations that we have made thus far. We found that we observed Coulomb blockade when an artificial atom was formed by electrostatically isolating electrons between two barriers. Ours was the first observation of Coulomb blockade in an electrostatically confined artificial atom in a silicon MOS system. This is what we had originally set out to measure when we began the work described in this thesis. We saw that even in one of our larger

lithographic structures we obtained addition energies several times larger than those that had been previously studied in our group. Furthermore we found that, in contrast to our expectations, the conductance through a single barrier is not monotonically increasing as a function of gate voltage. Rather there are conductance resonances due to the tunneling of electrons through a single barrier.

In section 4.3 we found that the conductance through a single barrier could be understood as tunneling resonances due to a small metallic puddle of electrons trapped in the barrier. This puddle of electrons behaves like an artificial atom in many regards. The conductance is dominated by Coulomb blockade giving rise to equally spaced conductance peaks. The temperature dependence of these conductance peaks shows that at the lowest temperatures the peaks are not dominated by thermally broadening. This is consistent with very strong coupling between the localized states of this electron puddle with the extended states in the leads. Measurements of the tunneling spectrum further bolster this picture. In particular we gain confidence in this picture by a careful comparison of $\frac{\Gamma}{\Delta\epsilon}$ to the Thouless scaling theory. Throughout this analysis we have seen the utility of using the concepts of an artificial atom to understand the conductance resonances in a single barrier.

However it must be stressed that conductance traces of most single barriers can not be interpreted so simply in terms of Coulomb blockade. For example the conductance trace shown in figure 4-7 can hardly be said to consist of equally spaced conductance peaks. The phenomenon of conductance peaks in a single barrier, however, is general. We have measured more than 35 devices over a wide range of voltages and *every* single barrier in all measurement configurations shows conductance resonances. In addition such resonances are observed in a variety of other material systems by a number of workers (see section 5.1); many of those observations show equally spaced conductance peaks. The rest of this thesis is devoted to a study of resonances in a single barrier; we will consider various models that try to account for these resonance and present a selection of experiments which characterize them. Most of the discussion uses the framework and terminology of artificial atoms both because this framework has proven itself to be useful, and because the framework can be easily generalized to the study of transport through a small number of localized electronic states. In the end we hope to use our short length-scale transport studies to further elucidate the nature of the localized states that exist at the band edge.

Chapter 5

Models of Conductance in a Barrier

This chapter discusses various models for conduction resonances in a single barrier. In chapter 3 we considered transport though localized states of an artificial atom (section 3.1) as well as considering transport through a single barrier (section 3.2). In that chapter we found that conductance resonances are characteristic of a system where there are localized states between the source and drain; we therefore expected such resonances when studying artificial atom, but not when studying a single barrier. However, in chapter 4 we saw that in the devices we are studying there are conductance resonances that occur in a single barrier; we deduced that these conductance resonances are due to the presence of localized states trapped by disorder within the barrier. By extending the techniques we used to study the localized states of an artificial atom to the study of the localized states in a single barrier we were able to learn a great deal about the nature of the states localized in a barrier (section 4.3). In fact, we even found that the states localized in a barrier had equally spaced peaks and behaved much like the artificial atoms that can be formed in double barrier structures.

Given this background, this chapter focuses on various models that can be used to understand the localized states in a single barrier. In particular we focus on how the electrons may be trapped within a barrier, a region that should otherwise be devoid of electronic states. We begin by summarizing the findings of other researchers, and discuss the widespread observation in many different material systems of conductance resonances in single barrier devices (section 5.1); we pay particular attention to the spacing of the conductance peaks that is reported by other workers. We then consider the possibility that the electrons are trapped within a barrier by their attraction to

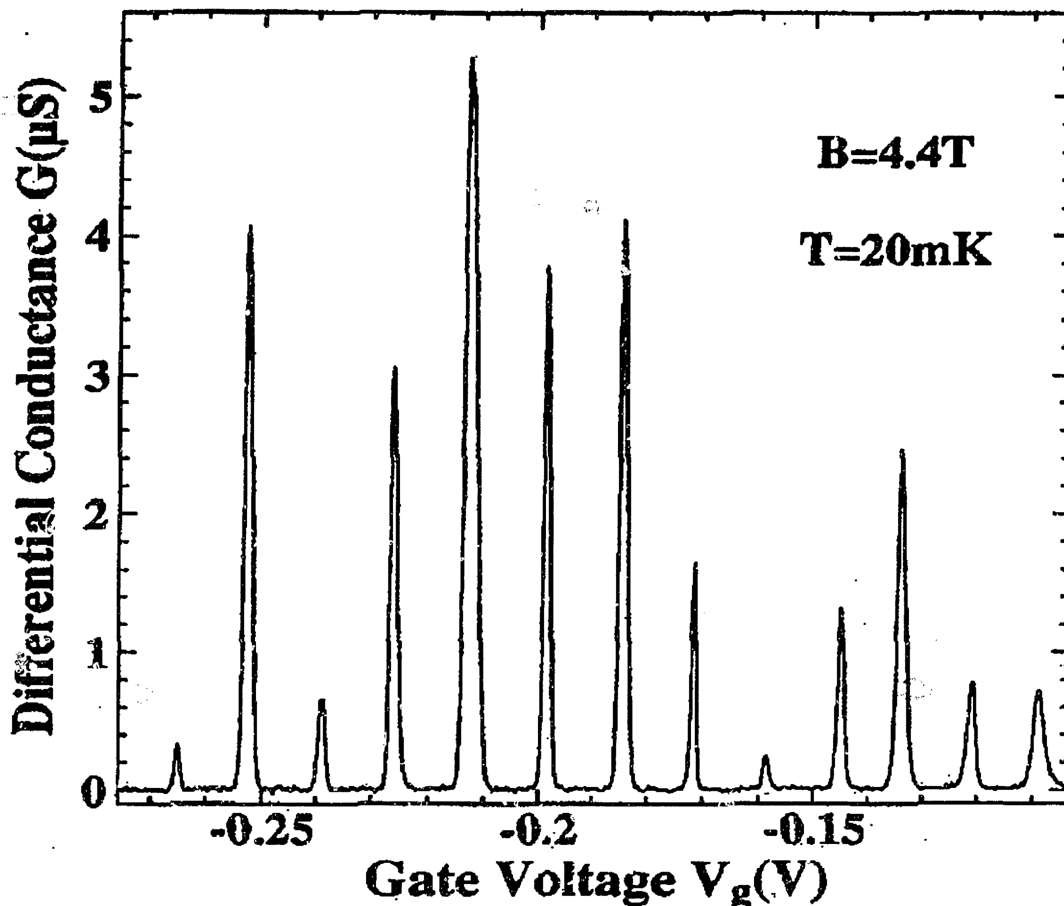

Figure 5-1: This figure shows a plot from Nicholls *et al.* [1] showing peaks number 15 – 27 of the equally spaced peaks that they observe in a single barrier fabricated in a GaAs/AlGaAs heterostructure. The gap in the gates that creates this barrier is approximately 300 nm in the direction of current flow and 300 nm across; its other properties are discussed in the text.

the image charges they induce in nearby metallic regions (section 5.2). Finally we turn our attention to various different ways in which the disorder potential can localize charges in a barrier (section 5.3). We consider the peak spacing predicted by the various models and find that none of them are able to account for the equally spaced resonances that we have observed (sections 4.3 and 6.2.4) and that are observed by others (section 5.1). We conclude this chapter by presenting a novel alternative explanation, which we call "electron puddles", to explain the presence of metallic regions trapped within a barrier (section 5.3.4). Chapter 6 then presents a detailed experimental study of the devices we have fabricated in light of the models that we have considered in this chapter.

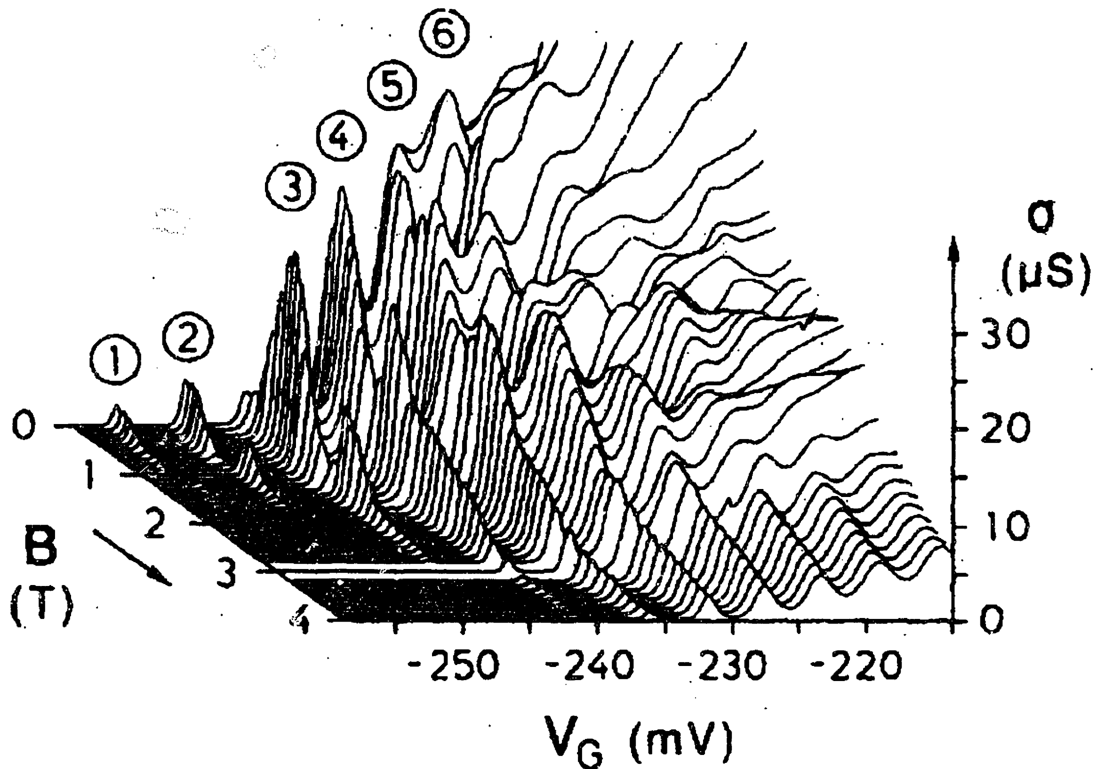

Figure 5-2: This figure shows a plot from Weis *et al.* [2] showing 10 periodically spaced peaks from a single barrier in a GaAs/AlGaAs heterostructure. The gap in the gates that creates this barrier is approximately 150 nm in the direction of current flow and 500 nm across; its other properties are discussed in the text.

5.1 Background Work

Despite our naive conception that a barrier should be devoid of localized electronic states, there have been numerous reports of tunneling resonance in single barriers [1, 2, 55, 56, 57, 58, 59, 60, 52, 51, 61]. These reports are not limited to one semiconducting material system, but rather are found in all the most carefully studied systems: silicon MOS systems [55, 56, 57, 59, 52, 61], GaAs/AlGaAs heterostructures [1, 2, 58], and in Si/SiGe heterostructures [60]. The important point is that the phenomenon of localized states in a barrier is general, and not limited to one set of devices or to one material system. The behavior at the conductance threshold is of technological interest, as is the nature of localized states in these systems.[1] Similarly from a basic

[1]The following technological case serves as an example of the importance of these localized states. Currently a major goal in the electronics industry is to lower the power required for operating various digital electronics so as to increase their ability to run on batteries. To lower the power consumption one must lower the voltage at which the devices are operated. This requires that the transistors used be capable of turning from "on" to "off" with a smaller change in gate voltage ΔV_g. The

physical perspective the widespread observation of this phenomenon suggests that its nature is general and worthy of further study.

We wish to focus our attention on two particular experiments from the literature. In both of these experiments equally spaced conductance resonances are observed in a single barrier. In the first experiment, shown in figure 5-1, Nicholls *et al.* [1] report that when studying a barrier created by electrostatic depletion of a a low density electron gas they observe more than 27 equally spaced conductance peaks.[2] They interpret these conductance oscillations as being due to Coulomb blockade in an artificial atom and calculate that the electrons are confined to 80 nm based on the capacitance of the artificial atom. In addition they claim the observation of equally spaced conductance peaks is observed for many different samples. The second experiment by Weis *et al.* [2] reports 10 equally spaced conductance peaks (see figure 5-2); this experiment is also performed in GaAs/AlGaAs barrier created by electrostatic depletion.[3] Weis *et al.* also interpret their observations in terms of Coulomb blockade, and estimate that the size of the artificial atom is 150 nm. Their device is noteworthy because its length[4] (in the direction of current flow, or the x-axis of figure 5-3) is $\approx$ 150 nm which is much shorter than its width of $\approx$ 600 nm giving it an aspect ratio that quite unlike a one-dimensional channel. Like Nicholls, Weis *et al.* report that they have made similar observations in many different devices. Finally we note that in both the work of Kopley *et al.* [57] and Takahashi *et al.* [52] there are equally spaced conductance resonances in a silicon MOS system with only one intentional barrier.[5]

We conclude that equally spaced conductance resonances occur in a wide variety of different systems. This conclusion is more restricted than our previous observation that conductance resonances in single barriers are ubiquitous. We will see below

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conductance threshold which we have been studying is the region between "on" and "off" which must be minimized to allow operation of digital electronics at lower voltages [18, p. 446]. Therefore an understanding of these localized states is of great interest.

[2]In GaAs/AlGaAs heterostructures a technique similar to one we showed in figure 2-1b is used to create a barrier by electrostatic depletion. In such a structure there is no upper metal gate as in figure 2-1, but rather the doping in the structure induces an electron gas at the GaAs/AlGaAs interface. The gates patterned with electron-beam lithography (in our system called "lower metal gates") are used to selectively deplete the electron gas. The size of the gap in Nicholls' gates is 300 nm $\times$ 300 nm and the gates are 80 nm above the plane of the electron gas. The sheet density in these devices is a low $5 \times 10^{10}\,\mathrm{cm}^{-2}$ with a mobility of $50,000\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$.

[3]The gates in this device are 86 nm above the plane of the electron gas. The sheet density in these devices is a moderate $3.4 \times 10^{11}\,\mathrm{cm}^{-2}$ with a mobility of $600,000\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$.

[4]Based on sketches shown in figure 1 of reference [2].

[5]Takahashi *et al.* observe more than 20 equally spaced conductance resonances. They believe that in their system electrons are confined by the shape of the Si/SiO_2 boundary. We have cited their work in the context of conductance resonances in a single barrier because the exact nature of their system is not known, and it may be related to the phenomenon we are considering.

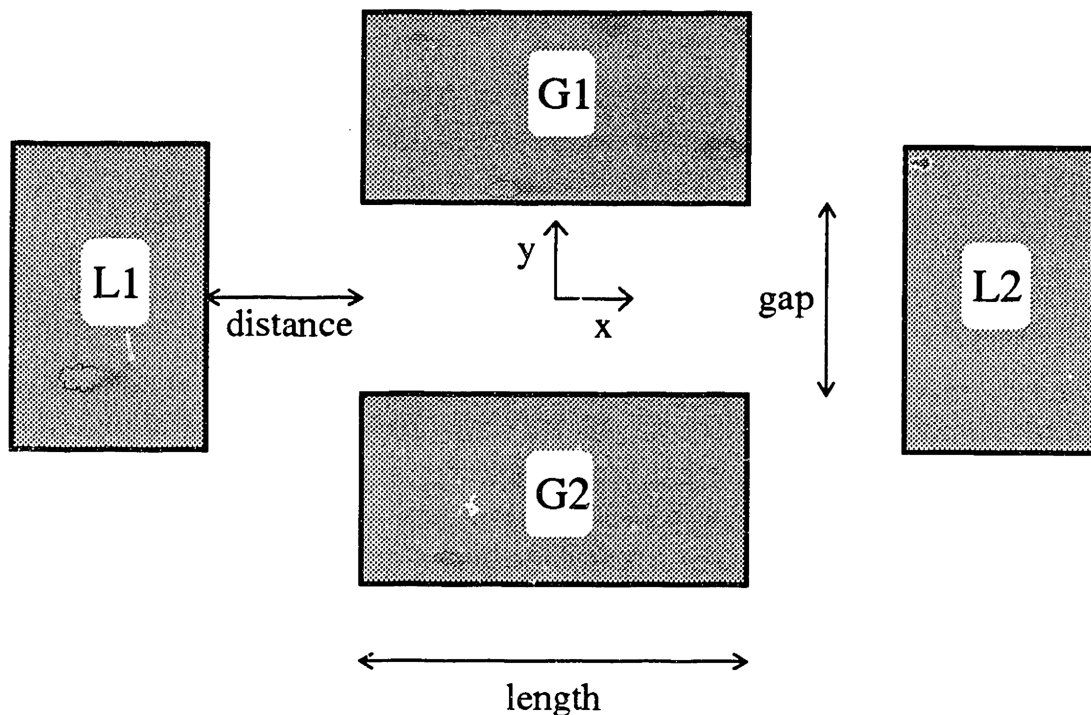

Figure 5-3: This figure shows the geometry for which we consider image charge trapping of electrons. The four nearby conductors in our device (see figure 4-6), consists of two leads (L1 and L2) and two lower metal gates (G1 and G2), and are considered to be perfect conductors. When an electron is placed in the barrier region between G1 and G2 it will induce image charges on all four conductors. These charges attract the electron and lower its energy. The shape of the image charge contribution to the potential energy depends on the values of the distance between the gates and the leads, d, the length of the gate region, l, and the gap between the gates, g. Under certain conditions the minimum of potential energy along the x-axis will be at the center of the barrier, thus giving rise to "image charge trapping".

in section 5.3.4 that such equally space resonances only occur when the electronic states trapped in a barrier form a single metallic region. That such metallic regions are commonly seen suggests that there is a compelling physical explanation for their formation.

5.2 Image Charge Trapping

An electron in the vicinity of a metal will induce an image charge that will attract the electron towards the metal. In the device that we have been studying[6] the single barrier that contains localized states is formed by biasing two metallic gates (see appendix B or figure 4-6); as an electron gets closer to the barrier the image charge it induces in the gates increases. If the attraction of the induced image charge is strong

[6]Such a configuration is also present in the work of Nicholls *et al.* [1] and Weis *et al.* [2].

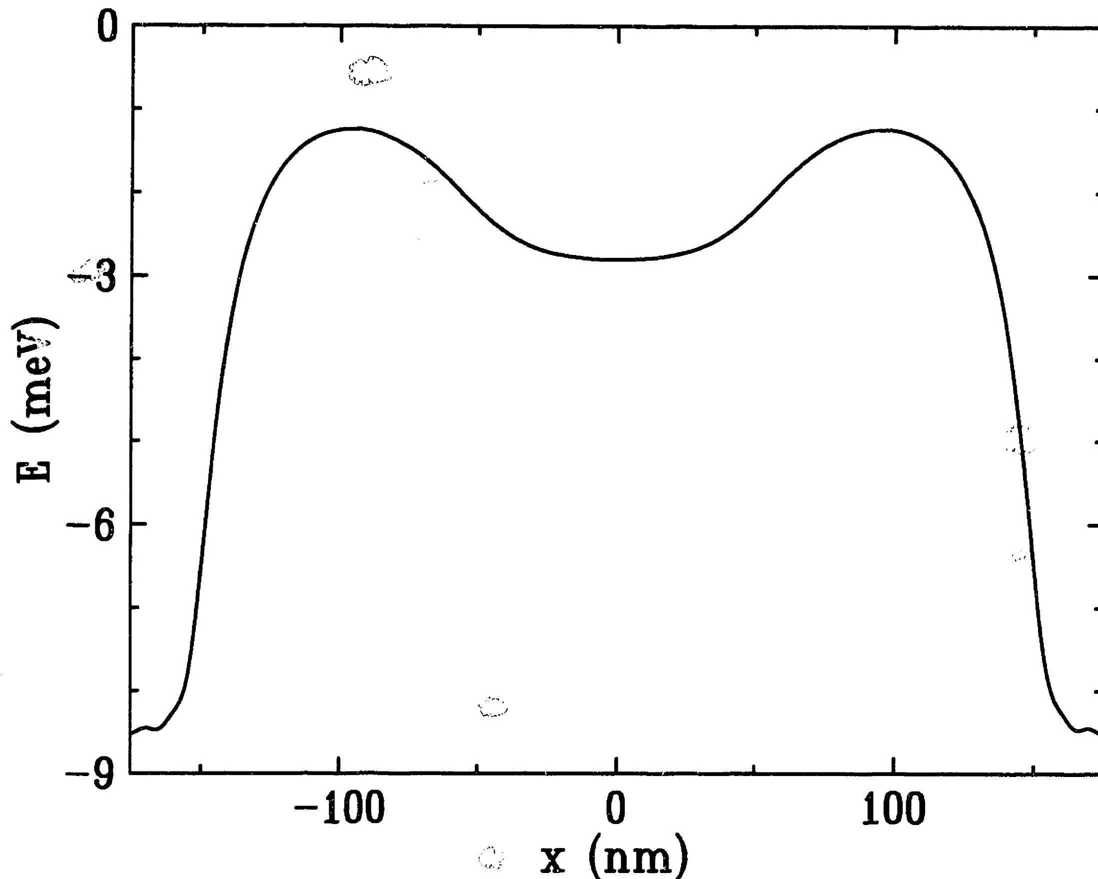

Figure 5-4: This figure shows the potential energy of a test electron placed in the barrier region. As the electron is moved along the x-axis its potential energy is lowest at $x = 0$ where it experiences the maximum attraction from the charges induced on the gates, G1 and G2 (see figure 5-3). In this figure the distance between the leads and the barrier is $d = 100$ nm, the length of the gate region is $l = 100$ nm, and the gap between the gates is $g = 50$ nm. The trapping energy for this configuration is 1.6 meV.

enough, an electron may be trapped in the barrier region. It has been suggested [62] that such "image charge trapping" may explain the electronic states that we have found to be localized within a single barrier. In this section we consider this possibility; while we will find that such an explanation does not adequately explain the the observation of states localized within a barrier, it does help us better understand the shape of the barrier.

We begin the discussion by clearly defining the geometry we will use to consider this problem. In figure 5-3 we show the geometry of the four conductors in which image charges will form. For the sake of illustration we have considered only the two leads (L1 and L2 in the figure) and the two lower metal gates and have neglected

the upper gate.[7] All four of these metallic regions are considered to be perfect conductors in the analysis that follows. We will then be interested in the energy of a test electron placed in the plane of the four conductors. The shape of the potential profile will depend on the separation of the four conductors. The important distances are the distance between the leads and the gates, d, the length of the gate region, l, and the gap between the gates, g (see figure 5-3). Some of the details of how the calculation is carried out are discussed in appendix C; here we focus on the results of the calculations. In the simulations we present below $l = 100\,\mathrm{nm}$, and $g = 50\,\mathrm{nm}$, while we vary d.

In figure 5-4 we see that as an electron is moved along the x-axis there is a energy minimum in the middle of the barrier region. As discussed above, the energy of an electron is reduced as it approaches a conductor and is attracted to the induced image charge. The energy of the electron will be at a minimum at the point of closest approach; for a path along the x-axis this attraction produces a minimum at the point $x = 0$. For this reason the energy of the electron will also be lowered as it approaches the leads at $x = \pm 150\,\mathrm{nm}$.[8] Similarly we see in figure 5-5 that the energy of the electron will be lowered as it moves along the y-axis towards the gates at $y = \pm 25\,\mathrm{nm}$; therefore the point at $(0,0)$ is not a minimum of the potential in the plane but rather a saddle point with a minimum in the x direction and a maximum in the y direction. This fact highlights a crucial feature of this simulation: we have not included any bias on the gates relative to the leads.

In the our experiment we must bias the lower gates negatively with respect to the leads if we are to repel electrons and create a barrier. This negative bias will give rise to a background potential that is independent of the contribution from the induced charge; the total potential will be the sum of two independent contributions, one from background potential and the other from the induced charges. The background potential will, in general, be a saddle point in the plane of the Si/SiO_2 with

[7]The effect of the upper gate is relatively small because it is 100 nm above the plane of the Si/SiO_2. Because of this large separation the fraction of the test electrons' charge that is imaged by the upper gate will be small. Furthermore, because the upper gate covers the whole structure the contribution from the charge induced on the upper gate to the potential energy will not dependent strongly on the position in the plane of the Si/SiO_2; thus the image charge induced on the upper gate will not give rise to a force on the test electron. The case we consider in the text, which neglects the upper gate, demonstrates the effect of "image charge trapping" and maximizes the magnitude of the trapping.

[8]In the simulation presented in figures 5-4, 5-5 and 5-6 the conductors are all at $z = 0$ while the image charge is placed at $z = 10\,\mathrm{nm}$. We have chosen this elevation since the spacing of grid points in the simulation is $\Delta = 10\,\mathrm{nm}$. For details on the details of the simulation and the significance of Δ see the discussion in appendix C.

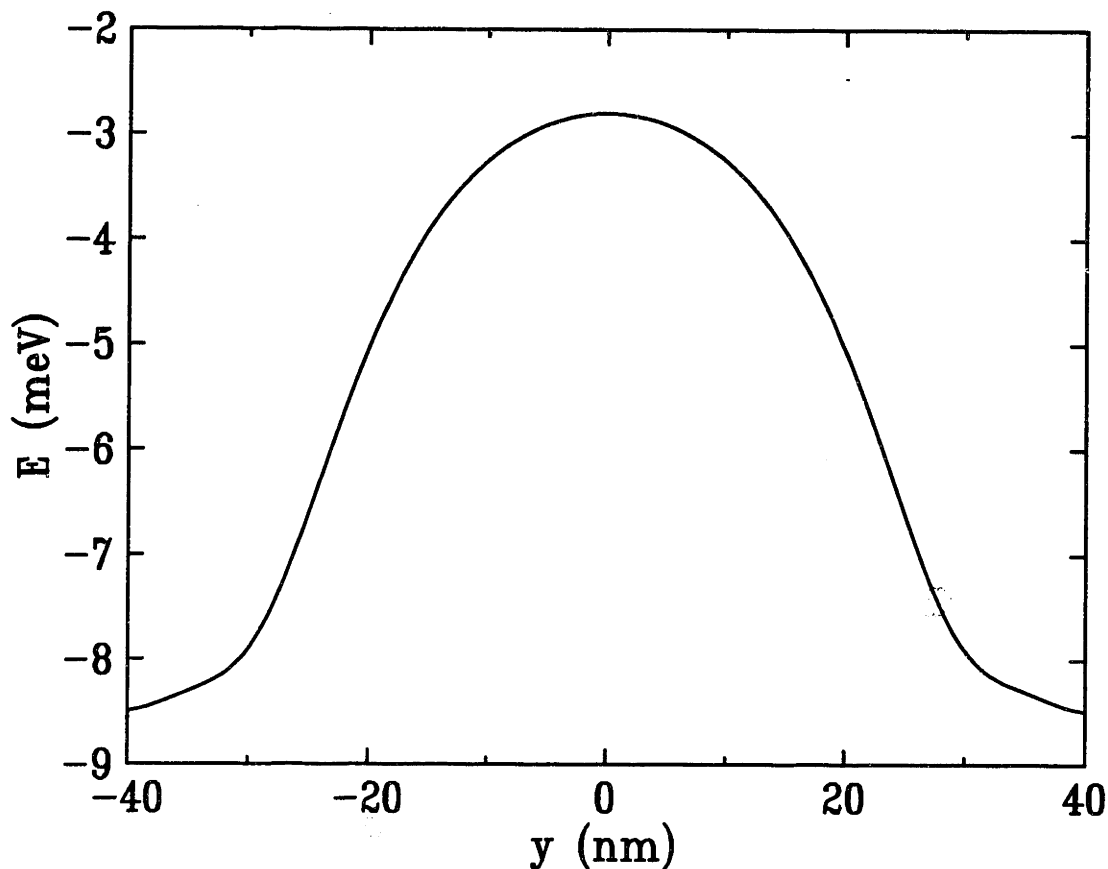

Figure 5-5: This figure shows the energy of an electron due to image charges as it moves along the y-axis. Because the gates G1 and G2 are grounded the electron is not repelled from them. Rather, the electron is attracted to image charges that form on the gates. This figure highlights our failure to include the background potential that repels the electrons from the lower metal gates. This background potential is a saddle point in the Si/SiO_2 plane with a minimum along the y direction and a maximum in the x direction. The background potential in the x direction will tend to reduce the magnitude of image charge trapping. For the simulations shown here $d = 100\,\text{nm}$, $l = 100\,\text{nm}$, and $g = 50\,\text{nm}$.

a maximum in the x direction and a minimum in the y direction. When the barrier is formed there is no electrons gas beneath the lower metal gates, and we can be sure that the *total* potential is at a minimum along the y direction; the repulsive background potential has overwhelmed the attraction of the electron to the region beneath the lower gates. This same background potential will be at a maximum along the x-axis at $x = 0$; whether there remains a minimum in the total potential along the x-axis will depend on the relative shape of the two components. We can be sure that any minimum that remains along the x-axis will be reduced in magnitude from the value shown in figure 5-4. Conversely, if the background potential is steeper than the induced potential and there is no minimum along in the x-axis then the shape of the total potential will be flattened by the attraction of the electron to its images.

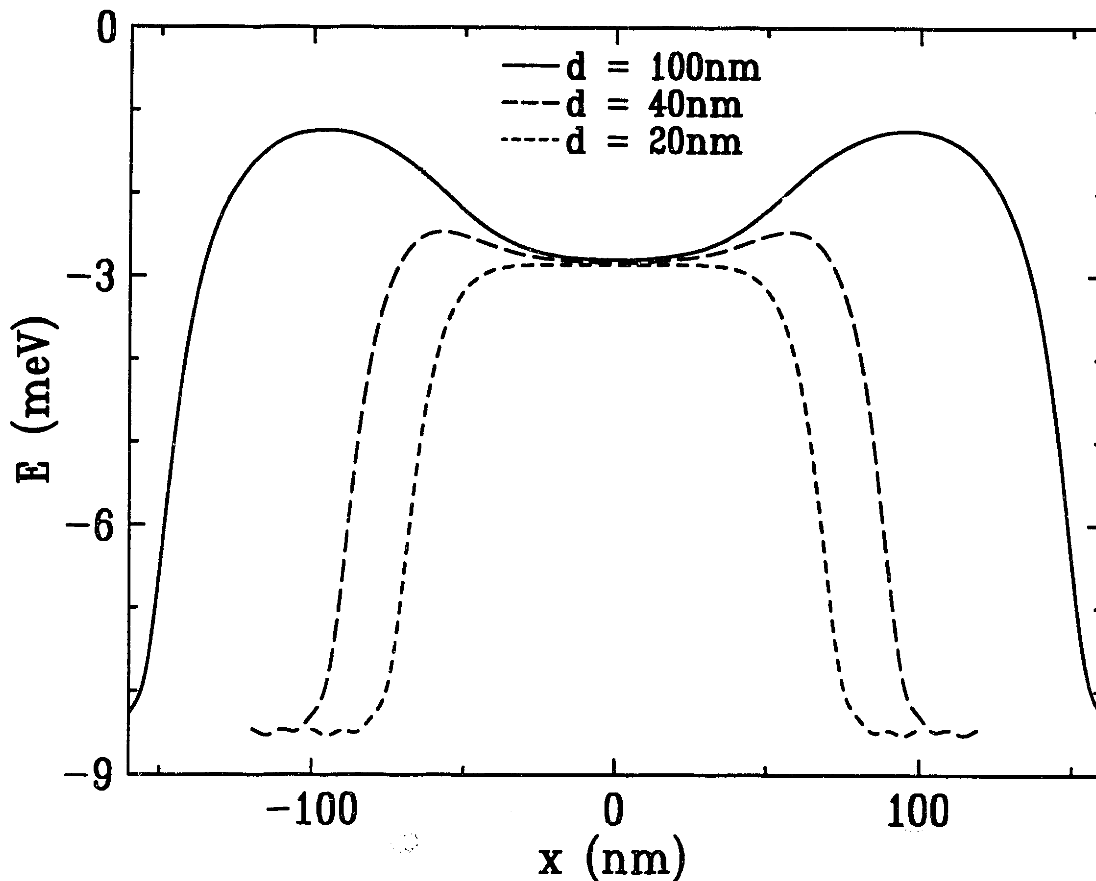

Figure 5-6: This figure shows how the magnitude of image charge trapping changes with the distance, d, between the leads and the gates. As the leads are moved closer to the gates the importance of the images induced in the leads increases. If $d = 100\,\text{nm}$ then $E_{trap} = 1.6\,\text{meV}$, if $d = 40\,\text{nm}$ then $E_{trap} = .37\,\text{meV}$, and if $d = 20\,\text{nm}$ then $E_{trap} = 4.2 \times 10^{-4}\,\text{meV}$. Since in our devices d is on order of 20 nm, the trapping energy will be much less than 1 meV.

Because the electron is attracted to the image charge formed in the leads as well as those formed in the gates the distance between the leads and the gates changes the magnitude of image charge trapping. In figure 5-6 we plot the potential energy of an electron along the x-axis for three different distances, d, between the leads and the gates (see figure 5-3). We clearly see that the magnitude of the image charge trapping is reduced as d is shortened and the attraction to the images induced in the leads become more important. The trapping energy, which we define as the difference between the maximum value of the energy along the x-axis and the energy at the origin $E_{trap} = E_{max} - E(x = 0)$, is a very sensitive function of d. For example in the configuration shown in figure 5-3 if $d = \infty$ then[9] $E_{trap} = 2.8\,\text{meV}$, if $d = 100\,\text{nm}$ then $E_{trap} = 1.6\,\text{meV}$, if $d = 40\,\text{nm}$ then $E_{trap} = .37\,\text{meV}$, and if $d = 20\,\text{nm}$ then

[9] If we remove the leads from the problem all together then $d = \infty$.

$E_{trap} = 4.2 \times 10^{-4}$ meV; thus E_{trap} is reduced dramatically by a factor of 880 as d is changed from 40 nm to 20 nm. In our devices d will depend on temperature, and gate voltage; we expect that it will be on order of 20 nm which is the thickness of the oxide separating the plane of the Si/SiO_2 and the lower metal gates. Therefore the maximum image trapping energy possible for our device is less than 1 meV.

We have found that while the attraction of an electron to nearby conductors will tend to create a energy minimum along the x-axis, this effect is unlikely to account for the trapping of electrons in a single barrier which gives rise to conductance resonances. We have seen that both the background potential and the image charges formed in the leads tend to lower or eliminate the ability of image charges to trap an electron in a barrier. However we have also seen that the attraction of the image charges will tend to flatten the shape of the barrier near its center.

5.3 Trapping by Disorder

Because of the experimental evidence that disorder plays an important role in trapping charges in the devices we are studying (see section 6.2.3) in this section we consider the various scenarios by which disorder my trap charge within a single barrier and give rise to the conductance resonances that we observe. In particular we will be concerned with the spacing of the conductance resonances that are predicted by various models of charge trapping. We will find that while various models can explain how disorder traps electrons in a single barrier, it is much more difficult to understand how electrons trapped in a single barrier are capable of forming the metallic regions necessary to observe equally spaced conductance resonances.

5.3.1 Localization by Repulsive Charges

A long, narrow conducting channel can be divided into smaller metallic regions by the presence of negatively charged impurities which locally depletes the electron gas and thus form tunnel barriers along the channel. If, by chance, there are only two such barriers then a conducting channel can be broken up and an artificial atom formed as shown in figure 5-7. This was the case in the work of Scott-Thomas *et al.* [46, 26] where equally spaced conductance oscillations were observed in a one dimensional channel. In fact, Scott-Thomas' experiments were the first to observe Coulomb blockade in a semiconductor structure. We would like to consider the possibility that such disorder is trapping the electrons within one of single barriers we have been studying.

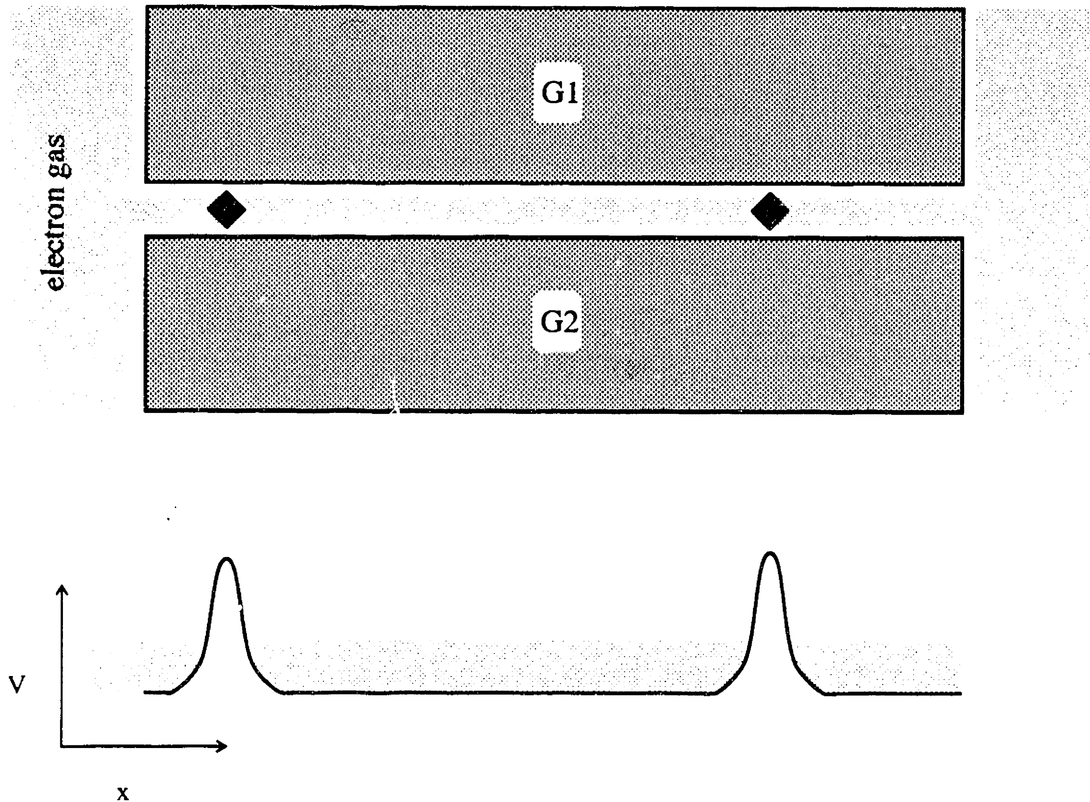

Figure 5-7: This figure shows a sketch of how repulsive impurities can divide a conducting channel and form an artificial atom. In the top part of the figure a narrow electron gas forms a conducting channel between two leads. If, however, two repulsive impurities (shown as black diamonds) happen to be located along the channel then they may form tunnel barriers and isolate an island of electrons; this structure is then an artificial atom. The bottom part of the figure shows a schematic potential diagram for the scenario shown in the top half of the figure.

For repulsive charges to isolate a conducting region the structure must be one dimensional in nature. If the width of the structure shown in figure 5-7 were larger than it length then one have to postulate a whole row of impurities replacing the single impurity in the figure; otherwise the electrons in the conductor could flow around the small regions where electrons were excluded by repulsive charges, and there would be a continuous conducting path from one lead to the other. Given the geometry of our structures (see appendix B) many of which have triangular gate tips (see figures B-2 and B-3) we must carefully consider the feasibility of this model for our system.[10] We also note that the same concern arises for the device used by Weis *et al.* has a width several times the length.

[10]Recall that *every* single barrier device we have measured shows conductance resonances. This is true regardless of geometry. See for example the conductance oscillations shown in figure 6-24 which are from a device with the gate geometry shown in figure B-3.

To assess the feasibility of repulsive charges isolating an electron gas in our devices we begin be computing the curvature of the conduction band as we move along the line between the two lower metal gates. At the Si/SiO_2 interface, under one of the lower metal gates, the Fermi level will be in the valence band[11] while between the lower metal gates the Fermi level will be at the edge of the conduction band.[12] Thus we may be certain that the bands bend by approximately the band gap, $E_g = 1.17\,\mathrm{eV}$, in the distance between the channel and the gates, $\frac{g}{2}$; assuming that near the minimum this bending is parabolic we may find the curvature of the band, K, in our device. Next we consider the shape of a potential of a unit charge, e, place above the plane of the Si/SiO_2 interface. If the charge is placed at $\vec{r}_{imp} = (0,0,d)$ then the potential at the point $\vec{r}$ in the plane will be

$$\phi(\vec{r}) = \frac{1}{\epsilon}\frac{e}{\sqrt{(\vec{r}-\vec{r}_{imp})^2}} \quad \text{since} \quad r_z = 0 \quad \text{we write} \quad \phi(\vec{r}) = \frac{1}{\epsilon}\frac{e}{\sqrt{\vec{r}^{\,2}+d^2}}$$

$$\text{then if} \quad \frac{\vec{r}^{\,2}}{d^2} \ll 1 \quad \text{we expand} \quad \phi(\vec{r}) = \frac{e}{\epsilon d}\left(1 - \frac{1}{2}\frac{\vec{r}^{\,2}}{d^2}\right) \quad . \qquad (5.1)$$

Since we want the negatively charged impurity to affect the whole center of the channel we insist that the curvature of the band, K, and the curvature of the impurity potential be equal and opposite. From this condition, $K = \frac{e^2}{2\epsilon d^3}$, we find the value to d for a given curvature, K; in our system we find $d = 5\,\mathrm{nm}$, which sets the length scale for the width of the channel. From this value of d we may compute the maximum of the potential $e\phi_{max} = \frac{e^2}{\epsilon d} = 75\,\mathrm{meV}$; any electrons above this energy can not be trapped by the repulsive impurity. While it is difficult to conceive of the gate structure shown in figure B-3 as forming a channel, we may assume that the potential of at the

[11]If we simply consider an MOS device with a Cr gate, we find that at low temperature the flatband voltage (see reference [21, Ch. 8]) for which there is no electric field induced across the oxide is $V_{fb} = -.7\,\mathrm{V}$. At the low temperatures at which we make our measurements in a lightly compensated semiconductor, the Fermi level will be in the acceptor level which is a mere $.045\,\mathrm{eV}$ above the valence band edge. Thus for any lower gate voltage $V_{lg} < V_{fb}$ we can be certain that the Fermi level under the Cr gates will be near the valence band. Most of the lower gate voltages we have applied are $V_{lg} < -1\,\mathrm{V}$ and meet this condition. If, as is likely the case, an accumulation layer of holes can not form under the Cr gates because there is no source of holes at low temperatures in the dark, then the bands will be bent even more extremely.

[12]This will certainly be the case in the model we are considering where at the channel center there is an electron gas. In general we expect that near threshold the maximum of the barrier along the x direction (we are using the same coordinate system shown in figure 5-3) will be at most several times the Fermi energy. This maximum along the x is at the saddle point discussed in section 5.2, and corresponds to the minimum in the y direction. Since the band gap is $1.17\,\mathrm{eV}$, while the Fermi energy is at most $E_f = 20\,\mathrm{meV}$ the minimum in the y direction will be at least $1\,\mathrm{eV}$ above the valence band edge.

Si/SiO_2 surface changes on the scale of the oxide thickness, 20 nm. For the estimates that follow we have chosen a rather liberal estimate for the length of the channel, $l = 100\,\text{nm}$.

We may now estimate the charging energy and the total number of electrons that it is possible to trap in a channel delimited by a repulsive charge. We approximate the channel by a long prolate spheroid[13] which has a capacitance [63, page 116] of

$$C_{ch} = \epsilon \frac{\sqrt{l^2 - d^2}}{\ln\left(\frac{l+\sqrt{l^2-d^2}}{l-\sqrt{l^2-d^2}}\right)} \quad . \tag{5.2}$$

The potential energy of the Nth electron added to this region will be $E_N = N\frac{e^2}{C_{ch}}$, and thus it will be trapped only if $E_N \lessapprox e\phi_{max}$. Thus the maximum number of electrons that can be trapped in this system, N_{max}, is

$$N_{max} = \frac{e^2}{C_{ch}}\frac{1}{e\phi_{max}} = \frac{l}{d}\frac{\sqrt{1-(\frac{d}{l})^2}}{\ln\left(\frac{l+\sqrt{l^2-d^2}}{l-\sqrt{l^2-d^2}}\right)} \quad . \tag{5.3}$$

That $N_{max} \propto \frac{l}{d}$ seems reasonable since when $N = N_{max}$ the density of electrons is equal to the charge density of the impurity in the plane,[14] $\frac{N}{ld} = \frac{1}{d^2}$; additional electrons will see a constant background of charge. For our system[15] $N_{max} = 10$, which is not unreasonable for the number of conductance peaks that we observe. In this calculation, however, we have neglected the kinetic energy due to confinement of the electrons in the channel, ε_{ch}; we really should have replaced $e\phi_{max}$ with $(e\phi_{max} - \varepsilon_{ch})$ in computing N_{max}. Based on the curvature, K, we used we find $\varepsilon_{ch} = 24\,\text{meV}$ thus reducing N_{max} to 7 electrons. If we account for the kinetic energy when we compute N_{max} we find that changing the width of the channel does not strongly influence the number of electrons trapped.[16] Only by greatly increasing the length of the channel is it possible to increase N_{max}. When considering this model we liberally choose $l = 100\,\text{nm}$, and nonetheless N_{max} is still too small to be plausible; a more conservative

[13] A spheroid with a long axis of length $2l$ and the other two axis both of length $2d$, with a total volume $\frac{4}{3}\pi l d^2$.

[14] The only difference between the two calculations is due to numerical factors from the exact capacitance formula.

[15] We have included a factor of $\frac{\epsilon_{Si}}{\epsilon_{SiO_2}}$ in our computation of N_{max}. This factor is due to the different dielectric constants that need to be used in the calculation of $e\phi_{max}$ and $\frac{e^2}{C_{ch}}$; this correction increases N_{max} by a factor of 3.

[16] If the width is decreased then d is decreased and $\frac{l}{d}$ is increased, however so is ε_{ch}, and there is little effect on N_{max}.

choice of $l = 50\,\text{nm}$ would have further reduced the number of electrons trapped to $N_{max} \approx 4$. On the other hand, in the experiments of Scott-Thomas [46, 26] where the devices had a much larger aspect ratio with $g \approx 70\,\text{nm}$ and $1\,\mu\text{m} < l < 10\,\mu\text{m}$ this model is more plausible; in Scott-Thomas' experiments we would expect the channel to trap many electrons and to have its conductance limited by Coulomb blockade.

The most severe problem with the model that the conductance resonances are due to charge trapping by repulsive impurities arises from the required impurity density. For most devices to have their channels constricted as shown in figure 5-7 the density of impurities must be $\approx \frac{1}{ld} = 2 \times 10^{11}\,\text{cm}^{-2}$, while the measured[17] impurity density is actually $\approx 6 \times 10^{10}\,\text{cm}^{-2}$. Given this impurity density we would expect that, on average, only one our of 4 devices would have two impurities in the channel and show conductance resonances. Instead we have failed to find a single barrier device of the more than 35 which we have measured that does not have conductance resonances. Given this problem and the restrictions on the number of charges trapped we believe that it is unlikely that the conductance resonances that we observe are due to repulsive impurities.

5.3.2 Trapping by Attractive Charges

It has been suggested by Kopely *et al.* [57] and McEuen *et al.* [58] that the states which give rise to resonances in a single barrier are due to attractive impurities in the vicinity of the barrier. They suggested that a Na^+ ion in the oxide above the barrier would create a local binding center that would create a localized state within the barrier region. Such attractive binding site gives rise to conductance resonances in a single barrier, which is the phenomenon they sought to explain. Each positively charged ion in the vicinity of the barrier can trap only one electron, much as one proton traps only one electron to from hydrogen.[18] As the gate voltage is swept through a conductance resonance an additional electron is added to the barrier (see section 3.1.2). Thus to have many conductance resonances it will be necessary bind multiple electrons; however this is only possible with multiple attractive impurities. In the next section we consider the nature of the peak spacing in the case where there are multiple binding sites within the barrier. We will see that to observe equally spaced

[17]These values are for fixed oxide charge and were measured by capacitance measurements on large areas fabricated on the same wafer as the nanostructures we have been discussing. For relevence of MOS capacitence measurements see [18, p. 379-383]

[18]Strictly speaking the proton has a second weakly bound state, H^-. However it is impossible for either the proton, H^+, or a sodium ion Na^+ to bind more than two electrons.

conductance resonances a metallic island is required (see discussion in section 5.3.4). Since it is not possible for a Na^+ ion to form a metallic island that contains several electrons, attractive charges can not explain equally spaced conductance resonances.

5.3.3 Spacing of Localized States in Barrier

Since a single attractive impurity will only bind one electron it can only account for a single conductance resonance; therefore to account for the many conductance resonances that we observe in each barrier we consider the possibility that there are multiple binding sites within a single barrier. In particular this section will be concerned with the spacing of the conductance resonances in such a system.

The model we are considering consists of a barrier region of length l and gap g (as in figure 5-3) with N_{max} randomly placed binding sites each with a random binding energy. In the simulation we compute the ground state configuration of N electrons arrayed among the N_{max} sites and find its energy, E_N. In the simulation we find difference of these energies, $\mu_N = E_N - E_{N-1}$; this difference is the analog of the chemical potential for a small system.[19] The values of μ_N are the energies at which an Nth electron will be added to the system, and when the Fermi energy in the leads $E_f = \mu_N$ the system is at a charge degeneracy point and a conductance resonance. Similarly, the separation between μ_N and μ_{N+1} is the analog of the spacing between conductance resonances.[20]

Since we hope know that the electron-electron interaction is very important in understanding the electronic states of a small system we must include them in our simulation. It is this interaction that makes finding the ground state of N electrons in N_{max} binding sites a complicated problem.[21] In our device there are several conductors in the vicinity of the channel which screen the interaction between electrons on different binding sites.; instead of using a simple Coulomb interaction between two binding sites we have included the effects of the conductors by using the same techniques we discussed in section 5.2 and appendix C.

[19] Strictly speaking the chemical potential is only a meaningful concept in an infinite system. For our purposes we adopt the definition above. By our definition if we allow exchange of particles with a reservoir with a Fermi energy, E_f, such that $\mu_N < E_f < \mu_{N+1}$ then electrons will be exchanged between the reservoir and our system until N electrons occupy the barrier. It is in this sense that we speak of the chemical potential of the states in the barrier.

[20] A very nice discussion of the analogy between the chemical potential in these systems and in chemical reactions is given in [45].

[21] The model we are solving is just a two dimensional finite size Coulomb glass; because of the wide number of systems with charged disorder, the Coulomb glass is of general interest.

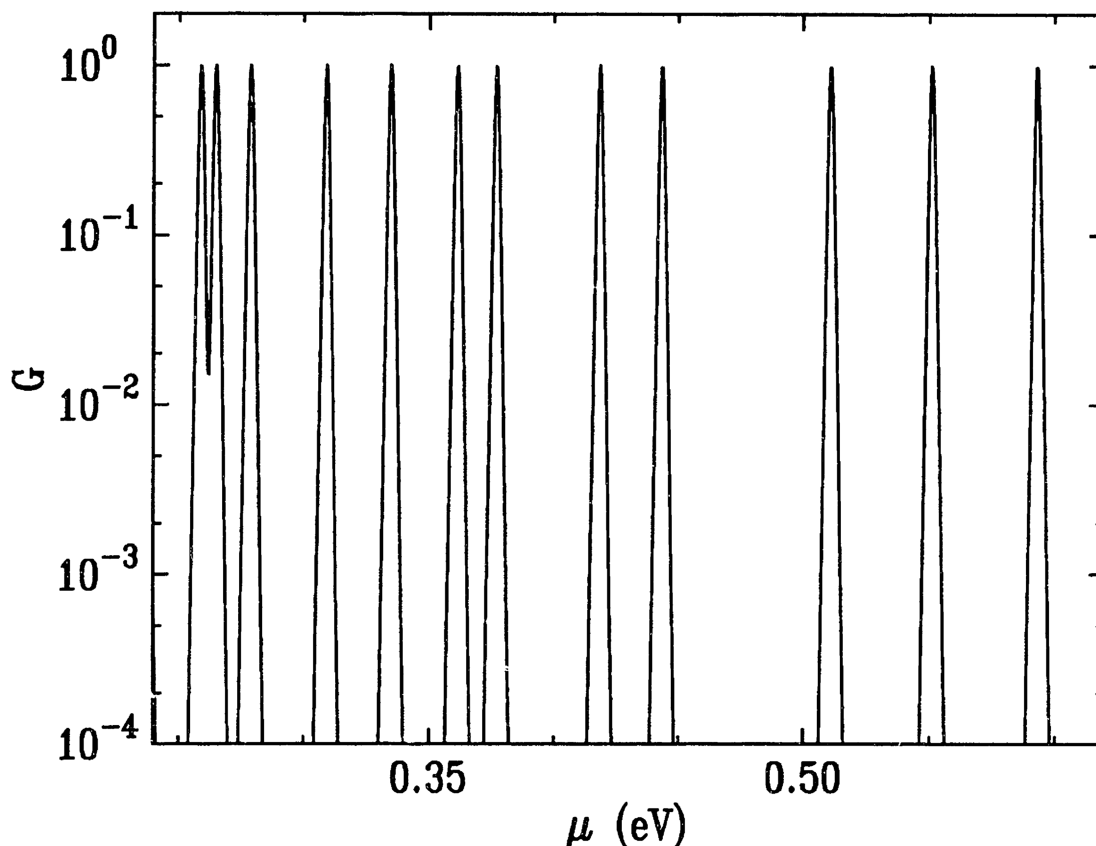

Figure 5-8: This figure shows a simulated conductance trace for a barrier 50 nm × 50 nm with 40 binding sites. In this figure we have placed a conductance peak with unit conductance and the shape of a Fermi-Dirac derivative at each of the charge degeneracy points, μ_N. This was done to facilitate comparison with experimental data, such as those shown in figures 5-1, 5-2, 4-8, and those shown in section 6.2.4. It is clear from the plot that there is a fairly large variation in the spacing of the peaks; the variation of peak spacing in this simulation is far larger than those of the experimental plots shown in the figures mentioned above, suggesting that this model is not applicable to those data. In this simulation there was effectively no variation in binding site energy, and the random peaks are due to the random positions of the binding sites. This plot shown peaks 21 – 31, and the $FWHM$ of the conductance peaks is .5 meV.

In figure 5-8 we show the results of our simulations in which there are large fluctuations in the spacing of the conductance peaks. While the simulation we are performing can give us the location of the conductance peaks they give us no information about the shape or amplitude of the peak. In figure 5-8 we have presented the data by placing the derivative of the Fermi-Dirac function[22] at each value of μ_N to facilitate comparison with the experimental data. When compared to figures 5-1, 5-2, 4-8, and those figures shown in section 6.2.4 it is clear the the fluctuations of peak spacings in figure 5-8 are much larger.

[22]We have used an arbitrary temperature so that $FWHM$ of the peaks was .02 times the average peak spacing. We then normalized the peaks to have unit conductance at their center.

The genesis of the fluctuations in the peak spacing shown in figure 5-8 is the random positions of the binding sites rather than their random energies. This is expected since the randomness in the positions of the sites results in random electron-electron interactions. For example in figure 5-8 the random binding energies range from $-.05\,\text{meV}$ to 0 while the average peak spacing, $s_N = \mu_{N+1} - \mu_N$, is $\overline{s} \approx 20\,\text{meV}$; on the other hand, the electron-electron interaction energy between sites has average fluctuation of 30 meV and matches the average peak spacing quite well.[23] We may quantify the fluctuations in peak spacing by their normalized standard deviation

$$\sigma_{norm} = \frac{\sqrt{\overline{s^2} - \overline{s}^2}}{\overline{s}} \tag{5.4}$$

where $\overline{s}$ is the average spacing between peaks, and $\overline{s^2}$ is the mean square of the spacing. In all the simulations we have performed σ_{norm} is very uniform and within $.55 < \sigma_{norm} < .65$, despite variations in $\overline{s}$ by more than a factor of five.[24] The simulations have varied the binding energy from .05 meV to 50 meV, the length of the channel from 50 nm to 200 nm, as well as forcing the sites to all lie along a narrow strip of 5 nm along the channel center while keeping the channel length at 50 nm; nonetheless, σ_{norm} has remained quite consistent showing that the main source of variation in the peak spacing remains the random position of the binding sites.

In these simulations we have treated the electrons classically and have not considered the possibility that they might delocalize within the barrier. The quantum mechanical coupling between sites may allow electronic states in which an electron is spread over several binding sites. In a bulk system we would characterize this spreading of the electronic states over several sites by the growth in the localization length,

[23]While the average binding sites range from $-.05\,\text{meV}$ to 0, the onsite energy also includes a contribution from image charge attraction discussed in section 5.2. If we include this energy in the binding energy than the average fluctuations in the binding energy are 1 meV. Nonetheless, it is clear that the average peak spacing for this simulation scales with the electron-electron interaction energy and not with the binding energy.

[24]In all of these simulations we discuss here there there are 40 binding sites. We might expect that the site density is given by the density of localized states at the metal-insulator transition, $\approx 3\times10^{11}\,\text{cm}^{-2}$ (see section 2.2) in the bulk two-dimensional electron gas. For a barrier $50\,\text{nm}\times 50\,\text{nm}$ this would then give approximately 8 states. However experience shows that the fluctuations in the peak spacing increases when adding the last several electrons because the number of possible electron configurations is greatly reduced and the effect of the random positions is enhanced. Thus in hopes of getting adequate statistics and of giving this model the best chance of success we have increased the number of sites to 40, and only considered the range $5 < N < 35$ when compiling statistics. If we consider the full range $1 < N < 40$ then σ_{norm} increases for all of the simulations, as do the fluctuations of σ_{norm}, thus we believe that the it is more meaningful to consider the range $5 < N < 35$.

ξ, as was discussed in section 3.3. In fact the model we are considering is similar to a finite size Anderson model with Coulomb correlations. If one considers the nature of the electronic states in such a system as the coupling grows it is possible that metallic islands form and subsequent electrons are added to the same area; this possibility and the nature of conductance resonances in such a regime are the subject of the next section. However, if the system consists of binding sites that are not coupled as we considered in this section then the electrons are localized on an individual binding sites and the conductance resonances are not be equally spaced.

5.3.4 Electron Puddles

What distinguishes a metal from a dielectric is its ability to screen internal electric fields; it is this screening that is responsible for the equal spacing of the conductance peaks in metallic artificial atoms. Since there are no internal fields, the artificial atom is at an equipotential and any electron is free to explore the whole metallic area; thus each new electron is added to an object of the same size which is characterized by a single capacitance, C_Σ. In artificial atoms with many electrons trapped between the barriers[25] the peak spacing is equal [27, 64]. In double barrier semiconductor artificial atoms the fluctuation in peak spacing is due to the fluctuations in the quantum mechanical confinement energy; in addition the peak spacing in these device tends to be reduced as more electrons are added and the artificial atom gets larger [32]. The details highlight the main point: to observe equally spaced conductance peaks each subsequent electron must be added to region with metallic screening.

To understand the origin of metallic areas in our devices we perform the following *gedanken* experiment. Let us imagine a high density degenerate electron gas[26] in the presence of disorder whose electronic states are shown schematically in figure 5-9. Since the electrons in the gas are delocalized and free to move they will form a metal and screen the effects of disorder. While the disorder is weak in nature then the changes in density will be minor, $\frac{\delta n}{n} \ll 1$. Since there are no large variations in density over the sample the Fermi energy will not vary much, and the states at

[25] We are referring to structures where an elemental metal is separated from two leads by tunneling barrier. Such a system is easily formed using Al/Al_2O_3 interfaces and may contain $> 10^9$ electrons and is usually referred to as Single Electron Transistor (SET). While it may be argued that these devices should not be considered an artificial atom because the discrete nature of their quantum mechanical level structure is smeared at $T = .05\,\mathrm{K}$, we will use this term so as not distract the reader. For the purposes of the discussion here these devices are excellent illustrations of the equally spaced conductance peaks in a system with metallic screening.

[26] Our electron gas is in the regime $k_B T \ll E_f$.

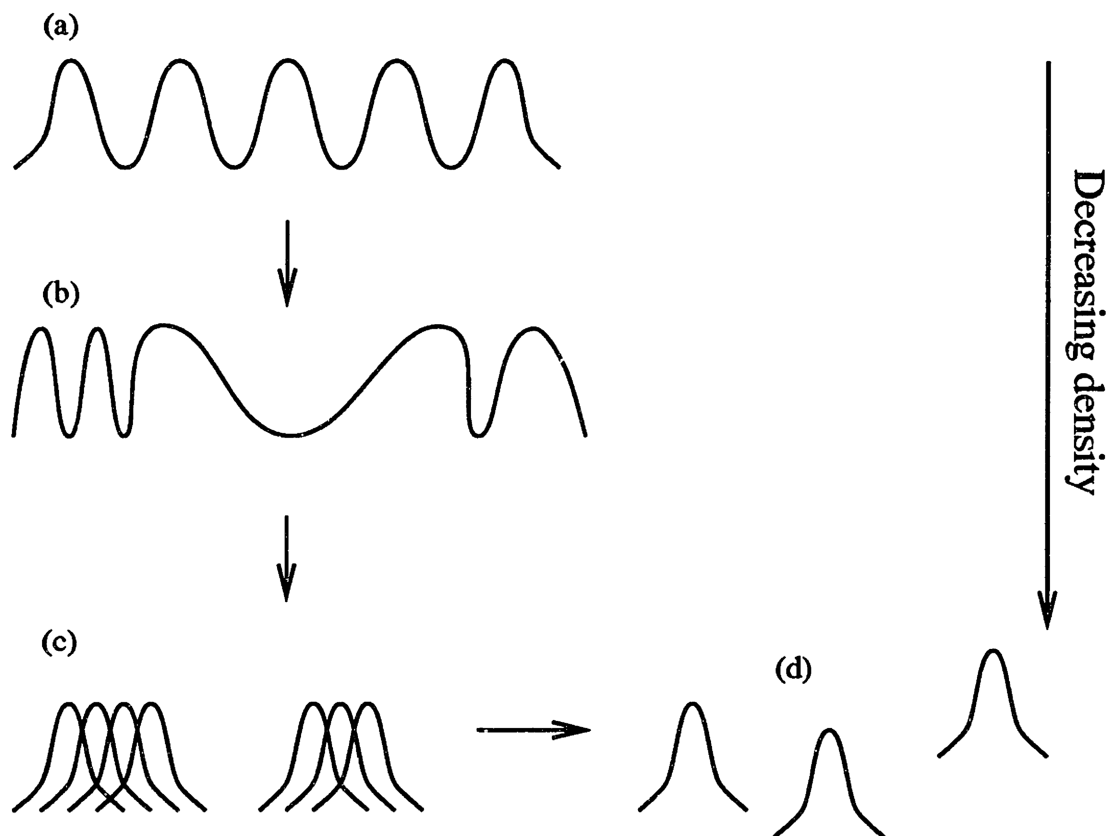

Figure 5-9: In this figure we show a sketch of how the electron wavefunctions change in a metal as the density is decreased. If there is a high density of electrons (a) then the Fermi sea will screen the disorder and wavefunctions at the Fermi level will be planewave states. As the number of electrons is decreased (b) the ability of the Fermi sea to screen is reduced, the fluctuations in metallic density become more noticeable, and the wavefunctions at the Fermi level are more affected by disorder. While the electrons are still delocalized the density will be higher in areas of lower potential energy. When the density is lowered still further (c,d) there are certain areas where the disorder is too repulsive to screen, and the metal breaks up. In figure (c) we suggest that the metal first breaks into metallic droplets before breaking apart into individual localized states (d). These metallic droplets, or "electron puddles", each of which contains several electrons, are still capable of metallic screening within the puddle. Previous theoretical treatments have focused on (b) and (d), and the case of "electron puddles" has not been carefully considered. We believe, however, that the equally space conductance resonances seen in figures 4-8, 5-1, and 5-2 and discussed in section 6.2.4 are evidence that such metallic "electron puddles" are forming in the disordered barriers we are studying.

the Fermi level will be planewave states; this situation is shown in figure 5-9a. If we now decrease the density of the electron gas then its ability to screen the disorder will be reduced and $\frac{\delta n}{n}$ will be almost unity. In this case electrons at the Fermi level will still be delocalized, but their wave function will no longer resemble a plane wave (see figure 5-9b). As the density is reduced still further the disorder in certain areas of the electron gas will overwhelm the ability of the electrons to screen, and the sample will break apart into metallic islands which we have dubbed "electron puddles". This idea was suggested by Levitov [65], and is shown in figure 5-9c. Each of these islands contains several electrons and is capable of metallic screening within its localized area; however, when an electric field is applied over a length scale much larger than the size of one of these puddles then the electrons can no longer effectively screen the field.[27] Finally as the density is reduced still further the electron-electron interaction will force the ground state to consists of isolated electrons localized in sites throughout the sample. This situation, shown in figure 5-9d, is akin to the models developed when considering hopping transport (see section 3.3). In our *gedanken* experiment we have just changed the density through the disorder induced metal insulator transition, which is generally known as the Anderson transition. We note that previous considerations of this problem have dealt with the limit of the dirty conductor and the limit of Coulomb correlations in hopping; however there is no unified theoretical treatment of screening as the density is varied through the metal-insulator transition. The model of "electron puddles" is a novel physical picture to try to understand the regime in the vicinity of the metal-insulator transition.

We believe that the equally spaced conductance oscillations seen in single barriers are due to the presence of an "electron puddle" in the barrier. If a single puddle were present in the barrier then as the gate voltage is swept electrons would be added to a small metallic region; this metallic region is much like an artificial atom and we expect to observe Coulomb blockade with equally spaced conductance resonances. It is just this that is observed in figures 5-1, 5-2, 4-8, and in the figures of section 6.2.4, and we believe that the experiments shown in these figures are evidence of the existence of "electron puddles".[28] Because of the generality of the physical argument, the lack

[27]In this case the electron puddle will develop a dipole moment much like that developed by a conductor in a uniform field. If the electric field persists over many such electron puddles then the net effect will resemble dielectric screening.

[28]In many of the other experiments discussed in chapter 6 the spacing between peaks is not equal. This may certainly be accounted for by the presence of multiple "electron puddles" within a single barrier. Given the lower mobility and higher degree of disorder found in samples fabricated in silicon MOS devices compared to those of GaAs/AslGaAs heterostructures, it is not surprising that there may be a higher density of electron puddles in a silicon MOS system. While we may explain unequal

of an existing and well developed theory, and the compelling experimental evidence from several different systems which lack other credible explanations, we believe that the idea of "electron puddles" merits further study.

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spacing within the electron puddle model, it may also be explained by other models as well (for example the one discussed in section 5.3.3).

Chapter 6

Measurements of Single Barriers

In this chapter we present measurements on several different single barrier devices. We have seen in chapter 4 that it is profitable to discuss the transport through a single barrier in terms of artificial atoms, while in chapter 5 we discussed various models to account for conductance resonances through a single barrier. The purpose of this chapter is to explore the diversity of experimentally observed behavior that these devices exhibit. Each section will discuss a different type of experiment: conductance versus gate voltage measurements for a variety of device geometries and voltage ranges, temperature dependence of conductance peaks, differential conductance measurements, changes in transport in a magnetic field, thermal cycle experiments, and crossing of conductance peaks. While we will compare these data to some of the simple models previously discussed in this thesis, the focus will be on presenting the data. We wish to give the reader some sense of what behavior is regularly observed in these devices despite (and maybe even because) all these data can not be simply understood within one model. This chapter is, therefore, rather heavy reading.

Before we delve into our detailed examination of these devices it is important to recall and stress some basic information that should be kept in mind. The measurements presented in this chapter are all of single barriers which show resonances in the conductance as a function of gate voltage (sections 4.3 and 4.4). The geometry of such a configuration is shown in figure 4-6. Despite our naive expectation that such devices should have monotonically increasing conductance (section 3.2.1) we have observed that of the more than thirty-five devices we have measured every single one shows conductance resonances at low temperatures. In addition $G(V_{ug})$ changes when the devices are thermally cycled indicating that these resonances are due to disorder (for more details see section 6.2.3). Finally, a fraction of the single barriers examined show equally spaced conductance peaks (sections 4.3, 5.3.4, and 6.2.4). With this

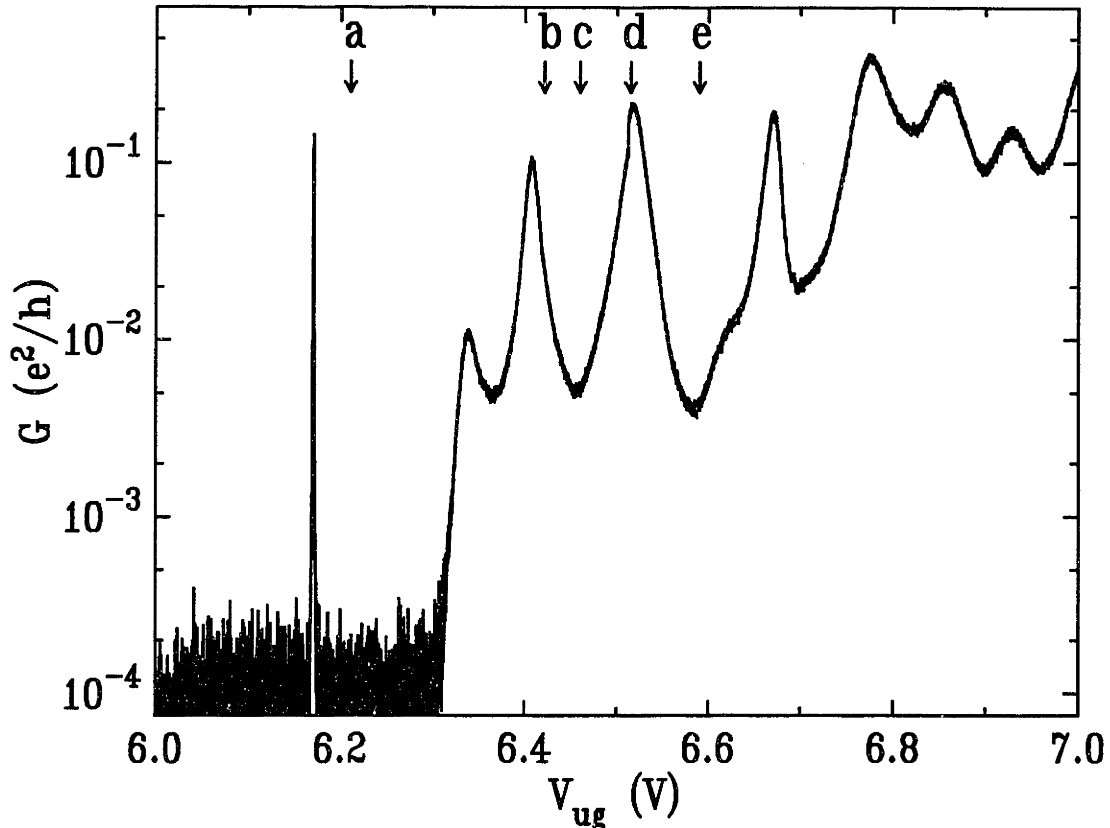

Figure 6-1: $G(V_{ug})$ showing the same device studied in section 4.3 in a similar bias regime. This figure shows smooth peaks with reasonable lineshapes with regular spacing, however the spacing is not equal. The letters point to different gate voltages at which tunneling spectra were measured (see section 6.4 and figures therein). Data taken at $T \approx .1$ K, $V_r = -3.0$ V, $V_l = +1.5$ V, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

background in mind we now begin our more detailed examination of the data.

6.1 Conductance versus Gate Voltage Experiments

In our typical experiment we measure conductance as a function of the voltage on the upper gate with fixed voltages on the lower gates. We have already seen that such traces can show equally spaced peaks whose shape we may hope to understand (figure 4-8) and randomly spaced peaks whose shape is far more mysterious (figure 4-7). Another such trace of $G(V_{ug})$ is presented in figure 6-1 and shows behavior that is intermediate; the peaks are single peaks without side lobes and are regularly spaced. However the peaks are not as equally spaced as those in figure 4-8. While the conductance resonances in this trace may be due to tunneling through a single

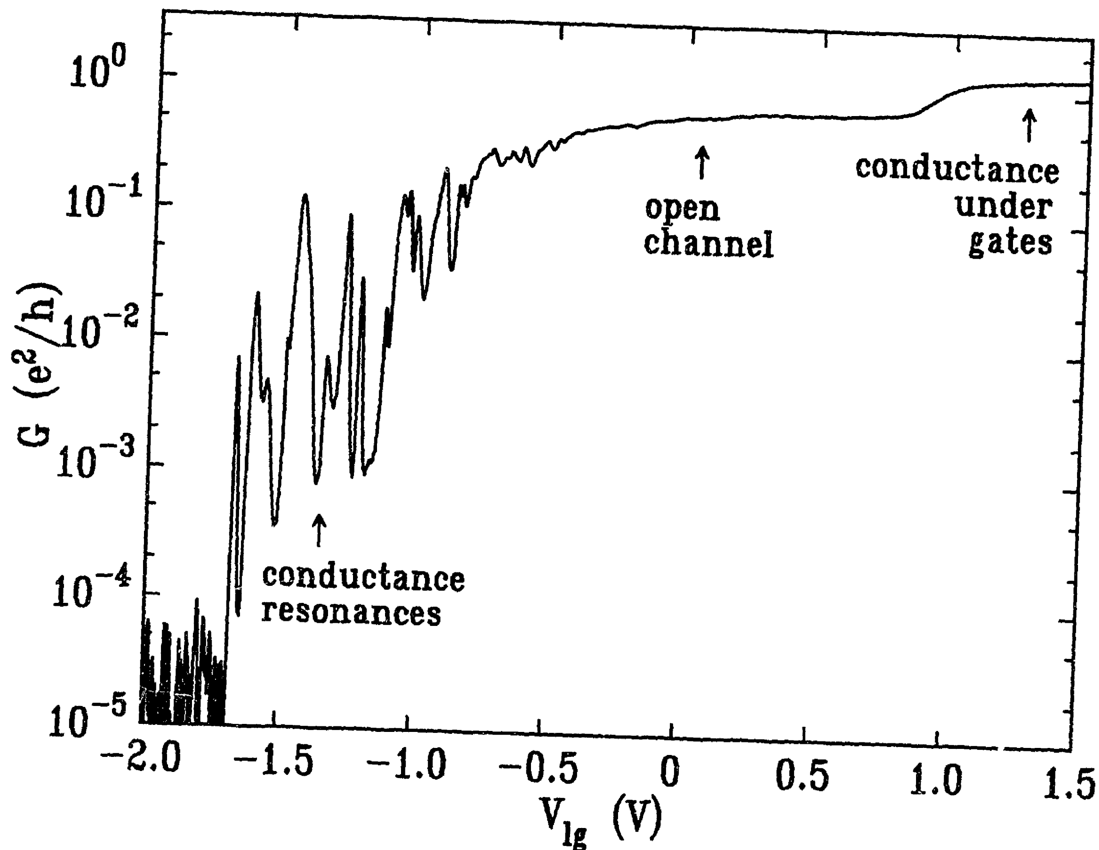

Figure 6-2: $G(V_{lg})$ showing conductance resonance for $-2.0 < V_{lg} < -0.5$ as would be expected due to capacitive coupling between lower metal gates and electronic states of the barrier. When $-0.5 < V_{lg} < +0.7$ the conductance is dominated by an open channel in the gap between the lower metal gates. Finally for $V_{lg} > +0.7$ electrons can flow in the electron gas that forms under the lower gates. Data taken at $T = .32\,\mathrm{K}$, $V_{ug} = +8.0\,\mathrm{V}$, on device F30 wafer #13. The gate geometry is an isosceles triangle of height 50 nm, with 150 nm gap.

electron puddle, as we believe is the case in figure 4-8, the variation in spacing is not as uniform and there is no systematic trend in the width of the peaks. We also note that this trace was taken on the same device as that shown in figure 4-8 after thermal cycling. The rest of this section will focus on measurement of the conductance as a function of gate voltage in an attempt to uncover general trends in these data.

6.1.1 Conductance versus Lower Gate Voltage

In figure 6-2 we show the conductance of a device as a function of lower gate voltage. We begin by noting that there are conductance peaks in this trace just as we have seen in a measurement of $G(V_{ug})$. The lower gates are capacitively coupled to the electronic states in the barrier as is the upper gate and therefore changing the lower gate voltage will also change the energy of the electronic states in the barrier. Since we

expect conductance resonances each time an electronic state in the barrier is resonant with the Fermi level, sweeping the lower gate will result in conductance peaks. These conductance peaks are confined to the region $-2.0 < V_{lg} < -0.5$. At lower gate voltages below -2.0 there are no visible resonances; if there are states in the barrier resonant with the Fermi level at gate voltages below this, then these states must carry currents well below the noise floor of our measurement system.

As the lower gate voltage is raised, and the barrier lowered, transport is no longer dominated by tunneling through electronic states in the barrier. Note the increase in conductance at approximately $V_{lg} = +0.7\,\mathrm{V}$; at this voltage a metallic electron gas forms underneath the lower metal gate, and electrons can now flow underneath these lower gates instead of being confined to the gap between them. When $V_{lg} < +0.7$ we can be certain the observed conductance is due to electron transport in the regions where there is no lower metal gate. For $-0.25 < V_{lg} < +0.7$ transport is due to a conducting channel in the region between the two lower metal gates. Now the barrier has been lowered to the extent that, at its minimum in the middle of the gap, it is below the Fermi level in the leads and electrons can now flow over the barrier as opposed to tunneling through it. As expected the conductance in this region is $\approx \frac{e^2}{h}$; however the conductance is not quantized because the electrons do not traverse the barrier ballistically.

By comparing the capacitance between the electronic states in the barrier with the different lower metal gates it is possible to determine where these states are located. A larger capacitance to one gate than to another indicates that the electronic states in the barrier are located closer to one gate than to the other. If we apply a negative voltage to the right pair of lower gates while the left pair is biased so that it has electron gas underneath it then we expect that the conductance resonances are all due tunneling through the states in the right barrier. While this assumption is quite reasonable we have tested it nonetheless. By measuring the shift in the upper gate position of a conductance peak, δV_{ug}, when the right pair of lower gates is changed by δV_{right} we can determine $\frac{C_{right}}{C_{ug}} = -\frac{\delta V_{ug}}{\delta V_{right}}$; similarly we may determine $\frac{C_{left}}{C_{ug}}$. In such a measurement we found that $\frac{C_{right}}{C_{ug}} \approx 3.7$ while $\frac{C_{left}}{C_{ug}} \approx .2$; the capacitance of the right gates are larger by a factor of twenty than those of the left gates thus showing that the resonances are due to tunneling through electronic states that are located in the right barrier.

6.1.2 Lineshape of Conductance Peaks

The shape of the conductance peak can reveal a great deal about the nature of the tunneling process. If we are tunneling through an isolated resonance we expect the peak to be determined by the convolution of the natural lineshape and the derivative of the Fermi-Dirac function (see section 3.1.4 equation 3.12). When the temperature is low then the lineshape of the conductance peak will be dominated by the natural lineshape of the resonance. If the electron is tunneling through a lifetime broadened resonance we expect the natural lineshape to be a Lorentzian given by equation 3.14 where Γ is the half width at half maximum and $\frac{h}{\Gamma}$ is the lifetime of the state. In this case we expect to see a Lorentzian lineshape when $k_BT \ll \Gamma$. However we noted in our examination of the lineshape of the single barrier device exhibiting Coulomb blockade (see section 4.3.4) that the lineshape was not a Lorentzian. This deviation from Lorentzian lineshape is very interesting and may reflect the nature of the resonance or the nature of tunneling into the resonance. In this section we examine several other conductance resonances in an attempt to further explore this issue.

We begin by focusing our attention of figure 6-3 which shows $G(V_{ug})$ taken at $T \approx .1\,\mathrm{K}$. In this figure there are a variety of differently shaped peaks. We wish first to note that many of those peaks have shapes that we would not anticipate for a simple thermally broadened resonance. In addition we see a double peak at $V_{ug} = 3.9\,\mathrm{V}$; such double peaks are commonly seen in these data. At higher V_{ug}, however, there are three peaks whose shape appears quite reasonable to the eye; we will examine the second of these peaks. The peak at $V_{ug} = 4.14\,\mathrm{V}$ fits well to the convolution of a Lorentzian and the derivative of a Fermi-Dirac function as expected from equation 3.12. We find that the width of the peak grows linearly with increasing temperature (see figure 6-15) as expected from equation 3.15 which states $FWHM = \frac{C_\Sigma}{C_g}(3.52k_BT+2\Gamma)$. From this linear relation we use the slope of this line to obtain $\frac{C_g}{C_\Sigma} = .0071$, and the $T = 0$ intercept of this line to find $\Gamma = 8.4\,\mu\mathrm{eV}$. From these values we estimate the temperature of the electrons when our refrigerator is at base temperature to be $T_{res} = \frac{1}{3.52k_B}\frac{C_g}{C_\Sigma}(FWHM - 2\Gamma) = .096\,\mathrm{K}$; this value is consistent with our experimental setup.[1] Thus the two energy scales that determine the width

[1] While the base temperature of the dilution refrigerator is $T \approx .02\,\mathrm{K}$ the electrons in these mesoscopic systems are hotter. This discrepancy is due to the decoupling of the electronic degrees of freedom from the lattice degrees of freedom which occurs at low temperatures. Since the electrons are heated by electrical noise transmitted down the fridge wires, their temperature is much higher than that of the helium in the refrigerator. One of the dominant sources of noise is the Johnson

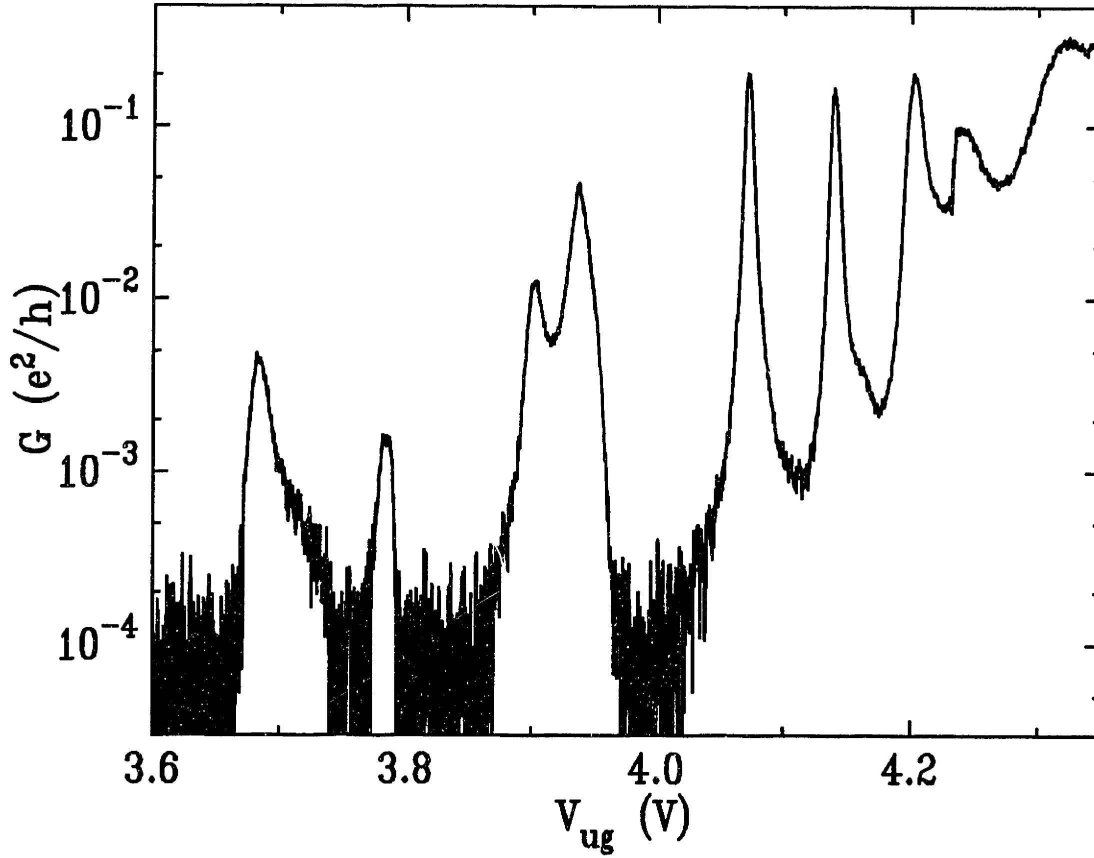

Figure 6-3: $G(V_{ug})$ showing peaks with a variety of different lineshapes. At $V_{ug} = 3.9\,\mathrm{V}$ there is a double peak, while the peaks at $V_{ug} = 3.67\,\mathrm{V}$ and $V_{ug} = 3.78\,\mathrm{V}$ have a peculiar shape. On the other hand the peaks at $V_{ug} = 4.07\,\mathrm{V}$, $V_{ug} = 4.14\,\mathrm{V}$, and $V_{ug} = 4.20$ appear to have a shape reminiscent of that expected from equation 3.12. In figure 6-4 we examine the lineshape of the figure at $V_{ug} = 4.14\,\mathrm{V}$ in more detail. Data taken at $T \approx .1\,\mathrm{K}$, $V_r = -6.5\,\mathrm{V}$, $V_l = +1.5\,\mathrm{V}$, device G21 wafer #7. The gate geometry is a rectangle of length 40 nm, width 80 nm, with 90 nm gap.

of the peak are of about the same magnitude, $k_B T_{res} = 8.3\,\mu\mathrm{eV}$ and $\Gamma = 8.4\,\mu\mathrm{eV}$. We expect that in this regime the lineshape will not be dominated by either of the two lineshapes but should instead be fit by the convolution of the two lineshapes. In figure 6-4 we show the expected lineshape given the parameters we have determined in our analysis above. We see that the experimental curve is fit well by the calculated lineshape over two orders of magnitude in the conductance on the low gate voltage side.

We now examine the lineshape of a conductance peak which is not dominated by thermal broadening. Again in this device we analyze the peak width as a function of

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noise of our room temperature electronics. To appropriately filter this noise and obtain the lowest electron temperatures filters mounted at low temperatures are required. Given the experimental setup in our lab, however, we would expect an electron temperature of approximately .1 K, in good agreement with this measurement.

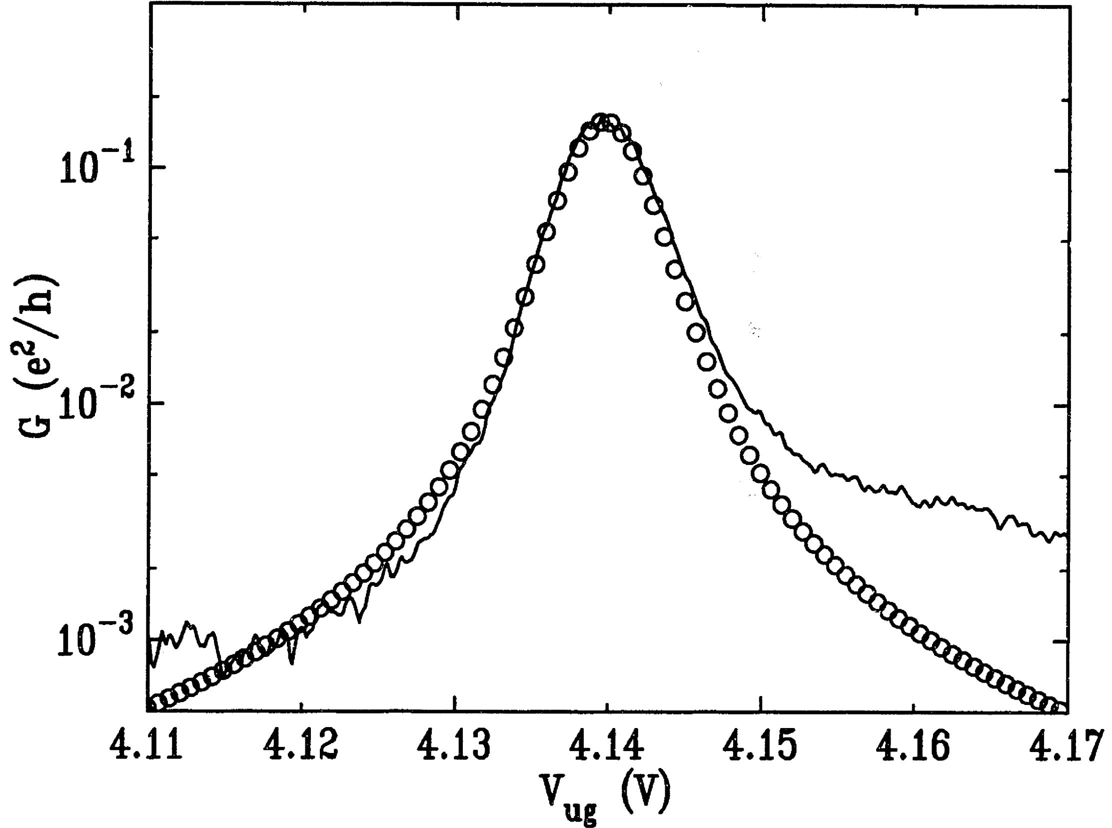

Figure 6-4: An expanded view of the peak at $V_{ug} = 4.14$ from figure 6-3. We have fit this peak to a thermally broadened Lorentzian determined from equation 3.12 with $\Gamma = 8.4\,\mu\text{eV}$, $T = .096\,\text{K}$, $\frac{C_g}{C_\Sigma} = .0071$ as discussed in the text. The experimental curve is plotted as a solid line while the fit to these data is plotted with open circles. Since $\frac{\Gamma}{k_B T} \approx 1$ the shape of the peak is not dominated by either the Lorentzian lineshape or by the derivative of the Fermi-Dirac function. For details on device as experimental conditions see the caption of figure 6-3.

temperature (see figure 6-14) to determine the relevant energy scales. Following the reasoning presented above we find $\frac{C_g}{C_\Sigma} = .035$, and $\Gamma = 127\,\mu\text{eV}$, and we thus estimate the temperature of the electrons to be $T_{res} = .12\,\text{K}$. In this case because $\frac{\Gamma}{k_B T} = 12$ we expect the lineshape to be dominated by the natural broadening. In figure 6-5 we plot the measured conductance as well as a Lorentzian with the width, $\Gamma = 127\,\mu\text{eV}$. We see that the Lorentzian fits the experiment quite well and even accounts for the tails of the conductance resonance on the high gate-voltage side. Because the conductance resonance is not symmetric the Lorentzian can not account for the tails on the low gate-voltage side. As we saw in figure 4-12, Γ can change as a function of gate voltage; such a change in the tunneling rate might account for the asymmetry in this peak. For this value of $\frac{\Gamma}{k_B T}$ the deviations between a Lorentzian and a thermally broadened Lorentzian would be imperceptible on the scale of figure 6-5.

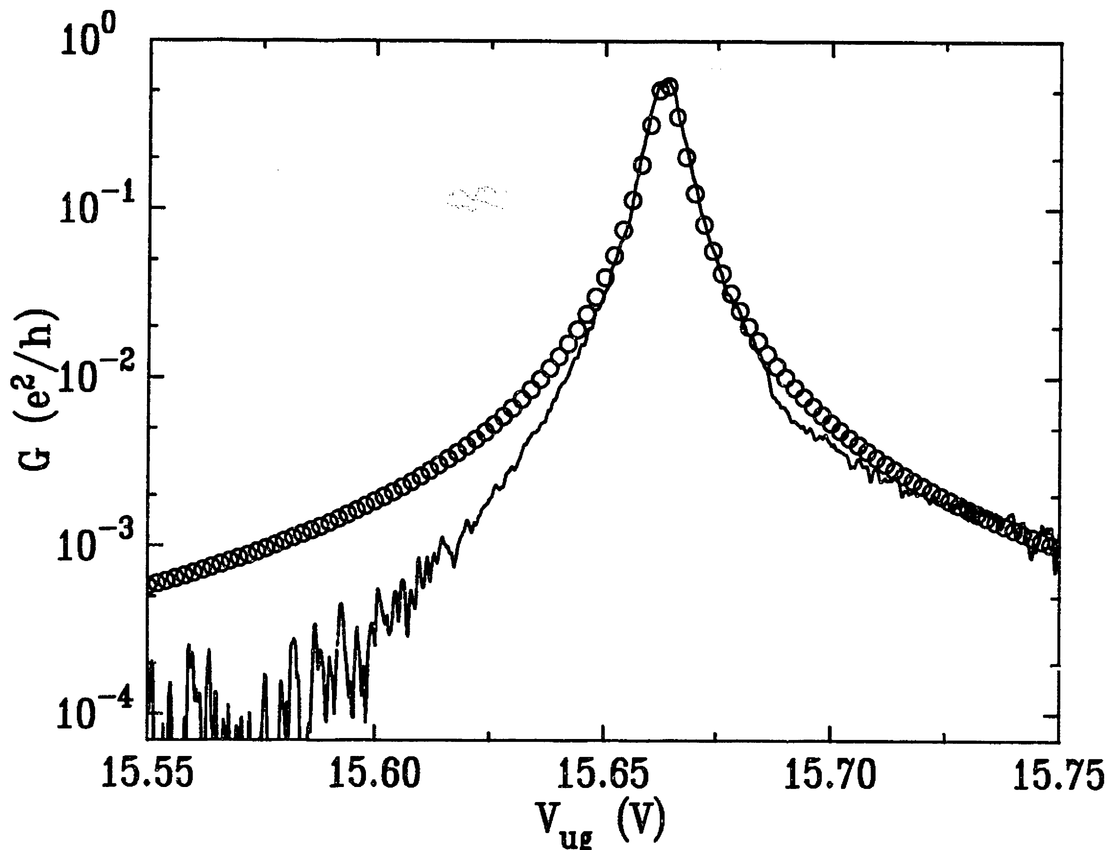

Figure 6-5: The detail of a conductance resonance that is well fit by a Lorentzian lineshape. The width of the Lorentzian is obtained from the $T = 0$ intercept of the width versus temperature. The parameters used in this fit are $\frac{C_g}{C_\Sigma} = .035$, $\Gamma = 127\,\mu\text{eV}$. Because $\frac{\Gamma}{k_B T} = 12$ the lineshape of a Lorentzian and a thermally broadened Lorentzian are indistinguishable on this scale. Data taken at $T \approx .1\,\text{K}$, $V_l = -4.0\,\text{V}$, $V_r = +1.5\,\text{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

6.1.3 Current versus Gate Voltage: Hidden Peaks

When examining a trace of $G(V_{ug})$ it is not be possible to observe a conductance resonances whose maximum conductance is below the noise floor of our instrumentation. For example, we measure only one conductance resonance between $V_{ug} = 6.0\,\text{V}$ and $6.3\,\text{V}$ in figure 6-1; from the spacing at higher gate voltages we might have expected another resonance in this range. Our failure to see a resonance does not mean that there are no states in the barrier being occupied in this energy range, rather that the conductance resulting from tunneling through those states are too small to measure. As we noted in section 5.3 the occupation of a state in the barrier changes the potential of all the other states in the area. This is true whether the state is associated with a large amplitude conductance peak or is a "dark" state whose conductance amplitude is too low to measure. In fact there may be a state that is strongly coupled

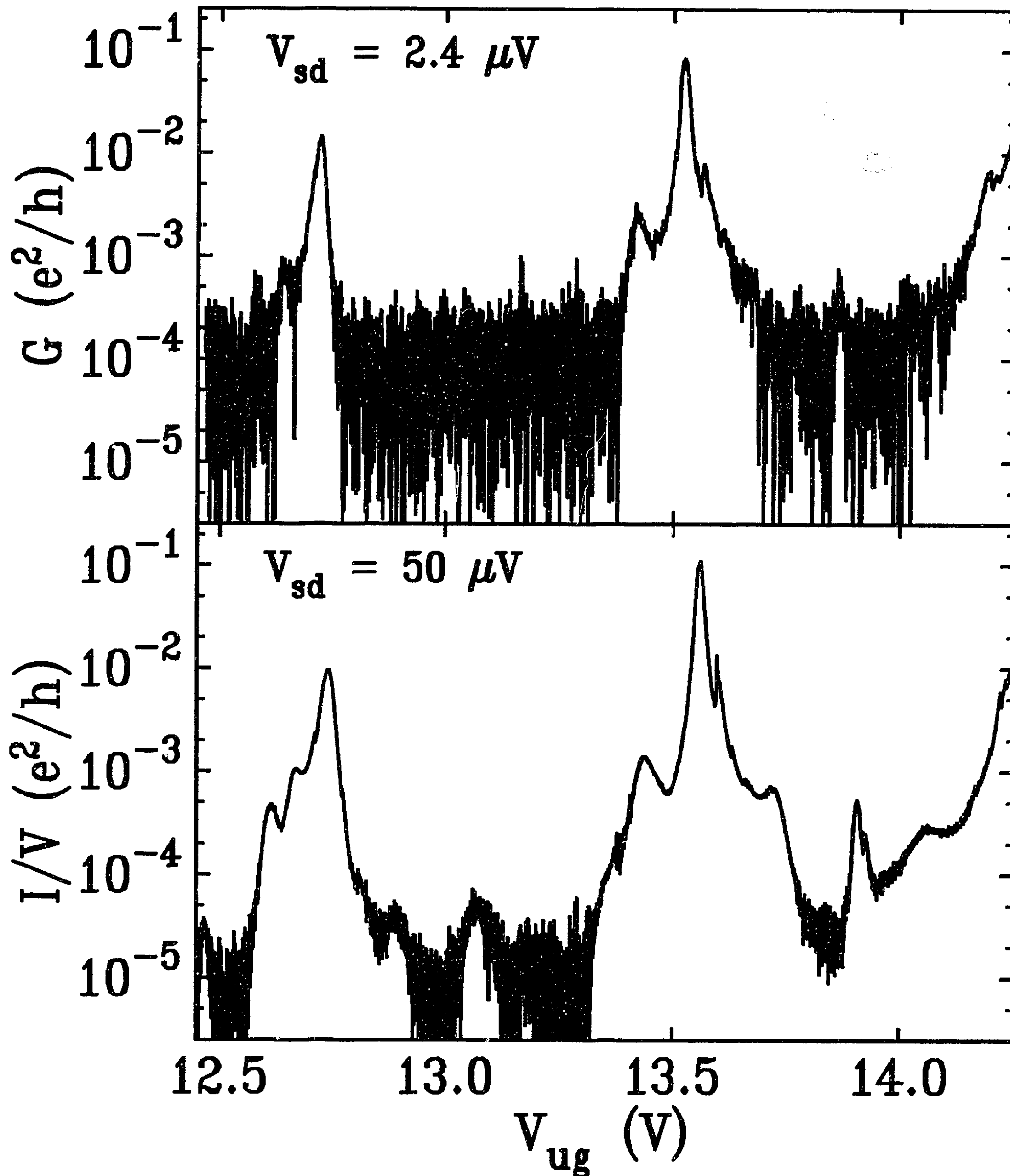

Figure 6-6: $G(V_{ug})$ is shown in the top panel for an applied bias of $2.4\,\mu$V. The bottom panel shows the normalized current $\frac{I}{V}$ when a larger bias of $50\,\mu$V is applied across the device. We have plotted both figures in the same units to aid comparison. While all of the peaks that appear in the top panel also appear in the bottom one, the bottom panel also shows "dark" peaks that can not be seen when the bias is lower. For example, the peak seen in the bottom panel at $V_{ug} = 13.1\,$V has a coupling that results in a current that is too low to measure when a low bias is applied across the device; no trace of it is evident in the top panel. The top plot uses lock-in techniques, while in the bottom one we have made a DC measurement of current. Data taken at $T \approx .1\,$K, $V_r = -2.0\,$V, $V_l = +1.5$ on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

to one lead but poorly coupled to the other; since the amplitude of the conductance peak is equivalent to two resistors in series (equation 3.2) it will be determined by the weaker of the two couplings. Thus it is possible that when this "dark" state is resonant with the Fermi level in the leads its occupation will be changing quickly despite the lack of a conductance peak.

We may test this idea by lowering the conductance noise in our measurements and looking for additional resonances. Since the noise that limits our measurement is current noise rather than conductance noise, and since by increasing the bias applied across our device the same conductance will result in a higher current, we may hope to lower our conductance noise floor by measuring at higher applied bias. In figure 6-6 we have plotted a measurement of the current through a barrier at two different applied biases; in the top panel the bias is $2.4\,\mu$V, while in the bottom panel the bias is $50\,\mu$V. There are three obvious conductance peaks in the top panel all of which are also visible in the bottom panel. However there are additional conductance peaks that are clearly visible in the bottom panel which were not visible in the top one. For example, the peak seen at $V_{ug} = 13.1$ V in the bottom panel has a conductance well below the noise floor of the trace shown in the top panel, and there is not hint of a feature at that gate voltage in the lower bias measurement. For this reason care must be taken when measuring the peak spacing from a conductance trace.

When a bias larger than the thermal voltage, $\frac{k_BT}{e}$, is applied across the device the current is no longer linear in the voltage. The occupation of the electronic states in the barrier will depend on the bias voltage, and the nature of the measurement is quite different. Because the current is not linear in voltage, the amplitude of the peak in $\frac{I}{V}$ may increase; in addition we expect that the peak width will increase with increasing bias. In the lower panel of figure 6-6 the amplitude of the peaks at $V_{ug} = 12.75$ V and at 13.5 V is larger than in the upper panel, and it is obvious that we can not increase the applied bias without changing the nature of our measurement. However, it behooves us to remember that our failure to see a conductance peak *can not* be taken as evidence that no additional electron has been trapped in the barrier.

6.2 Peak Spacing

The spacing between the conductance peaks is a measure of the energy difference between states of N and $N+1$ electrons. In an artificial atom the spacing between peaks is regular because the addition energy is dominated by the electron-electron interaction which is approximately constant for a metallic island. However in a nonin-

teracting system dominated by disorder, we expect the energy of states to be randomly distributed and therefore we would expect the peak spacing to be random. In this section we examine in more detail the typical behavior observed in these devices. We will observe that the spacing of peaks is roughly correlated with the size of the device, and increases as the device gets smaller. In addition we will see that the peak spacing changes with thermal cycle, showing that the conductance resonances are due to tunneling through a disordered region. Finally we will examine how the peak spacing can change with temperature and see some more examples of conductance traces that have regular spacings.

6.2.1 Changes with Lithographic Size

Since the peak spacing is a measure of the addition energy we expect that as the device is made smaller and the electron-electron interaction becomes more important the spacing should increase. The peak spacing will also decrease if the electronic states confined in the barrier are randomly distributed in energy. In this case, even if the density of electronic states per unit area does not decrease due to additional confinement, the area of the barrier is reduced and thus the spacing between states is increased.

We begin by comparing two barriers that have the same nominal lithographic dimensions. We present here two such pairs, one pair has a lithographic gap of 50 nm (figure 6-7), and the other pair has a lithographic gap of 200 nm (figure 6-8). Each barrier within a pair has a different threshold and a different pattern of peaks. These differences are due both to accidental differences in the lithography of nominally identical barriers, and to the differences in the random potential experienced by each of the two barriers. For example in figure 6-7 the threshold value for the left barrier is approximately $V_{ug} = 8.5\,\text{V}$, while for the right barrier the threshold is much higher $V_{ug} = 12.5\,\text{V}$. Because the gap in this device is very small (50 nm) any small fluctuations in the electron-beam lithography during device patterning which result in slight differences in the size of the gap can cause large shifts of threshold. However similar fluctuations in the device with a gap of 200 nm shown in figure 6-8 result in smaller fluctuations in the threshold.

We now would like to compare the peak spacing of these two devices. To make an accurate comparison we should compare the devices in the gate voltage range where all the conductance resonances are above the background noise, otherwise we

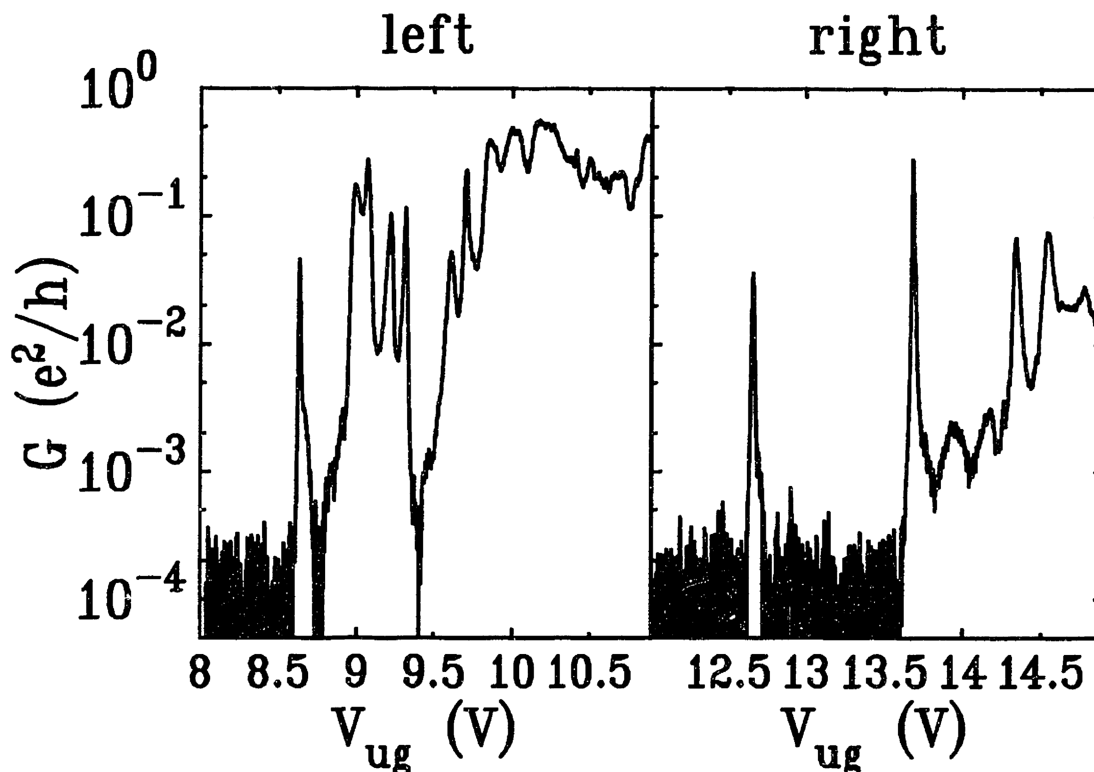

Figure 6-7: $G(V_{ug})$ for two nominally identical barriers. Both these barriers are have the same lithographic dimension and shape. In addition both are similarly biased (left: $V_l = -2.0\,\text{V}$, $V_r = +1.5\,\text{V}$, and right: $V_r = -2.0\,\text{V}$, $V_l = +1.5\,\text{V}$). Both the threshold for conductance and the peak spacing are different for the two barriers. The peak spacing is $\Delta V_{ug} = .17\,\text{V}$ for the left barrier and $\Delta V_{ug} = .22\,\text{V}$ for the right barrier; the higher threshold and peak spacing of the right barrier is consistent with a slightly smaller barrier. This figure should be compared with figure 6-8 which shows two other nominally identical barriers. Data taken at $T \approx .1\,\text{K}$, biases as noted above on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

may be missing peaks with conductance too low to measure[2] (see section 6.1.3). If we now examine figure 6-7 we find that the spacing of peaks in the left barrier is $\Delta V_{ug} \approx .17\,\text{V}$ while in the right barrier $\Delta V_{ug} \approx .22\,\text{V}$. In figure 6-8 the spacings are $\Delta V_{ug} \approx .07\,\text{V}$ and $\Delta V_{ug} \approx .06\,\text{V}$ for the left and right barriers respectively. The nominally identical barriers resemble each other and can be clearly distinguished from a barrier of different size. It is worth noting that the right barrier in figure 6-7 has larger peak spacing then the left barrier; this observation is consistent with the right barrier's higher threshold and can similarly be accounted for by a fluctuation in the lithography that makes the right barrier smaller. We have thus seen that the peak

[2]To avoid this problem we exclude the gate voltage region between the first conductance peak and the subsequent rise in background conductance. For example in the right barrier of figure 6-7 we exclude the region $V_{ug} < 13.5\,\text{V}$, while in the left barrier of that figure we only exclude the region below the first peak at $V_{ug} = 8.6\,\text{V}$.

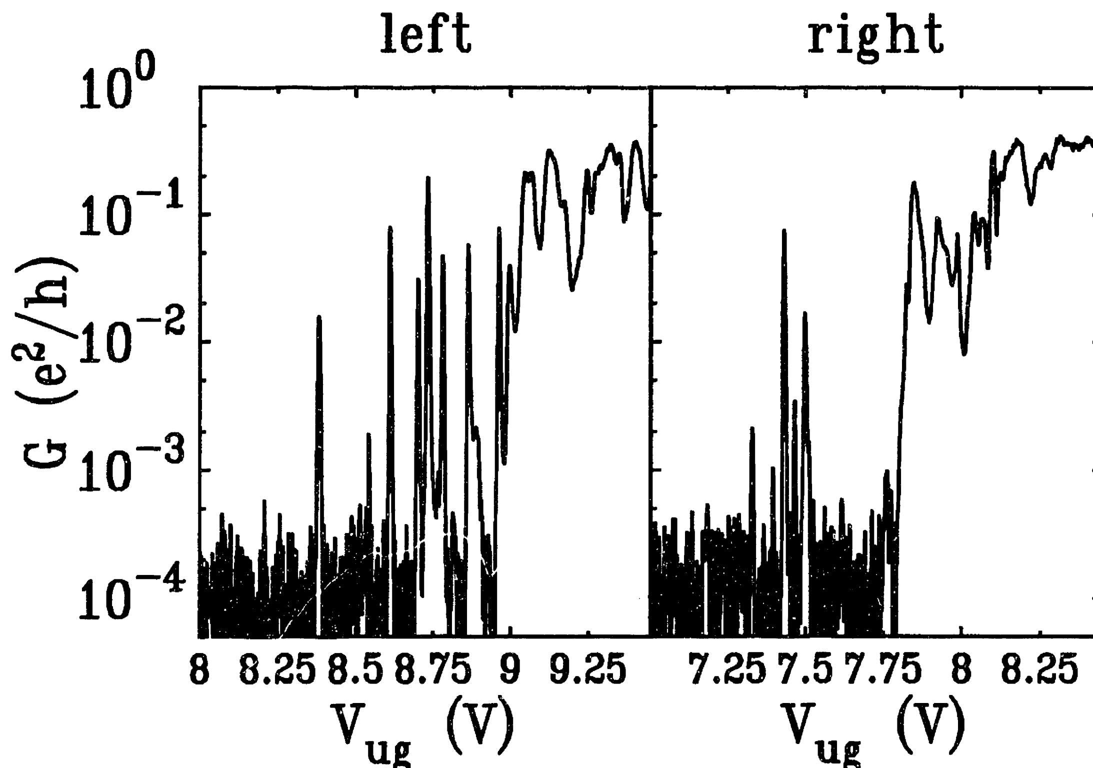

Figure 6-8: $G(V_{ug})$ for two nominally identical barriers. Both these barriers are have the same lithographic dimension and shape. In addition both are similarly biased (left: $V_l = -4.5\,\text{V}$, $V_r = +1.5\,\text{V}$, and right: $V_r = -4.5\,\text{V}$, $V_l = +1.5\,\text{V}$). These traces should be compared to figure 6-7; the device shown here has a larger gap. Because of that larger gap the threshold voltage is lower, there is less variation between nominally identical devices, and the peaks are more closely spaced by a factor of three (note that the gate voltage scale in this figure is half that in figure 6-7). These two devices have peak spacings that are quite close. Data taken at $T \approx .1\,\text{K}$, lower gate voltages as noted above, device B31 wafer #13. The gate geometry is an isosceles triangle of height 100 nm, with 200 nm gap.

spacing is larger for the smaller devices, as we had expected.

6.2.2 Changes with Lower Gate Voltage

We may carry out a similar analysis of the peak spacing for the same device seen in figure 6-7 with different lower gate voltages applied. We have previously seen that when the lower gate voltage is made more negative then the conductance threshold is shifted to higher upper gate voltage. While the barrier still shows conductance resonances, we would expect that the exact shape and size of the barrier will be different. Intuitively we expect that the barrier is confined more tightly in the lateral dimension. In figure 6-9 we compare the same device at two different lower gate voltages. As expected the upper gate threshold voltages shifts to higher voltages as the lower gate voltage is made more negative. In addition the peak spacing changes

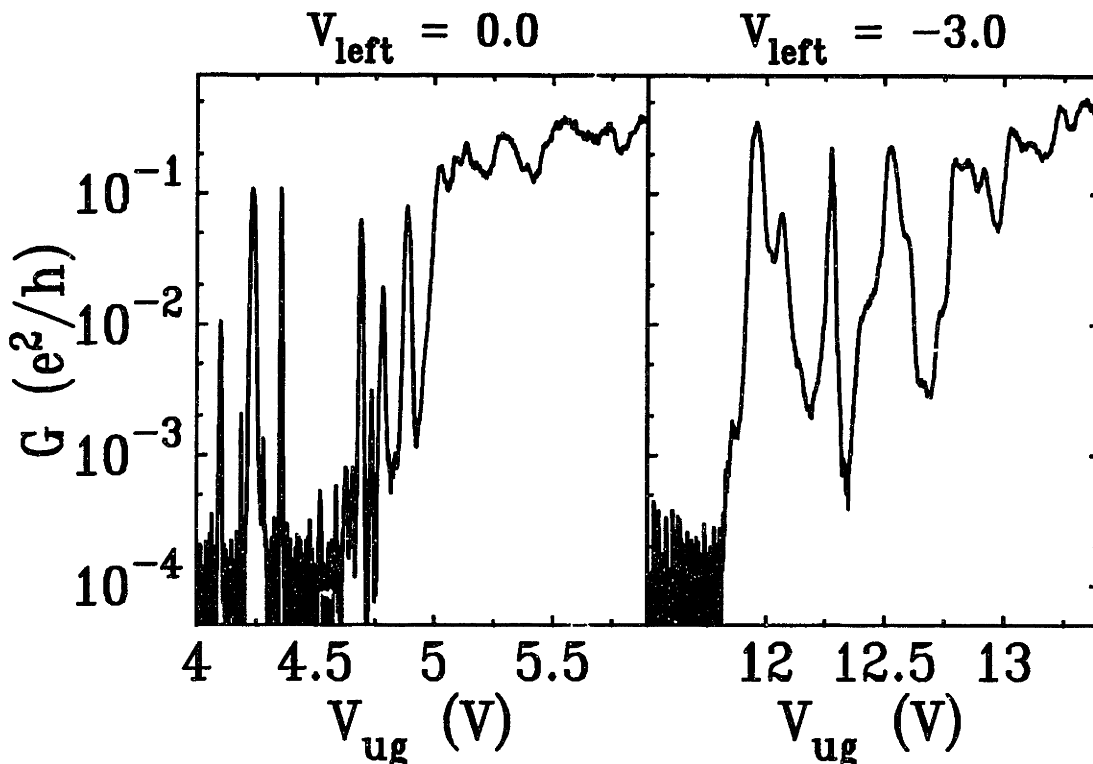

Figure 6-9: $G(V_{ug})$ for the same device with different different lower gate voltages. We see that the upper gate threshold voltages shifts to higher voltages as the lower gate voltage is made more negative. In addition the peak spacing changes from $\Delta V_{ug} = .07\,\text{V}$ for $V_l = 0.0\,\text{V}$ to $\Delta V_{ug} = .12\,\text{V}$ for $V_l = -3.0\,\text{V}$. This indicates that the lower gate is confining the barrier more tightly. Data taken at $T \approx .1\,\text{K}$, $V_r = +1.5\,\text{V}$, V_l as noted, on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

from $\Delta V_{ug} = .07\,\text{V}$ for $V_l = 0.0\,\text{V}$ to $\Delta V_{ug} = .12\,\text{V}$ for $V_l = -3.0\,\text{V}$. The change in peak spacing when a more negative lower gate voltage is applied suggests that, in fact, the barrier is more tightly confined and thus smaller.

6.2.3 Thermal Cycle Experiments

To test the extent to which the conductance resonances in a single barrier are affected by disorder we have performed several thermal cycle experiments. At low temperature[3] the configuration of charged defects and ions is frozen; since it is the electric fields of these defects and ions that gives rise to the disorder potential at low temperatures the disorder potential is frozen into one realization of the ensemble of its possible configurations. However when the device is warmed to room temperature

[3]As a rule of thumb we consider $T \lesssim 50\,\text{K}$ to be a low enough temperature to fix the configuration of most impurities. To perform a thermal cycle we would like to warm the device up to at least $T \approx 200\,\text{K}$.

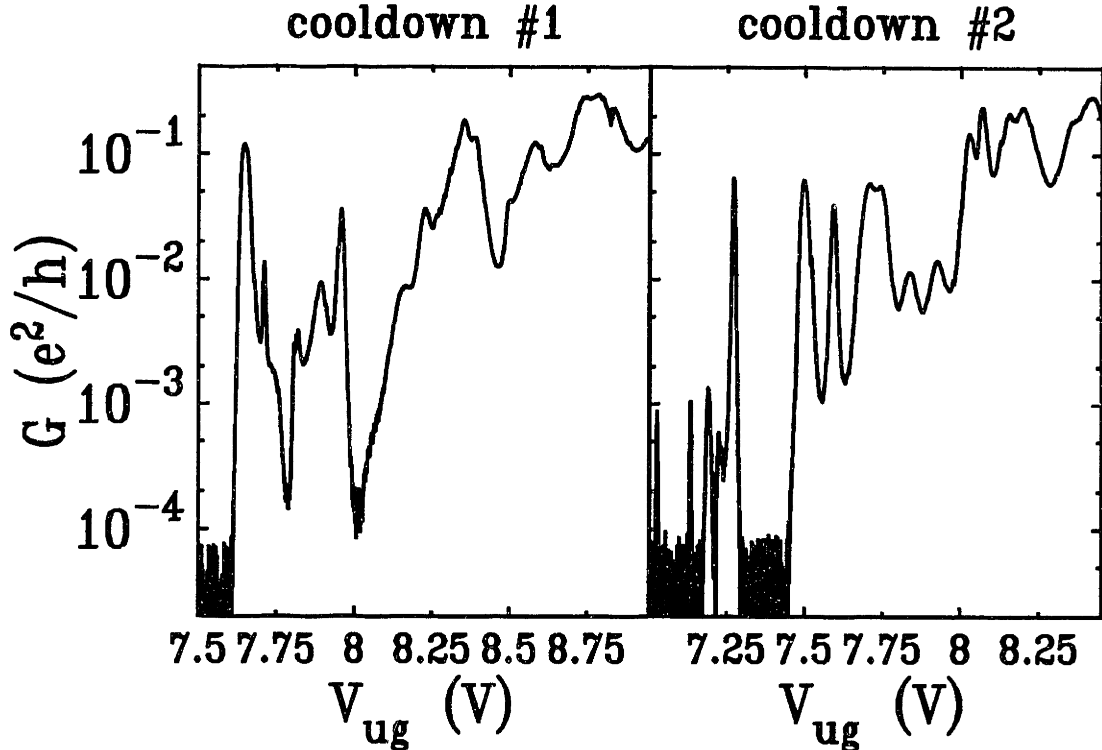

Figure 6-10: $G(V_{ug})$ for the same barrier before and after thermal cycle. The device is biased with the same lower gate voltages in both traces. The difference between the two plots shows that the electronic states of the barrier are greatly changed with thermal cycle; we may conclude that the conductance through the barriers is therefore dominated by the impurity potential. The average peak spacing is $\Delta V_{ug} \approx .10$ V during cooldown #1 and $\Delta V_{ug} \approx .11$ V during cooldown #2. For both plots data taken at $T = .32$ K, $V_l = -1.5$ V, $V_r = +1.5$ V, device F30 wafer #13. The gate geometry is an isosceles triangle of height 50 nm, with 150 nm gap.

the availability of thermal energy allows the disorder potential to fluctuate. When the device is cooled again the impurity potential will now be frozen into a different configuration than during the first cooldown. Changes of $G(V_{ug})$ with thermal cycle demonstrate that the electronic states of a single barrier and thus its conductance resonances are dominated by disorder. In particular we noted in section 3.1.6 that even in artificial atom whose size is defined by lithography the peak amplitudes will change when the device is thermally cycled; in these artificial atoms, however, the peak spacing will not be affected by a change in the disorder potential since the peak spacing is dominated by the Coulomb blockade of electrons confined to a lithographically defined area. Therefore we wish examine how both the amplitude and peak spacing change with thermal cycle.

In our devices both the peak spacing and the peak heights change as a function of thermal cycle. In figure 6-10 we plot $G(V_{ug})$ for the same device during two different cooldowns. Between cooldowns we warmed the device to $T \approx 280$ K for about 30

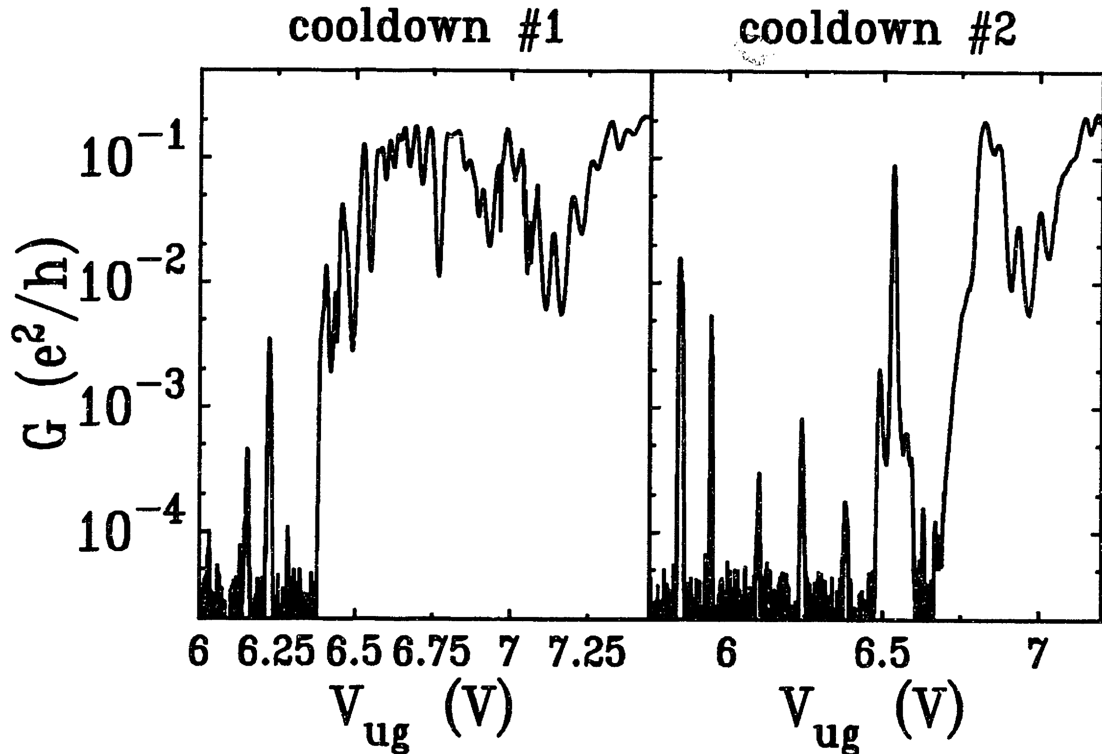

Figure 6-11: $G(V_{ug})$ for the same barrier before and after thermal cycle. The device is biased with the same lower gate voltages in both traces as is figure 6-10. The average peak spacing is $\Delta V_{ug} \approx .06\,\text{V}$ during cooldown #1 and $\Delta V_{ug} \approx .08\,\text{V}$ during cooldown #2. For both plots data taken at $T = .32\,\text{K}$, $V_l = +1.5\,\text{V}$, $V_r = -1.5\,\text{V}$, device F30 wafer #13. The gate geometry is an isosceles triangle of height 50 nm, with 150 nm gap.

minutes. The two traces are quite different and the conductance peaks in cooldown #1 seem to be unrelated to the conductance peaks in cooldown #2. The threshold for the onset of the conductance resonances has shifted by about $\Delta V_{ug} = .5\,\text{V}$ following the thermal cycle. In addition there do not appear to be any sets of peaks which have the same spacing in the two traces. This indicates that the electronic states in the barrier which give rise to conductance peaks have changed when the device was thermally cycled. All these observations are also true of the device presented in figure 6-11. While the peaks may differ between the two cooldowns the average peak spacing does not change markedly; in figure 6-10 the average spacings are $\Delta V_{ug} = .10\,\text{V}$ in cooldown #1 and $\Delta V_{ug} = .11\,\text{V}$ in cooldown #2 while in figure 6-11 the average spacings are $\Delta V_{ug} = .06\,\text{V}$ in cooldown #1 and $\Delta V_{ug} = .08\,\text{V}$ in cooldown #2. In section 6.2.1 we saw that the average peak spacing was related to the size of the barrier therefore we conclude that the size of the barrier does not change appreciably with thermal cycle. The device shown in figures 6-10 and the one shown in figure 6-11 have nominally identical lithographic dimensions and yet their average peak spacing is different; we

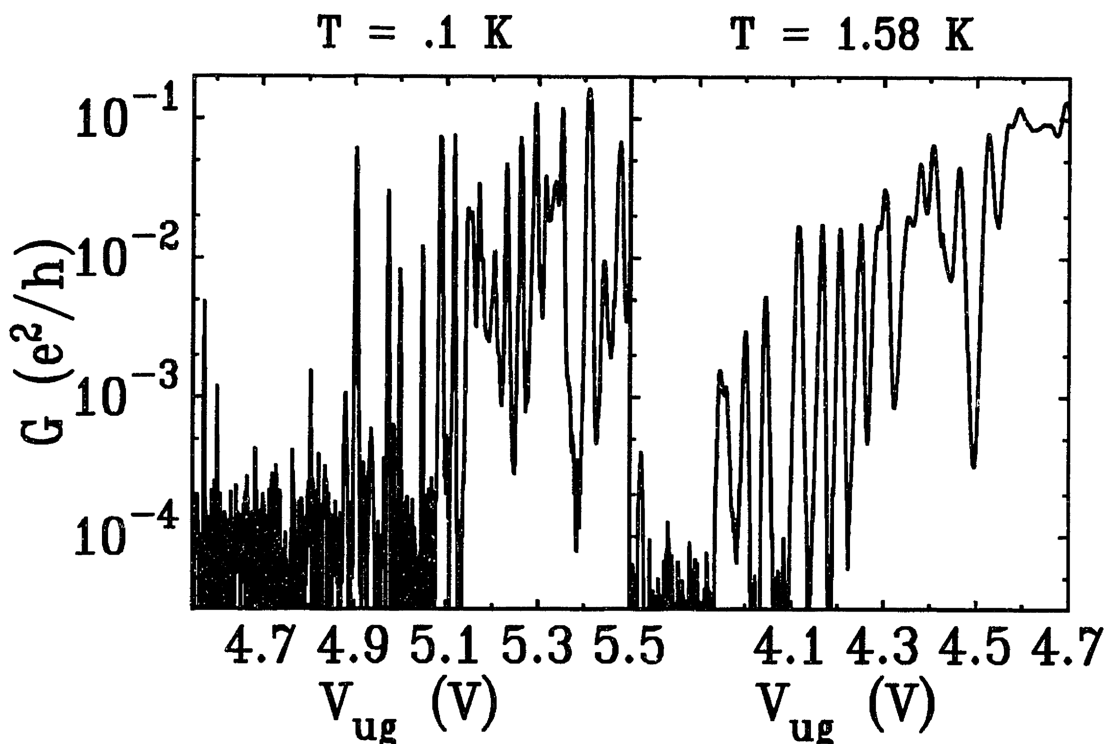

Figure 6-12: $G(V_{ug})$ for the same barrier at two different temperatures. While at higher temperature the peak spacing is regular at lower temperatures the spacing appear less regular. This may be due to our inability to measure certain peaks with very low conductance at $T = .1\,\mathrm{K}$, while at $T = 1.58\,\mathrm{K}$ these peaks have increased conductance. Data taken with $V_l = -1.5\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

may therefore conclude that the variations in size between these devices is due to fluctuations in the size of the gap written by electron-beam lithography and not to the fluctuations in the impurity potential.

From our observation that the conductance peaks totally change when the device is thermally cycled we may conclude that the conductance through the barrier is dominated by the impurity potential. However because thermal cycling does not change the average peak spacing we may also conclude that the size of the barrier is not sensitive to the disorder potential. Rather the size of the barrier is determined by the lithography, and fluctuations in nominally identical devices arise from the differences in the gate patterns that are written during electron-beam lithography.

6.2.4 Regular Spacing

In this section we wish to bring some additional examples of devices where the peak spacing is very regular. As we discussed in section 5.3.4 the regular spacing of peaks is particularly interesting and suggestive of the picture of electron puddles. For this

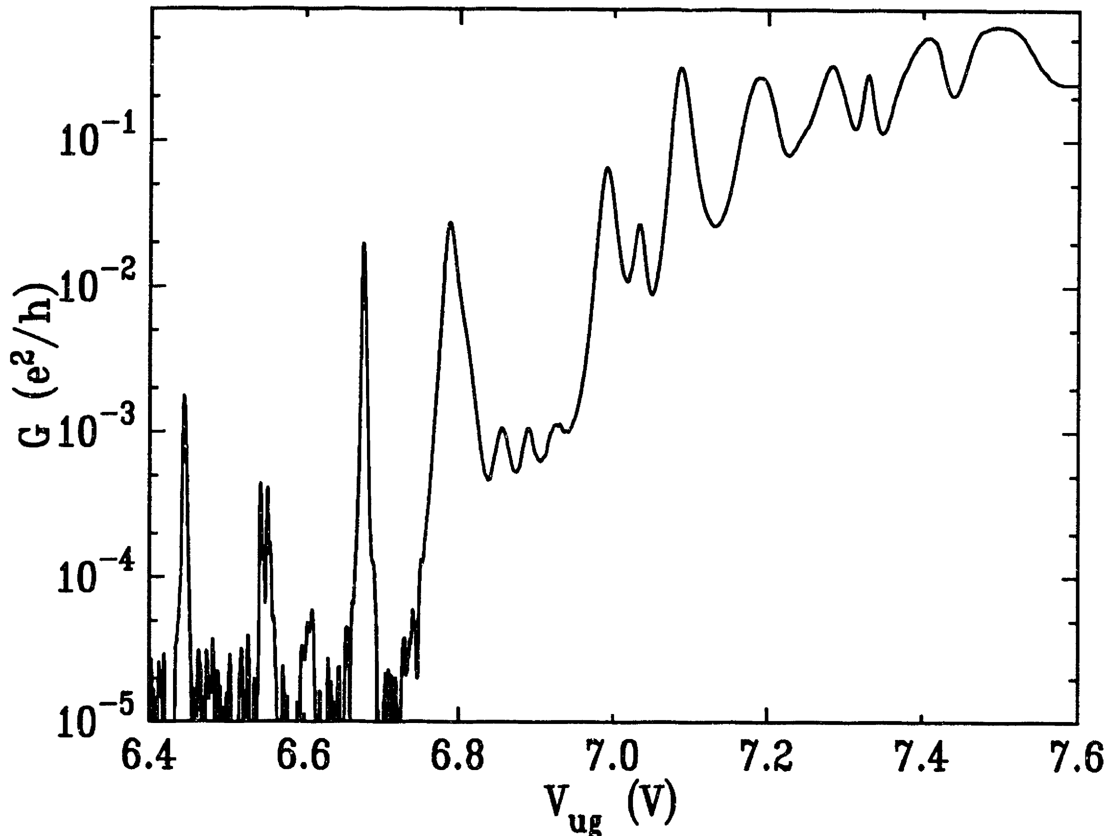

Figure 6-13: $G(V_{ug})$ showing many regularly spaced conductance peaks. Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -2.5\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

reason we would like to give some more attention to the circumstances in which the peaks are regularly spaced. Finally we do not want to leave the reader with the impression that only one device ever showed equally spaced conductance oscillations.

In some devices the peak spacing appears to be more regular as the temperature is raised. An example of such a device is presented in figure 6-12 where we see the $G(V_{ug})$ for two temperatures, $T = .1\,\mathrm{K}$ and $T = 1.58\,\mathrm{K}$. In comparing these two traces it appears that the peak spacing is more regular at higher temperatures. In part this is due to the fact that many of the conductance peaks have an amplitude that increases as a function of temperature (see section 6.3); in particular many of the lowest peaks have enhanced conductance at higher temperatures. Thus certain peaks that we observe at higher temperatures have conductances that are too low to measure at lower temperatures (see section 6.1.3); with these peaks missing $G(V_{ug})$ appears to have irregular spacing.

We draw the readers attention to the fact that many of the data sets that we already presented in this section do have regularly spaced peaks. In particular fig-

ures 6-1, 6-7 right, 6-9 $V_{left} = -3.0$, and 6-10 all show regular spacing. Finally we turn our attention to figure 6-13 which show a large number of regularly spaced peaks. Furthermore we wish to remind the reader that this system is not the only one in which regularly spaced peaks have been observed in the conductance of a single barrier. We saw in figures 5-1 and 5-2 that such peaks were observed in GaAs/AlGaAs heterostructures. Clearly the observation of such equally spaced peaks is compelling and understanding it is important.

We would like to close this section on the spacing of conductance peaks by summarizing what we have learned. We have found that the conductance peaks are due to transport through the narrow gap between lower metal gates, and that the peak spacing is well correlated with the size of this gap. The smaller the gap the larger the average spacing. We have also seen that the effective size of the barrier region may be smaller due to fluctuations in the lithography, and that the effective size may also be reduced by biasing the lower gate more negatively. Thermal cycling the device rerandomizes the impurity potential and changes the peak amplitudes and spacing, though it does not change the average spacing. Finally we have seen that many conductance traces from a variety of device can exhibit regularly spaced peaks.

6.3 Temperature Dependence of Conductance Peaks

The temperature dependence of a conductance resonances can give us a great deal of important information about the nature of the resonance. In particular if the width increases linearly with temperature, as we would expect (section 3.1.4), the slope of the line determines $\frac{C_g}{C_\Sigma}$, the conversion from gate voltage to energy; in addition the intercept of the line determines Γ, the natural linewidth of the resonance, and we may find the residual electron temperature, T_{res}, from the difference between the width of the base temperature peak and the width expected from Γ (see section 6.1.2). We have also seen that the temperature dependence of the amplitudes can be used to distinguish different tunneling regimes (section 4.3.1). In this section we present more data on the temperature dependence of conductance resonances. We will see that the temperature dependence of the peaks can not be simply understood from the theories that we have previously considered in sections 3.1.4 and 3.3.1.

We begin by considering how the peak shown in figure 6-5 changes with temperature. In the top panel of figure 6-14 we see the width of the peak as a function of

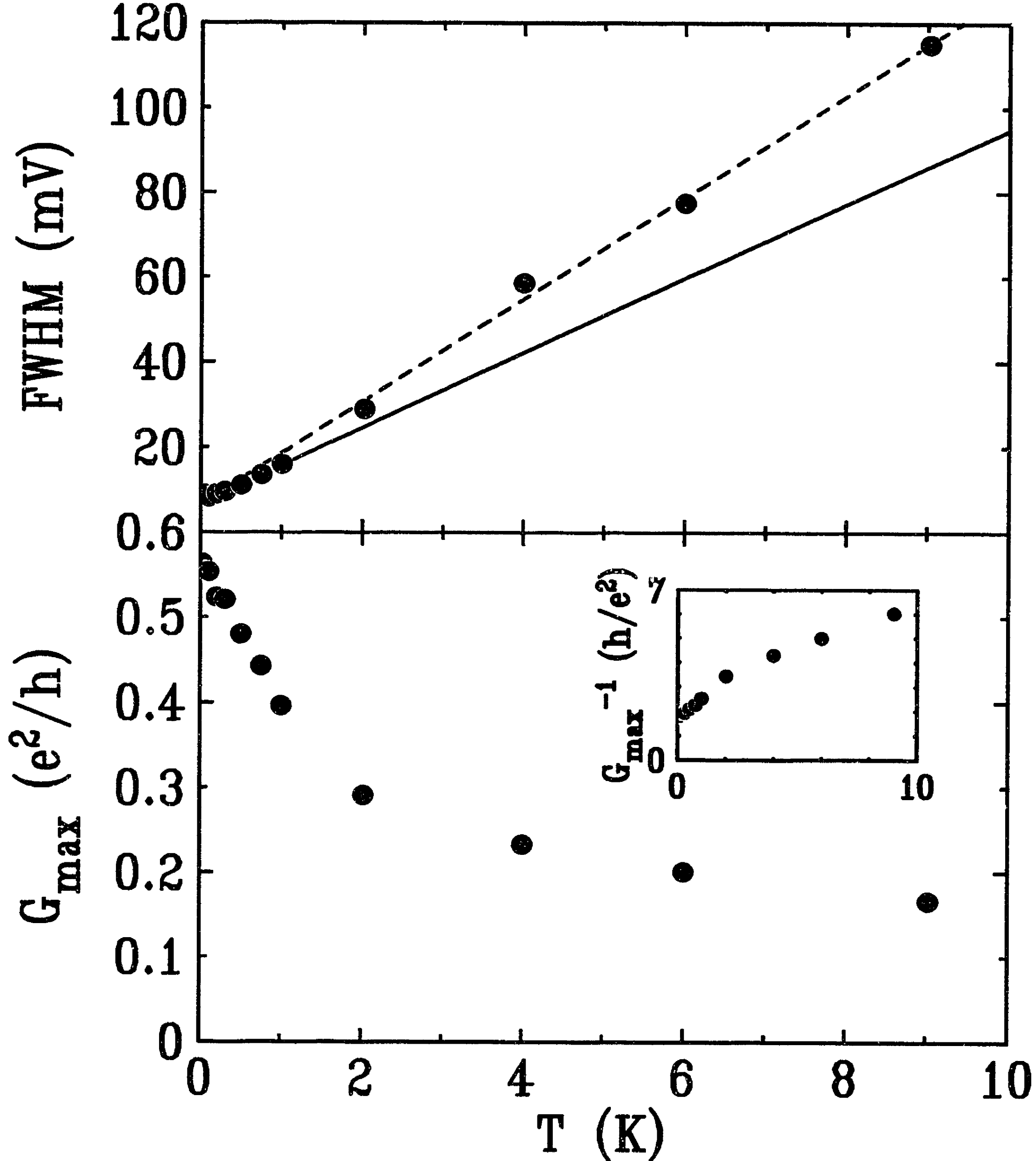

Figure 6-14: This figure shows the temperature dependence of the peak shown in figure 6-5. In the top panel we present the temperature dependence of the full width at half maximum. We fit the width to two lines: one in the temperature range $.1\,\mathrm{K} < T < 1\,\mathrm{K}$ (solid line), and one in the range $2\,\mathrm{K} < T < 10\,\mathrm{K}$ (dashed line). The different physical parameters extracted from these two fits are discussed in the text. We do not understand the nature of the crossover between these two range, but note that it occurs around $k_B T = \Gamma$. In the bottom panel we plot the temperature dependence of the peak amplitude, G_{max}, and in the inset we plot the inverse of the peak amplitude. The amplitude decreases with increasing temperature as expected for resonant tunneling when the peak shape is determined by the derivative of the Fermi-Dirac function. However at high temperature the expected behavior $G_{max} \propto T^{-1}$ is not observed, rather the amplitude seems to approach the asymptotic value $G_{max} \approx .11\frac{e^2}{h}$. Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -4.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

temperature over a broad range of temperatures. The first thing to notice is that the peak width increases with increasing temperature as we had expected. However instead of a simple linear increase, there seems to be two different linear regimes; while the linear fits in the two different ranges have different slopes, they have the same intercept. The linear fit in range $.1\,\mathrm{K} < T < 1\,\mathrm{K}$ is marked with a solid line while the fit in the range $2\,\mathrm{K} < T < 10\,\mathrm{K}$ is marked with a dashed line. When analyzing the line over the range $.1\,\mathrm{K} < T < 1\,\mathrm{K}$ we find $\frac{C_g}{C_\Sigma} = .035$, $\Gamma = 124\,\mu\mathrm{eV}$, and $T_{res} = .14\,\mathrm{K}$. Performing an identical analysis for the higher temperature regime, $2\,\mathrm{K} < T < 10\,\mathrm{K}$, we find $\frac{C_g}{C_\Sigma} = .025$, $\Gamma = 83\,\mu\mathrm{eV}$, and $T_{res} = .13\,\mathrm{K}$. We do not understand this crossover in the temperature dependence of the peak width; though it is noteworthy that there also seems to be a crossover in the behavior of the amplitude at the same temperature. Since the crossover seems to occur between 1 K and 2 K it seems reasonable to hypothesize that the crossover is related to the natural linewidth, $\frac{\Gamma}{k_B} \approx 1 - 1.5\,\mathrm{K}$. The discrepancy between the values of $\frac{C_g}{C_\Sigma}$ and Γ for these two fits give us some sense of the error that is associated with extracting the energy scales from the temperature dependence of the width. In figure figure 6-5 we used the parameters extracted from the fit at in the low temperature regime. However the expected lineshape that we plotted in that figure is not changed observably if we use the parameters for the high temperature regime because the $T = 0$ intercept of the two regimes is very similar despite the difference of 50% in Γ. Finally we would like to note that for this device we have independently measured $\frac{C_g}{C_\Sigma}$ by measuring the differential conductance at base temperature and solving equation 3.5. Our measurements agree well with those obtained above; for one lead we find $\frac{C_g}{C_\Sigma} = .026$ while for the other lead we find $\frac{C_g}{C_\Sigma} = .027$.

We would like to now turn our attention to the temperature dependence of the amplitude of the conductance resonance we have been considering. The temperature dependence of the peak amplitude, G_{max}, is shown in the bottom panel of figure 6-14, while the inset shows the temperature dependence of the inverse of the amplitude G_{max}^{-1}. As we discussed in section 3.1.4 we expect $G_{max} \propto T^{-1}$ when the peakshape is dominated by the derivative of the Fermi-Dirac function (equation 3.13), but at lower temperatures when $k_B T \ll \Gamma$ the amplitude is expected to saturate. In figure 4-9 we saw this sort of behavior though the crossover from a the temperature independent amplitude to $\Gamma_{max} \propto T^{-1}$ was more abrupt than expected. In this device the amplitude temperature dependence at low temperatures in consistent with the saturation we would expect to see for the convolution of a Fermi-Dirac derivative with a Lorentzian. However at higher temperatures the peak amplitude does not seem to

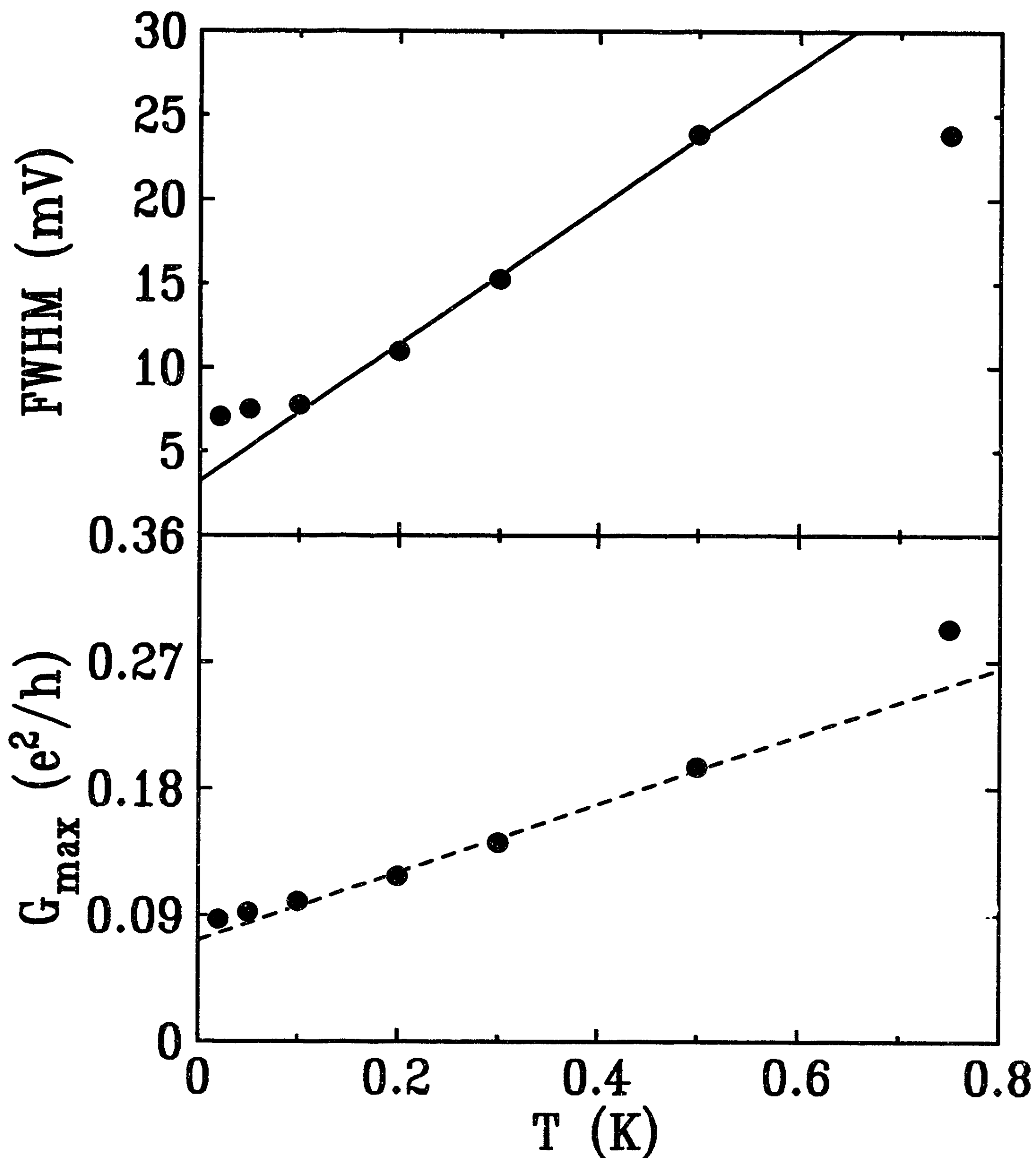

Figure 6-15: This figure shows the temperature dependence of the peak at $V_{ug} = 4.14\,\text{V}$ in figure 6-3 whose detailed lineshape is shown in figure 6-4. In the top panel we see the characteristic linear increase of the width of the conductance peak. At low temperatures we see the expected roll off of the width as the electrons decouple from the refrigerator and their temperature saturates at around $T = .12\,\text{K}$. In the bottom panel we see G_{max}, the amplitude of the conductance peak, *increasing linearly* with increasing temperature. We have fit the points in the range $.1\,\text{K} < T < .6\,\text{K}$ to a line to show how linear the increase is; such a linear increase of G_{max} is seen in a majority of the conductance peaks. This functional form is mysterious and is discussed at length in the text. Data taken with $V_r = -6.5\,\text{V}$, $V_l = +1.5\,\text{V}$, device G21 wafer #7. The gate geometry is a rectangle of length 40 nm, width 80 nm, with 90 nm gap.

be approaching the limiting value $G_{max} \propto T^{-1}$. Rather it seems to be asymptotically approaching $G \approx .11\frac{e^2}{h}$ instead of 0. Finally, as noted above, visual inspection of the curve in figure 6-14 reveals a crossover in the amplitude at $1\,K < T < 2\,K$ of unknown origin.

In figure 6-15 we plot the temperature dependence of the height and width of the peak shown in figure 6-4. Again we analyze the width data by fitting the width of the peak to a line between $.1\,K < T < .6\,K$ to determine the energy scales and find $\frac{C_g}{C_\Sigma} = .0074$, $\Gamma = 12\,\mu\text{eV}$, and $T_{res} = .11\,\text{K}$. A different choice of the temperature range would result in our finding different energy scales. Because the choice of the temperature range over which to analyze the peak width is the dominant source of error in this measurement we wish to briefly focus on the question of how sensitively the analysis depends on the choice of temperature range. In choosing the lowest temperature to use for fitting we avoid $T < .1$ because the electrons and the lattice decouple at those low temperatures making it difficult to know the actual electron temperature. If we considered the temperature range $.15\,K < T < .6\,\text{K}$, a slightly more restricted range than was considered above, we find: $\frac{C_g}{C_\Sigma} = .0071$, $\Gamma = 8.4\,\mu\text{eV}$, and $T_{res} = .13\,\text{K}$. We have not included the point at $T = .75\,\text{K}$ because at that temperature the peak to valley ratio is approximately two and it therefore becomes difficult to accurately measure of the width of the peak.[4] Having excluded $T < .1\,\text{K}$ and $T > .6\,K$ on physical grounds, we have seen that the variation of the quantities T_{res}, $\frac{C_g}{C_\Sigma}$, and Γ we find by choosing different ranges over which to fit the data is not very large. Even in our analysis of the data from figure 6-14 where we considered two very different ranges of temperatures ($.1\,\text{K} < T < 1\,\text{K}$ and $2\,\text{K} < T < 10\,\text{K}$) we saw that the variation of $\frac{C_g}{C_\Sigma}$ was less than 30%. The most sensitive parameter we compute is Γ because it depends both on the slope of the linear fit as well as its intercept; however even for this parameter the variation is less than 35%.

While we may understand the temperature dependence of the width of the peaks in figure 6-15, the dependence of the amplitude on temperature is far more mysterious. In the bottom panel we see that G_{max} is *increasing* with increasing temperature. As we saw from equation 3.12 we expect that for resonant tunneling G_{max} will not increase at higher temperatures. In these data, however, G_{max} actually seems to

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[4]This should not be surprising because the peak spacing around the peak we are examining is $\Delta V_{ug} = 70\,\text{mV}$ (see figure 6-3). Using $\frac{C_g}{C_\Sigma} = .075$, this corresponds to an addition energy of $U = .5\,\text{meV}$. We have seen (figure 4-10) that for a temperature $\frac{k_BT}{U} = .1$ thermal fluctuations of the charge can result in totally smeared features in the conductance. For the data in figure 6-15, we expect the fluctuations to be large when $T = .1\frac{U}{k_B} = .6\,\text{K}$, and thus we doubt the reliability of any points above this temperature.

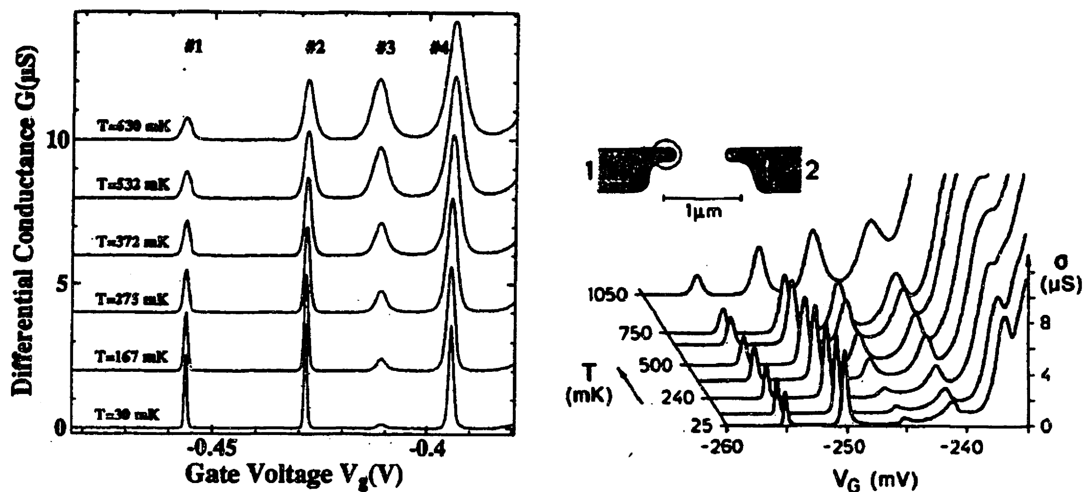

Figure 6-16: This figure shows how $G(V_g)$ changes as a function of temperature for the resonances in two different single barrier devices fabricated in a GaAs/AlGaAs heterostructure. The left panel shows the measurements of Nicholls *et al.* [1], while the right panel shows the measurements of Weis *et al.* [2]. Both studies observe that some conductance peaks have increasing as a function of increasing temperature while other conductance resonances have maximum amplitude that decreases with increasing temperature. In both studies the authors observe large number of equally spaced conductance resonances which we have interpreted as being due to tunneling through the electron puddles trapped in a single barrier (see section 5.3.4). The various temperature dependences of the conductance resonances that we have reported in this study and those found by Nicholls and Weis are similar, and we believe they are due to tunneling through the electron puddles in that are trapped in a single barrier.

be increasing linearly; this behavior is not confined to this particular peak but is seen in more than half of the peaks we have studied. In addition some of the conductance resonance in single barriers in GaAs/AlGaAs heterostructures also increase with increasing temperature as seen in figure 6-16.[5] While the hopping conductance increases with temperature the behavior of G_{max} must be distinguished from the functional form of equation 3.18, $G \propto \exp\left[-\left(\frac{T_0}{T}\right)^{\alpha}\right]$. The behavior observed in figure 6-15 has a finite conductance as the temperature is lowered, while for hopping we expect that the conductivity will be suppressed at lower temperatures just as activated behavior is suppressed as the temperature is decreased. Hypothesizing that the finite value of conductance is due to the small sample size is inconsistent with variable range hopping; either there exists a direct channel to tunnel from source to drain and resonant tunneling dominates, or the transport is due to multiple inelastic hops which give rise to the characteristic increasing temperature dependence[6] of equation 3.18. The remaining possibility is that the finite conductivity at low temperatures is due to the finite temperature of the electrons; if this is correct then we need only account for the amplitudes of the peaks in the range $T > .1\,\mathrm{K}$. Even in this more limited temperature range, the conductivity of the peaks that we observe increases by a large enough factor that we expect to see the typical sigmoidal curve associated with the temperature dependence of the hopping conductivity (see figure 3-4). This curvature is not observed in figure 6-15, nor is it in most of the other peaks that manifest enhanced G_{max} at higher temperatures. We must therefore conclude that the behavior of the peak amplitude in figure 6-15 is not consistent with either resonant tunneling or with hopping.

An alternative explanation for a peak amplitude that increases with increasing temperature involves postulating that the resonant tunneling that predominates at low temperatures is enhanced by a parallel conduction mechanism as the temperature is raised. Since the total conductance will be a sum of the two parallel channels we need to consider the temperature dependence of both the channels. For example

[5]The exact functional form of the increase of G_{max} with temperature for the peaks shown in figure 6-16 is not published by either Nicholls [1] or by Weis [2].

[6]The only consistent explanation that allows variable range hopping to have a finite value of conductance as $T = 0$ is to assume that there is a hopping path that gives rise to each conductance peak. Because of the small sample size each of the several states that the electron hops through has a finite width. At $T = 0$ residual transport is possible despite the fact that the levels in the hopping path do not align because each level has a finite density-of-states at the Fermi level because of its intrinsic levelwidth. As the temperature is increased inelastic process allow the electron to access a higher conductivity path thus leading to increased conductance. This explanation however requires that the all the resonances in the hopping path are distributed in energy by less then their width, which seems unlikely.

consider the case when electrons can tunnel through the ground state of N electrons trapped in the barrier or they can tunnel through an excited state that has a higher conductance. At low temperatures there will be no electrons in the leads with enough energy to tunnel through the excited state, and the conductance will be dominated by the contribution from resonant tunneling. As the temperature is increased the population of electrons in the leads at the energy of the excited state will rise, and so too will the excited state's contribution to the conductance. In artificial atoms conductance peaks whose amplitude increases with temperature have been shown to be correlated with a weakly coupled ground state in parallel with a strongly coupled excited state [38]. This conductance mechanism tends to give a rise in the conductance that is activated $G(T) - G(T=0) \propto \exp(-\frac{\Delta\varepsilon}{k_B T})$ with the activation energy being the excitation energy, $\Delta\varepsilon$; this is not we have observed in figure 6-15 which shows a linear increase in the conductance. However by postulating several excited states, each with an appropriate choice of couplings and energies, a linear temperature dependence of the peak amplitude can be constructed. Given our observation that the majority of conductance peaks have an an increasing amplitude with increasing temperature, it seems likely that the mechanism that gives rise to this behavior is not due to the accidental congruence of the excited state energies and couplings. While it has been suggested that this increased conductance may be due to many body effects, the temperature dependence of this peak remains mysterious.

In conclusion we have analyzed the temperature dependence of the width and amplitude of conductance peaks. We have seen that the temperature dependence of the width allows us to extract the conversion between gate voltage and energy and thereby extract the relevant energy scales of the device being studied; such analysis was used extensively when comparing the peak shape to theory (section 6.1.2). However there are some cases, not presented here, where the width is temperature independent. The cause of this behavior is not known and its occurrence is mentioned here for completeness. Furthermore we have seen that the temperature dependence of the peak amplitude is far more mysterious and can not simply be understood from the models that we presented in chapter 3. Only about one quarter of the conductance peaks display the characteristic decrease in peak amplitude with increasing temperature we expect for resonant tunneling. Another one quarter are essentially temperature independent, while the conductance of approximately half of the peaks increases with increasing temperature as we discussed in our analysis of figure 6-15. Finally we saw in figure 6-16 that conductance resonances in two different single barriers in GaAs/AlGaAs heterostructures also showed the same variety of temperature

dependences reported in our study; both of the GaAs barriers showed equally spaced conductance resonances suggesting the presence of a single electron puddle in each of these devices. This suggests that the various temperature dependences reported in this section are due to tunneling through electron puddles that are localized in a barrier.

6.4 Tunneling Spectra

By applying a bias across the single barrier we are studying we can measure the tunneling spectrum of the states within the barrier. In section 3.1.3 we showed that the tunneling spectrum, a measurement of the differential conductance as a function of applied bias, measures the tunneling density-of-states of the region being studied; this technique has proven its utility in the study of artificial atoms [14, 30, 15] and we used it to measure the excitation energy in section 4.3.2. In this section we present measurements of the tunneling spectra from several devices, with a particular focus on measurement of the tunneling spectra from the device shown in figure 6-1. We will find that these spectra are not a straight forward measurement of the density-of-states of the barrier region, but can give important information about the states localized in the barrier. The purpose of this section is to present some of the diverse behavior that we have observed when measuring the tunneling spectra.

Since the interpretation of features in the tunneling spectra can be complicated we begin by discussing how a feature's dependence on gate voltage which can help distinguish the nature of a feature. For example, we saw in section 3.1.3 that if a peak in the differential conductance is due to an excited state becoming accessible to tunneling as the state crosses the source Fermi level the feature's position in applied bias will shift in one direction as the gate voltage is increased (equation 3.4) while if the peak in differential conductance is due to an excited state crossing the drain Fermi level then the peak's position in applied bias will shift in the other direction (equation 3.3). In both of these cases the bias at which a feature appears in the tunneling spectrum is expected to shift linearly with changes in gate voltage because the energy of the state is being changed linearly by the gate's capacitive coupling to the state. If the energy of an electronic state does not depend linearly on gate voltage, but rather the nature of the electronic state changes as the gate voltage is changed then the bias at which the associated feature appears in the tunneling spectrum will

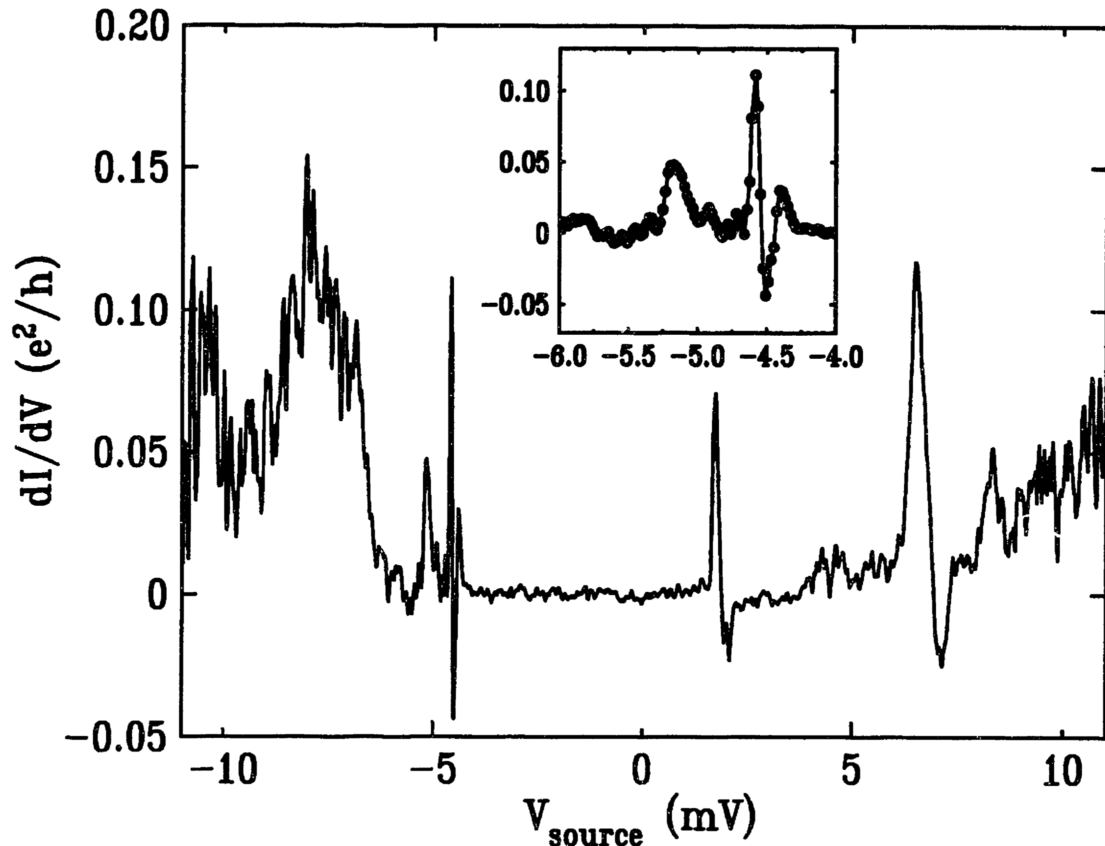

Figure 6-17: This figure shows the tunneling spectrum with the gate voltage set approximately 20 mV above the lowest conductance peak at the position indicated by arrow "a" in the plot of $G(V_{ug})$ shown in figure 6-1. In the figure shown here there is a well defined gap near zero bias as well as several well defined features; both observations are characteristic of spectra taken with the gate voltage set near the first conductance peak. Based on the gate voltage evolution of these features we find $\frac{C_t}{C_\Sigma} = .24$, and $\frac{C_\ell}{C_\Sigma} = .08$. Several of the features ($V_{source} = 2\,\mathrm{mV}$, $V_{source} = 7\,\mathrm{mV}$, $V_{source} = -4.5\,\mathrm{mV}$) show negative differential conductance; this feature has been observed in a number of other devices and is also seen in figure 6-18 and also in GaAs devices [1]. The inset shows a detailed view of the feature at $V_{source} = -4.5\,\mathrm{mV}$ showing that it too has clear signs of negative differential conductance. This trace was taken at $V_{ug} = 5.992$ (the discrepancy in V_{ug} from figure 6-1 is due to a drift in the position of the peaks). Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -3.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

not shift linearly with gate voltage.[7] It is also possible that there will be a feature in the differential conductance that is not due to transport through a particular localized state but rather is due to transport through the continuum of states; we would expect that the bias at which such a feature occurs may also change nonlinearly with gate voltage.

We wish to begin our discussion of the data by examining the tunneling spectrum shown in figure 6-17 which shows a well developed gap near zero bias and several sharp features. This spectrum was obtained at the gate voltage indicated by arrow "a" in the plot of $G(V_{ug})$ shown in[8] figure 6-1, and is in the region where the conductance between the peaks is less than our conductance noise floor. In most of the devices we have studied it is only when the gate voltage is set in the vicinity of the first peak that there is a well developed zero bias gap and sharp features whose gate voltage dependence suggests that they are due to excited states. As will be seen below in figures 6-19, 6-20 and 6-21 at higher gate voltages the zero bias gap is not as well developed and the gate voltage dependence of the features in the tunneling spectrum is far more mysterious. Based on the gate voltage dependence[9] of the features observed in figure 6-17 we may ascribe the features at $V_{source} = 2\,\mathrm{mV}$ and $V_{source} = 7\,\mathrm{mV}$ to the additional current as electronic states cross the source Fermi level (see equation 3.4). Similarly the features at $V_{source} = -4.5\,\mathrm{mV}$ and $V_{source} = -8\,\mathrm{mV}$ are due to electronic states crossing the Fermi level in the drain (see equation 3.3). Working with equations 3.5 and 3.6, we determine that $\frac{C_s}{C_\Sigma} = .24$, and $\frac{C_g}{C_\Sigma} = .08$; based on a similar study of the gate voltage dependence of the tunneling spectra when a bias is applied to

[7] An example of such a nonlinear shift would be the case where changing the gate voltage changes the shape of the potential that confines the electrons. While the the energy of electronic states in such a system will still be shifted due to capacitive coupling to the gate, the energy of the states will also be changed because the quantum mechanical eigenstates in the new potential will be different. In addition there are other more esoteric effects that can give rise to states whose energy does not change linearly with gate voltage. One particularly interesting case involves the Kondo resonance which is known from magnetic impurities in noble metals. Taking advantage of the analogy between atoms and artificial atoms, a similar effect has been predicted in artificial atoms [35, 34]. In such a system there would be a feature that developed at the Fermi level (zero bias) that would be independent of gate voltage.

[8] Figures 6-17, 6-19, 6-20, 6-21, and 6-22 show tunneling spectra from the device whose conductance as a function of gate voltage, $G(V_{ug})$ is shown in figure 6-3. The discrepancy of .45 V in the values of gate voltage between figure 6-3 and the figures shown in this section is due to the drift of the position of the peaks that occurred between the different experiments. The peak amplitudes and spacings, however, remained unchanged. To aid the reader we have marked the gate voltage positions in figure 6-3 with letters.

[9] The gate voltage dependence of all of the features shown in figures 6-17, 6-19, and 6-20 can be seen in two figures which show "movies" of the spectra. The movies shown in figures 6-21 and 6-22 are discussed below and show how the spectra evolve with gate voltage.

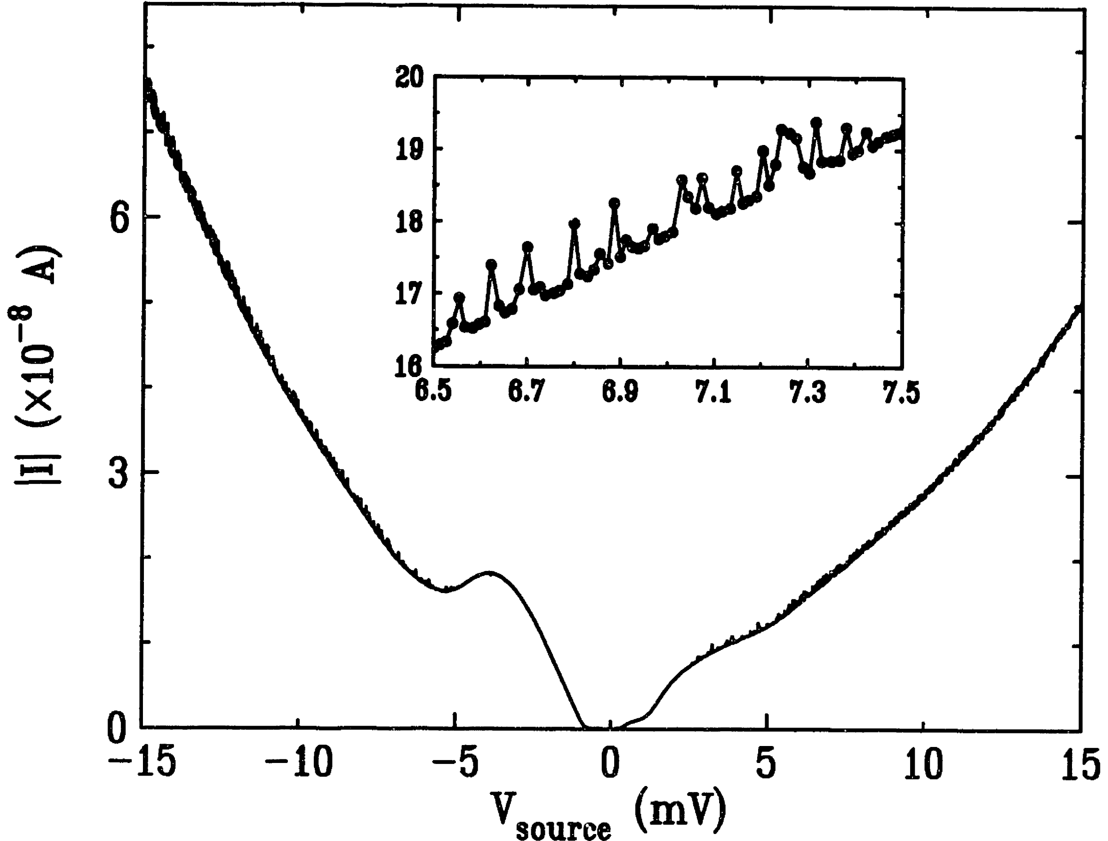

Figure 6-18: This figure shows current versus applied bias for the same device shown in figure 6-3 with $V_{ug} = 3.756$. This figure shows negative differential conductance with the current decreasing as the bias is increased from $V_{source} = -4\,\text{mV}$ to $V_{source} = -6\,\text{mV}$. Similar negative differential conductance is see in figure 6-17. In addition at higher bias, $V_{source} < -8\,\text{mV}$ and $V_{source} > 5\,\text{mV}$ there is an increase in current noise. In the inset we see an expand view of the current noise that shows that the measured current points are following two parallel curves. This bistability is due to a nearby charge trap charging and discharging. It is this type of switching that causes the noise that is seen at higher bias in all of the measurements of the differential conductance. Data taken with $V_r = -6.5\,\text{V}$, $V_l = +1.5\,\text{V}$, device G21 wafer #7. The gate geometry is a rectangle of length 40 nm, width 80 nm, with 90 nm gap.

the drain we find $\frac{C_d}{C_\Sigma} = .5$, and $\frac{C_g}{C_\Sigma} = .07$. These two measurements agree quite well and we can be confident that $\frac{C_g}{C_\Sigma} \approx .08$; furthermore, it is quite reasonable to assume that the remaining capacitance is due to the lower gates[10] thus giving $\frac{C_{lower}}{C_\Sigma} = 1 - \frac{C_s}{C_\Sigma} - \frac{C_d}{C_\Sigma} - \frac{C_g}{C_\Sigma} = .18$. We may then convert the spacing of features in figure 6-17 to find the spacing of excited states, $\Delta\varepsilon \approx 2\,\text{meV}$.

There are several other features of figure 6-17 that are noteworthy. Three of the features in differential conductance are not simple peaks, but rather also have a component where $\frac{dI}{dV}$ is negative; this behavior can be seen clearly in figure 6-17 in

[10]In general we find that $\frac{C_{lower}}{C_{ug}} \approx 2 - 4$. This value is therefore quite reasonable.

the features at $V_{source} = 7\,\mathrm{mV}$, at $V_{source} = 2\,\mathrm{mV}$, and can be seen in the inset of that figure where we have shown the feature at at $V_{source} = -4.5\,\mathrm{mV}$ on an expanded scale. Such negative differential conductance has been seen in many of the devices that we have studied. It has also been seen in studies of tunneling through the state of a single barrier in a GaAs device [1], as well as having been observed in artificial atoms. In figure 6-18 we show an $I(V_{source})$ trace from a different device which also shows negative differential conductance. In the latter figure, which is obtained by a DC measurement,[11] we can see the current decreasing as the applied bias is increased from -4 to -6 mV.

The other feature of figure 6-17 that is characteristic of the tunneling spectrum of these devices is the increase in noise at larger biases (seen in this figure at $V_{source} < -7\,\mathrm{mV}$). All of the other spectra that will be presented below also show such an increase in the level of noise. Again we turn to figure 6-18 where we observe that a higher biases there seems to be an increase in current noise. In the inset of that figure we have plot the current on an expanded scale; it is clear that the points plotted in the inset are following two parallel curves. This is exactly what would be expected if there were a nearby charge trap whose occupancy were fluctuating; the presence of the electron in the charge trap changes the potential of the barrier and effectively acts as a gate thus changing the current through the barrier. Since the trap only has two possible states we can think of measuring two different $I(V_{source})$ traces, one with the trap filled, and one with the trap empty. Which of the two possible functions $I(V_{source})$ determines the current will depend on whether the trap is occupied, while our ability to distinguish these two traces will depend on the switching rate of the trap.[12] The rapid changes in current that occur when a nearby charge trap switches its occupancy cause noise in the measurement of the differential conductance. Since in figure 6-18 we observe switching at higher biases, and we therefore expect the noise level in the differential conductance to increase at higher bias.

We now turn our attention to several other spectra taken at higher gate voltages. As we noted previously, tunneling spectra taken when the gate voltage is near the first conductance peak are different from the spectra taken at higher gate voltages

[11]Differential conductance is usually measured by adding a small AC bias to the applied DC bias. By using lock-in techniques to detect the AC component of current and make a direct measurement of the differential conductance. The observation of negative differential conductance using both techniques assures us that the phenomenon is not due to a problem with our instrumentation.

[12]In the measurement shown in figure 6-18 the response of our instruments is fast enough and the switching time slow enough to distinguish the two states. The response time of our DC measurement system is about 50 ms which is about six times faster than the response time of our lock-in measurement system.

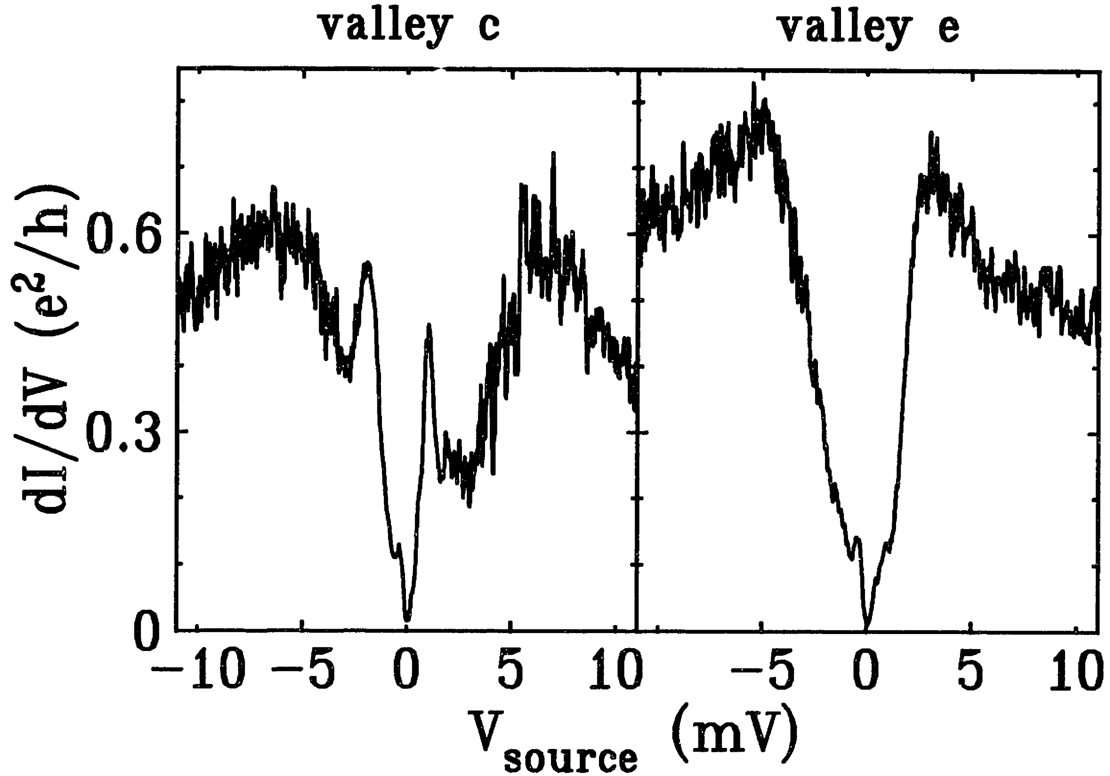

Figure 6-19: Tunneling spectra for the gate voltages labeled "c" and "e" in figure 6-1. In this region of gate voltage the zero bias conductance is finite even at the conductance minimum between peaks and the tunneling spectra have a minimum at zero bias despite the lack of a well developed gap. The additional features seen in these spectra do not evolve in gate voltage as would be expected for electronic states crossing the quasi-Fermi level in one of the leads. For this reason their origin is unknown. The trace labeled "c" was taken at $V_{ug} = 5.992$, while that labeled "e" was taken at $V_{ug} = 6.098$ (the discrepancy in V_{ug} from figure 6-1 is due to a drift in the position of the peaks). Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -3.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

when the minimum conductance is larger. In figure 6-19 we show two spectra taken in the valleys marked "c" and "e" in figure 6-1. In this gate voltage region the valley conductance is $\approx .02\frac{e^2}{h}$, well about our noise floor. The large value of conductance at zero bias is obvious in figure 6-19 where the value of differential conductance at zero bias does not vanish. It is important to notice that while there is a suppression of the differential conductance near zero bias there is no well developed tunneling gap. The absence of such a gap distinguishes this spectrum from those seen in artificial atoms dominated by Coulomb blockade; devices dominated by Coulomb blockade should have a tunneling gap when the gate voltage is between peaks. While these spectra show additional features such as the peaks in valley "c" at $V_{source} = -3\,\mathrm{mV}$, $V_{source} = -7\,\mathrm{mV}$, $V_{source} = 2\,\mathrm{mV}$ and $V_{source} = 7\,\mathrm{mV}$, the nature of these features is not clear from their dependence on gate voltage; in figures 6-21 and 6-22 just how

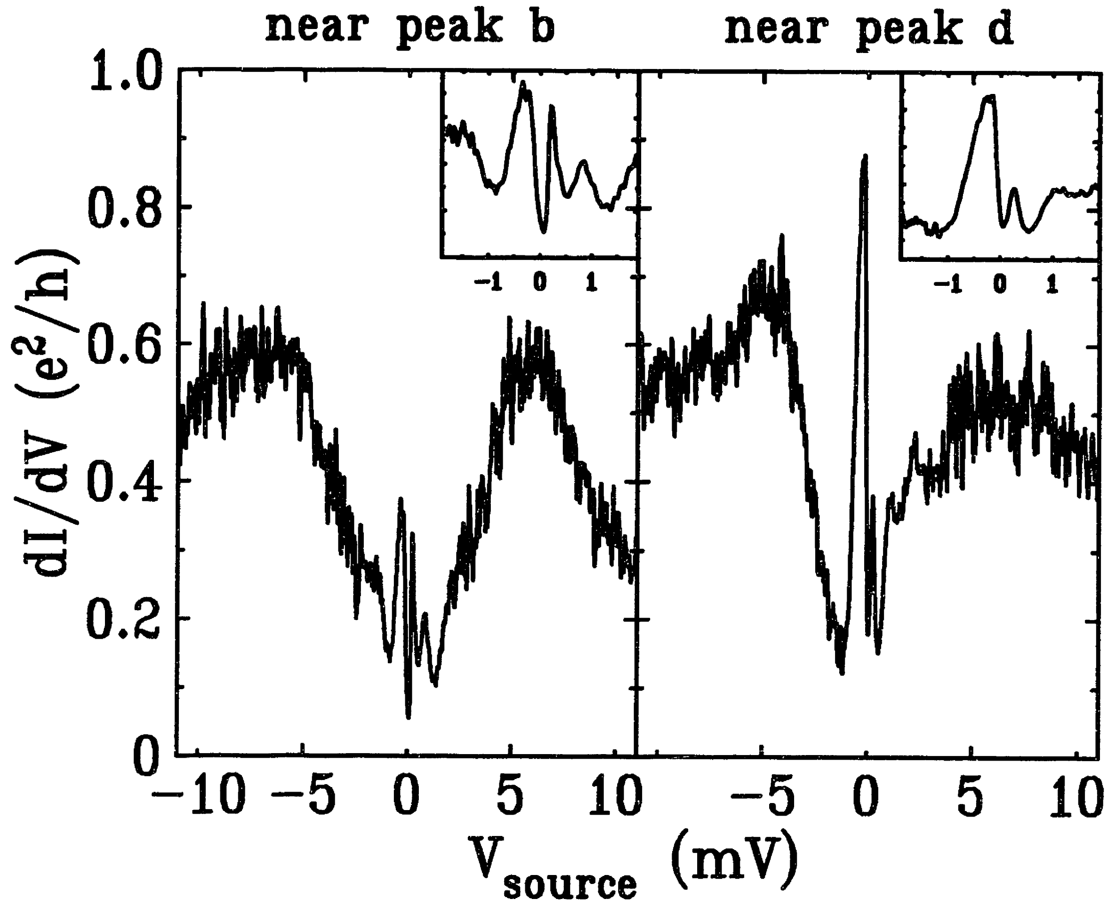

Figure 6-20: Tunneling spectra for the gate voltages labeled "b" and "d" in figure 6-1. In both panels the gate voltage is positioned near the maximum of a conductance peak. The insets in the upper right corner of each spectrum shows the differential conductance near zero bias in greater detail. Because these traces are taken near a conductance peak there is a finite zero bias conductance. In addition since the gate voltage is not exactly at the maximum of conductance a small change in the applied bias lines up the the center of conductance resonance with one of the quasi-Fermi levels which results then in an increase in current and a peak in differential conductance. The other features are more difficult to interpret because of their strange dependence on gate voltage. The trace labeled "b" was taken at $V_{ug} = 5.956$, while that labeled "d" was taken at $V_{ug} = 6.046$ (the discrepancy in V_{ug} from figure 6-1 is due to a drift in the position of the peaks). Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -3.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

peculiar the gate voltage dependence of these features really is.

In figure 6-20 we see spectra taken near the conductance peaks at the gate voltage values indicated by "b" and "d" in figure 6-1. We begin by examining the insets of this figure which show the differential conductance near zero bias is greater detail. Because both of these traces are taken near a peak maximum there is a finite zero bias conductance. In addition, because the gate voltage is positioned near a conductance resonance, a small change in the applied bias aligns the resonance with one of the leads giving a sharp rise in current and a peak in the differential conductance at a small bias, $|V_{source}| < 1\,\mathrm{mV}$. If the gate voltage were positioned to be at the peak maximum then the differential conductance would be maximum at zero bias. As we noted when discussing figure 6-19 the nature of the additional features that are observed in these spectra is not known.

Finally we would like to consider a "movie" of how the tunneling spectra change as a function of gate voltage. As we discussed earlier it is just such a measurement that helps us assess the nature of features in the differential conductance. In figure 6-21 we have plotted $V_{ug} + (.02 \times \frac{dI}{dV} \times \frac{h}{e^2})$ as a function of applied bias, V_{source}. Since there is a change in gate voltage, $\Delta V_{ug} = 3\,\mathrm{mV}$, between subsequent tunneling spectra the effect of plotting the data in this way is to offset subsequent spectra; using this method changes induced by the gate voltage in $\frac{dI}{dV}(V_{source})$ can be visualized. In figure 6-22 we have plotted the same data using the color of each point to represent the value of the differential conductance at that point. This second method emphasizes slightly different features; trends that are not visible in one rendering of the data may be easier to see in the other. We begin by considering the lowest gate voltage range $5.65\,\mathrm{V} < V_{ug} < 5.85\,\mathrm{V}$. In this range[13] we observe the gate voltage dependence of several of the features seen in figure 6-17. These features depend linearly on the gate voltage as expect from the analysis in section 3.1.3 and two characteristic slopes are visible, one in which the features move to higher V_{source} with increasing gate voltage, and one where features move to lower V_{source} with increasing gate voltage. It is by analyzing these slopes using equations 3.5 and 3.6 that we extracted the values of $\frac{C_g}{C_\Sigma} = .08$ and $\frac{C_s}{C_\Sigma} = .24$ that we noted above. As the gate voltage is raised above 5.85 V the tunneling spectra and their gate voltage dependence become more difficult to interpret. For example a careful observation of the region $5.9\,\mathrm{V} < V_{ug} < 6.1\,\mathrm{V}$ shows that the features have several different slopes; the interpretation of such behavior is difficult and was discussed on page 131. It is particularly interesting that in the

[13]Note that the values of gate voltage shown in figures 6-21 and 6-22 are .45 V lower than those shown in figure 6-1. See footnote 8 on page 133.

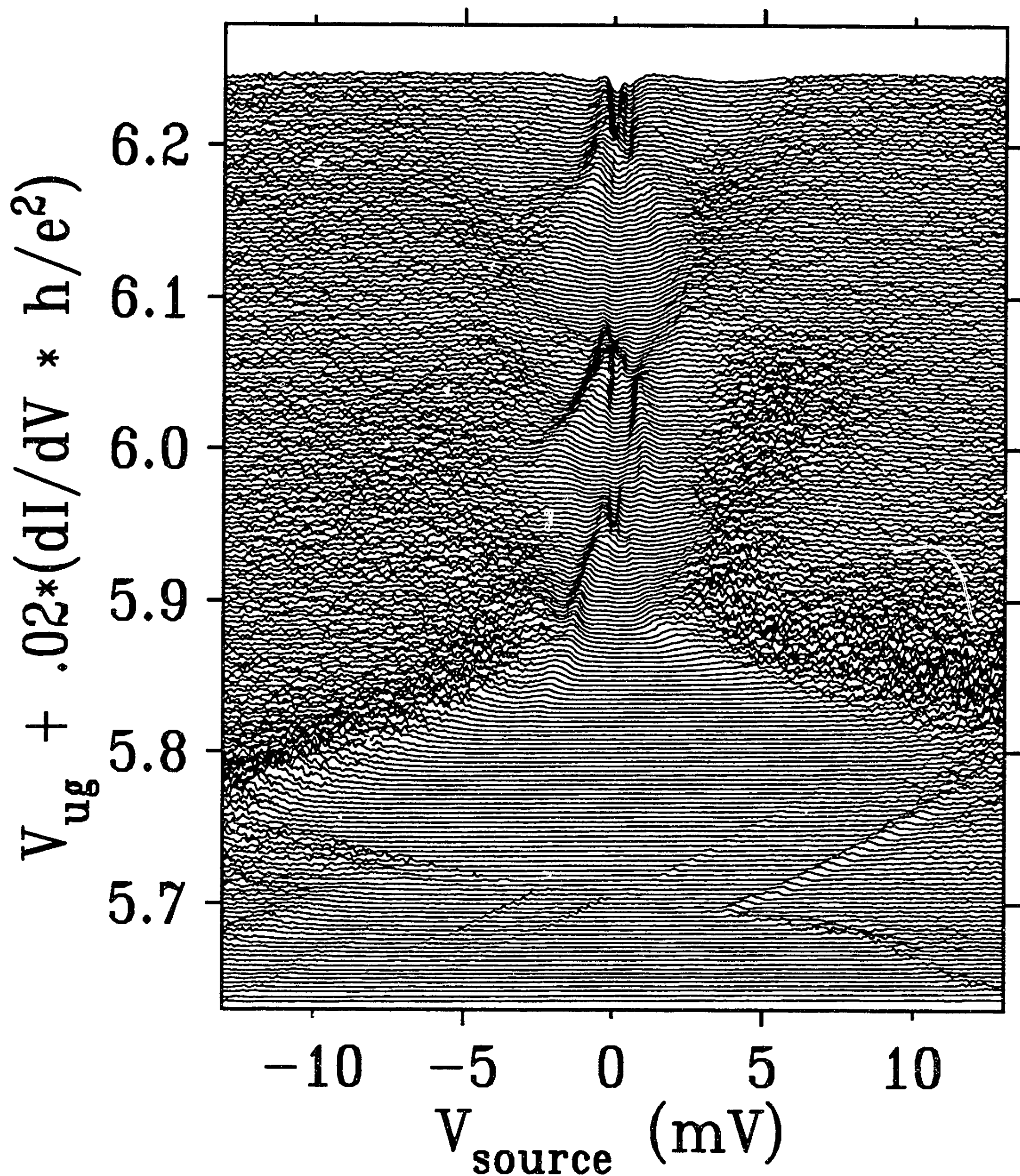

Figure 6-21: This figure shows the evolution of features in the tunneling spectra as a function of gate voltage. This is done by plotting $V_{ug} + (.02 \times \frac{dI}{dV} \times \frac{h}{e^2})$ as a function of applied bias, V_{source}, and changing V_{ug} by 3 mV from trace to trace. In the range $5.65\,\text{V} < V_{ug} < 5.85\,\text{V}$ the features in the tunneling spectrum shift linearly as discussed in section 3.1.3, while in the range $5.9\,\text{V} < V_{ug} < 6.1\,\text{V}$ the gate voltage dependence of the tunneling spectrum is not understood. Interestingly there is overlap of these two regions when $5.85\,\text{V} < V_{ug} < 5.9\,\text{V}$. Similar behavior is observed by Nicholls *et al.*and shown in figure 6-23 Data taken at $T \approx .1\,\text{K}$, $V_r = -3.0\,\text{V}$, $V_l = +1.5\,\text{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

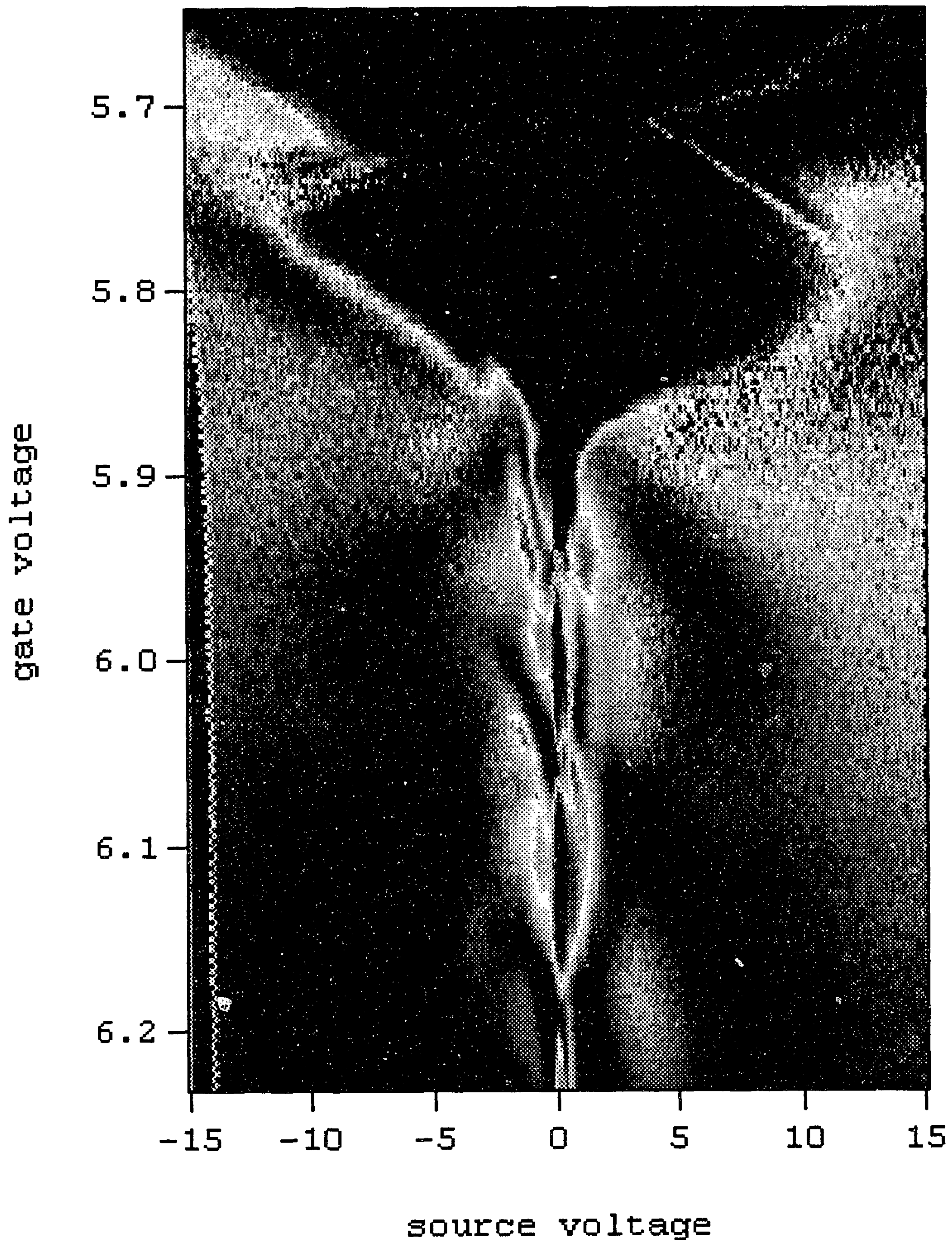

Figure 6-22: This figure shows the same data as seen in figure 6-21. Here we plot the source voltage versus the gate voltage as in figure 6-21 but use the magnitude of the differential conductance to determine the color of the point; larger values of the differential conductance are denoted by lighter colors. Plotting the data in this manner highlights different trends in the data. In particular some of the features in the range $5.9\,\mathrm{V} < V_{ug} < 6.2\,\mathrm{V}$ are clearer in this figure than in figure 6-21. Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -3.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$, device G20 wafer #7. The gate geometry is an isosceles triangle of height 100 nm, with 100 nm gap.

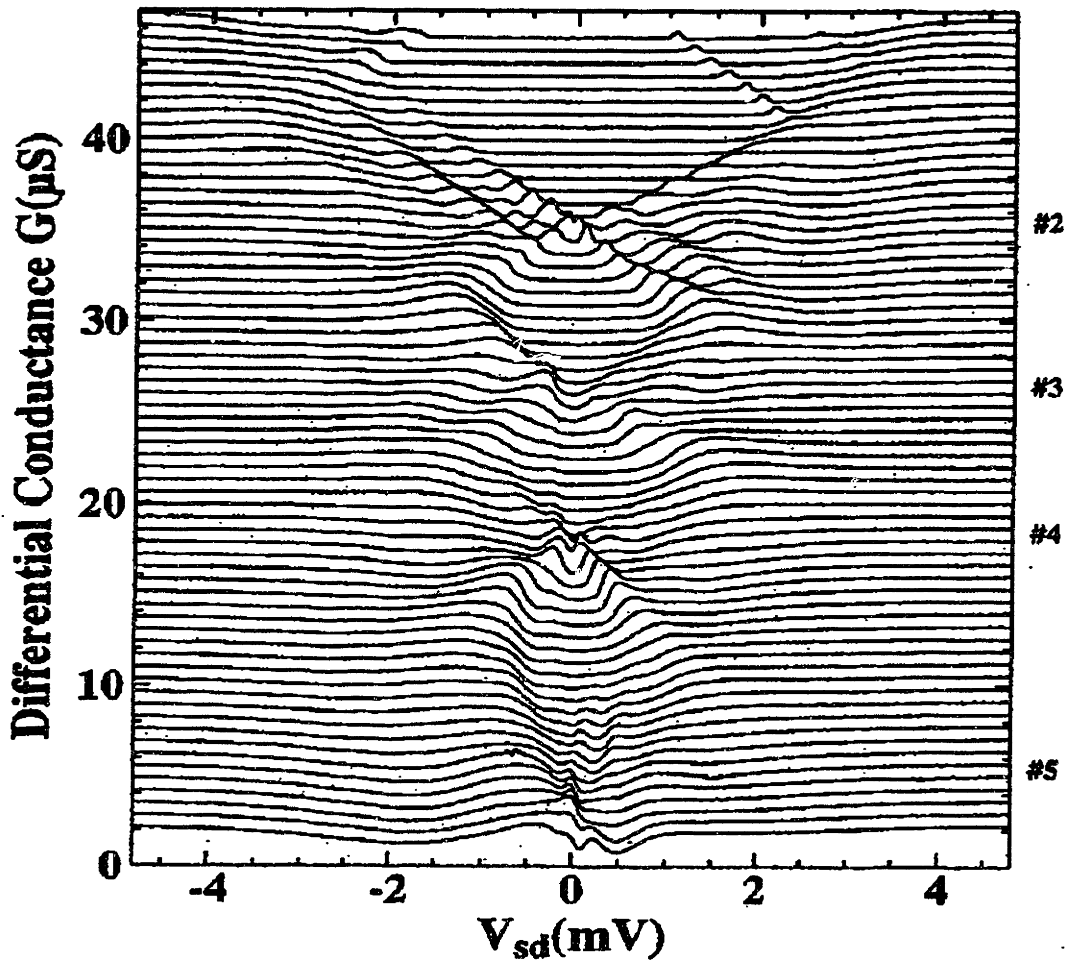

Figure 6-23: A movie The tunneling spectra of a single barrier in a GaAs/AlGaAs heterostructure device. This figure is obtained from Nicholls *et al.* [1]. This movie is a measurement of the same device that showed many periodic conductance peaks in a single barrier (figure 5-1), and the numbers on the on the ordinate labels the peak number as seen in the left panel of figure 6-16. Because of the strong evidence that the tunneling resonances in this device are due a single electron puddle, and because of the similarity of this figure to figure 6-21 we conclude that such behavior is intrinsic to the tunneling spectra of electron puddles.

region 5.85 V < V_{ug} < 5.9 V there is a feature at $V_{source} \approx -2$ mV. This feature is characteristic of the behavior of the tunneling spectra at higher gate voltage, but extends below 5.85 V where the gate voltage features from 5.65 V < V_{ug} < 5.85 V are still obvious. The overlap of these two sets of features exemplifies the strange behavior that is observed in this differential conductance movie. Finally we wish to draw the readers attention to figure 6-23 taken from Nicholls *et al.* [1] which shows a movie of the tunneling spectra that are qualitatively similar to figure 6-21. We recall that Nicholls *et al.* saw many periodic conductance peaks (figure 5-1) in this same device. Given the resemblance of the movies and the strong evidence that Nicholls *et al.* are studying a system with a single electron puddle we conclude that the strange qualitative features of the movies shown in figures 6-21 and 6-23 are intrinsic to the tunneling spectra of electron puddles.

We wish to conclude this section by reviewing the behavior of tunneling spectra from typical single barrier devices; much of this typical behavior have been observed in the device we presented above. When the gate voltage is in the vicinity of the first conductance peak we observed that the tunneling spectrum had a well developed gap, with clear features that evolved linearly in gate voltage. Some of the features observed in this range showed negative differential conductance, a finding that we saw in both DC and AC measurements and was also seen in GaAs barriers [1]. As the gate voltage is increased the nature of the spectrum at low bias changes, and there is no well developed tunneling gap. When the differential conductance is measured at a conductance peak there is a maximum at zero bias, but otherwise there is always a local minimum at zero bias. Finally we have seen that while the features in the differential conductance at these higher gate voltages do not have a linear dependence on gate voltage and can not be simply interpreted within the linear models presented in section 3.1.3 they are intrinsic to tunneling spectra of electron puddles.

6.5 Magnetic Field Induced Changes

In this section we discuss how an application of a magnetic field changes the conduction through a single barrier. As we discussed in section 3.1.5 the magnetic field changes the nature of the electronic states, and can therefore affect the transport of electrons. In our studies we have applied magnetic fields normal to the plane of the Si/SiO_2 interface and we are therefore affecting both the orbital and spin degrees of

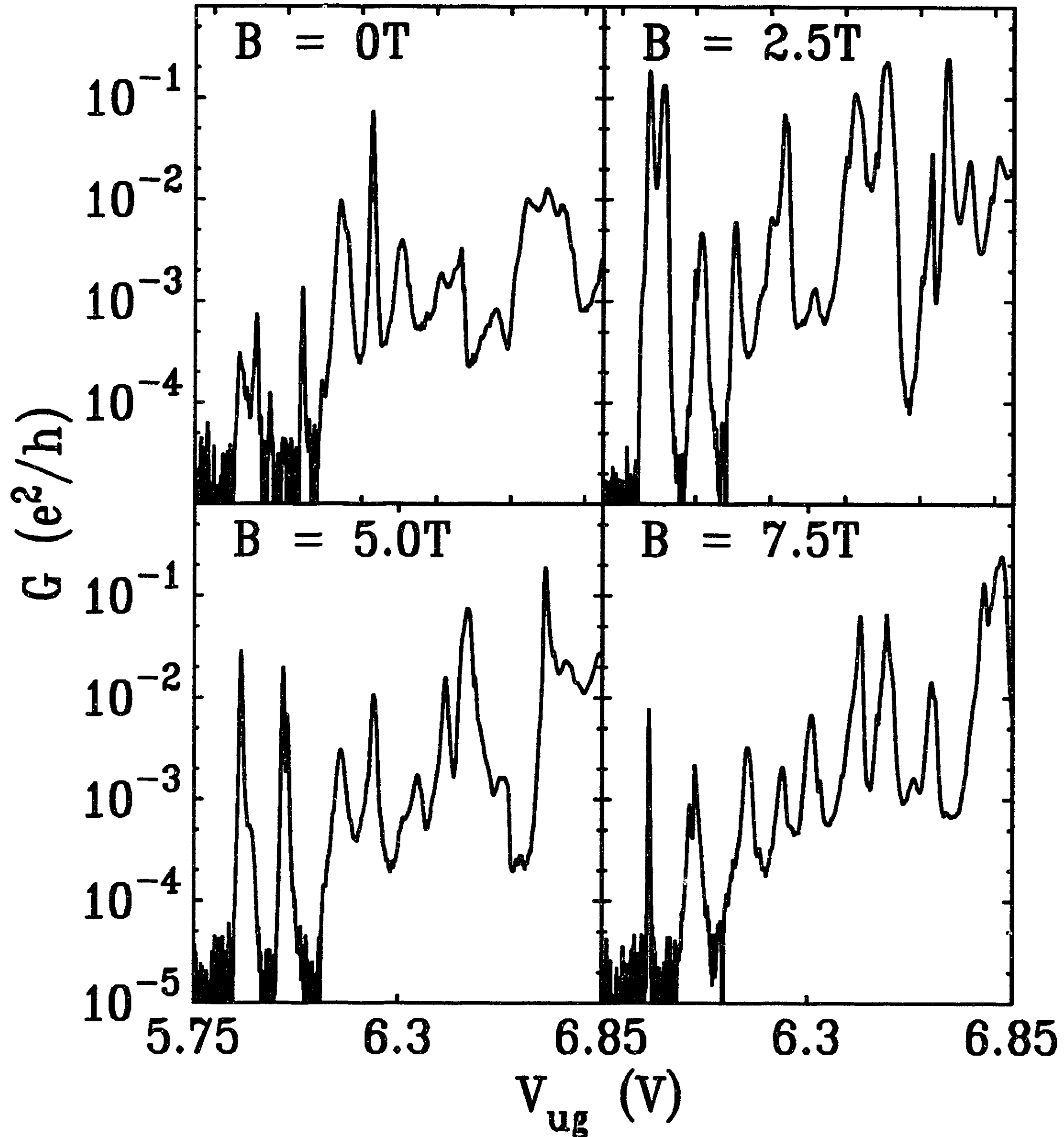

Figure 6-24: $G(V_{ug})$ as the magnetic field is changed by increments of 2.5 T from $B = 0$ T to $B = 7.5$ T. The figure shows that the amplitude, width, lineshape, and spacing changes as the magnetic field is increased. These changes shows that the transport through the electronic states in the barrier is sensitive to the magnetic field. The average peak spacing, however does not change, thus showing the size of the barrier region does not depend on magnetic field. In the trace at $B = 7.5$ T the peaks are equally spaced; we have observed this effect in several different devices. The meaning of these equally spaced peaks is discussed in the text. During each trace the field is being changed by $\Delta B = 50$ mT. Data taken at $T \approx .1$ K, $V_l = -1.0$ V, $V_r = +1.5$ V on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

freedom.[14] In our experiment we have applied fields that occur up to magnetic field strengths of 7.6 T. At these fields the electronic states in the two-dimensional electron gases in the leads do not change significantly, and therefore there are only minimal changes in the conductivity of the leads (see figure 2-4 and discussion of section 2.2). Therefore all of the changes that we study in this section are due to magnetic field induced changes in transport through a single barrier.

From the data in figure 6-24 it is clear that the magnetic field changes the nature of the electronic states that govern transport through the barrier. The amplitude, width, shape, and spacing of the conductance peaks change as the perpendicular magnetic field is increased from $B = 0\,\mathrm{T}$ to $B = 7.5\,\mathrm{T}$; a full "movie" of the changes induced by the application of a magnetic field is shown in figure 6-26. The movie shows that the field changes $G(V_{ug})$ in many ways which reflects the fact that the characteristics of each of the individual resonances themselves are changing as the field is increased. To verify that the observed changes in the conductance are due the magnetic field and not due to spurious changes in the system we standardly repeat all magnetic field experiments comparing the data obtained while sweeping the field up with the data obtained while sweeping the field down; we present only experiments in which the data show the same features independent of sweep direction, and we may be sure that the changes we observe in conductance are due to changes in transport through a single barrier caused by the magnetic field. While the magnetic field changes the individual resonances, it should be noted however, that the average spacing of the resonances does not change over the field range that we have examined. Since we saw in section 6.2 that the peak spacing is a measure of the device size, we may therefore conclude that the effective barrier size does not change as the magnetic field is applied.

The conductance resonances are not suppressed as the magnetic field is increased, but rather many of the resonances have increased coupling at higher magnetic fields. For example, the feature at $V_{ug} = 5.9\,\mathrm{V}$ in figure 6-24 has a conductance of $G \approx 5 \times 10^{-4}\,\frac{e^2}{h}$ at $B = 0\,\mathrm{T}$, which grows with increasing field and is 400 times larger at

[14]By applying a magnetic field that is in the plane of the Si/SiO_2 interface it is possible to distinguish between orbital and spin degrees of freedom. The magnetic field only affects electrons as they gather phase by moving in the field and having their different Feynman paths enclose flux. Because the electrons are very tightly confined in the plane of the Si/SiO_2, with a spatial extent of only several nanometers, their different paths can not enclose much flux and therefore the field does not significantly affect their orbital motion. However their spins still couple to the magnetic field, and therefore any changes that are seen in a parallel field are due to spin effects. While the actual situation is not quite so simple, we will not dwell on the details here because in our experiments we have only applied perpendicular magnetic fields.

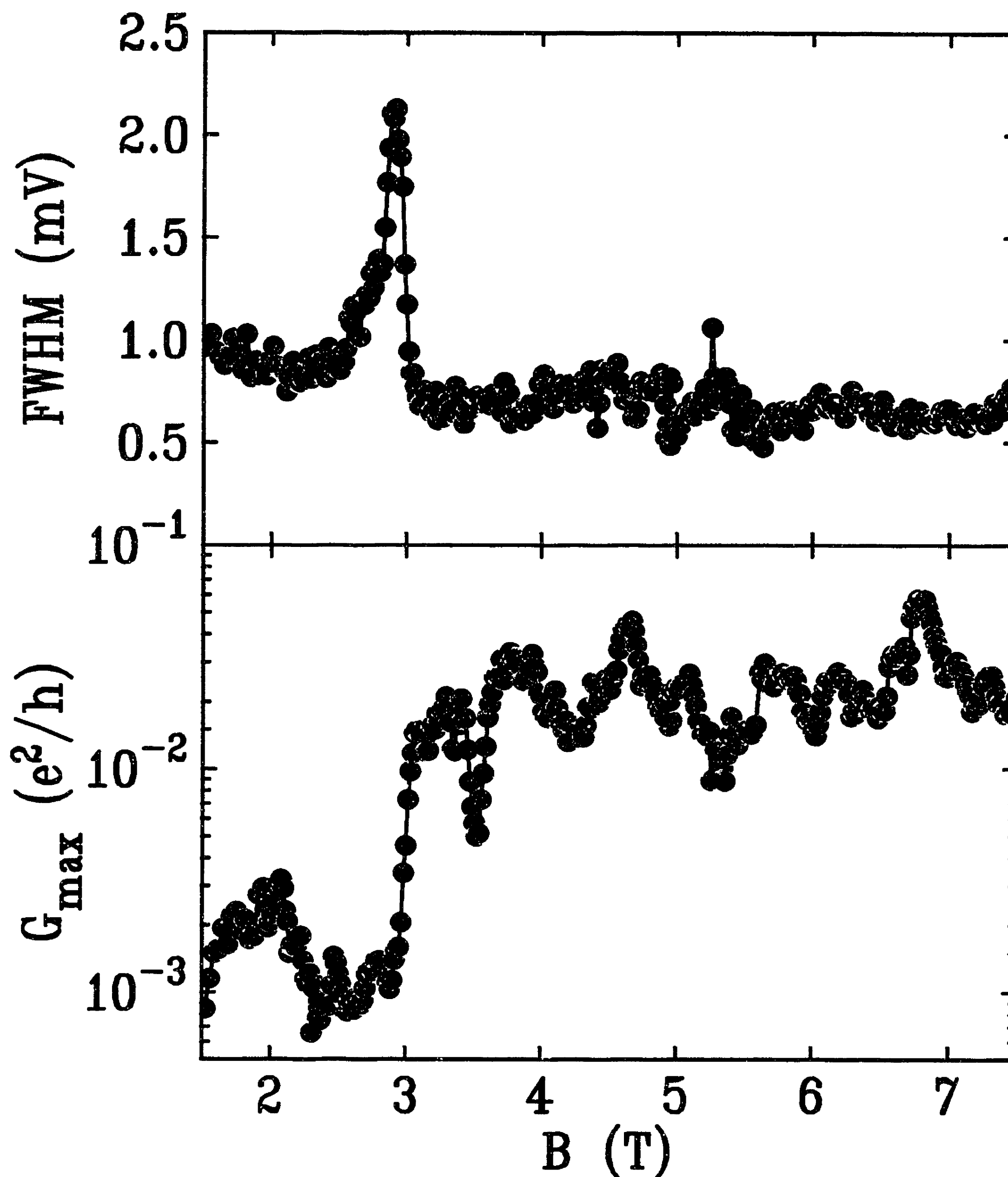

Figure 6-25: The width, $FWHM$, and amplitude, G_{max} of a conductance peak is plotted as a function of perpendicular magnetic field. These values are obtained by fitting the measured conductance peak at magnetic field intervals of 16 mT. At $B = 3$ T the state responsible for electron transport through the barrier undergoes a transition; the amplitude increases by a factor of twenty, and the width increases by a factor of two over a narrow field range, $\Delta B = .18$ T. These changes are due to increased coupling between the state in the barrier and the leads. This result is particularly surprising because increasing the magnetic field tends to localise electrons and reduce their coupling to the leads. During each trace the field is being changed by $\Delta B = 50$ mT. Data taken at $T \approx .1$ K, $V_r = -1.5$ V, $V_l = +1.5$ V on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

$B = 2.5\,\mathrm{T}$. This increased coupling is particularly surprising based on our expectation that a perpendicular magnetic field will enhance the confinement of electrons and decrease the conductance (see sections 3.1.5 and 3.3.2).[15] Another example is shown in figure 6-25 where we plot the width and amplitude of a conductance peak as a function of magnetic field. In this figure there is a distinct feature in both the peak width and amplitude that occurs at $B = 3\,\mathrm{T}$ which indicates that the state through which the electron is tunneling has enhanced coupling. At this field the peak amplitude increases by a factor of twenty and the width of the conductance peak increases by a factor of two over a narrow range in field, $\Delta B = .18\,\mathrm{T}$. From the discussion in section 6.1.2 it is clear that the width of some conductance peaks is determined not by thermal broadening but by the natural lineshape of the resonance, we therefore interpret the sudden rise in the peak width seen in the bottom panel of figure 6-25 as a rise in the natural linewidth of the resonance.[16] On page 45 we saw that the coupling that determines the total width of the peaks is calculated by considering conductors in parallel and is therefore dominated by the more conductive barrier, while the coupling that determines amplitude is calculated by considering conductors in series and is therefore dominated by the less conductive barrier. Thus the rise in the width of the peak is interpreted as increased conductance in the more transparent barrier, while the rise in the amplitude of the peak implies increased conductance in the more opaque barrier. However the rise of both couplings at the same field implies that the electronic state which is responsible for conduction has undergone a more fundamental change. In fact the temperature dependence of the conductance peak changes; at low fields the amplitude of the conductance resonance increases with increasing temperature, while at high fields the amplitude decreases with increasing temperature as would be expected for resonant tunneling.[17] We have observed similar transitions where the width of a conductance peak increases at higher fields in several different devices. It appears that this phenomenon is general despite

[15]The conductance through a barrier should be suppressed when the one flux quantum pierces the area enclosed by the Feynman paths that contribute to tunneling. If the width of the barrier is estimated at $w = 20\,\mathrm{nm}$, and the strength of the perpendicular field is $B = 7.5\,\mathrm{T}$ then we expect tunneling to be suppressed when an electron is tunneling a distance of $\frac{\Phi_0}{Bw} = 27\,\mathrm{nm}$.

[16]The measured width of the conductance resonance is in units of gate voltage. To convert the width in gate voltage to a width in energy we must multiply by $\frac{C_g}{C_\Sigma}$. Therefore it is possible that rise in the measured width is due to a sudden change in $\frac{C_g}{C_\Sigma}$ at $B = 3\,\mathrm{T}$ and not to a change in the energy scale that determines the resonance width. Whatever the nature of the rise in the width of the conductance peak, it is clear that at $B = 3\,\mathrm{T}$ there is a transition of the state responsible for electron transport.

[17]For a more detailed discussion of the significance of increasing conductance with increasing temperature and of the temperature dependence in general see section 6.3.

the surprising nature of the increased coupling at magnetic fields of several Tesla.

Another important effect that the magnetic field can have on the electronic states in a barrier is seen in figure 6-24 where at $T = 7.5\,\mathrm{T}$ the conductance peaks are equally spaced. As we discussed in section 5.3.4 equally spaced conductance peaks are a sign that each subsequent electron is being add to the same metallic region rather than being trapped in individual localized states. We also speculated that if electrons in a disordered region do break up into "puddles," than there may be several such puddles in a single barrier thus masking the equal spacing that we expect from a single puddle. It is within this context that we wish to interpret our observation that the application of a perpendicular magnetic field can cause the peak spacing to become periodic.

Based on the lowering of the effective electrostatic energy due to the exchange interaction it has been hypothesized [66, 67] that electrons arrange themselves in a compact distribution in artificial atoms. In systems where the electrons are confined by the external potential there is a competition between the repulsion of the electron-electron interaction and the attraction of the exchange interaction. Since the exchange interaction is short range and only affects electrons with overlapping wavefunctions the exchange attraction seeks to maximize the number of electrons occupying wavefunctions that do have an overlap with other occupied states. The exchange energy can therefore be thought of as giving rise to a surface tension term in the Hamiltonian [65] that favors compact electron puddles, however because of Fermi statistics the effective surface tension only attracts electrons in the same spin state to each other. In [19] a careful experimental study revealed that these effects can be observed in artificial atoms; there Klein *et al.* found that as the the exchange effects can be tuned by an application of the perpendicular magnetic field and the subsequent alignment of the spins of the electrons.[18] Therefore as the magnetic field is increased we might expect that it will be energetically favorable for any electron puddles localized in a barrier to coalesce into a single puddle. In such a case the conductance traces would only have equally spaced conductance peaks at values of the magnetic field where the surface tension has forced the electrons to coalesce into a single electron puddle. It is just such behavior that is observed in figure 6-24.

[18]It should be noted that the alignment of the spins that enhances the exchange interaction in [19] is not due the Zeeman energy. Rather it is a complex interplay between the confinement potential, the electron-electron interaction, and the degeneracy of each of the Landau levels that the electrons occupy. As the field is increased the degeneracy of the Landau levels is increased and more electrons can be accommodated in the same spin state,thus causing the electrons' spin to become aligned at higher magnetic fields.

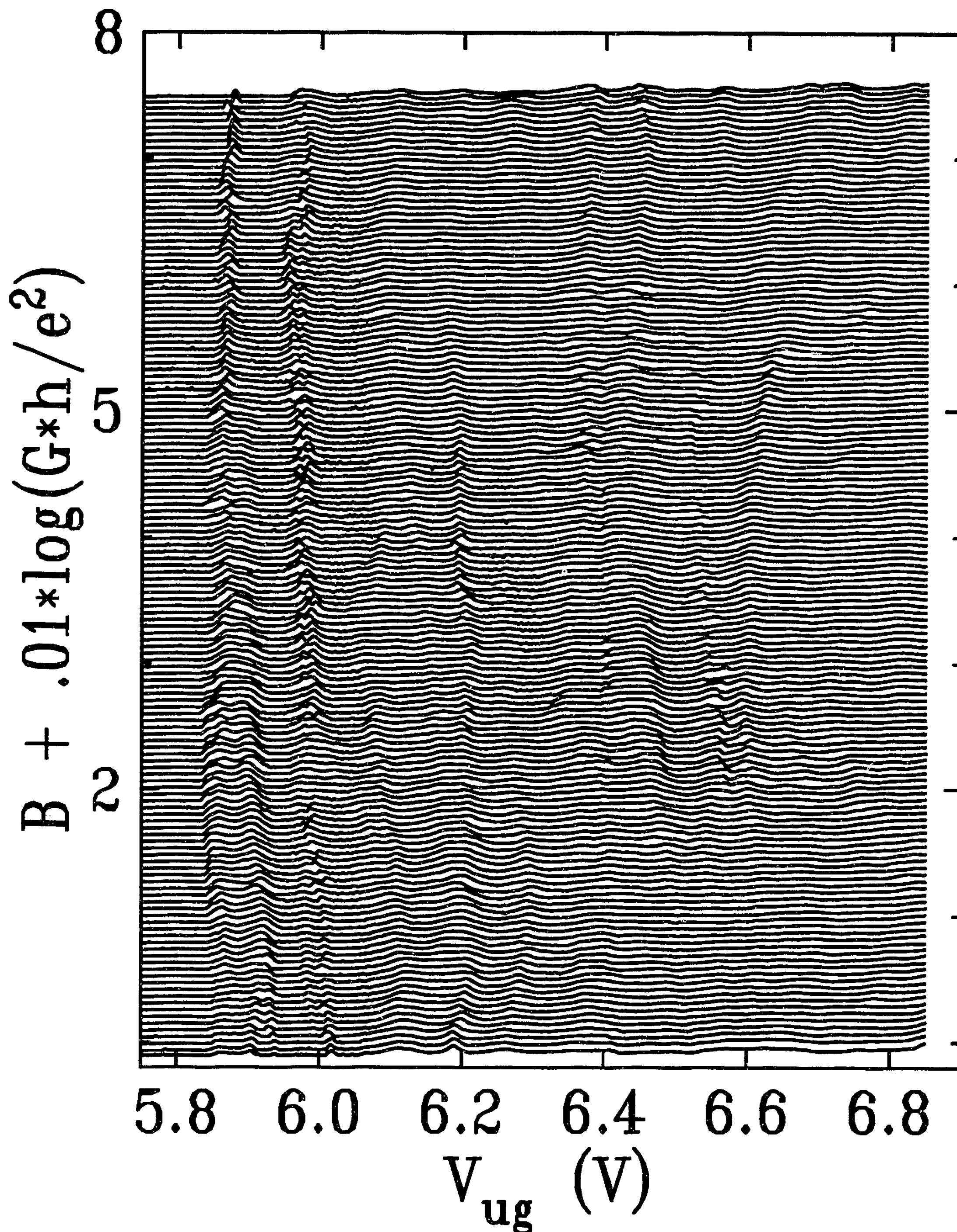

Figure 6-26: This plot shows a movie of how $G(V_{ug})$ changes as a function of magnetic field. The graph actually plots $B + .01\log(G \times \frac{h}{e^2})$ as a function of gate voltage, where B is in units of Tesla. The field changes by $\Delta B = 50\,\mathrm{mT}$ from trace to trace, and thus each subsequent plot of $G(V_{ug})$ is offset by a constant amount. In this way changes induced by the magnetic field in $G(V_{ug})$ can be visualized, and we observe that the spacing, amplitude, and width of conductance resonances change in complex ways as a function of perpendicular magnetic field. Data taken at $T \approx .1\,\mathrm{K}$, $V_l = -1.0\,\mathrm{V}$, $V_r = +1.5\,\mathrm{V}$ on device B30 wafer #13. The gate geometry is a right triangle of 50 nm gap.

Chapter 7

Conclusions

In this thesis we have presented our work studying nanostructures in a silicon MOS system. We have successfully fabricated and measured the first electrostatically confined artificial atoms in a Si/SiO_2 system. Using a layer of SiO_2 20 nm thick we have positioned the confining gates closer to the two-dimensional electron gas than was possible in an GaAs/AlGaAs system, thus allowing us to create a sharper confining potential. In a device of size $250\,\mathrm{nm} \times 250\,\mathrm{nm}$, one of the larger devices we fabricated, we found that the addition energy was $U = 1.9\,\mathrm{meV}$, several times larger than previous work [13]. However, studying these double barrier devices was complicated by the the existence of tunneling resonances in each of the two barriers which we used to isolate the artificial atom from the leads.

Our serendipitous discovery of resonances in a single electrostatically defined barrier indicates that electrons can be localized by the impurity potential. Much of this thesis has been devoted to the careful study of the strange properties of these resonances. We have found that the temperature dependence and the tunneling spectra of these localized states can not be fully explained within a single-particle picture. We have also found that similar resonances in a single barriers are reported in a diverse set of different material systems. We have considered the possibility that the electrons might be localized in a barrier by their attraction to image charges they induce in nearby metallic regions and find that this mechanism could not account for the localization of electrons in these devices. Furthermore, we have performed several different experiments which show conclusively that the localized electronic states are a consequence of the disorder in the samples.

One of the most surprising properties of these resonances is that they are roughly equally spaced in gate voltage. Since the separation of the resonances in gate voltage is proportional to U, the addition energy, our observation means that there are only

small variations in U as the number of electrons is changed. We have considered two different models in which disorder can trap electrons and find that neither can account for the equal spacing of the conductance resonances. One of the models is unable to account for the number of resonances observed, while the other is unable to account for the equal spacing of the resonances.

We propose that the resonances in single barriers occur because the disorder results in "electron puddles". These puddles, we suggest, were the consequence of the breakup of the delocalized metallic states in the barrier region as the density of electrons is decreased. Thus we believe that the complex behavior observed in our experiments reflects the nature of the electron puddles that have formed in the barrier. Because of the observation of similar equally spaced resonances in single barrier devices fabricated in other material systems we conclude that these electron puddles are not specific to the type of disorder found in the Si/SiO_2 material system but are more general.

To conclude, we have used tunneling spectroscopy to measure the electronic states of a small region of disordered material in which we can tune the electron density. Our experiments elucidate the transport properties of the electronic states in the tail of the band, an issue which is of growing technological interest (see section 5.1). Furthermore, our findings strongly suggest that there is a range of density in which the states in this region are "electron puddles". Despite their great physical importance, the nature of the electronic states near the metal-insulator transition are not understood [4, 20]. This study has made the contribution of suggesting and providing experimental evidence that these states consist of electron puddles.

Appendix A

Process Details

1. Start with p-type <100> prime grade wafers
   - either 25 – 45 Ω cm or 5 – 8 Ω cm
2. Clean Wafers
3. Grow 2200 Å field oxide
   - Wet oxidation, (1000 °C, 30 – 32 minute wet oxidation, 2 minute anneal).
4. Define alignment marks
   - mask level *EBEAMMARKS* designed at Lincoln Labs for ebeam/I-line cross alignment. Use thick resist (1.8 μ, SPR-518A) and fusion baking to withstand long silicon etch. Tortured resist must be stripped carefully.
   - local and global marks for I-line stepper done by dry etch through field oxide (2200 Å) and 1.25 μ etch into silicon substrate.
   - local and global marks for ebeam. These marks use same dry etch as stepper alignment marks and have field oxide etched away in window surrounding marks. Contrast mechanism is sharp step in silicon substrate. Field oxide removed to eliminate charging (see below).
5. Open windows in the field oxide
   - Expose maks level (*FOX*), thin resist (1.1 μ of SPR-511A). Window opened for active device region

- window opened around ebeam alignment marks (using Lincoln mask *E-BEAMMARKS*) so that ebeam can align to trench etch without charging problems. Exposure of both masks (*FOX* and *EBEAMMARKS* done in same exposure step).
- wet etch to surface of substrate for sloped sidewalls (BOE-930).

6. Grow sacrificial oxide

   - The amorphous sacrificial oxide reduces ion channelling and allows for contamination from ion implantation to be easily removed.
   - 365 Å oxide, 1000 °C dry oxidation for 37 minutes, with 10 minute anneal.

7. Ion implantation of for ohmic contacts

   - expose mask level *NIMP* using thick resist fusion baked. Strip resist carefully because it has been very heavily implanted (gasonics dry strip, piranha, SC1) to make sure no edges of resist remain.
   - Implant P ions (dose $4 \times 10^{15}\,\mathrm{cm}^{-2}$ at 90 KeV) giving metalic doping at depth of $.35\,\mu$ at low temperatures. To aviod carrier freezeout and have metalic doping at low temperatures requires doping density $> 3 \times 10^{19}\,\mathrm{cm}^{-3}$.

8. Etch sacrificial oxide.

   - Wet etch (100:1 HF : H_2O for slow etch)

9. Grow gate oxide

   - This is critical step because oxide quality can greatly affect device characteristics. There should be a minimum of delay between this step and deposition of CVD oxide.
   - Three different thickness of SiO_2 were grown, 365 Å, 200 Å, and 100 Å. Each was dry oxide grown at 975 °C. Times were not recorded.

10. Write lower gate pattern

    - Ebeam pattern written in 500 Å of PMMA.
    - To obtain 500Å we used 950 K molecular weight PMMA in 1% solution spun on at 2000 RPM for 40 seconds and baked at 180 °C for 30 minutes.

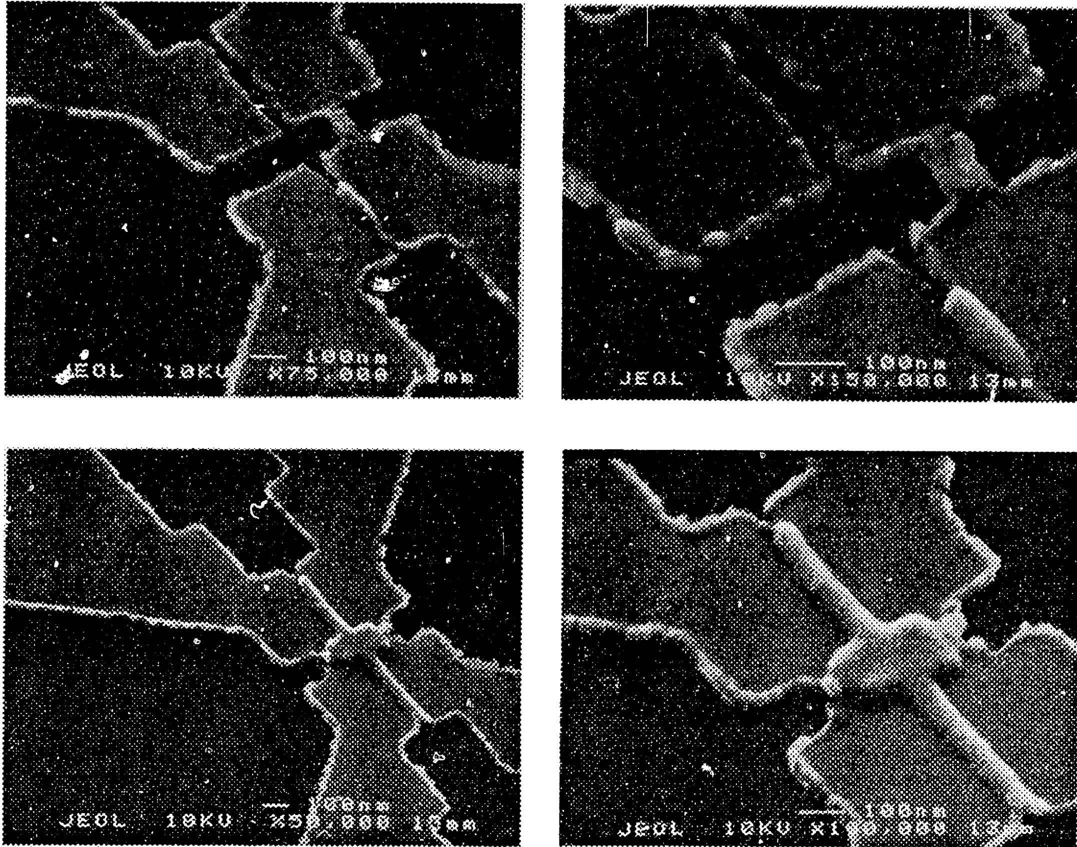

Figure A-1: Scanning electron micrographs of a metal pattern that failed to liftoff correctly. This was probably due to a poor PMMA profile because of an incorrect exposure or because the electron beam was not correctly adjusted.

- Variety of gate patterns written at various exposure doses. Gate patterns were chosen to give many possible device realizations (for details of gate patterns see file explaining lower gate pattern). Exposure doses ranged from 220 – 300 $\mu\,\mathrm{C\,cm^{-2}}$. A broad range of gate patterns and exposure doses were used to ensure that some fraction of the devices yielded working devices. Some examples of failed ebeam patterning are given in figure A-1.
- For process tests there is also a optical mask that could be substituted for the ebeam lithography (mask *REFR*). This mask has a variety of test structures patterned in the lower gate metal. Thin resist was used and liftoff was performed in with acetone as with PMMA coated wafers. The resist was not hardbaked to aid in liftoff.

11. Deposit and lift off Cr.

- Cr film thickness ranged from 150 – 200 Å. Because the PMMA was 500 Å

thick, Cr films thicker than 200 Å generally did not lift off well.

- Liftoff of ebeam samples was performed in acetone (20 minutes) with ultrasound with wafer facing down. This was followed by a 10 minute methanol rinse, and a DI cascade rinse. The acetone was replaced after every liftoff for fear the Cr particles in the acetone might stick to the wafer and contaminate its surface. For this same reason liftoff was performed on only 1 – 2 wafers at a time.
- Clean wafers in standard photoresist stripper and reintegrate into main silicon process.

12. Pattern and Deposit second Cr layer

    - Initial trials found that Cr lines of $5\,\mu$ width failed to be continuous over the feild oxide after rapid thermal anneal (RTA) at 1000 °C. Thinking that this would be remedied by a thicker layer of Cr taking the step over the field oxide, I added a second Cr layer. After various tests we found that even with this layer the lower gate is not continuous over a field oxide step after a 1000 °C RTA. Whether this layer is required is therefore in doubt.
    - Coat with thin resist (no hardbake). Expose mask layer BANDA and develop.
    - Some samples were ashed before having the second Cr layer deposited. This was done because in some tests the first and second Cr layer did not stick to each other well. In particular the second layer would easily come off when probed in a probe station. It is believed that this was due to a layer of organic contamination between the two Cr layers. The ash was performed to remove this organic layer. The ash was chosen to be very mild and was performed for .5 – 1 minute at 125 W in 7.5% O_2, 92.5% He.
    - Deposit 500 Å of Cr onto wafers and liftoff resist. Liftoff procedure for thin resist was the same as for the PMMA (see above).
    - Probe Cr lines to ensure they are continuous across field oxide step.

13. Deposit Low Temperature CVD oxide

    - Deposition using a low temperature (approximately 420 °C) SiH_4 process. Deposited thickness was 800 – 850 Å.

14. Rapid Thermal Anneal (RTA)

- This step was included in process based on experience of John Scott-Thomas. He found that the mobility of devices fabricated with a simlar process to mine had enhanced mobilities if annealed at high temperature [26, p. 45]. Given this experience we wanted to anneal at high temperature and chose to do so in an RTA.
- RTA took place at different temperatures and times for different samples. Successful settings include 900 °C for 30 seconds, 850 °C for 60 seconds, 850 °C for 120 seconds, 675 °C for 120 seconds. The wafers were ramped to final temperature at 50 °C/sec and all the anneals were performed in dry N_2.
- RTA performed at 1000 °C resulted in the of Cr lower metal gates not being electrically continuous across a field oxide step. Since the actual devices have contacts to the lower gates on the field oxide and the lower gates must take the step down the the gate oxide this is a critical problem. Adding the second Cr layer (see above) did not help this problem. The only solution was to anneal at a lower temperature. RTA preformed at 900 °C had continuous metal, aneals performed at 950 °C had some continuous metal wires, while anneals performed at 1000 °C where universally discontinuous. During RTAing visible grains to grew in the Cr gates. The higher the anneal temperature the more pronounced the the grain growth in the Cr. Whether the grain growth is realted to the discontinuity of the Cr wires is not known.
- Backside of wafer had to have oxide stripped. The RTA uses a pyrometer measuring the backside of the wafer to monitor the temperature of the wafer. Since SiO_2 has a different emisivity than Si the pyrometer requires the backside have no oxide.
- This step also serves to densify the CVD oxide as well as to diffuse and activating the implant.
- Rapid Thermal Anneal for 30 seconds at 1000 °C.

15. Etch contact holes through oxide

    - expose mask level *HOL* using thin resist.
    - etch oxide for contact holes to both the lower metal gate (Cr), and to the source/drain implants. We considered making this two different etches

(one to Cr and the other to source/drain) but this saves photo steps and is easier. Since Cr layer is very tough and does not etch in HF based solution, there is no problem exposing it to the etch for extended periods.

- Use monitor with oxide stack to get correct etch time. This monitor should have gate oxide (the thickest combination used in the lot) and CVD oxide on top. In addition the monitor should be undergo RTA at the highest temperatures used on any of the device wafers. Using monitor with thickest gate oxide and highest RTA temperature will ensure that the monitor requires the longest etch time. Thus it will give an upper bound on etch times. Overetch device wafers by 15% – 20%. Neither Cr nor source/drain regions have any problem with overetching.
- Use Silox Vapor Etch III for the etchant. I do not remember the advantage of this etchant, but it was chosen specifically for this task. Perform etch in dark by covering bath with opaque material (Al foil) or turning off lights, or both. When exposed to lights the source/drain regions turn interesting colors. Presumeably this is due to a photovoltage that is developed between p-substrate and n^+ regions when exposed to light. The photovoltage then drives some weird chemestry in the etch solution. The coloreed regions seemed to work as good ohmics, but better to avoid the whole problem.
- Do not strip photoresist with dry strip. I had a big problem with using gasonics (downstream plasma etcher). The reactive O_2 oxidized the Cr and made it insulating. Use a wet photoresist strip instead.
- After etching is a perfect time to probe wafers to ensure that everything is still working. I checked continutity of Cr lines, Cr lines taking step over field oxide, and source/drain to substrate diode. This was also done to ensure that all the contact windows were open.

16. Deposit and pattern Al

- Al served both as the upper metal gate, the contact to the lower metal gate, and the contact to the n^+ source/drain implants.
- A 120 second Ar ion sputter was performed before Al deposition to ensure that the Al contacted the active regions and not a region with native oxide.
- Deposit 2000 Å of Al by sputtering. Evaporation c Al contaminated devices with very high levels of Na^+, and sputtering seemed the better alternative despite potential damage to the wafer by energetic ions.

- expose mask level *METL* using thin resist. This exposure is more sensitive because the mask is clear field and is more suseptible to dust and dirt. Also exposure had to be adjusted because of high reflectivity of Al coating.
- Wet etch Al with standard wet etchant (Olin-1960). Use brightly colored colored wafer as etch monitor.

17. Deposit AlSi on the back of the wafer.
    - Done to provide backside contact to substrate.
    - Sputter to get good contact to the backside.
18. Sinter wafer in forming gas.
    - Done in forming gas at 425 °C for 20 minutes.
    - This step reduces oxide trap density and helps extablish good contact to the source/drain regions.

Appendix B

Gate Geometries

This appendix will help the reader understand the geometry of the gate patterns used in this study. Throughout this document each time we have presented experimental data we have included details that specify the device that was measured at the end of the figure caption in which the data was presented. Here we clarify the exact meaning of the notation we have used to specify the devices.

Each of the single barrier devices has one of the following geometries: rectangle (figure B-1), isosceles triangle (figure B-2), or right triangle (figure B-3). The different dimensions are shown in each of the figures, and a brief explanation is given in the figure caption.

In figure B-4 we show a the mask used to pattern a single die of devices. The caption explains the naming convention used to label the different device locations within each die.

More notes have been compiled and stored on the computer in the Kastner lab. Any researcher who hopes to use the devices we have fabricated is advised to read the various files included in the directory `(kastner):/data/david/thesis/notes/`.

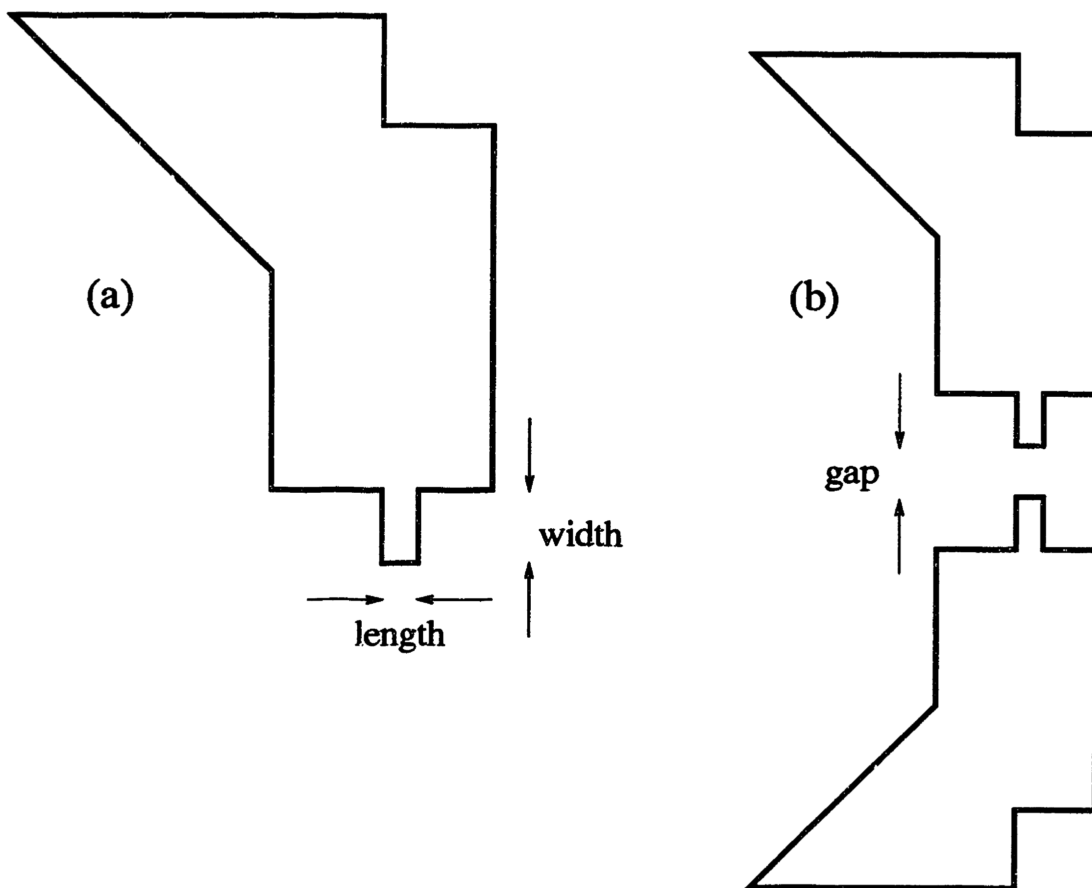

Figure B-1: **This figure shows the geometry for a single barrier with a rectangular shape. Figure (a) shows a the pattern of a single gate, while figure (b) shows the gap between two such gates placed across from each other. Thus, for example, in the device described in figure 6-3 the gate geometry was rectangular as shown in this figure with a length of 40 nm, a width of 80 nm, and a 90 nm gap.**

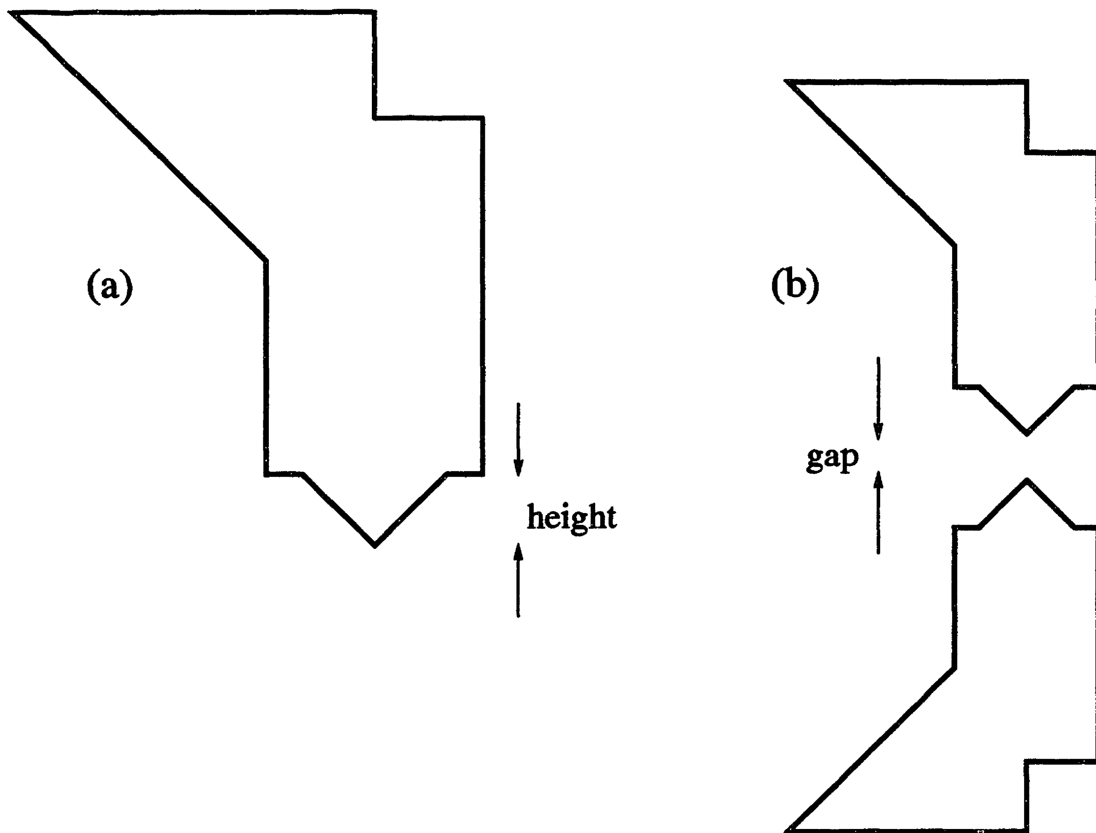

Figure B-2: **This figure shows the geometry for a single barrier with an isosceles triangular geometry. Figure (a) shows the pattern of a single gate, while figure (b) shows the gap between two such gates placed across from each other. The tip of the gates shown in this figure is an isosceles triangle with a height shown in the figure and a base of two times the height. Thus, for example, in the device described in figure figure 6-1 the gate has a height of 100 nm with a gap of 100 nm.**

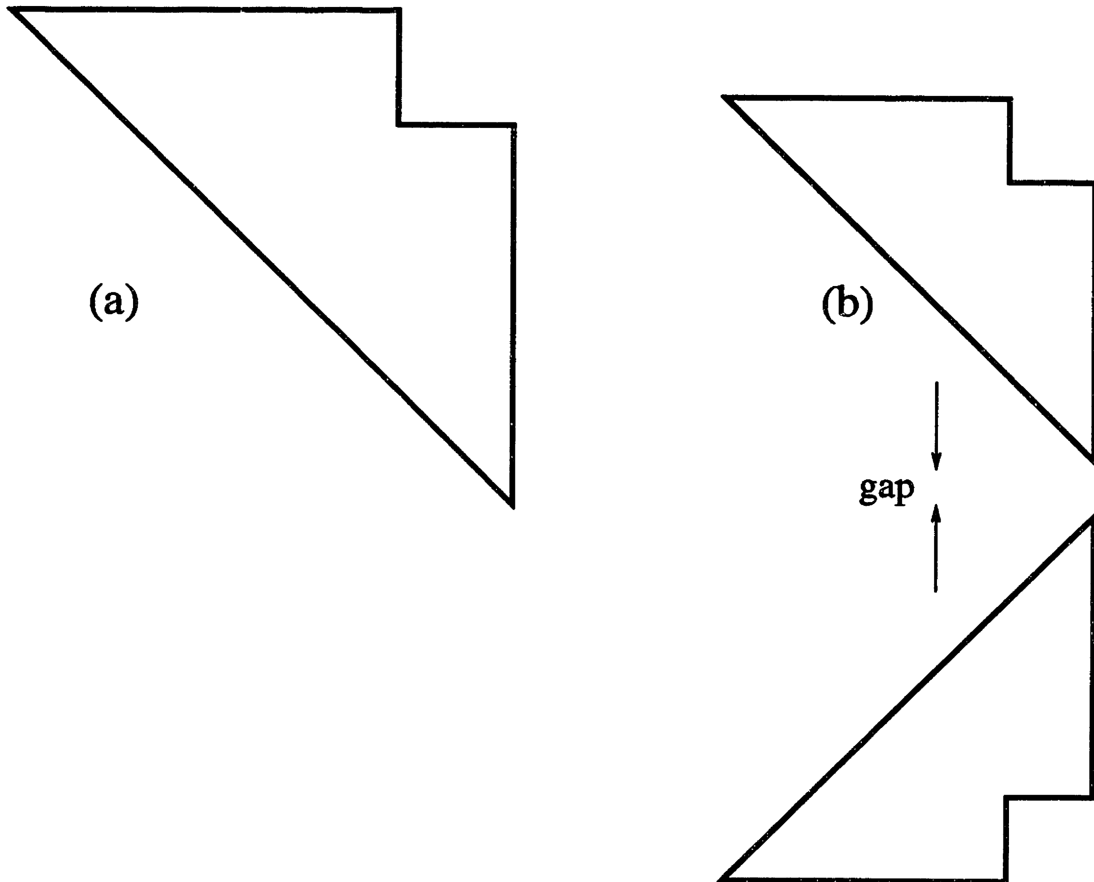

Figure B-3: This figure shows the geometry for a single barrier with an right triangular geometry. Figure (a) shows the pattern of a single gate, while figure (b) shows the gap between two such gates placed across from each other. The gate tip shown in this figure has a 45 degree angle. For example, in the device described in figure figure 6-6 the gap between the two gates is 50 nm. The fact that gates with this geometry show conductance resonance strongly suggests that the resonances are not caused by image charge trapping (see section 5.2) or by the trapping of charges in a one dimensional channel (see section 5.3.1).

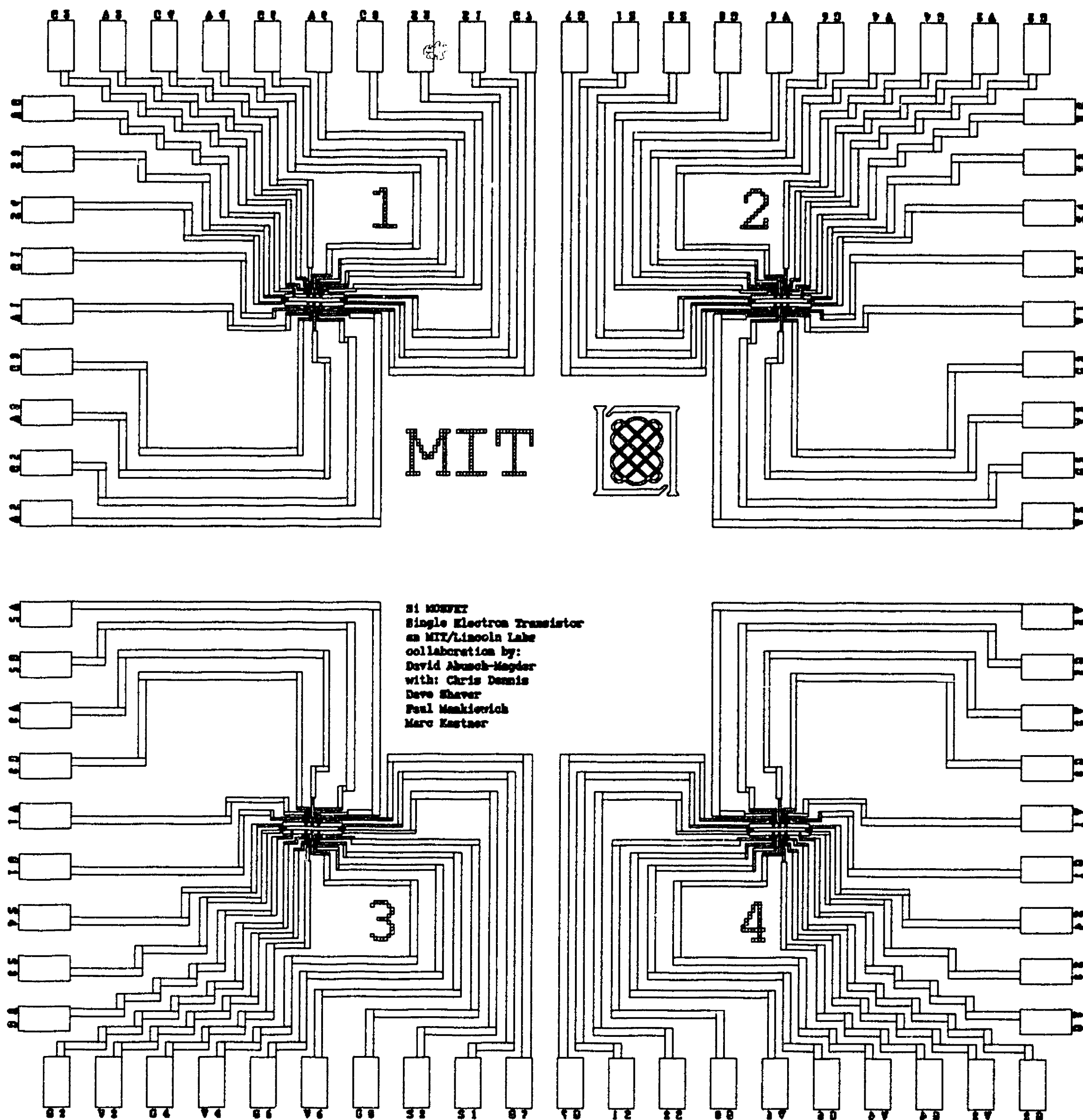

Figure B-4: This figure shows the wiring of a single die. There are eight die (labeled A – H) each of which has different lower gate patterns; just one of these is shown in this figure. Each die has four wiring groups (labeled 1 – 4 as seen in this figure) each of which contains two sets of devices (labeled 0 or 1). Each device in turn consists of two identical barriers which can form an artificial atom. Figure 6-1 is a measurement of device G20; thus it is measurement of the 0th device, in wiring group number 2, of the die labeled G.

Appendix C

Computation of Energy of an Image Charge

This appendix explains the calculations that were discussed in section 5.2. While we believe that this technique is straightforward we wish to make explicit the manner in which we carried out the calculations. Because the details of the calculations interrupt the flow of chapter 5 we have included them here. We refer to figures shown in section 5.2 and assume that the reader is familiar with the motivation of this calculation as discussed in that section.

To tackle the problem of computing the energy of a test charge in the presence of nearby conductors we have discretized the system shown in figure 5-3 and solved it numerically. Each conductor is considered to consist of discrete points separated by a distance Δ, labeled by index i, at position $\vec{r}_i$, with charge ρ_i, and potential V_i. We write the energy of the Coulomb interaction in this system as

$$E(\vec{r}_1, \vec{r}_2) = \frac{\rho_1 \rho_2}{\epsilon \sqrt{(\vec{r}_1 - \vec{r}_2)^2 + \delta^2}} \tag{C.1}$$

which includes a cutoff for close distances[1] and the dielectric constant, ϵ. We will use the boundary condition that the potential at infinity is zero. The inverse capacitance

[1] We have chosen a cutoff for close distance to be $\delta = .3\Delta$. This was chosen by testing various alternatives for the case of a charge above a plane. Since an exact form for the energy in this case is available we were able to compare the results of the simulation to the exact results. In this way we were able to chose a value for $\frac{\delta}{\Delta}$ that most closely reproduced the exact results.

between points i and j can be written as

$$B_{i,j} = \frac{1}{\epsilon\sqrt{(\vec{r}_i - \vec{r}_j)^2 + \delta^2}} \tag{C.2}$$

and the capacitance matrix is $\mathbf{C} = \mathbf{B}^{-1}$. As expected we may compute the charge on a point i due to the voltages of the other points by writing $\rho_i = \sum_j C_{i,j} V_j$.

When a test charge of total charge e is placed at $\vec{r}_t$ it changes the potential throughout space. At the location of the point i there is now a potential

$$\phi_i = \frac{e}{\epsilon\sqrt{(\vec{r}_i - \vec{r}_t)^2 + \delta^2}} \tag{C.3}$$

due to the test charge. However, for the conductors must remain at an equipotential charge and there charge be induced on them. We will consider all of the gates to be at $V = 0$, and can then compute this charge to be $\rho_i = -\sum_j C_{i,j}\phi_j$. The potential of the conductor is now

$$V_i = \phi_i + \sum_j B_{i,j}\rho_j = \phi_i - \sum_{j,k} B_{i,j}C_{j,k}\phi_k = \phi_i - \sum_k \delta_{i,k}\phi_k = \phi_i - \phi_i = 0 \tag{C.4}$$

as required. And finally the energy of the test charge in the presence of the conductors can be written as

$$E_t = -\frac{1}{2}\sum_i \phi_i\rho_i = -\frac{1}{2}\sum_{i,j}\phi_i C_{i,j}\phi_j \tag{C.5}$$

and computed. By a slight modification of our boundary conditions we may bias the different conductors to a non-zero voltage. In textbooks the same mathematical trick is used to extend the treatment of a charge near a ground plane to the case where the plane is at a finite voltage [63, Ch. 3]. In that case we fix the background voltage of the ith point which is in the conductor Ω (Ω will be either L1, L2, G1 or G2 of figure 5-3) $V_i^0 = V_\Omega$. Now we define the background charge as $\rho_i^0 = \sum_j C_{i,j}V_j^0$, having included the effect of the dielectric constant. We write the total energy of a test charge as:

$$E_t = \sum_i \phi_i(\rho_i^0 - \frac{1}{2}\rho_i) = \sum_{i,j}\phi_i C_{i,j}(\epsilon V_j^0 - \frac{1}{2}\phi_j) \quad . \tag{C.6}$$

In writing the energy of the test charge we have treated the background charge due to the voltage on the gates differently from the induced charge. As the test charge is brought from infinity the charge it induces is also brought in from infinity giving rise

to the factor of $\frac{1}{2}$. However the background charge on the gates is present as the test charge is moved in from infinity and therefore there is no factor of $\frac{1}{2}$.

In section 5.3.3 we consider a model in which me must compute the interaction energy of two electrons in the presence of conductors. We extend the calculations carried out above to the case of two electrons, one at $\vec{r}_1$ and the other at $\vec{r}_2$. Their direct interaction will be modified by the presence of the nearby conductors and the total energy will be:

$$E_{1,2} = \frac{e^2}{\epsilon\sqrt{(\vec{r}_1 - \vec{r}_2)^2}} - \frac{1}{2}\sum_i \phi_{1,i}\rho_{2,i} = \frac{e^2}{\epsilon\sqrt{(\vec{r}_1 - \vec{r}_2)^2}} - \frac{1}{2}\sum_{i,j} \phi_{1,i}C_{i,j}\phi_{2,j} \quad . \tag{C.7}$$

Notice that there are no source terms in this expression. Also notice that the since the capacitance matrix is symmetric ($C_{i,j} = C_{j,i}$) which ensures that that the energy of electron 1 interacting with electron 2 is the same as that of electron 2 interacting with electron 1.

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