Techniques for High Data Rate Modulation and Low Power Operation of Fractional-N Frequency Synthesizers

by

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Abstract

A digital compensation method is described that allows fractional-N frequency synthesizers to be directly modulated at high data rates while simultaneously achieving good noise performance. The technique allows digital phase/frequency modulation to be achieved at high data rates (> 1 Mbit/s) without mixers or D/A converters in the modulation path. The resulting transmitter design is primarily digital in nature and reduced to its fundamental components — a frequency synthesizer that accurately sets the output frequency, and a digital transmit filter that provides good spectral efficiency.

The synthesizer is implemented as a phase locked loop (PLL). To achieve good noise performance with a simple design, the PLL bandwidth is set to a low value relative to the data bandwidth. A digital compensation filter is then used to undo the attenuation of the PLL transfer function seen by the data. This filter adds little complexity to the transmitter architecture since it can be combined with the digital transmit filter; the overall filter is efficiently implemented by using a ROM to perform the required convolution with input data.

Measured results from a prototype indicate that good performance, low power operation, and high levels of integration are achieved with the approach. Specifically, a 1.8 GHz transmitter was built that supports data rates in excess of 2.5 Mbit/s using Gaussian Frequency Shift Keying (GFSK), the same modulation method used in the digital enhanced cordless telecommunications (DECT) standard. The phase noise of the unmodulated synthesizer was measured at -132 dBc/Hz at 5 MHz offset from the carrier frequency. (Simulations show that the modulated synthesizer achieves -132 dBc/Hz at 5 MHz offset at 1.25 Mbit/s data rate.)

The key circuits in the prototype were implemented on a custom, 0.6 um CMOS IC that consumes 27 mW. Included on the IC are an on-chip filter that requires no tuning or external components, a digital MASH Sigma-Delta converter that achieves low power operation through pipelining, and an asynchronous, 64 modulus divider (prescaler) that supports any divide value between 32 and 63.5 in half cycle increments of its input. An external divide-by-2 prescaler allows the divider to operate at half

the frequency of the voltage controlled oscillator (VCO), and changes the range of divide values to be all integers between 64 and 127.

Thesis Supervisors: Charles G. Sodini and Mitchell D. Trott
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He had no beauty or majesty to
attract us to him,
nothing in his appearance
that we should desire
him.
But he was pierced for our
transgressions,
he was crushed for our
iniquities;
the punishment that brought us
peace was upon him,
and by his wounds we are
healed.

Isaiah 53:2,5

Acknowledgments

The work presented in this thesis could not have happened without the help and support of many people. Mitch Trott introduced me to communication theory, and was supportive of my efforts to pursue the hardware side of that field. His suggestions were invaluable to my efforts of modeling the modulated PLL. Charlie Sodini introduced me to analog circuit design and device physics; he believed in me from the beginning of this effort, and has been a constant source of encouragement throughout its duration. Ted Tewksbury championed the project at Analog Devices, and saved the day many a time when implementation obstacles arose. Hae-Seung Lee taught me the art of analog circuit design; I am indebted to his instruction. Anantha Chandrakasan taught me low power circuit design techniques, and spent time with me as I investigated low power Σ-Δ topologies.

The people at Analog Devices played crucial roles in the design and implementation of the synthesizer. Jean-Marc Mourant and Geoff Dawe provided guidance on RF issues; their insight overcame many mysteries in that field. Peter Katzin was a sounding board for system issues, and helped me avoid pitfalls that only experience can warn you about. Zoran Zvonar listened to my ideas for modulation methods, and was a strong influence in my final choice of GFSK. Dan Fague provided insight of practical issues related to GFSK and the DECT standard. Paul Ferguson gave valuable advice related to the layout of my circuits, and analysis of their behavior. Bob Broughton helped me through the difficult task of making phase noise measurements of the system. Rob Weiner did an amazing job of bonding the die.

My colleagues at MIT provided a great deal of technical assistance, and also enriched my experience with their friendships. Jeff Gealow taught me many things about UNIX; he and Jen Lloyd provided the framework I used for writing the Cadence technology file needed for layout of the IC. Dan McMahill tested and built several circuits that allowed me to demonstrate the transmitter, and provided help with many practical matters. Don Hitko also provided practical insight, especially with respect to FrameMaker. Duke Xanthopoulos and Jim Goodman came to my aid when I encountered problems with software tools.

Marilyn Pierce helped me through many administrative matters in the EECS department; Monica Bell and Lisa Bella provided assistance in this area, as well. Pat Varley guided me through the paperwork involved in my many purchases, and did an

excellent job as our group's secretary.

Rob Gilmore from Qualcomm provided very useful information on phase noise measurement methods and PLL design issues. DARPA provided funding for this project under contract DAAL-01-95-K-3526.

I would like to thank my parents, Charles and Emily, and my sisters, Nikki and Missy, for their love, support, and encouragement through these many years of graduate school. I thank God for bringing me through this experience; to Him be the glory.

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Chapter 1

Introduction

The use of wireless products has been rapidly increasing the last few years, and there has been world wide development of new systems to meet the needs of this growing market. Characteristics such as low power operation, small size, and low cost have become the dominant design criteria by which these systems are judged. As a result, new circuit techniques have been sought to allow increased integration of radio transmitters and receivers, along with new radio architectures that take advantage of such techniques.

Motivated by the above goals, a low power and high performance narrowband transmitter for wireless communication that is highly integrated in silicon technology is presented in this thesis. As a driving application, the transmitter has been designed to meet the needs of a wireless video system depicted in Figure 1.1. Such a system requires digital modulation to be performed at data rates in excess of 1 Mbit/s. Rather than incrementally improving an existing design, a digital compensation technique is presented that allows the transmitter to be reduced to its fundamental components so that high integration and low power dissipation are achieved. New circuit techniques are employed to obtain high performance in the proposed design.

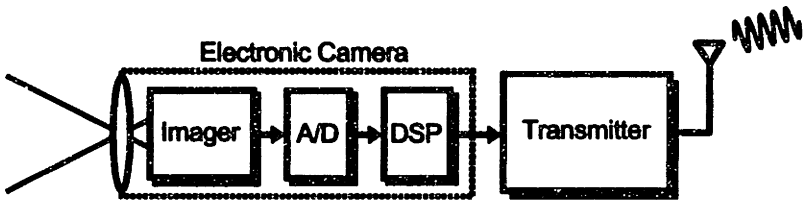


Figure 1.1: A driving application: wireless video.

The remainder of this chapter presents an overview of the thesis. We will begin by narrowing the focus of the project and presenting performance goals. Background information related to transmitter architectures is reviewed, and motivation for the proposed transmitter topology presented. The challenges of implementing such a de-

sign are then discussed, and an implementation that overcomes the primary obstacles is outlined. Finally, a detailed outline of the thesis is presented.

1.1 Area of Focus

Figure 1.2 displays a general block diagram of a narrowband transmitter capable of digital communication. The system consists of a modulator block that varies the

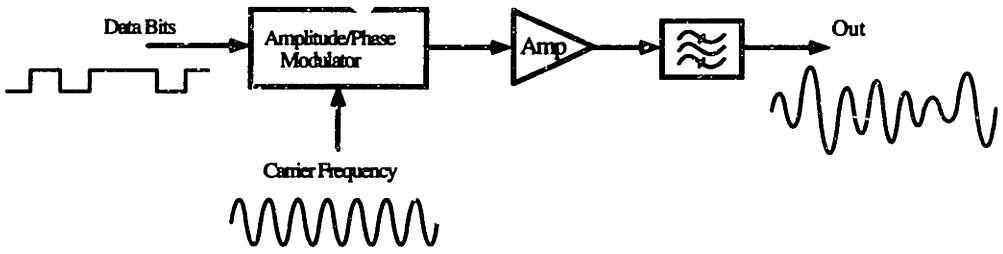


Figure 1.2: General block diagram of a narrowband transmitter.

amplitude, phase, or frequency of an output sine wave in response to an incoming bit sequence, a power amplifier, and a bandpass filter that is broad enough to pass all allowable communication channels. Assuming Figure 1.2 is representative of all narrowband transmitters, modifications to its architecture are primarily limited to the modulator block. Because of this fact, the focus of this thesis will be restricted to this block; the power amp and bandpass filter will be considered only in enough detail to address their impact on the modulator design.

The primary aspect of the modulator block that must be considered in relation to the power amp is the choice of modulation. Since power amps are most power efficient when producing a constant envelope signal [1–3], amplitude modulation should be avoided. Therefore, we will restrict our attention to phase or frequency modulation.

The impact of the bandpass filter on the modulator is limited primarily to noise issues. Since it must be wide enough to pass all channels, the filter does little to attenuate noise produced by the modulator just outside of the desired channel bandwidth. Therefore, the modulator must meet fairly stringent noise requirements, as will be specified below.

1.2 Modulator Architectures

Radio transmitters revolve around a common goal — a low frequency modulation signal must be translated to a desired RF band. Since the advent of the superheterodyne design by Armstrong (which dates back to 1918 [4]), the majority of high performance, narrowband transmitters have accomplished this frequency translation using mixers

and an intermediate frequency (IF) region of operation to perform highly-selective filtering [4]. While such an approach offers excellent radio performance (low spurious noise for transmitters), it carries with it a high cost of implementation in light of efforts to integrate radio architectures. Specifically, this approach is impeded by the inability to integrate the high-Q, low-noise, low-distortion bandpass filters required at IF frequencies (often on the order of 70 to 100 MHz for 900 MHz systems) [5].

For the above reasons, research into non-heterodyne architectures has taken place over the last few years in response to the growing demand for portable communication devices. Indeed, the use of direct carrier modulation has now become widespread in transmitters [5], which allows the channel shaping filters to be implemented at baseband and thus be integrated. A large wave of such designs implementing the global system for mobile communication (GSM) standard at 900 MHz in bipolar technology have appeared in the last five years, as described in [6–11]. Boasting of high integration, these chips achieved transmitter power consumptions as low as 162 mW [8], not including the power amplifier or baseband circuitry. In an effort to further reduce power through integration, Abidi et al. set out to create an all-CMOS transceiver that would implement all functions associated with their own frequency-hopped, 900 MHz, spread spectrum modulation scheme on one chip with the exception of the antennas and 900 MHz passive bandpass filters [12]. The power consumption of the transmitter portion of this chip is currently estimated at 300 mW, of which 60 mW can be attributed to the on-chip power amplifier. All told, the lowest power consumption of any high performance transmitter to date at 900 MHz (excluding the power amplifier) is probably around 200 mW, and is based on the design described by Stetzler et al. with an estimate of 30 mW for the baseband circuitry [13].

Motivated by the existing digital enhanced cordless telecommunications standard (DECT) [14], and the newly allocated PCS band in North America, a push for transceivers that operate at 1.8 GHz in silicon technology has recently taken place [15–19]. Of the new designs, the one that appears most promising in terms of power consumption involves the direct modulation of a VCO. An example of this approach was described by Heinen et al. in [15], which claimed a transmitter power consumption of 90 mW (excluding PLL circuitry, baseband circuitry, and power amplifier). Estimating the total power consumption of this approach at 150 mW (the power amplifier is excluded, the power consumption of the PLL circuitry is assumed to be 30 mW [20], and the baseband circuitry is assumed to be 30 mW [13]), we are led to the conclusion that this new design dissipates less power than its direct conversion counterparts operating at half the carrier frequency (i.e., 900 MHz).

What is the advantage of directly modulating the VCO? To answer this question, Figure 1.3 displays the basic operations that are used to perform frequency translation in the above designs. The prevalent method, shown in part (a), is to use a mixer to multiply the modulation signal by a periodic waveform produced by a voltage controlled oscillator (VCO) whose frequency is precisely set through the action of a frequency synthesizer. In the case of direct conversion, the modulation waveform is

an analog signal composed of I and Q channels which are directly translated from baseband to the desired RF frequency and then added together. The superheterodyne approach uses at least two stages of mixers to accomplish the frequency translation so that an intermediate filtering stage can be employed. As discussed above, the direct conversion method is preferred to achieve high integration. However, it should be noted that this method requires two mixers and D/A converters to accommodate the I and Q channels.

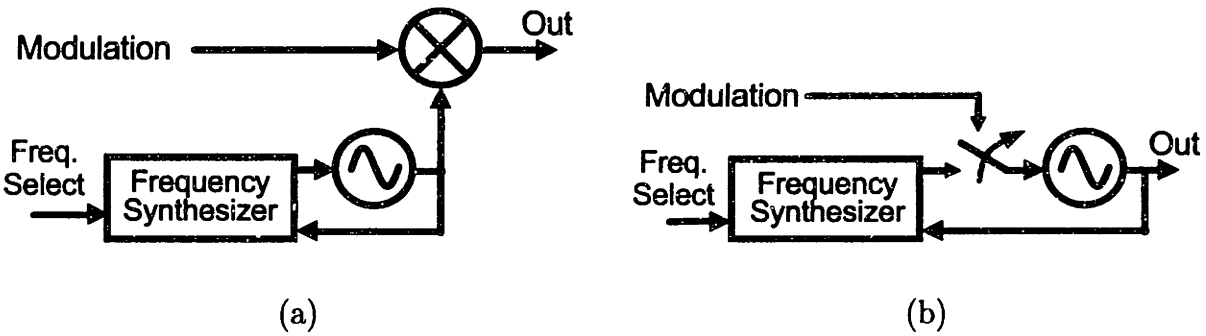


Figure 1.3: Two current approaches of modulation upconversion: (a) mixer based, (b) direct modulation of VCO.

The removal of all mixers can be accomplished by using the VCO to perform the required frequency translation. As illustrated in part (b) of the figure, the translation is accomplished by injecting the baseband, *analog* modulation signal into the input of the VCO after the frequency synthesizer has guided the VCO output to the desired carrier frequency. (Note that a multi-bit D/A converter is required to produce the analog modulation signal.) The advantage of Heinen's approach is now seen — the transmitter is reduced to a simpler structure since all mixers are removed. This technique restricts the modulated RF output to be phase or frequency modulated, but this is desirable from the standpoint of achieving high efficiency in the power amp as previously discussed.

Although simple in theory, there are many challenging implementation issues associated with direct modulation of the VCO. The primary source of difficulty is that the mapping from the VCO input to its output frequency is sensitive to process and temperature variations, thus requiring control by the frequency synthesizer to achieve an accurate frequency setting. However, if the frequency synthesizer is allowed to influence the VCO during modulation, it will interfere with the modulated data. This problem is solved by using an 'open loop' approach in which the frequency synthesizer is disconnected during transmission. However, in the absence of influence by the synthesizer, the frequency setting of the VCO becomes very sensitive to undesired perturbations. As a result, great steps must be taken to achieve high isolation of the VCO input from such perturbations, and all leakage currents must be minimized to avoid significant frequency drift during modulation. As Heinen explains in [21],

the isolation requirements for this method exclude the possibility of a one chip solution. Therefore, while the approach offers a significant advantage in terms of power dissipation, the goal of high integration is lost.

In contrast to the approach of directly modulating the VCO, Riley et al. introduced a technique in [22] to *indirectly* modulate the VCO by varying the divide value within a phase locked loop. In order to get fine resolution on the divide value, Riley made use of a fractional-N architecture with noise shaping discussed in [23–25]. The beauty of this technique lies in the fact that modulation of the VCO is performed in a closed loop manner through the influence of the frequency synthesizer. Therefore, the problem of frequency drift during modulation is eliminated, and the isolation requirements at the VCO input are greatly reduced at frequencies within the PLL bandwidth. The input to the synthesizer is digital in nature, which allows elimination of the multi-bit D/A converter that is required when directly modulating the VCO. In effect, Riley's approach amounts to directly modulating a frequency synthesizer.

1.3 Phase Locked Loop Frequency Synthesis

The first step toward implementing a modulated frequency synthesizer is to choose the synthesizer topology. The indirect method which involves the use of a phase locked loop (PLL) has the advantages of low power, feasibility of monolithic implementation, and phase coherence during frequency transitions [23, 26, 27]. There have been many approaches to the topological design of such synthesizers over the last 20 years represented in the literature [23–25, 27–38], with implementations in silicon at and above the 1 GHz range given in [39–45]. The point that is important to glean from these many approaches is that it is quite challenging to build a monolithic, low complexity synthesizer that simultaneously has low phase noise, fine frequency resolution, and fast dynamics.

Figure 1.4 displays the classical PLL frequency synthesizer topology consisting of a voltage controlled oscillator (VCO), a phase/frequency detector (PFD), a loop filter, a divider, and reference frequency source. Accurate control of the phase, and thus frequency, of the VCO is achieved through the feedback action of the loop. This feat is accomplished by using an error signal to control the VCO — specifically, the PFD produces a signal corresponding to the phase difference between the divided output and a reference frequency source, which is then 'smoothed' by the loop filter and fed into the VCO input. In equilibrium, the actions of the PLL lead to a condition known as 'lock' in which the frequency of the VCO, F_{out}, tracks that of the reference frequency, F_{ref}, such that

$$F_{out} = NF_{ref},$$

where N is the value of the divider. Assuming the reference frequency is held constant, the VCO frequency is changed by altering the divide value, N.

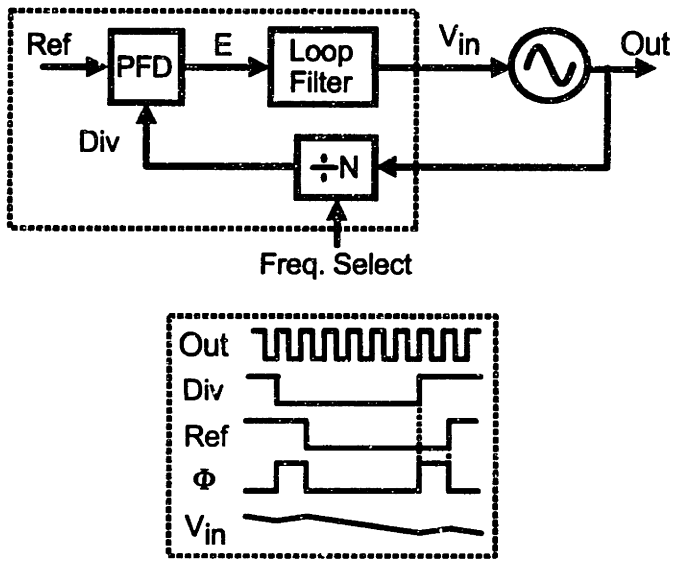


Figure 1.4: A phase locked loop frequency synthesizer.

Physical implementation of the divider within a PLL is easily accomplished using digital circuit techniques so long as N is constrained to be an integer. This restriction sets the resolution of the synthesizer to the value of the reference frequency, so that high frequency resolution requires the choice of a low reference frequency. In order to prevent large spurious noise levels, a low reference frequency must be accompanied by a small PLL bandwidth, which leads to slow dynamics [46]. Thus, there is a very restrictive tradeoff involved in achieving high bandwidth and high resolution in the classical PLL structure, which has prompted research into modifications of this architecture to ease this tradeoff.

The method of fractional-N synthesis was introduced in an effort to improve the resolution vs. bandwidth relationship of the classical PLL structure by removing the restriction that N be an integer [46]. The benefit of this approach is the uncoupling of the output frequency resolution from the choice of reference frequency — high resolution can be achieved even when a high reference frequency is chosen. Figure 1.5 illustrates this technique, and reveals that noninteger N values are produced by dithering between integer values. Specifically, the carry out bit of an accumulator circuit is used to control the choice of instantaneous divide value, which leads to a periodic dithering pattern. An illustration of typical signals associated with such an approach, as shown in Figure 1.6, reveals that the periodic dithering pattern leads to a periodic phase error pattern of lower frequency than that of the reference frequency. Suppression of the resulting spurious noise requires that the bandwidth of the PLL be placed well below the frequency of the periodic error pattern, which undermines the effort to obtain a high bandwidth.

As a means toward improving the performance of fractional-N synthesis, Fisher et

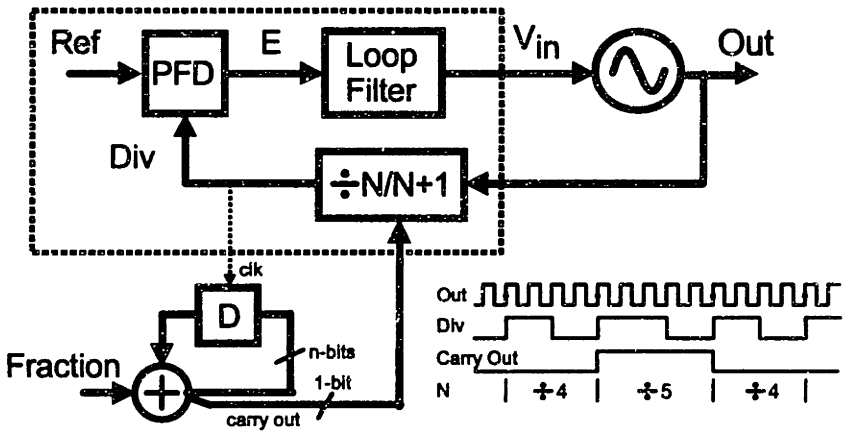


Figure 1.5: The fractional-N synthesizer architecture.

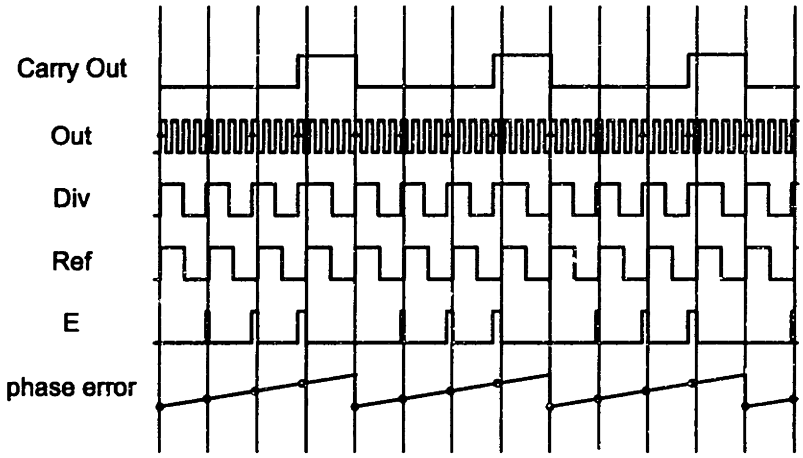


Figure 1.6: Signals associated with fractional-N synthesis with N=4.25.

al. proposed a technique now referred to as phase interpolation [29,30] to increase loop dynamics while maintaining low phase noise and fine frequency resolution. Fisher's approach made use of a D/A converter to cancel out spurious noise caused by the periodic dithering pattern described above. While high performance can be achieved with this approach, power dissipation is increased since a high speed D/A converter is required.

Rather than canceling out spurious noise with a D/A converter, Riley et al. in [23,27] and Miller et al. in [24,25] described a technique that prevents such noise from being produced by *altering* the dithering pattern in fractional-N synthesis. Here a connection was made between fractional-N synthesis and Σ-Δ D/A converters, the action of which is illustrated in Figure 1.7. The drawing depicts time and frequency domain views of a Σ-Δ D/A converter that achieves M-bit resolution by dithering a 1-bit D/A with a Σ-Δ modulator and smoothing the two-level sequence with an

analog lowpass filter to produce the desired analog output. High order Σ-Δ modulators are known to exhibit low spurious content when an input signal of sufficient activity is used [47]. In addition, an attractive aspect of Σ-Δ modulators is their property of shaping the resulting quantization noise into high frequencies. This last characteristic allows the analog lowpass filter to attenuate much of the quantization noise without affecting the input signal, whose energy is assumed to be confined to low frequencies. Application of this method to fractional-N synthesis is accomplished by simply replacing the digital accumulator with a Σ-Δ modulator.

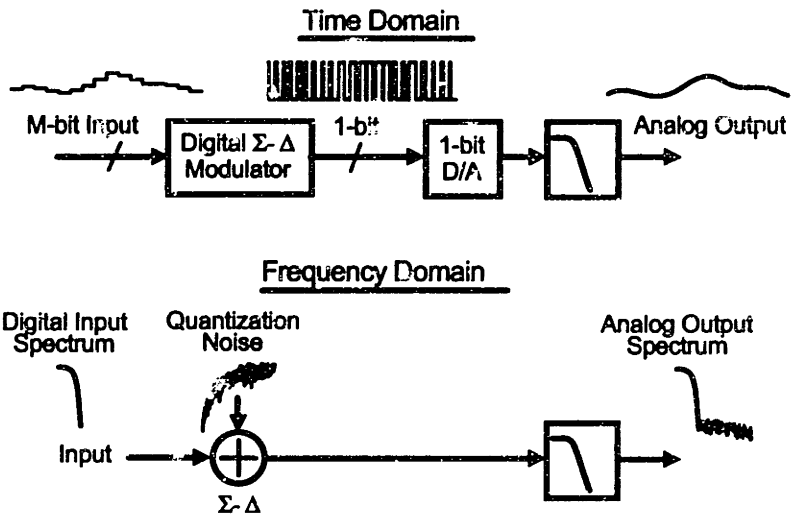


Figure 1.7: A 1-bit Σ-Δ D/A converter.

1.4 Direct Modulation of a Frequency Synthesizer

Given the PLL structure discussed above, we are now ready to attack the issue of modulation. Phase and/or frequency modulation of a frequency synthesizer is accomplished by varying its divide value according to input data. A simple method of performing this task is shown in Figure 1.8. Binary input data selects the divide ratio to be either N or $N+1$ depending on whether the input is 0 or 1, and N is chosen to achieve the desired carrier frequency. The output frequency settles to $F_{out} = NF_{ref}$, so that binary frequency shift keying (FSK) modulation is produced as N is varied. In the figure, the resulting output spectrum is illustrated under the assumption that $F_{ref} = 20$ MHz and that $N = 90$. The carrier frequency is seen to be 1.81 GHz, and the modulation frequency deviation equals F_{ref}.

Unfortunately, the FSK modulation method depicted in Figure 1.8 is not practical for most applications due to its inefficient use of spectrum. The spectral efficiency is greatly improved if a smooth transition is made during frequency transitions and the

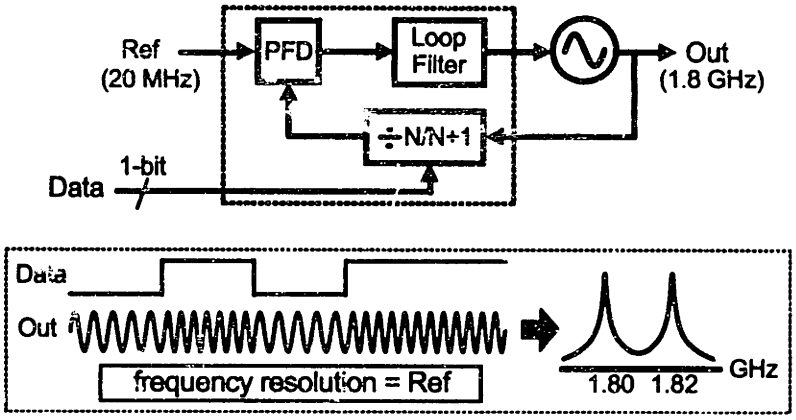


Figure 1.8: Direct modulation of a frequency synthesizer.

modulation deviation is optimized. Figure 1.9 illustrates a fractional-N modulator that achieves high spectral efficiency by using a digital transmit filter to obtain smooth transitions in the modulation data, and a digital Σ-Δ modulator to dither the divide value according to the resulting modulation sequence. This architecture was proposed by Riley et al. in [22]. The resulting spectrum is compact, and its overall shape is set by the digital filter assuming that the PLL dynamics have sufficient bandwidth. The digital transmit filter would typically be implemented as an FIR filter, which allows the convolution operation between it and the binary input data to be carried out with a lookup procedure that maps current and previous data samples, along with time information, to the filtered output waveform [22]. Physical implementation of the lookup procedure is accomplished with a ROM whose address lines are controlled by the input data and time information generated by a counter.

A direct analogy between the above fractional-N modulator and Σ-Δ D/A converter can be made by deriving a linearized model of the synthesizer dynamics. Figure 1.10 depicts such a model in the frequency domain. The digital transmit filter confines the modulation data to low frequencies, the Σ-Δ modulator adds quantization noise that is shaped to high frequencies, and the PLL acts as a lowpass filter that passes the input but attenuates the Σ-Δ quantization noise. The output of the linearized model corresponds to the instantaneous frequency of the synthesizer, which is considered analog in nature. A key constraint to consider is that the PLL bandwidth must be greater than the transmit filter bandwidth in order to avoid distortion of the modulation signal.

The modulator structure depicted in Figure 1.9 can well be considered the minimal topology necessary for frequency or phase modulation. Its architecture is composed of two core components — a frequency synthesizer and a transmit filter. The synthesizer is necessary in order to produce an RF output waveform that can be accurately set to desired frequencies. The transmit filter is necessary to produce a spectrally efficient modulation signal. Thus, the approach presented by Riley would appear to be the

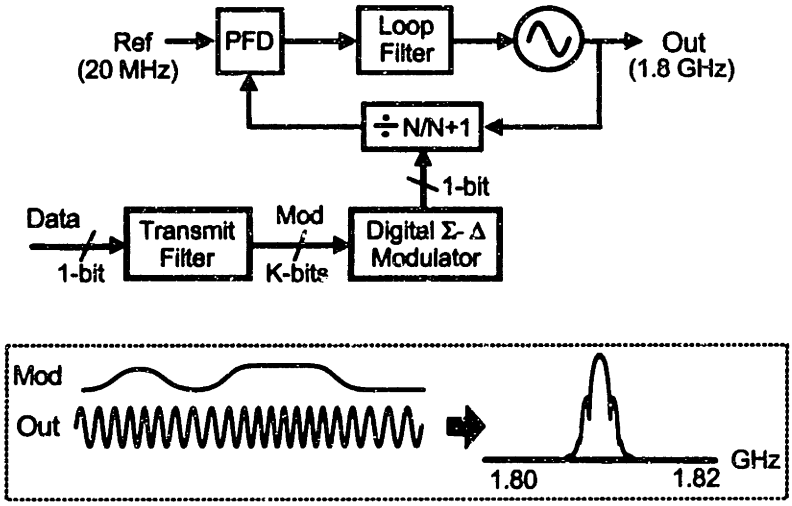


Figure 1.9: A spectrally efficient, fractional-N modulator.

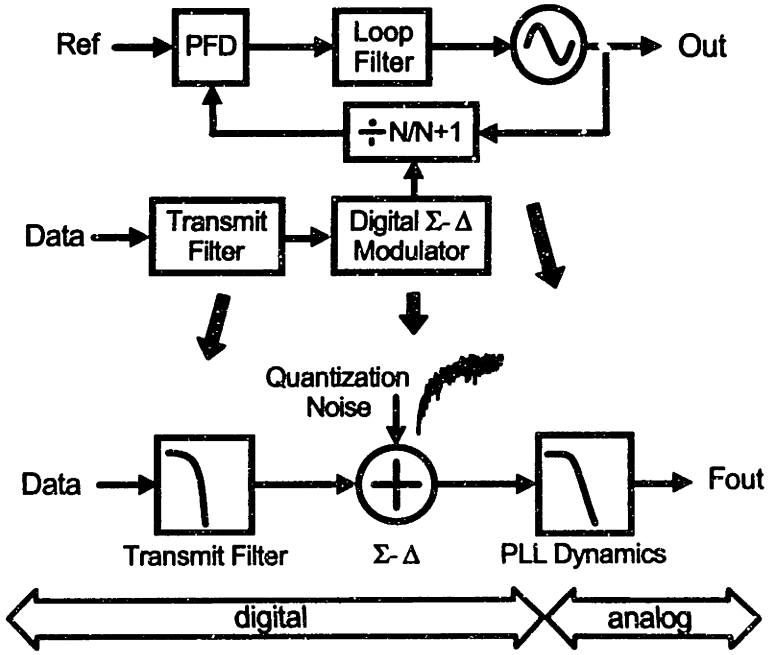


Figure 1.10: Linearized model of fractional-N modulator.

optimal topology to achieve low power operation, high integration, and high spectral efficiency.

1.5 The Challenge of Achieving High Data Rates and Low Noise

There is one significant drawback to Riley's modulator topology — the modulation bandwidth must be less than the PLL bandwidth. This constraint imposes a severe conflict between achieving high data rates and good noise performance. Figure 1.11 illustrates that high data rates require a wide PLL bandwidth, but low output noise requires a low PLL bandwidth in order to properly attenuate the Σ-Δ quantization noise.

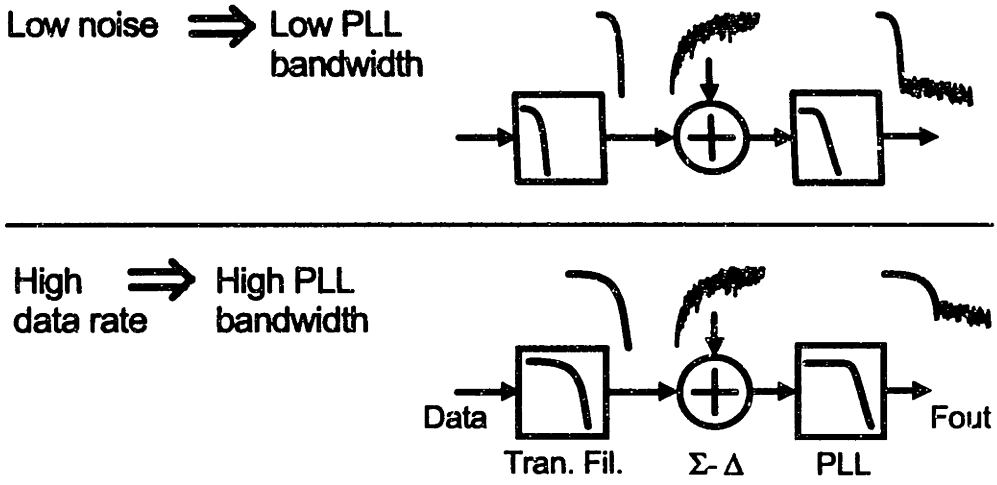


Figure 1.11: The conflict of high data rate and low noise performance.

How low must the PLL bandwidth be set to achieve the required noise performance? The answer to this question depends on three parameters:

- The required noise specification,
- The order of the Σ-Δ modulator and PLL transfer function,
- The sample rate of the Σ-Δ (i.e., the value of the F_{ref}).

By increasing the order of the Σ-Δ, the noise is further pushed to high frequencies, allowing a wider PLL bandwidth. However, the order of the PLL transfer function must also be increased to achieve acceptable attenuation of the noise at high frequencies. The setting of the sample rate of the Σ-Δ provides another handle for achieving the required noise performance — high sample rates distribute the quantization noise over a wide frequency region, therefore allowing a wider PLL bandwidth.

Figure 1.12 displays the required combination of PLL (Σ-Δ) order and Σ-Δ sample rate to achieve a variety of data rates where the output phase noise due to Σ-Δ

quantization noise is set to -136 dBc/Hz at 5 MHz offset from the carrier. (A Butterworth transfer function is assumed for the PLL, and the relation between PLL bandwidth, f_o, and data rate, $1/T_d$, is assumed to be $f_o T_d = 0.7$. An explanation for these settings is provided later in the thesis.) This noise specification is chosen to achieve an overall noise specification that is less than -131 dBc/Hz at 5 MHz offset after accounting for the effect of VCO noise.

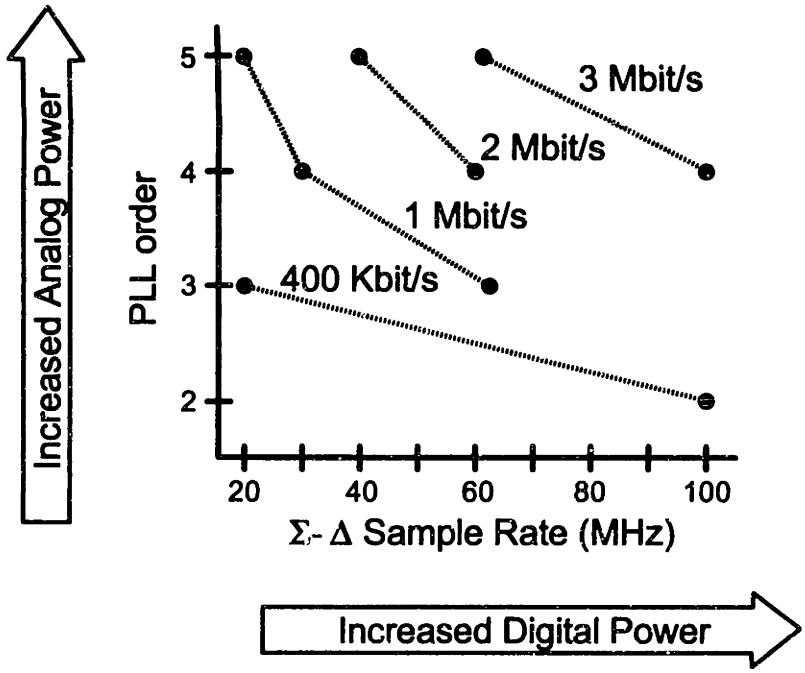


Figure 1.12: Achievable data rates vs. PLL order and Σ-Δ sample rate.

Figure 1.12 reveals that the achievement of high data rates requires high PLL orders and high Σ-Δ sample rates. An increase in PLL order leads to increased power and complexity in the analog section of the PLL in order to realize additional poles and/or zeros, and perform tuning [48] to insure that these poles/zeros are accurately set. Such tuning is particularly critical for PLL orders greater than 2 in order to assure stable PLL dynamics. An increase in Σ-Δ sample rate leads to increased power in the digital section of the modulator since it leads to an increased clock speed for the Σ-Δ and ROM circuitry. Thus, the figure reveals that an increase in data rate leads to increased power levels in the fractional-N modulator.

1.6 Proposed Method

The primary contribution of this thesis is a proposed compensation method that allows the data bandwidth to exceed the PLL bandwidth by over an order of magnitude

with little increase in the power dissipation or complexity of the fractional-N modulator. As illustrated in Figure 1.13, the increase in data rate is achieved by cascading a digital compensation filter, which is the inverse of the PLL transfer function, with the digital transmit filter. The resulting transfer function seen by the data is flat, which allows the data rate to exceed the PLL bandwidth. The compensation filter can be implemented by simply combining it with the transmit filter and altering the ROM storage values. Noise is not amplifed by using the compensation method since it alters the transmit filter rather than acting on an analog input signal.

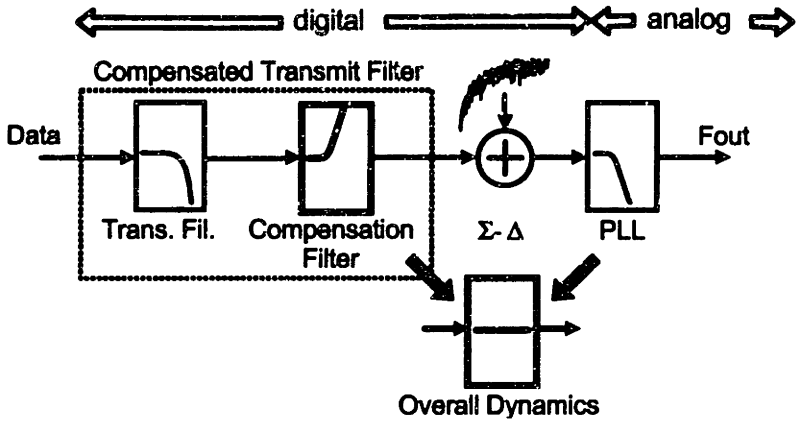


Figure 1.13: Proposed compensation method.

Table 1.1 displays the achievable data rates at different Σ-Δ sample rates using compensation; the noise specification was identical to that used to generate Figure 1.12, and the order was restricted to two for reasons discussed later in the thesis. Figure 1.14 compares the achievable data rate with compensation at a Σ-Δ sample rate of 20 MHz to the achievable data rates without compensation; we see that compensation allows high data rates to be achieved with relatively low complexity and power dissipation. The calculated data rates with compensation are based on the available dynamic range within the implemented PLL, a point that is touched upon below.

Σ-Δ sample rate	20 MHz	40 MHz	80 MHz
Max. data rate	3.4 Mbit/s	4.8 Mbit/s	4.9 Mbit/s

Table 1.1
Theoretically achievable data rates using compensation for second order PLL.

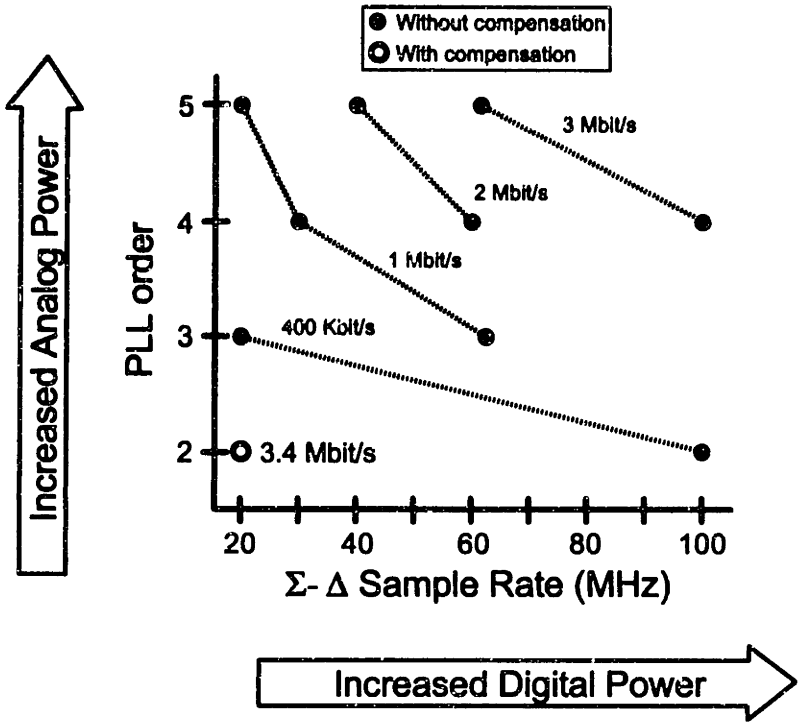


Figure 1.14: Comparison of achievable data rates with and without compensation vs. PLL order and Σ-Δ sample rate.

1.7 Issues

There are two issues that must be considered when implementing the proposed compensation method. The first is that, in practice, mismatch will occur between the compensation filter and PLL dynamics. While the compensation filter is digital and therefore fixed, the PLL dynamics are analog in nature and sensitive to process and temperature variations. Figure 1.15 illustrates that a parasitic pole/zero pair and high frequency gain error occurs when the bandwidth of the PLL is too high. A similar situation occurs when the gain is too low. As will be described later, the parasitic pole/zero pair causes intersymbol interference and modulation deviation error. Thus, it is important to strive for a PLL implementation that has accurate PLL dynamics despite process and temperature changes.

The second issue is that the achievement of high data rates requires a large dynamic range in the modulation path. As shown in Figure 1.16, the compensated transmit filter amplifies high frequency components in the input data stream. The resulting modulation signal experiences an increased signal swing that must be accommodated in the modulation path. To achieve data rates in excess of 1 Mbit/s, the 1-bit pathway into the divider is not sufficient. An increase in this pathway requires the use of multiple-bit output Σ-Δ and a multi-modulus divider that supports a wide

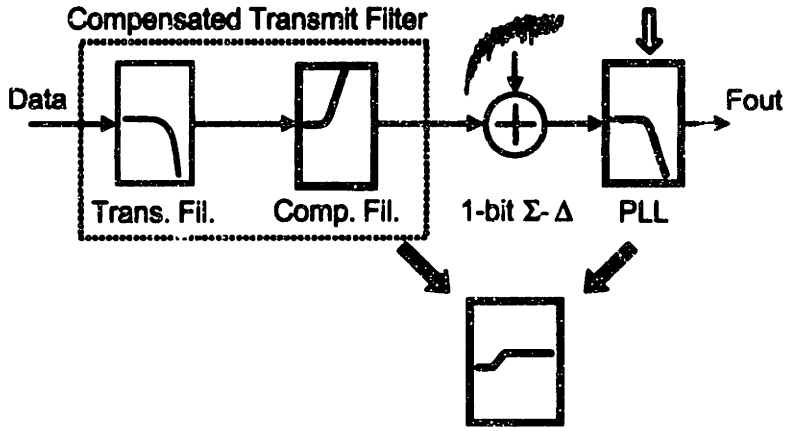


Figure 1.15: The effect of mismatch.

range of divide values.

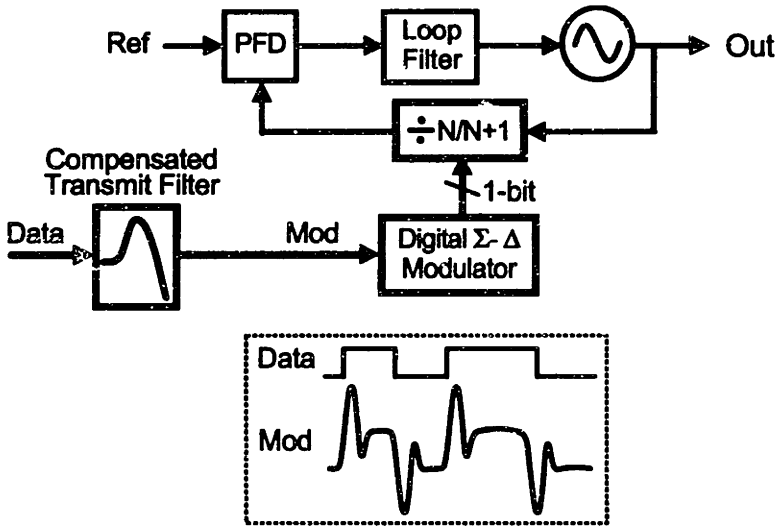


Figure 1.16: High data rate costs dynamic range.

1.8 Implementation Highlights

To show proof of concept of the proposed compensation method, the system depicted in Figure 1.17 was built using a custom, CMOS fractional-N synthesizer that contains several key circuits. Included are an on-chip, continuous-time filter that requires no tuning or external components, a digital MASH Σ-Δ modulator with 6 output bits that achieves low power operation through pipelining, and a 64 modulus divider that

supports any divide value between 32 and 63.5 in half cycle increments. The inclusion of the external divide-by-2 prescaler allows the CMOS divider input to operate at half the VCO frequency, and changes the range of divide values to all integers between 64 and 127.

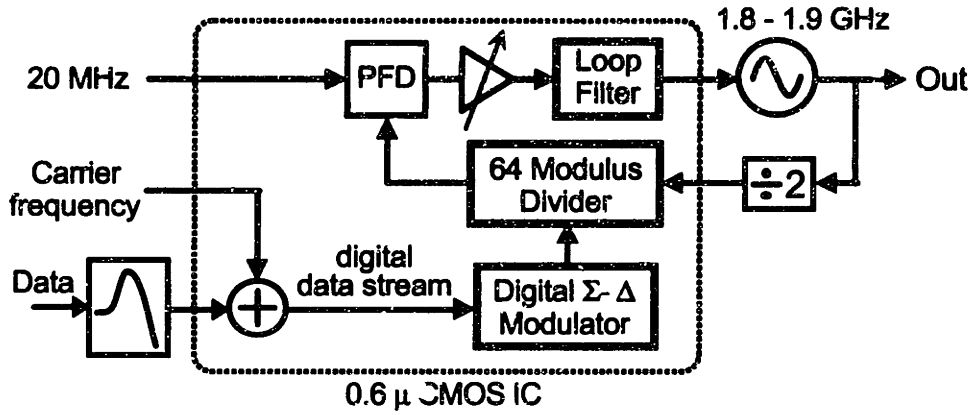


Figure 1.17: Overall System.

Table 1.2 lists the specifications of the prototype frequency synthesizer IC. The power of the proposed system is roughly half that of a DECT system described by Heinen in [15], which is believed to be representative of the lowest power transmitter architecture available at the present time. It should be noted that the spurious noise was measured without an output bandpass filter on the transmitter. The inclusion of this filter should lower the spurious response to less than -80 dBc.

Power consumption	27 mW
Maximum Data Rate	2.85 Mbit/s
Carrier Frequency	1.81 GHz to 1.89 GHz
Modulation	GFSK
Spurious Noise	< -60 dBc
Phase Noise	< -131 dBc/Hz at 5 MHz offset

Table 1.2
Modulator specifications.

The modulation method chosen for the prototype is Gaussian Frequency Shift Keying (GFSK). This method is similar to Gaussian Minimum Shift Keying (GMSK) [49], the difference being that GFSK allows a tolerance on the modulation index, h. (By definition, h is the ratio of the peak-to-peak frequency deviation of the transmitter output to its data rate.) This tolerance is necessary when using the compensation method since mismatch between the compensation filter and PLL dynamics changes

the frequency deviation of the transmitter output. (An explanation of this phenomenon is provided in Chapter 6.) The value of h is 0.5 in the case of GMSK, which causes the phase of the transmitter output to increment or decrement by $\pi/2$ radians during each data symbol period. In the case of GFSK as used in DECT, $h = 0.5 \pm 0.05$.

Although the proposed compensation method is applicable to modulation methods other than GFSK, we will restrict our analysis to this case since it provides a benchmark for our results. Specifically, we will strive to meet the performance standards of DECT; our primary goal will be the achievement of a data rate in excess of 1 Mbit/s with a noise spectral density that is less than -131 dBc/Hz at 5 MHz offset.

In the implementation, the 64 modulus divider and 6 output bit Σ-Δ modulator provide a dynamic range for the compensated modulation data that is wide enough to support data rates in excess of 2.5 Mbit/s. The on-chip loop filter allows an accurate PLL transfer function to be achieved by tuning just one PLL parameter — the open loop gain. A brief overview of each of these components will now be presented.

1.8.1 Divider

To achieve a low power design, it is desirable to use an asynchronous divider structure to minimize the amount of circuitry operating at high frequencies. As such, a multi-modulus divider structure was designed that consists of cascaded divide-by-2/3 sections [50]; this architecture is an extension of the common dual-modulus topology [45, 51–53]. Shown in Figure 1.18 for an 8-modulus example, this divider structure allows a wide range of divide values to be achieved by allowing a variable number of input cycles to be 'swallowed' per output cycle. Each divide-by-2/3 stage normally divides its input by two in frequency, but will swallow an extra cycle per OUT period when its control input, D_i, is set to 1. As shown for the case where all control bits are set to 1, the number of IN cycles swallowed per OUT period is binary weighted according to the stage position. For instance, setting $D_0 = 1$ causes one cycle of IN to be swallowed, while setting $D_2 = 1$ causes 4 cycles of IN to be swallowed. Proper selection of $\{D_2 D_1 D_0\}$ allows any integer divide value between 8 and 15 to be achieved.

The 64 modulus divider that was developed for the prototype system uses a similar principle to that discussed above, but has a modified first stage to achieve high speed operation. Specifically, the implemented architecture consists of a high speed divide-by-4/5/6/7 state machine followed by a cascaded chain of divide-by-2/3 state machines as illustrated in Figure 1.19. The divide-by-4/5/6/7 stage accomplishes cycle swallowing by shifting between 4 phases of a divide-by-2 circuit. Each of the 4 phases is staggered by one IN cycle, which allows single cycle pulse swallowing resolution despite the fact that two cascaded divide-by-2 structures are used. This phase shifting approach, which is also advocated in [53], allows a minimal number of components to operate at high frequencies — the first two stages are simply divide-

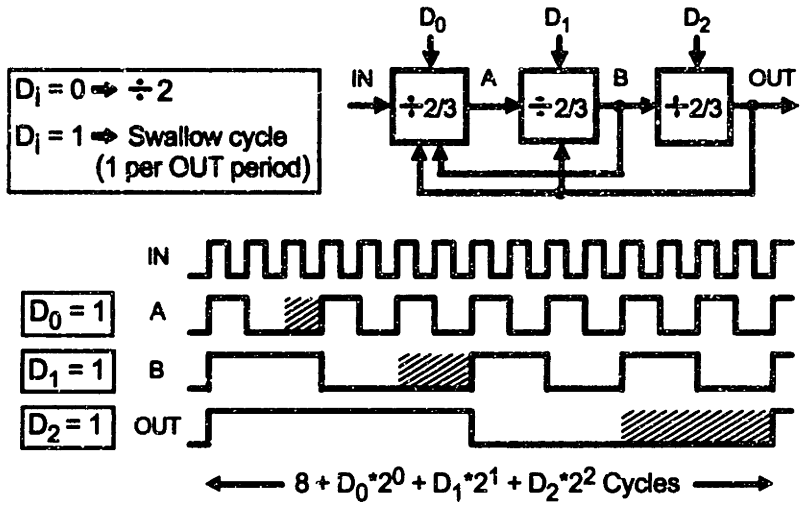


Figure 1.18: An asynchronous, 8-modulus divider topology.

by-2 circuits, not state machines. Also, the fact that control signals are not fed into the first divide-by-2 circuit allow it to be placed off-chip in the prototype.

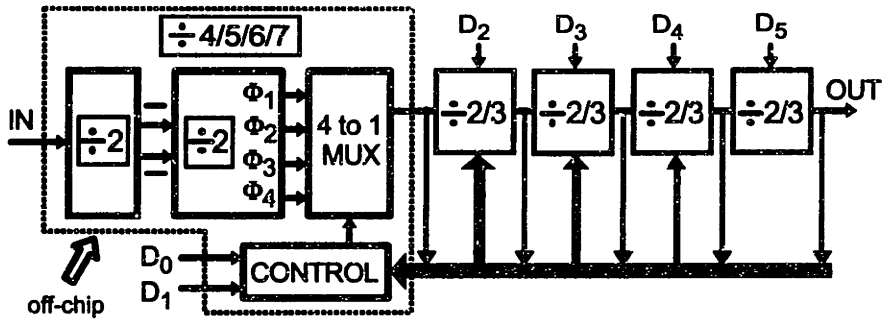


Figure 1.19: An asynchronous, 64 modulus divider implementation.

1.8.2 Loop Filter

The achievement of accurate PLL dynamics is accomplished in the prototype system with the variable gain loop filter topology depicted in Figure 1.20. Surrounding stages relevant to the loop filter description are included and will now be described. The PFD output is a square wave voltage waveform whose duty cycle varies according to the input modulation data. The shaded region corresponds to the approximate duty cycle span that 2.5 Mbit/s would take up in the prototype. A conversion of the PFD output from voltage to current is made by the charge pump, which yields two complementary current waveforms with modulated duty cycles. These current

waveforms are fed into the inputs of an opamp that integrates one current and adds to it a first order filtered version of the other current. The first order pole, w_p, is created using a switched capacitor technique, which reduces its sensitivity to thermal and process variations and removes need for tuning the time constant. An important characteristic of the loop filter is that it has a continuous-time output despite the fact that the discrete-time switched capacitor method is used to set its time constant.

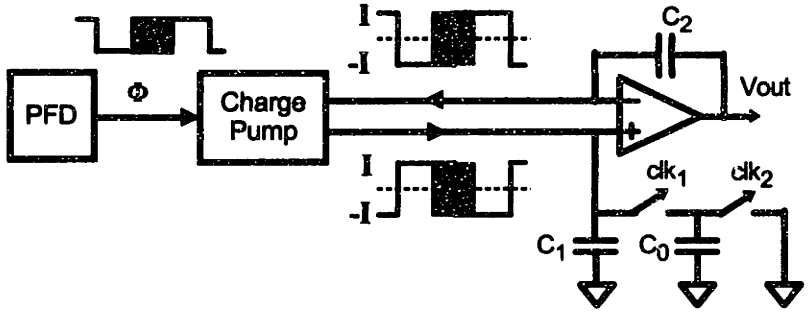


Figure 1.20: PFD, charge pump, and loop filter.

Since the loop filter achieves accurate time constants that are insensitive to process and temperature variations, the only parameter that needs to be tuned to obtain accurate PLL dynamics is its open loop gain. In the illustrated topology, gain control is achieved by varying the value of I produced by the charge pump. This leads to the need for a variable current charge pump, which is described later in the thesis.

1.8.3 Σ-Δ structure

A low power, digital Σ-Δ modulator was realized in the prototype by using a pipelining technique to allow reduction of its power supply voltage. The use of this technique relied on the fact that the Σ-Δ could be implemented as a MASH structure [47] since a multiple bit output is required. (A MASH structure of order n requires at least n output bits [47].)

Figure 1.21 illustrates the second order, MASH topology used in the prototype; it consists of cascaded first order sections that contain no surrounding feedback loops. This structure is pipelined by applying a well known technique that has been used for adders and accumulators [54, 55]. Figure 1.22 illustrates a 3-bit example; the key principle is that registers are inserted in the carry chain of the adder to reduce its critical path. To achieve time alignment between the input and the delayed carry information, registers are also included to skew the input bits. The adder output is realigned in time by performing an "align shift" of its bits as shown. The same approach can be applied to digital accumulators since there is no feedback from higher to lower bits. Since its basic building blocks are adders and accumulators, this technique allows a MASH Σ-Δ modulator of *any order* to be pipelined.

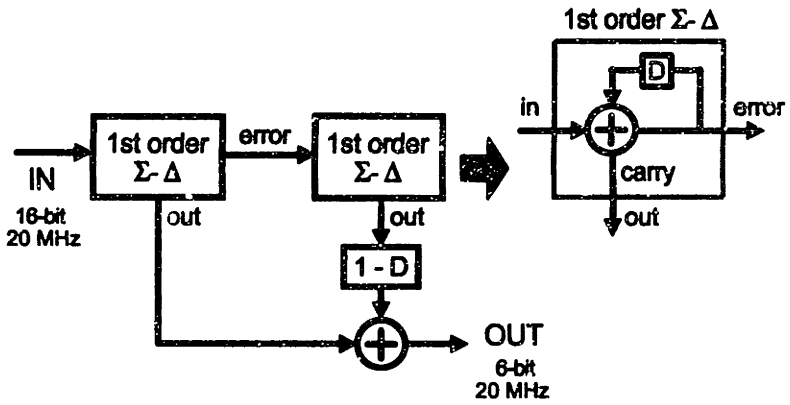


Figure 1.21: A second order, digital MASH, Σ-Δ structure.

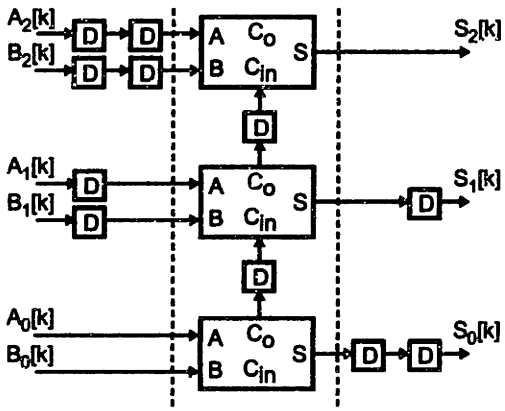


Figure 1.22: A pipelined adder topology.

1.9 Contributions

The primary contribution offered by this thesis is the introduction, analysis, and verification of a digital compensation method that increases, by over an order of magnitude, the data rate that can be achieved when directly modulating a fractional-N synthesizer. This method is used in a prototype transmitter capable of achieving data rates in excess of 2.5 Mbit/s with a PLL bandwidth of 84 kHz and an overall architecture that is primarily digital in nature. Simplicity and power savings are achieved in its design by virtue of the fact that no mixers or D/A converters are required in the modulation path. Good performance is also achieved — measured results from the prototype indicate that it meets the performance specifications required for DECT.

The idea of using compensation to modulate a PLL frequency synthesizer at data rates beyond its bandwidth is not new; patents that advocate such an idea are found in [56–59]. However, the approaches presented in these patents are intimately tied to

modulation methods in which data enters as an *analog* signal to a node (or nodes) within the PLL. The compensation filters are implemented as analog circuits; this approach requires several component values to be accurately set, and leads to the amplification of noise in those frequency regions where the input signal is increased.

In contrast, the technique presented here achieves compensation by simply *modifying* the digital transmit filter of the transmitter, which is required to achieve good spectral efficiency. This method of implementation adds little power or complexity to the synthesizer design, and does not lead to amplification of noise. In contrast to the requirement that several components be accurately set, the presented method allows accurate matching between the compensation and PLL transfer functions to be achieved by proper adjustment of *one parameter*, the open loop gain of the PLL. The resulting transmitter architecture achieves a high level of integration, low power dissipation, and good performance.

1.10 Overview of Thesis

The remaining chapters in this thesis provide further analysis and implementation details pertaining to the proposed compensation method. They are organized into three different sections. The first section, Chapters 2-6, focuses on modeling and analysis related to the technique. The second section, Chapters 7-9, presents the circuit designs used in the prototype. The last section, Chapters 10-11, describe the overall design of the prototype and present simulated and measured results.

The first section begins with the presentation of a linearized model of the fractional-N synthesizer. This model allows the influence of the PLL dynamics on modulation and noise performance to be quantified (Chapters 2 and 3). The known technique of modulating the synthesizer within its bandwidth is then evaluated; it is shown that data rates in excess of 1 Mbit/s are difficult to achieve with this approach (Chapter 4). The proposed method is then introduced, and the achievable data rates with this approach are quantified (Chapter 5). The influence of mismatch is discussed, with particular focus on the effects of using type II feedback within the PLL (Chapter 6).

The description of the various circuit designs in the prototype focus on the multi-modulus divider, the digital data path, and the analog phase comparison path within the PLL. The divider chapter discusses the philosophy underlying its architecture, and then presents implementation details (Chapter 7). The Σ-Δ modulator is described with particular focus on the pipelining technique used to achieve its low power dissipation (Chapter 8). Finally, the PFD, charge pump, and loop filter designs are presented, which form the analog phase comparison path. Analysis of the resulting transfer function in this path is covered in detail (Chapter 9).

The last section of the thesis begins with a discussion of the design procedure used to set the PLL transfer function in the prototype. Analytically based calculations are made of the noise performance of the resulting system (Chapter 10). Finally,

simulated and measured results are presented (Chapter 11).

Chapter 2

Modeling

This chapter presents detailed models of the fractional-N synthesizer that will be used in later chapters to characterize the influence of its dynamics on noise and modulation performance. First, a linearized, frequency-domain model of the PLL is derived; the resulting block diagram differs from that used in classical PLL analysis [60] by its inclusion of a linearized divider model, which is necessary for modulation analysis of the compensated system. Parameterization of the PLL dynamics by a transfer function, $G(f)$, follows; this single function can be used to describe the relationship between all signals of interest in the PLL. A discussion of Σ-Δ modulation applied to frequency synthesis ensues. The chapter concludes by presenting a complete model of the synthesizer that includes the effects of the Σ-Δ modulator. The resulting structure is parameterized in terms of $G(f)$, and separated into noise and modulation sections.

2.1 PLL Basics

Figure 2.1 gives a block diagram of a PLL, along with a snapshot of the signals associated with various nodes in this system. A PLL achieves its functionality through the use of feedback. As shown in the figure, this action is accomplished by first dividing the output frequency of the VCO and then comparing its phase to the phase of the reference source in order to produce an error signal. The phase comparison operation is done through the use of a phase/frequency detector (PFD) which also acts as a frequency discriminator when the PLL is out of lock. Practical implementations of the PFD are nonideal, and lead to the introduction of high frequency components in the error signal. These components must be attenuated before feeding the error signal into the VCO input; this task is accomplished by the loop filter. By using the error signal to steer the VCO input voltage, the feedback action of the PLL accurately sets the output carrier frequency, F_{out_c}, to be

$$F_{out_c} = N_{nom} F_{ref},$$

where F_{ref} corresponds to the reference frequency, and N_{nom} is the nominal value of $N[k]$. Variation of $N[k]$ leads to modulation of the output frequency about F_{out_c}.

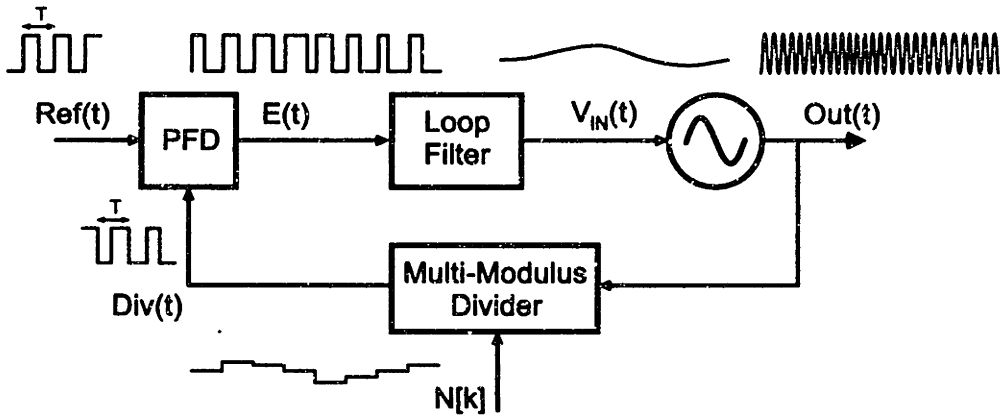


Figure 2.1: A PLL and associated signals when the divide value is varied.

2.2 Frequency Domain Model

A model of the PLL dynamics that links deviations in the divide value to phase deviations at the PLL output is now derived. Our analysis is based on the principle of superposition; in particular, we will subtract out the nominal condition that $F_{out_c} = N_{nom}F_{ref}$ when defining all phase variables of interest. Given these variable definitions, we will derive equations that describe the behavior of the PFD and Divider components. Block diagrams of all the PLL components are then presented, and combined to form the overall PLL model.

2.2.1 Definition of Phase/Frequency Signals

We begin our modeling effort by defining instantaneous frequency signals associated with the divider, PLL, and reference outputs. The instantaneous frequency of the divider output during time interval k is defined to be

$$F_{div}[k] = \frac{1}{t_k - t_{k-1}},$$

where t_k is the time at which the k^{th} rising edge of the divider output, $Div(t)$, occurs; Figure 2.2 illustrates the relevant notation. Substitution of $t_k = kT + \Delta t_k$ into the above expression yields

$$F_{div}[k] = \frac{1}{T + \Delta t_k - \Delta t_{k-1}}. \tag{2.1}$$

Alternatively, the divider output can be expressed in terms of the instantaneous frequency of the PLL output, which is assumed to be relatively constant during the time intervals marked by t_k. Specifically, we define the PLL output frequency during time interval k as $F_{out}[k]$, and write

$$F_{div}[k] = \frac{F_{out}[k]}{N[k]}. \tag{2.2}$$

Finally, the reference frequency is defined as

$$F_{ref} = 1/T.$$

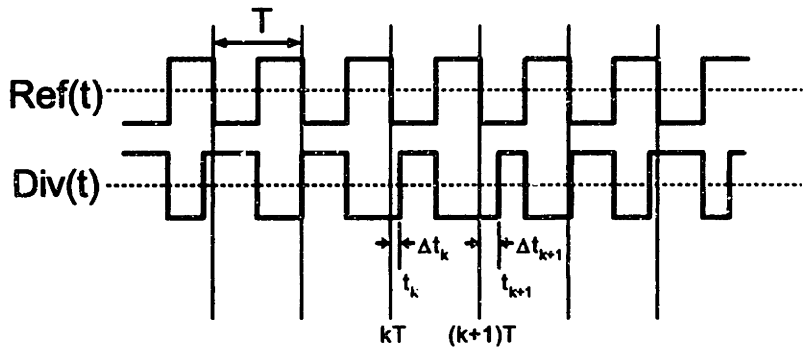


Figure 2.2: Definition of t_k.

Given the above frequency variables, we now derive expressions for phase deviations at the reference, divider, and PLL outputs in recursive form. These signals are considered to be continuous-time in nature, but will be defined only at sample times t_k. By definition, the phase deviation of the reference source is zero, so that

$$\Phi_{ref}[k] = 0. \tag{2.3}$$

Samples of the phase deviations at the divider output are defined by

$$\Phi_{div}[k] - \Phi_{div}[k-1] = 2\pi \left(F_{div}[k] - \frac{1}{T}\right)(T + \Delta t_k - \Delta t_{k-1}); \tag{2.4}$$

Similarly, samples of the PLL output phase deviation, $\Phi_{out}[k]$, are defined by

$$\Phi_{out}[k] - \Phi_{out}[k-1] = 2\pi \left(F_{out}[k] - N_{nom}\frac{1}{T}\right)(T + \Delta t_k - \Delta t_{k-1}) \tag{2.5}$$

2.2.2 Derivation of PFD Model

The relationship between $\Phi_{ref}[k]$, $\Phi_{div}[k]$, and $E(t)$ will be briefly examined here; further modeling details linking these variables are given in Chapter 9. We begin by defining a phase error signal as

$$\Phi_e[k] = \Phi_{ref}[k] - \Phi_{div}[k].$$

Substitution of Equations 2.3 and 2.4 into the above expression yields

$$\Phi_e[k] = 2\pi \frac{\Delta t_k - \Delta t_{k-1}}{T} + \Phi_e[k-1] \tag{2.6}$$

with the aid of Equation 2.1. To obtain a nonrecursive expression for $\Phi_e[k]$, we first relate its value to an initial time sample i:

$$\Phi_e[k] = 2\pi \sum_{m=i+1}^{k} \frac{\Delta t_m - \Delta t_{m-1}}{T} + \Phi_e[i]. \tag{2.7}$$

Assuming initial conditions are zero, we obtain

$$\Phi_e[k] = \frac{\Delta t_k}{T} 2\pi. \tag{2.8}$$

We relate $\Phi_e[k]$ to $E(t)$ by constructing a new signal, $\hat{\Phi}_e(t)$, as

$$\hat{\Phi}_e(t) = \sum_{k=-\infty}^{\infty} \Phi_e[k]\delta(t - kT); \tag{2.9}$$

this signal is an impulse train that is modulated by the instantaneous phase error samples, $\Phi_e[k]$. (The 'hat' symbol serves as a reminder that $\hat{\Phi}_e(t)$ is a modulated impulse train rather than a continuous signal.) As explained in Chapter 9, the error signal generated by the PFD output can be approximated as

$$E(t) \approx \frac{T}{\pi} \hat{\Phi}_e(t) + E_{spur}(t), \tag{2.10}$$

where $E_{spur}(t)$ is a square wave of period T with fifty percent duty cycle. By defining signals $\hat{\Phi}_{div}(t)$ and $\hat{\Phi}_{ref}(t)$ as

$$\hat{\Phi}_{div}(t) = \sum_{k=-\infty}^{\infty} \Phi_{div}[k]\delta(t - kT), \quad \hat{\Phi}_{ref}(t) = \sum_{k=-\infty}^{\infty} \Phi_{ref}[k]\delta(t - kT) = 0, \tag{2.11}$$

$E(t)$ is described in terms of the divider and reference phase signals as

$$E(t) \approx \frac{T}{\pi} (\hat{\Phi}_{ref}(t) - \hat{\Phi}_{div}(t)) + E_{spur}(t). \tag{2.12}$$

Note that the impulses forming $\hat{\Phi}_{div}(t)$ are referenced to time kT, while the samples in $\Phi_{div}[k]$ are referenced to time t_k. Our PFD model therefore ignores time jitter caused by Δt_k; the impact of this jitter will be discussed in Chapter 9.

2.2.3 Derivation of Divider Model

We now relate the PLL and divider output phase deviations by linearizing the action of the divider. To do so, we first decompose the divide value at time increment k as

$$N[k] = N_{nom} + n[k],$$

where $n[k]$ represents the instantaneous divide value deviation from its nominal setting of N_{nom}. (Note that both $n[k]$ and N_{nom} may be non-integer in value.) All approximations to follow are based on the assumption that $|n[k]| \ll N_{nom}$ for all k.

Proceeding with the derivation, we first combine Equations 2.2 and 2.4 to obtain

$$\Phi_{div}[k] - \Phi_{div}[k-1] = 2\pi \left(\frac{F_{out}[k]}{N[k]} - \frac{1}{T} \right) (T + \Delta t_k - \Delta t_{k-1}); \tag{2.13}$$

This expression can be approximated as

$$\Phi_{div}[k] - \Phi_{div}[k-1] \approx 2\pi \left(\frac{1}{N_{nom}} \left(1 - \frac{n[k]}{N_{nom}} \right) F_{out}[k] - \frac{1}{T} \right) (T + \Delta t_k - \Delta t_{k-1}). \tag{2.14}$$

Since $(F_{out}[k]/N_{nom})(T + \Delta t_k - \Delta t_{k-1}) \approx 1$, Equation 2.14 can be reduced to

$$\Phi_{div}[k] - \Phi_{div}[k-1] \approx \frac{2\pi}{N_{nom}} \left(\left(F_{out}[k] - N_{nom} \frac{1}{T} \right) (T + \Delta t_k - \Delta t_{k-1}) - n[k] \right). \tag{2.15}$$

Finally, we use Equation 2.5 to express the above relationship as

$$\Phi_{div}[k] - \Phi_{div}[k-1] \approx \frac{2\pi}{N_{nom}} \left(\Phi_{out}[k] - \Phi_{out}[k-1] - n[k] \right). \tag{2.16}$$

To obtain a non-recursive version of Equation 2.16, we first relate values at time k to those at an initial time sample i

$$\Phi_{div}[k] - \Phi_{div}[i] \approx \frac{2\pi}{N_{nom}} \left(\Phi_{out}[k] - \Phi_{out}[i] - \sum_{m=i+1}^{k} n[m] \right).$$

By setting $i = 0$ and assuming initial conditions are zero, we obtain

$$\Phi_{div}[k] \approx \frac{2\pi}{N_{nom}} \left(\Phi_{out}[k] - \sum_{m=1}^{k} n[m] \right). \tag{2.17}$$

To allow closed loop analysis of the overall PLL, it is advantageous to recast Equation 2.17 in terms of impulse trains as

$$\hat{\Phi}_{div}(t) \approx \frac{2\pi}{N_{nom}} \left(\hat{\Phi}_{out}(t) - \int_{-\infty}^{t} \hat{n}(\tau) d\tau \right), \tag{2.18}$$

where

$$\hat{\Phi}_{out}(t) = \sum_{k=-\infty}^{\infty} \Phi_{out}[k] \delta(t - kT), \quad \hat{n}(t) = \sum_{k=-\infty}^{\infty} n[k] \delta(t - kT),$$

and $\hat{\Phi}_{div}(t)$ is defined in Equation 2.11.

2.2.4 Modeling of Divider Sampling Operation

So far, we have examined phase deviation signals within the PLL only at sample points set by t_k. However, the output phase deviation of the PLL, $\Phi_{out}(t)$, that is generated by the VCO is assumed to be continuous-time in nature. We now discuss a frequency domain model that links this continuous-time signal to the impulse train representation, $\hat{\Phi}_{out}(t)$, used in the divider model.

$\Phi_{out}(t)$ and $\hat{\Phi}_{out}(t)$ are stochastic in nature, and therefore have undefined Fourier transforms. We seek the frequency-domain relationship between these two signals; its derivation will be obtained by temporarily assuming that these signals are deterministic in nature, and that their Fourier transforms are well defined as

$$\Phi_{out}(f) = \int_{-\infty}^{\infty} \Phi_{out}(t) e^{-j2\pi ft} dt, \quad \hat{\Phi}_{out}(f) = \int_{-\infty}^{\infty} \hat{\Phi}_{out}(t) e^{-j2\pi ft} dt.$$

Since the impulses in $\hat{\Phi}_{out}(t)$ effectively sample $e^{-j2\pi ft}$ when forming $\hat{\Phi}_{out}(f)$, we obtain

$$\hat{\Phi}_{out}(f) = \sum_{k=-\infty}^{\infty} \hat{\Phi}_{out}[k] e^{-j2\pi fTk}.$$

It is a property of the Fourier transform [61] that $\Phi_{out}(f)$ and $\hat{\Phi}_{out}(f)$ are related as

$$\hat{\Phi}_{out}(f) = \frac{1}{T} \sum_{n=-\infty}^{\infty} \Phi_{out}(f - \frac{n}{T}).$$

Thus, $\hat{\Phi}_{out}(f)$ is composed of copies of $\Phi_{out}(f)$ that are scaled in magnitude by $1/T$ and shifted in frequency from one another with spacing $1/T$. We will assume that the bandwidth of $\Phi_{out}(f)$ is much smaller than $1/T$, so that negligible aliasing occurs between the copies of $\Phi_{out}(f)$ within $\hat{\Phi}_{out}(f)$. In addition, it is assumed that the continuous-time, lowpass filtering performed by the VCO and loop filter reduces the influence of the high frequency components in $\hat{\Phi}_{out}(f)$ to negligible levels. (The influence of $\hat{\Phi}_{out}(f)$ is manifested within the PLL through the signal $\hat{\Phi}_e(t)$ by the PFD output, which passes through the loop filter and VCO dynamics before influencing $\Phi_{out}(t)$.)

These concepts are illustrated for a general signal, $x(t)$, in Figure 2.3. The drawing suggests that the overall dynamics of the PLL are influenced primarily by the 'baseband' copy of $\Phi_{out}(f)$ within $\hat{\Phi}_{out}(f)$. As shown at the bottom of the figure, we model the conversion between these signals *in the frequency-domain* as a simple scaling operation of the continuous-time signal by $1/T$. Although this assumption will break down when trying to perform noise analysis at frequencies close to $1/T$, it will prove useful and reasonably accurate when performing closed loop analysis for most frequencies of interest in our application. Note that the double outline of the box in the figure is meant to serve as a reminder that the model is an approximation since copies of the baseband signal are produced.

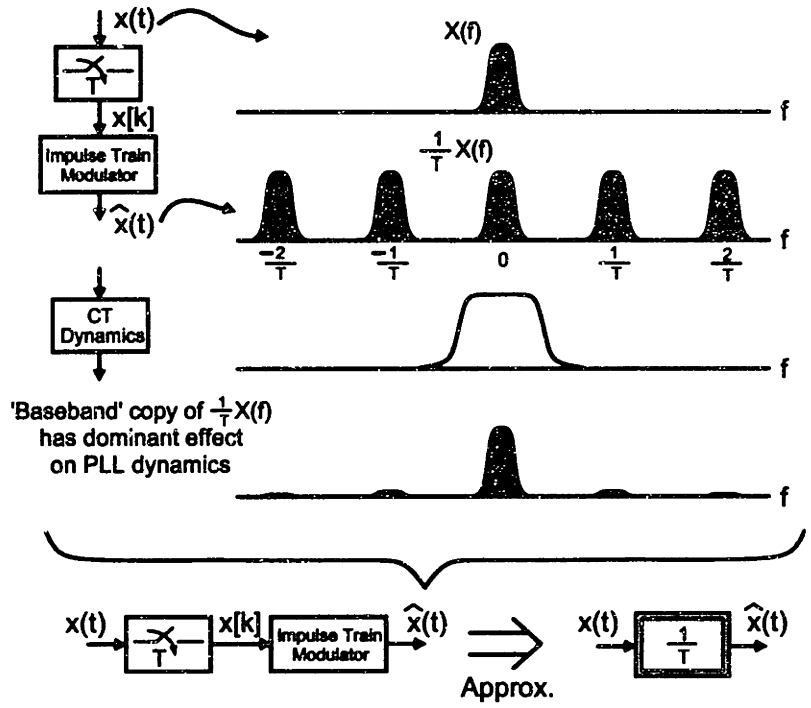


Figure 2.3: Frequency domain modeling of discrete-time signals in PLL.

2.2.5 Overall Model

Figure 2.4 displays linearized, frequency-domain models for each of the PLL components. We briefly review the significant characteristics of each block.

The divider effectively samples the continuous-time output phase deviation, $\Phi_{out}(t)$, and then divides its value by N_{nom}. The output phase of the divider, $\hat{\Phi}_{div}(t)$, is directly influenced by $\hat{\Phi}_n(t)$, which is formed as the integration of deviations in the divider value, $\hat{n}(t)$. The integration of $\hat{n}(t)$ is a consequence of the fact that the divider output is a *phase* signal, whereas $\hat{n}(t)$ causes an incremental change in the divider output *frequency*. Since $\hat{n}(t)$ and $\hat{\Phi}_n(t)$ consist of modulated impulse trains, the integration operation between them is modeled as the transfer function $1/(1-D)$, where $D = e^{-j2\pi fT}$.

The PFD can be considered as a translator between the discrete-time phase error, $\Phi_e[k]$, and the continuous-time signal, $E(t)$, that is sent into the loop filter. In other words, the PFD can be viewed as a DT to CT converter. Assuming that phase detection is implemented digitally as an XOR gate, the DT to CT conversion amounts to creating a square-wave output whose instantaneous duty cycle is a function of $\Phi_e[k]$. As Chapter 9 explains, the resulting waveform, $E(t)$, can be expressed as the sum of an impulse train modulated by $\Phi_e[k]$, and a square wave with constant duty cycle, $E_{spur}(t)$. In the PFD model shown in Figure 2.4, we have defined a perturbation

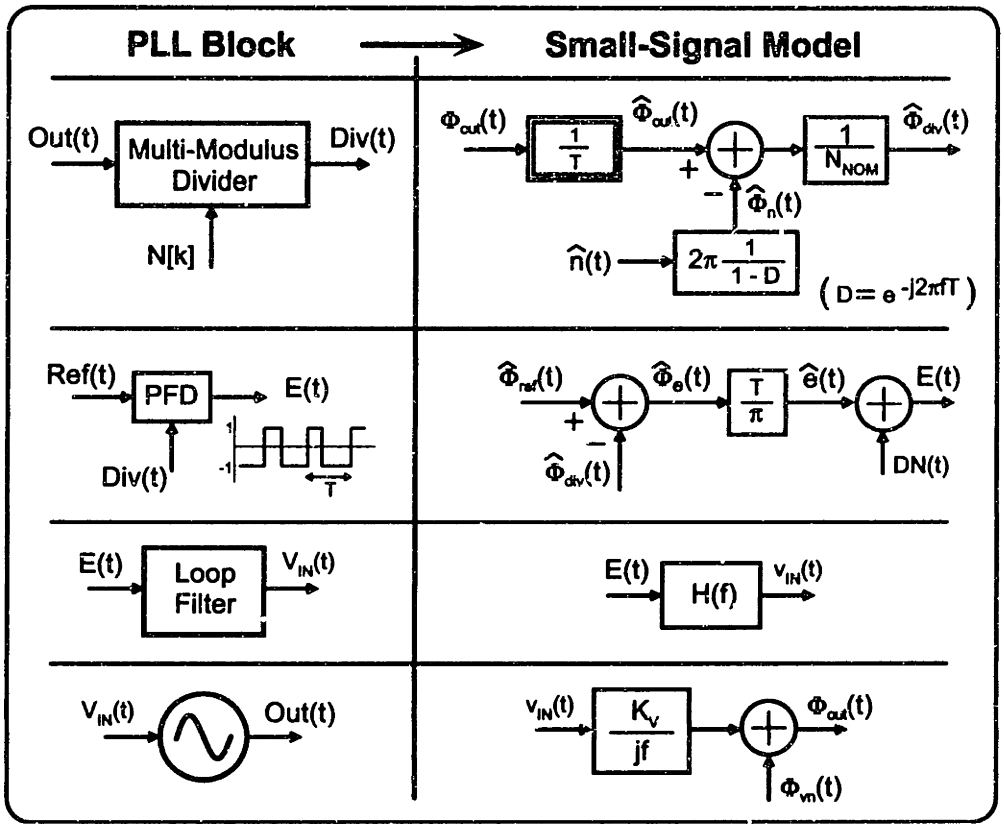


Figure 2.4: Linearized models of PLL components.

source, $DN(t)$, that consists of the sum of $E_{spur}(t)$ and jitter noise from the reference frequency, divider logic, and PFD [46]. $E_{spur}(t)$ will cause spurious noise at frequencies that are multiples of $1/T$, while the jitter noise is expected to be broadband in nature. As a side remark, it should be noted that the PFD model assumes phase deviations are small so that the frequency detection capability of the PFD need not be considered.

As for the remaining components, the loop filter is modeled as a frequency domain transfer function, $H(f)$, and the VCO is represented by an integrator with gain K_v (Hz/V) that produces an output phase signal. The VCO includes an accompanying noise source, $\Phi_{vn}(t)$, to model phase noise that occurs in a practical implementation of a VCO. In the context of analysis in this thesis, we will assume that the spectral density of $\Phi_{vn}(t)$ decreases with increasing offset frequency from the carrier at -20 dB/dec [62,63].

Each of the component models are combined to form the overall PLL linearized model shown in Figure 2.5.

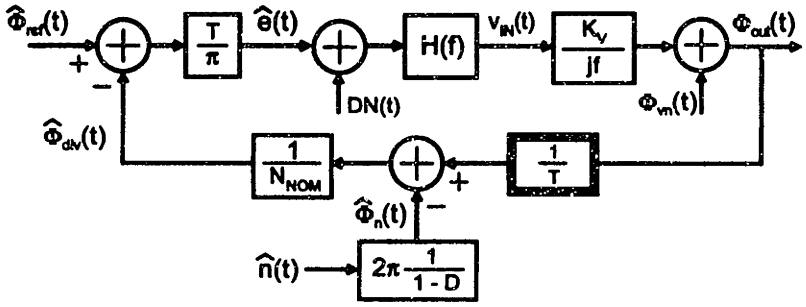


Figure 2.5: Overall PLL model.

2.3 Parameterization of the PLL Model

It will prove useful to parameterize the model shown in Figure 2.5 in terms of a transfer function defined as

$$G(f) = \frac{H(f)K_v/(\pi N)}{jf + H(f)K_v/(\pi N)}. \tag{2.19}$$

Since $H(f)$ is lowpass in nature, $G(f)$ has the following property:

$$G(f) \longrightarrow 1 \text{ as } f \longrightarrow 0, \qquad G(f) \longrightarrow 0 \text{ as } f \longrightarrow \infty, \tag{2.20}$$

implying that $G(f)$ is also a lowpass filter. The value of introducing $G(f)$ is that all transfer functions of interest within the PLL can be parameterized by it, and therefore be easily related to one another.

The relationships between the divider signal, $\hat{\Phi}_n(t)$, VCO noise, $\Phi_{vn}(t)$, and PFD noise, $DN(t)$, to the output phase, Φ_{out}, are given by the transfer functions shown in Figure 2.6; these transfer functions were derived from Figure 2.5. Figure 2.6 provides the insight that VCO noise is highpass filtered and the PFD noise lowpass filtered before influencing the output phase.

The bottom portion of Figure 2.6 provides an alternative representation of the influence of the divider signal on the output phase. Its derivation is obtained by approximating the delay element D as

$$D = e^{-j2\pi fT} \approx 1 - j2\pi fT, \quad \text{for } f \ll 1/T, \tag{2.21}$$

and changing the order of the two cascaded blocks between $\hat{n}$ and Φ_{fm}. The last model will be used in the modulation analysis to follow, and reveals that the divider modulation signal, $\hat{n}(t)$, effectively passes through a path consisting of a D/A converter and lowpass filter and is then converted to phase by an integration operation.

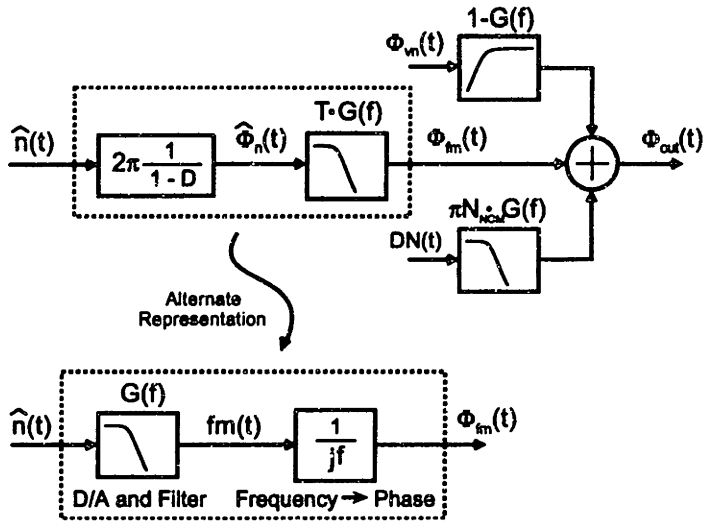


Figure 2.6: Parameterized PLL model.

2.4 Frequency Control Without Σ-Δ Modulation

Figure 2.7 illustrates modulation of the PLL output frequency that occurs when its divider value, $\hat{n}(t)$, is varied. (For convenience in later analysis, we introduce $n(t)$ as a continuous-time signal that is sampled to form the modulated impulse train, $\hat{n}(t)$.) The output frequency is changed about the carrier frequency as illustrated, resulting in a form of frequency shift keyed (FSK) modulation. Since $\hat{n}(t)$ can only be altered in integer steps, the minimum deviation of the output frequency is $1/T$.

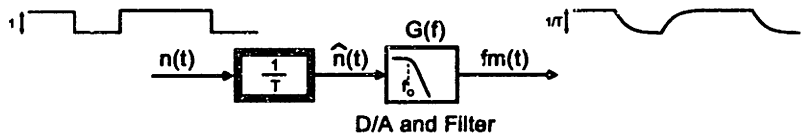


Figure 2.7: Simple FSK modulation of the PLL.

Referring back to Figure 2.6, the achievement of good noise performance requires the value of cutoff frequency of $G(f)$, defined as f_o, to be well below $1/T$; this must be done in order to properly attenuate the spurious tones present in $DN(t)$ [28]. An interesting viewpoint of this situation is to consider the PFD output as a coarse signal that is dithered between 1 and -1 and then smoothed by the PLL dynamics, $G(f)$, to produce a finer resolution signal. For such smoothing to be effective, the dynamics of the PLL must be much slower than the dithering rate.

To achieve good modulation performance, it is desirable to set the value of f_o high enough that the bandwidth of $G(f)$ does not attenuate the modulation signal in its

high frequency region. Modulation at high data rates therefore requires a correspondingly high value of f_o, which in turn forces $1/T$ to be even higher. Unfortunately, a high value of $1/T$ yields poor frequency resolution, yielding a direct tradeoff between the achievement of high resolution and fast dynamics.

2.5 Σ-Δ Modulation Principles

By using fractional-N techniques, we can decouple the frequency resolution from the choice of reference frequency by using a 'dithering modulator'; this method increases the resolution of the synthesizer by dithering the divide value at a high rate and using the PLL dynamics, $G(f)$, to perform smoothing. The resulting 'averaged' value of $\hat{n}(t)$ can be changed in 'fractional' increments, so the effective value of $\hat{n}(t)$ and N_{nom} are no longer constrained to be integer. The price paid for the increase in resolution is the introduction of quantization noise.

The characteristics of this new quantization noise, which we will denote as $\hat{q}(t)$, are determined by the method of dithering. If periodic dithering is chosen, as effectively done by the PFD, then the quantization noise will have spurious components. The spur of lowest frequency must occur at a value less than or equal to $1/(2T)$ since $\hat{n}(t)$ consists of samples spaced T apart. The low frequency spurious content imposes difficulty in realizing a $G(f)$ with high bandwidth that adequately attenuates such components. Moreover, the frequency of these spurs will typically shift as the average of $\hat{n}(t)$ is changed, which further complicates efforts of achieving good noise performance. Typically, this problem is dealt with by cancelling out such noise at the PFD output by using a method known as phase interpolation [46]. Such an approach requires a D/A converter operating at the reference frequency, which can be very unattractive when seeking a low power solution since a high reference frequency is desirable.

Rather than using periodic dithering, a better solution is to randomize the dithering pattern such that it accurately produces the desired average divider value while creating quantization noise with minimal spurious content. The quest for non-periodic dithering has led to several techniques that introduce randomization through various means [23,28]. The most elegant of these methods appears to be a method presented by Riley et al. that draws from the field of Σ-Δ D/A converters [23]. Such D/A converters are capable of achieving output analog signals of high resolution with a coarse D/A converter; the high resolution is obtained with a dithering technique known as Σ-Δ modulation. This method produces quantization noise that is 'shaped' such that most of its energy is placed at high frequencies. Low spurious content can be achieved provided that the order of the modulator is adequately high and/or the input to the converter varies sufficiently with time [47].

The use of Σ-Δ modulation in fractional-N synthesis is illustrated in Figure 2.8. The Σ-Δ modulator translates the M-bit digital input sequence to an L-bit sequence,

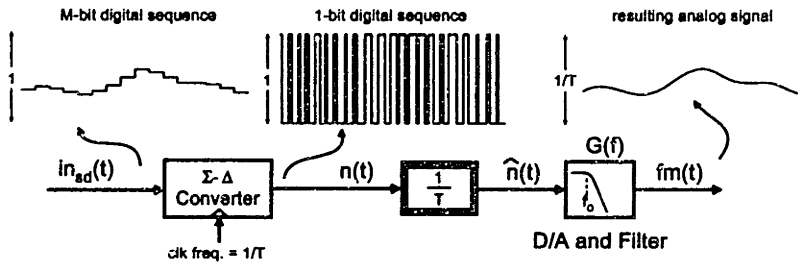


Figure 2.8: Σ-Δ modulation applied to Fractional-N synthesis.

where $L < M$. (For simplicity in the figure, we show the case where $L = 1$; the remaining portion of this thesis will focus on the case in which $L > 1$.) As illustrated, the M-bit input sequence is assumed to vary slowly with respect to the rate of dithering so that the smoothing filter has an adequate number of samples to 'average' for reconstruction of the high bit-width input of the modulator.

2.5.1 Fractional-N Modulator Model

Proper modeling of the Σ-Δ converter is dependent on the architecture chosen. Two types prevail — the single loop and MASH structure. For a transmitter application, we argue that the MASH structure is the better choice for four reasons. First, it is unconditionally stable, so that there is never a need to reset internal integrators. Such actions cause glitches in the dithered signal, which can lead to missing data bits and/or timing jumps in the transmitted sequence. Second, the MASH architecture is readily pipelined (Chapter 8), which leads to considerable power savings. Third, the MASH topology imposes no transfer function on its input which would affect the modulated waveform. Finally, the MASH structure supports a full dynamic range regardless of its order.

Figure 2.9 displays the model for an n^{th} order MASH Σ-Δ converter placed within the PLL modulation section. The MASH model is represented as the addition of the delayed input signal and the shaped quantization noise, $\hat{q}(t)$. Under the assumption of a high order structure and/or a sufficiently varying input, the quantization error is modeled as the output of a filter with transfer function $(1 - D)^n$ that is driven by a white noise sequence, $\hat{r}(t)$, whose samples are uniformly distributed between 0 and 1. (Simulations of the prototype confirm that such modeling is accurate in our application when modulation is applied.) The updated PLL model places the Σ-Δ to the right of the sampling operation since it is discrete-time in nature, and includes the integration operation that yields $\Phi_{fm}(t)$.

A frequency domain interpretation of the interaction between the Σ-Δ modulator and PLL dynamics is revealed through the example spectra in Figure 2.9. The slowly varying nature of the input causes its energy to be confined to low frequencies relative

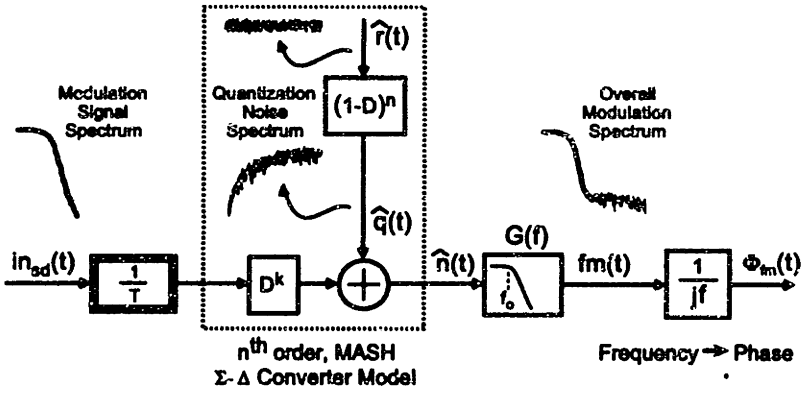


Figure 2.9: Model of frequency modulation of the PLL output when its divide value is dithered by a Σ-Δ modulator.

to $1/T$. The quantization noise has low energy content at these low frequencies due to the shaping action of the Σ-Δ. By filtering the high frequency portion of the overall signal, $\hat{n}(t)$, with $G(f)$, much of the quantization noise is removed without affecting the input. (This last point assumes that the bandwidth of the input is less than f_o.)

It is convenient to recast Figure 2.9 into the model shown in Figure 2.10, which separates the influence of the quantization noise from the desired modulation signal. The repartitioned model ignores the delay of the input through the Σ-Δ since it has

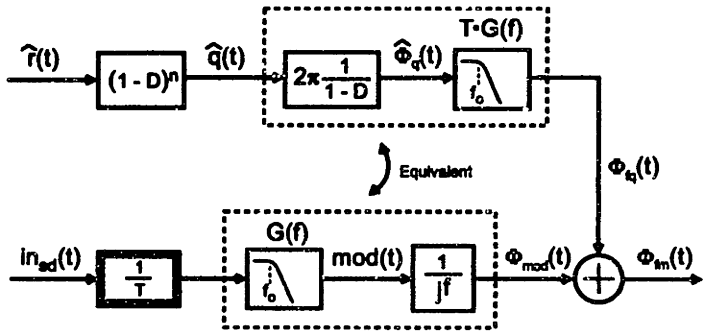


Figure 2.10: Alternate representation of Σ-Δ model.

no influence on the dynamics of the PLL. The noise section can be further simplified by deriving the power spectrum of $\hat{\Phi}_q(t)$ and then removing all blocks to the left of this signal. To do so, we use the fact that $D = e^{-j2\pi fT}$ to obtain

$$S_{\hat{\Phi}_q}(f) = \left|2\pi\left(1 - e^{-j2\pi fT}\right)^{(n-1)}\right|^2 S_{\hat{r}}(f). \tag{2.22}$$

After simplifying the above expression and substituting $S_{\hat{r}}(f) = 1/12$, which is derived on the assumption that $\hat{r}(t)$ is white and uniformly distributed between 0 and 1, we

obtain

$$S_{\hat{\Phi}_q}(f) = \frac{(2\pi)^2}{12}\left(2\sin(\pi f T)\right)^{2(n-1)}. \tag{2.23}$$

Figure 2.11 illustrates the resulting PLL model, which now includes the effect of Σ-Δ modulation; the structure is partitioned into modulation and noise analysis sections to aid analysis in the following chapters.

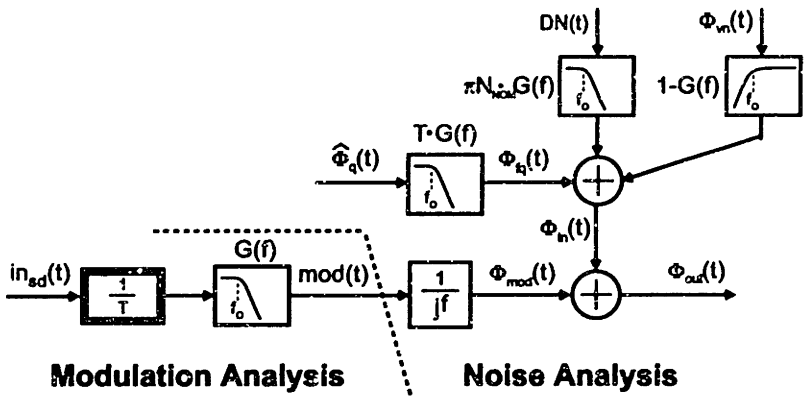


Figure 2.11: Separation of PLL model into signal and noise sections.

2.6 Summary

This chapter presented a linearized, frequency-domain model of the PLL. The effects of using Σ-Δ modulation to increase synthesizer resolution were included in the analysis, and transfer functions were derived that describe the influence of modulation and noise sources on the output phase of the synthesizer. These transfer functions are parameterized by a common function, $G(f)$, which allows ready comparison to one another. The chapters to follow use these transfer functions to perform analysis of modulation and noise performance of the fractional-N synthesizer.

Chapter 3

Noise Properties of a Modulated Synthesizer

This chapter examines the influence of the PLL noise sources in Figure 2.11 on the output spectrum of the synthesizer. We will focus particularly on the effects of such noise at high frequency offsets from the carrier; the noise requirements for a transmitter are very strict in this range to avoid interfering with users in adjacent channels. In the case of the DECT standard, the phase noise density can be no higher than -131 dBc/Hz at a 5 MHz offset [14, 15]. Noise at low frequency offsets is less critical, and need only be below the modulation signal by enough margin to insure an adequate signal-to-noise ratio.

We begin by exploring the nonlinear relationship between the overall phase noise density modeled in Figure 2.11 and the output spectrum when modulation is applied. The overall phase noise density is then broken down into its three major components, which are PFD, VCO, and Σ-Δ quantization noise. The influence of the PLL dynamics, $G(f)$, and Σ-Δ sample rate, $1/T$, on each of these components is explored. It is shown that the settings of $G(f)$ and $1/T$ have negligible impact on the VCO noise, and should be set according to the level of attenuation required of the Σ-Δ quantization noise. (The Σ-Δ quantization noise is assumed to be higher than the PFD noise at the frequencies of concern, so that the influence of PFD noise can be neglected.) The chapter concludes by quantifying the parameter space of $G(f)$ and $1/T$ which reduces the influence of the Σ-Δ quantization noise on the overall phase noise density to -136 dBc/Hz at 5 MHz offset.

3.1 The Relationship Between $\Phi_{tn}(t)$, $\Phi_{mod}(t)$, and the Output Spectrum

Figure 3.1 illustrates the connection between the phase variables modeled in Figure 2.11 and the output of the transmitter, which is a phase modulated sine wave.

Reviewing the notation, $Out(t)$ is the transmitter output, $\Phi_{mod}(t)$ is the phase deviation of $Out(t)$ due to modulation, and Φ_{tn} is the overall phase noise of $Out(t)$.

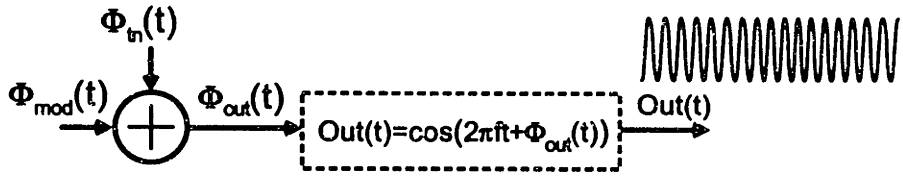


Figure 3.1: Illustration of the relationship between modeled phase, $\Phi_{out}(t)$, and the transmitter output, $Out(t)$.

The relationship in Figure 3.1 is expressed mathematically as

$$Out(t) = \cos(2\pi f_c t + \Phi_{mod}(t) + \Phi_{tn}(t)). \tag{3.1}$$

Using a familiar trigonometric identity, we expand Equation 3.1 as

$$Out(t) = \cos(2\pi f_c t + \Phi_{mod}(t))\cos(\Phi_{tn}(t)) - \sin(2\pi f_c t + \Phi_{mod}(t))\sin(\Phi_{tn}(t)). \tag{3.2}$$

We form an approximation of the above expression based on the assumption that the noise fluctuations are small so that $|\Phi_{tn}(t)| \ll 1$ for all t

$$Out(t) \approx \cos(2\pi f_c t + \Phi_{mod}(t)) - \sin(2\pi f_c t + \Phi_{mod}(t))\Phi_{tn}(t) \tag{3.3}$$

To obtain the power spectrum of $Out(t)$, we take the autocorrelation of Equation 3.3 and make use of the fact that $\Phi_{tn}(t)$ has zero mean and is uncorrelated with the modulation signal, $\Phi_{mod}(t)$. Defining $R_{out}(t) = R\{Out(t)\}$ as the autocorrelation of $Out(t)$, we obtain

$$R_{out}(t) \approx R\{\cos(2\pi f_c t + \Phi_{mod}(t))\} + R\{\sin(2\pi f_c t + \Phi_{mod}(t))\}R\{\Phi_{tn}(t)\}$$

The output power spectrum, defined as $S_{out}(f) = S\{Out(t)\}$, is found by taking the Fourier transform of the above expression:

$$S_{out}(f) \approx S_{out_m}(f) + S_{out_m}(f) * S_{\Phi_{tn}}(f), \tag{3.4}$$

where '$*$' denotes the convolution operation, and

$$S_{out_m}(f) = S\{\sin(2\pi f_c t + \Phi_{mod}(t))\}, \quad S_{\Phi_{tn}}(f) = S\{\Phi_{tn}(t)\}.$$

Thus, we see that when directly modulating a frequency synthesizer, the output spectrum is formed as the addition of a noiseless modulation spectrum, S_{out_m}, and a 'smoothed' noise spectrum, $S_{out_m}(f) * S_{\Phi tn}(f)$. This smoothing operation has a significant impact on the spurious performance of the transmitter, as discussed in the following section.

3.2 Interaction of Modulation and Noise on Output Spectrum

It is generally assumed that a non-tunable, bandpass filter is used at the output of the transmitter to remove harmonic components of the VCO. This filter must be capable of passing all channels available to the transmitter, and will be assumed to have a bandwidth that is on the order of 15 MHz in the context of this thesis.

Any out-of-channel noise emitted by the modulated PLL within the bandwidth of the output bandpass will pass through the filter and interfere with other channels. The near-far problem [46] will accentuate the effect of such noise, and leads to strict out-of-channel noise requirements. Outside this bandwidth, the noise requirements for the PLL output are less strict due to the attenuation offered by the filter. Noise requirements at frequencies within the channel are also less strict, and need only be below the modulation signal by enough margin to insure an adequate signal-to-noise ratio. Therefore, it is at *intermediate offset frequencies*, where the noise is neither overshadowed by the modulation spectrum or reduced by the output filter, that *requirements are most stringent.* Our target performance specification in this region is to achieve output noise that is less than -131 dBc/Hz at 5 MHz.

Figure 3.2 illustrates Equation 3.4 for the case in which GFSK modulation is applied; the two plots illustrate the noiseless modulation spectrum, $S_{out_m}(f)$, and the phase noise spectrum, $S_{\Phi_{tn}}(f)$, before and after smoothing. In the figure, we see that the spurious tone at $1/T$ is converted to phase noise by the smoothing operation. Therefore, excellent spurious performance can be achieved when directly modulating a frequency synthesizer — all spurs are convolved with the modulation spectrum and turned into phase noise.

Figure 3.2 reveals that the transmitter output spectrum will experience increased phase noise levels at frequencies close to $1/T$ due to the convolution of the modulation spectrum with the reference frequency spur. Fortunately, noise at this frequency range will be significantly attenuated by the output bandpass filter so long as $1/T$ is set sufficiently higher than its bandwidth.

The spectra $10 \log S_{out_m}(f)$ and $10 \log S_{\Phi_{tn}}(f)$ are assumed to have units of dBc/Hz, so that

$$\int_{-\infty}^{\infty} S_{out_m}(f) df \approx 1.$$

Assuming that $S_{tn}(f)$ contains negligible levels of spurious tones in the intermediate frequency range, and that its shape does not contain sharp peaks relative to the bandwidth of the modulation spectrum, we can approximate the smoothed spectrum within this region as

$$S_{out_m}(f) * S_{\Phi tn}(f) \approx S_{\Phi tn}(f) \quad (f \text{ in intermediate region}).$$

Simulations of the prototype system indicate that the above approximation is accurate at frequency offsets close to 5 MHz for the prototype system discussed in Chapter 10.

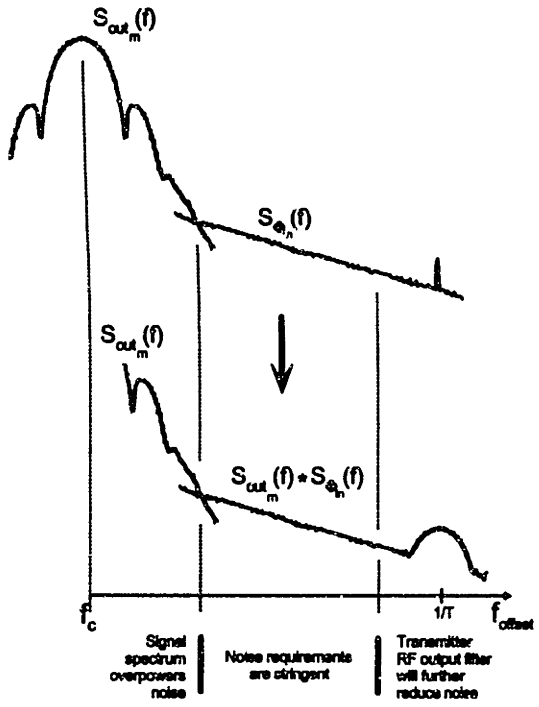


Figure 3.2: Signal and noise components of the modulated output spectrum.

As a sidenote, it is worthwhile to compare the VCO based approach of upconversion to that based on mixers. In the case of ideal mixer-based upconversion, the spurs in the local oscillator (L.O.) signal are also convolved with the modulation signal and turned into phase noise. However, a practical mixer also passes 'feedthrough' components to its output which are not convolved with the modulation signal; any spurs in their spectrum are passed to the output spectrum. The achievement of low spurious noise with a direct conversion approach using mixers is highly problematic due to this issue.

3.3 The Influence of PLL Parameters on Noise Performance

The primary PLL parameters that must be considered in designing the synthesizer are the Σ-Δ sample rate, $1/T$, and parameterizing transfer function, $G(f)$. (Note that the reference frequency is also equal to $1/T$.) To evaluate the influence of these parameters on noise performance, it is necessary to decompose the overall noise, $\Phi_{tn}(t)$, in terms the various noise sources that influence it. Figure 3.3 displays example power spectra of these noise components. The VCO noise, $\Phi_{vn}(f)$, is assumed to have a power spectral density, $S_{\Phi_{vn}}(f)$, that rolls off at -20 dB/dec in the frequency ranges

considered [62,63]. The Σ-Δ quantization noise, $\hat{\Phi}_q(t)$, has a power spectrum, $S_{\hat{\Phi}_q}(f)$, that is periodic in frequency about $1/T$ due to the fact that it is a discrete-time signal with sample rate of $1/T$. The PFD noise, $DN(t)$, is composed of a spurious signal with a fundamental frequency of $1/T$ and random, white noise resulting from jitter in the divider and PFD; its spectrum is denoted as $S_{DN}(f)$.

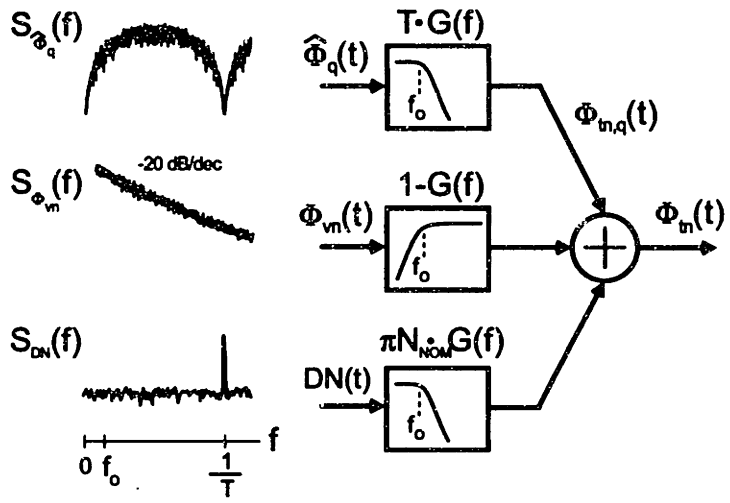


Figure 3.3: View of noise components.

As seen by the many different transfer functions in Figure 3.3, the settings of $G(f)$ and $1/T$ have dramatically different effects on the manner in which these noise sources influence the overall output noise, $\Phi_{tn}(t)$. To achieve a design procedure involving these parameters, we will break up analysis of their influence into two sections. The first section will use qualitative arguments to deduce a design strategy, and the second will quantitatively establish a design space for the PLL parameters that achieves the required noise performance.

3.3.1 Qualitative Analysis

Table 3.1 provides a qualitative description of the influence of $G(f)$ and $1/T$ on the overall phase noise, $\Phi_{tn}(t)$, with respect to the individual noise sources depicted in Figure 3.3. The statements in the table are derived by inspection of Figure 3.3, and are limited to the consideration of noise performance at intermediate frequency offsets. (This frequency range is assumed to be higher than the cutoff frequency of $G(f)$.)

Inspection of Table 3.1 reveals that the PLL parameters have no influence on the VCO at the frequency range considered. Therefore, $\Phi_{vn}(t)$ need not be considered when designing the PLL. However, the VCO must be properly designed so that its phase noise is less than the overall desired noise specification.

	Decrease cutoff frequency of $G(f)$	Increase order of $G(f)$	Increase $1/T$
VCO noise, $\Phi_{vn}(t)$	no effect	no effect	no effect
PFD noise, $DN(t)$	reduced	reduced	reduced
Quant. noise, $\hat{\Phi}_q(t)$	reduced	reduced	reduced

Table 3.1
Influence of parameters in $G(f)$ and of $1/T$ on individual noise source contributions to the overall phase noise spectral density, $S_{\Phi_{tn}}(f)$, at intermediate frequency offsets.

The influence of $S_{DN}(f)$ on $S_{\Phi_{tn}}(f)$ is given by the expression

$$|\pi N_{nom} G(f)|^2 S_{DN}(f),$$

which reveals that the PFD noise is multiplied by N_{nom}^2. Therefore, it is highly beneficial to use a low divide value to reduce the effects of PFD noise; this objective is accomplished by choosing a high reference frequency, $1/T$. In fact, to achieve attenuation of the spurious portion of $DN(t)$ by the output bandpass filter, $1/T$ *should be set higher than its bandwidth.* Reduction of the PFD noise is also accomplished by choosing a low cutoff frequency and/or high order for $G(f)$.

Reduction of the Σ-Δ quantization noise is achieved by the same PLL parameter conditions specified for the PFD noise: a high reference frequency, low cutoff frequency, and high PLL order are all desirable. Since much of the energy of the Σ-Δ quantization noise is shaped into high frequencies, we will assume that this noise source dominates over the PFD noise at intermediate frequency offsets. Therefore, quantitative selection of the PLL parameters will be based on achieving adequate attenuation of $\hat{\Phi}_q(t)$. (For the design parameters chosen for the prototype, simulated and measured results in Chapter 11 verify that the Σ-Δ noise is the dominant noise source at frequency offsets close to 5 MHz.)

3.3.2 Quantitative Analysis

We now compute the PLL parameter space that achieves overall output noise that is less than -131 dBc/Hz at 5 MHz offset. Several assumptions will be made in this analysis. First, the crossover point of the modulation spectrum, $S_{out_m}(f)$, and smoothed noise spectrum, $S_{out_m}(f) * S_{\Phi_{tn}}(f)$, will be considered to be greater than f_o. This assumption holds when the data rate is set as high as possible so that the bandwidth of the modulation signal is the same or higher than the bandwidth of the PLL dynamics, $G(f)$. Second, we assume a simple parameterization of $G(f)$ as a Butterworth transfer function with order m and a cutoff frequency of f_o:

$$|G(f)|^2 = \frac{1}{1 + (f/f_o)^{2m}}. \tag{3.5}$$

The above expression is chosen for the sake of simplicity in calculations; other filter responses could certainly be implemented. Third, it will assumed that the VCO noise density rolls off at -20 dB/dec.

We begin by defining $S_{\Phi_{tn,q}}(f)$ to be the output noise density that occurs if all noise sources are set to zero except for the Σ-Δ quantization noise; this function is calculated as

$$S_{\Phi_{tn,q}}(f) = \frac{1}{T}\left(\frac{(2\pi)^2}{12}\left(2\sin(\pi fT)\right)^{2(n-1)}\right)|T \cdot G(f)|^2 . \tag{3.6}$$

We can simplify the above expression by taking advantage of the assumption that $1/T$ is higher than the bandwidth of the output bandpass filter. This choice confines the critical frequency region to $f_o \ll f \ll 1/T$, so that the following approximations can be made:

$$\sin(\pi fT) \approx \pi fT, \qquad |G(f)|^2 \approx (f_o/f)^{2m} . \tag{3.7}$$

Equation 3.6 then becomes

$$S_{\Phi_{tn,q}}(f) \approx T\frac{(2\pi)^2}{12}(2\pi fT)^{2(n-1)}(f_o/f)^{2m}. \tag{3.8}$$

For convenience, the above equation is placed in a logarithmic scale that yields units of dBc/Hz for the spectral density magnitude:

$$10\log(S_{\Phi_{tn,q}}(f)) \approx 10\log\left(T\frac{(2\pi)^{2n}}{12}T^{2(n-1)}f_o^{2m}\right) - 20(m+1-n)\log(f). \tag{3.9}$$

This expression reveals that $S_{\Phi_{tn,q}}(f)$ has a constant rolloff, within the frequency range considered, of $-20(m+1-n)$ dB/dec. Intuitively, $S_{\Phi_{tn,q}}(f)$ should be matched in slope to the VCO noise, which requires that the order of the Σ-Δ equal the order of $G(f)$, i.e., $n = m$. We will assume that this constraint holds, so that the order of $G(f)$ is considered to be n from this point forward. The constant term in Equation 3.9 should be chosen to reduce $S_{\Phi_{tn,q}}(f)$ below the VCO noise limit by proper adjustment of f_o.

The last step in our analysis is to determine the values of f_o that achieve the noise requirements under different values of Σ-Δ order, n, and reference frequency, $1/T$. Rearrangement of equation 3.8 and substitution of $m = n$ leads to the expression

$$f_o = f^{1/n}\left(S_{\Phi_{tn,q}}(f)\right)^{1/(2n)}\frac{12^{1/(2n)}}{2\pi}\left(\frac{1}{T}\right)^{1-1/(2n)} . \tag{3.10}$$

Figure 3.4 provides a plot of Equation 3.10 with $10\log S_{\Phi_{tn,q}}(f)$ set at -136 dBc/Hz at $f = 5$ MHz.

As a minor detail, it should be noted that Figure 3.4 is only valid when $G(f)$ is described by Equation 3.5. In practice, this assumption is not quite true. As discussed

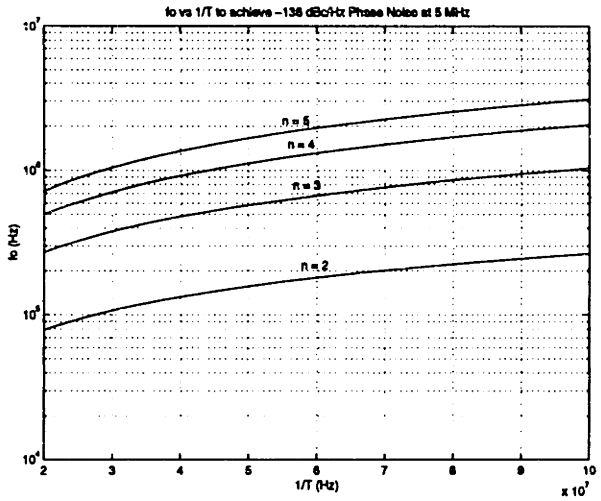


Figure 3.4: Calculation of f_o, $1/T$, and n that achieve $S_{tn,q}(f)$ of -136 dBc/Hz at 5 MHz offset.

in Chapter 6, the effects of a parasitic pole/zero pair, f_{cp} and f_z, must be included in the transfer function of $G(f)$ in Equation 3.5 since the PLL will be implemented as a type II system. This parasitic pole/zero pair will scale $S_{\Phi tn,q}(f)$ by the factor $|f_{cp}/f_z|^2$.

Of greater significance is the fact that Figure 3.4 reveals that there is a cost for increasing f_o; namely, n and/or $1/T$ must be increased in order to maintain the required noise performance. For instance, the choice of $f_o = 80$ kHz allows relatively low settings of $n = 2$ and $1/T = 20$ MHz, while $f_o = 1$ MHz requires n to be at least 3 with a high value of $1/T = 100$ MHz, or $1/T$ to be at least 30 MHz with a high value of $n = 5$.

3.4 Summary

This chapter examined the influence of PLL noise sources and component parameters on the output spectrum of the synthesizer. It was argued that the reference frequency, which is the same as the Σ-Δ sample rate, should be set higher than the bandwidth of the output bandpass filter. In addition, an argument was made that the Σ-Δ quantization noise is the chief noise source that must be considering when designing the transmitter to achieve the required noise performance. The parameter space of PLL parameters was presented that achieves reduction of the overall phase noise due to Σ-Δ quantization noise to -136 dBc/Hz at 5 MHz offset.

Chapter 4

The Challenge of High Data Rate Modulation

Using the fractional-N approach to frequency synthesis, it is straightforward to realize a transmitter that performs phase/frequency modulation in a continuous manner by direct modulation of the synthesizer. Figure 4.1 illustrates a simple transmitter capable of GMSK or GFSK modulation from [22]. The binary data stream is first convolved with a digital FIR filter that has a Gaussian shape. (Physical implementation of this filter can be accomplished with a ROM whose address lines are controlled by consecutive samples of the data and time information generated by a counter.) The digital output of this filter is summed with a nominal divide value and fed into the input of a digital Σ-Δ converter, the output of which controls the instantaneous divide value of the PLL. The resulting variation of the divide value causes the output frequency to be varied according to the modulation data about the carrier frequency set by the nominal divide value. Assuming that the PLL dynamics have sufficiently high bandwidth, the characteristics of the modulation waveform are determined primarily by the digital FIR filter and thus accurately set.

Figure 4.2 depicts a linearized model of the synthesizer dynamics in the frequency domain. The digital transmit filter confines the modulation data to low frequencies, the Σ-Δ modulator adds quantization noise that is shaped to high frequencies, and the PLL acts as a lowpass filter that passes the input but attenuates the Σ-Δ quantization noise. In the figure, $G(f)$ is calculated as

$$G(f) = \frac{K_v H(f)/(\pi N_{nom})}{jf + K_v H(f)/(\pi N_{nom})}, \tag{4.1}$$

where $H(f)$, K_v, and N_{nom} are the loop filter transfer function, the VCO gain (in Hz/V), and the nominal divide value, respectively. An analogy between the fractional-N modulator and a Σ-Δ D/A converter can be made by treating the output frequency of the PLL as an analog voltage.

A key issue in the system is that the Σ-Δ modulator adds quantization noise

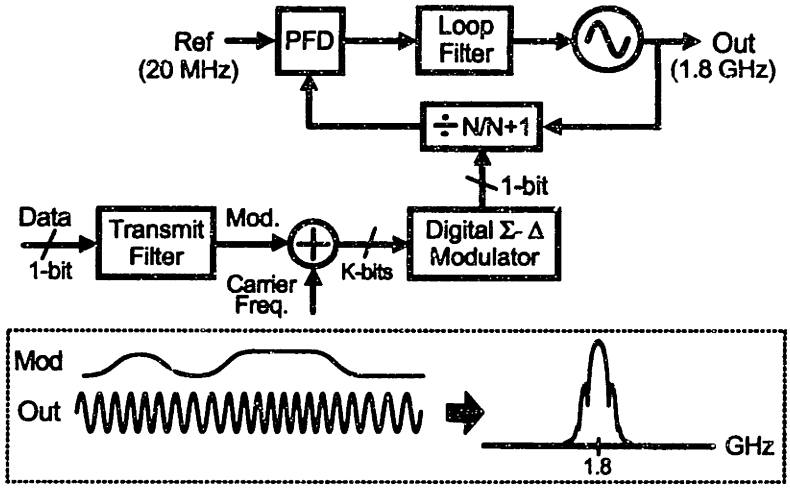


Figure 4.1: A spectrally efficient, fractional-N modulator.

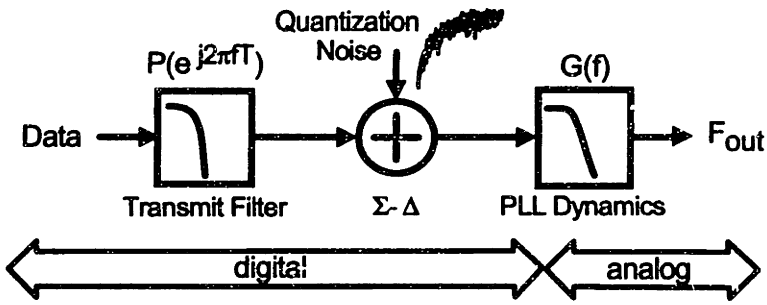


Figure 4.2: Linearized model of fractional-N modulator.

at high frequency offsets from the carrier. The noise requirements for a transmitter are very strict in this range to avoid interfering with users in adjacent channels. In the case of the DECT standard, the phase noise density can be no higher than -131 dBc/Hz at a 5 MHz offset [21].

As discussed in Chapter 3, sufficient reduction of the Σ-Δ quantization noise can be accomplished through proper choice of the Σ-Δ sample rate, which is assumed to be equal to the reference frequency, and the PLL transfer function, $G(f)$. (Note that this problem is analogous to that encountered in the design of Σ-Δ D/A converters, except that the noise spectral density at high frequencies, rather than the overall signal-to-noise ratio, is the key parameter.) One way of achieving a low spectral density for the noise is to use a high sample rate for the Σ-Δ so that the quantization noise is distributed over a wide frequency range and its spectral density reduced. Alternatively, the attenuation offered by $G(f)$ can be increased; this is accomplished by decreasing its cutoff frequency, f_o, or increasing its order, n.

Unfortunately, a low value of f_o adversely affects modulation performance by

lowering the achievable data rate of the transmitter. This fact can be observed from Figure 4.2; the modulation data must pass through the dynamics of the PLL, so that its bandwidth is restricted by that of $G(f)$.

In the remaining portions of this chapter, we will quantify the relationship between the PLL parameters that is required to achieve the desired noise and data rate performance. The PLL parameters considered are its bandwidth, f_o, its order, n, and the Σ-Δ sample rate, $1/T$.

4.1 Data Rate versus PLL Bandwidth

To calculate the optimal choice of f_o relative to data rate, we temporarily ignore the issue of noise and examine the modulation path depicted in Figure 4.3, which is taken directly from Figure 2.11. (Note that $mod(t)$ has units of Hz.) Figure 4.3 includes the effects of the transmit filter with the input signal defined as a binary, continuous signal, $in_w(t)$.

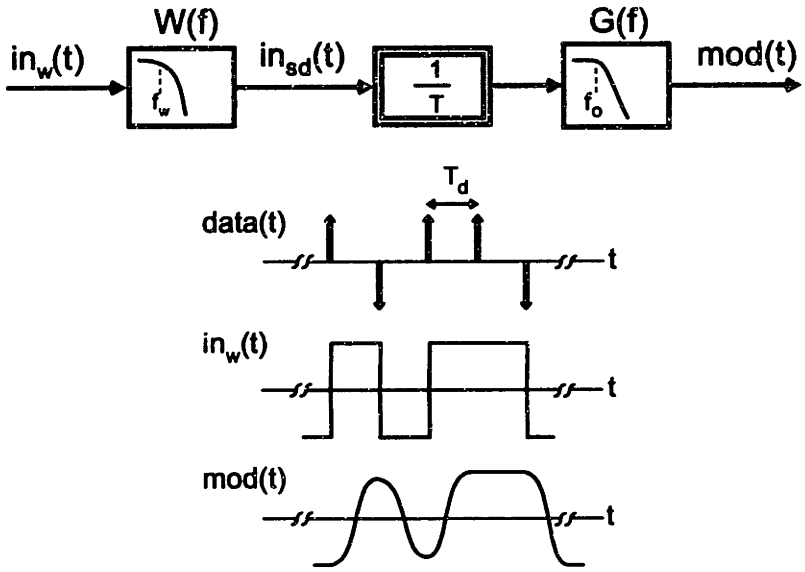


Figure 4.3: Model of data path.

In practice, the transmit filter, $P(e^{j2\pi fT})$, is implemented in discrete-time; its input data is assumed to be in the form of binary modulated impulses shown as $data(t)$ in the figure. The connection between $P(e^{j2\pi fT})$ and $W(f)$ in the figure is that $P(e^{j2\pi fT})$ consists of samples of $rect(T_d, t) * W(f)$, where '$*$' is the convolution operator, and $rect(T_d, t)$ is defined to be $1/T_d$ for $0 \leq t < T_d$ and zero otherwise. We use the $W(f)$ parameterization in our analysis here since it is consistent with the description of GMSK modulation in the original paper [49].

Figure 4.3 reveals that the signal path is characterized by the joint filtering action of $W(f)$ and $G(f)$. We define an overall transmit filter as $T(f)$, and readily derive

this transfer function from the block diagram as

$$T(f) = \frac{1}{T}W(f)G(f).$$

As labeled in the figure, the respective 3 dB bandwidths of $T(f)$, $W(f)$, and $G(f)$ are defined as B, f_w, and f_o, respectively.

To implement GFSK modulation, $T(f)$ must have a Gaussian shape and its bandwidth, B, must be set in proportion to the data rate, defined as $1/T_d$; this relationship is parameterized by the product BT_d. A low value of BT_d is desirable to obtain a transmitter with good spectral efficiency. If the product value is chosen too low, however, excessive intersymbol interference will result [49]. The optimal setting of BT_d is somewhat application specific, but we again appeal to the DECT specification as a benchmark and assume for the analysis to follow that

$$BT_d = 0.5$$

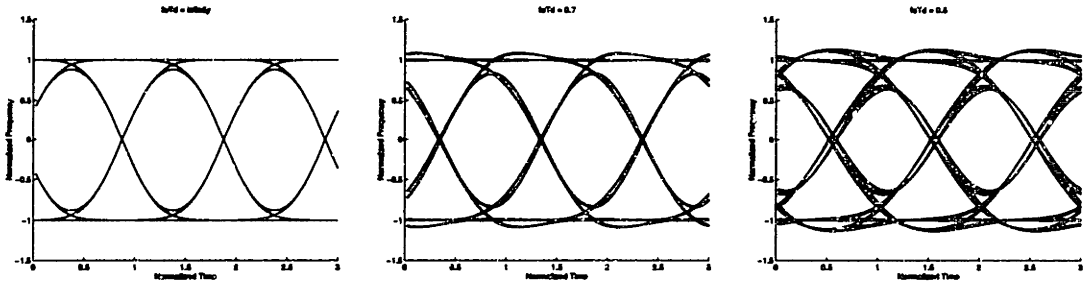
To obtain well controlled modulation characteristics, it is desirable to set $f_w < f_o$ in order to minimize the influence of $G(f)$. In this case, the overall transmit filter is approximated as

$$T(f) \approx \frac{1}{T}W(f).$$

The reason for wanting to minimize the influence of $G(f)$ is that its analog nature, and the constraints placed on it by implementation and noise issues, prevents its response from ideally shaping the modulation data. In contrast, the digital nature of $W(f)$ allows it to realize a symmetric, Gaussian response that is close to ideal.

While a low value of f_w relative to f_o leads to a better controlled transmit filter, it carries the price of a reduced data rate. Therefore, we seek a choice of f_w that is no lower than necessary to achieve the desired transmit filter performance. This choice can be found empirically by assuming a representative transfer function for $G(f)$ and plotting the eye diagrams that result for different values of f_o while $W(f)$ is fixed as a Gaussian filter with bandwidth $f_w = 0.5/T_d$. Figure 4.4 depicts the simulated results of such an experiment in which $G(f)$ was chosen, for the sake of simplicity in calculations, to be a third order Butterworth response. (Similar results were obtained for $n = 4$ and $n = 5$, which are not shown for the sake of brevity.) The plots reveal that the level of intersymbol interference increases as f_o is reduced. Based on the figure, an appropriate choice is

$$f_o T_d = 0.7.$$



(a) (b) (c)

Figure 4.4: Normalized Eye Diagrams for various values of f_oT_d: (a) $f_oT_d = \infty$, (b) $f_oT_d = 0.7$, (c) $f_oT_d = 0.5$.

4.2 Data Rate versus PLL order and Σ-Δ Sample Rate

We now compute the relationship between data rate and the PLL parameter space that achieves the noise performance described in Chapter 3.

For clarity, we briefly review assumptions made in that chapter. $G(f)$ is assumed to be a Butterworth response of order n:

$$G(f) = \frac{1}{1 + (jf/f_o)^n},$$

and the spectral density of the noise at the transmitter output due to quantization noise is expressed as

$$S_{\Phi_q}(f) = \left(T\frac{(2\pi)^2}{12}\left(2\sin(\pi fT)\right)^{2(n-1)}\right)|G(f)|^2, \tag{4.2}$$

where T is the Σ-Δ sample period, and a MASH structure [47] of order n is assumed for the modulator. $G(f)$ is chosen as Butterworth response for the sake of simplicity in calculations; other responses could certainly be implemented. Note that the order of the MASH Σ-Δ is assumed to be the same as the order of $G(f)$ so that the rolloff characteristics of Equation 4.2 and the VCO noise are matched at high frequencies (-20 dB/dec).

Figure 4.5 displays the resulting parameters at different data rates; these values were calculated from Figure 3.4 in chapter 3 under the assumption that f_oT_d equals 0.7. (The parameter space in Figure 3.4 was computed by setting Equation 4.2 to -136 dBc/Hz at 5 MHz; this specification was chosen to achieve less than -131 dBc/Hz at 5 MHz offset after adding in VCO phase noise.)

The figure reveals that the achievement of high data rates and low noise must come at the cost of high power dissipation and complexity when attempting direct

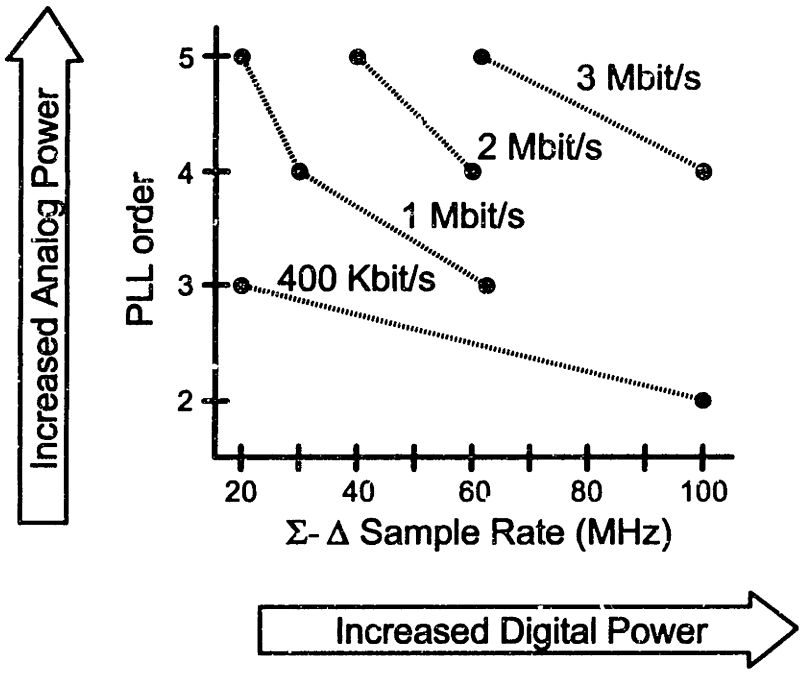


Figure 4.5: Achievable data rates vs. PLL order and Σ-Δ sample rate when $S_{\Phi_{in,q}}(f)$ is -136 dBc/Hz at $f = 5$ MHz.

modulation of the synthesizer. In particular, the power consumed by the digital circuitry is increased at a high Σ-Δ sample rate due to the increased clock rate of the Σ-Δ modulator and the digital FIR filter, $W(f)$. The power consumed by the analog section is increased for high values of PLL order since additional poles and zeros must be implemented. This issue is aggravated by the need to set these additional time constants with high accuracy in order to avoid stability problems in the PLL. If tuning circuits are used to achieve such accuracy [48], spurious noise problems could also be an issue.

4.3 Summary

This chapter explored issues associated with direct modulation of a fractional-N synthesizer. Analysis was performed under the constraint that the modulation bandwidth lie within the bandwidth of the PLL. It was shown that the required parameter space of the PLL that allows high data rates and low noise to be achieved is problematic when desiring a low power, low complexity implementation. Specifically, data rates in excess of 1 Mbit/s with phase noise of -136 dBc/Hz due to Σ-Δ noise require a Σ-Δ sample rate of 60 MHz or a PLL order that is greater than three. A high PLL order is undesirable for achieving a simple, lower power implementation of analog circuits in the PLL. A high Σ-Δ sample rate leads to high power consumption in the digital

portion of the synthesizer.

Chapter 5

Proposed Approach

The obstacles of high data rate modulation discussed in Chapter 4 are greatly mitigated if the modulation bandwidth is allowed to exceed that of the PLL. In this case, the bandwidth of $G(f)$ can be set sufficiently low that an excessively high PLL order or Σ-Δ sample rate is not necessary to achieve the required noise performance.

Figure 5.1 illustrates the proposed method that achieves this goal. By cascading a compensation filter, $C(f)$, with the digital FIR filter, the transfer function seen by the modulation data can be made flat by setting $C(f) = 1/G(f)$. This new filter is simple to implement in a digital manner — by combining it with the FIR filter, we need only alter the ROM storage values. Since the input to the modified FIR filter is a binary, digital data sequence that is noiseless, the compensation filter does not increase noise levels at its output over the uncompensated filter. Savings in area and power of the ROM can be achieved over the uncompensated method since the number of time samples that need to be stored are dramatically reduced.

The technique allows an increase in the achievable data rate for a given value of f_o by trading dynamic range for bandwidth. To explain, $C(f)$ must increase the high frequency content of the modulation signal to compensate for the attenuation imposed by $G(f)$. This leads to an increase in the modulation signal swing, which consumes dynamic range within internal nodes of the PLL. The maximum achievable increase in data rate is set by the PLL node that imposes the tightest restriction on signal deviation.

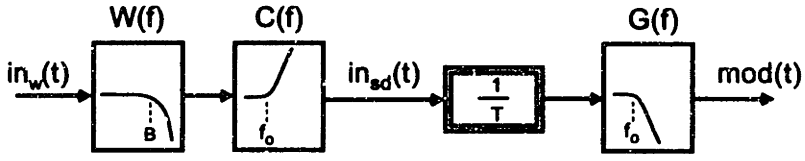


Figure 5.1: Compensation Method

The remainder of this chapter will evaluate the achievable data rates that can be

obtained using the proposed compensation method. We first derive an analytical form for the compensated FIR filter, defined as $W_c(f)$, when GFSK modulation is used. The resulting filter expression is then used to evaluate the dynamic range required of the divider and PFD at different data rates. Computation of the achievable data rates follows. A final section is included to discuss the benefits of the approach with respect to the implementation of the FIR transmit filter.

For the analysis to follow, we will assume an ideal, second order PLL transfer function:

$$G(f) = \frac{1}{1 + \frac{jf}{f_o Q} + \left(\frac{jf}{f_o}\right)^2}; \tag{5.1}$$

$C(f)$ is the inverse of $G(f)$:

$$C(f) = 1 + \frac{jf}{f_o Q} + \left(\frac{jf}{f_o}\right)^2. \tag{5.2}$$

The $n = 2$ case is chosen over higher order PLL topologies to obtain a simple PLL implementation. (The method is less effective at higher values of n due to the increased dynamic range requirements.)

5.1 Derivation of Compensated FIR Filter Under GFSK Modulation

To obtain GFSK modulation, $W(f)$ is chosen as a Gaussian filter whose time-domain description is

$$w(t) = \frac{T}{4}\frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{1}{2}\left(\frac{t}{\sigma}\right)^2}, \quad \sigma = \frac{.833\,T_d}{\pi}. \tag{5.3}$$

The above choice of σ sets BT_d=0.5, and the chosen scale factor of $w(t)$ achieves a modulation index of $h = 0.5$. Implementation of the compensation scheme is accomplished by convolving $w(t)$ with $c(t)$, the time domain version of $C(f)$. Examination of equation 5.2 reveals that convolution by $c(t)$ amounts to adding scaled versions of the first and second derivatives of $w(t)$ to itself. We therefore construct an overall filter, denoted as $w_c(t)$, as

$$w_c(t) = w(t) * c(t) = w(t) + \frac{1}{2\pi f_o Q} w'(t) + \frac{1}{(2\pi f_o)^2} w''(t). \tag{5.4}$$

The required derivatives can be calculated analytically for the Gaussian pulse defined in Equation 5.3, which yields

$$w_c(t) = \left(1 - \frac{1}{2\pi Q f_o \sigma}\left(\frac{t}{\sigma}\right) + \frac{1}{(2\pi f_o \sigma)^2}\left(-1 + \left(\frac{t}{\sigma}\right)^2\right)\right) w(t). \tag{5.5}$$

For analysis to follow, it is convenient to parameterize the above expression in terms of the ratio $1/(f_oT_d)$. This goal is accomplished through substitution of σ with its value given in Equation 5.3

$$w_c(t) = \left(1 - \frac{1}{1.66Qf_oT_d}\left(\frac{t}{\sigma}\right) + \frac{1}{(1.66f_oT_d)^2}\left(-1 + \left(\frac{t}{\sigma}\right)^2\right)\right) w(t). \qquad (5.6)$$

This last expression reveals that the signal swing of $w_c(t)$ increases in proportion to $1/(f_oT_d)^2$ for large values of $1/(f_oT_d)$. (For higher orders of $G(f)$, defined as n, the resulting signal swings are amplified according to $1/(f_oT_d)^n$.) Since $1/(f_oT_d)$ is the ratio of the modulation data rate to the bandwidth of the PLL, we see that high data rates lead to large signal swings of $w_c(t)$. The achievable data rates using compensation are limited by the ability of the PLL to accommodate this increased signal swing.

5.2 Implementation of Compensated FIR Filter

Implementation of the compensated filter can be accomplished with a ROM. To do so, the filter must be modified such that its input is in the form of a binary impulse stream with sample rate $1/T_d$. This modification allows the convolution of the resulting filter with its input data to be performed using a lookup procedure that is implemented by a ROM.

The desired modification is performed by convolving $w_c(t)$ with a rectangular window function defined as

$$\text{rect}(T_d, t) = \begin{cases} 1/T_d, & -\frac{T_d}{2} \le t \le \frac{T_d}{2} \\ 0, & \text{elsewhere.} \end{cases} \qquad (5.7)$$

We denote the resulting filter as $p_c(t)$, where

$$p_c(t) = w_c(t) * \text{rect}(T_d, t). \qquad (5.8)$$

The input data to this filter, defined as $data(t)$, is shown in Figure 5.2; this signal is in the desired form of a binary impulse stream. The compensated FIR filter is, therefore, implemented as samples of $p_c(t)$.

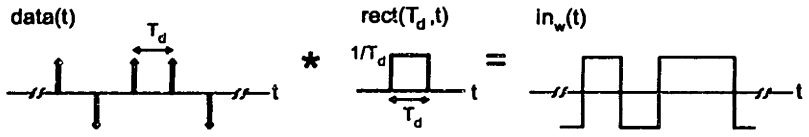


Figure 5.2: The relationship between $in_w(t)$ and $data(t)$.

5.3 Achievable Data Rates

Calculation of the maximum achievable data rate using compensation will now be discussed. Two issues must be considered in this analysis — the available dynamic range within the PLL, and the amount of dynamic range required at a given data rate.

5.3.1 Available Dynamic Range

The determination of available dynamic range requires examination of nodes internal to the PLL. Examination of Figure 5.3 reveals that five nodes are affected by modulation: $E(t)$, $V_{in}(t)$, $Out(t)$, $Div(t)$, and $N[k]$. $G(f)$ attenuates the modulation signal before influencing $F_{out}(t)$, the instantaneous frequency of $Out(t)$. Therefore, the frequency deviation at this node is not increased by the compensation. This implies that the voltage variation on $V_{in}(t)$ is also not affected since $V_{in}(t) = 1/K_v F_{out}(t)$. The signal deviation of the divider output, $Div(t)$, will be increased, but this node does not directly impose a range constraint. The deviation of $N[k]$, however, increases substantially and is limited by the modulus of the divider, which corresponds to the number of output bits of the Σ-Δ. Deviation of the duty cycle of $E(t)$ due to modulation is also increased. Since the duty cycle can vary no more than one cycle, $E(t)$ imposes a strict limit on the modulation signal swing.

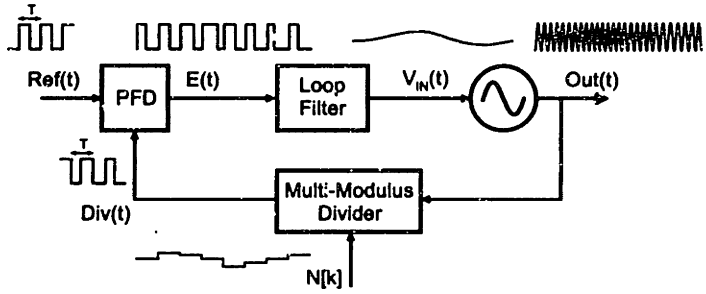


Figure 5.3: Phase/Frequency modulation using divider in PLL.

The dynamic range offered by the divider will be dependent on the implementation used. Here we will assume the multi-modulus divider topology described in Chapter 7, which allows a high dynamic range while achieving low power consumption. The architecture consists of cascaded divide-by-2/3 stages that can 'swallow' a specified number of input cycles to achieve a range of frequency division values. The cycle swallowing method sets limits in the achievable range of the divider as described in Table 5.1. As revealed by the table, the dynamic range of the divider depends on the nominal divide value chosen. The maximum achievable range is achieved with high values of N_{nom} that lie halfway between the minimum and maximum values. For instance, when 5 divide-by-2/3 stages are used, the maximum range is achieved when

$N_{nom} = 47.5$, at which point a range of ± 15.5 is available. If N_{nom} is changed to 40, the range lowers to ± 8. If N_{nom} is set to 90, the range jumps to ± 26.

Number of Stages	Range of Divide Values	Maximum Dynamic Range
4	16-31	15
5	32-63	31
6	64-127	63

Table 5.1
Range of divide values for multi-modulus divider used in prototype.

The dynamic range of $E(t)$ can be no larger than the variation of its duty cycle over one period. Unfortunately, even this range cannot be achieved in practice due to limited dynamics and offset that will occur in the PFD and loop filter implementations.

The impact of limited dynamics on $E(t)$ is illustrated in Figure 5.4, which depicts a charge pump that converts the PFD output into current pulses of amplitude $+I$ and $-I$ that are fed into the loop filter. The average value of current fed into the loop filter in one cycle is intended to be a linear function of the duty cycle; any significant nonlinearities will distort the modulation signal and should be avoided. This goal can be met so long as the modulation signal does not create pulses with width shorter than the transient time associated with current transitions. Pulses that are too short will have a peak amplitude below the desired value of $+I$ or $-I$, and distort the average current produced during the cycle. Therefore, the achievement of acceptable linearity requires a minimum and maximum duty cycle to be enforced which are determined by the transient characteristics of the charge pump. We will assume that the minimum and maximum values are symmetric so that the duty cycle of $E(t)$ has the range of $[\epsilon, 100 - \epsilon]$ percent, where ϵ is set according to the transient time, defined hereafter as t_ϵ.

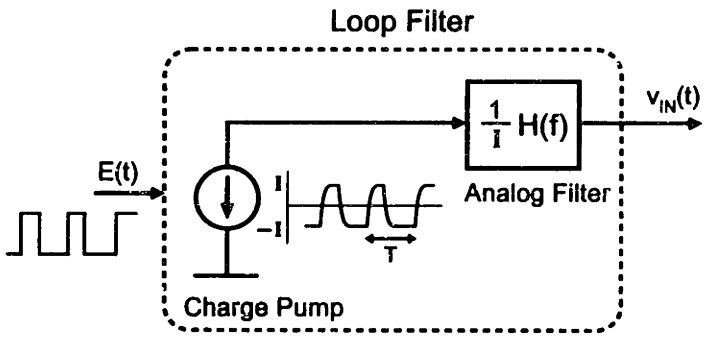


Figure 5.4: Implementation of D/A Function within G(f).

Given the constraints imposed by transients, the highest effective dynamic range for $E(t)$ is achieved when the nominal duty cycle is fifty percent. An offset in $E(t)$ is defined as a shift in the nominal duty cycle from the optimal value, and has the effect of reducing dynamic range. To explain, the modulation signal varies the duty cycle of $E(t)$ an identical amount above and below its nominal value; if the usable range of $E(t)$ is [25, 75] percent, then a nominal duty cycle of 50% yields an effective dynamic range of ±25%. An offset of +10% would yield a nominal duty cycle of 60%, which would reduce the effective range to ±15%.

5.3.2 Dynamic Range Requirements Versus Data Rate

Compensation leads to an increased signal swing at the divider input, $N[k]$, and an increase in the variation of the duty cycle for $E(t)$. To quantify the dynamic requirements of the PLL at different data rates, we examine the linearized model of the fractional-N modulator with compensation as shown in Figure 5.5. The $in_w(t)$ signal is fed into the compensated digital filter, $w_c(t)$, and then sent to the Σ-Δ modulator as $in_{sd}(t)$. The Σ-Δ modulator maps $in_{sd}(t)$ to integer values that are fed into the divider as $\hat{n}(t)$, resulting in added quantization noise, $\hat{q}(t)$. The modulation in the divide value is manifested as a varying duty cycle in $E(t)$, which is sent to the VCO after passing through the loop filter.

Note that in the context of analysis, the placement of the sampling function is arbitrary. By appropriate placement of this function, an estimation of the signal swing of $N[k]$ and duty cycle variation of $E(t)$ can be made using continuous-time analysis techniques. In doing so, it is important to remember that the sampling operation scales by $1/T$ only in the *frequency domain*; in the time domain, the amplitude of the signal at its sample points is preserved. Therefore, the signal deviation of discrete-time signals is approximately the same as the continuous-time signals they are sampled from.

The dynamic range requirements at the divider input, $\hat{n}(t)$, can be determined directly from the resulting signal swings of $in_{sd}(t)$ at different data rates. We note the following relationship:

$$\text{Deviation}\left(\hat{n}(t)\right) = \text{Deviation}\left(in_{sd}(t)\right) + \text{Deviation}\left(\hat{q}(t)\right). \tag{5.9}$$

Deviation of the quantization noise, $\hat{q}(t)$ depends on the order and topology of the Σ-Δ, but not on data rate. For instance, the quantization noise of a second order MASH Σ-Δ structure consumes roughly 4 integer values (i.e., 2 bits), while that of a third order MASH consumes about 8 values (3 bits). Therefore, calculation of the deviation of $\hat{n}(t)$ is performed by simply adding a constant quantization noise level to the deviation of $in_{sd}(t)$.

The deviation of $in_{sd}(t)$ can be calculated numerically by convolving a random, binary, impulse sequence with $p_c(t)$ and then measuring the peak-to-peak amplitude of the resulting sequence. This method was applied as $p_c(t)$ was changed under a

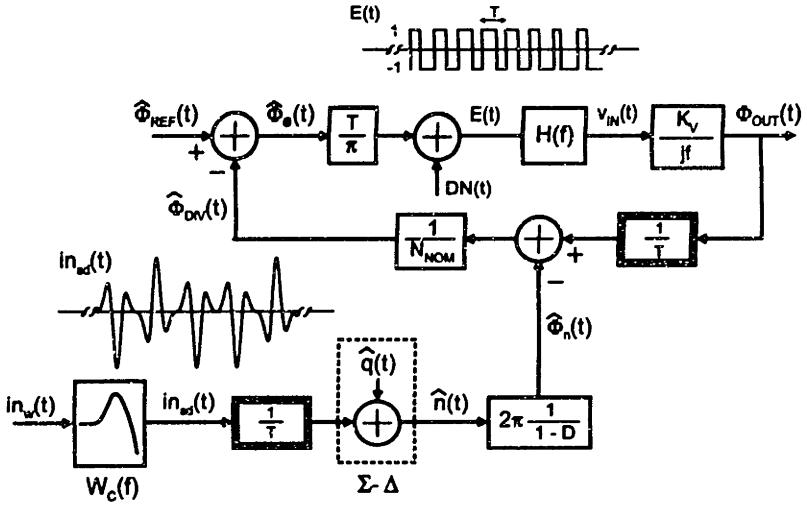


Figure 5.5: Linearized model of fractional-N modulator with compensation.

range of values for $1/(f_o T_d)$; Figure 5.6 displays the results of the numerical analysis under three different values of $1/T$. As observed in the figure, the signal swing of $in_{sd}(t)$ is reduced as $1/T$ is increased. To explain this behavior, note that the nominal output frequency of the PLL, F_{out_c}, is related to nominal divide value, N_{nom}, and the reference frequency, $1/T$, as

$$F_{out_c} = N_{nom}\frac{1}{T}.$$

Deviations of the divide value about N_{nom} are effectively multiplied by $1/T$ before influencing the PLL output frequency. Therefore, to achieve a given frequency deviation at the PLL output, the divide value deviation is reduced when $1/T$ is increased.

Calculation of the duty cycle variation of $E(t)$ is a bit more involved, and will be carried out through determination of the impulse response between the data stream, $in_w(t)$, and the instantaneous phase error, $\hat{\Phi}_e(t)$. A block diagram of this relationship is shown in Figure 5.7. The limitation that the duty cycle variation of $E(t)$ be less than one cycle corresponds to

$$-\pi < \hat{\Phi}_e(t) < \pi. \tag{5.10}$$

Determination of the dynamic range requirements at $E(t)$ can therefore be performed by calculating the signal deviation of $\hat{\Phi}_e(t)$ and comparing it to the above limits.

Figure 5.8 displays a rearranged version of Figure 5.7 that simplifies the analysis to follow. Substitution was made for D at low frequencies relative to $1/T$:

$$D = e^{-j2\pi fT} \approx 1 - j2\pi fT, \quad \text{for } f \ll 1/T.$$

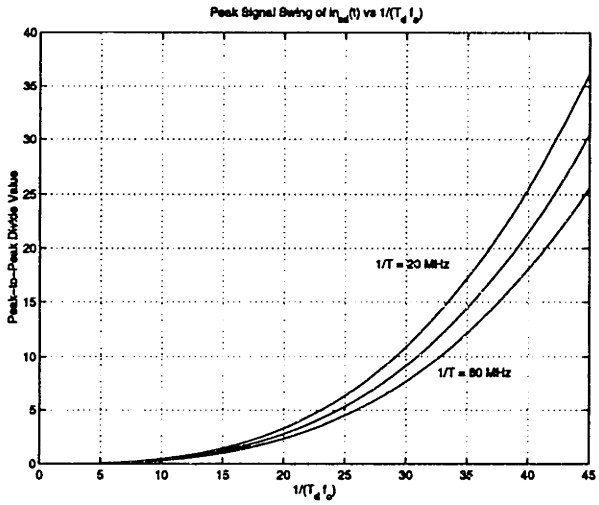


Figure 5.6: Resulting signal deviation of $in_{sd}(t)$ as a function of $1/(f_o T_d)$ for $1/T$ equal to 20, 40, and 80 MHz.

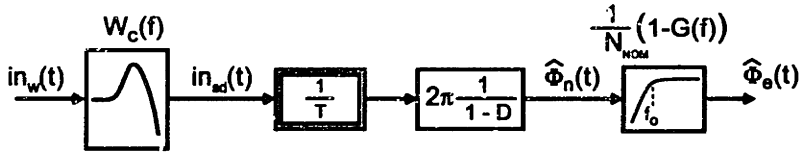


Figure 5.7: Block diagram of transfer function relationship between $in_w(t)$ and $\hat{\Phi}_e(t)$.

Also, the sampling operation was moved to the right portion of the block diagram so that calculations could proceed in a continuous-time framework; we define the continuous-time version of $\hat{\Phi}_e(t)$ as $\Phi_e(t)$.

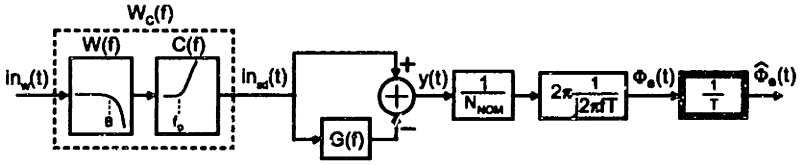


Figure 5.8: Rearranged block diagram of transfer function relationship between $in_w(t)$ and $\hat{\Phi}_e(t)$.

The impulse response from $in_w(t)$ to $\Phi_e(t)$, defined as $z(t)$, will now be computed. Using the expression for $w_c(t)$ given in Equation 5.4 and the fact that $C(f)G(f) = 1$,

we obtain the impulse response from $in_w(t)$ to $y(t)$ as

$$w_c(t) - w(t) = \frac{1}{2\pi f_o Q} w'(t) + \frac{1}{(2\pi f_o)^2} w''(t). \tag{5.11}$$

The overall impulse response is then calculated by recognizing that $1/(j2\pi f)$ corresponds to the integration operation, resulting in

$$z(t) = \frac{2\pi}{N_{nom} T} \left(\frac{1}{2\pi f_o Q} w(t) + \frac{1}{(2\pi f_o)^2} w'(t) \right). \tag{5.12}$$

An analytical form of the above expression can be obtained for $w(t)$ defined in Equation 5.3 as

$$z(t) = \frac{1}{N_{nom} T f_o} \left(\frac{1}{Q} \frac{1}{1.66 f_o T_d} \left(\frac{t}{\sigma} \right) \right) w(t). \tag{5.13}$$

Calculation of the deviation of $\Phi_e(t)$ was performed numerically by convolving a random, binary data sequence with the convolution of rect(T_d, t) and $z(t)$ under a range of values of $1/(f_o T_d)$. The measured deviations were normalized to the constraint given in Equation 5.10 and are displayed in Figure 5.9. Since $\hat{\Phi}_e(t)$ consists of samples of $\Phi_e(t)$, the deviation of $\hat{\Phi}_e(t)$ is approximately the same as that calculated for $\Phi_e(t)$ in Figure 5.9. It is important to note that, unlike the case for $N[k]$, the deviation of $\Phi_e(t)$ is *independent of the value of* $1/T$.

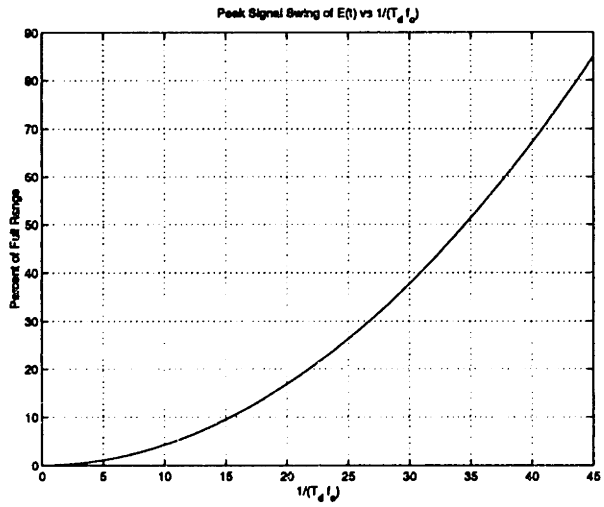


Figure 5.9: Percent deviation of $\Phi_e(t)$ versus $1/(f_o T_d)$. (100 % deviation corresponds to a peak-to-peak deviation of $\Phi_e(t)$ that is 2π.)

5.3.3 Achievable Data Rates versus n and $1/T$

Calculation of the achievable data rate using compensation is now computed by comparing the signal deviations required for different values of $1/(T_d f_o)$ to the dynamic range available to $E(t)$ and $N[k]$. This analysis is implementation dependent and requires a few assumptions to be made.

We will assume the parameter values shown in Table 5.2 for three different values of $1/T$. The choice of $t_\epsilon = 5$ ns was made for pedagogical reasons — 5 ns is large enough to show the effect of t_ϵ on the dynamic range of $E(t)$ with increasing $1/T$, and small enough to allow the $1/T = 80$ MHz case. The value of t_ϵ in the actual prototype was not explicitly computed, but is inferred to be on the order of 5 ns since the maximum data rate it supports (2.85 Mbit/s) is close to the value we calculate here (3.4 Mbit/s). The offset value for $E(t)$ was chosen as 0% and N_{nom} was chosen to maximize the effective divider range for each value of $1/T$ through appropriate selection of the carrier frequency. In practice, a range of values for N_{nom} must be considered since the carrier frequency varies according to which transmit channel is selected.

	$1/T = 20$ MHz	$1/T = 40$ MHz	$1/T = 80$ MHz
Transient Time, t_ϵ	5 ns	5 ns	5 ns
Offset	0 %	0 %	0 %
N_{nom}	95.5	47.5	23.5
Carrier Frequency	1.91 GHz	1.9 GHz	1.88 GHz

Table 5.2
Parameter values for evaluation of achievable data rates using compensation.

Table 5.3 displays the achievable data rates versus $1/T$ when n is constrained to be two; note that the values of 'Maximum f_o' listed in the table are derived by inspection of Figure 3.4. Under the assumed conditions, *each case was limited in range by* $E(t)$, whose effective range was computed as $(T - 2t_\epsilon)/T$. The results reveal that data rate increases very little with high values of $1/T$ due to the reduction in dynamic range that occurs at nodes $E(t)$ and $\hat{N}(t)$.

Comparison of Table 5.3 to Figure 4.5, as illustrated in Figure 5.10, demonstrates that the compensation method allows higher data rates to be achieved for lower values of n and $1/T$. To obtain data rates above 1 Mbit/s, the uncompensated approach requires $G(f)$ to be at least fourth order or $1/T$ to be at least 60 MHz. By using compensation, data rates on the order of 3 Mbit/s can be achieved with n equal to two and $1/T$ equal to 20 MHz. Therefore, the approach appears very promising as a method that achieves high data rates with significant power and complexity savings over methods that confine the modulation data to the bandwidth of $G(f)$.

	$1/T = 20$ MHz	$1/T = 40$ MHz	$1/T = 80$ MHz
Effective Range of $E(t)$	80 %	60 %	20 %
Effective Range of $\hat{N}(t)$	63	31	15
Maximum $1/(f_o T_d)$	43	37	22
Maximum f_o	80 kHz	130 kHz	223 kHz
Maximum Data Rate	3.4 Mbit/s	4.8 Mbit/s	4.9 Mbit/s

Table 5.3
Achievable data rates with compensation.

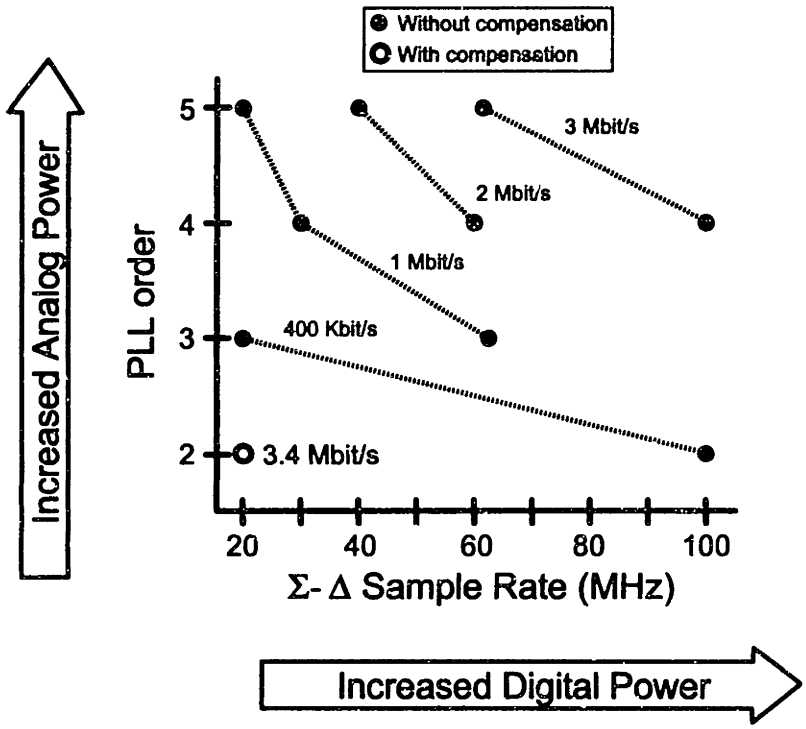


Figure 5.10: Comparison of achievable data rates with and without compensation vs. PLL order and Σ-Δ sample rate.

5.3.4 Simulated Signals at 3.33 Mbit/s

It is useful to visualize the resulting PLL signals under modulation with the proposed compensation method. Figure 5.11 displays the results of a C simulation of a modulated, type II, second order PLL with reference frequency equal to 20 MHz, a cutoff frequency of 84 kHz, and an input data rate of 3.33 Mbit/s; a block diagram of this system is shown in Chapter 10 as Figure 10.3. The resulting range of divide values, 25, is close to that predicted by Figure 5.6 with $1/(f_o T_d) = 40$. A subtle point to this comparison is the fact that the predicted divide range must be multiplied by the ratio

f_z/f_{cp} as explained in the following chapter, and quantization noise added which is produced by the second order Σ-Δ. In the simulation, $f_z/f_{cp} = 0.818$, and the Σ-Δ quantization noise consumes 4 levels.

Figure 5.12 displays signals from the same simulation but a smaller time scale than those shown in Figure 5.11. Note that the simulated duty cycle variation is close to that predicted by Figure 5.9 after it has been scaled by $f_z/f_{cp} = 0.818$. Specifically, the predicted range is 0.818(67) = 55%; the minimum pulse width is therefore 22.5%.

5.4 ROM Power Savings

Given the fact that compensation has been shown to allow power savings in the PLL by reducing n and $1/T$ for high data rates, it is natural to question if an increase in power is required to perform the digital signal processing (DSP) that implements the filtering required in this approach. Fortunately, the method potentially *decreases* the amount of power required in the DSP section over the noncompensated approach, as will now be explained.

The complexity and power required in implementing the ROM filtering method depends on the required storage bits needed in the ROM, and the speed at which those bits need to be accessed. Using an uncompensated approach, Figure 4.5 shows that a relatively high value of $1/T$ is required to achieve high data rates. $1/T$ corresponds to the speed at which the ROM must be run, and the ratio of $1/T$ to the data rate, $1/T_d$, corresponds to the number of samples must be stored in the ROM. Therefore, high values of $1/T$ with relation to $1/T_d$, lead to high levels of power usage in the ROM.

By using compensation, $1/T$ is lowered in an absolute manner and relative to the data rate, $1/T_d$. The compensated FIR filter, $p_c(t)$, will be very close in length to its uncompensated counterpart. Therefore, provided that the number of bits per sample required in the ROM does not increase substantially with compensation, this method will yield power savings in the ROM implementation over the noncompensated approach.

5.5 Summary

This chapter presented a compensation approach that allows the data bandwidth to greatly exceed that of the PLL. It was shown that the cost of this method is an increased dynamic range requirement on the divider and PFD components. The required range was quantified for each of these components, and is was shown that the PFD presents the bottleneck to achieving high data rates. Assuming a well designed charge pump, the maximum data rate was determined to be on the order of 3.3 Mbit/s.

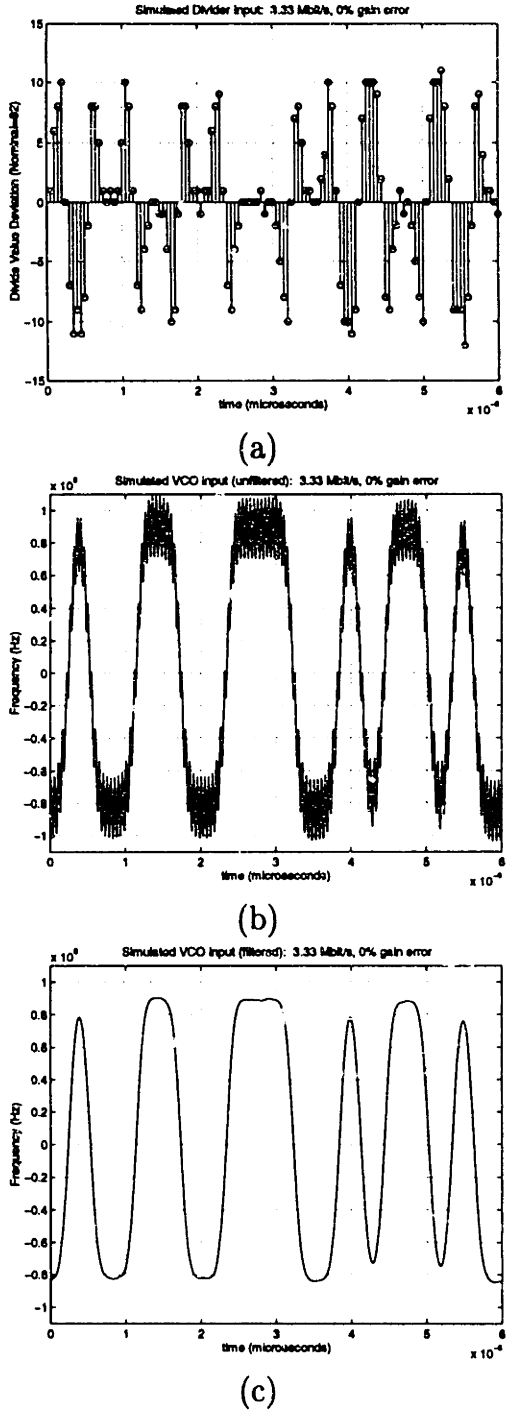


Figure 5.11: Simulated signals within PLL at 3.33 Mbit/s data rate when using compensation: (a) divider input deviation, (b) VCO input, (c) VCO input after being filtered with a 7 MHz Hamming filter.

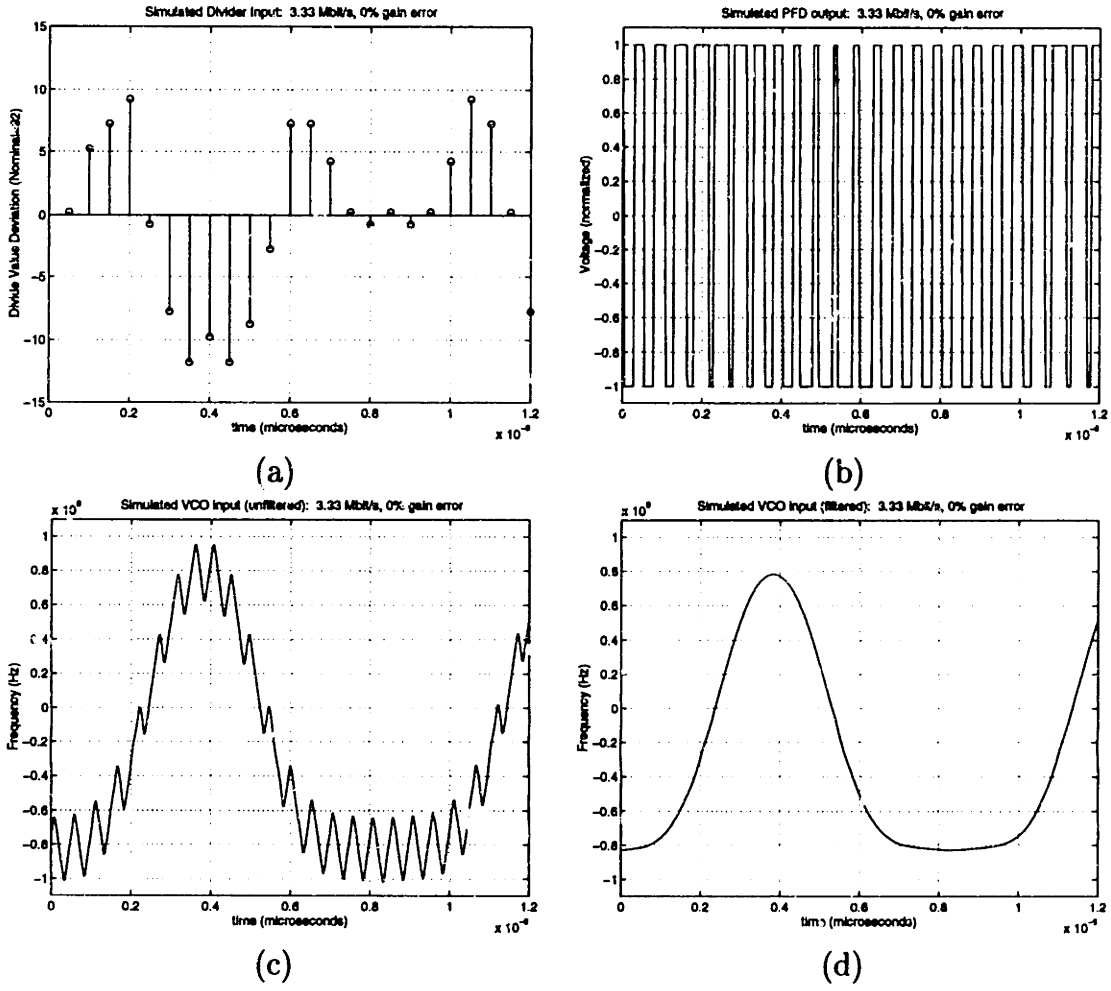


Figure 5.12: Simulated signals within PLL at 3.33 Mbit/s data rate when using compensation (reduced time scale): (a) divider input deviation, (b) PFD output, (c) VCO input, (d) VCO input after being filtered with a 7 MHz Hamming filter.

Chapter 6

The Influence of Mismatch

Analysis thus far has assumed ideal, second order PLL dynamics and a perfect match between $G(f)$ and the inverse of $C(f)$. In practice, $G(f)$ will contain parasitic poles and zeros and will be sensitive to process and temperature variations, so that the ideal response can not be achieved. The effect of these nonidealities on the modulated signal will be the focus of this section.

The analysis to follow will make use of the root locus technique to examine closed loop behavior in the PLL. When using this method, it will be convenient to work in the complex S-plane by substituting $s = j2\pi f$ in the PLL model. Figure 6.1 displays the resulting PLL block diagram, where, for clarity, extraneous signals have been removed using the principle of superposition.

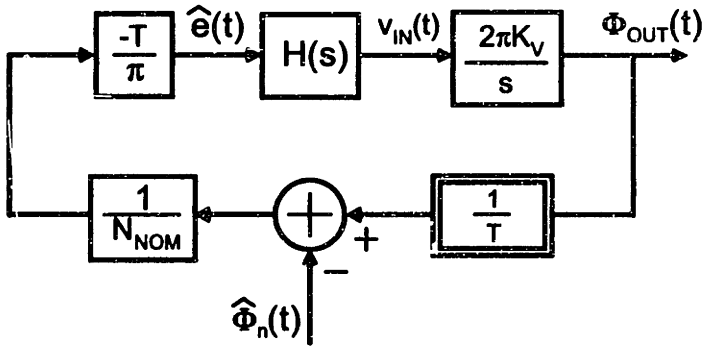


Figure 6.1: Laplace domain PLL model with extraneous signals removed.

6.1 The Choice of Loop Filter

In striving for high dynamic range, the achievement of low offset at $E(t)$ is complicated by the fact that the carrier frequency will often change according to which communication channel is selected. $E(t)$ must steer the nominal value of $V_{in}(t)$, the

input to the VCO, such that the desired carrier frequency is obtained. Therefore, to maintain the nominal duty cycle of $E(t)$ at 50%, either an external signal must be supplied to accommodate the changing DC levels of $V_{in}(t)$, or high DC gain must be placed between $E(t)$ and $V_{in}(t)$. In the interest of minimizing power consumption, the latter choice seems appropriate.

A high DC gain between $E(t)$ and $V_{in}(t)$ can be achieved by placing an integrator in the loop filter, $H(s)$. Since the VCO also acts as an integrator, the PLL becomes a type II feedback system [64]. A zero is required in such systems to achieve stability, and an extra pole included to achieve second order rolloff in $G(f)$ at high frequencies. Therefore, the loop filter takes on the transfer function

$$H(s) = K_l \frac{1 + s/(2\pi f_z)}{s(1 + s/(2\pi f_p))}, \tag{6.1}$$

where $f_z < f_p$ to allow stability to be achieved.

6.2 Resulting Closed Loop Behavior

The root locus method is a convenient analysis tool for studying the influence of the loop filter on the closed loop behavior of the PLL. This approach generates the 'locus' of closed loop pole locations resulting from an open loop transfer function as its gain is varied. For the analysis to follow, the closed loop zeros correspond to the open loop zeros and are included on the root locus diagram.

To compute the locus of PLL poles, its open loop transfer function is obtained with the aid of Figure 6.1 and Equation 6.1 as

$$\frac{2K_v K_l}{N_{nom}} \left(\frac{1 + s/(2\pi f_z)}{s^2(1 + s/(2\pi f_p))} \right).$$

The left term in the above expression, $2K_v K_l / N_{nom}$, is defined to be the open loop gain. The loop filter pole and zero are chosen as

$$f_p \approx \sqrt{2} f_o, \quad f_z = f_p/11 \tag{6.2}$$

for reasons described below.

The resulting root locus is shown in Figure 6.2, which reveals that the closed loop system has three poles and one zero. By proper choice of the loop gain, the poles consist of a complex-conjugate pair with magnitude f_o, and a real-valued pole, f_{cp}. Setting $Q = 0.707$ leads to equal real and imaginary parts for the complex pole pair, where the real part is approximately equal to half of f_p, so that $f_p = \sqrt{2} f_o$. By choosing $f_z \ll f_p$, the zero location has only a small effect on the position of the complex poles.

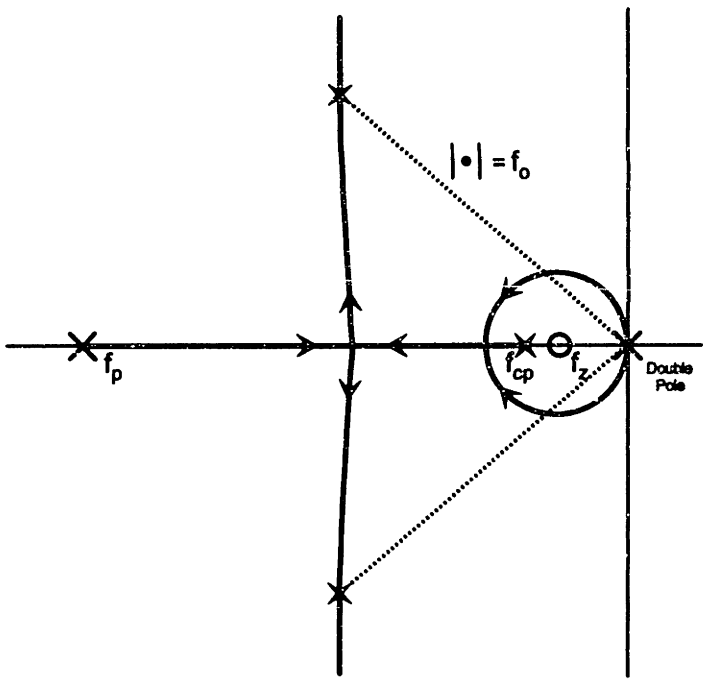


Figure 6.2: Root locus of PLL transfer function.

The pole/zero information provided by the root locus can be used to construct the Fourier domain expression of the closed loop dynamics as

$$G(f) = \frac{1 + jf/f_z}{1 + jf/f_{cp}} \left(\frac{1}{1 + \frac{jf}{f_o Q} + \left(\frac{jf}{f_o}\right)^2} \cdot \right) \tag{6.3}$$

The DC gain of the above expression is verified to be correct by observing $G(f) \longrightarrow 1$ as $f \longrightarrow 0$. The closed loop PLL dynamics therefore include a parasitic pole/zero pair, f_{cp} and f_z, in which f_z is slightly smaller than f_{cp}, and both f_z and f_{cp} are much less than f_o.

6.3 Effect on Compensation

Ideally, $C(f)$ should be set equal to the inverse of $G(f)$. However, inclusion of the parasitic pole/zero pair found in Equation 6.3 will greatly complicate the implementation of this filter. An IIR implementation of $C(f)$ would require recursive computation, so that multipliers and adders would be needed in addition to a ROM to perform the necessary filtering. An FIR approximation of the parasitic response allows a ROM only solution. However, the ROM resulting from this approach would be orders of magnitude larger than if the parasitic pole/zero pair were ignored since $f_{cp} \ll f_o$.

In light of the goal to achieve low power consumption, the additional complexity required in each of the above approaches is highly undesirable.

A better approach is to simply allow a mismatch between $C(f)$ and the inverse of $G(f)$ by ignoring the parasitic pole/zero pair when forming the compensation filter, so that

$$C(f) = 1 + \frac{jf}{f_o Q} + \left(\frac{jf}{f_o}\right)^2$$

as formerly assumed. This choice leads to an overall transfer function that is influenced by the parasitic pole/zero pair and, therefore, no longer ideal:

$$T(f) = W(f)C(f)G(f) = \frac{1 + jf/f_z}{1 + jf/f_{cp}} W(f). \tag{6.4}$$

Fortunately, the impact of the undesired dynamics in Equation 6.4 is greatly reduced by two factors. First, the influence of f_{cp} is significantly reduced by its proximity to f_z. Second, the use of compensation allows the data modulation to be set high such that much of its energy resides in frequencies much higher than the location of the parasitic pole/zero pair. To explain these points, Equation 6.4 is rewritten as

$$T(f) = \frac{f_{cp}}{f_z} W(f) + \frac{1 - f_{cp}/f_z}{1 + jf/f_{cp}} W(f). \tag{6.5}$$

To aid intuition, Figure 6.3 depicts the above relationship in both time and frequency domains. The time domain picture reveals that the parasitic pole produces an undesired 'tail' response of long duration that is excited by incoming data. A tail response excited by one data symbol affects future symbols, causing intersymbol interference (ISI) to occur. The frequency domain illustration reveals that the resulting ISI is excited by energy content in the data signal residing at frequencies within the bandwidth of a lowpass filter formed by the parasitic pole. Therefore, the relative influence of the ISI on the data is reduced as the ratio of B to f_{cp} is increased. The ISI influence is also lowered according to the proximity of f_{cp} to f_z since the magnitude of the lowpass is equal to $1 - f_{cp}/f_z$. If the ISI is sufficiently small such that it can be ignored, the resulting transmit filter is approximated as

$$T(f) = \frac{f_{cp}}{f_z} W(f), \tag{6.6}$$

which reveals that a gain error occurs that is also reduced according the proximity of f_{cp} to f_z.

Equation 6.6 expresses the fact that the parasitic pole/zero pair in Equation 6.3 scales the effective gain of $G(f)$ by the factor f_{cp}/f_z. This gain change must be considered when designing $W(f)$ and when evaluating the noise performance of the transmitter. Specifically, $w(t)$ should be set to

$$w(t) = \left(\frac{f_z}{f_{cp}}\right) \frac{T}{4} \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{1}{2}\left(\frac{t}{\sigma}\right)^2}, \quad \sigma = \frac{.833\, T_d}{\pi}. \tag{6.7}$$

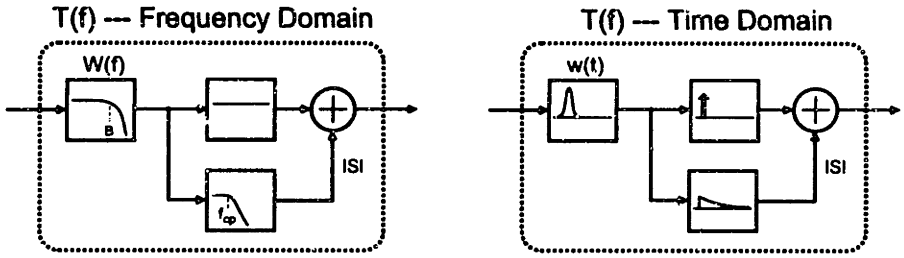


Figure 6.3: Intersymbol interference due to parasitic pole/zero.

rather than the expression in Equation 5.3. As for noise performance, the gain change of $G(f)$ mildly affects the derivation in Chapter 3 of the parameter space f_o, $1/T$, and n that achieves $S_{\Phi_{tn,q}}(f)$ = -136 dBc/Hz at f = 5 MHz. Specifically, $S_{\Phi_{tn,q}}(f)$ must be multiplied by $|f_{cp}/f_z|^2$, which leads to a slightly higher noise level than -136 dBc/Hz at the computed parameter values. The increase in noise will be quantified in Chapter 10 for the parameters values chosen for the prototype.

6.4 Additional Sources of Mismatch

In practice, $G(f)$ will be affected by process and temperature variations that create further mismatch between it and the inverse of $C(f)$. The location of its complex pole pair is most sensitive to two PLL system parameters — the open loop gain, $2K_vK_l/N_{nom}$, and the loop filter pole, f_p. Figure 6.4 illustrates the effect of variations in these parameters on the closed loop poles. Changes in f_p shift the complex poles horizontally, and changes in open loop gain shift them vertically.

The consequences of mismatch between $G(f)$ and $1/C(f)$ are similar to those just discussed for type II implementation of the PLL. Essentially, parasitic pole/zero pairs are added to the transmit filter response, which cause intersymbol interference and modulation deviation error. These undesired parasitics will be located close to f_o, which is at a much higher frequency than occupied by the pole/zero pair, f_{cp} and f_z. To mitigate the influence of ISI, it is desirable to set the ratio B/f_o to be large. In addition, some method must be used to achieve reasonable accuracy of f_p and the open loop gain despite temperature and process variations.

6.5 Minimization of Mismatch

In seeking a means of controlling f_p and open loop gain, it is important to first observe the factors that influence them. The open loop gain is determined by several PLL components, as evidenced by its formulation as $2K_vK_l/N_{nom}$. However, f_p is influenced only by the setting of an RC time constant within the loop filter. Given

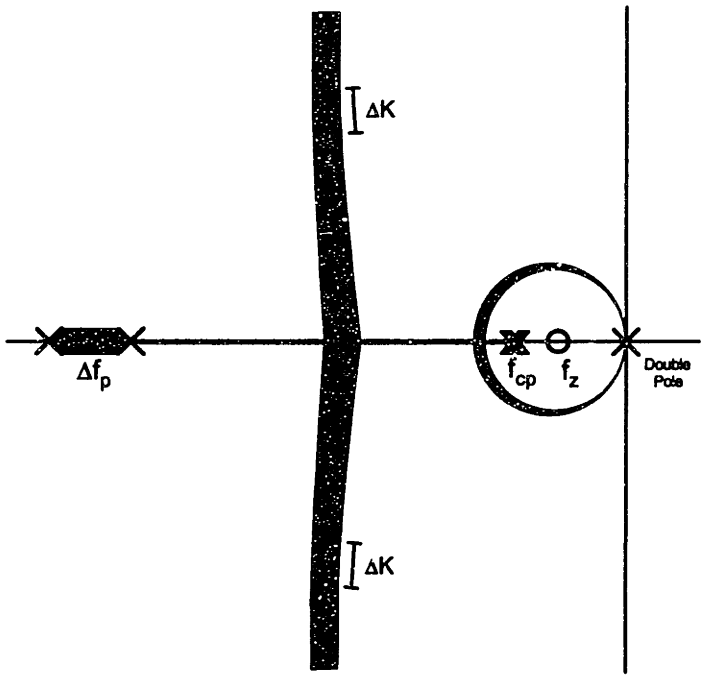


Figure 6.4: Root locus of PLL transfer function.

these facts, a strategy is now presented.

It is well known that accurate RC time constants can be realized through the use of switched-capacitor techniques [65]. Figure 6.5 illustrates the application of this method to produce a parallel RC combination that can be placed at the output of the charge pump. The time constant formed is completely controlled by a ratio of capacitors and a clock frequency which can both be accurately set in modern integrated circuits.

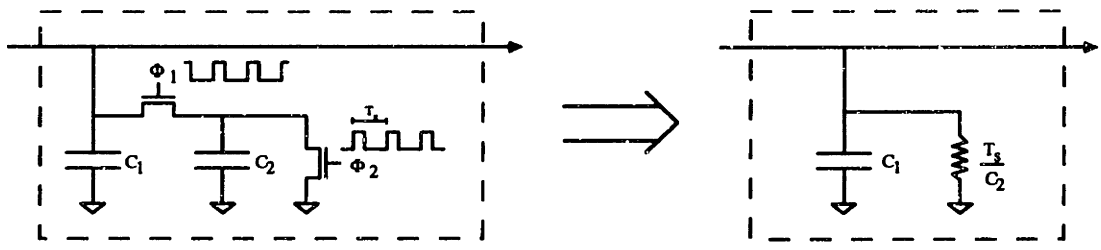


Figure 6.5: Accurate setting of f_p using a switched capacitor technique

A method for correctly adjusting the gain parameter was not pursued as part of this thesis work, and is a subject of future research. If this architecture were applied to the DECT standard, the tolerance required on this parameter would be ±10%. It is believed that similar tuning techniques to those used with continuous-time filters [48] could be used to achieve this accuracy. Another possibility is to place

additional complexity in the receiver, and have it tune the transmitter based on its received waveforms. A final option is to use a ROM to store factory calibrated gains for different carrier frequency settings. (The VCO gain changes with its nominal frequency setting.) Success of this approach depends on having a VCO whose gain does not vary by more than $\pm 10\%$ over the lifetime of the product.

6.6 Summary

This chapter discussed the impact of mismatch between the PLL dynamics, $G(f)$, and compensation filter, $C(f)$. The primary effects of such mismatch were shown to be ISI and modulation deviation error. Minimization of the mismatch is achieved by using a switched capacitor network to set f_p, and setting the open loop gain through appropriate means.

Chapter 7

Divider

We now describe the multi-modulus divider architecture used in the prototype. The topology supports a large, contiguous-range of divide values with speed and power performance comparable to the popular dual-modulus architecture.

We begin by providing an architectural overview of the divider. The basic operation of the divider is explained, along with a phase shifting technique that minimizes the number of components operating at high frequencies. The circuit implementation of the divider is then discussed in detail.

7.1 Architectural Approach

To achieve a low power design, it is desirable to use an asynchronous divider structure to minimize the amount of circuitry operating at high frequencies. The dual-modulus approach achieves such a structure, and has been successfully used in many high speed, low power designs [45, 51–53, 66]. (A specific example is a 1.5 GHz 64/65, 128/129 bipolar design from Motorola that consumes less than 2 mW [66].)

The multi-modulus divider presented in this chapter is an extension of the popular dual-modulus topology; the ripple counter contained in the dual-modulus design is replaced with cascaded divide-by-2/3 sections [50]. The design achieves further power reduction by applying a phase shifting technique [53] to the first stage of the divider.

This section provides further details of the multi-modulus divider architecture used in the prototype. We begin with a general description of the dual-modulus approach, and then explain the extension of this method to multi-modulus structures. Finally, architectural details are provided of the divide-by-2/3 sections used in the divider design. In particular, the merits are described of using the phase shifting, as opposed to the common 'gated approach', technique for pulse swallowing.

7.1.1 The Dual-Modulus Divider

A dual modulus N/M divider, or prescaler, performs frequency division to produce an output with a cycle time that equals either N or M cycles of its input. Most modern designs of this component have an architecture that consists of a 'pulse swallowing' state machine at the input followed by an asynchronous ripple counter [45, 51–53]. The advantage of this topology is that only a small section of the overall divider (i.e., the pulse swallowing state machine) operates at the high frequency of the input; the stages that follow operate at progressively lower frequencies.

Figure 7.1 illustrates a dual-modulus 8/9 prescaler as an example of this approach. The structure consists of a divide-by-2/3 state machine followed by an asynchronous divide-by-4 section. The core of the 2/3 state machine is a divide-by-2 circuit that 'swallows' an input cycle when a binary control signal, *CON*, is asserted. The number of input cycles swallowed per output cycle is limited to be either zero or one by the control qualifier block. As illustrated by the figure, the 8/9 prescaler produces an output consisting of 9 input cycles when *CON* is set to 1 in the previous output cycle. When *CON* is set to 0, the input cycle is not swallowed so that the output consists of 8 input cycles.

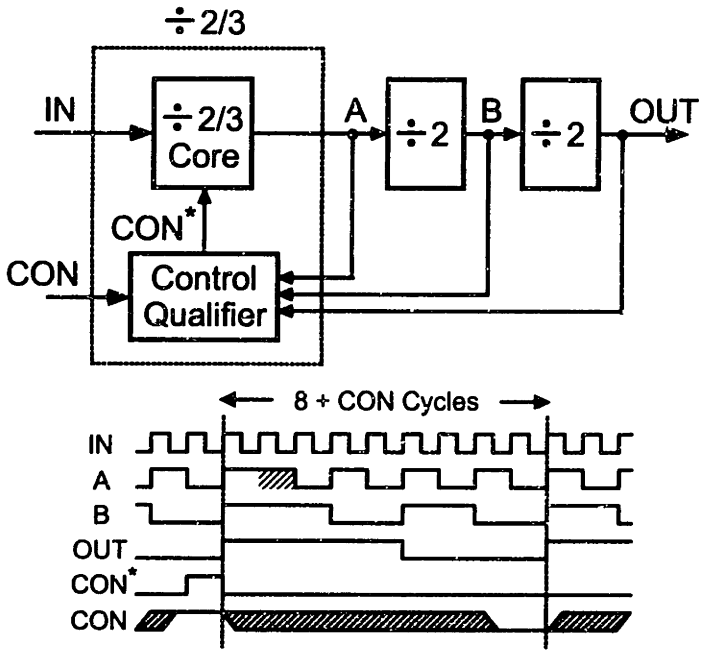


Figure 7.1: An 8/9 dual modulus divider.

Qualification of the control signal is typically performed by gating its value to the 2/3 state machine core when the output of each divider section is zero. As illustrated in Figure 7.1, CON^* becomes asserted only when *CON* is asserted and the nodes A,

B, and OUT are all zero. This gating technique has the advantage of being relatively insensitive to the delays in A, B and OUT that result from the asynchronous nature of the divider. Inspection of the figure reveals that the time window of the all-zero state of A, B, and OUT is unaffected if B and OUT are slightly delayed since these signals transition to the low state well before A.

7.1.2 A Multi-Modulus Divider Architecture

The dual-modulus approach can be extended to realize multi-modulus prescalers that are capable of frequency division over a large, contiguous range. To do so, the asynchronous divide-by-2 sections of the dual modulus divider are replaced with divide-by-2/3 state machines [50]. The design increases the range of divide values to include all integers between 2^k and $2^{k+1}-1$, where k is the number of divide stages within the prescaler. By maintaining an asynchronous counting method, the speed and power dissipation remains comparable to the dual modulus approach.

Figure 7.2 illustrates the approach for an 8 modulus prescaler that supports all integer divide values between 8 and 15. Composed of three cascaded divide-by-2/3 blocks, three binary control bits are used to swallow cycles at progressively lower frequencies. As in the dual-modulus case, qualifying logic embedded within each divide-by-2/3 section is used to limit each stage to one cycle skip per period of OUT.

To explain its operation, the figure shows the case in which all 3 of the control signals are asserted so that a divide value of 15 is produced. Generalizing, we see that one, two, or four input cycles are swallowed when CON_0, CON_1, or CON_2 are asserted, respectively. Therefore, the number of swallowed input cycles is binary weighted according to the variable CON, which is defined as

$$CON = \{CON_2 CON_1 CON_0\}.$$

Through appropriate setting of this variable, any integer number of input cycles between 0 and 7 may be swallowed. As an example, selection of $CON = \{101\}$ leads to 5 input cycles being swallowed, and $CON = \{011\}$ leads to 3 input cycles being swallowed. Since the swallowed cycles add to the base division value of the structure, the total number of input cycles per output cycle is computed in this example as $8 + CON_2 2^2 + CON_1 2^1 + CON_0 2^0$.

7.1.3 Divide-by-2/3 Architecture

The divide-by-2/3 structures form the basic building blocks of the multi-modulus divider used in the prototype. These structures may be implemented by augmenting a divide-by-2 circuit with gating or multiplexing logic [53]. This section will outline the advantages of the multiplexing method over the gating method in achieving high speed performance with low power consumption.

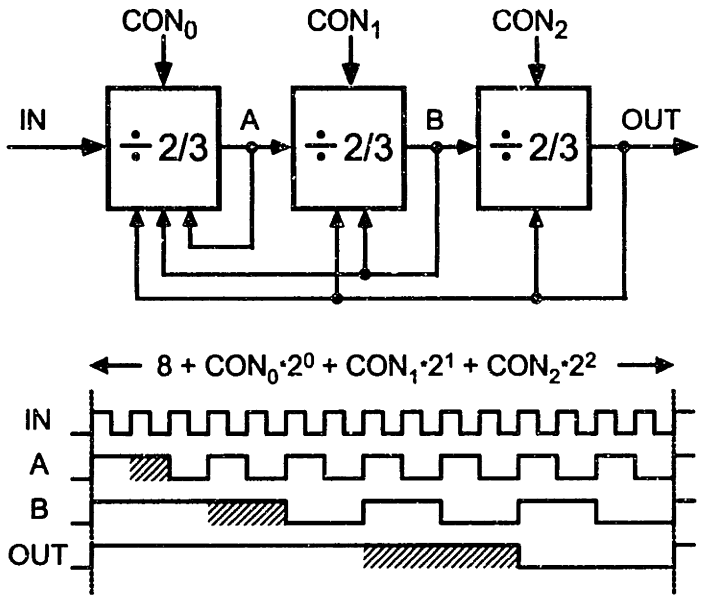


Figure 7.2: An 8 modulus divider.

Figure 7.3 illustrates an efficient divide-by-2 structure known as the Johnson counter [52]. The structure consists of two level-triggered latches that are cascaded within a negative feedback loop. Maximum operating speed of this structure is determined by the propagation delay of the input of each latch to its respective output when the latch is made transparent by the clock. Specifically, the input period, T_{IN}, must satisfy the relation:

$$\frac{T_{IN}}{2} - T_s > \text{delay}_1 = \text{delay}_2,$$

where T_s is defined as the setup time of each latch.

To create a divide-by-2/3 circuit, a common approach is to augment the Johnson counter to swallow cycles by gating the feedback signal into one of its latches. Figure 7.4 provides an example of the gating approach where the setting of CON^* equal to zero leads to the swallowing of a pulse.

A generalized view of this approach is illustrated in Figure 7.5, which lumps the combinational and memory logic required for gating into the Gating Logic block. The function of this block is to extend the assertion of signal A by one input cycle whenever the control signal is asserted. Since A is propagated to the output, this leads to the swallowing of an input cycle.

A few points are in order

1. Proper timing of signal A is typically achieved with latches that are clocked synchronously with the Johnson counter latches, leading to a significant increase

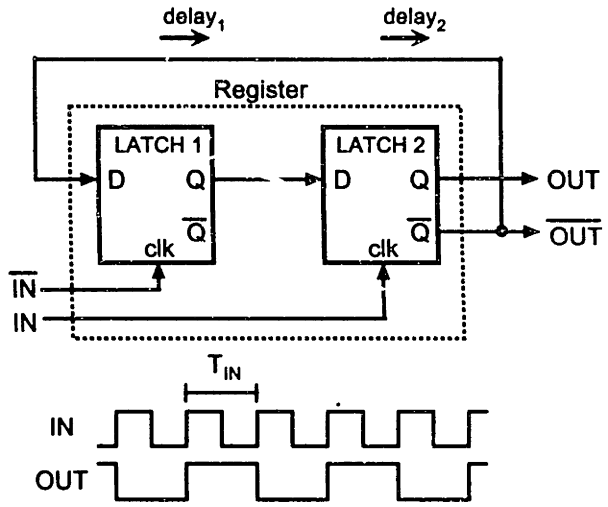


Figure 7.3: A divide-by-2 circuit implemented as a Johnson counter.

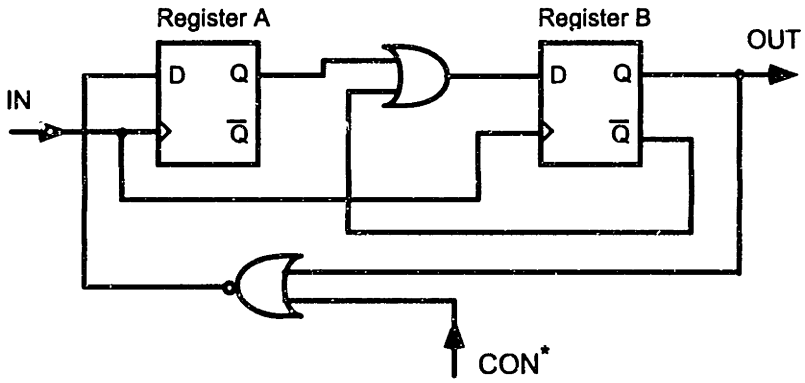


Figure 7.4: Example of divide-by-2/3 implementation using gating logic.

in the number of components operating at the high input frequency over the divide-by-2 structure. This leads to high load capacitance on the high speed input, which requires a larger buffer from the VCO, thus increasing power dissipation.

2. The maximum operating speed of the divide-by-2/3 structure is less than the basic divide-by-2 topology since the gating logic adds to the propagation delay from the output of latch 2 to the input of latch 1. Referring to Figure 7.5, the input period must satisfy the relation:

$$\frac{T_{IN}}{2} - T_s > \text{delay}_2 + \text{delay}_3,$$

which is longer than that of the divide-by-2 circuit.

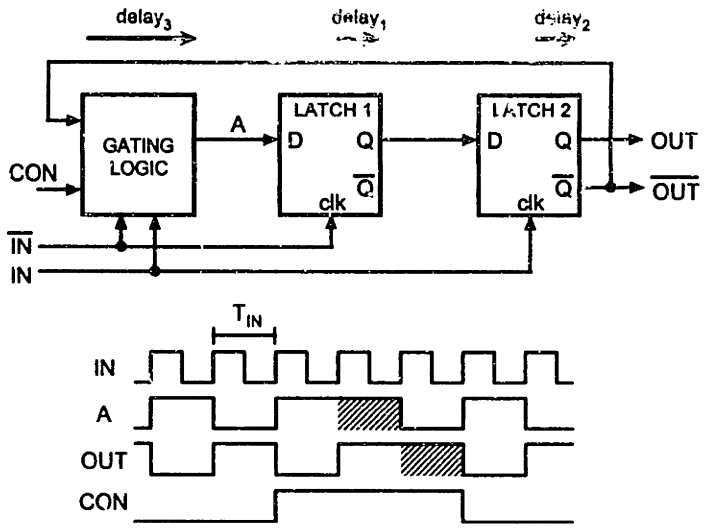


Figure 7.5: A divide-by-2/3 core circuit implemented by gating the feedback in a Johnson counter.

An alternative method of realizing the divide-by-2/3 structure is to multiplex the output of the divide-by-2 circuit. Figure 7.6 illustrates this approach. In this case, the control signal selects either Φ_A or Φ_B from the Johnson counter to produce the output signal. Cycles can then be swallowed by properly shifting from one phase to the other, i.e. Φ_A to Φ_B and vice-versa.

This technique has the following advantages over the gated approach:

1. The operating speed of the structure can be set as high as the divide-by-2 circuit allows since it is not impeded by extra delays

2. The MUX circuitry operates at half the input frequency

3. The capacitive load presented to the input is the same as that of the divide-by-2 structure.

It should be noted that the multiplexed structure requires care in its design to assure that the two phases of its differential input, Φ_A and Φ_B, are close to 180 degrees apart. Otherwise, jitter will occur in the transition times of OUT as it switches between Φ_A and Φ_B. (The time between transitions of OUT will not be a multiple of the input period, T_{IN}, if Φ_A and Φ_B are not 180 degrees apart.)

The operating frequency of the MUX circuitry can be further reduced by applying the phase shifting principle to a divide-by-2 circuit with a 4 phase output. Figure 7.7 illustrates that this type of divider can be cascaded with a standard divide-by-2 structure to produce a divide-by-4/5 circuit. Explaining, one of four phases from the 4 phase divider is directed to the output at any given time, and input cycles are

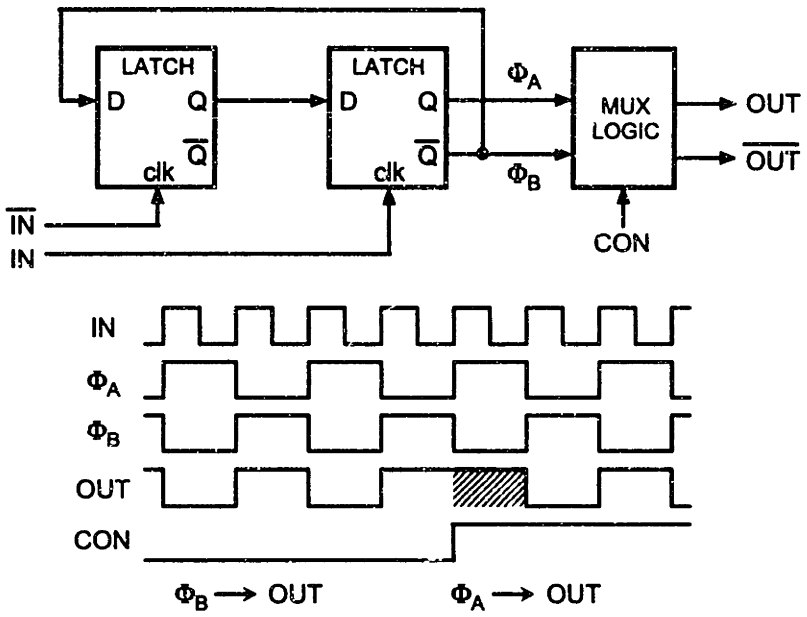


Figure 7.6: A divide-by-2/3 core circuit implemented by multiplexing the divided output of a Johnson counter.

swallowed by shifting the output from one phase to another. The figure illustrates a shift from Φ_1 to Φ_2 to swallow one input cycle.

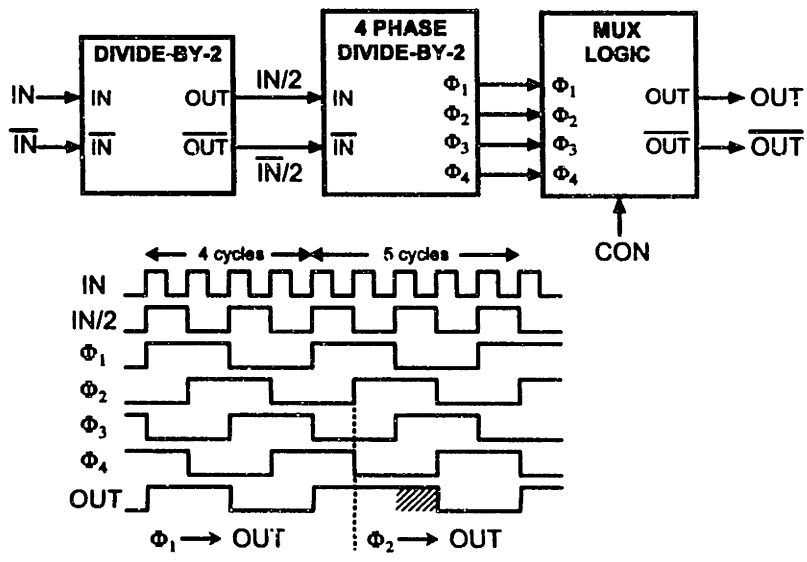


Figure 7.7: A divide-by-4/5 structure implemented by multiplexing a 4 phase divide-by-2 circuit.

The concept illustrated in Figure 7.7 is very useful for implementation of the first divider stage within a dual or multi-modulus divider. Since the operating frequency is reduced at later stages, the first stage presents the strongest challenge in terms of realizing the required speed while maintaining low power consumption. However, to use the divide-by-4/5 stage within a multi-modulus divider, consideration must be given to the fact that its nominal division value is twice that of a divide-by-2/3 structure. A divide structure cascaded after the divide-by-4/5 circuit therefore has half the cycle swallowing resolution than needed to realize a contiguous range of divide values.

Figure 7.8 illustrates the divide-by-4/5/6/7 topology used in the prototype. By following the divide-by-4/5 circuit with at least two divide-by-2/3 sections, the problem of decreased cycle resolution is solved by allowing the divide-by-4/5 circuit to swallow *more than one input cycle* during one cycle of OUT. Division by 4/5/6/7 is accomplished by designing the divide-by-4/5 circuit such that it swallows 0 to 3 input cycles during each cycle of OUT; the figure shows the case for which the first stage accomplishes a divide-by-7 operation by swallowing 3 input cycles. The overall divide range of the topology in Figure 7.8 is 16 through 31, which is the same as would be achieved by cascading four divide-by-2/3 sections.

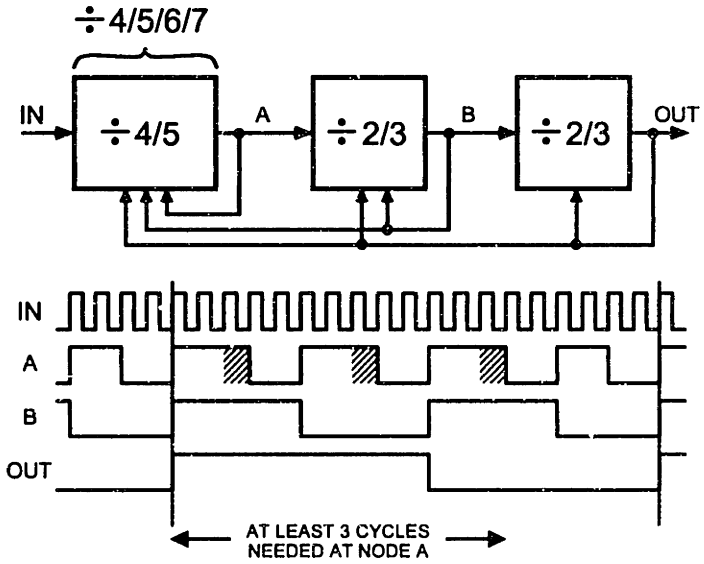


Figure 7.8: Timing diagram of a divide-by-4/5 structure performing a divide-by-7 operation by swallowing 3 input cycles per OUT period.

7.2 Implementation

Figure 7.9 displays the architecture of the 64 modulus divider used in the prototype. The structure has a contiguous divide range of 32 through 63.5 in half steps of its input, $IN/2$. The divide-by-2/2.5/3/3.5 circuit is implemented using a similar structure to that illustrated in Figure 7.7, with the initial divide-by-2 removed. The inclusion of an external divide-by-2 circuit in front of the divider yields integer divide increments ranging from 64 to 127.

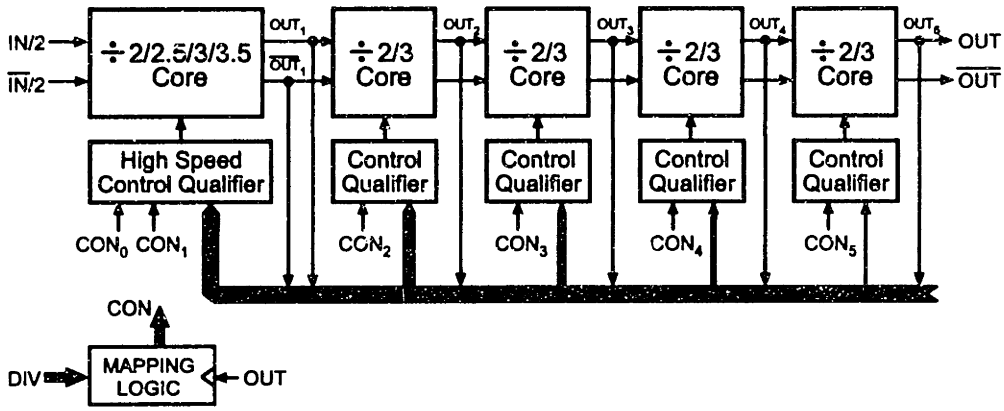


Figure 7.9: A 64 modulus divider architecture.

The circuits to be presented were designed with the priority of achieving a robust design rather than the lowest possible power consumption. Despite this fact, the presented multi-modulus design achieves power dissipation performance that is comparable to dual-modulus divider topologies that have been implemented by other researchers in similar CMOS processes [53].

To achieve a robust design, the overall strategy that guided the choice of the following circuits was to strive for the highest speed possible. To do so, the stacking of devices was avoided in all critical paths, especially the relatively slow PMOS transistors. In addition, the number of cascaded gates was kept to a minimum.

7.2.1 Divide-by-2/2.5/3/3.5 Core Design

Figure 7.10 displays the overall architecture of the divide-by-2/2.5/3/3.5 design. Priority was given to the achievement of high speed operation in the shown blocks since their front end was required to run at speeds approaching 1 GHz.

Four-Phase Divide-by-2 Topology and Input AMP

Figure 7.11 displays a high speed, four-phase, divide-by-2 topology from [67] that is well suited for high speed operation in a CMOS process. The structure is essentially

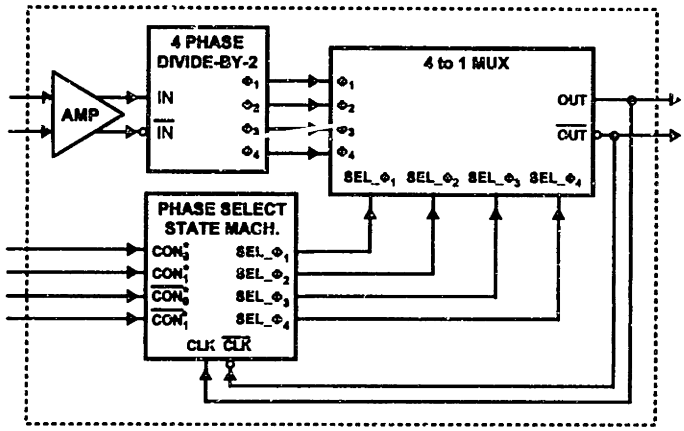


Figure 7.10: Divide-by-2/2.5/3/3.5 architecture.

a Johnson counter that achieves high speed by avoiding the stacking of NMOS or PMOS transistors. The latch operates by using PMOS devices to drive current into its output nodes according to a clock signal, and NMOS devices to selectively discharge the nodes according to signals supplied by the other latch.

Describing its operation, the latch is made non-transparent, meaning that its output nodes have no effect on the other latch, during the time its PMOS devices are turned off by the $IN/2$ signal. In this state, the input signals coming from the other latch are able to discharge their respective nodes without the change immediately propagating back to itself. The speed of the discharge is aided by the fact that the input NMOS devices do not need to 'fight' PMOS current, since the PMOS devices are turned off. When $IN/2$ turns the latch's PMOS devices back on, the resulting current is hampered from charging up one of the nodes by the input NMOS device that is turned on. The two latch nodes are then forced to complementary voltage levels by the positive feedback action that occurs from the cross-coupled NMOS pair. The node with a high voltage level acts to discharge a node in the other latch, and the process continues to produce the Johnson counter action.

The input signals $IN/2$ and $\overline{IN/2}$ are supplied from an off-chip divide-by-2 prescaler having an ECL compatible signal swing (i.e., 300 to 600 mV peak-to-peak). However, the divide-by-2 topology in Figure 7.11 requires input signals at CMOS levels (i.e., close to the supply rails). The amplifier circuit shown in Figure 7.12 was used at each of the 4-phase divider's inputs to supply the necessary amplification.

Briefly describing its operation, the amplifier is essentially a CMOS inverter that has resistive feedback to its input to provide biasing. Transistors M_1 and M_2 form the inverter, and M_3 and M_4 are weaker devices that equalize the inverter input and output in the absence of an input signal. The external input signal is AC coupled to the amplifier using an on-chip poly-poly capacitor, C_1, that is set to roughly ten times the value of the total parasitic capacitance at the inverter's input. Proper sizing of

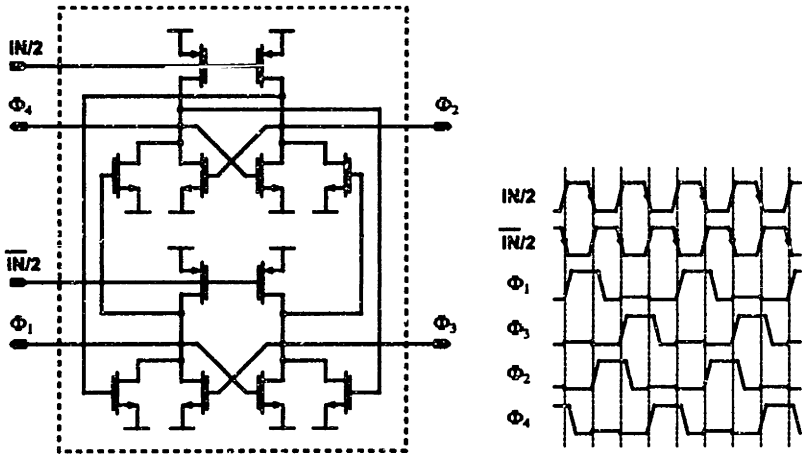


Figure 7.11: A four-phase divide-by-2 circuit.

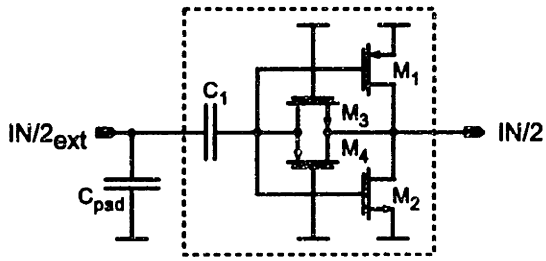


Figure 7.12: High speed ECL to CMOS amplifier.

M_3 and M_4 allows the resulting RC combination formed by M_3, M_4, and C_1 to be made sufficiently large to pass a 900 MHz signal with little attenuation.

The advantages offered by the inverter based amplifier in Figure 7.12 are its simplicity and the large swing it affords. Simplicity in the design helps to reduce power dissipation, and is achieved by using a single stage design that has no additional biasing circuitry. The large swing is the consequence of modulating both the NMOS and PMOS currents. This approach should be compared to class A designs which feed a constant-current into the drain of an NMOS device whose gate forms the amplifier input. The class A structure is impeded from achieving a high output voltage swing due to the fact that the NMOS device enters the triode region at low points in the swing; the finite resistance of the NMOS device in triode region is turned into a non-negligible voltage by the constant current feeding into it. By using the inverter based design, the PMOS current is lowered while the NMOS device is in the triode region. The resulting voltage is lower, thereby yielding a higher swing.

Four to One Multiplexer Topology

The multiplexer design, shown in Figure 7.13, uses gated, pseudo-NMOS buffers to achieve high speed switching between phases. The pseudo-NMOS technique achieves higher speed than attained with CMOS circuits due to the reduced input capacitance at each gate. (The inputs to pseudo-NMOS gates consist only of NMOS devices, whereas the inputs of CMOS gates consist of both NMOS and PMOS devices.) The use of the pseudo-NMOS technique leads to the consumption of static power. However, the operating frequency of the multiplexer is roughly 1 GHz in this application, which leads to a dynamic power consumption (caused by charging and discharging the input capacitance of each gate) that is on the same order as the static power consumption. Since the input capacitance of each pseudo-NMOS gate is roughly half that of its CMOS counterpart, the combined static and dynamic power in the pseudo-NMOS gates should be roughly equal to the dynamic power that would occur in a CMOS implementation.

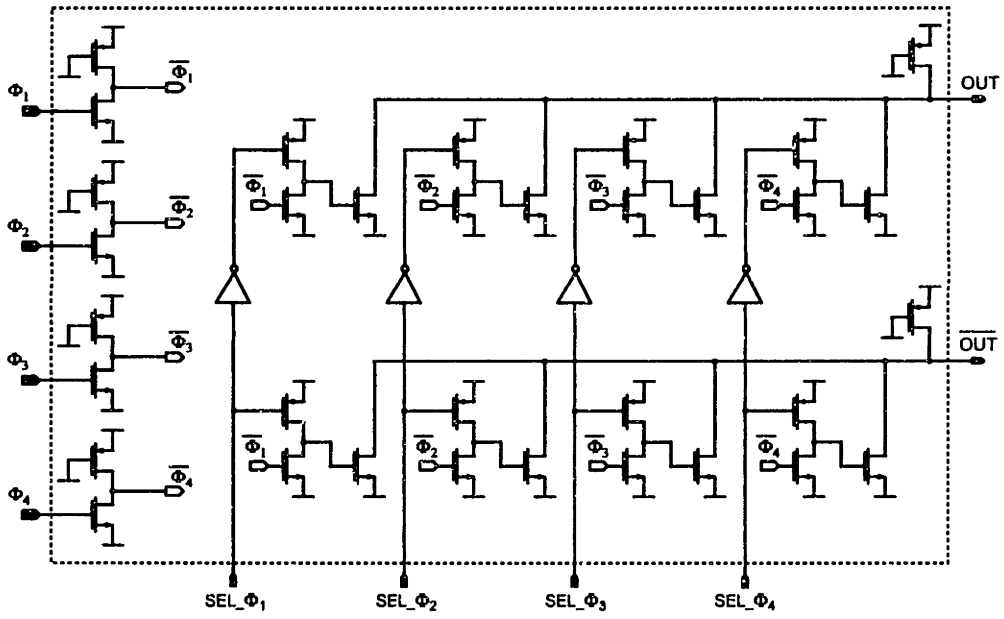


Figure 7.13: Multiplexer topology.

Briefly explaining the operation of the multiplexer, a given phase is gated to the input of a 4-input NOR gate by turning on the PMOS device with its corresponding *SEL_*Φ signal. For instance, when *SEL_*Φ_1 is set high, a buffered version of Φ_1 is passed on to *OUT* and blocked from reaching $\overline{OUT}$.

An advantage of the shown topology is that it provides inverting and noninverting paths to the output that are closely matched in their timing. This property allows the adjoining divide-by-2/3 section to achieve low jitter as it switches between phases

OUT_1 and $\overline{OUT}_1$. In addition, the low skew between the output signals allows their use as a two phase clock for the phase select state machine.

Phase Select State Machine

A state machine is required for control of the select signals on the multiplexer to achieve proper switching between phases when swallowing input cycles. To describe the implementation of this circuit, we first discuss an approach of controlling the order and timing of phase transitions to prevent glitches from occurring in the output. A method of selectively stopping on specific phases is then discussed which provides a means of controlling the number of pulses swallowed during each cycle of the overall divider output.

Figure 7.14 illustrates the timing strategy used to transition between phases. The diagram shows the case in which input cycles are swallowed during three consecutive OUT cycles. As illustrated, the phase transitions are performed as a two step process that is triggered by rising edges of OUT and $\overline{OUT}$. The operation avoids glitches by switching in a phase that is not active during the time that the switching takes place. Referring to the figure, a transition from Φ_1 and Φ_2 to Φ_2 and Φ_3 being directed to OUT is accomplished by switching in Φ_3 on the rising edge of OUT when Φ_1 is active, and switching out Φ_1 on the rising edge of $\overline{OUT}$ when Φ_4 is active.

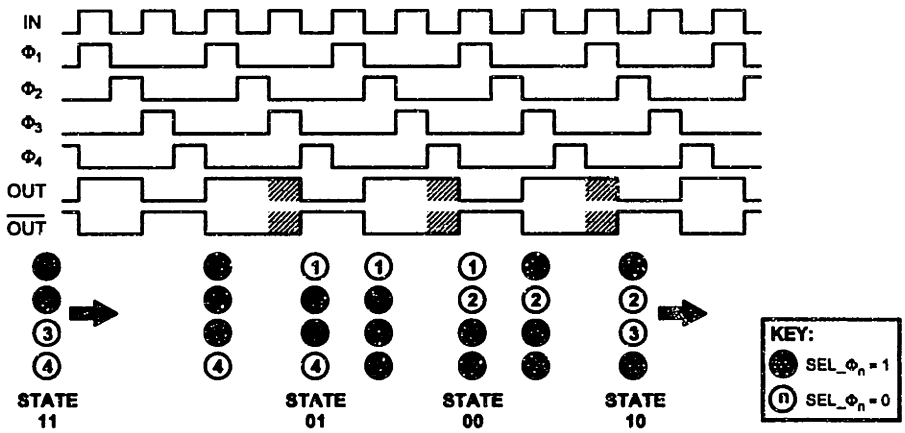


Figure 7.14: Multiplexer control strategy to realize glitch-free phase switching.

The above timing strategy is described in the form of a state transition diagram in Figure 7.15. For convenience, the switch settings are now placed in circular configuration with order indicated by the shown key. The states are separated into two groups — half of the states are labeled with state numbers and the other half are not. The former group represents the core switch configurations that are switched between to achieve cycle swallowing. The latter group is composed of transition states that allow switching between core states in a glitch-free manner.

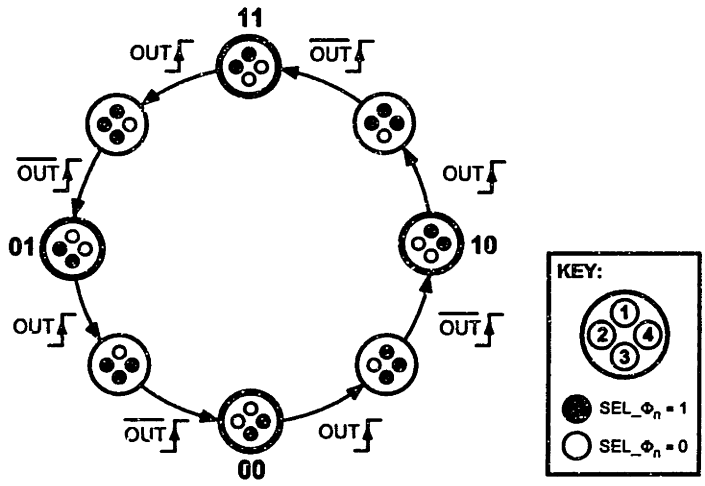


Figure 7.15: State transition diagram to achieve phase switching control strategy.

Figure 7.16 reveals that the desired state transition diagram can be realized in a simple manner by chaining together two registers in a negative feedback configuration. The structure is essentially a divide-by-4 counter whose various phases are tapped off to form the required MUX selection signals. However, registers are required that have the unconventional characteristic of setting both Q and $\overline{Q}$ high during certain falling transitions of $\overline{OUT}$.

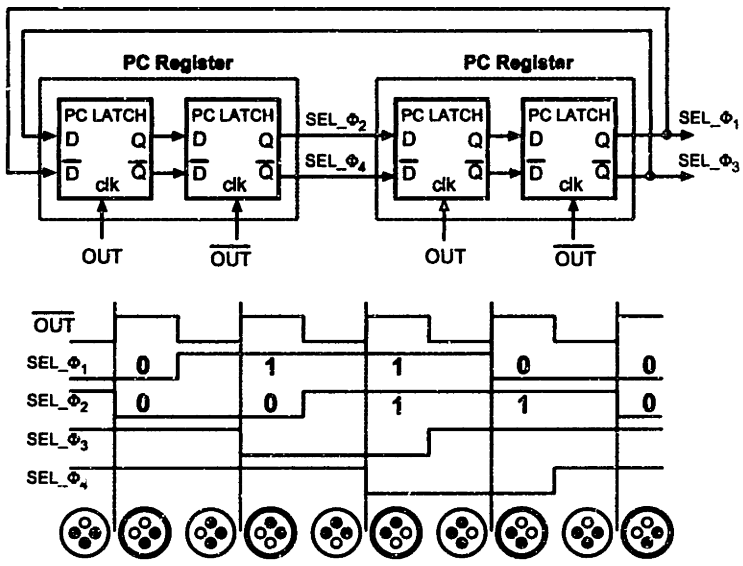


Figure 7.16: An efficient implementation of the phase switching state diagram.

The realization of a register with the required behavior can be obtaining by us-

ing latches with the topology shown in Figure 7.17. Referring to this structure as a PMOS-coupled (PC) latch, its operation is described in the timing diagram shown within the figure. A given latch node, $\overline{Q}$, is set high by bringing D low while CLK is set low. Assuming that Q was already high, this leads to both nodes being high during the time that CLK remains low. On the rising edge of the CLK, the underlying NMOS cross-coupled pair begins to reduce the voltage across both latch nodes. Assuming that D is still low and $\overline{D}$ high, node Q falls in voltage faster than $\overline{Q}$. The positive-feedback action of the cross-coupled NMOS devices amplifies the resulting difference in node voltages to produce complementary outputs. The cross-coupled PMOS devices aid the positive feedback action, and allow the latch to retain a complementary output during times that D and $\overline{D}$ are both set high.

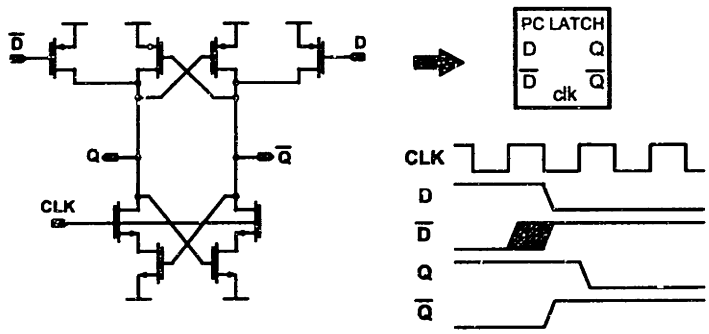


Figure 7.17: Proposed PMOS-coupled latch design.

Aside from realizing the behavior needed to implement the state diagram in Figure 7.16, the PMOS-coupled latch has the advantage of being a fast structure. The stacking of PMOS devices is avoided, and transitions on the output are accomplished without 'fighting' the cross-coupled NMOS and PMOS pairs.

The state diagram in Figure 7.15 fails to include a mechanism for stopping on specified phases to control the number of cycles that are swallowed in a given time frame. A stopping mechanism is included in Figure 7.18, and is accomplished by 'blocking' the transition of selection signals, SEL_Φ_i, to high levels.

The selective blocking action is accomplished through a slight modification of the PC registers shown in Figure 7.17. As illustrated in Figure 7.19, the outputs of the register are selectively blocked from going high by preventing the outputs of the first latch in the register from going low. The placement of NMOS transistors in the first latch accomplishes this behavior, as verified by the truth table shown in the figure. Note that the stacking of PMOS devices is still avoided.

The complete state machine implementation is shown in Figure 7.20. As shown, a simple and high speed topology is achieved by simply modifying the divide-by-4 structure to include selective blocking behavior. The included truth table reveals that the setting of the control variables, $\{CON_1 CON_0\}$, equals the state stopped on.

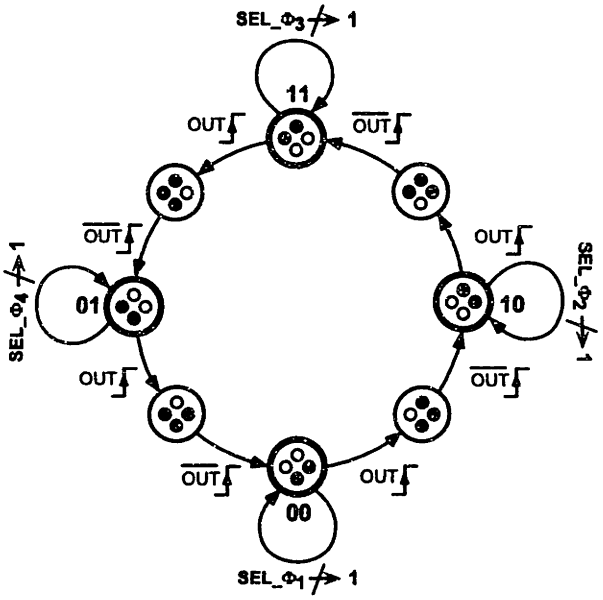


Figure 7.18: Complete state diagram to realize appropriate transitions between and selective stopping on divider phases.

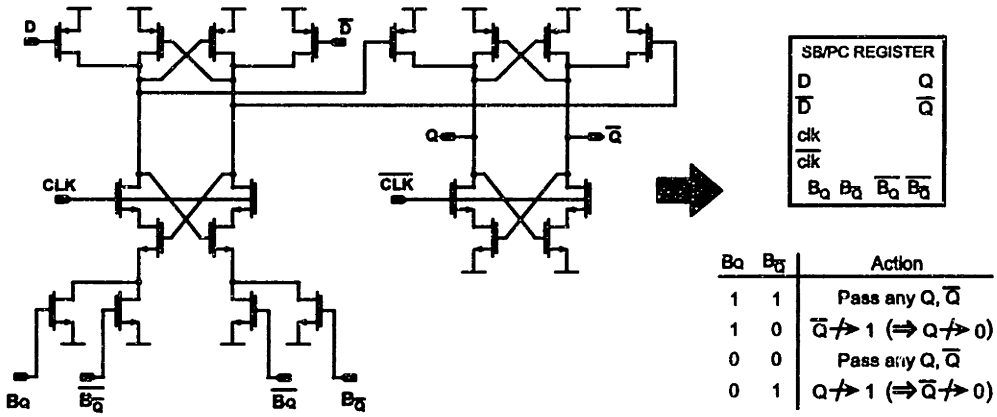
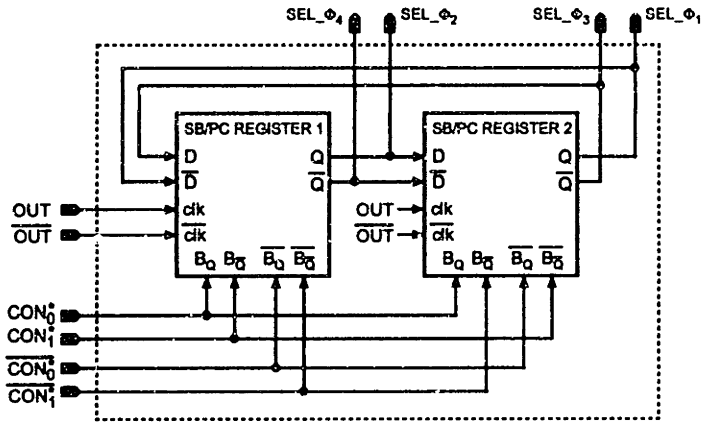


Figure 7.19: Selective-blocking (SB) register using PMOS-coupled (PC) latches.

7.2.2 Divide-by-2/3 Core Design

Figure 7.21 shows a divide-by-2/3 topology that is a modified version of the divide-by-2/2.5/3/3.5 structure discussed above. High speed is attained by using the same 4-Phase Divide-by-2 structure, and a similar multiplexer style. The fast circuit speed



Stop State	Required Blocking Action	REG 1 B_Q $B_{\overline{Q}}$	REG 2 B_Q $B_{\overline{Q}}$	CON_1^* CON_0^*
0 0	$SEL\_\Phi_1 \not\rightarrow 1$ ($SEL\_\Phi_3 \not\rightarrow 0$)	0 0	0 1	0 0
1 0	$SEL\_\Phi_2 \not\rightarrow 1$ ($SEL\_\Phi_4 \not\rightarrow 0$)	0 1	0 0	1 0
1 1	$SEL\_\Phi_3 \not\rightarrow 1$ ($SEL\_\Phi_1 \not\rightarrow 0$)	1 1	1 0	1 1
0 1	$SEL\_\Phi_4 \not\rightarrow 1$ ($SEL\_\Phi_2 \not\rightarrow 0$)	1 0	1 1	0 1

Figure 7.20: Complete state machine implementation to control phase transitions.

is needed in the first divide-by-2/3 section in order to satisfy the delay requirements imposed by the control qualification circuitry of the preceding divide-by-2/2.5/3/3.5 section. The speed requirements are greatly reduced for following stages, but the same structure is used for simplicity in design.

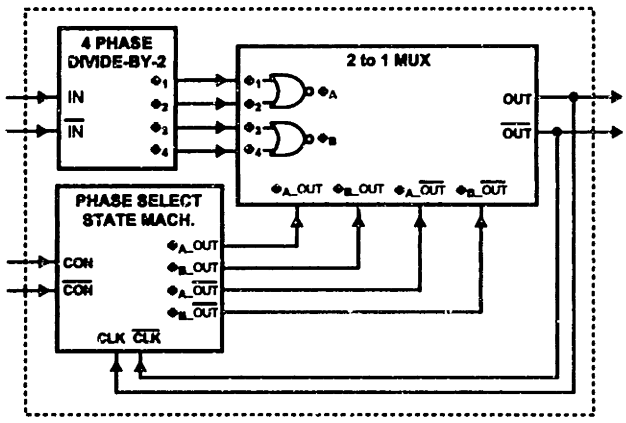


Figure 7.21: Divide-by-2/3 core design.

Multiplexer Design

Figure 7.22 shows the multiplexer design for the divide-by-2/3 stages. The four phases from the divide-by-2 circuit are combined with an OR operation to produce two complementary phases, Φ_A and Φ_B. These phases are gated to the output signals, OUT and $\overline{OUT}$, using PMOS devices that are controlled by four different control signals as shown in the figure. It is important to observe that the default state of a given output is high when neither phase is gated to it.

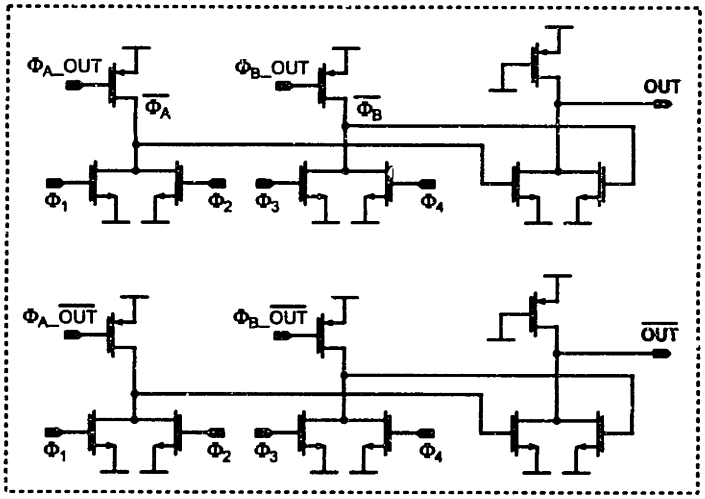


Figure 7.22: Multiplexer for divide-by-2/3 core.

Divide-by-2/3 State Machine

The phase transition sequence illustrated in Figure 7.23 accomplishes cycle swallowing through phase transitions in a glitch free manner. The state of each of the four control signals is shown during the swallowing of two pulses, and are separated by dashed lines into phases sent to OUT and phases sent to $\overline{OUT}$. Darkened bubbles imply that a particular phase is sent to the respective output, and blank bubbles imply that the phase is blocked from going to the output. As shown, there are points where neither phase is sent to their respective output, which leads to the output going to a high level during that time.

A state transition diagram that achieves the desired phase transition behavior is shown in Figure 7.24. Core states are again labeled with state numbers, and are connected with transition states that allow glitch-free transitioning between phases. Selective stopping on state 0 or 1 is achieved through the setting of the control variable, CON.

Implementation of the state transition diagram is accomplished with three cascaded PC latches as shown in Figure 7.25. The operation of the state machine is

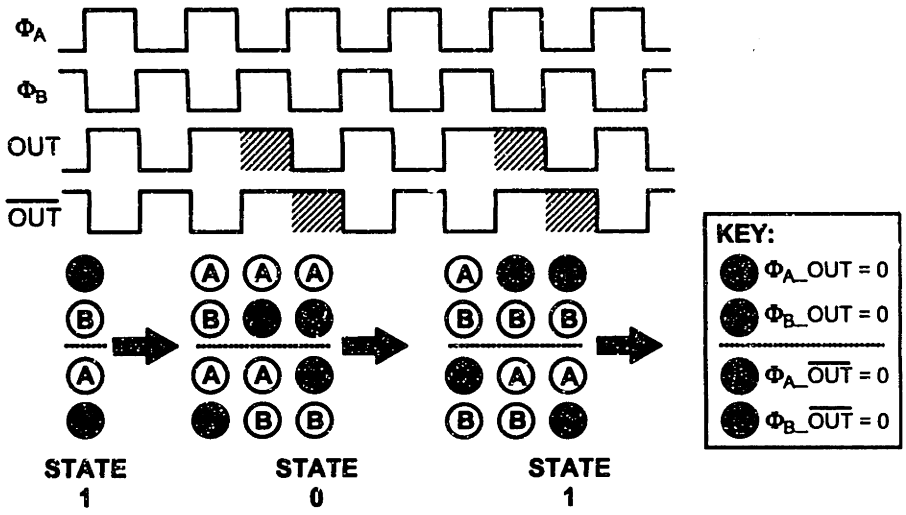


Figure 7.23: Divide-by-2/3 phase transition timing.

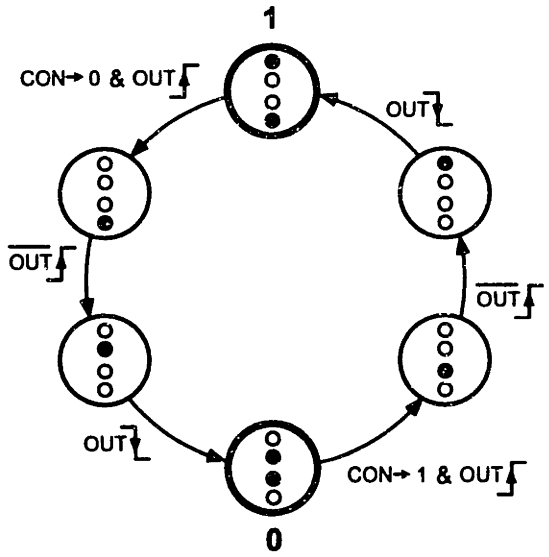


Figure 7.24: Divide-by-2/3 state transition diagram.

described by the timing diagram included in the figure.

7.2.3 Control Qualification Circuits

Figure 7.26 shows the control qualification circuit and timing diagram for the divide-by-2/2.5/3/3.5 block. The illustrated topology gates the control signals, which are brought in as complementary pairs, to the state machine inputs when each of the

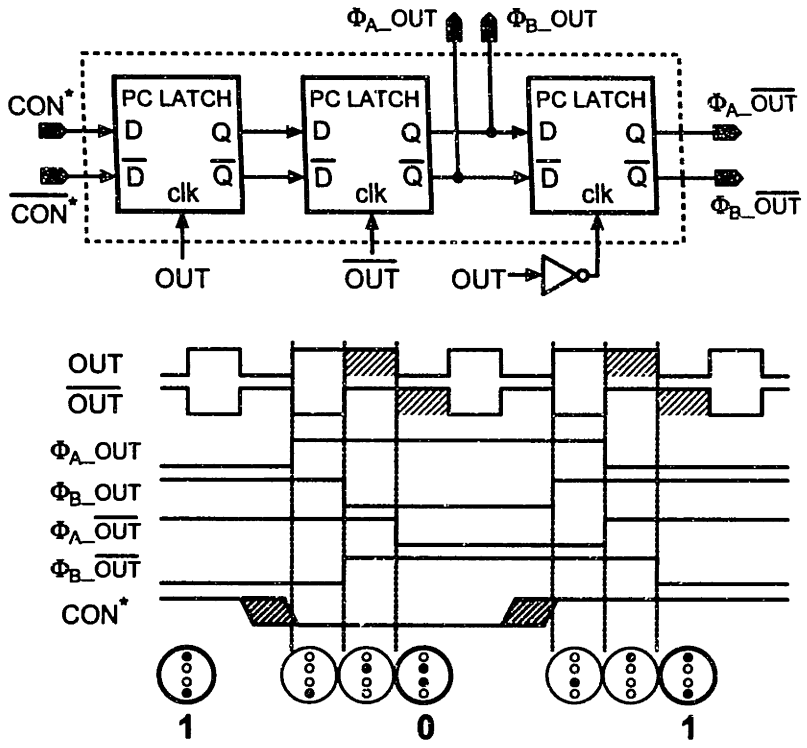


Figure 7.25: Divide-by-2/3 state machine implementation.

following divide-by-2/3 output stages have low outputs. High speed is achieved by using gating logic similar to that in the multiplexer circuits, and the high speed latch used in the divide-by-2 circuit. Note that two identical sections are used to gate CON_0 and CON_1, the circuit for CON_1 not being shown.

Control qualification for the divide-by-2/3 sections is also accomplished by gating the control signals when each of the following divide-by-2/3 outputs is low. The circuit used in the first section following the divide-by-2/2.5/3/3.5 block is shown in Figure 7.27.

7.2.4 Mapping Logic

The mapping of desired division values to their respective control signals is shown for the divide-by-2/2.5/3/3.5 structure in Figure 7.28. As revealed by the example shown in Figure 7.28(A), the number of swallowed pulses within one overall divide cycle is set by incrementing the current stopping state by the required division value. A circuit that accomplishes the required operation is shown in Figure 7.28(B).

The mapping logic for the divide-by-2/3 sections is very simple to implement since the swallowing of a pulse is accomplished by simply complementing the control signal. Figure 7.29 reveals that the required circuitry is implemented as a registered XOR

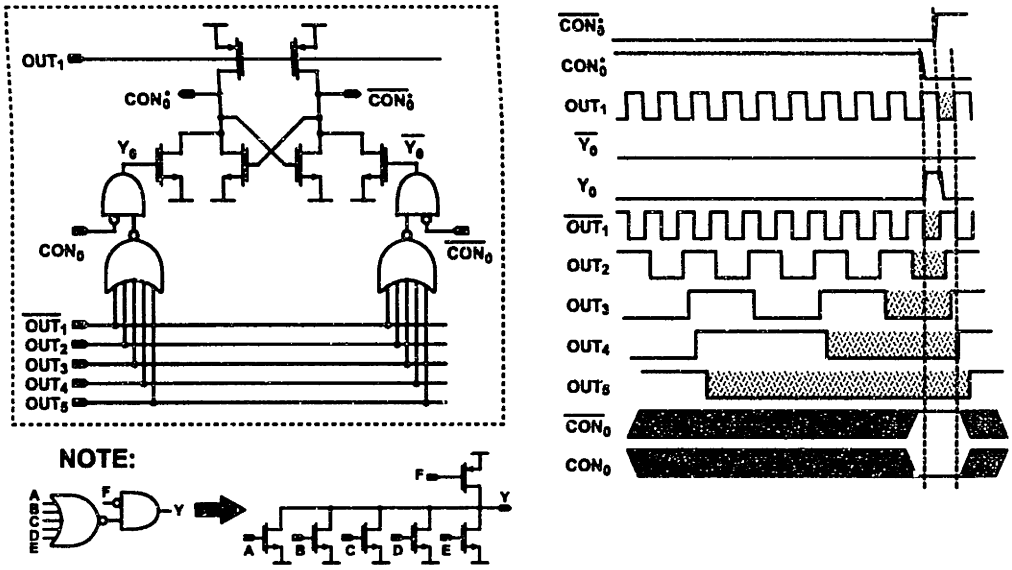


Figure 7.26: Qualification circuit and timing for divide-by-2/2.5/3/3.5 section.

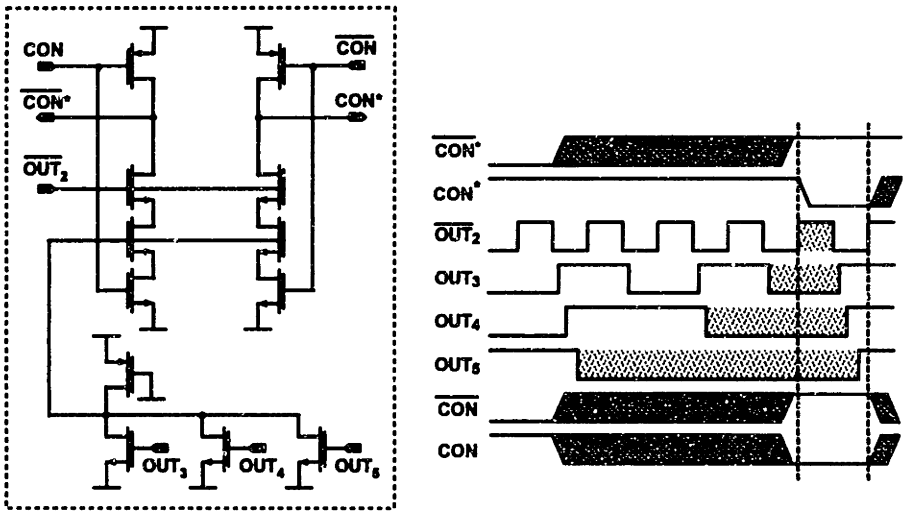


Figure 7.27: Qualification circuit and timing for divide-by-2/3 sections.

gate.

7.3 Summary

This chapter presented architectural and implementation details of the 64 modulus divider used in the prototype system. The design uses an extended version of the

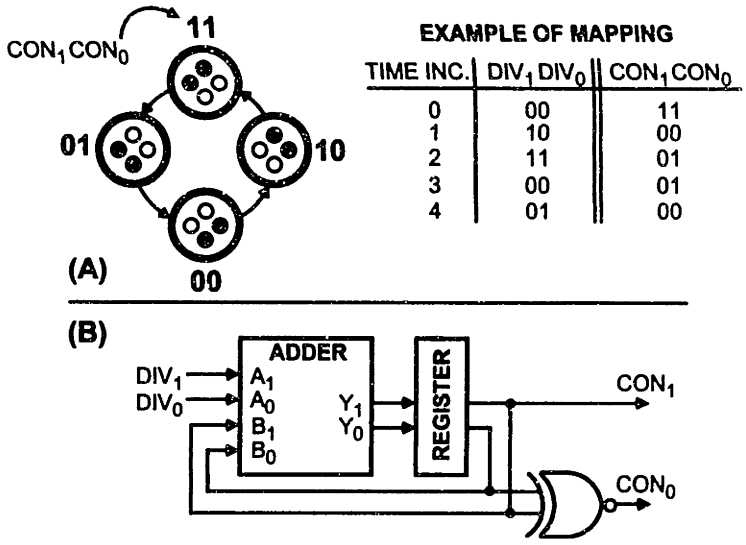


Figure 7.28: Mapping logic from divide value to control signal for divide-by-2/2.5/3/3.5 section.

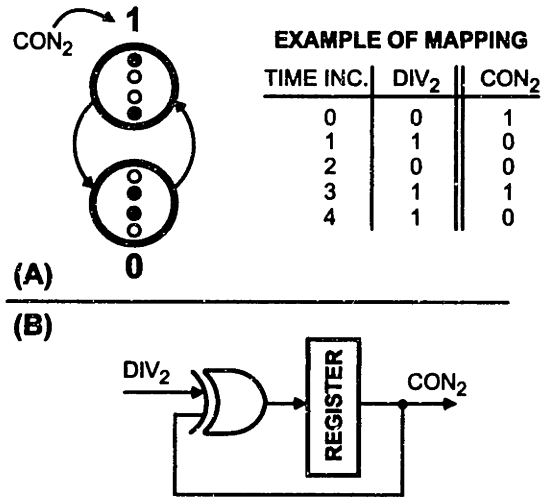


Figure 7.29: Mapping logic from divide value to control signal for divide-by-2/3 section.

dual-modulus structure to realize a contiguous range of divide values that span from 32 to 63.5 in half cycle increments. A phase shifting technique allows a minimal number of components to operate at high frequencies — the first two stages in the divider are divide-by-2 circuits as opposed to state machines. An initial divide-by-2 stage is placed off-chip in the prototype, which lowers the frequency coming into the IC and changes the divide range to 64 through 127 in integer increments.

Chapter 8

Digital Data Path

This chapter describes the digital data path of the transmitter, which is composed of the blocks shown in Figure 8.1. A brief description of the operations performed in this pathway is now given. First, the binary data is convolved with the compensated transmit filter using a ROM and then added to a constant digital word corresponding to the nominal divide value, N_{nom}; Figure 8.2 displays the bit alignment between these signals. The value of N_{nom} sets the carrier frequency by virtue of the fact that $F_{out_c} = N_{nom}F_{ref}$. A Σ-Δ modulator then quantizes the resulting 16-bit sequence into a 6-bit sequence which is fed into the input of the divider.

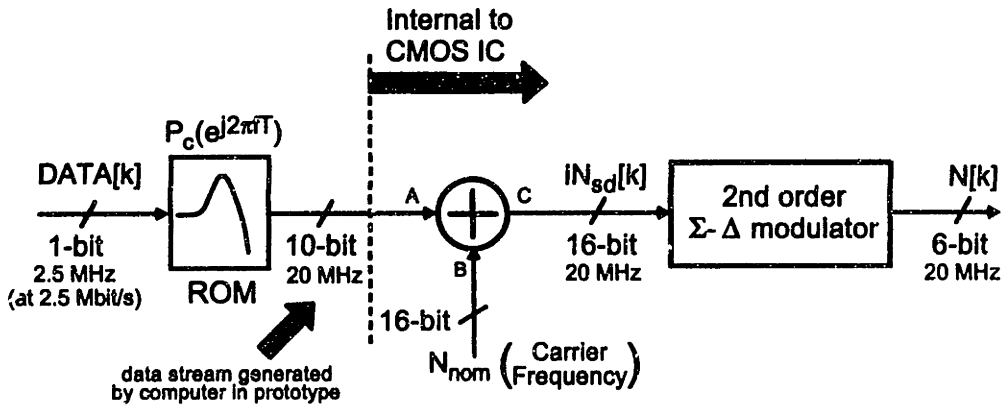


Figure 8.1: Digital data path to divider input.

To achieve the goal of low power, a pipelining technique discussed in [54, 55] is applied to the Σ-Δ modulator and adder in Figure 8.1. This approach allows the required throughput rate to be achieved with lower circuit speed, thus permitting reduction of power supply voltage. The cost of pipelining is an increase in the circuit area, and capacitance that must be switched during use. However, low power dissipation is achieved with supply scaling despite the increased capacitance, as discussed in [68].

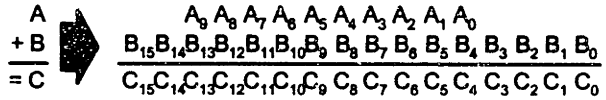


Figure 8.2: Bit alignment between modulation signal and N_{nom} when added to form $IN_{sd}[k]$.

We begin by reviewing the basic topology and properties of the second order, MASH Σ-Δ modulator used in the prototype. The pipelining technique is then presented, and its impact on the overall digital path design is described. Finally, issues related to the depth of pipelining are discussed, and circuit descriptions given.

8.1 Topology

Figure 8.3 shows the second order MASH Σ-Δ topology used in the prototype. The basic building blocks of the structure are first order sections consisting of accumulators whose carry bits are used as output. Each first order stage adds noise according to the relationship

$$out[k] = in[k] + (D-1)e[k], \tag{8.1}$$

where we have invoked the notation $D^i e[k] = e[k-i]$. In the presence of a sufficiently active input, $e[k]$ can be considered a white noise source with spectral density

$$S_e(f) = 1/12. \tag{8.2}$$

A single first order Σ-Δ stage thus adds quantization noise whose energy is shaped into high frequencies, as seen by examining the spectral density of the output:

$$S_{out}(f) = S_{in}(f) + \left|e^{-j2\pi fT} - 1\right|^2 S_e(f). \tag{8.3}$$

The cascade of two stages, as depicted in the figure, leads to second order noise shaping according to the relationship

$$S_{OUT}(f) = S_{IN}(f) + \left|(e^{-j2\pi fT} - 1)^2\right|^2 S_e(f). \tag{8.4}$$

This last expression is calculated from the equation:

$$OUT[k] = out_1[k] + (1 - D)out_2[k] = IN[k] + (1-D)^2 e_2[k], \tag{8.5}$$

where $e_2[k]$ is assumed to have the same spectral density as $e[k]$ described above.

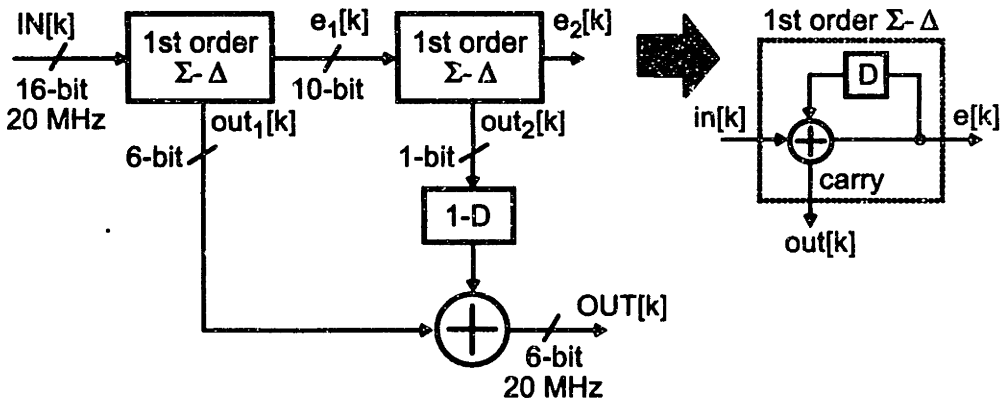


Figure 8.3: A second order, digital MASH structure.

8.2 Pipelining Technique

A MASH structure of any order has adders and accumulators for its basic building blocks. These components can be pipelined [54, 55] using a technique that will now be described.

The carry chain forms the critical delay path for adders; the carry signal must propagate from the least to most significant bit during each addition operation. This leads to a proportional relationship between the time required for computation and the number of bits in the adder. Pipelining of the carry path at the bit level breaks this relationship by allowing the carry information to travel through only one bit stage per clock cycle regardless of the number of bits in the adder.

Implementation of this approach is accomplished by inserting registers in the carry path, as illustrated in Figure 8.4 for a 3-bit example. The shading in the adder symbol shown in the figure distinguishes the structure from a standard adder (which does not contain registers in its carry path). To achieve time alignment between the input and the delayed carry information, registers are used to skew the input bits. As indicated in the figure, we refer to this operation as "pipe shifting" the input. The adder output is realigned in time by performing an "align shift" of its bits as shown.

The same pipelining approach can be applied to accumulators, as illustrated in Figure 8.5. At first glance, it is somewhat surprising that this technique would work for this structure since feedback is present. However, it is important to note that there is *no* feedback from higher to lower bits. The passing of carry information therefore takes place in open loop fashion, which allows pipelining to be applied without influencing stability.

A MASH Σ-Δ converter of *any order* can be pipelined using the techniques thus described. Using the symbols introduced in the previous two figures, Figure 8.6 depicts a pipelined, second order MASH topology. Briefly describing its operation, each first order Σ-Δ is realized as a pipelined accumulator with feedback removed

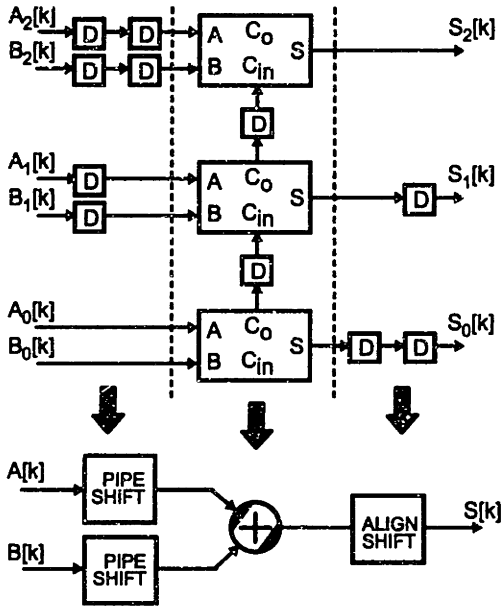


Figure 8.4: A pipelined adder topology.

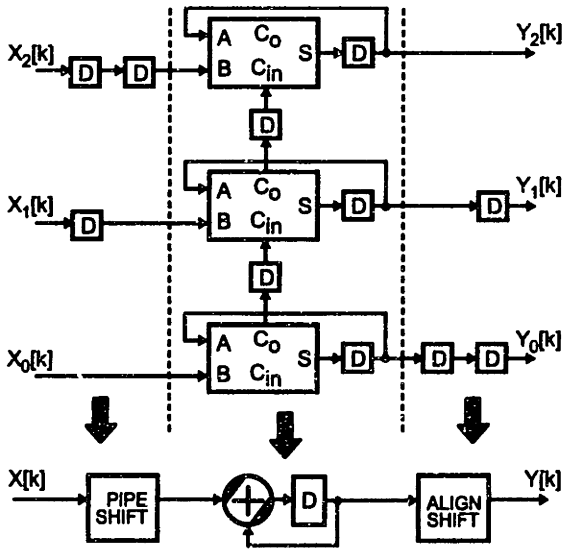


Figure 8.5: A pipelined accumulator topology.

from the most significant bits in its output. The output of the second stage is fed into the filter $1 - D$, which is implemented with two pipelined adders and a delay element, A. Note that a delay, B, is inserted between these two adders in order to pipeline their sum path, which requires a matching delay, C, in the path above for time alignment. A delay, D, must also be included in the output path of the first Σ-Δ stage to compensate for the time delay incurred through the second stage. The

complete pipelined Σ-Δ topology requires pipe shifting of its input data and align shifting of its output data as discussed above. It is useful to note that once a signal is placed in the "pipe shifted domain", it can be sent through any number of cascaded, pipelined adders and/or accumulators. Therefore, only one pipe shift and align shift need be done in the entire structure.

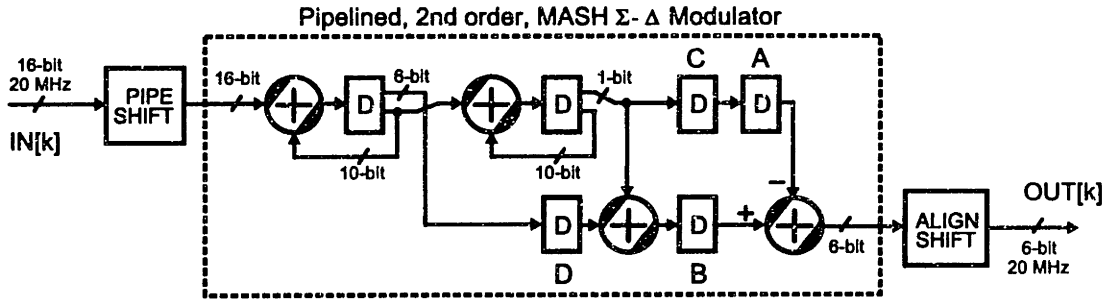


Figure 8.6: A pipelined, second order, digital MASH structure.

Figure 8.7 illustrates the implementation of the overall digital path using pipelining. To achieve flexibility, the compensated digital transmit filter was implemented in software and the resulting digital data stream fed into the custom CMOS IC. Within the IC, all components are pipelined to achieve low power operation. Note that the carrier frequency signal was not pipe shifted since it is constant during modulation.

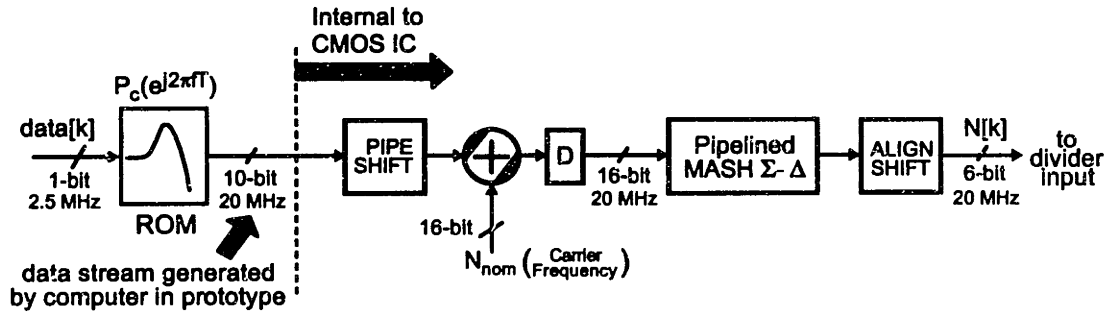


Figure 8.7: Pipelined digital data path to divider input.

8.3 Depth of Pipelining

Although the pipelining technique has been presented as the placement of registers in the carry path after *each* of the one-bit adders, this need not be the case. For instance, registers could be placed between *every other* one-bit adder. In this case, the carry information needs to pass through two stages per cycle rather than one.

Although the delay through the structure is then increased by a factor of two, the area consumed by the many registers required for pipelining is cut in half. In fact, savings in power are potentially obtained in this case if the energy consumption of the registers required for pipelining far outweighs that of the adder cells. The choice of the pipelining level should be made with respect to both area constraints and relative energy consumption within the overall system.

In the context of this work, the choice of pipelining level was made in consideration of the power of other components on the CMOS chip. Specifically, it was found that 2-bit level pipelining of the digital data path dropped its power consumption to a negligible amount in comparison to the high speed divider. Since the 2-bit approach allows an area reduction over the 1-bit approach, it was deemed the better choice for this application. Higher levels than 2-bit were not considered since the further savings in area would be minor, and could lead to higher power dissipation.

8.4 Circuit Implementation

Figure 8.8 and Figure 8.9 illustrate the dynamic TSPC registers and static adder structure used to implement the digital data path on the 0.6 micron CMOS chip. The adder structure was designed such that its carry logic transistors were small, having roughly the same size as those implementing the sum logic. Generally, this is not the case — carry logic transistors are usually made much larger than their sum counterparts in order to speed up the carry chain. Since the carry chain has been pipelined in our case, there is no need for such large transistors. The resulting decrease in area of the adder cell somewhat alleviates the increase in area accrued by the pipelined registers. As for the registers, a dynamic topology was chosen over a static version to obtain lower area. The TSPC technique simplified the clocking scheme by allowing only one clock line.

Evaluation of the power consumption of each of the above circuits was done using the HSPICE simulation tool; the results with a 1.5 Volt supply are shown in Table 8.1. The table reveals that the adder circuit has twice the energy consumption per operation as that of the registers. For simplicity in analysis, we will conservatively assume that both types of registers consume the same power as the noninverted register.

Component	Energy consumption
Static adder	.150 fJ/operation
Noninverting TSPC register	.075 fJ/operation
Inverting TSPC register	.056 fJ/operation

Table 8.1
Energy consumed by circuit blocks within the digital data path with a 1.5 volt supply

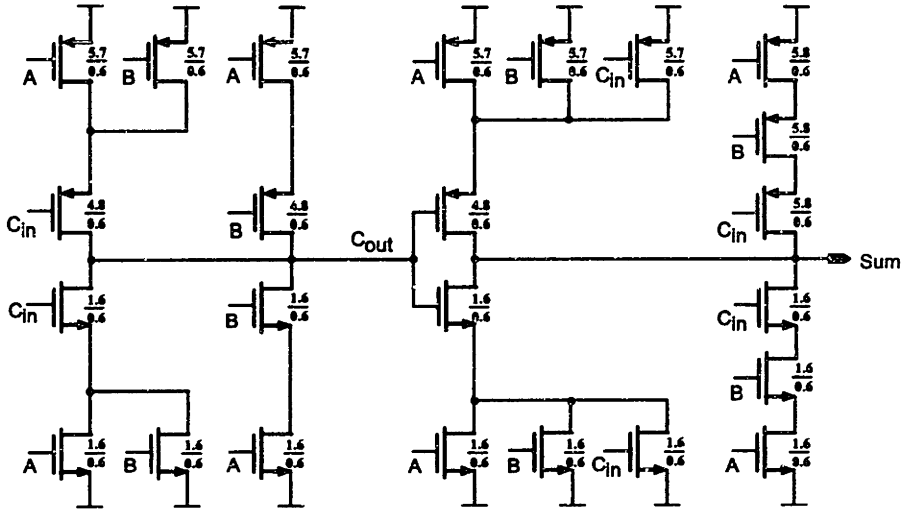
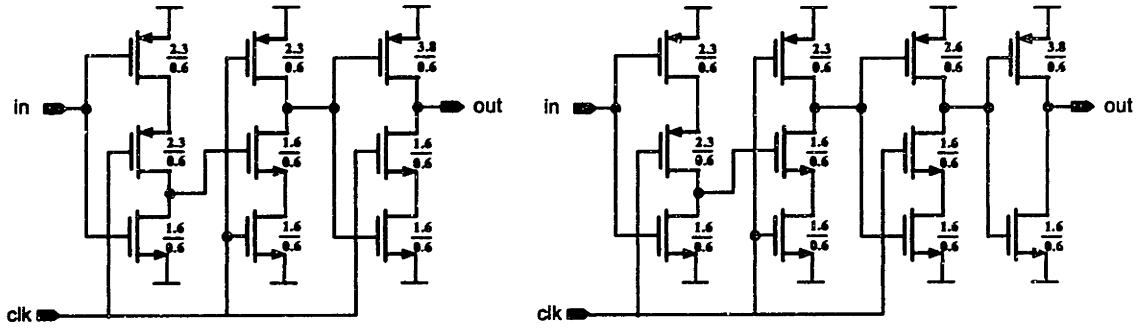


Figure 8.8: A static mirror adder circuit.



(a) (b)

Figure 8.9: Dynamic TSPC register circuits: (a) inverting, (b) non-inverting.

Table 8.2 presents a tabulation of the number of adders and registers required in the digital data path contained in the CMOS IC under pipelined and non-pipelined conditions; the numbers were obtained directly through examination of Figures 8.6 and 8.7. Energy estimates with a 1.5 V supply were computed from Table 8.1 and 8.2 as:

Adder energy: 8.1 fJ/operation,
Register energy: 7.9 fJ/operation.

Given that the energy dissipation of CMOS circuits is directly proportional to the amount of capacitance switched, we see that the capacitance added by the pipelining technique is less than a factor of two over the non-pipelined case. However, a speedup of a factor of 8 is gained — the carry path must pass through 2 one-bit adders as

opposed to 16 one-bit adders per clock cycle.

Case	Adders	Registers
Non-pipelined	54	21
Pipelined (2-bit)	54	105

Table 8.2
Number of adders and registers for the pipelined (2-bit) and non-pipelined case of the digital data path.

Figure 8.10 displays the measured power dissipation of the Σ-Δ modulator for a range of supply voltages. The plot reveals that power dissipation increases as roughly the square of the supply voltage, which is expected since the energy required to charge capacitance C is $\frac{1}{2}CV_{dd}^2$ [68].

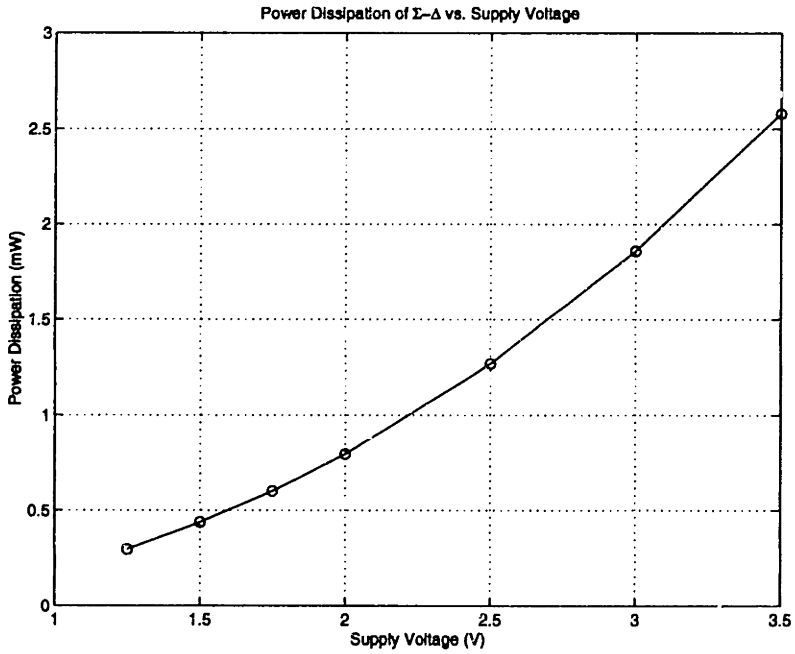


Figure 8.10: Measured power dissipation of Σ-Δ vs. supply voltage.

8.5 Summary

This chapter presented implementation details of the Σ-Δ modulator and surrounding circuits in the digital data path used in the prototype. It was shown that a well known pipelining technique for adders and accumulators can be applied to the MASH Σ-Δ structure to achieve low power operation of this component.

Chapter 9

Analog Phase Comparison Path

The achievement of accurate PLL dynamics is accomplished in the prototype system with the variable gain loop filter topology depicted in Figure 9.1. In a mathematical sense, the input to the filter is the instantaneous phase error between the reference frequency and divider output. Here we use the definition of phase described in Chapter 2, and denote the instantaneous phase of *Ref* and *Div* as $\Phi_{ref}[k]$ and $\Phi_{div}[k]$, respectively. The instantaneous phase error at the PFD output, E, is defined as

$$\Phi_e[k] = \Phi_{ref}[k] - \Phi_{div}[k].$$

In the actual circuit, $\Phi_e[k]$ manifests itself as the deviation of the PFD output duty cycle from its nominal value of fifty percent. As modulation data is applied, the changing value of $\Phi_e[k]$ causes the duty cycle to be swept across a range of values; the shaded region in the figure corresponds to the deviation that occurs when GFSK modulation at 2.5 Mbit/s is applied.

To produce a signal that is a filtered version of $\Phi_e[k]$, the output of the PFD is converted to complementary current waveforms by a charge pump before being sent into the inputs of an on-chip loop filter. The conversion to current allows the filtering operation to be performed without resistors, and also provides a convenient means of performing gain control of the resulting transfer function using the D/A converter shown. An integrator is included in the loop filter, which forces the average current from the charge pump to be zero and the nominal duty cycle to be, ideally, fifty percent when the PLL is locked.

A fifty percent nominal duty cycle is desired to avoid the dead-zone of the PFD, and thus reduce distortion of the modulation signal. Such an approach is seldom used in PLL circuits due to power consumption and spurious noise issues. Fortunately, the system discussed in this paper does not suffer from these problems due to the fact that the charge pump output current is very small (at its largest setting, it toggles between +3.5 uA and -3.5 uA), and the loop filter bandwidth is very low (84 kHz) in comparison to the PFD output frequency (20 MHz). The resulting spur at the transmitter output is less than -60 dBc at 20 MHz when measuring the transmitter in

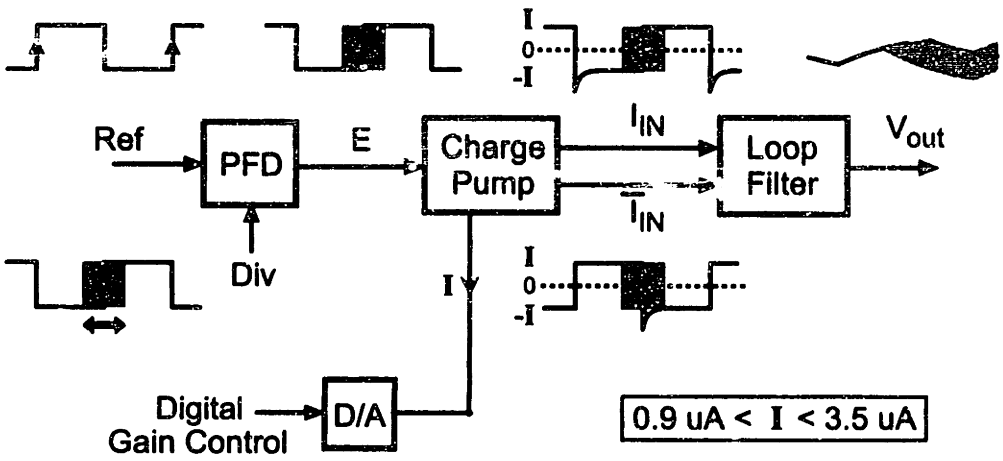


Figure 9.1: Analog phase comparison path consisting of a PFD, charge pump, and loop filter.

an unmodulated state without an RF bandpass filter at its output. When modulated, this spur is convolved with the modulation signal and thus turned into phase noise; it is reasonable to assume that this noise is reduced to a negligible level when the RF bandpass filter is included due to its high frequency offset.

This chapter describes implementation and modeling details of the variable gain loop filter. We begin by providing circuit level details of the PFD, charge pump, loop filter, and D/A shown in Figure 9.1. A frequency-domain model of the overall filter is then presented, and its derivation given. The chapter concludes by examining the effects of large duty cycle deviations in E.

9.1 Implementation

This section describes the circuits used to implement the various component blocks in Figure 9.1.

9.1.1 PFD

The requirement of a fifty percent nominal duty cycle at the output of the PFD prevents this component from being implemented by a common tri-state design [60]. The circuit implementation chosen for the PFD, depicted in Figure 9.2, is taken directly from on an extended XOR design described in [44]. Under locked conditions in the PLL, phase comparison is accomplished in the structure through the use of an XOR gate. The phase detection region of the XOR gate is extended to 360 degrees by dividing *Ref* and *Div* by two in frequency before sending these signals to its inputs,

which leads to a PFD output frequency equaling the reference frequency. When the PLL is out of lock, frequency detection is accomplished by gating the XOR output with the outputs of two cross coupled registers that force the PFD to a high or low value according to the sign of the frequency error between *Div* and *Ref*.

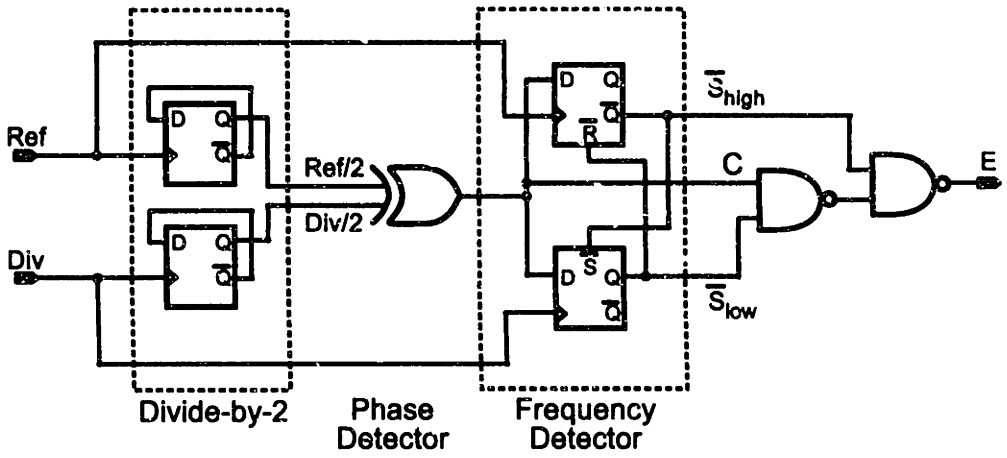


Figure 9.2: Schematic diagram of PFD.

To provide more detail of the phase detector portion of the PFD, Figure 9.3 illustrates the DC characteristic of the XOR gate as a function of the phase difference in its input signals. As discussed in [60], the DC output of the XOR gate is a triangular function of the DC value of $\Phi_e[k]$. Since the effective gain of the XOR corresponds to the slope of its DC characteristic, we see that the gain of the PFD flips between positive and negative values as $\Phi_e[k]$ is changed. Since the stability of the PLL feedback loop is a function of the sign of the PFD gain, the operation of the XOR is seen to vary between stable and unstable regions. In the context of the PLL feedback loop, a positive sign for the phase detector gain will be assumed to yield stable dynamics.

The stable and unstable regions of the XOR gate can be discerned by the value of its output, C, on rising transitions of *Ref* and *Div*. In the stable region, C is low when *Ref* transitions high and is high when *Div* transitions high. The opposite conditions are true in the unstable region.

The frequency detector portion of the PFD uses the above XOR characteristics to advantage. Specifically, the registers within the frequency detector monitor the value of C at positive transitions of *Ref* and *Div* to determine the XOR gate's current region of operation. If the XOR is in the stable region, which is the case under locked conditions, its output passes directly to the PFD output. If the XOR enters the unstable region, the output of the PFD is set either low or high according to the state diagram shown in Figure 9.4. As indicated in the figure, the PFD output is set high if the *Ref* transition is the first to occur in the unstable region. Conversely

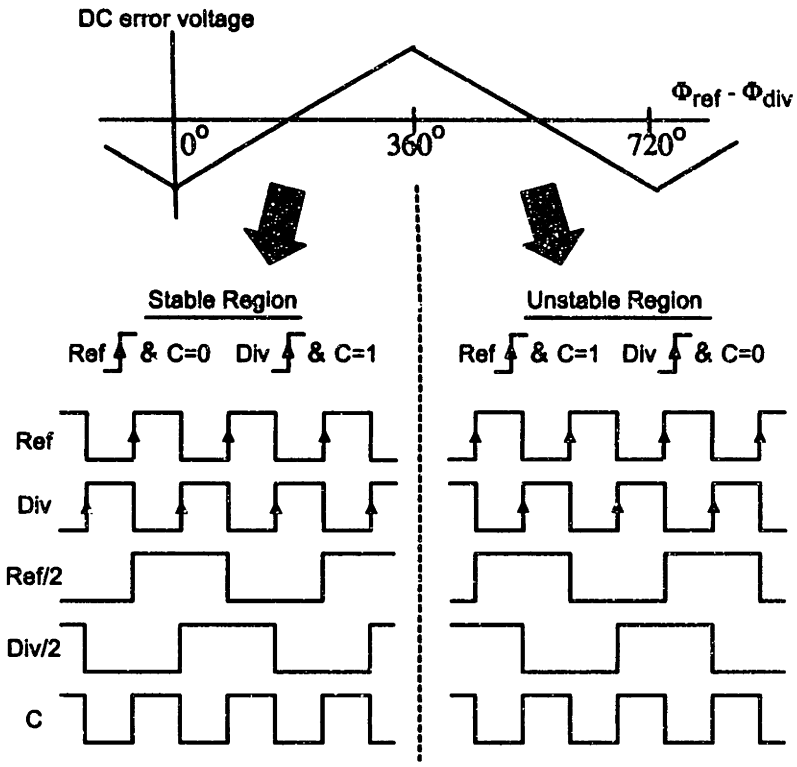


Figure 9.3: XOR characteristic and associated signals within the PFD.

the PFD output is set low if the *Div* transition occurs first in the unstable region. These output values remain constant until the XOR enters back into its stable region. Figure 9.5 provides an example of the signals that occur in the PFD logic when the frequency of *Div* is higher than that of *Ref*. In this case, *E* correctly directs the VCO to lower its output frequency by virtue of its low average value.

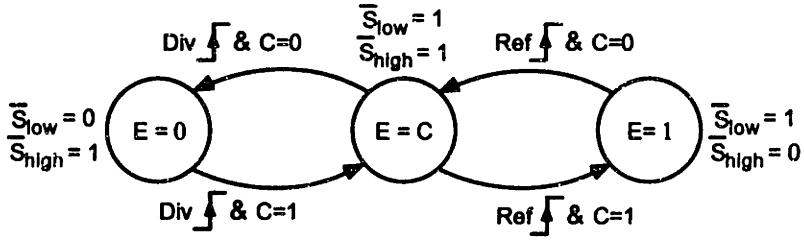


Figure 9.4: State transition diagram of the frequency detector portion of the PFD.

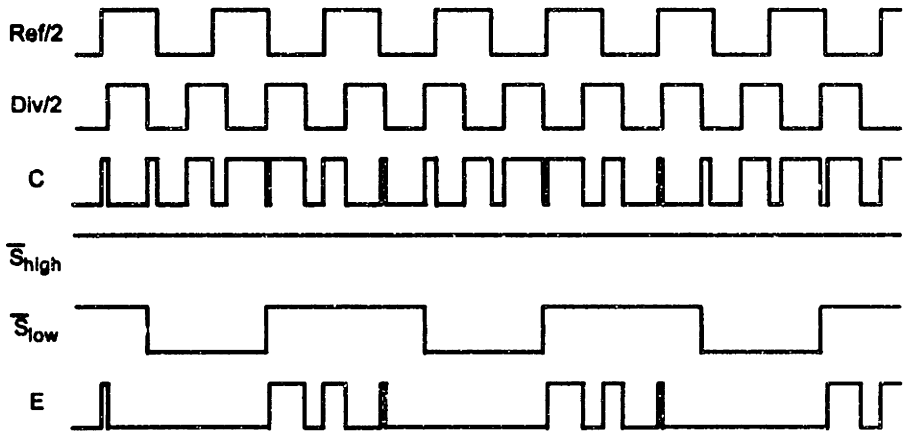


Figure 9.5: Example of signals produced from PFD when *Div* frequency is too high.

9.1.2 Charge Pump

Proper design of the charge pump is critical for the achievement of high data rates since it forms the bottleneck in dynamic range that is available to the modulation signal. Figure 9.6 illustrates the fundamental issues that need to be considered in its design. To avoid distortion of the modulation signal, the variation in duty cycle should be limited to a range that allows the output of the charge pump to settle close to its final value following all positive and negative transitions. Figure 9.6(a) shows the dynamic range available for a well designed charge pump; the nominal duty cycle is fifty percent and the transition times are fast. Figure 9.6(b) demonstrates the reduction in dynamic range that occurs when the nominal duty cycle is offset from 50 percent. This offset is caused by a mismatch between positive and negative currents produced by the charge pump. (The type II PLL dynamics force an average current of zero.) Finally, Figure 9.6(c) illustrates a case in which the charge pump has slow transition times, the result again being a reduction in dynamic range.

The charge pump topology was designed with the above issues in mind, and is illustrated in Figure 9.7. The core component of the architecture is a differential pair (M_1 and M_2) that is fed from the top by two current sources, I_1 and I_2, and from the bottom by a tail current, I_{tail}. Ideally, I_1 and I_2 are equal to I and I_{tail} to $2I$, where I is adjusted by a 5-bit D/A that controls the voltage at node $V_{D/A}$. Transistors M_1 and M_2 are switched on and off according to E, which ideally causes I_{IN} and $\overline{I}_{IN}$ to switch between I and $-I$.

To achieve a close match between the positive and negative currents of each charge pump output, the design strives to set $I_1 = I_2$ and $I_{tail} = I_1 + I_2$. In the first case, I_1 and I_2 are implemented as cascoded PMOS devices whose layout is optimized to achieve high levels of device matching. Unfortunately, device matching cannot be used to achieve a close match between I_{tail} and $I_1 + I_2$ since they are generated by

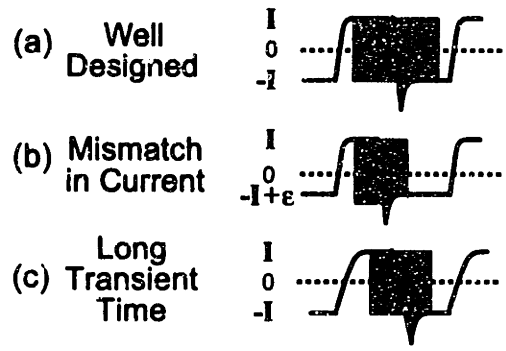


Figure 9.6: Effect of transient time and mismatch on duty cycle range.

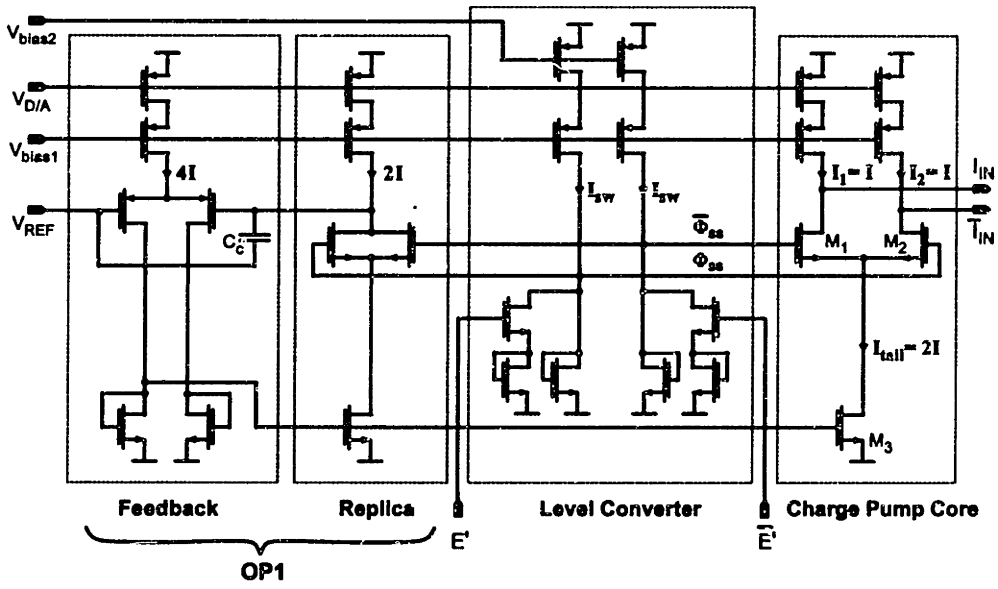


Figure 9.7: Charge pump implementation.

different *types* of devices. To circumvent this obstacle, a feedback stage is used to adjust I_{tail} by comparing currents produced by a replica stage. This technique allows I_{tail} to be matched to $I_1 + I_2$ to the extent that the replica stage is matched to the core circuit.

The achievement of a low transient time in the charge pump response is obtained by careful design of signal and device characteristics at the source nodes of M_1 and M_2. First, the parasitic capacitance at this node is minimized by using appropriate layout techniques to reduce the source capacitance of M_1 and M_2, the drain capacitance of M_3, and the interconnect capacitance between each of the devices. Second, the voltage deviation that occurs at this node when E switches is minimized. The level converter

depicted in Figure 9.7 accomplishes this task by reducing the voltage variation at nodes $\Phi_{ss}(t)$ and $\overline{\Phi}_{ss}(t)$ to less than 350 mV and setting an appropriate DC bias.

An additional level converter is required between the PFD output, E, and charge pump inputs, E' and $\overline{E'}$ since separate supplies are used for the digital and analog sections of the chip. The level converter shown in Figure 9.8 transfers the E signal between these supplies. In addition, this circuitry allows a bit from an on-chip shift register to set the sign of the open loop gain.

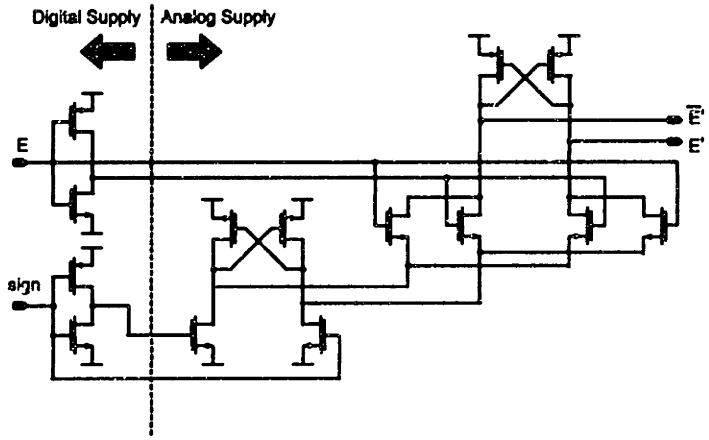


Figure 9.8: Interface circuitry between PFD and charge pump that level converts E from digital to analog supplies, and sets the sign of the open loop gain.

9.1.3 Loop Filter

The on-chip loop filter uses an opamp to integrate one of the charge pump currents and add it to a first order filtered version of the other current. Shown in Figure 9.9, this topology yields a transfer function that is closely approximated as

$$H(f) = K_I \frac{1 + jf/f_z}{jf(1 + jf/f_p)}, \quad f_z = 11.6\text{kHz}, f_p = 127\text{kHz}. \tag{9.1}$$

Details of the accuracy of this approximation, as well as its derivation, are presented in the modeling section of this chapter. The open loop gain, K_I, is adjusted by varying the charge pump output current, I. The first order pole, f_p, is created using a switched capacitor technique, which reduces its sensitivity to thermal and process variations and removes any need for tuning. Note that, although this time constant is formed through a sampling operation, the output of the switched capacitor filter is a continuous-time signal. Finally, the value of the zero, f_z, is determined primarily by the ratio of capacitors C_3 and C_2 under the assumption that the complementary charge pump output currents are matched.

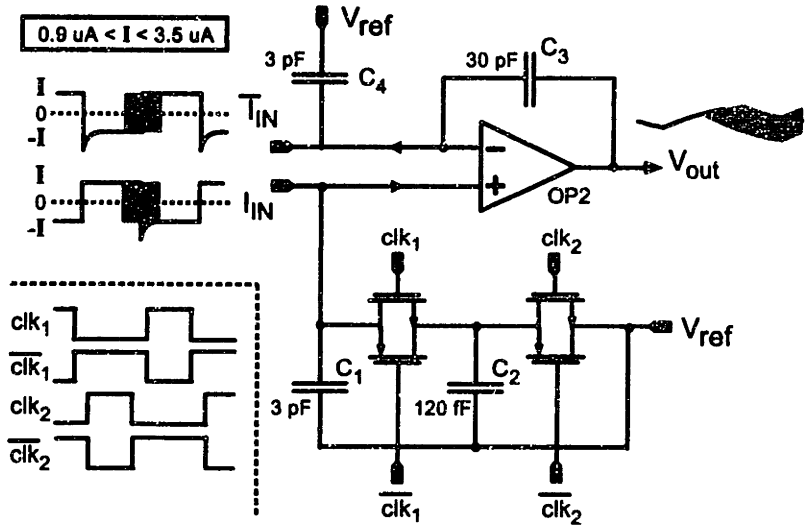


Figure 9.9: Loop filter implementation.

A particular advantage of the filter topology is that the rate of sampling C_1 and C_2 can be set high since it is independent of the settling dynamics of the opamp. As such, clk_1 and clk_2 are set to the PFD output frequency, 20 MHz, to avoid aliasing problems.

As illustrated in Figure 9.10, the opamp is realized with a single-ended, two-stage topology chosen for its simplicity and wide output swing. Its unity gain frequency was designed to be 6 MHz; this value is sufficiently higher than the bandwidth of the GFSK modulation signal at 2.5 Mbits/s to avoid significantly affecting it. It is recognized that the single ended structure has higher sensitivity to substrate noise than a differential counterpart. However, little would be gained in this case by making it fully differential since the output of the opamp is connected directly to the varactor of an LC based VCO, which is inherently single ended. Fortunately, measured results in Chapter 11 show that substrate noise does not significantly degrade the noise performance of the synthesizer.

The limited dynamics of the opamp prevent it from following the fast transitions of its input current waveforms. To prevent these waveforms from adversely affecting the performance of the charge pump and opamp, the voltage swing that appears at the input terminals of the opamp is reduced to a low amplitude (less than 40 mV peak-to-peak) by capacitors C_1 and C_4. (The resulting voltage waveform is approximately triangular in nature.) In the case of C_1, this capacitor also serves as part of the switched capacitor filter.

A large voltage swing at the input terminals of the opamp would undermine the operation of the charge pump and loop filter circuitry. A high amplitude triangle wave would alter $I_{IN}(t)$ according to the finite output resistance of the charge pump

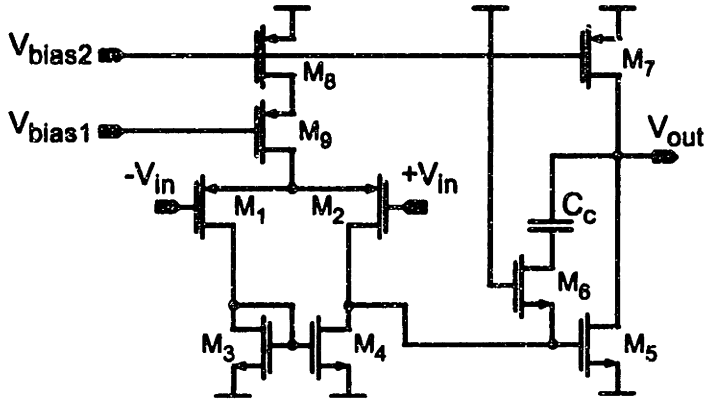


Figure 9.10: Opamp implementation for loop filter.

output; this issue is aggravated by the fact that the charge pump output is cascoded and therefore supports a very limited signal swing over which all transistors in its output stage are kept in saturation. In regards to the opamp, a large signal swing at its input terminals would cause the input differential pair, composed of M_1 and M_2 in Figure 9.10, to exhibit transconductance behavior that is highly nonlinear.

9.1.4 D/A Converter and Biasing

Figure 9.11 illustrates the biasing architecture for the charge pump and loop filter sections. The 5-bit D/A converter that controls the charge pump current, I, is incorporated into this network and adds little power over that required for biasing.

Figure 9.12 displays the resulting values of I obtained from HSPICE when the D/A control bits are switched across their 32 possible combinations. The resulting response is seen to be quite nonlinear; fortunately, this does harm transmitter performance since the D/A is not in the modulation path. Note that the spikes seen in the characterization plot are an artifact of the transient response of the D/A.

9.2 Modeling

Although the loop filter topology of Figure 9.9 has a very simple implementation, exact analysis of its behavior is quite difficult, if not intractable, from an analytical standpoint. This difficulty stems from the fact that modulation of its input is accomplished through duty cycle modulation of a square wave, which greatly complicates efforts to use straightforward Fourier analysis. Fortunately, an approximate analytical model of the loop filter behavior can be derived that is accurate over a wide frequency range. The key to this approximation is to treat the charge pump output

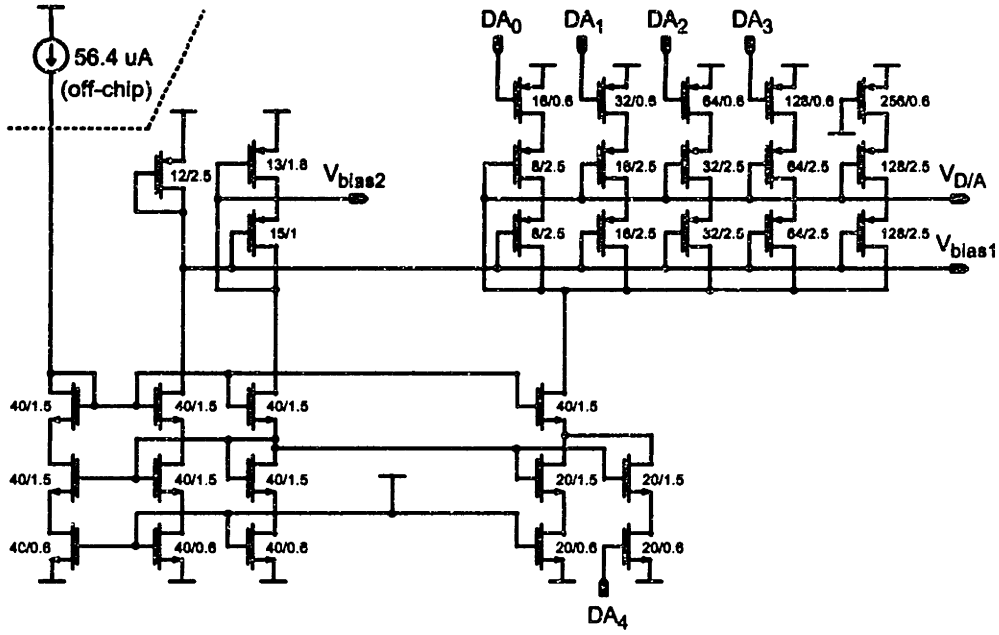


Figure 9.11: D/A converter (5-bit) and biasing circuitry.

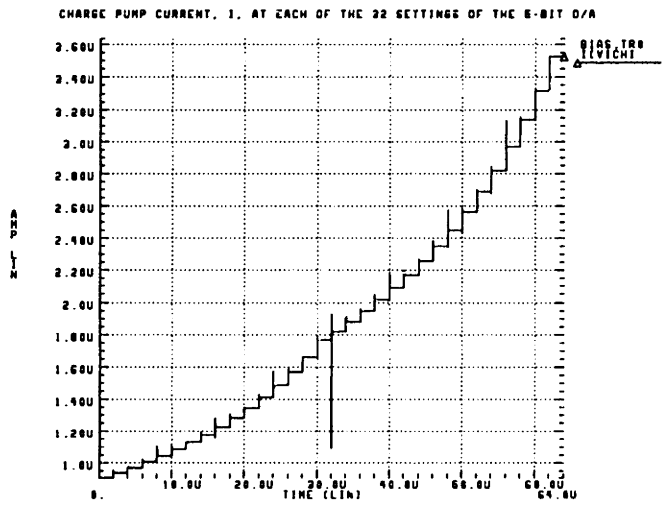


Figure 9.12: Characterization of 5-bit D/A converter.

as the sum of a square wave and a time-varying impulse train.

Figure 9.13 depicts an exact decomposition of $I_{IN}(t)$ into a square wave, $I_{spur}(t)$,

and a time-varying pulse train, $I_e(t)$ such that

$$I_{IN}(t) = I_e(t) + I_{spur}(t). \tag{9.2}$$

As its name implies, $I_{spur}(t)$ has energy content only at discrete frequencies that are multiples of its fundamental frequency, $1/T$. The energy of $I_e(t)$, however, is dispersed over a wide frequency range due to its time-varying nature.

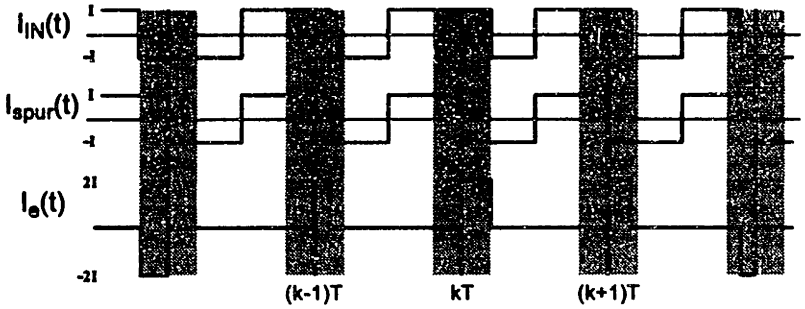


Figure 9.13: Decomposition of $I_{IN}(t)$.

If the pulse widths of $I_e(t)$ are small, this signal can be approximated as a series of impulses to obtain

$$I_{IN}(t) \approx \hat{I}_e(t) + I_{spur}(t), \tag{9.3}$$

where we have defined

$$\hat{I}_e(t) = \sum_{k=-\infty}^{\infty} Q_e[k]\delta(t - kT). \tag{9.4}$$

Since a phase error of 2π radians corresponds to the period T, the area of each impulse, $Q_e[k]$, can be related to the instantaneous phase error,$\Phi_e[k]$, by the expression

$$Q_e[k] = T\left(\frac{\Phi_e[k]}{2\pi}\right)2I. \tag{9.5}$$

We can directly relate $\hat{I}_e(t)$ to the modulated impulse train version of the phase error, $\hat{\Phi}_e(t)$, as

$$\hat{I}_e(t) = \frac{T}{\pi} I\hat{\Phi}_e(t), \tag{9.6}$$

where $\hat{\Phi}_e(t)$ is defined as

$$\hat{\Phi}_e(t) = \sum_{k=-\infty}^{\infty} \Phi_e[k]\delta(t - kT). \tag{9.7}$$

The overall current, $I_{IN}(t)$, is then expressed as

$$I_{IN}(t) = \frac{T}{\pi} I\hat{\Phi}_e(t) + I_{spur}(t). \tag{9.8}$$

Figure 9.14 depicts a model of the analog phase comparison path based on Equation 9.8. The PFD and charge pump scale the phase error impulse train, $\hat{\Phi}_e(t)$, and send noninverted and inverted versions of this signal, along with $I_{spur}(t)$, into the inputs of the loop filter. Within the filter, the switched capacitor network is approximated by an RC loop filter, where the value of resistance is calculated as

$$R_2 = \frac{T}{C_2}. \tag{9.9}$$

The overall transfer function from $\hat{\Phi}_e(t)$ to $V_{out}(t)$ is therefore derived from the figure as

$$\left(\frac{TI}{\pi}\right) \frac{1 + j2\pi f(C_3 + C_1 + C_4)R_2}{j2\pi f C_3(1 + j2\pi f C_1 R_2)}, \tag{9.10}$$

from which we obtain the loop filter transfer function, $H(f)$, as

$$H(f) = I\frac{1 + j2\pi f(C_3 + C_1 + C_4)R_2}{j2\pi f C_3(1 + j2\pi f C_1 R_2)}. \tag{9.11}$$

The transfer function from $I_{spur}(t)$ to $V_{out}(t)$ is computed from Figure 9.14 as

$$\frac{1 + (C_1 + C_4)/C_3}{j2\pi f C_1}. \tag{9.12}$$

Note that the above transfer functions do not include the effect of finite opamp bandwidth, which will cause further attenuation at high frequencies. The unity-gain bandwidth of the opamp is approximately 6 MHz in the prototype; this value is high enough to avoid affecting the modulation data, and has the desirable characteristic of further attenuating the Σ-Δ quantization noise at high frequencies. The additional attenuation also lowers the spurious component caused by $I_{spur}(t)$ well below the value predicted in Expression 9.12. These effects will be seen in measured results presented Chapter 11.

The remainder of this chapter will present a derivation of the above transfer relations and describe the frequency range over which they are valid. This analysis will be performed under the assumption that the approximation in Equation 9.8 holds. We will begin by focusing on the switched capacitor implementation of R_2. The remaining portion of the loop filter implementation will then be analyzed.

In addition, a final section is included to discuss the impact on analysis for cases in which $I_e(t)$ experiences large deviations in its pulse width. In particular, we will examine the difference in power spectrums of $I_{IN}(t)$ and Equation 9.8 when the synthesizer is modulated at 2.5 Mbit/s.

9.2.1 Switched Capacitor Implementation

Figure 9.15 depicts a closed loop model of the switched capacitor network used within the loop filter. As shown, the capacitor C_1 integrates current directed into it to create

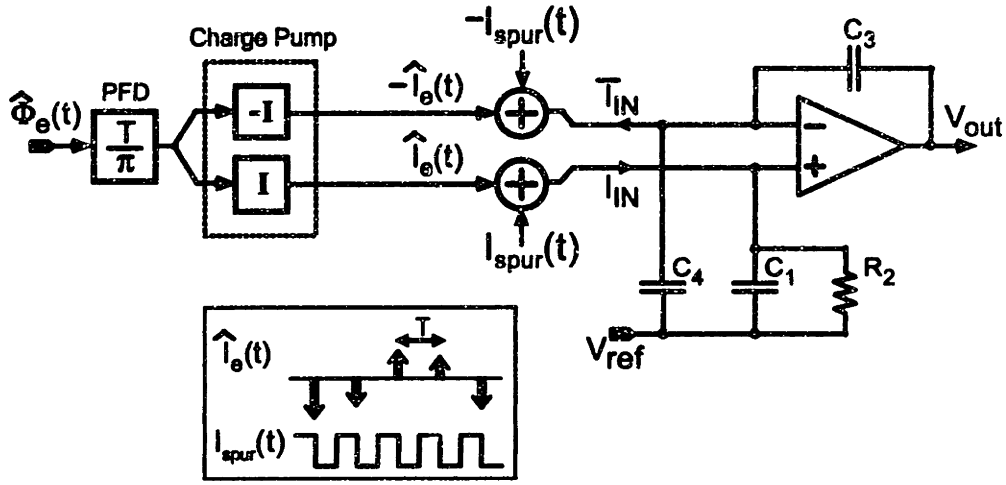


Figure 9.14: Loop filter model.

the voltage $V_1(t)$. During the time that the clk_1 switch is turned off, the gain of this integration operation is $1/C_1$. When the clk_1 switch is turned on, the gain factor is reduced to $1/(C_1+C_2)$ and $V_1(t)$ drops in value by the ratio $C_1/(C_1+C_2)$ due to the inclusion of capacitor C_2. The gain factor reduction and value change is modeled as a multiplication operation with a signal $X_{clk}(t)$ defined as:

$$X_{clk}(t) = \begin{cases} 1 & \text{when } clk_1 \text{ switch is off} \\ \alpha & \text{when } clk_1 \text{ switch is on} \end{cases} \quad \text{where } \alpha = \frac{C_1}{C_1+C_2}. \tag{9.13}$$

A flow of charge occurs between the top and bottom plates of C_2 during the time the clk_1 switch is open and the clk_2 switch closed, and is denoted as $\hat{I}_F(t)$ in the figure. Assuming that the transition of the clk_1 switch from on to off occurs at times $kT+t_o$, $\hat{I}_F(t)$ is an impulse train in current described as

$$\hat{I}_F(t) = \sum_{k=-\infty}^{\infty} Q_F[k]\delta(t-kT-t_o-\epsilon), \tag{9.14}$$

where ϵ is an arbitrarily small value that places the impulses just to the right of $kT+t_o$. The inclusion of ϵ clarifies the evaluation of integral expressions that follow.

The choice of T as the period of clk_1 and clk_2, which is the same as that of the charge pump output, is important in light of aliasing issues. As previously discussed, the charge pump output contains the large spurious signal $I_{spur}(t)$. Although C_1 acts as an anti-alias filter with its integrating action, this spurious component will manifest itself in voltage across C_1 with non-negligible magnitude. It would be highly undesirable to alias this spur to lower frequencies since its attenuation by the overall PLL dynamics would be less effective at such frequencies. The choice of T as the

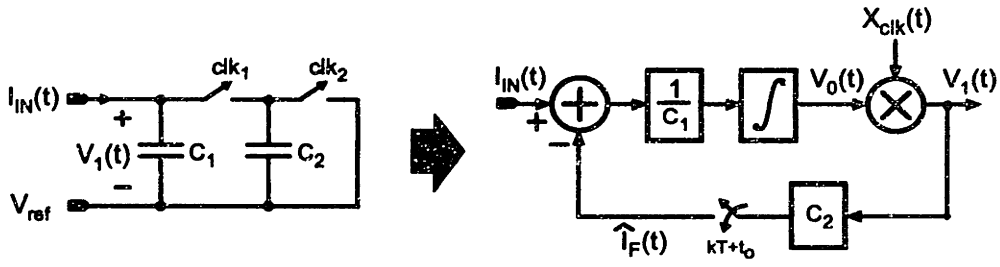


Figure 9.15: Model of first order switched capacitor filter.

period of clk_1 and clk_2 avoids aliasing problems since samples of $I_{spur}(t)$ at these instants appear as a constant voltage (i.e., are mixed down to DC).

To derive a transfer function between $I_{IN}(t)$ and $V_1(t)$ in Figure 9.15, we first seek a description of the influence of $I_{IN}(t)$ on $\hat{I}_F(t)$. At sample times $kT + t_o$, inspection of the figure reveals

$$Q_F[k] = C_2 \left(\frac{C_1}{C_1 + C_2} V_0(kT + t_o) \right). \tag{9.15}$$

By subtracting the above relationship from itself at time increment $k - 1$, and substituting $V_0(kT + t_o) - V_0((k-1)T + t_o)$ with an equivalent integral expression, we obtain

$$Q_F[k] - Q_F[k-1] = \frac{C_2}{C_1 + C_2} \int_{(k-1)T+t_o}^{kT+t_o} (I_{IN}(t) - \hat{I}_F(t))dt. \tag{9.16}$$

The above relationship can be simplified by appealing to the decomposition of $I_{IN}(t)$ in Equation 9.2, and noting that

$$\int_{(k-1)T+t_o}^{kT+t_o} I_{spur}(t)dt = 0. \tag{9.17}$$

Substitution of Equations 9.14 and 9.17 into 9.16 yields

$$Q_F[k] - Q_F[k-1] = \frac{C_2}{C_1 + C_2} \int_{(k-1)T+t_o}^{kT+t_o} I_e(t)dt - \frac{C_2}{C_1 + C_2} Q_F[k-1]. \tag{9.18}$$

Evaluation of the integral of $I_e(t)$ in Equation 9.18 depends on the value of the sampling offset, t_o. Figure 9.16 illustrates the relevant signals involved; it is assumed in the drawing that the clk_1 switch is turned on when this signal is high. The value of t_o is discerned by the location of the impulses of $\hat{I}_F(t)$, which occur at the falling edges of clk_1. As depicted in the figure, two cases are encountered when choosing t_o. Case 1 corresponds to the placement of the $\hat{I}_F(t)$ impulses within the time span over which the pulses in $I_e(t)$ are modulated. Under Case 2 conditions, the $\hat{I}_F(t)$ impulses are placed outside of this modulation region. Evaluation of the integral relationship

in Equation 9.18 is greatly influenced according to which case is valid. For Case 2 conditions, we have

$$\int_{(k-1)T+t_o}^{kT+t_o} I_e(t)dt = Q_e[k]. \tag{9.19}$$

The above relationship does not hold in Case 1, however, since the integral will be effected by portions of $Q_e[k]$ and $Q_e[k-1]$. In the prototype, t_o was chosen to be zero so that *the Case 1 condition holds.*

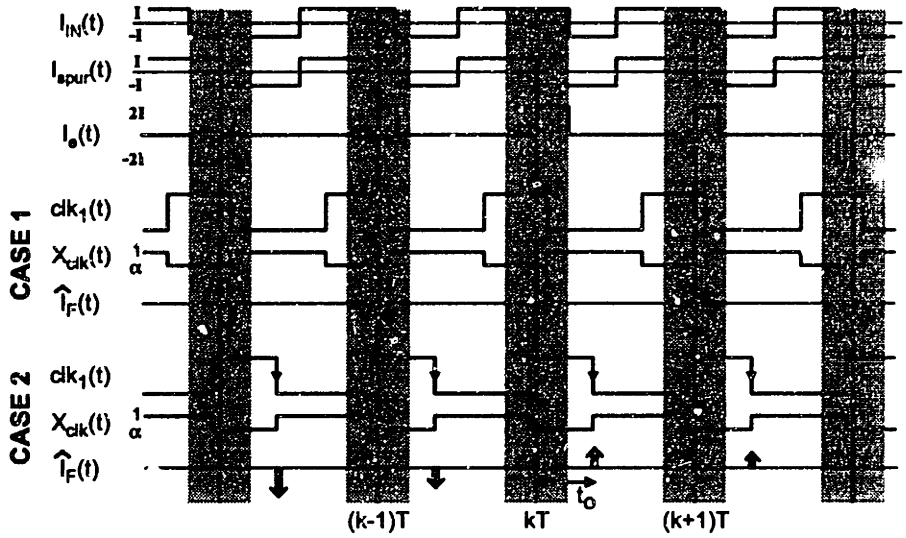


Figure 9.16: Example signals occurring in first order switched capacitor filter.

To provide a convenient notation for analysis of Case 1, we shall decompose $Q_e[k]$ into two parts. Specifically, we refer to $Q_L[k]$ and $Q_R[k]$ as the portions of $Q_e[k]$ that occur before and after t_o, respectively, so that

$$Q_e[k] = Q_L[k] + Q_R[k]. \tag{9.20}$$

Figure 9.17 uses shading to indicate the resulting decomposition for an arbitrary value of t_o under Case 1 conditions. The integral of $I_e(t)$ over the light shaded time region yields $Q_L[k]$, and its integral over the dark shaded region yields $Q_R[k]$. The value of $Q_R[k]$ can be described mathematically as

$$Q_R[k] = \begin{cases} Q_e[k] - 2It_o & \text{if } Q_e[k] \geq 2It_o, & t_o \geq 0 \\ Q_e[k] & \text{if } Q_e[k] \geq 0, & t_o < 0 \\ Q_e[k] & \text{if } 2It_o \leq Q_e[k] \leq 0, & t_o < 0 \\ 2It_o & \text{if } Q_e[k] \leq 2It_o, & t_o < 0 \\ 0 & \text{otherwise} \end{cases} \tag{9.21}$$

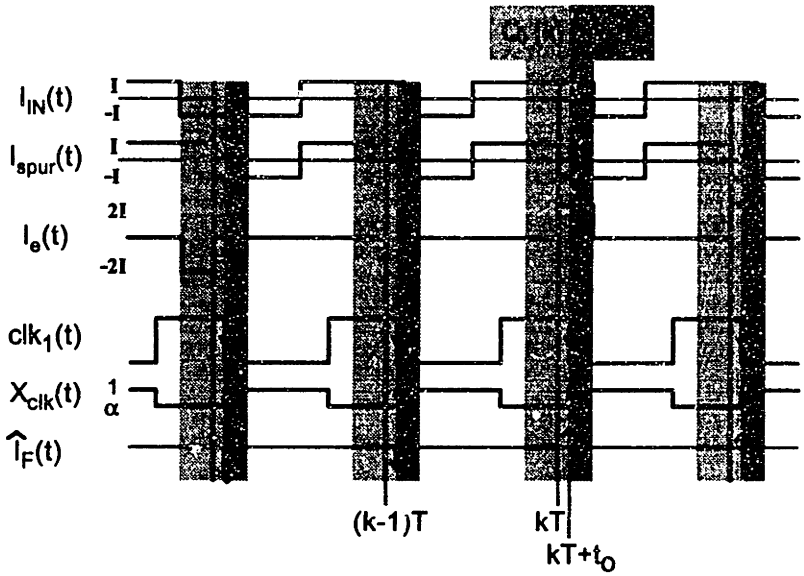


Figure 9.17: Definition of $Q_L[k]$ and $Q_R[k]$.

Given the above decomposition, Equation 9.18 is evaluated under Case 1 conditions as

$$Q_F[k] - \frac{C_1}{C_1 + C_2} Q_F[k-1] = \frac{C_2}{C_1 + C_2} \left(Q_R[k-1] + Q_L[k] \right). \tag{9.22}$$

Using Equation 9.20, we obtain

$$Q_F[k] - \frac{C_1}{C_1 + C_2} Q_F[k-1] = \frac{C_2}{C_1 + C_2} \left(Q_{IN}[k] - (Q_R[k] - Q_R[k-1]) \right). \tag{9.23}$$

The above expression extends to Case 2 by setting $Q_R[k]$ to zero for all k.

Inspection of Equation 9.23 reveals a significant fact — the value of the feedback charge $Q_F[k]$ is completely described by a discrete-time relationship involving $Q_e[k]$. As such, the switched capacitor circuit can be viewed as a continuous-time system that is fed with the signals shown in Figure 9.18. By assuming $I_e(t)$ is an impulse train with $t_o = 0$, and combining its charge with $\hat{I}_F(t)$, we approximate the summing current in Figure 9.18, $I_s(t)$, as

$$I_s(t) = \sum_{k=-\infty}^{\infty} Q_S[k] \delta(t - kT) + I_{spur}(t), \quad \text{where } Q_S[k] = Q_e[k] + Q_F[k]. \tag{9.24}$$

We are now in a position to derive the transfer function relationship between $\hat{\Phi}_e(t)$ and $V_1(t)$. This analysis will be done from a deterministic standpoint; $Q_e[k]$, $Q_R[k]$, and $Q_S[k]$ will be assumed to have nonzero Z-transforms. This being said, we begin

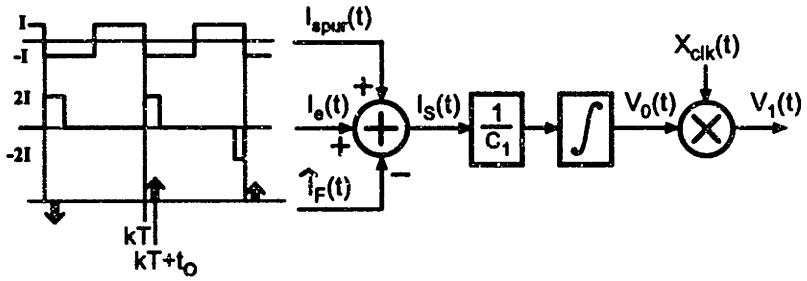


Figure 9.18: Signals associated with switched capacitor filter.

by taking the Z-transform of Equation 9.23 to obtain

$$Q_F(z) = \frac{C_2}{C_1 + C_2}\left(\frac{1}{1 - \frac{C_1}{C_1+C_2}z^{-1}}\right)\left(Q_e(z) - (1 - z^{-1})Q_R(z)\right). \tag{9.25}$$

Given the definition of $Q_S[k]$ in Equation 9.24, we then find that

$$Q_S(z) = \frac{1}{C_1 + C_2}\left(\frac{1 - z^{-1}}{1 - \frac{C_1}{C_1+C_2}z^{-1}}\right)\left(C_1 Q_e(z) + C_2 Q_R(z)\right). \tag{9.26}$$

Figure 9.19 shows the resulting transfer function relationship, where Equation 9.5 was used to relate $Q_e[k]$ to $\Phi_e[k]$. This derivation assumes $V_1 \approx V_0$, which is an accurate approximation in the prototype since $C_1/(C_1 + C_2)$ is very close to one.

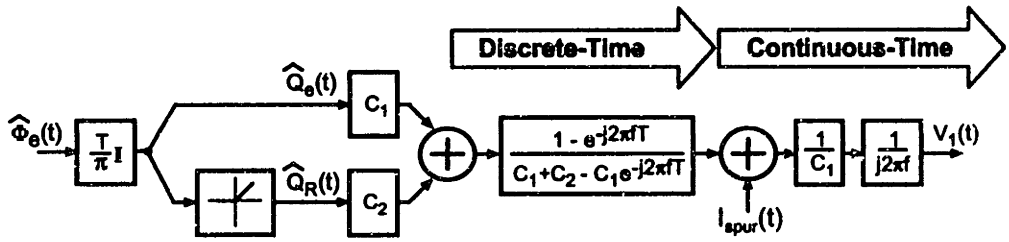


Figure 9.19: Frequency domain view of switched capacitor filter, PFD, and charge pump assuming the pulse widths in $I_e(t)$ are small and $t_o = 0$.

9.2.2 Integrating Section

Figure 9.20 displays the remaining portion of the loop filter that must be included in our modeling effort. Here we have defined

$$\tilde{V}_1(t) = V_1(t) + V_{ref}, \tag{9.27}$$

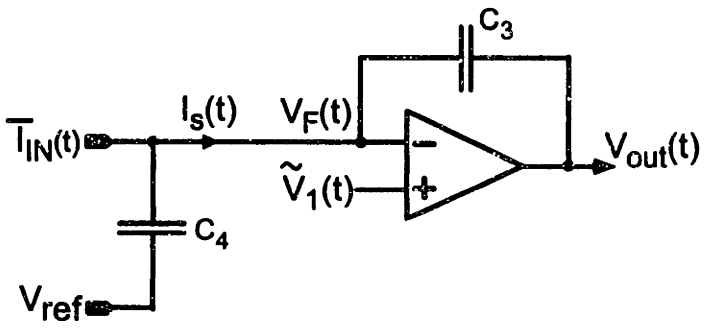


Figure 9.20: Integrating portion of loop filter.

which corresponds to the output voltage of the switched capacitor network.

Our first step will be to derive the relationship between $\bar{I}_{IN}(t)$, $\tilde{V}_1(t)$, and $V_{out}(t)$. Using the voltage and current variables defined in Figure 9.20, we write

$$V_{out}(t) = -\frac{1}{C_3}\int_{-\infty}^{t} I_S(\tau)d\tau + V_F(t). \tag{9.28}$$

The relationship between $I_S(t)$ and $\bar{I}_{IN}(t)$ is given as

$$I_S(t) = \bar{I}_{IN}(t) - C_4\frac{dV_F(t)}{dt}. \tag{9.29}$$

Substitution of Equation 9.29 into 9.28 leads to

$$V_{out}(t) = -\frac{1}{C_3}\int_{-\infty}^{t} \bar{I}_{IN}(\tau)d\tau + \left(1 + \frac{C_4}{C_3}\right)\tilde{V}_1(t), \tag{9.30}$$

where it has been assumed that $V_F(t) = \tilde{V}_1(t)$ due to the action of the opamp. Figure 9.21 depicts this relationship in graphical form, from which we see that the output of the overall filter is given as the sum of $\tilde{V}_1(t)$ and the integral of $\bar{I}_e(t)$ and $\bar{I}_{spur}(t)$.

The transfer function relationship between $\hat{\Phi}_e(t)$, $\tilde{V}_1(t)$, and $V_{out}(t)$ is shown in Figure 9.22. The derivation of this figure follows from Figure 9.21, the relationship $\bar{I}_{IN}(t) = -I_{IN}(t)$, and Equation 9.5.

9.2.3 Overall Model

Figure 9.23 depicts the overall model of the loop filter based on those in Figures 9.19 and 9.22. In obtaining its derivation, the impact of the V_{ref} term within $\tilde{V}_1(t)$ was ignored since $V_{out}(t)$ can assume an arbitrary DC level due to the integrating action of the loop filter.

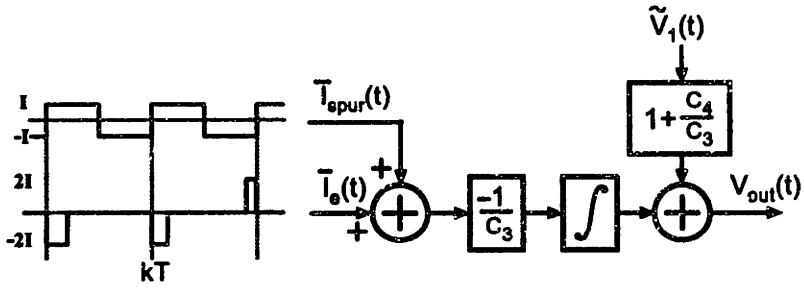


Figure 9.21: Signals associated with integrating portion of loop filter.

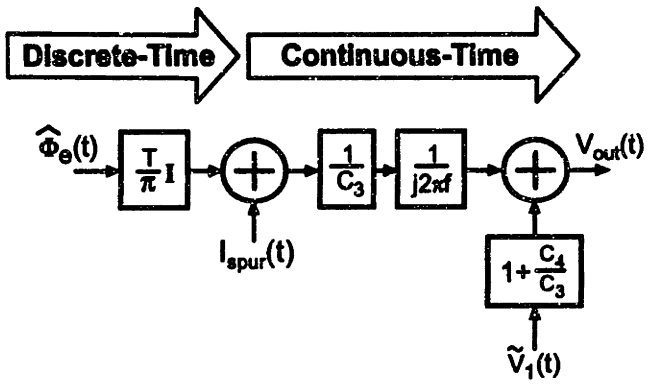


Figure 9.22: Frequency domain model of integrating portion of loop filter, PFD, and charge pump assuming the pulse widths in $I_e(t)$ are small and $t_o = 0$.

We define the transfer function from $\hat{Q}_e(t)$ to $V_{out}(t)$ in Figure 9.23 to be $(1/I)H_d(f)$;

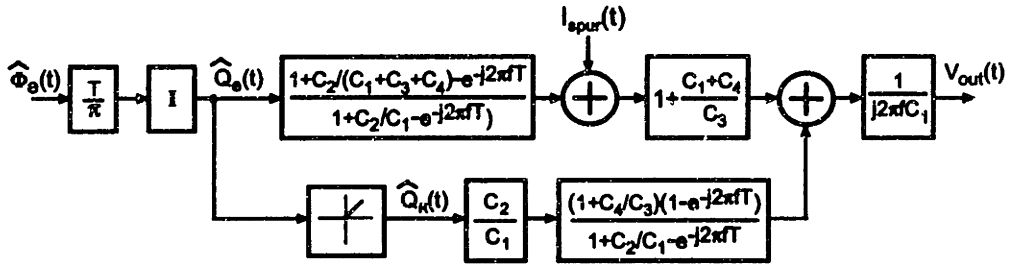


Figure 9.23: Overall model of PFD, charge pump, and loop filter assuming the pulse widths of $I_e(t)$ are small and $t_o = 0$.

calculation of this function follows directly from the figure as

$$H_D(f) = I\frac{C_1 + C_2 + C_3 + C_4 - (C_1 + C_3 + C_4)e^{-j2\pi fT}}{j2\pi fC_3(C_1 + C_2 - C_1e^{-j2\pi fT})}. \tag{9.31}$$

The continuous-time approximation of the loop filter dynamics, $H(f)$, that is expressed in Equation 9.11 is derived from the above equation by substituting

$$e^{-j2\pi fT} \approx 1 - j2\pi fT. \tag{9.32}$$

The above approximation is accurate at frequencies much less than $1/T$. Finally, we define the transfer function from $\hat{Q}_R(t)$ to $V_{out}(t)$ to be $(1/I)H_R(f)$, and calculate its value as

$$H_R(f) = I\frac{(C_2/C_1)(C_3 + C_4)(1 - e^{-j2\pi fT})}{j2\pi fC_3(C_1 + C_2 - C_1e^{-j2\pi fT})}. \tag{9.33}$$

Figure 9.24 displays the relative magnitudes of $H(f)$, $H_D(f)$, and $H_R(f)$ for the capacitor values denoted in Figure 9.9. The figure reveals a very close between match between $|H(f)|$ and $|H_D(f)|$, and a relatively low magnitude for $|H_R(f)|$. Figure 9.25 compares $H(f)$ and $H_D(f)$ in more detail, and shows that the magnitude and phase difference between these two transfer functions is negligible to frequencies as high as 10 MHz. The low relative magnitude of $H_R(f)$ hints that the undesirable production of $Q_R[k]$ under Case 1 conditions has little consequence on the performance of the filter. This fact is confirmed by simulations shown in Chapter 11.

9.3 The Impact of Large Pulse Widths in $I_e(t)$

The loop filter model was derived on the assumption that the pulse widths in $I_e(t)$ are small, which allowed this signal to be approximated as an impulse train. But what does 'small' mean, and what are the consequences of violating this assumption? Unfortunately, the answer to these questions is difficult to ascertain in an analytical fashion. Our recourse is to appeal to the computer, and *simulate* the effect of such conditions. In this section, we will limit our focus to the effects of non-negligible pulse widths on the power spectrum of $I_{IN}(t)$. Simulated results in Chapter 11 will show the influence of this condition on the transmitter output spectrum.

In choosing our experiment for simulation, we will limit ourselves to a case that is immediately relevant — modulation of the duty cycle of $I_{IN}(t)$ to achieve 2.5 Mbit/s data transfer using GFSK. All simulations are performed with custom software written in the C programming language.

The simulated power spectrum of $I_{IN}(t)$ contains spurs with a fundamental frequency of 2.5 Mbit/s that are produced as a result of the pulse width modulation of $I_{IN}(t)$. A proof of the existence of these spurs will given in order to explain their appearance.

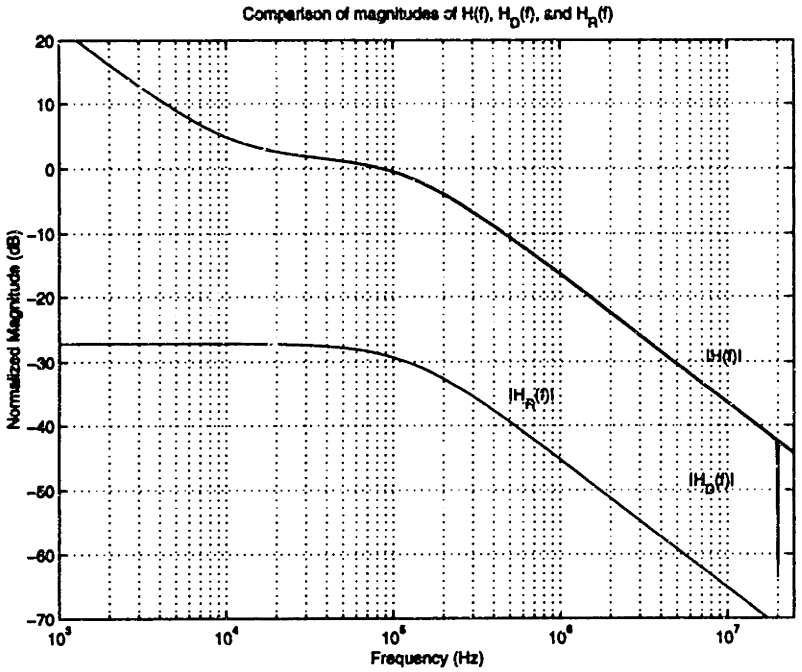


Figure 9.24: Comparison of $|H(f)|$, $|H_D(f)|$, and $|H_R(f)|$ (scale is normalized).

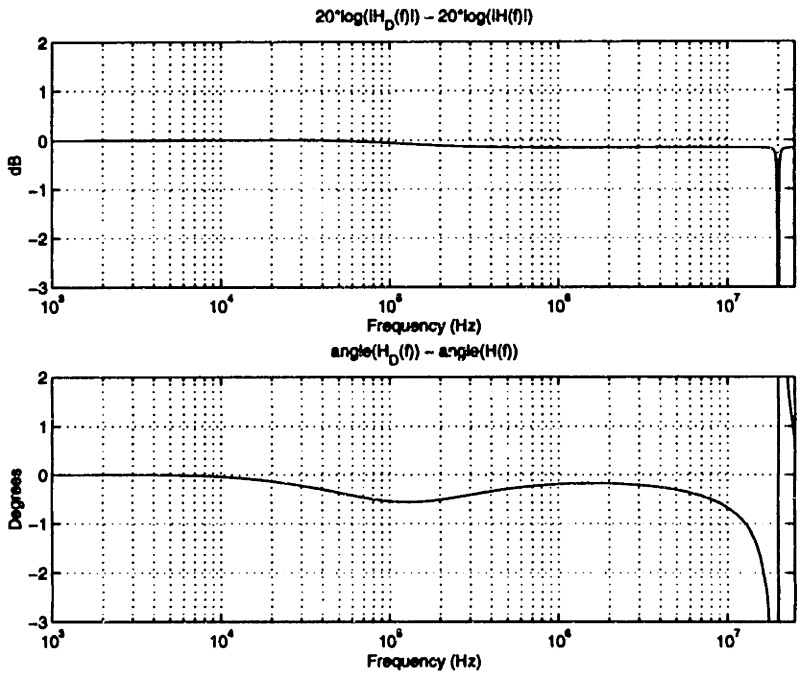


Figure 9.25: Comparison of the magnitude and phase of $H(f)$ and $H_D(f)$.

9.3.1 Examination of Power Spectrum of $I_{IN}(t)$ at 2.5 Mbit/s

We now compare the power spectrum of $I_{IN}(t)$ to the power spectrum of its approximate formulation when $I_e(t)$ is treated as a modulated impulse train.

For clarity, we begin by describing the signals of interest. Referring back to Figure 9.13, we restate the fact that $I_{IN}(t)$ can be *exactly* decomposed as

$$I_{IN}(t) = I_e(t) + I_{spur}(t). \tag{9.34}$$

$I_e(t)$ is described mathematically as

$$I_e(t) = 2I \sum_{k=-N}^{N} \text{rect}\left(t - kT, \frac{T}{2\pi}\Phi_e[k]\right), \tag{9.35}$$

where $\Phi_e[k]$ represents the instantaneous phase error between *Div* and *Ref* at sample period k of the reference clock, and $\text{rect}(a, b)$ is defined to be

$$\text{rect}(a,b) = \begin{cases} 1, & 0 \le a < |b| \quad \text{for } b \ge 0, \\ -1, & |b| \le a < 0 \quad \text{for } b < 0, \\ 0, & \text{otherwise.} \end{cases} \tag{9.36}$$

The approximation of $I_e(t)$ as an impulse train yields the expression

$$I_e(t) \approx 2I \sum_{k=-N}^{N} \frac{T}{2\pi}\Phi_e[k]\delta(t - kT). \tag{9.37}$$

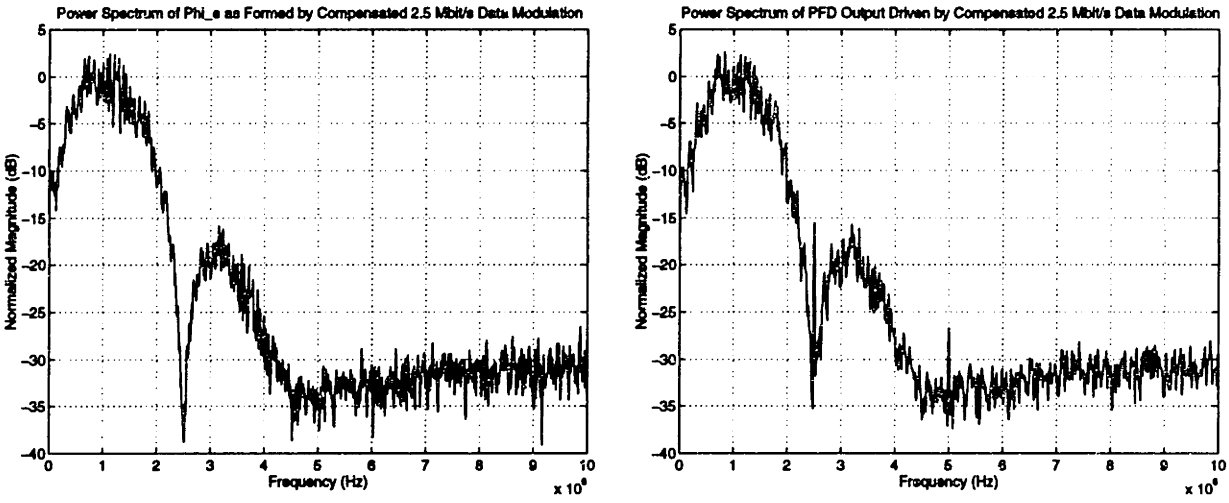
In effect, $I_e(t)$ ideally sends *samples* of the phase error to the loop filter (Equation 9.37), but is limited by practical considerations to sending pulses to the loop filter whose *width* is controlled by the phase error (Equation 9.35). A last signal of interest is $\hat{\Phi}_e(t)$, which is defined to be an impulse train that is modulated by samples of the phase error:

$$\hat{\Phi}_e(t) = \sum_{k=-\infty}^{\infty} \Phi_e[k]\delta(t - kT). \tag{9.38}$$

A useful method of evaluating the effect of non-negligible pulse widths on the loop filter analysis is to compare the power spectra of $I_{IN}(t)$ and $\hat{\Phi}_e(t)$ under such conditions. To do so, a comprehensive C simulation was performed of the entire PLL with its instantaneous divide value modulated to achieve a 2.5 Mbit/s GFSK data rate. The compensation method described in this thesis was employed to achieve this high data rate, and the resulting pulse width variation in $I_e(t)$ was approximately thirty percent of the period, T. In the simulation, the PLL was chosen to have 84 kHz bandwidth, $1/T$ was set to 20 MHz, and the loop filter was implemented as an ideal filter with transfer function:

$$H(f) = K_l \frac{1 + jf/(11\text{kHz})}{jf(1 + jf/(127\text{kHz}))}.$$

Also, the simulation included no noise sources other than the quantization noise inherent to using a second order MASH Σ-Δ converter. Figure 9.26 illustrates the resulting power spectra at frequencies less than $1/(2T)$, and demonstrates that there is a close correspondence between the spectra of $I_{IN}(t)$ and $\hat{\Phi}_e(t)$. (Note that the absolute value of the peak spectra magnitude has been normalized to 0 dB in both cases.) The only discernable difference in the spectra is the appearance of a small amount of spurious content in $I_{IN}(t)$ at multiples of the symbol rate, 2.5 MHz. As shown by simulation in Chapter 11, these spurs have negligible impact on the performance of the transmitter since they are convolved with the modulation signal at its output (and thus turned into phase noise of low density).



(a) (b)

Figure 9.26: Power spectra of (a) $\hat{\Phi}_e(t)$ and (b) $I_{IN}(t)$ under 2.5 Mbit/s GFSK modulation.

Additional differences between $I_{IN}(t)$ and $\hat{\Phi}_e(t)$ are observed by comparing their spectra at higher frequencies. Since $\hat{\Phi}_e(t)$ is constructed with discrete-time samples, its power spectrum must consist of replicas, spaced $1/T$ apart in frequency, of the density graph shown in Figure 9.26(a). Using the same C simulation described above; Figure 9.27 displays the spectrum of $I_{IN}(t)$ out to 50 MHz. As the figure reveals, the power spectrum of $I_{IN}(t)$ is not quite periodic; subtle differences are seen between its density at baseband and the 'pseudo' replicas at multiples of $1/T$. Fortunately, the differences are inconsequential in light of the attenuation of the high frequency components of $I_{IN}(t)$ imposed by the loop filter, VCO, and the output bandpass filter of the transmitter.

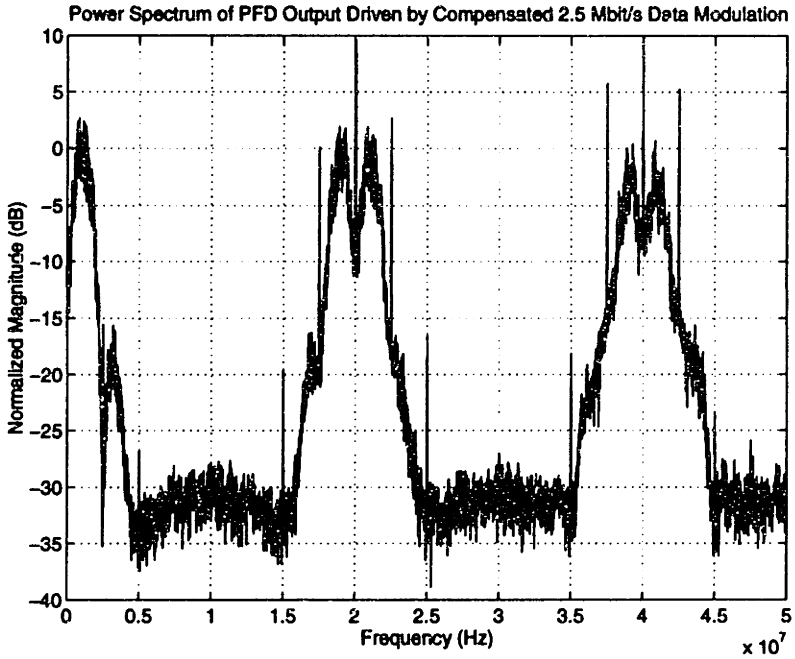


Figure 9.27: Power spectrum of $I_{IN}(t)$ at high frequencies.

9.3.2 Explanation for Existence of Spurs at Multiples of $1/T_d$

Simulations reveal that duty cycle modulation of the PFD output, $E(t)$, causes spurs in its output spectrum spaced at multiples of the data rate, $1/T_d$, in frequency. The source of these spurs will now be explained by providing a proof of their existence; it will be assumed that GFSK modulation with $BT_d = 0.5$ is performed.

Our first step is to examine the structure of the PFD output, $E(t)$ under the given modulation conditions. In any given symbol period k, whose length is T_d, the duty cycle variation of $E(t)$ takes on one of eight possible paths since it is affected by data symbols at time $k-1$, k, and $k+1$ (see [22] for details). Quantization noise from the Σ-Δ modulator, along with other noise sources in the PLL, causes random deviations in the instantaneous duty cycle of $E(t)$ about the path set by the modulation data. Therefore, we can construct the PFD output as

$$E(t) = \sum_{k=-\infty}^{\infty} h(m[k], v[k], t - kT_d), \tag{9.39}$$

where $h(m[k], v[k], t)$ is the PFD waveform associated with modulation signal $m[k]$ and noise signal $v[k]$; $h(m[k], t)$ is nonzero only for $0 \leq t < T_d$. By definition, $m[k] \in \{1, \cdots, 8\}$ for all k, and is set according to data bits at time $k-1$, k, and $k+1$. When considering only Σ-Δ quantization noise, $v[k] \in \{1, \cdots, p\}$ for all k, where p is the number of combinations possible for the Σ-Δ quantization noise samples in

the time span T_d. The influence of other noise sources is incorporated into $v[k]$ in an approximate manner by quantizing their values and mapping the resulting combinations to values in $v[k]$, which requires that p be increased.

Given $E(t)$ as described in Equation 9.39, the autocorrelation of $E(t)$ is computed as

$$R_{EE}(t,\tau) = \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} E\left(h(m[k], v[k], t - kT_d)h(m[n], v[n], t - nT_d + \tau)\right). \quad (9.40)$$

$E(t)$ is a cyclostationary process since

$$R_{EE}(t + T_d, \tau) = R_{EE}(t, \tau).$$

To achieve a wide-sense stationary process, we define

$$E'(t) = E(t + \theta),$$

where θ is a random phase epoch [69] that is uniformly distributed on $[0, T_d]$ and independent of $m[k]$ and $v[k]$. The autocorrelation of $E'(t)$ is computed as

$$R_{E'E'}(t,\tau) = \frac{1}{T_d} \int_0^{T_d} R_{EE}(t + \theta, \tau) d\theta;$$

this expression is independent of t due to the fact that $R_{EE}(t + T_d, \tau) = R_{EE}(t, \tau)$. Therefore, $R_{E'E'}(t,\tau)$ can be expressed as $R_{E'E'}(\tau)$ and computed at $t = 0$ as

$$R_{E'E'}(\tau) = \frac{1}{T_d} \int_0^{T_d} R_{EE}(\theta, \tau) d\theta;$$

A more useful form of $R_{E'E'}(\tau)$ can be derived at large values of τ. Under this condition, Equation 9.40 can be written as

$$R_{E'E'}(\tau) = \frac{1}{T_d} \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \int_0^{T_d} E(h(m[k], v[k], \theta - kT_d))E(h(m[n], v[n], \theta - nT_d + \tau)) \quad (9.41)$$

under the assumption that $m[k]$ and $v[k]$ are independent of $m[n]$ and $v[n]$ for $|k-n| \gg 0$. The statistics of $m[k]$ and $v[k]$ are assumed to be the same for all k; we define

$$g(t) = E(h(m[k], v[k], t))$$

for some arbitrary value of k, and rewrite Equation 9.41 as

$$R_{E'E'}(\tau) = \frac{1}{T_d} \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \int_0^{T_d} g(\theta - kT_d)g(\theta - nT_d + \tau)d\theta, \quad |\tau| \gg 0. \quad (9.42)$$

Since $g(t)$ is nonzero only for $0 \leq t < T_d$, we obtain

$$R_{E'E'}(\tau) = \frac{1}{T_d} \int_0^{T_d} g(\theta) \left(\sum_{n=-\infty}^{\infty} g(\theta - nT_d + \tau) \right) d\theta, \quad |\tau| \gg 0. \tag{9.43}$$

To prove that spurs occur in $E'(t)$ with a fundamental frequency $1/T_d$, we must show that

$$R_{E'E'}(\tau) = R_{E'E'}(\tau + T_p) \text{ as } \tau \longrightarrow \infty, \tag{9.44}$$

for $T_p = T_d$, but not for $T_p < T_d$. By inspection of Equation 9.43,

$$R_{E'E'}(\tau + T_p) = R_{E'E'}(\tau) \tag{9.45}$$

for $T_p = T_d$, which essentially completes the proof.

It remains only to rule out the possibility that Equation 9.44 holds for $T_p < T_d$. To prove this, we express Equation 9.43 as an inner product

$$R_{E'E'}(\tau) = g(\theta) \cdot \left(\sum_{n=-\infty}^{\infty} g(\theta - nT_d + \tau) \right), \quad \theta \in [0, T_d].$$

and note, by the Cauchy-Schwartz inequality, that

$$R_{E'E'}(\tau) < R_{E'E'}(iT_d), \quad \forall \theta \in (0, T_d) \tag{9.46}$$

for all integers i under the condition that

$$\sum_{n=-\infty}^{\infty} g(\theta - nT_d + \tau) \neq \sum_{n=-\infty}^{\infty} g(\theta - nT_d) \text{ for } \forall \tau \in (0, T_d). \tag{9.47}$$

If Equation 9.46 holds, Equation 9.44 cannot be true for $T_p < T_d$.

To show that Equation 9.46 is valid, we verify the condition stated in Equation 9.47. Figure 9.28 displays $g(t)$ as computed by simulation under 2.5 Mbit/s GFSK modulation with $BT_d = 0.5$; the effects of Σ-Δ quantization noise, charge pump noise, and VCO noise were all included in the simulation. Inspection of the figure reveals that Equation 9.47 is indeed satisfied.

9.4 Summary

This chapter presented implementation and modeling details of the variable gain loop filter used in the prototype. Circuit details were given of the PFD, charge pump, loop filter, and D/A converter used in this structure. A frequency-domain model of this block was derived under the assumption of small duty cycle variation. Simulations were presented that show that the effect of large duty cycle variation is to produce spurs at multiples of the data rate frequency. Fortunately, as will be seen in Chapter 11, these spurs are convolved with the modulation data, and therefore turned into phase noise, before affecting the transmitter output.

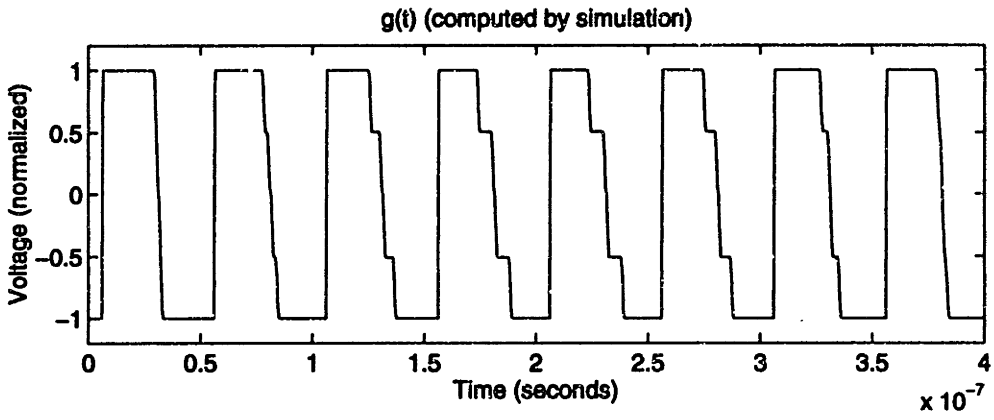


Figure 9.28: Computed value of $g(t)$ from simulation data.

Chapter 10

Prototype System

This chapter describes the design and implementation of a prototype system built to provide proof of concept of the compensation method; the system supports data rates in excess of 2.5 Mbit/s with a PLL bandwidth of 84 kHz. A 64 modulus divider and 6 output bit Σ-Δ modulator provide a wide dynamic range path for the modulation signal, and an on-chip loop filter allows an accurate PLL transfer function to be achieved by tuning just one PLL parameter — the open loop gain.

We begin by discussing implementation details and providing measured values of the power dissipation of key circuits. A linearized model of the system is then presented, followed by the design strategy used to set the relevant PLL parameters. Finally, a detailed noise analysis of the system is given at the end of the chapter.

10.1 Implementation

Figure 10.1 displays a block diagram of the prototype; at the heart of this system is a custom, CMOS fractional-N synthesizer IC that includes the key circuits discussed in earlier chapters of this thesis. The on-chip loop filter requires no tuning or external components to set its time constants, the digital MASH Σ-Δ modulator achieves low power operation through pipelining, and the asynchronous, 64 modulus divider supports any divide value between 32 and 63.5 in half cycle increments. An external divide-by-2 prescaler is used so that the CMOS divider input operates at half the VCO frequency, which modifies the range of divide values to include all integers between 64 and 127. Also, a digital 32K FIFO buffer is used in conjunction with a computer to provide the digital modulation stream that is fed into the input of the Σ-Δ modulator.

Figure 10.2 displays a die photograph of the custom IC, which was fabricated in a 0.6 micron, double poly, double metal, CMOS process with threshold voltages of $V_{tn} = 0.75V$ and $V_{tp} = -0.88V$. The entire die is 3 mm by 3 mm.

The overall power dissipation of the custom IC is 27 mW. Table 10.1 lists the

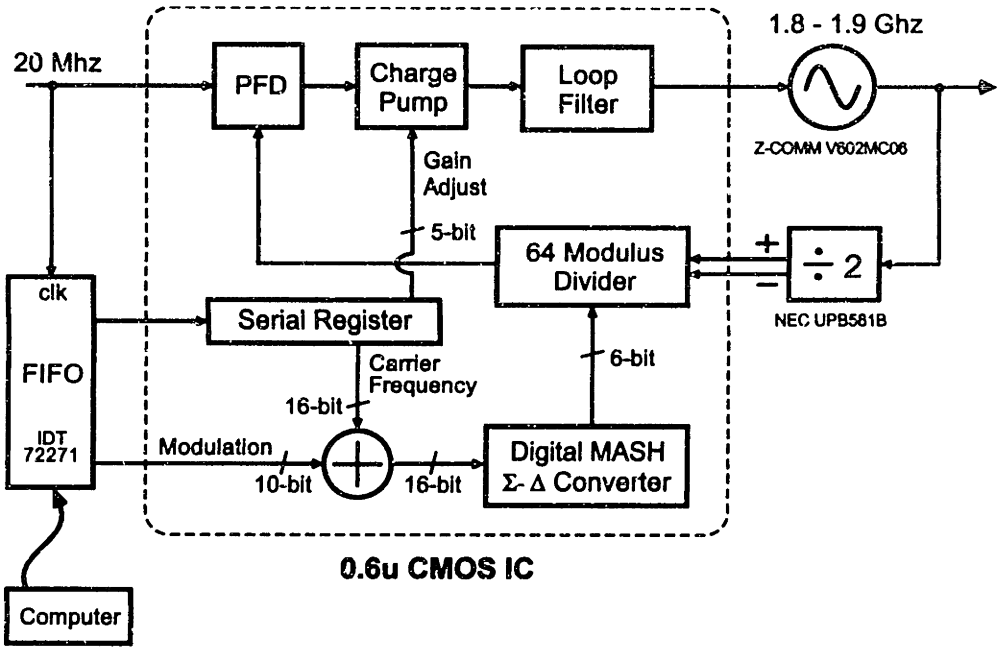


Figure 10.1: Block diagram of prototype system.

power consumed by individual circuits. The supply voltages of each component were set as low as possible to minimize their power dissipation. At the cost of higher power dissipation, all circuits could be powered by a single 3.3 Volt supply.

Component	Divider	Filter	Σ-Δ	Other
Power	22 mW	2.5 mW	0.33 mW	2.4 mW
Supply Voltage	3 V	3.3 V	1.25 V	3.3 V

Table 10.1
Power dissipation of IC circuits.

10.2 Linearized Model

A linearized, frequency-domain model of the prototype system is shown in Figure 10.3. The open loop transfer function of the system consists of two poles at zero frequency, a pole at f_p, and a zero at f_z. Additional poles and zeros occur are present in the system due to the effects of finite opamp bandwidth and other nonidealities; care was taken to insure that these additional poles and zeros occur at high frequencies and therefore have little interaction with the modulation data. Although they will be

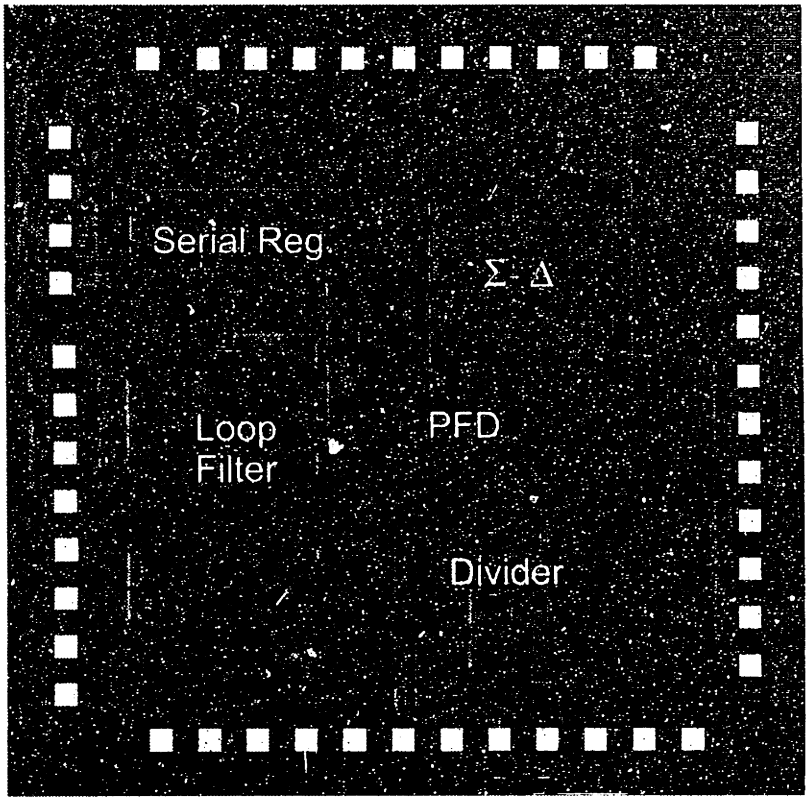


Figure 10.2: Die photo of custom IC used in the prototype.

ignored in the analysis to follow, their influence will be seen at high frequencies (i.e., $f > 6$ MHz) in measured noise plots of the system presented in Chapter 11.

The closed loop pole locations for the system are displayed in the root locus diagram shown in Figure 10.4. The diagram reveals that appropriate adjustment of the open loop gain of the PLL leads to a complex conjugate pair of poles with natural frequency f_o, and a real valued pole f_{cp}. The closed loop transfer function between the divider input and the transmitter output contains a zero, f_z, that largely cancels the effect of f_{cp}.

10.3 Selection of Parameters

The compensation approach presented in this thesis allows the PLL bandwidth to be set well below that of the modulation data, thereby allowing the PLL transfer function to be set according to noise requirements. For all calculations in this chapter, the PLL transfer function will be defined as $G(f)$ and is related to the PLL parameters

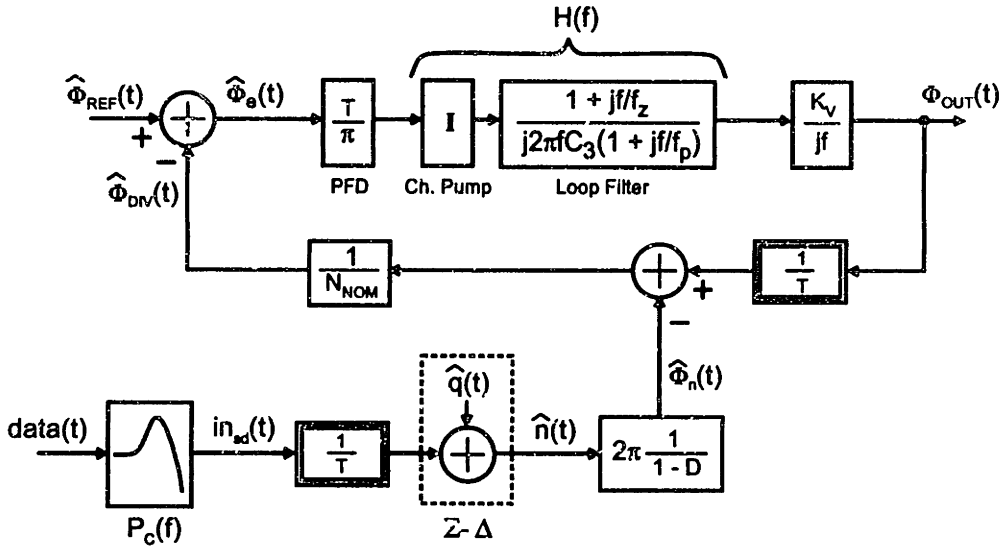


Figure 10.3: Linearized, frequency-domain model of prototype system.

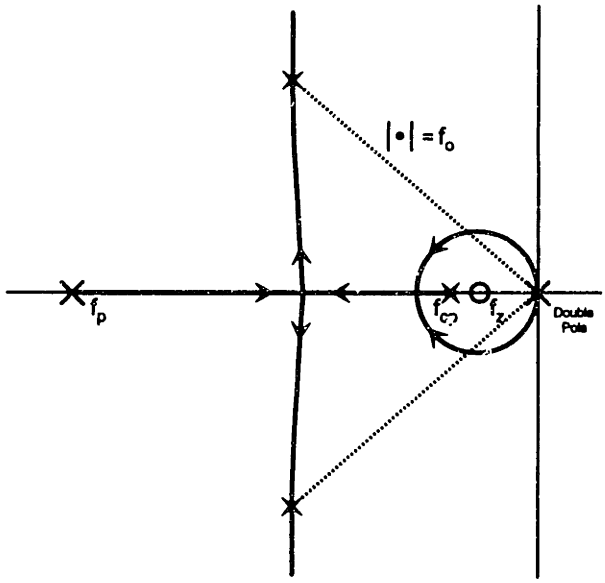


Figure 10.4: Root locus of PLL.

as

$$G(f) = \frac{H(f)K_v/(\pi N_{nom})}{jf + H(f)K_v/(\pi N_{nom})}, \tag{10.1}$$

where $H(f)$ is the loop filter transfer function

$$H(f) = I\frac{1 + f/f_z}{(j2\pi f C_3)(1 + jf/f_p)}. \tag{10.2}$$

The above parameterization of $H(f)$ allows us to express $G(f)$ as

$$G(f) = \frac{1 + jf/f_z}{1 + jf/f_{cp}}\left(\frac{1}{1 + \frac{1}{f_o Q}jf + \frac{1}{f_o^2}(jf)^2}\right). \tag{10.3}$$

To obtain a parameterization of $G(f)$ that achieves the required noise specification, we must select an appropriate value of f_o. The value of f_o, in turn, should be set according to the order of the PLL, n, and the value of the reference frequency, $1/T$.

To achieve a low power transmitter design, it is desirable to choose low values for $1/T$ and n. The selection of $1/T$ is constrained to be higher than the bandwidth of the output bandpass filter of the transmitter so that this filter attenuates the effects of the reference frequency. We will assume that the bandwidth of the output bandpass filter is on the order of 15 MHz, so that a choice of $1/T = 20$ MHz seems appropriate. The choice of $n = 2$ leads to a simple PLL implementation.

Given the above choices for $1/T$ and n, we select $f_o = 84$ kHz based on the plots in Figure 3.4 of Chapter 3. This parameter combination would set $S_{\Phi_{tn,q}}(f)$ equal to -136 dBc/Hz at $f = 5$ MHz if $G(f)$ were a Butterworth filter. As discussed in Chapter 6, $S_{\Phi_{out,q}}(f)$ will be slightly higher than this value in the prototype system due to the parasitic pole/zero pair, f_{cp} and f_z, that occurs. It will be shown later in this chapter that $f_{cp}/f_z = 1.22$ for $f_o = 84$ kHz, $1/T = 20$ MHz, and $n = 2$, which leads to $S_{\Phi tn,q}(f)$ = -134.3 dBc/Hz at $f = 5$ MHz for this parameter combination. This noise specification is sufficiently low to insure that the Σ-Δ induced noise does not present a bottleneck in achieving overall transmitter noise that is less than -131 dBc/Hz at 5 MHz offset. Of course, the VCO must be designed to have adequately low phase noise spectral density to achieve this overall noise specification.

The values of open loop gain, K, and pole/zero frequencies, f_p and f_z, that achieve $f_o = 84$ kHz were calculated with MATLAB and are displayed in Table 10.2. Note that the open loop gain is defined in terms of parameters in Figure 10.3 as

$$K = \frac{2IK_v}{C_3 N_{nom}}. \tag{10.4}$$

These open loop settings lead to a closed loop PLL transfer function, as described by Equation 10.3, with parameter values of

$$f_z = 11.6 \text{ kHz}, f_p = 127 \text{ kHz}, f_{cp} = 14.2 \text{ kHz}, f_o = 84.3 \text{ kHz}, Q = 0.75. \tag{10.5}$$

Parameter	K	f_p	f_z
Value	32.6e9	127.2 kHz	11.6 kHz

Table 10.2
Open loop parameter settings in PLL that achieve a closed loop response with $f_o =$ 84 kHz.

The VCO gain, charge pump current, and capacitor values must be appropriately set within the loop filter to obtain the open loop parameters specified in Table 10.2. Figure 10.5 expands the block diagram of the prototype to indicate the parameters of interest, and includes significant sources of noise that will be used to calculate the noise performance of the transmitter. Drawing from Chapter 9, f_p and f_z are related to the parameters in Figure 10.5 by the following expressions:

$$\begin{aligned} f_p &= 1/(2\pi C_1(T/C_2)), \\ f_z &= 1/(2\pi(C_3 + C_1 + C_4)T/C_2). \end{aligned} \tag{10.6}$$

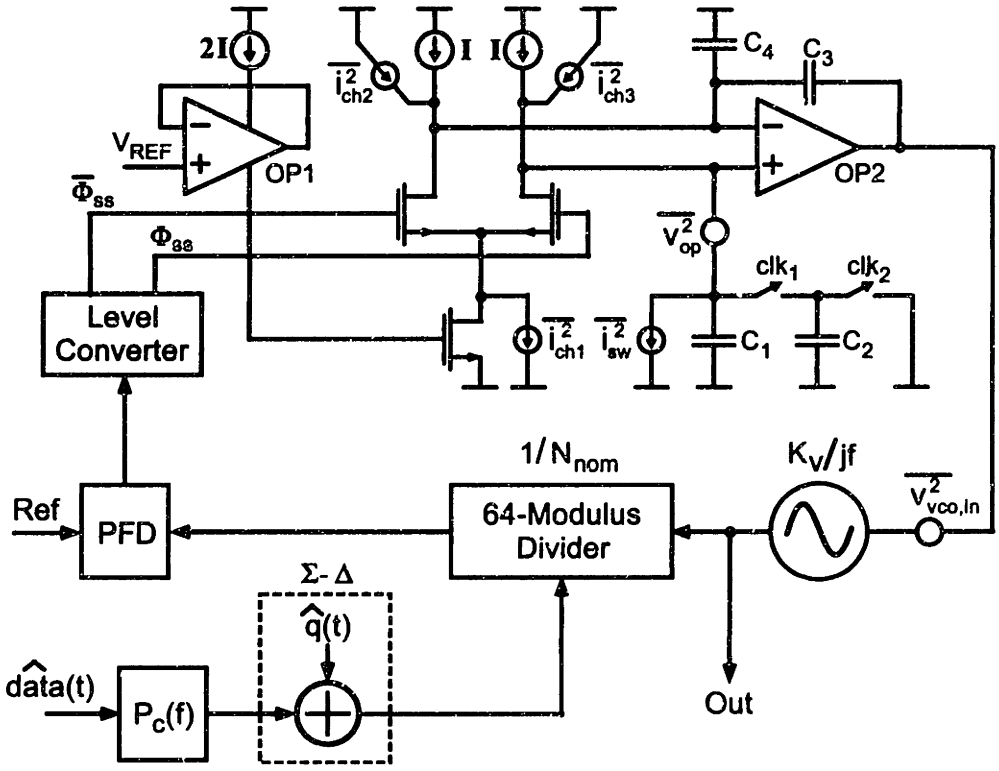


Figure 10.5: Expanded View of PLL System.

Table 10.3 displays parameter settings that achieve the desired values of K, f_p, and f_z. Their derivation follows from a few key pieces of information. First, a

reference frequency, $1/T$, of 20 MHz is assumed, which leads to $N_{nom} = 92$ to achieve an output carrier frequency of 1.84 GHz. The value of K_v is 30 MHz/V since a Z-COMM V602MC06 part was used to implement the VCO. A large value of C_3 is desirable to obtain good noise performance, but its value cannot be made much higher than 30 pF due to area constraints on the die of the custom IC.

Parameter	Value	Parameter	Value
C_1	3 pF	C_2	120 fF
C_3	30 pF	C_4	3 pF
I	1.5 uA	T	1/(20 MHz)
K_v	30 MHz/V	N_{nom}	92

Table 10.3
Component values for prototype system.

The final step in design of the frequency synthesizer is to insure that nonideal effects of OP1 and OP2 do not significantly affect the modulation data as it passes through the PLL transfer function. Aside from issues described in Chapter 9, the primary objective in designing OP1 and OP2 is to insure a high unity gain bandwidth relative to the modulation bandwidth. (Note that the feedback ratio of each opamp is very close to unity.) Table 10.4 lists the relevant specifications in the prototype. In the case of OP1, a bandwidth of 7 MHz is adequately fast to allow excellent tracking between the tail current of the charge pump and its top currents. The choice of 6 MHz for OP2 allows data rates as high as 2.85 Mbit/s to be achieved without distortion by its dynamics. The limited bandwidth of OP2 has the benefit of increasing the attenuation of noise produced by the Σ-Δ modulator and charge pump/loop filter circuitry at high frequencies.

Parameter	OP1 Value	OP2 Value
Open Loop Gain	83 dB	86 dB
Unity Gain Bandwidth	7 MHz	6 MHz
Phase Margin	80 degrees	72 degrees

Table 10.4
Simulated opamp specifications.

10.4 Noise Calculations

Table 10.5 displays the value of each noise source shown in Figure 10.5. Many of these values were obtained through AC simulation of the relevant circuits in HSPICE. Note

that all noise sources other than $\hat{q}(t)$ are assumed to be white, so that the values of their variance suffice for their description. This assumption holds for the VCO provided that its output phase noise rolls off at -20 dB/dec as predicted by Leeson's model [62,63]; the -20 dB/dec rolloff is achieved in the model since $v_{vco,in}(t)$, which has a flat spectral density, passes through the integrating action of the VCO. As will be seen in measured data in Chapter 11, the actual VCO doesn't quite follow Leeson's model, but is close enough that calculations and measured results agree well at the intermediate frequency offsets of interest.

Noise Source	Origin	Nature	Calculation	Value
$\overline{i^2_{ch1}}$	Ch. Pump, OP1	CT	HSPICE	1.2E-24 A^2/Hz
$\overline{i^2_{ch2}}$, $\overline{i^2_{ch3}}$	Ch. Pump	CT	HSPICE	1.8E-25 A^2/Hz
$\overline{i^2_{sw}}$	Switched Cap	DT	Equation 10.8	1.0E-26 A^2/Hz
$\overline{v^2_{op}}$	OP2	CT	HSPICE	1.85E-16 V^2/Hz
$\overline{v^2_{vco,in}}$	VCO	CT	Equation 10.7	1.4E-16 V^2/Hz
$\hat{q}(t)$	Σ-Δ	DT	Equation 10.9	—

Table 10.5
Values of noise sources within PLL.

The input referred noise of the VCO was calculated from open loop phase noise measurements of the VCO and the expression

$$10\log(\overline{v^2_{vco,in}}\,|K_v/(jf)|^2) = \text{-143 dBc/Hz at } f = 5 \text{ MHz}, \tag{10.7}$$

where K_v is 30 MHz/V. The value of the kT/C noise current produced by the switched capacitor operation, $\overline{i^2_{sw}}$, was calculated as

$$\overline{i^2_{sw}} = (1/T)kT_KC_2, \tag{10.8}$$

where k is Boltzmann's constant, and T_K is temperature in degrees Kelvin. Finally, the spectral density of the Σ-Δ quantization noise was calculated as:

$$S_{\hat{q}}(f) = \frac{1}{12}\left(2sin(\pi fT)\right)^{2n}, \tag{10.9}$$

where $n = 2$ is the order of the Σ-Δ modulator.

10.4.1 A Simplified Model for Noise Analysis

To analyze the effect of the noise sources in Table 10.5 on the transmitter output, it is convenient to lump them into three dominant components. Figure 10.6 depicts

such a model, and denotes the relevant noise sources as $i_{sum}(t)$, $v_{sum}(t)$, and $\hat{q}(t)$. Comparison of Figures 10.6 and Figure 10.5 reveals that

$$\begin{aligned} \overline{i_{sum}^2} &= f_i(\overline{i_{ch1}^2}, \overline{i_{ch2}^2}, \overline{i_{ch3}^2}, \overline{i_{sw}^2}) \\ \overline{v_{sum}^2} &= f_v(\overline{v_{vco,in}^2}, \overline{v_{op}^2}), \end{aligned} \tag{10.10}$$

where $f_i(\cdot)$ and $f_v(\cdot)$ are appropriately defined functions. Rather than explicitly determining $f_i(\cdot)$ and $f_v(\cdot)$, we make the following argument:

$$\begin{aligned} \overline{i_{sum}^2} &\approx \overline{i_{ch1}^2}/2, \\ \overline{v_{sum}^2} &\approx \overline{v_{vco,in}^2} + \overline{v_{op}^2}. \end{aligned} \tag{10.11}$$

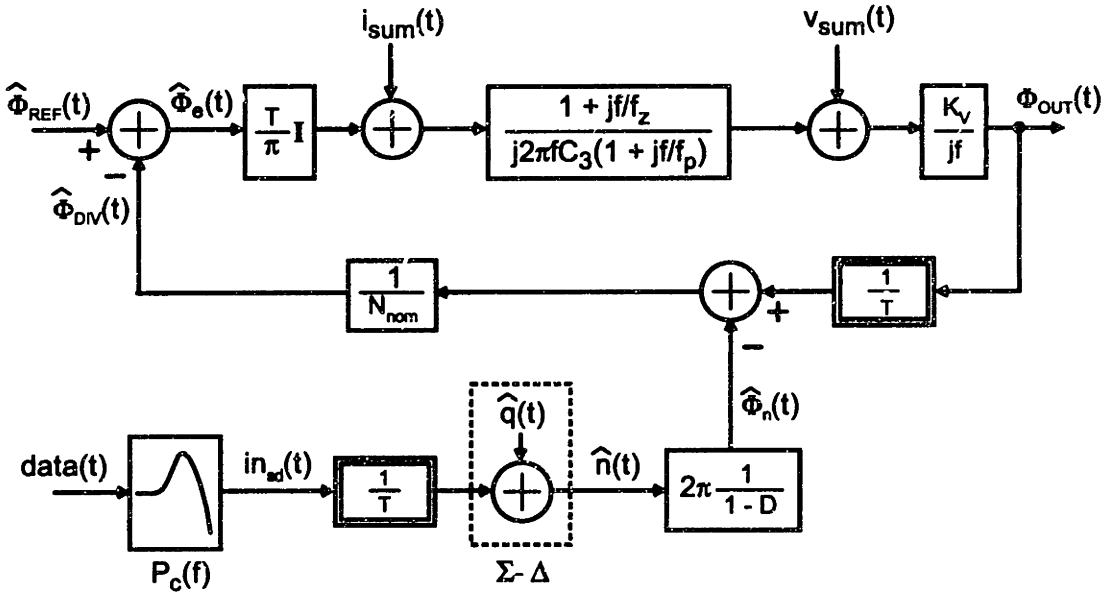


Figure 10.6: Model of test system with lumped noise sources added.

The validity of $\overline{i_{sum}^2} \approx \overline{i_{ch1}^2}/2$ is argued in two steps, the first of which is presented in Figure 10.7. In the drawing, superposition is used to break up the response of the opamp into the transfer functions associated with current coming into each of its terminals. The negative terminal is connected to a noise source with variance $\overline{i_a^2}$, and the positive terminal to a noise source with variance $\overline{i_b^2}$. (It is assumed that $\overline{i_a^2} = \overline{i_b^2}$.) For frequencies greater than f_z, the magnitude of the transfer function from the positive terminal is greater than that associated with the negative terminal. The opposite is true for frequencies less than f_z. Thus, the output of OP2 is influenced by *either* the $\overline{i_a^2}$ source or the $\overline{i_b^2}$ source, but *not both* (except when the frequency is close

to f_z). Therefore, we achieve approximately the same spectral density at the output of OP2 by connecting the same noise source to each of the terminals.

Examination of Table 10.5 reveals that $\overline{i_{ch1}^2}$ is an order of magnitude larger than $\overline{i_{ch2}^2}$, $\overline{i_{ch3}^2}$, and $\overline{i_{sw}^2}$. Since the $\overline{i_{ch1}^2}$ noise source is switched alternately between the positive and negative terminals of OP2, its contribution to $i_{sum}(t)$ will be pulsed in nature. At the nominal duty cycle of fifty percent, we would expect the energy of $\overline{i_{ch1}^2}$ to be split equally between the positive and negative terminals of OP2. As such, $\overline{i_{sum}^2}$ is then $\overline{i_{ch1}^2}/2$. This intuitive argument was verified using a detailed C simulation of the PLL with no modulation signal applied (i.e., the duty cycle of the charge pump remained constant except for variations due to Σ-Δ quantization noise). Note that $\overline{i_{sum}^2}$ should have a different value than $\overline{i_{ch1}^2}/2$ if the nominal duty cycle is offset from its desired value of fifty percent.

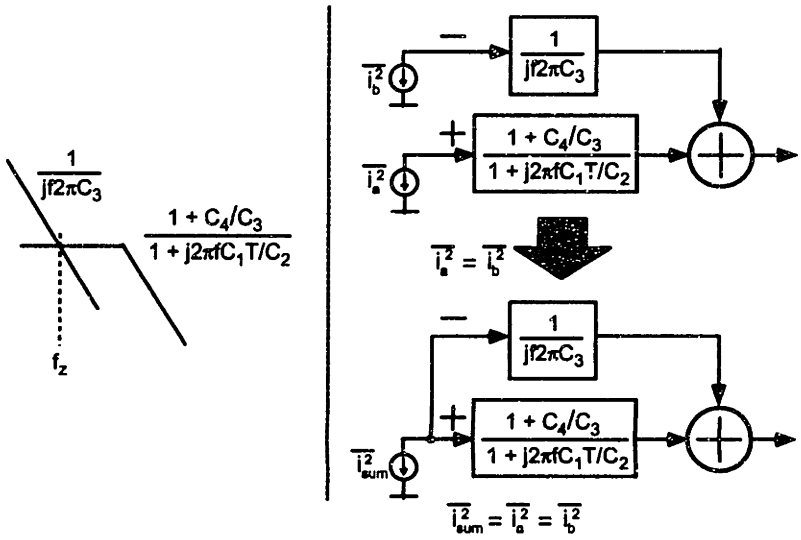


Figure 10.7: The lumping together of current noise sources entering OP2.

Since Table 10.5 reveals that $\overline{v_{vco}^2}$ is of the same order of $\overline{v_{op}^2}$, we simply add these components to obtain $\overline{v_{sum}^2} \approx \overline{v_{vco}^2} + \overline{v_{op}^2}$. This expression is accurate at frequencies less than the unity gain bandwidth of OP2; the $\overline{v_{op}^2}$ noise source is passed to its output with a gain of approximately one in this region. At frequencies beyond OP2's bandwidth, the expression is conservatively high since $\overline{v_{op}^2}$ is attenuated in this frequency range.

10.4.2 Resulting Transmitter Output Noise

The effect of $i_{sum}(t)$, $v_{sum}(t)$, and $\hat{q}(t)$ on the transmitter output is now examined with the aid of Figure 10.6. All calculations will assume that $G(f)$ is described by Equation 10.3 with the parameter values specified in Equation 10.5.

Assuming that each of the three noise sources are independent of each other, we can express the overall noise spectral density at the transmitter output, $S_{tn}(f)$, as

$$S_{tn}(f) = S_{\Phi_v}(f) + S_{\Phi_i}(f) + S_{\Phi_q}(f), \tag{10.12}$$

where $S_{\Phi_v}(f)$, $S_{\Phi_i}(f)$, and $S_{\Phi_q}(f)$ are the noise contributions from $v_{sum}(t)$, $i_{sum}(t)$, and $\hat{q}(t)$, respectively. If we further assume that $i_{sum}(t)$ and $v_{sum}(t)$ are white, each of the above spectral density components is calculated from Figure 10.6 as

$$\begin{aligned} S_{\Phi_v}(f) &= \overline{i_{sum}^2}(\pi N_{nom}/I)^2 \left|G(f)\right|^2, \\ S_{\Phi_i}(f) &= \overline{v_{sum}^2} \left|K_v/(jf)\right|^2 \left|1 - G(f)\right|^2, \\ S_{\Phi_q}(f) &= (1/T)\tfrac{1}{12}\left((2\pi)^2 \left(2sin(\pi fT)\right)^{2(n-1)}\right) \left|T \cdot G(f)\right|^2. \end{aligned} \tag{10.13}$$

Plots of these spectra are shown in Figure 10.8. As shown in the figure, the influence of $i_{sum}(t)$ dominates at low frequencies, and the influence of $v_{sum}(t)$ and $\hat{q}(t)$ dominates at high frequencies.

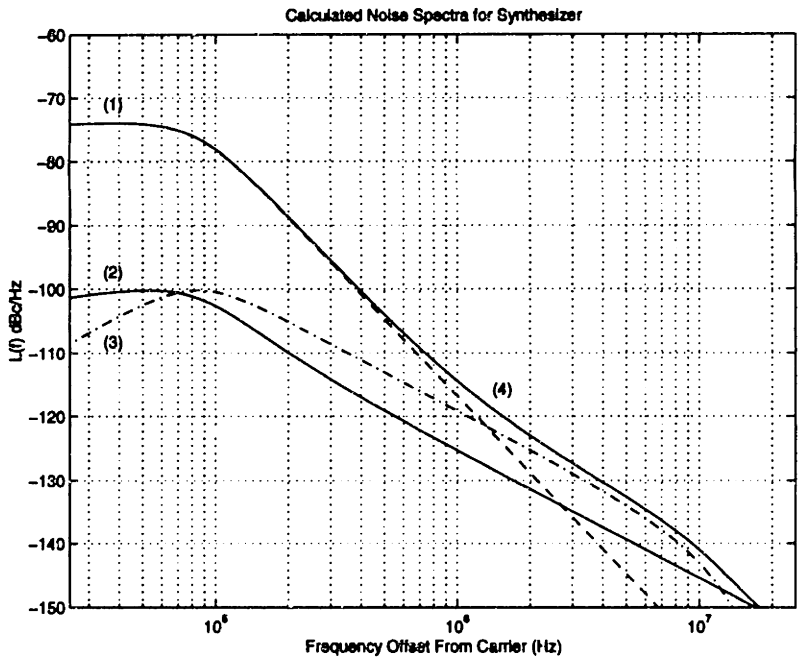


Figure 10.8: Calculated noise spectra of synthesizer: (1) charge pump induced, $S_{\Phi_i}(f)$, (2) VCO and opamp induced, $S_{\Phi_v}(f)$, (3) Σ-Δ induced, $S_{\Phi_q}(f)$, (4) overall, $S_{\Phi}(f)$.

10.5 Summary

This chapter presented design details of the prototype system. A reference frequency of 20 MHz and a closed loop PLL bandwidth of 84 kHz were chosen to achieve the required noise performance of the transmitter. Open loop parameters within the PLL were set to achieve the bandwidth specification; the root locus technique was applied to a linearized model of the PLL to accomplish this task. Finally, a detailed noise analysis was performed for the synthesizer in its unmodulated state. It was shown that noise from the charge pump circuitry dominates at low frequencies, and noise from the VCO and loop filter dominates at high frequencies.

Chapter 11

Results

The primary criteria by which a transmitter is judged are its accuracy in producing a modulation signal, and its noise performance. Evaluation of modulation integrity is established through the construction of eye diagrams from its received output. Examination of noise performance is undertaken with the use of spectral plots of the transmitter output. The following sections describe the characterization of the prototype in line with these methods.

The underlying philosophy of our presentation will be to present simulated results, explain them, and then show measured results to confirm the performance predicted by simulation. By replicating observed phenomenon with simulations, we are left with a high degree of confidence that our explanations of the phenomenon are sound.

The simulation results presented in this chapter have been computed with a custom C program. The modulation is performed by dithering the divide value in the PLL according to the proposed compensation method, and the transfer function of the PLL is set to have the same time constants and open loop gain as designed for the prototype. Also, the nominal frequency of the PLL is set to be 1.84 GHz so that it is identical to that used in prototype measurements. Nonidealities, such as the finite bit-width of the digital data path, are included in the simulation model.

11.1 Baseline Performance

Before examining simulated and measured results, it is useful to establish a baseline by which to evaluate them. To do so, we will show machine computed eye diagrams and output spectra for an ideal GFSK modulator at 1.25 Mbit/s and 2.5 Mbit/s data rates. We then show the impact of noise on the output spectrum of the actual transmitter by comparing the ideal, modulated output spectra to the calculated noise plot from Chapter 10.

11.1.1 Ideal Performance

Figure 11.1 shows the ideal eye diagrams and output spectra for GFSK modulation at $1/T_d = 1.25$ Mbit/s and $1/T_d = 2.5$ Mbit/s. The data used to generate these plots was machine computed using a custom C program; the modulation index was set at the nominal value of $h = 0.5$, from which the peak-to-peak modulation frequency deviation is calculated as $h/T_d = 625$ kHz at 1.25 Mbit/s, and $h/T_d = 1250$ kHz at 2.5 Mbit/s. Note that, at both data rates, the ideal output spectrum is the same as its modulation spectrum, i.e., $S_{out}(f) = S_{out_m}(f)$, since there is no noise in the system.

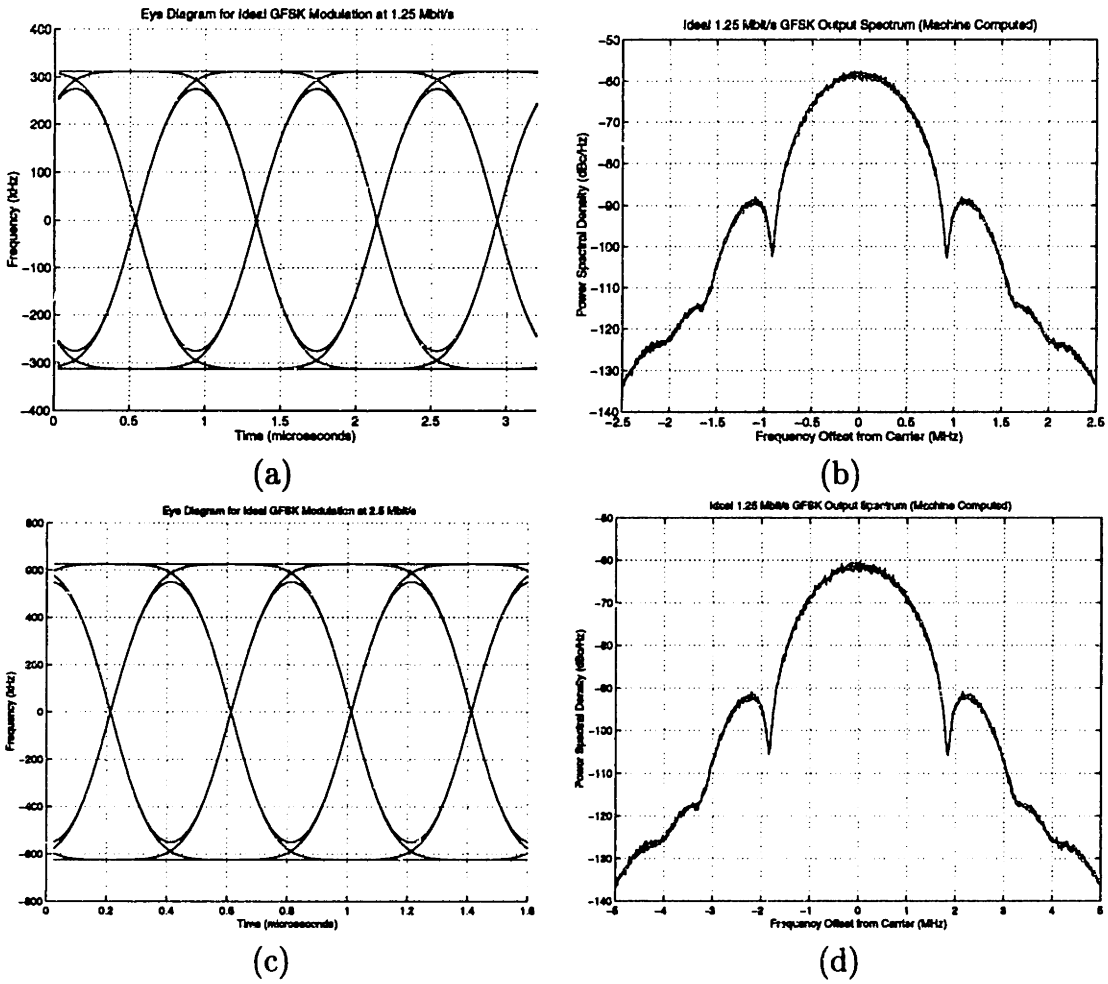


Figure 11.1: Ideal results for GFSK modulation (machine computed): (a) eye diagram at 1.25 Mbit/s, (b) output spectrum, $S_{out_m}(f)$. at 1.25 Mbit/s, (c) eye diagram at 2.5 Mbit/s, (d) output spectrum, $S_{out_m}(f)$, at 2.5 Mbit/s.

11.1.2 Influence of Noise on Output Spectrum

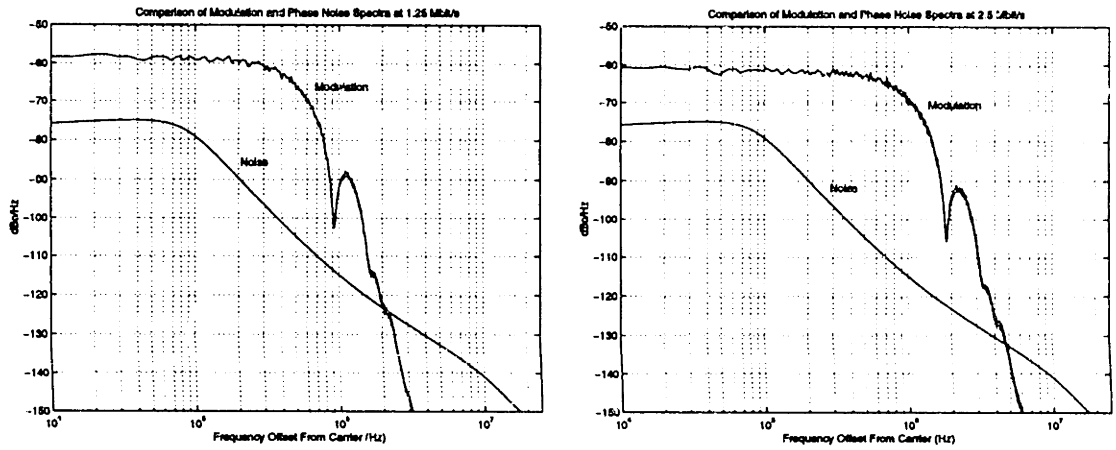
In practice, the output spectrum of the transmitter consists of the sum of the ideal modulation spectrum, $S_{out_m}(f)$, and its convolution with the unmodulated transmitter noise spectrum, $S_{out_m}(f) * S_{\Phi_{tn}}(f)$. Despite the complicated nature of this process, it turns out that a simple rule of thumb emerges for determining the overall output spectral density — at low frequency offsets relative to the crossover point of $S_{out_m}(f)$ and $S_{\Phi_{tn}}(f)$, $S_{out}(f) \approx S_{out_m}(f)$, and at intermediate frequency offsets that are higher than the crossover point, $S_{out}(f) \approx S_{\Phi_{tn}}(f)$. At high frequency offsets close to the reference frequency, the phase noise is dominated by the convolution of the reference spur with the modulation data. Each of these statements was discussed in Chapter 3, and will be confirmed with simulations shown later in this chapter.

It is worthwhile to examine $S_{out_m}(f)$ and $S_{\Phi_{tn}}(f)$ in the prototype system; comparison of these spectra provide an indication of the signal-to-noise ratio of the modulation spectrum at low frequency offsets, and the noise performance at intermediate frequency offsets. Figure 11.2 displays the ideal, machine computed modulation spectrum, $S_{out_m}(f)$, at data rates of 1.25 Mbit/s and 2.5 Mbit/s, and the calculated phase noise spectrum, $S_{\Phi_{tn}}(f)$, from Chapter 10. (Note that the calculated noise plot does not include spurious noise that is present at the reference frequency of $1/T = 20$ MHz.) The plots reveal that the modulation spectrum is over 15 dB higher than the noise at low frequencies; measured eye diagrams presented later in the chapter prove that the resulting signal-to-noise ratio is adequately high. In regards to noise performance, the plots indicate that -132 dBc/Hz can be achieved at the intermediate frequency offset of 5 MHz when the data rate is set to 1.25 Mbit/s. At 2.5 Mbit/s, however, the overall spectral density will be higher at this frequency offset since it is influenced by both the modulation and noise spectra.

11.2 Modulation Performance

Since our benchmark noise specification is set by the DECT standard, we will primarily examine the prototype modulation performance at 1.25 Mbit/s since this data rate is close to that used in DECT (1.12 Mbit/s) [14]. To show the influence of data rate on the compensation method, we will also examine the performance at twice this rate, i.e., 2.5 Mbit/s. (The maximum data rate of the prototype transmitter was measured at 2.86 Mbit/s, which is somewhat short of the theoretical maximum of 3.4 Mbit/s derived in Chapter 5. The most likely cause for this discrepancy is a nonzero offset in the PFD, which would lower the dynamic range of its output.)

To characterize modulation performance, we begin by showing a simulated eye diagram and output spectrum for the transmitter at 1.25 Mbit/s when the compensation filter is matched to the PLL transfer function. These plots are compared to the ideal case, and an explanation of discrepancies is given. We then show the effects of mismatch between the compensation filter and PLL dynamics, and the influence



(a) (b)

Figure 11.2: Comparison of simulated modulation and calculated noise spectra ($S_{out_m}(f)$ and $S_{\Phi_{tn}}(f)$, respectively): (a) 1.25 Mbit/s, (b) 2.5 Mbit/s.

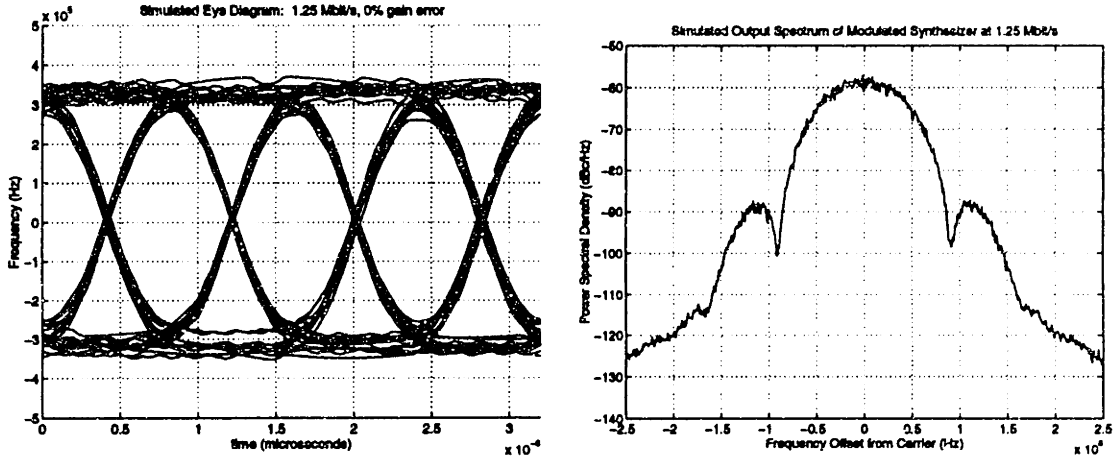
of data rate in relation to this issue. Finally, measured results are presented and compared to simulations.

11.2.1 Simulation Results

All simulations in this section ignore noise sources other than Σ-Δ quantization noise, and implement the loop filter as an ideal transfer function, rather than the switched capacitor structure used in the prototype. (The removal of such nonidealities allows us to isolate effects due to mismatch from those due to implementation details in the circuits.) All eye diagrams were generated directly from the simulated VCO input signal after it was filtered by a Hamming filter with a cutoff frequency of 7 MHz.

Figure 11.3 displays a simulated eye diagram and output power spectrum for the modulated synthesizer at 1.25 Mbit/s data rate when the PLL transfer function is matched to the compensation filter. The eye diagram indicates that the architecture is capable of excellent modulation performance; its eye is wide open and the frequency deviation is quite close to the $\pm$312 kHz deviation that is expected for GFSK modulation at 1.25 Mbit/s. The small level of ISI present in the eye diagram is caused by the parasitic pole/zero pair, f_{cp}/f_z, in the PLL transfer function as discussed in Chapter 6. The simulated power spectrum is close to ideal, but is slightly asymmetric and has higher spectral density than the ideal case at frequency offsets close to 2.5 MHz. The asymmetry is caused by the fact that the open loop gain varies with the modulation data since it is a function of the PLL divide value; this asymmetry will be more noticeable at 2.5 Mbit/s data rate, as will be shown shortly. The spectral density is higher than the ideal case at frequency offsets close to 2.5 MHz because of

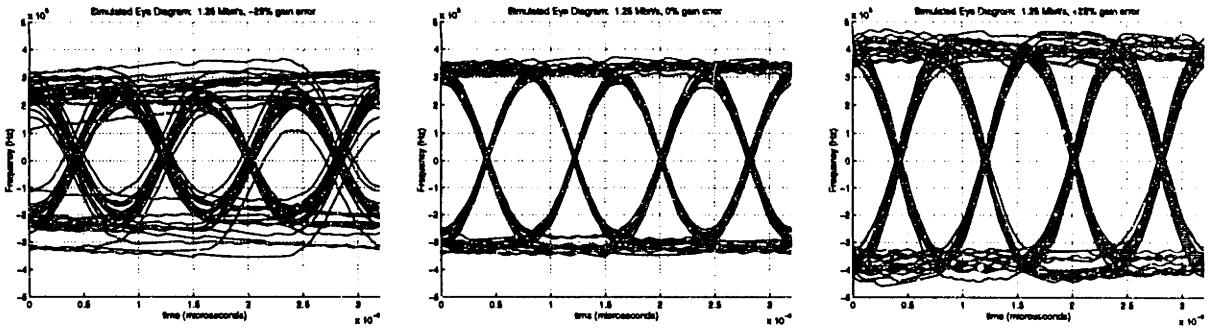
Σ-Δ quantization noise.



(a) (b)

Figure 11.3: Simulated results at 1.25 Mbit/s data rate: (a) eye diagram, (b) output spectrum, $S_{out}(f)$.

In a practical setting, the modulation data is influenced by temperature and process variations that shift the open loop gain of the PLL and cause mismatch between the compensation and PLL transfer functions. Figure 11.4 illustrates the effect of such open loop gain variation on the modulation signal for the case in which the gain is set $\pm 25\%$ away from its ideal setting. As seen by the results, the frequency deviation of the modulation signal is altered and the ISI is slightly increased.



(a) (b) (c)

Figure 11.4: Simulated eye diagrams at 1.25 Mbit/s for three different open loop gain settings: (a) -25% gain error, (b) 0% gain error, (c) 25% gain error.

To explain the observed ISI and deviation error, Figure 11.5 displays the transfer function seen by the data when the open loop gain of the PLL is too high. The result-

ing mismatch creates a parasitic pole/zero pair that occurs near the cutoff frequency of the PLL (84 kHz in this case). We can equivalently view the resulting transfer function as the sum of a lowpass and an allpass filter. ISI is introduced by the lowpass; this phenomenon can be viewed in the time domain as a parasitic time constant that interferes with modulation data coming from the allpass. The modulation deviation error is caused by the fact that the magnitude of the allpass is changed according to the amount of mismatch present.

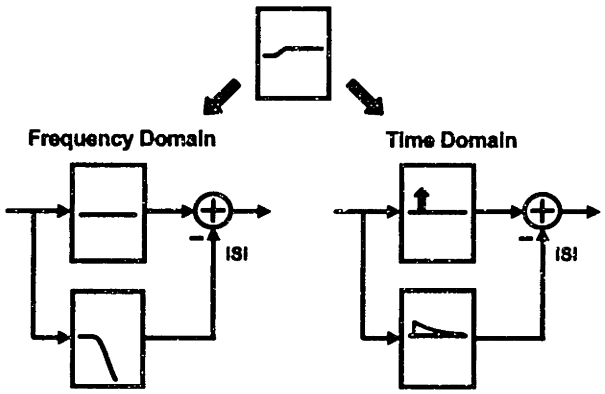


Figure 11.5: Graphical explanation of cause of deviation error and ISI.

To examine the influence of data rate on modulation integrity, Figure 11.6 shows a simulated eye diagram and power spectrum of the transmitter at 2.5 Mbit/s. The eye diagram indicates that excellent modulation performance is achieved at this data rate; its eye is wide open, the frequency deviation is quite close to the ideal of ±625 kHz, and the amount of ISI present is even less than that encountered at 1.25 Mbit/s. (The reason for the ISI being reduced will be explained shortly.) The simulated power spectrum is close to ideal, but is slightly asymmetric and has higher spectral density than the ideal case at frequency offsets close to 5 MHz. The asymmetry is increased over the 1.25 Mbit/s case due the increased signal swing of the divide value relative to its nominal value. The spectral density is higher than the ideal case at frequency offsets close to 5 MHz because of Σ-Δ quantization noise.

As observed by comparison of Figures 11.6 and 11.3, the amount of ISI that occurs under matching conditions at 2.5 Mbit/s is much less than that which occurs at 1.25 Mbit/s. Figure 11.7 reveals that this statement is also true under mismatched conditions by its comparison to Figure 11.4.

Figure 11.8 provides an intuitive explanation for the data rate dependence of ISI. As illustrated, the data signal is corrupted by the portion of its energy that passes through the lowpass filter formed by mismatch. Data signals that have large bandwidth relative to this lowpass will experience small levels of ISI since the relative ISI energy will be much less than that of the data. As the data bandwidth is decreased,

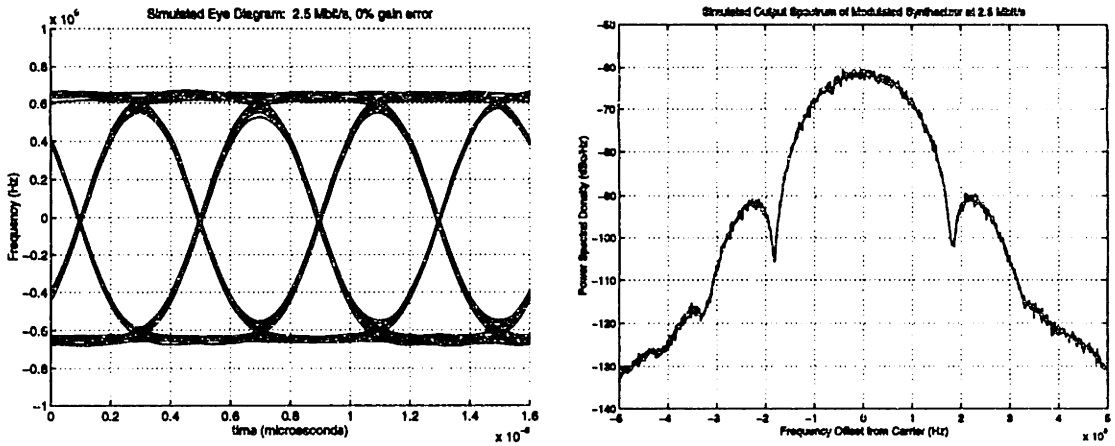


Figure 11.6: Simulated results at 2.5 Mbit/s data rate: (a) eye diagram, (b) output spectrum, $S_{out}(f)$.

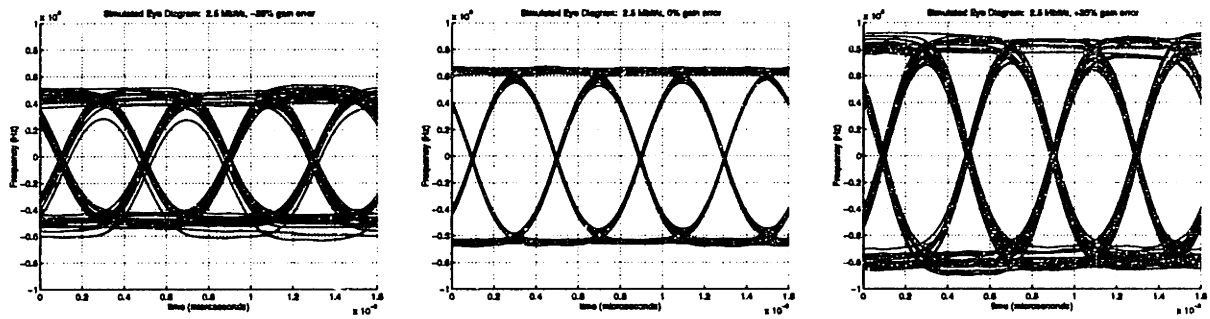


Figure 11.7: Simulated eye diagrams at 2.5 Mbit/s for three different open loop gain settings: (a) -25% gain error, (b) 0% gain error, (c) 25% gain error.

the ratio of ISI energy to data energy increases and the effects of ISI become more pronounced.

11.2.2 Measured Results

Figure 11.9(a) depicts a measured eye diagram at 1.25 Mbit/s taken from the prototype using an HP 89441A modulation analyzer; the corresponding spectrum shown in Figure 11.9(b) was obtained with an HP 8563E spectrum analyzer. The same instruments were used to obtain the eye diagram and power spectrum of the prototype at 2.5 Mbit/s that are shown in Figure 11.10. Each of these figures indicate that the measured modulation performance of the prototype is very close to that predicted by

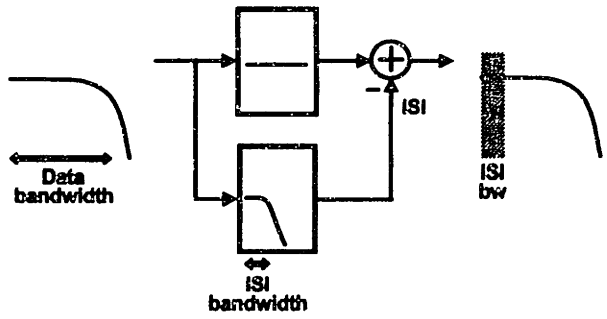
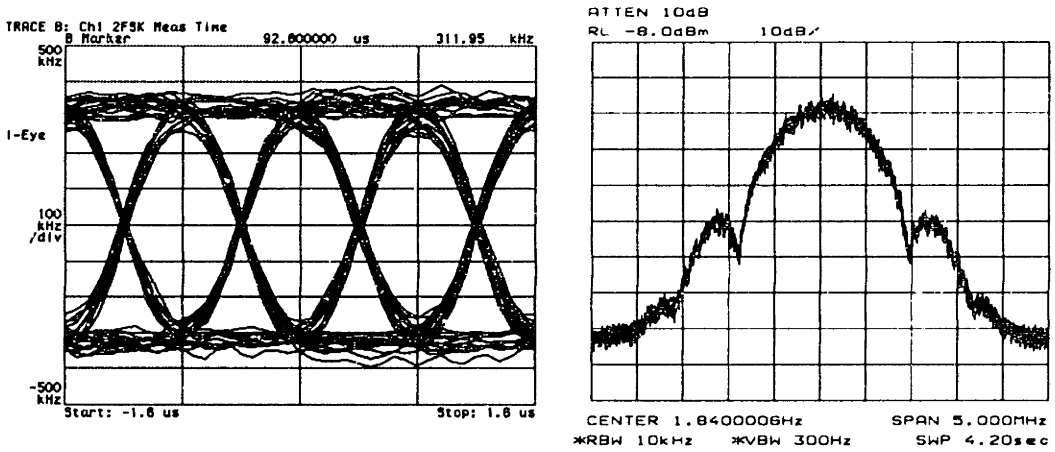


Figure 11.8: Graphical explanation of dependence of ISI level on data rate.

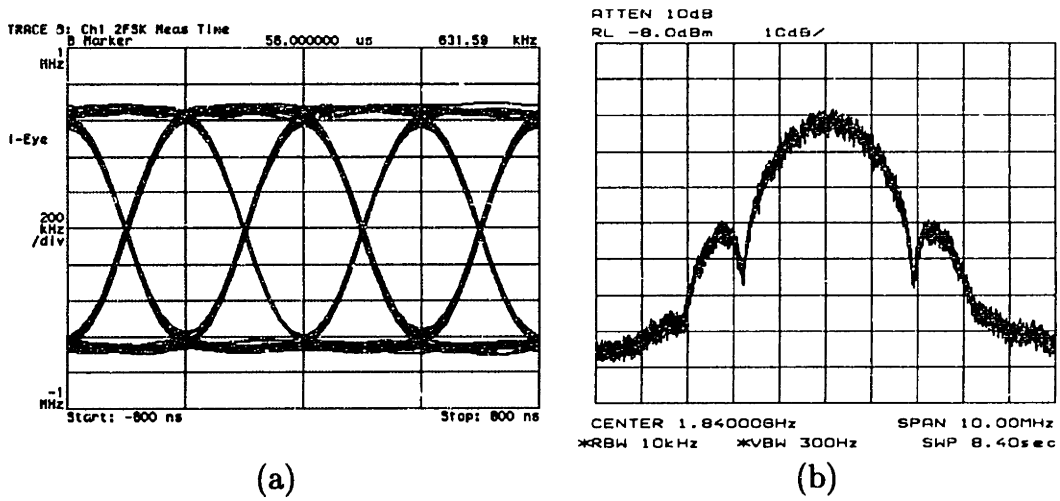
simulations.



(a) (b)

Figure 11.9: Measured results at 1.25 Mbit/s data rate with zero open loop gain error: (a) eye diagram, (b) output spectrum (1.84 GHz center frequency, 5 MHz span).

It is important to understand that the spectral plots in Figures 11.9 and 11.10 cannot be used to infer the noise performance of the transmitter; the spectra shown are not accurate at high frequency offsets due to the limited dynamic range of the spectrum analyzer used to obtain them. The reason for the inaccuracy is that the input signal to the spectrum analyzer cannot be made sufficiently large, in comparison to the instrument's noise floor, to accurately measure the input spectral density at the low levels that occur at high frequency offsets. Measurements of the transmitter phase noise at these high frequency offsets are shown in the next section.



(a) (b)

Figure 11.10: Measured results at 2.5 Mbit/s data rate with zero open loop gain error: (a) eye diagram, (b) output spectrum (1.84 GHz center frequency, 10 MHz span).

Figure 11.11 shows measured eye diagrams from the prototype at three open loop gain settings and two different data rates. The measured results shown in Figure 11.11 are nearly identical to those obtained from simulation.

11.3 Noise Performance

The noise performance of the transmitter is evaluated in this section. We begin by showing simulated spectra of the transmitter in its unmodulated state, and then use simulations to examine the impact of modulation on the output spectrum. Measured results are then presented and compared to simulations.

11.3.1 Noise Measurement Considerations

We seek an overall noise specification at the transmitter output that is less than -131 dBc/Hz at 5 MHz offset from the carrier when the data rate is set to 1.25 Mbit/s. Measurement of this low noise value is problematic with spectrum analyzers due to their limited dynamic range. To mitigate this problem, all noise measurements were taken with an HP 3048A phase noise measurement system that was used in conjunction with the frequency discriminator method. Unfortunately, the dynamic range of this instrument is insufficient to measure phase noise at the desired levels while the transmitter is modulated. (The energy of the phase transitions is greatly

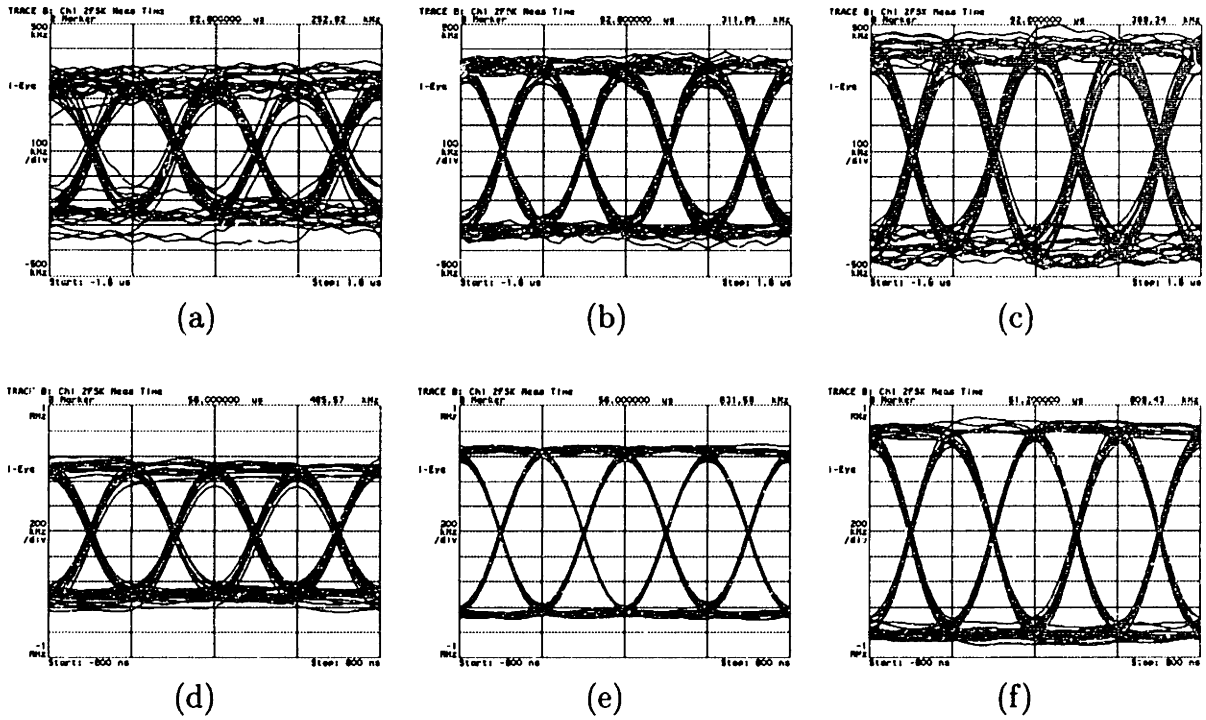


Figure 11.11: Measured eye diagrams at 1.25 Mbit/s and 2.5 Mbit/s for three different open loop gain settings: (d) 1.25 Mbit/s, -25% gain error, (e) 1.25 Mbit/s, 0% gain error, (f) 1.25 Mbit/s, 25% gain error, (a) 2.5 Mbit/s, -25% gain error, (b) 2.5 Mbit/s, 0% gain error, (c) 2.5 Mbit/s, 25% gain error.

increased during modulation, which forces the HP 3048A to bypass its LNA and thereby increase its noise floor.)

To overcome this obstacle, the transmitter's modulated noise performance will be inferred from measured phase noise data taken from the transmitter in its unmodulated state. Specifically, it will be assumed that at an offset frequency of 5 MHz and a data rate of 1.25 Mbit/s, the modulated transmitter output spectrum, $S_{out}(f)$, has the same spectral density as its unmodulated phase noise spectrum, $S_{\Phi_{ln}}(f)$. We will present simulated results that confirm that this is a reasonable assumption.

When measuring the phase noise of the transmitter in its unmodulated state, the digital data path is exercised with a periodic dithering sequence applied to the least significant bit of its modulation bus. Application of the dithering sequence avoids the generation of spurious noise in the Σ-Δ modulator, and is used when obtaining both simulated and measured phase noise spectra when the Σ-Δ is included. Figure 11.12 displays one period of the dithering sequence that was used, along with its power spectrum. The sequence was generated by sending half a cycle of a digitized sine

waveform into the input of a first order, MASH Σ-Δ modulator. A relatively flat spectrum was achieved for the sequence by a trial-and-error procedure; namely, the amplitude of the input sine wave was reduced until acceptable results were obtained. The resulting spectrum in Figure 11.12 is seen to have a periodic bumpiness. Fortunately, this bumpiness has negligible impact on the transmitter output spectrum; an explanation its occurrence was not determined. Note that one period of the sequence is 32K samples long, which translates to a fundamental frequency of 610 Hz since the data is fed in at 20 MHz.

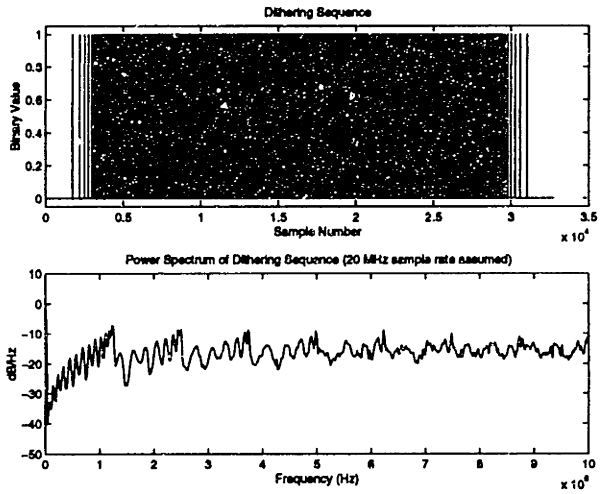


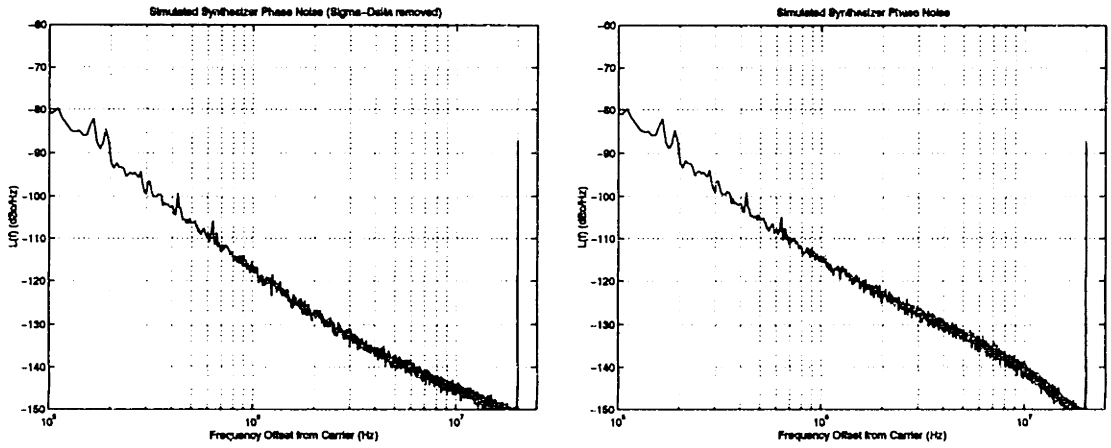
Figure 11.12: Binary dithering sequence fed into least significant bit of digital modulation path.

11.3.2 Simulated Results

The simulation model of the transmitter in this section includes the noise sources $I_{sum}(t)$ and $V_{sum}(t)$ described in the Chapter 10 so that an accurate representation of $S_{\Phi_{in}}(f)$ is achieved. A model for the switched capacitor loop filter that is used in the prototype is also included; this filter is operated under Case 1 conditions, as defined in Chapter 9.

Figure 11.13 shows the simulated output phase noise, $S_{\Phi_{in}}(f)$, of the unmodulated transmitter with the Σ-Δ removed and in place. These spectra agree well with the calculated noise spectrum displayed in Figure 10.8 of Chapter 10. (Note that I was set to 1.5 uA in the simulations.) The simulated spectra include the spurious tone that is present at 20 MHz due to the fifty percent nominal duty cycle of the PFD output. A bumpiness is seen in the simulated spectra at frequencies between 1 and 10 MHz; this phenomenon is an artifact of the decreased number of sample points used to compute the spectrum at lower frequencies, and imperfections in the numerical

procedure used to generate the charge pump noise (i.e., the sequences do not have a perfectly flat spectrum). Simulated data at frequencies lower than 100 kHz is not shown due to the small number of data points calculated for this region.



(a) (b)

Figure 11.13: Simulated phase noise, $S_{\Phi_{tn}}(f)$, of unmodulated synthesizer: (a) Σ-Δ removed, (b) Σ-Δ in place and appropriately dithered.

Comparison of Figure 11.13(a) to Figure 11.13(b) reveals that Σ-Δ quantization noise has the dominant influence on phase noise performance at intermediate frequencies. With the Σ-Δ included, the phase noise density at 5 MHz offset frequency is -132 dBc/Hz.

The influence of modulation on the output spectrum is seen in Figure 11.14, which displays plots of $S_{out}(f)$ and $S_{\Phi_{out}}(f)$ at two different data rates. ($S_{out}(f)$ is the power spectral density of the transmitter output, while $S_{\Phi_{out}}(f)$ is the power spectral density of the *instantaneous phase* of the transmitter output. See Chapter 3 for details.) At 1.25 Mbit/s, we see that $S_{out}(f) \approx S_{\Phi tn}(f)$ for frequencies in the range of 5 MHz; this confirms that measurements of $S_{\Phi_{tn}}(f)$ can be used to evaluate the noise performance of the modulated transmitter at this frequency offset. At 2.5 Mbit/s, the output spectral density is raised to -130 dBc/Hz at 5 MHz offset due to the higher bandwidth of the modulation signal.

A few artifacts appear in $S_{\Phi_{out}}(f)$ that deserve explanation. First, spurious tones are seen at multiples of the data rate; these tones are an artifact of modulating the duty cycle of the PFD output, as discussed in Chapter 9. Fortunately, the spurs do not show up in the output spectrum, $S_{out}(f)$, since they are convolved with the modulation spectrum. Second, each plot of $S_{\Phi out}(f)$ contains bumps at 20 MHz; their appearance is a direct consequence of compensating the discrete-time signals used to create $\Phi_{mod}(t)$, as will now be explained. Using notation from Chapter 5, compensation of $in_{sd}(t)$ causes its spectral density, $S_{in_{sd}}(f)$, to rise dramatically at

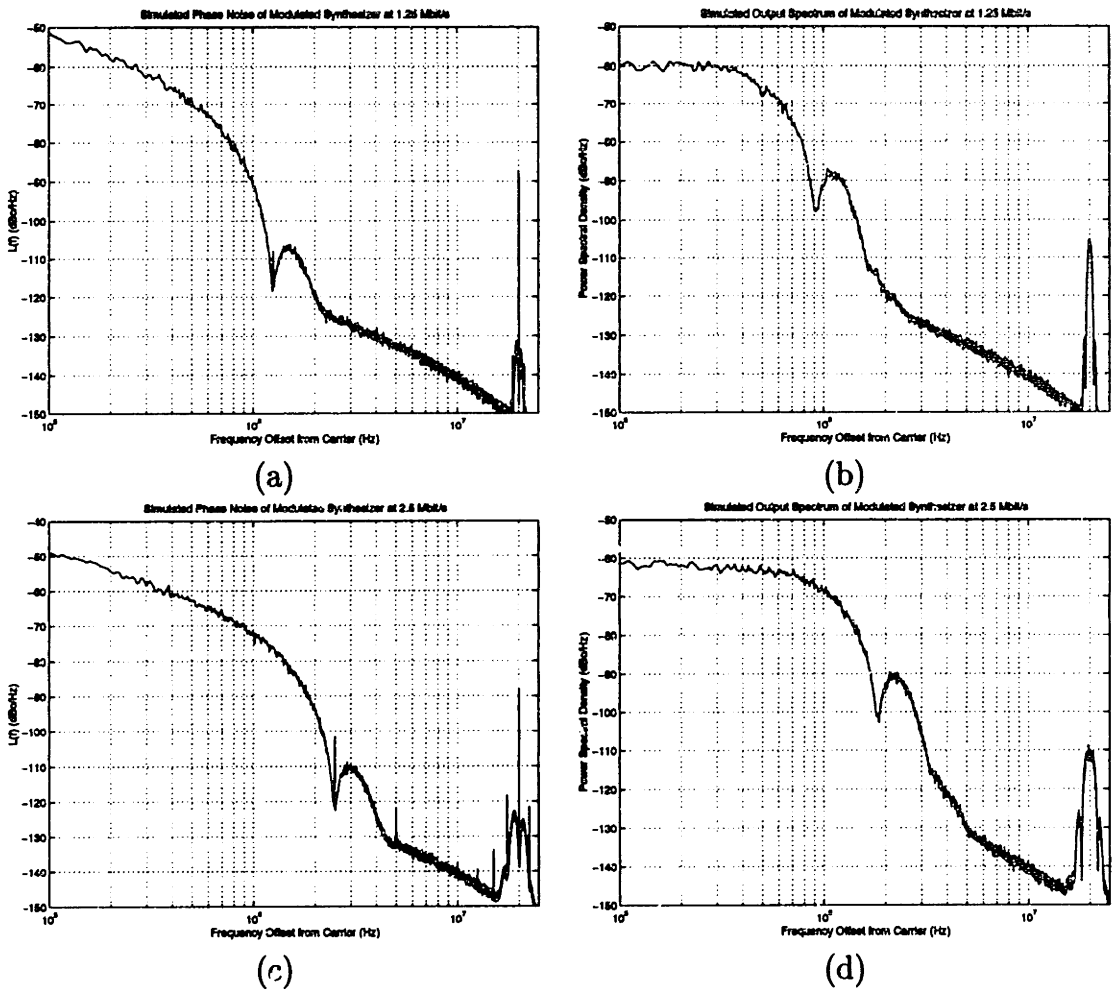


Figure 11.14: Simulation results of PLL output spectrum with noise sources included: (a) $S_{\Phi_{out}}(f)$ at 1.25 Mbit/s, (b) $S_{out}(f)$ at 1.25 Mbit/s, (c) (a) $S_{\Phi_{out}}(f)$ at 2.5 Mbit/s, (d) $S_{out}(f)$ at 2.5 Mbit/s.

frequencies higher than f_o until the bandwidth of $W(f)$, B, is reached. At frequencies higher than B, $S_{in_{sd}}(f)$ falls sharply due to attenuation imposed by $W(f)$. Since $in_{sd}(t)$ is effectively sampled at rate $1/T = 20$ MHz, a replica of its spectrum is seen at 20 MHz; the relatively low DC value of $S_{in_{sd}}(f)$ causes the replica to appear as two bumps, and attenuation by continuous-time filtering in the PLL causes the bumps to be asymmetric.

The primary artifact seen in $S_{out}(f)$ is a bump at 20 MHz that is caused by convolution of the modulation signal, $S_{out_m}(f)$, with the reference spur. The high relative magnitude of this replica spectrum overshadows the effects of the bumps produced by $\Phi_{mod}(t)$ in $S_{\Phi out}(f)$. It is important to note that the simulation model does not model the finite bandwidth of the loop filter opamp, OP2, which will further

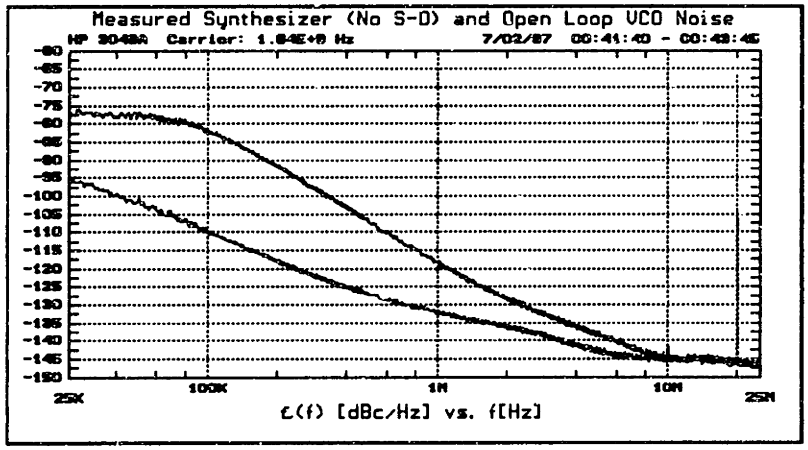
decrease the magnitude of the output power spectrum at high frequency offsets.

11.3.3 Measured Results

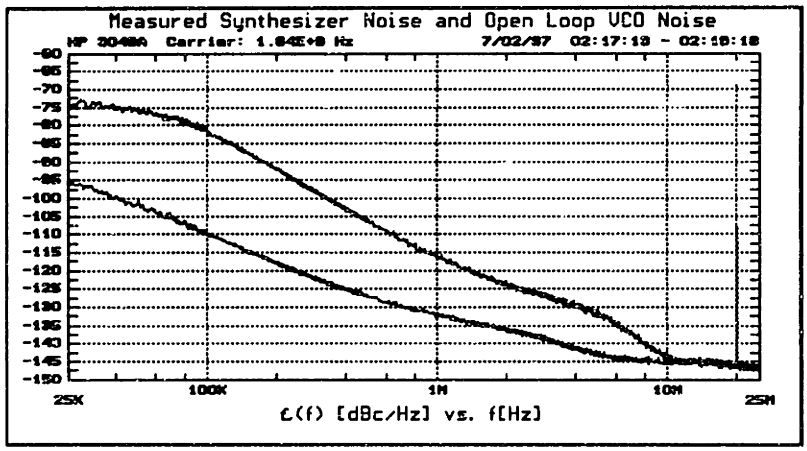
Figure 11.15 shows measured plots of $S_{\Phi_{tn}}(f)$ and the open loop phase noise of the VCO from the transmitter prototype; the plots were obtained from an HP 3048A phase noise measurement system. In Figure 11.15(b), the binary data stream shown in Figure 11.12 was fed into the LSB of the modulation path to randomize the internal states of the Σ-Δ modulator and reduce spurious content. The resulting spectra compares quite well with the calculated curve in Figure 10.8, especially at high frequency offsets close to 5 MHz. At low frequencies, the measured noise is within about 3 dB of the predicted value; the higher discrepancy in this region might be attributed to the fact that $\overline{i_{ch1}^2}$ was calculated without considering the transient response of the charge pump, and that an offset in the PFD duty cycle may be present. The spur at 20 MHz offset, which is due to the fifty percent nominal duty cycle of the PFD, is less than -60 dBc.

11.4 Summary

The chapter presented simulated and measured results to characterize the modulation and noise performance of the transmitter. Measured eye diagrams from the prototype indicate that the transmitter achieves excellent modulation performance at 1.25 Mbit/s and 2.5 Mbit/s when the PLL transfer function and compensation filter are matched. The effect of mismatch is to introduce ISI and frequency deviation error, which were quantified at open loop gain errors of $\pm 25\%$. In regards to noise performance, measurements and simulations were used to infer that the prototype achieves an output phase noise spectral density of -132 dBc/Hz at 5 MHz offset at 1.25 Mbit/s data rate.



(a)



(b)

Figure 11.15: Measured phase noise, $S_{\Phi_{in}}(f)$, of unmodulated synthesizer and of open loop VCO: (a) Σ-Δ removed, (b) Σ-Δ in place and appropriately dithered.

Chapter 12

Conclusions

A digital compensation method was described that allows fractional-N frequency synthesizers to be directly modulated at high data rates while simultaneously achieving good noise performance. The technique allows digital phase/frequency modulation to be achieved without mixers or D/A converters in the modulation path. The resulting transmitter design is primarily digital in nature and reduced to its fundamental components — a frequency synthesizer that accurately sets the output frequency, and a digital transmit filter that provides good spectral efficiency.

The synthesizer is implemented as a phase locked loop (PLL). To achieve good noise performance with a simple design, the PLL bandwidth is set to a low value relative to the data bandwidth. A digital compensation filter is then used to undo the attenuation of the PLL transfer function seen by the data. This filter adds little complexity to the transmitter architecture since it can be combined with the digital transmit filter; the overall filter is efficiently implemented by using a ROM to perform the required convolution with input data.

The idea of using compensation to modulate a PLL frequency synthesizer at data rates beyond its bandwidth is not new; patents that advocate such an idea are found in [56–59]. However, the approaches presented in these patents are intimately tied to modulation methods in which data enters as an *analog* signal to a node (or nodes) within the PLL. The compensation filters are implemented as analog circuits; this approach requires several component values to be accurately set, and leads to the amplification of noise in those frequency regions where the input signal is increased.

In contrast, the technique presented here achieves compensation by simply *modifying* the digital transmit filter; its implementation adds little power or complexity to the synthesizer design, and does not lead to amplification of noise. The presented method allows accurate matching between the compensation and PLL transfer functions to be achieved by proper adjustment of *one parameter*, the open loop gain of the PLL. The resulting transmitter architecture achieves a high level of integration, low power dissipation, and good performance.

To provide proof of concept of the method, a 1.8 GHz transmitter was built that

supports data rates in excess of 2.5 Mbit/s using Gaussian Frequency Shift Keying (GFSK), the same modulation method used in the digital enhanced cordless telecommunications (DECT) standard. The phase noise of the unmodulated synthesizer was measured at -132 dBc/Hz at 5 MHz offset from the carrier frequency.

The key circuits in the prototype were implemented on a custom, 0.6 um CMOS IC that consumes 27 mW. Included on the IC are an on-chip, continuous-time filter that requires no tuning or external components, a digital MASH Sigma-Delta converter that achieves low power operation through pipelining, and an asynchronous, 64 modulus divider (prescaler) that supports any divide value between 32 and 63.5 in half cycle increments of its input. An external divide-by-2 prescaler allows the divider to operate at half the frequency of the voltage controlled oscillator (VCO), and changes the range of divide values to be all integers between 64 and 127.

12.1 Future Research

A method for correctly adjusting the open loop gain parameter was not pursued as part of this thesis work, and is a subject of future research. If this architecture were applied to the DECT standard, the tolerance required on this parameter would be $\pm 10\%$. It is believed that similar tuning techniques to those used with continuous-time filters [48] could be used to achieve this accuracy. Another possibility is to place additional complexity in the receiver, and have it tune the transmitter based on its received waveforms. A final option is to use a ROM to store factory calibrated gains for different carrier frequency settings. (The VCO gain changes with its nominal frequency setting.) Success of this approach depends on having a VCO whose gain does not vary by more than $\pm 10\%$ over the lifetime of the product.

The power dissipation of the multi-modulus divider dominates that of the custom IC; further reduction of the transmitter power consumption must begin with this component. A promising avenue is to use alternative technologies, such as BiCMOS or advanced CMOS processes, to achieve the high speed requirements of the divider circuits at lower power levels. From an architectural standpoint, new topologies can be examined for the divide-by-2 stages in the divider. Some interesting possibilities include the use of inductors to resonate out load capacitance, or entirely different structures such as dynamic frequency dividers [70].

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Appendix A

Board Design

This appendix includes the instructions and schematics for the PC board used in the prototype system.

A.1 Overview

A six layer board was built as part of the prototype system. The board consists of 3 signal layers and 3 ground planes that are interleaved, as illustrated in Figure A.1 below. Note that, to allow flexibility in troubleshooting, no solder mask was put on the board, and signals were routed on Signal Layer 1 whenever possible.

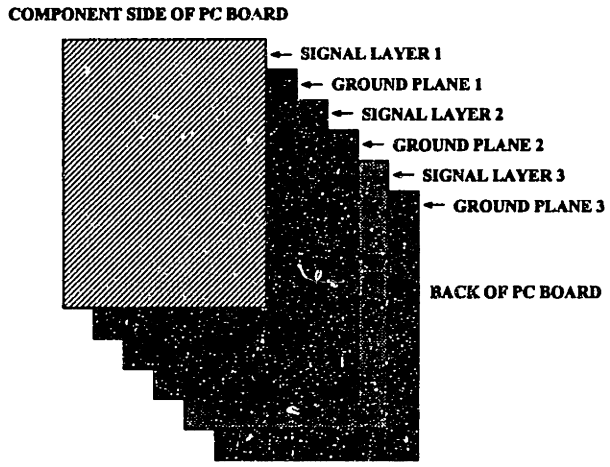

Figure A.1: Description of layers in PC board.

Several of the signals on the board run at frequencies in the range of 2 GHz; their respective board traces are required to have 50 Ohms characteristic impedance. To achieve this impedance, these signals were routed on Signal Layer 1 with 18 mil wide traces, and a dielectric thickness of 10 ± 1 Mils was specified between Signal Layer

1 and Ground Layer 1. An FR4 glass epoxy laminate ($\epsilon_r = 4.4 \pm .?$) is used as the dielectric between all the board layers.

A.2 Schematics

The schematic for the board is divided into four separate pages: A top level diagram, a Digital Control Block, an RF Block, and a Power Block. The Digital Control Block requires 3.3 V and 5 V power supplies, while the RF and Power Blocks require 12 V. For convenience; bypass capacitors are drawn as one instance with the notation *X number* indicating the number of such capacitors. For instance, in the Digital Control Block schematic, there are 17 bypass capacitors whose values are all 0.1 uF.

A.3 Layout

Great care was taken in the layout of several sections of the board. The RF section consists of parts that are operating at 1.8 GHz with risetimes on the order of hundreds of picoseconds. The Digital Block runs at a much lower 20 MHz (with one 40 MHz signal), but still required care in layout in order to avoid coupling noise into the RF section. The strategy taken for the Digital Section is as follows: all traces are routed on the topmost signal layer when possible, and kept as short as practical if they are outputs of the IDT72271 or 74LCX541 chips, or the 40 MHz oscillator. In the RF section, all traces are kept to the minimum possible length, and sized to have 50 Ohms characteristic impedance where indicated. Also, sharp corners on these lines have been avoided.

Figure A.2 illustrates a preliminary layout of the Digital and RF sections, and indicates where the Power Block is approximately located. This layout was followed closely in terms of placement, but optimized where possible according to the strategy described above. In the drawing, I have included many of the signal lines, as well as the 3.3 V, 5 V, and 12 V power supply traces in different shades of gray to indicate their respective board layer.

In regards to the grounding strategy, all Ground planes are connected together at numerous points on the board using plated through holes. In line with this strategy, ALL component ground leads are connected to all 3 Ground planes using plated through holes. (this is true throughout the board, not just the RF section). Particular effort was made in the RF section to assure minimum inductance to ground for each component (i.e. plated through holes are placed underneath and immediately next to all ground leads). To increase isolation, all signal traces on the topmost layer (particularly in the RF section) are surrounded (with about 40 Mils distance) with GROUND that is connected to all 3 Ground planes with numerous plated through holes, as illustrated in Figure A.3.

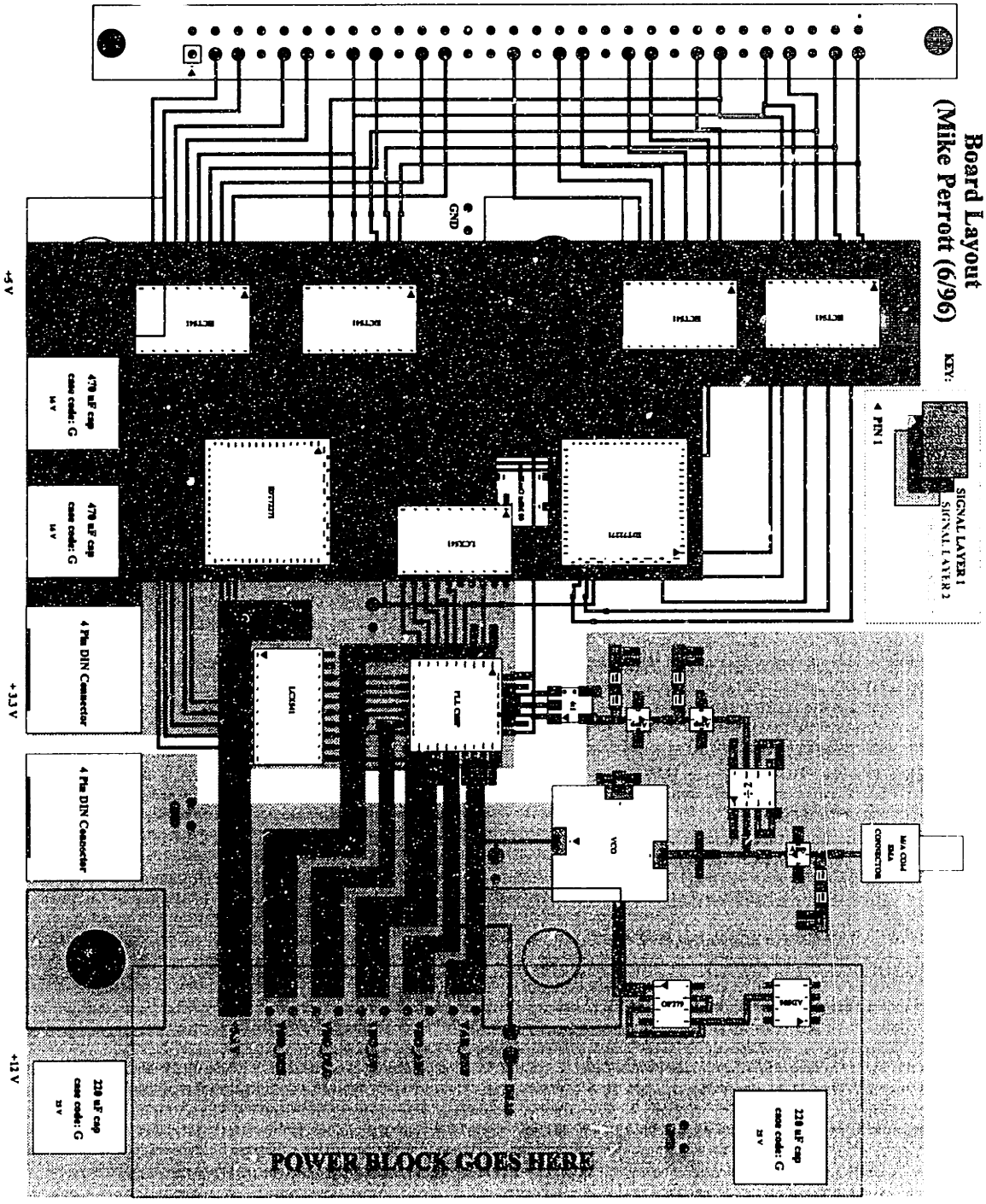

Figure A.2: Preliminary layout of PC board.

Special consideration was ma' ling the grounding of the V602MC06 VCO and the PLL CHIP. Each of th(ckages have metal base packages that serve as ground. Therefore, Signal Layer 1 underneath the VCO is patterned as described in

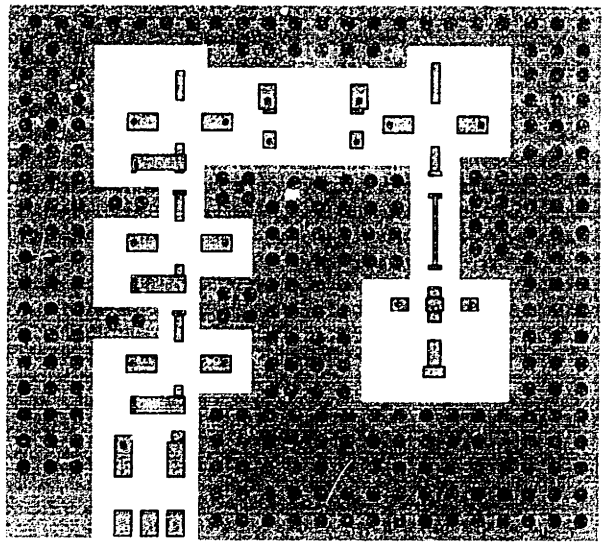

Figure A.3: Illustration of plated through holes in PC board.

Z-Communications, Inc. Application Note AN-101. The same strategy was applied to grounding of the PLL CHIP.

The 40 MHz oscillator is placed on the back of the PC board to allow a shorter trace length to the associated LCX541 input pin. An approximate placement is shown in Figure A.2.

As mentioned above, only part of the Power Block is shown in the layout diagram; the rest of it is placed on the right side of the board as indicated by the dashed box. The layout of this section used the topmost layer as much as possible in order to allow an easy means of accessing the signals in this block (particularly those signals at the interface of the Power Block — IBIAS, VAR_REF, etc.).

It should be noted that the board can be mounted to a probe station containing 4 mount points that are spaced 3 by 2 inches apart. The need for these mount points led to holes that are 250 Mil in diameter on the PC board; the portion of the PC board touching the mount points is free of back side components. The location of the mount points are indicated in Figure A.4, which includes relevant dimensions. For practical reasons, only two diagonal probe station holes were cut into the board, as indicated by solid circles in the diagram. Although the board is not screwed into the other two mount points, contact is still be made which requires the back side of the board to be free of components in the area indicated by the dashed squares.

Finally, 4 screw holes, each 250 Mil in diameter, are included on the board for the mounting of stand-offs.

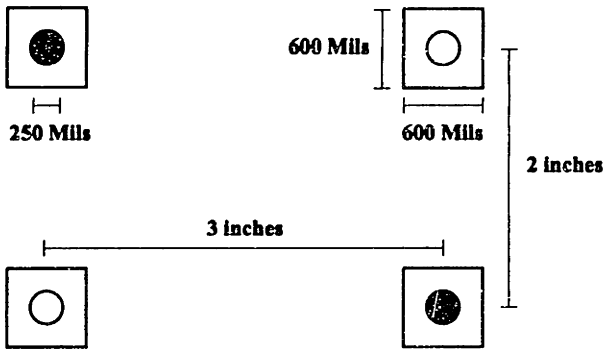

Figure A.4: Mount points on PC board.

A.4 Mechanical Information

All mechanical drawings are included at the end of this packet of material. The total IC pin count on the board is 396. The stated pin counts do not include headers, resistors, capacitors, or connectors since these can be derived easily from the parts list on the board.

Quantity	Part Number	Description
2	CP-2440-ND (Digi-Key)	4-Position Circular DIN Conn.
1	AHS60G-ND (Digi-Key)	60 Pin, 100 Mil Shrouded Ribbon Conn.
1	2064-0000-00	M/A-COM SMA Right Angle Jack
7	S2011-01-ND (Digi-Key)	2 Pin, 100 Mil Header
1	S2011-02-ND (Digi-Key)	4 Pin, 100 Mil Header
1	S2011-12-ND (Digi-Key)	24 Pin, 100 Mil Header
4	74HCT541ADW	5 V buffer
2	IDT72271L20PF	SuperSync 32K FIFO
2	74LCX541DW	3.3 V buffer
1	XC650CT-ND (Digi-Key)	40 MHz Oscillator
5	MSA-0910	6 GHz Amp
1	UPB581B	Divider by 2 Prescaler
1	V602MC06	1.8 GHz VCO
1	ETC4-1T-6	.8 - 2 GHz transformer
4	AD586JR	5V reference
1	LM334M	current reference
4	OP279GS	high current op amp
5	ST5P502CT-ND (Digi-Key)	5K trimpot
8	PCS5106CT-ND (Digi-Key)	Tantalum, size D, 25V, 10 uF cap.
29	PCC104BCT-ND (Digi-Key)	Ceramic, size 1206, 0.1 uF cap.
8	PCC220CVCT-ND (Digi-Key)	Ceramic, size 0603, 22 pf cap.
2	PCC220CQCT-ND (Digi-Key)	Ceramic, size 0402, 22 pf cap.
3	PCC222BVCT-ND (Digi-Key)	Ceramic, size 0603, 2200 pf cap.
13	PCC102BVCT-ND (Digi-Key)	Ceramic, size 0603, 1000 pf cap.
12	PCC102BQCT-ND (Digi-Key)	Ceramic, size 0402, 1000 pf cap.
2	PCE2046CT-ND (Digi-Key)	Electrolytic, size G, 16 V, 470 uF cap.
2	PCE2048CT-ND (Digi-Key)	Electrolytic, size G, 25 V, 220 uF cap.
10	P60.4CCT-ND (Digi-Key)	Metal film, size 0805, 60.4 ohm res.
2	P68.1HCT-ND (Digi-Key)	Metal film, size 0603, 68.1 ohm res.
2	P27.4HCT-ND (Digi-Key)	Metal film, size 0603, 27.4 ohm res.
1	P49.9HCT-ND (Digi-Key)	Metal film, size 0603, 49.9 ohm res.
2	P100LCT-ND (Digi-Key)	Metal film, size 0402, 100 ohm res.
3	P1kCCT-ND (Digi-Key)	Metal film, size 0805, 1 Kohm res.
1	3H32M	Mini Systems RF package for PLL CHIP

Table A.1
Parts list for PC board in prototype

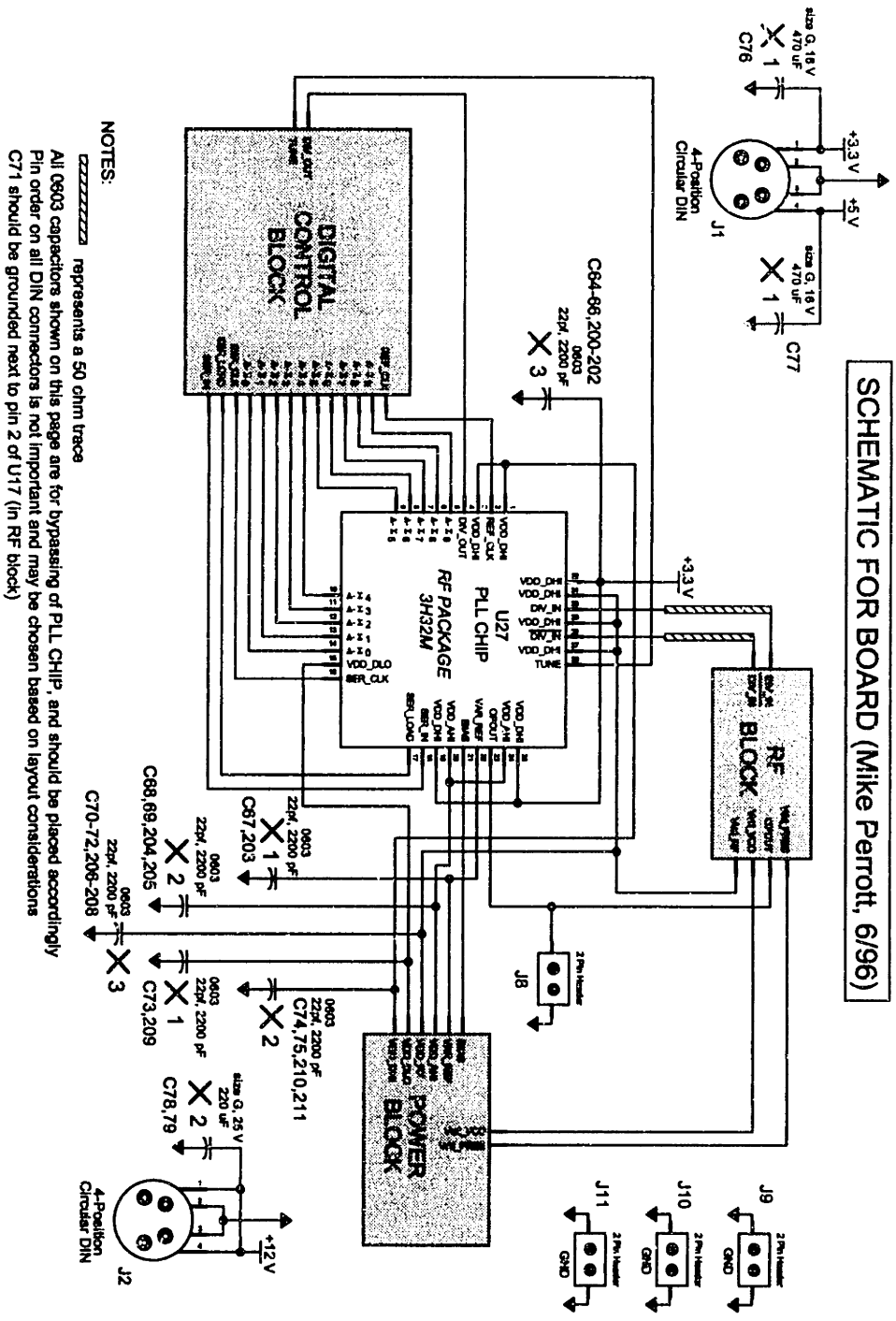

Figure A.5: Primary schematic diagram of PC board.

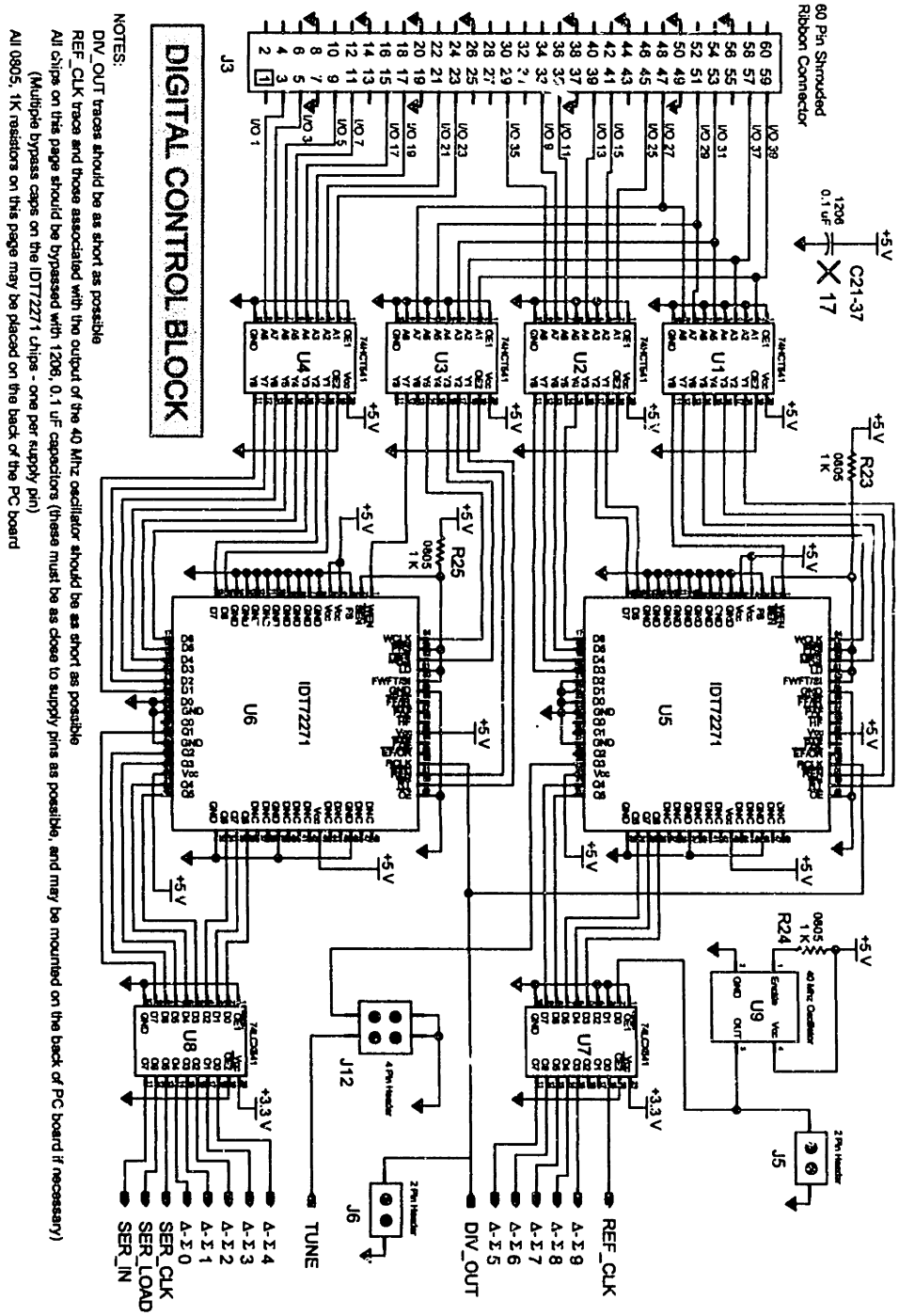

Figure A.6: Schematic diagram of I/O section of PC board.

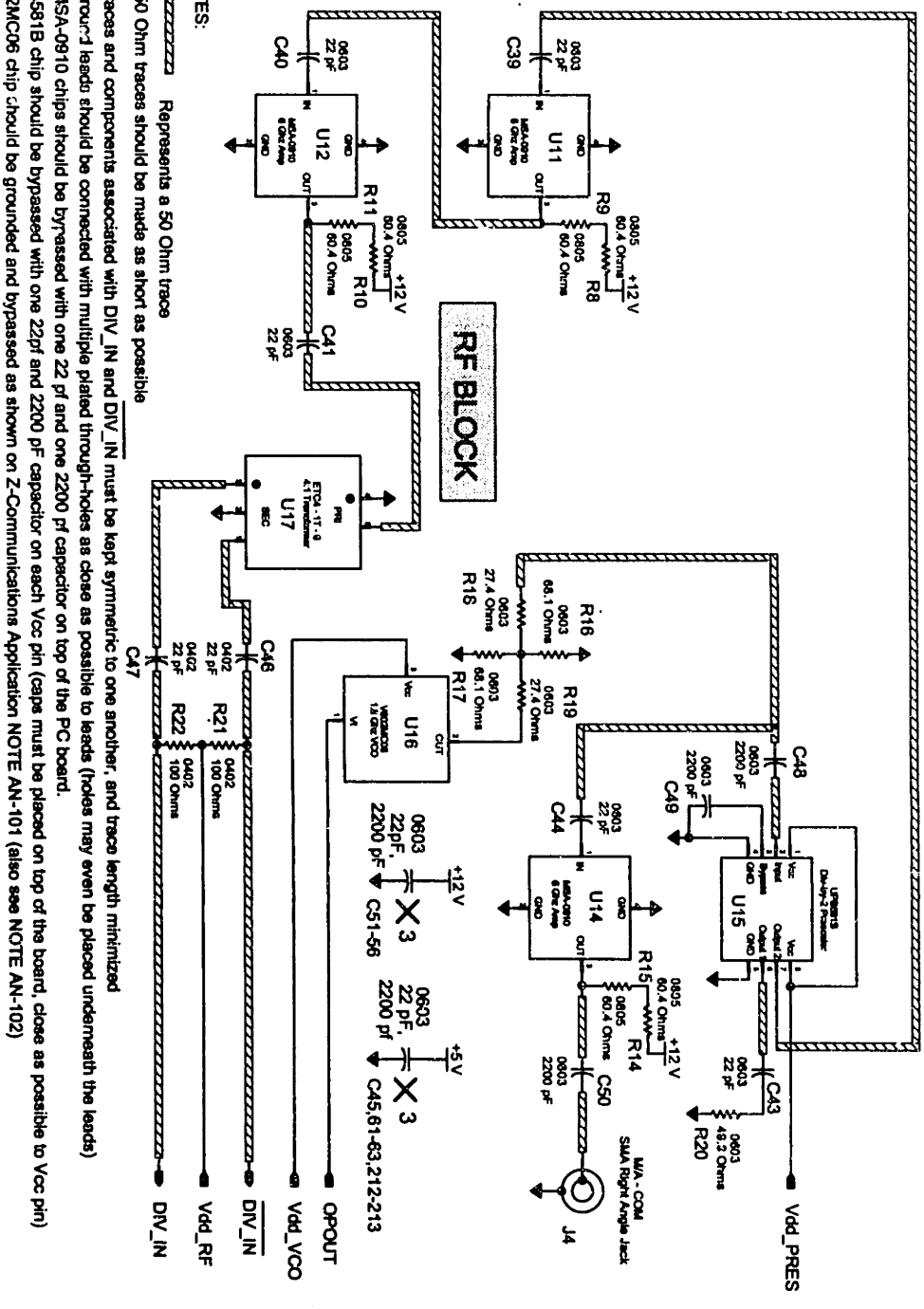

Figure A.7: Schematic diagram of RF section of PC board.

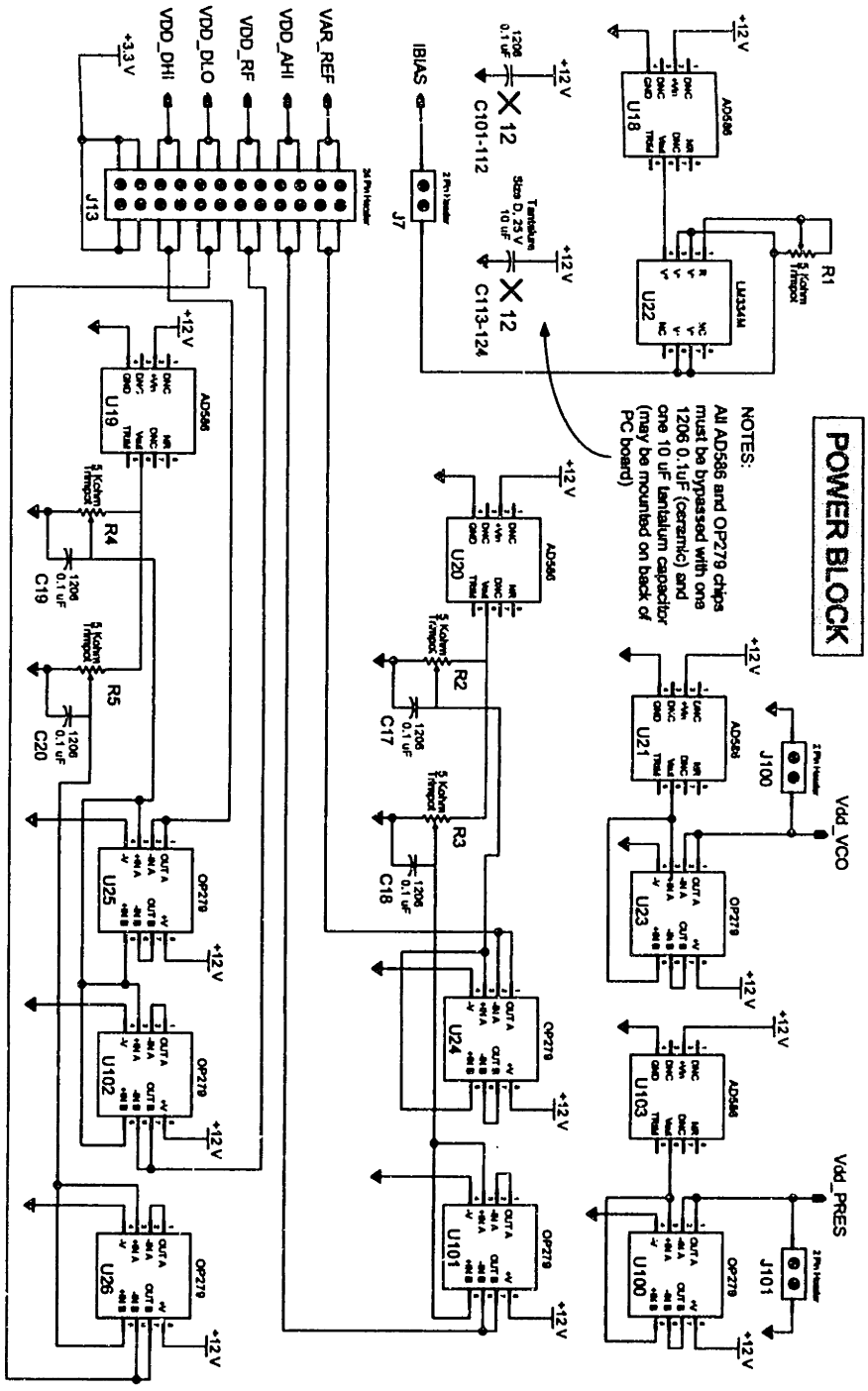

Figure A.8: Schematic diagram of power regulating section of PC board.

Appendix B

Bonding Diagram

Figure B.1 displays the bonding diagram for the custom IC used in the prototype.

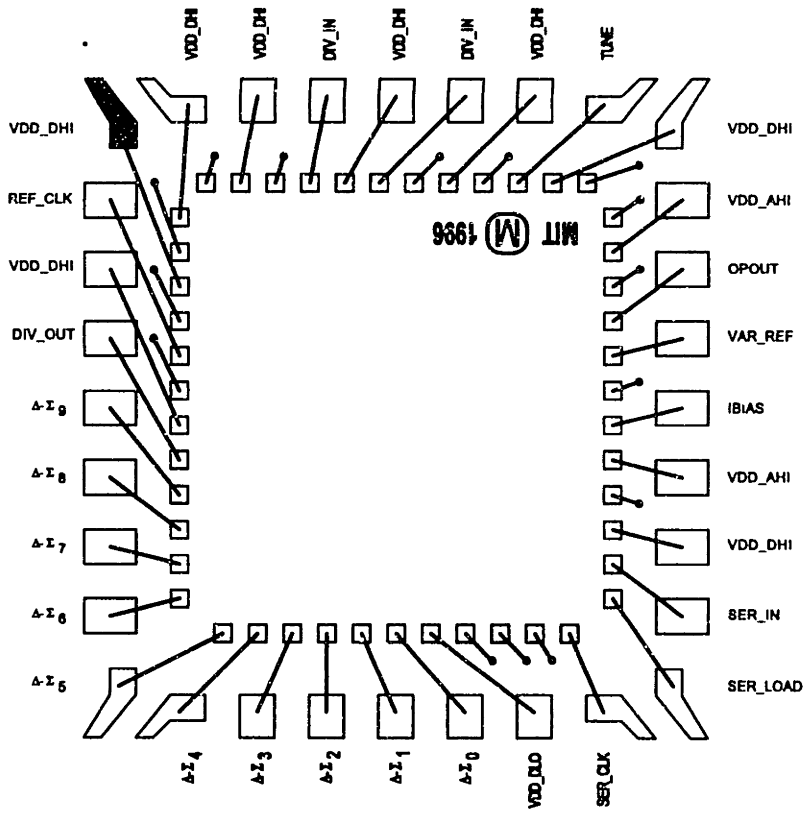

Figure B.1: Bonding diagram of custom PLL IC.