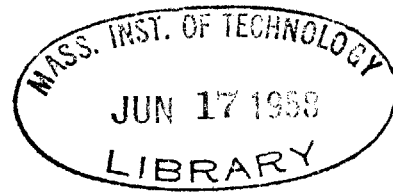# DESIGN OF A CRYOTRON COMPUTER

by

FRED HERZFELD

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

BACHELOR OF SCIENCE

at the

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June, 1958

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Signature of Author ....
Department of Electrical Engineering, May 26, 1958

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Chairman, Departmental Committee of Theses

DESIGN OF A CRYOTRON COMPUTER

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Submitted to the Department of Electrical Engineering on
May 26, 1958 in partial fulfillment of the requirements
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ABSTRACT

The work reported in this thesis is the development of the
logical and associated circuitry of a general purpose digital
computer employing cryotrons.

Following a discussion of the basic switching functions in
two forms of realizations, and a discussion of a pulse detector
with complementary output, the general organization of the
cryotron computer is presented.

Diagrams of the computer logical circuitry and the asso-
ciated terminal equipment are given. A read-out amplifier
for the low-level cryotron output was designed, constructed,
and tested in a cryotron circuit. Proper operation of the
read-out amplifiers in conjunction with cryotron circuits was
achieved. A method of building the cryotron computer in plug-
in modules is presented. Coupling between modules is mag-
netic.

Thesis Supervisor: Dr. Dudley A. Buck

ACKNOWLEDGMENT

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CHAPTER I

INTRODUCTION

1.1 HISTORY

In the evolution of science and technology the trend toward more complex systems has forced a continual search for means to miniaturize, to investigate and apply the various phenomena of solid-state devices.

In the computer field there has been the ever more important search for methods which will increase the speed of operation of the computer. There are three solutions to the combined problem of attaining small size and high speed. First, new circuitry which will permit the present relatively slow components to function more efficiently, as for example, an otherwise slow counter employing high speed carry propagation. Second, the development of new components which are inherently applicable as high speed devices. Along with these two solutions there is the possibility of reduction in size through smaller construction and packaging. The third and perhaps most important region in which we hope to find solutions to the problem is in a combination of new circuitry with new components which are not only fast but small. This then is the problem: Find a new component which is inherently small and develop the associated new circuitry. In this thesis we will be dealing mainly with the circuitry of a newly developed component.

The development of the cryotron[1] by D. A. Buck has opened another path along which we may hope to achieve both high speed and microminiaturization. The cryotron consists of a super-

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1. Superscripts refer to references listed in the Bibliography.

conductor whose superconductive state may be destroyed by the application of a magnetic field. It is a two-state device operating in the temperature region near absolute zero; dissipating power only during the transition period; easily fabricated in extremely small size; and whose upper switching frequency limit has been estimated between 100 and 1,000 megacycles.

Operation at this low temperature implies not only that the device has a very low noise level, but also that it will have an extremely long life. Its two-state nature implies simple circuitry for a binary system. Dissipation of power during the switching transition only means less formidable requirements on the power source. The small size in which the cryotron may be fabricated means that larger systems can be packaged into a smaller space. Along with these advantages there is the possibility of extreme speed as the cryotron becomes physically smaller.

1.2 OBJECTIVE

There are four parts that will be considered. First, the design of a small general purpose stored program digital computer using cryotron circuitry. Second, the design of reliable read-out amplifiers. Third, the construction of both the computer and the associated terminal equipment. Last and most important, the testing of the computer to determine the reliability of the cryotron in a large system. We will proceed from the discussion of the capabilities of the cryotron itself to the analysis of the Block Diagram logic, through the circuitry of the individual blocks and the problems of construction.

CHAPTER II

BASIC CRYOTRON SWITCHING CIRCUITS

2.1 THE SINGLE CRYOTRON

The basic component of the computer, the cryotron, is a device which depends on the destruction of superconductivity by a magnetic field.[2] The behavior of the cryotron is somewhat like an electro-mechanical relay[3] and yet between them there is a distinct difference in the number of "contacts" and in "contact resistance". A single electromechanical relay can have any number of contacts or contact pairs, while a single cryotron can have only normally closed contacts, and in the usual wire-wound form of construction has only one normally closed (superconductive) contact. The resistance of the open contact on an electromechanical relay is essentially infinite, preventing current flow. The cryotron gate (contact), on the other hand, presents approximately 0.001 ohm when resistive, thus as a series type switch it introduces only a small resistance which has little or no effect on the current flow. The closed contacts of the electro-mechanical relay present only a very small resistance, while the gate resistance of the superconductive cryotron is exactly zero. Useful switching with the cryotron can be accomplished by intro-ducing the very small gate resistance into a path in which is flowing, and at the same time providing an alternate superconductive path for the current; that is, using it as a parallel switch.

2.2 THE BASIC CIRCUITS

2.21 CIRCUITS AND NOTATION

In the design of digital computers there are a number of basic circuits from which any functional relationship may be synthesized. In particular there are the OR, AND, NOT, and INHIBIT circuits.

The FLIP-FLOP and the DELAY are also of great importance as individual circuits although they may be constructed through the use of the simpler basic circuits. A PULSE DETECTOR of importance when the input signal is not in complementary form had to be developed.

Throughout the discussion we will make use of the TRANSMISSION rather than the HINDRANCE notation, and the duality that exists between the two systems will be particularly noted in a comparison of the OR and the AND circuits.

2.22   THE OR CIRCUIT

The two general equations which specify the OR circuit may be written as:

$$F = \sum_{k}^{K} A_k \qquad\qquad \overline{F} = \prod_{k}^{K} \overline{A}_k \qquad\qquad (1a, b)$$

where the A_k's and the $\overline{A}_k$'s are the complementary inputs. F and $\overline{F}$ represent the complementary outputs. While it is usual to consider only Equation 1a for the OR function, it was stated that an alternate shunt path for the current must be provided, and this is given in equation form by the dual of Equation 1a, namely 1b. The realization of these switching functions in terms of cryotron hardware is shown in Figure 1. This is only a typical circuit, and it must be recognized that many other circuit realizations of the functions (1a, b) are possible. For the condition $F = 0$ we note that the source current I_s must flow through the control of cryotron C_2. The gate of C_2 must therefore be resistive, and that of C_1 superconductive. For any other input condition we have $F = 1$ and there are one or more gates on the F side which will be resistive, and one or more gates on the $\overline{F}$ side which will be superconductive. The source current I_s must therefore flow through the control of cryotron C_1. The outputs may be determined by sensing the gates of C_1 and C_2.
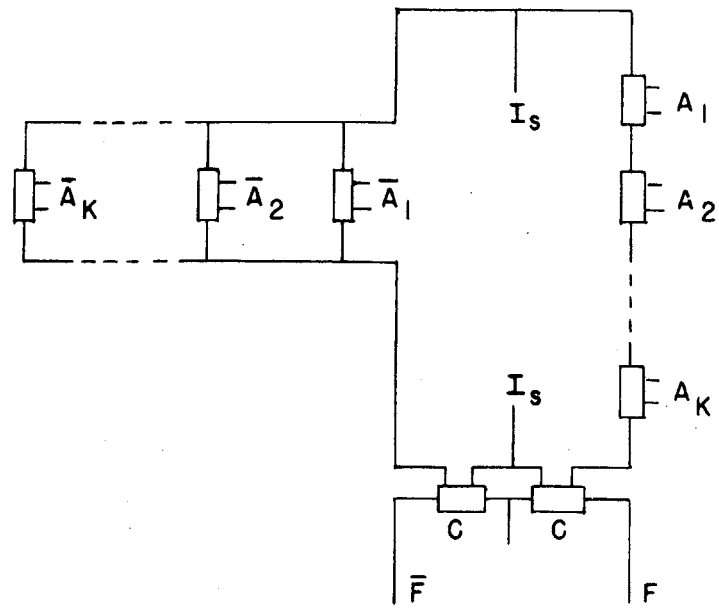
FIGURE 1   GENERAL OR   CIRCUIT
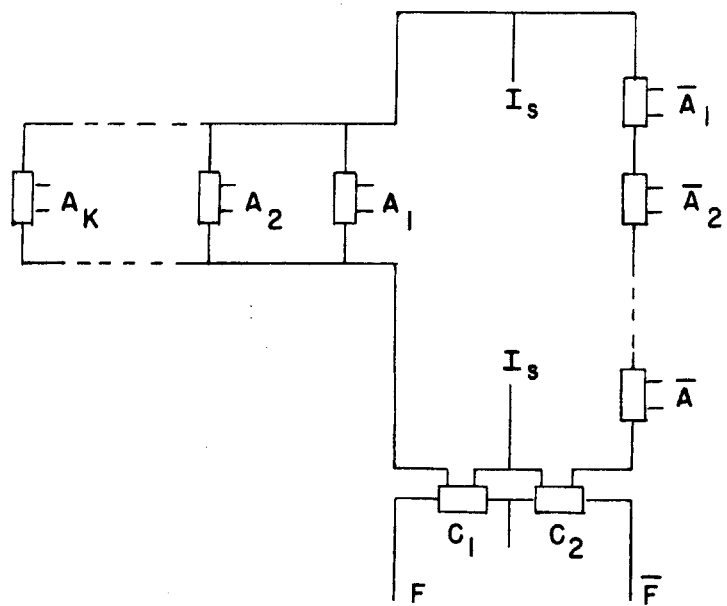
FIGURE 2   GENERAL   AND   CIRCUIT

2.23   THE AND CIRCUIT

We have previously mentioned the hindrance and transmission notations of Boolean Algebra as applied to switching circuits, the two systems being mathematical duals. Thus we may notice that the general equations for the AND circuit given by Equations 2a, b are the duals of Equations 1a, b.

$$F = \prod^K A_k \qquad\qquad \overline{F} = \sum^K \overline{A}_k \qquad\qquad (2a, b)$$

Except for an exchange in variables, 2a, b and 1a, b are identical and all that is required is an exchange of input lines and an exchange of output interpretation. This is shown in Figure 2. This duality is of particular importance in cryotron circuitry since the shunt or dual path must be present, and complementary inputs and outputs are also usually necessary.

2.24   THE NOT CIRCUIT

The NOT circuit performs an inversion of the input variable. Thus for cryotron circuitry, since both the variable and its complement are usually present, the NOT circuit may be realized by an interchange of the output lines. If however the input is not present in complementary form the reader is refered to section 2.28 where a method of obtaining the complement is given.

2.25   THE INHIBIT CIRCUIT

The INHIBIT function may be stated as:

$$F = X \cdot \overline{Y} \qquad\qquad \overline{F} = \overline{X} + Y \qquad\qquad (3a, b)$$

where Y is the inhibitor and X and Y any variables or function of variables. Figure 3 is a simple form of this function as realized without the use of dual X inputs although complementary Y inputs are required, and is a GATING TYPE realization. The INHIBIT circuit may also be realized by a proper choice of inputs to the AND circuit.

Y ·INPUT

$X\overline{Y}$
OUTPUT

X   INPUT

$\overline{Y}$ INPUT
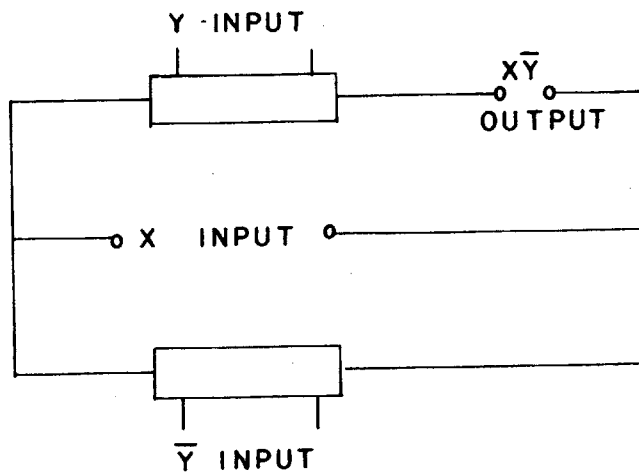
FIGURE 3   INHIBIT GATE

2.26 THE FLIP-FLOP

A simple form for the FLIP-FLOP was shown[1] to be that given
in Figure 4a, with the block symbol representing it shown in Figure 4b.
If we consider the source current I_s flowing through the gate of C_1,
the gate of C_2 being resistive, then it must also flow through the gate
of C_3 and through the controls of C_4 and C_6. In flowing through the
control of C_4 it will prevent itself from flowing through the gate of
C_2. The inputs are no longer required and the source current will
remain in the same path. If an input is now applied to the control of
C_1, the current will decay in the first path and build up in the alter-
nate one and the FLIP-FLOP WILL change its state, which may be
sensed by testing the output gates of cryotrons C_5 and C_6. For such
switching to occur the magnitude of the current I_s is given by Equation
4, and further details on the switching may be found in reference 4.

$$I_c < I_s < 2I_c \tag{4}$$

where I_c is the magnitude of the current at the threshold of switching.

2.27 THE DELAY

A digital time delay may be achieved by interconnecting a series
of FLIP-FLOPS in such a manner that a pulse travels down the line,
flipping one after the other, as shown in Figure 5. Input and output
gates may be combined thus requiring only four cryotrons per delay
time plus two output cryotrons. By using only four cryotrons it is
also possible to get short unit delay times.

2.28 COMPLEMENTARY-OUTPUT PULSE DETECTOR

It is pointed out above that the cryotron lends itself best to
complementary circuitry. There are however times when com.pple-
mentary inputs are not readily available, as for example in pulse
detection, and it is necessary to use a circuit which will convert
the presence or absence of a pulse into complementary outputs, one

ONE INPUT   CR 1   CR 3   CR5 ZERO OUTPUT

I_s

ZERO INPUT   CR 2   CR 4   CR 6 ONE OUTPUT

(A)

ONE INPUT   FLIP-FLOP   ZERO OUTPUT
I_s I_s
ZERO INPUT   ONE OUTPUT
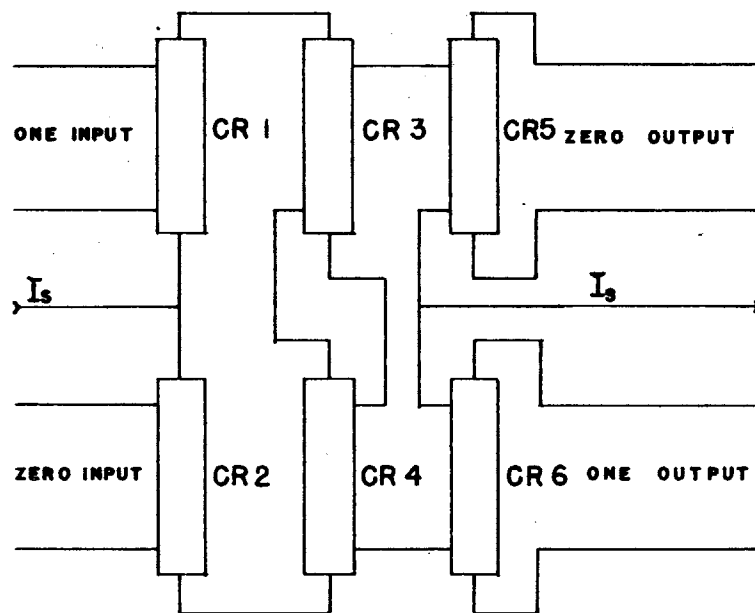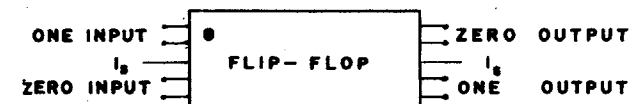
(B)

FIGURE 4   (A) CRYOTRON FLIPFLOP CIRCUIT   (B) BLOCK SYMBOL

PULSE INPUT

DELAYED
OUTPUT PULSE

C   FF   FF   FF   FF

I_s

COMPLEMENT
OUTPUT
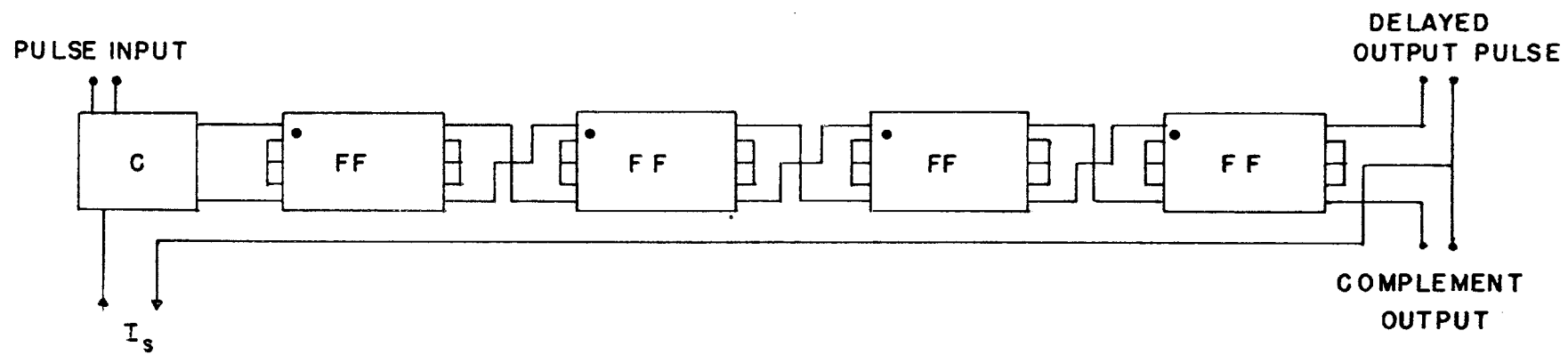
FIGURE 5   CRYOTRON   DELAY CIRCUIT

indicating that a signal is present and the other indicating that there is no signal. The circuit diagram of such a pulse detector is shown in Figure 6.

When there is no input pulse, cryotrons C_1 and C_3 have no current flowing in their control windings. The gates of C_1 and C_3 are therefore superconductive. The source current I_s has only one path available through which it may flow, namely through the control of C_2 and the gate of C_1. This is the only superconducting path since there is a resistance in series with the other, produced by the gate of C_2 through the control of which the source current must always flow. This method of producing the resistance is used in order that the magnitude of the resistance is approximately that of any normal gate; however any resistance of proper magnitude may be substituted. Thus the current must choose the path which is entirely superconductive.

If there is a pulse present, C_1 and C_3 have current flowing in their control windings. The gates of C_1 and C_3 are therefore resistive. The source current I_s now has two parallel resistive paths in which to flow, and the current in the control of C_4 is determined by the ratio of the two resistances. Assuming that the resistances are equal, the current in the control of C_4 will be less than I_c, the transition current (the restriction on I_s is again given by Equation 4.) and the gate of C_4 will be superconductive, while the gate of C_3 is resistive.

As shown in the diagram the source current I_s may be applied to the gates of C_3 and C_4 to sense their state and the outputs thus obtained labeled NO INPUT and YES INPUT.

INPUT

NO INPUT

CR3

CR1

CR4

CR2

YES INPUT

I_s
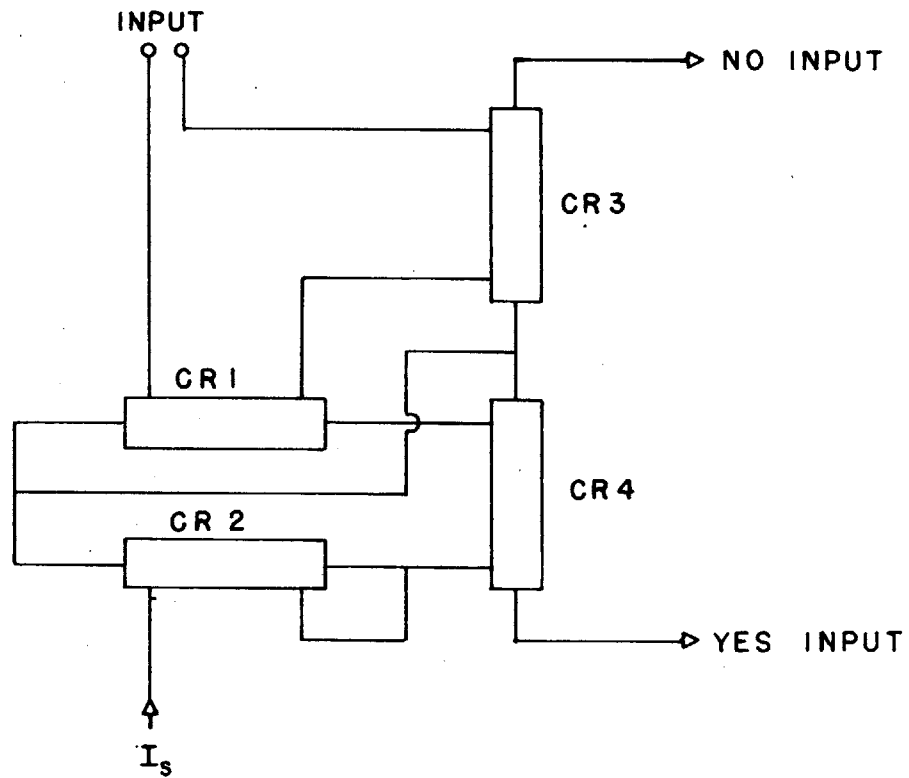
FIGURE 6   COMPLEMENTATION   CIRCUIT

CHAPTER III

GENERAL ORGANIZATION

3.1 SPECIFICATIONS

The design of a computer must start with a decision as to what the computer is to be capable of performing. Since the purpose of this thesis is to develop the logical and associated circuitry of a general purpose digital computer using cryotrons for all of the switching elements, it is of importance to decide which functions or commands will best illustrate the use of cryotrons in a large system and provide a means for evaluating the performance of the system. For this purpose we have chosen to design a single address machine which has the 14 instructions listed in Table 1. While these 14 are only a few of the many instructions which could be built into the computer they will serve to illustrate the design principles. The number of digits in a word determines the precision with which the computer can handle numbers, and for the cryotron computer a word length of 11 binary digits was arbitrarily chosen. If one of these 11 is used for the sign digit (or the Tag for instructions) the number of digits for the address part of an instruction is fixed at 6 and the number of words in storage at 64. With 64 storage locations it will be possible to operate the computer with several program loops for long-time operation evaluation.

The computer panel was designed to provide as much flexibility as could reasonably be expected. The panel layout is shown in Figure 7. It provides visual observation of the data in the ACCUMULATOR, INPUT and OUTPUT registers, the INSTRUCTION COUNTER and the CONTROL register. For each of these there is a set of switches, (S), provided for manually correcting or setting the data at any of the mentioned units at a computer HALT POINT, and a push button,(P), for transfering the information

TABLE I

INSTRUCTION	SYMBOL	CODE	DESCRIPTION
Stop	STP	0000	Computer stops regardless of information in address part of instructions. Indicates STOP on panel.
Add	ADD	0001	The number stored at the indicated address is added to the contents of the accumulator, and the sum remains in the accumulator.
Subtract	SUB	0010	The number stored at the indicated address is subtracted from the contents of the accumulator and the difference remains in the accumulator.
Multiply	MUL	0011	The number stored at the indicated address is multiplied by the contents of the accumulator. The eleven least significant remain in the M register.
Clear and Add	CLA	0100	The accumulator is reset to zero and the number stored at the indicated address is placed in the accumulator.

Store	STR	0101	The number in the accumulator is placed in the indicated storage location; previous content of the storage location is discarded, and the contents of the accumulator remain unchanged.
Transfer	TRA	0110	The next instruction is taken from the address indicated.
Transfer if Negative	TRN	0111	The next instruction is taken from the address indicated if the sign of the accumulator is negative, otherwise the next instruction is taken in normal sequence. Zero is interpreted as negative.
Transfer on Overflow	TRO	1000	The next instruction is taken from the address indicated if an overflow occured on the previous operation, otherwise the next instruction is taken in normal sequence. Overflow register reset; accumulator remains unchanged.
Shift Right	SHR	1001	The number in the accumulator is shifted to the right by the number of places indicated in the address part of the instructions. Sign remains unchanged. Shifted digits enter the M register.

| Shift Left | SHL | 1010 | The number in the accumulator is shifted to the left by the number of places indicated in the address part of the instructions. Digits shifted to the left of the tenth order are discarded. Sign remains unchanged. |

| Print | PRT | 1011 | The word at the indicated address is placed in the PRINT register and printed by the Flexowriter as a SIGN plus four octal digits. |

| Halt Point | HLT | 1100 | Computer comes to a halt. All registers remain unchanged. Computer will start with the next instruction in sequence when ex-restarted. Indicates HALT on panel. |

| Read In | RDN | 1101 | The number in the input register is placed in the memory at the location specified by the address part of the instructions. Previous contents of the memory location are discarded. |
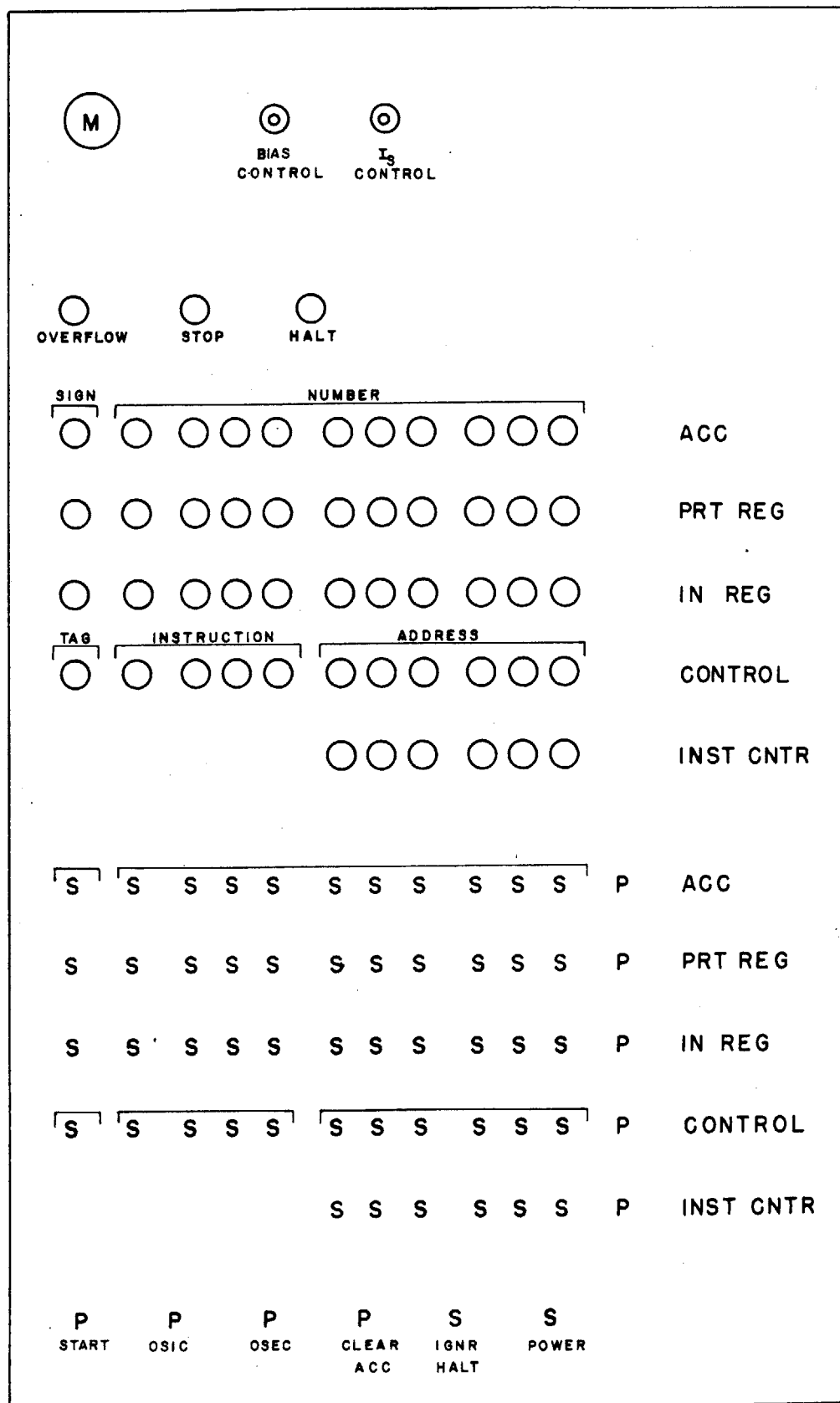
FIGURE 7   COMPUTER   PANEL

stored in the switches to the respective register. Visual indication is provided for the OVERFLOW, PROGRAM STOP and HALT POINT. Switches are provided for PROGRAM START, OPERATE SINGLE INSTRUCTION CYCLE, OPERATE SINGLE EXECUTION CYCLE, CLEAR ACCUMULATOR, CLEAR INSTRUCTION REGISTER, and IGNORE HALT POINT.

A meter and two potentiometers are provided to monitor the source current and properly set the level of the read-out amplifiers.

3.2 PULSE SEQUENCE

From the basic Block Diagram of the cryotron computer, Figure 8, the sequence of pulses necessary for the various instructions was determined. To minimize the number of such pulses for a given instruction, the sequence was arranged so that a given pulse could perform several functions simultaneously. The generation of the pulses and the switching networks which distribute them are discussed in detail in Chapter IV of this thesis; in this section the pulse sequences for each of the various instructions are determined. Each sequence is divided into two distinct cycles - the instruction cycle and the execution cycle.

3.21 THE INSTRUCTION CYCLE

One of the pulses of every command either advances the instruction counter by ONE or, if it is a transfer command, places the transfer address in the instruction counter. The last pulse from any of the execution matrices routes the clock pulses to the instruction cycle selection matrix. If the computer is being started manually the instruction counter is set to the address of the first instruction (usually zero) and the clock pulses are diverted from both the instruction cycle and the execution cycle matricies until the START
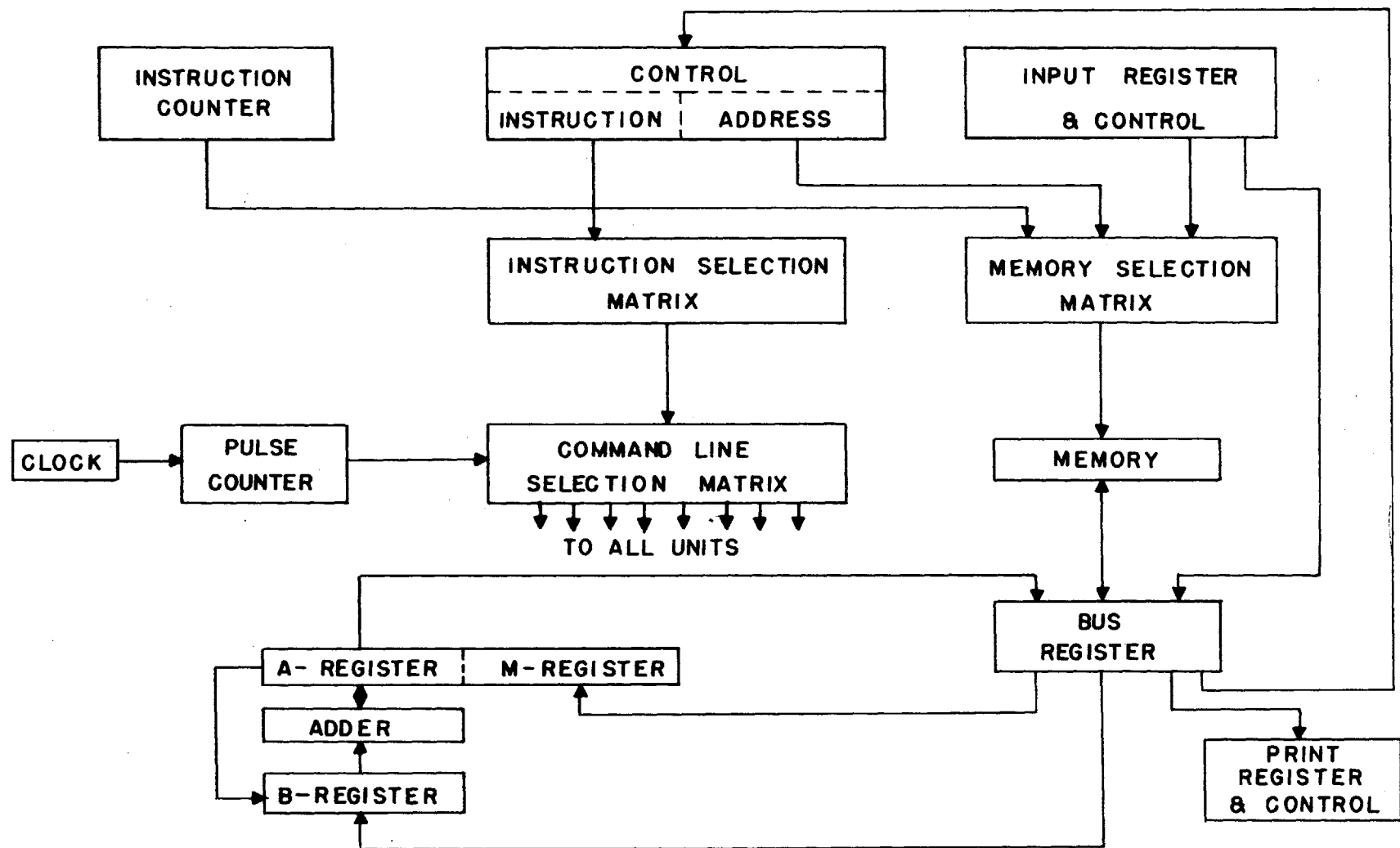
FIGURE 8   BLOCK DIAGRAM OF CRYOTRON COMPUTER

button is depressed. The pulse sequence to the various command lines for performing the INSTRUCTION CYCLE is given in Table 2.

3.22 THE EXECUTION CYCLE

The pulse sequence during the operation of the EXECUTION CYCLE is also determined from the Block Diagram. Since one of the instructions allows a TRANSFER ON OVERFLOW, the first pulse in every sequence with the exception of the PRINT is a test for overflow. The pulse sequence for the various commands during the execution cycle is given in Table III. Having determined the sequence of pulses that is required for the various arithmetic operations we turn to the design of the individual units.

TABLE II

PULSE NUMBER	OPERATION
P_0	Cut off command lines
P_1	Read Memory into Bus
P_2	Read Bus into Control
P_3	Switch clock to execution cycle.

TABLE III

PULSE NUMBER	OPERATION
ADDITION	
P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Memory into Bus
P_3	Read Bus into B register
P_4	Read A register into Adder Read B register into Adder Pulse Carry to Add
P_5	Read sum into A register Advance Instruction counter
P_6	Switch clock to instruction cycle
SUBTRACTION	
P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Memory into Bus
P_3	Read $\overline{\text{Bus}}$ into B register
P_4	Read A register into Adder Read B register into Adder Pulse Carry to Add.
P_5	Read sum into A register Advance Instruction counter
P_6	Switch clock to instruction cycle.

STORE

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read A register into Bus
P_3	Read Bus into Memory Advance Instruction Counter
P_4	Switch clock to instruction cycle

TRANSFER

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Address into Instruction counter
P_3	Switch clock to Instruction cycle

TRANSFER IF NEGATIVE

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read address into Instruction counter if sign of A register is negative
P_3	Switch clock to Instruction cycle

TRANSFER ON OVERFLOW

P_0	Cut off command lines
P_1	Pusle TRANSFER ON OVERFLOW line
P_2	Switch clock to Instruction cycle

STOP

P_0	Pulse to STOP flip-flop of clock

MULTIPLY

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Memory into Bus
P_3	Read A register into B register via complement if necessary Read Bus into M register via complement if necessary Store sign in SIGN storage register
P_4	ZERO set A register ZERO set Adder
P_5	Read A register into Adder Read B register into Adder Pulse carry to Add if right hand order of M register is ONE
P_6	Read sum into A register if right hand order of M register is ONE
P_7	Shift Right
P_8	Zero set sign order

The sequence of pulses P_5, P_6, P_7, and P_8 each occur a total of ten times in the above sequential order

P_{45}	Complement A register if necessary via sign storage register
P_{46}	Advance Instruction counter
P_{47}	Switch clock to instruction cycle

HALT

P_0	Pulse to Halt flip-flop of clock

READ IN

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Input Register into Bus

P_3	Read Bus into Memory Advance Instruction counter
P_4	Switch clock to instruction cycle

CLEAR AND ADD

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read Memory into Bus
P_3	Read Bus into B register ZERO set A register
P_4	Read A register into Adder Read B register into Adder Pulse carry to Add
P_5	Read sum into A register Advance Instruction counter
P_6	Switch clock to instruction cycle

SHIFT RIGHT

P_0	Cut off command lines
P_1	Test for overflow
P_2	Read $\overline{\text{ADDRESS}}$ into counter
P_3	Advance instruction counter
P_{a1}	First shift right pulse
P_{an}	Last shift right pulse
P_{am}	Switch clock to instruction cycle

SHIFT LEFT

Identical to SHIFT RIGHT except that P_{a1} through P_{an} go to shift left command line

PRINT

P_0	Cut off command lines
P_1	Read memory into Bus
P_2	Read Bus into Print register ZERO set print counter
P_3	Advance instruction counter
P_4	Pulse to print flip-flop
P_5	Detour clock pulses from print command line selection matrix counter

CHAPTER IV

COMPUTER CIRCUIT

4.1 THE MEMORY UNIT

4.11 THE MEMORY

The cryotron Flip-Flop memory of the computer was designed to read information into and out of the Bus register. Each bit in the memory consists of a flip-flop and two gating cryotrons as is shown in Figure 9. The output gates of the same order in each word are connected in parallel and are labeled BI (Bus Input) as are the input controls of the same order in each word (labeled BO - Bus output). The two gating cryotrons for each bit determine whether that particular bit will deliver a pulse to the Bus or receive a pulse from the Bus. The gating cryotrons of every bit in a word are all connected in series and are driven by the complementation circuit, as shown, so that when there is no input to the complementation circuit these gates are cut off, or resistive. When a complementation circuit has an input applied, the gating cryotrons of this word are superconductive. Selection of a word, then, is accomplished by applying an input to the complementation circuit which represents the chosen word. Reading to and from the Bus is now accomplished by a pulse to either command line 11 or 12.

The current on either of the command lines (11 or 12) can flow only through the bit selection gates of the selected word thus preventing other words from responding.

The source current for the complementation circuits is not shown in Figure 9. However, all the source currents in the computer are in series, and therefore only one external current source is required.
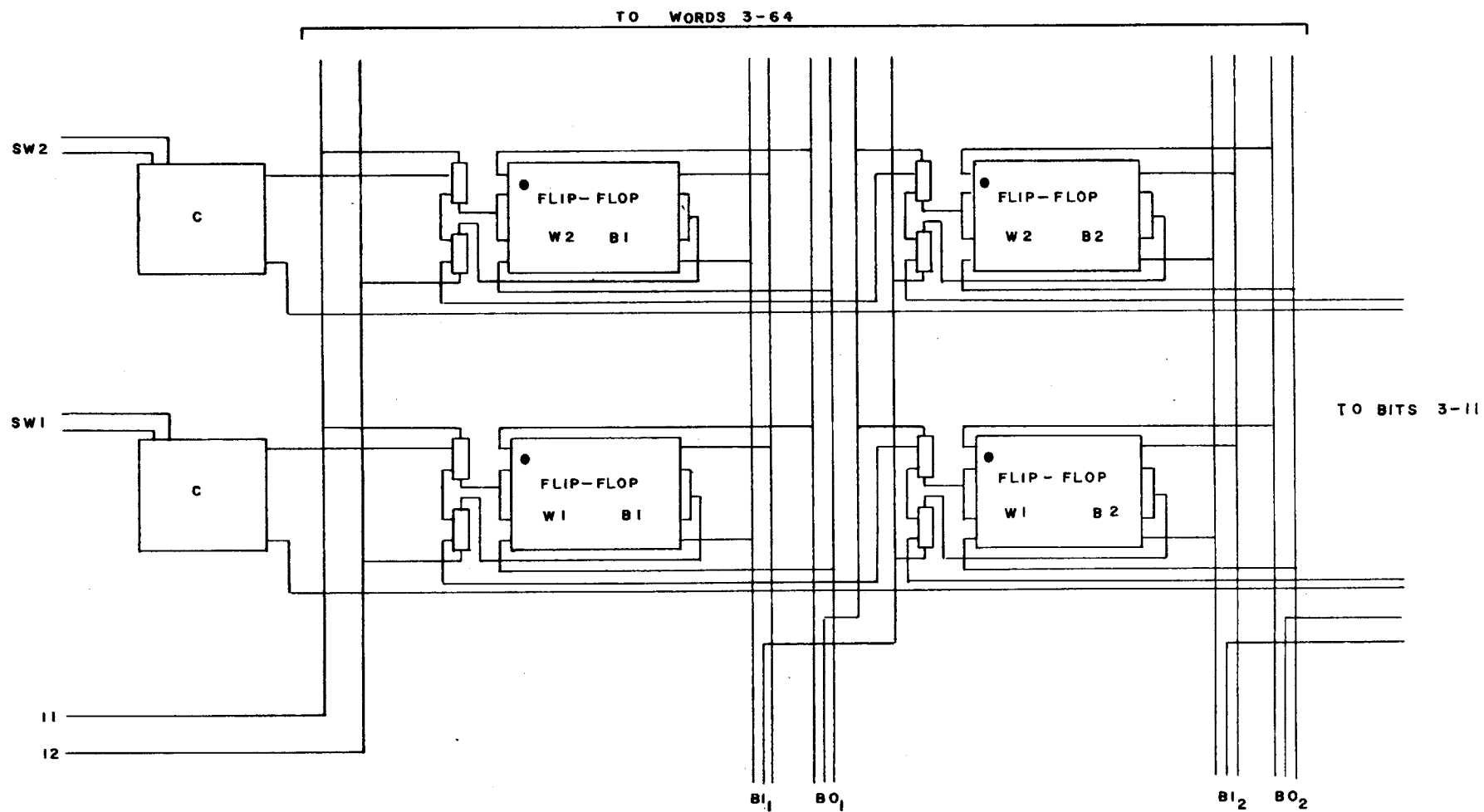
FIGURE 9   CRYOTRON FLIP-FLOP MEMORY WITH COMMAND LINES TO BUS REGISTER

4.12 THE MEMORY SELECTION MATRIX

The **MEMORY SELECTION MATRIX** is realized in the form of a tree rather than a rectangle in order to reduce the number of cryotrons in any series path, and therefore to reduce the time constant of the circuit. The circuit is shown in Figure 10. The outputs of the six digits of the **ADDRESS** part of an instruction enter at the top of the Figure, and a source current I_s enters the tree and is distributed through the gates as shown. The output lines, labeled 0 through 63, go to the respective word selection complementation circuit inputs denoted SWxx in Figure 9.

4.2 THE PRINT UNIT

4.21 THE PRINT REGISTER

The **PRINT REGISTER** operates along the same lines as the memory, requiring only one gating cryotron per bit. The register is always being read out into the **PRINT TRANSLATION MATRIX**, by the current I_s and the information is changed by properly applying pulses to the complementation circuits. Flip-Flop FF_s stores the sign of the word to be read out. FF_1 stores the most significant digit, and all other FF's are grouped in threes as an octal code. The four output lines go to the TEN POSITION SWITCH. The circuit is shown in Figure 11.

4.22 TEN POSITION SWITCH FOR PRINT TRANSLATION MATRIX

The TEN POSITION SWITCH, Figure 12, is used to convert the output of the PRINT REGISTER into ten separate lines for the PRINT TRANSLATION MATRIX. Although the two matrices could have been combined in one circuit it was decided to perform the functions separately.
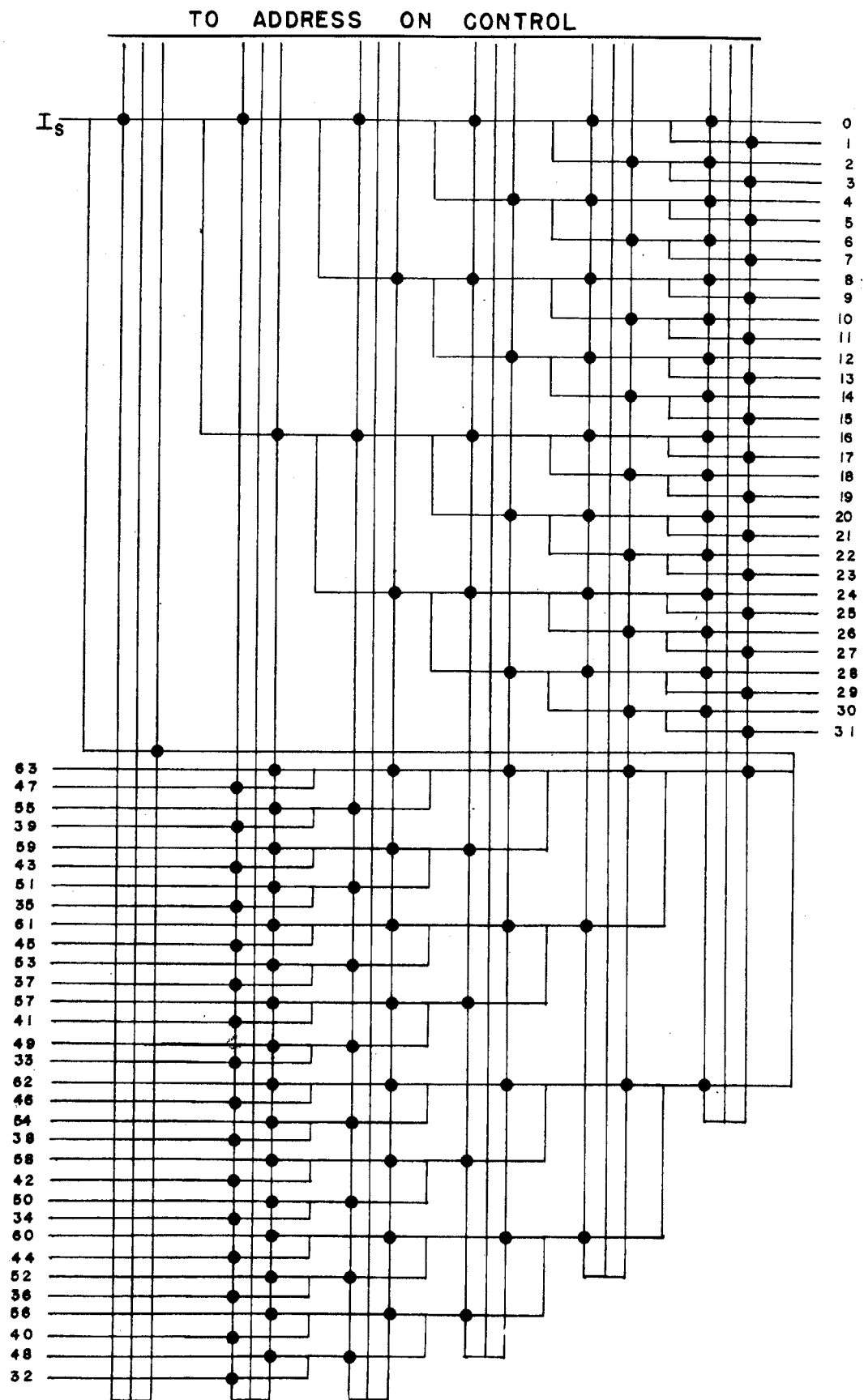
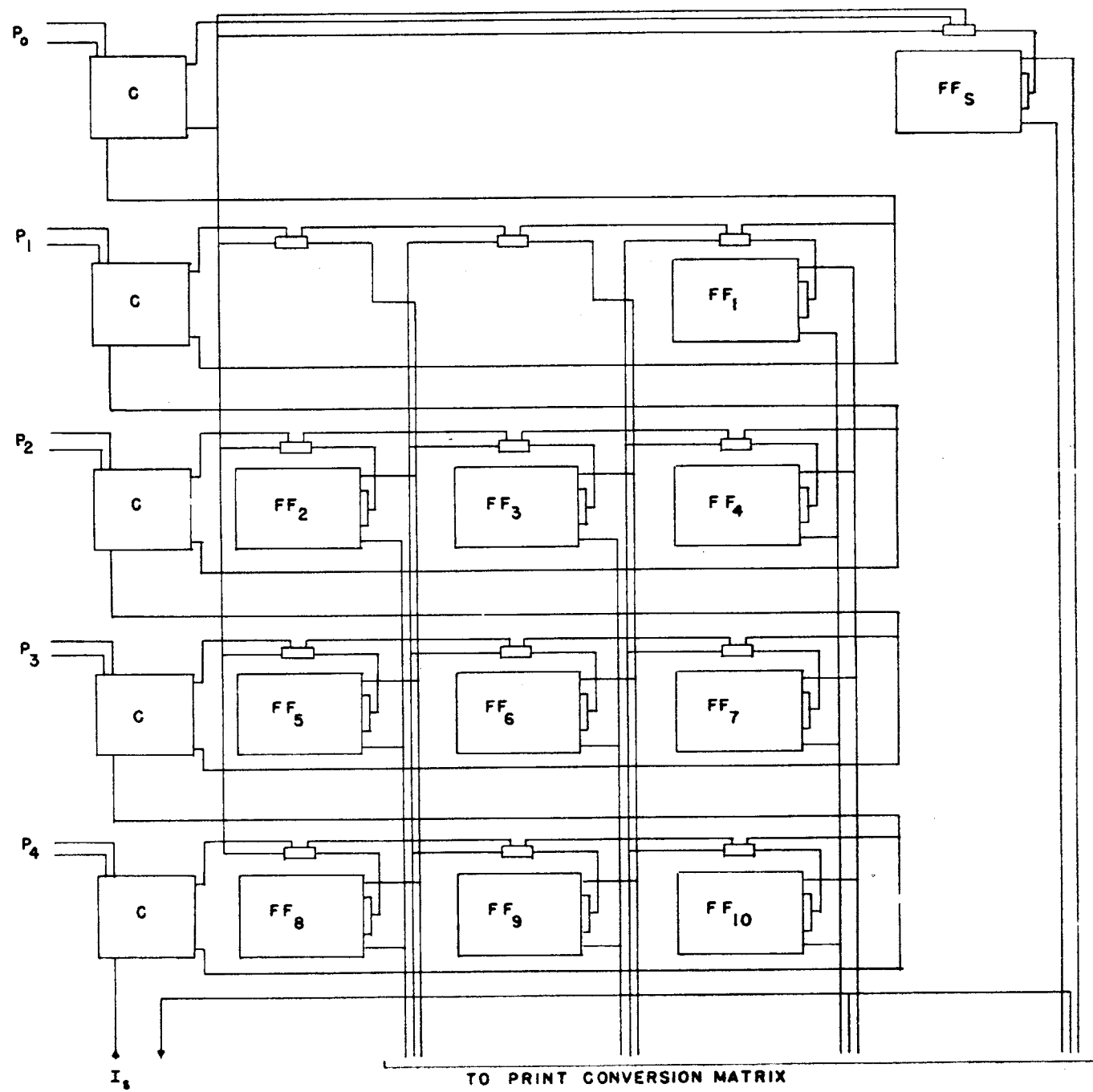FIGURE 10   MEMORY   SELECTION   MATRIX   TREE

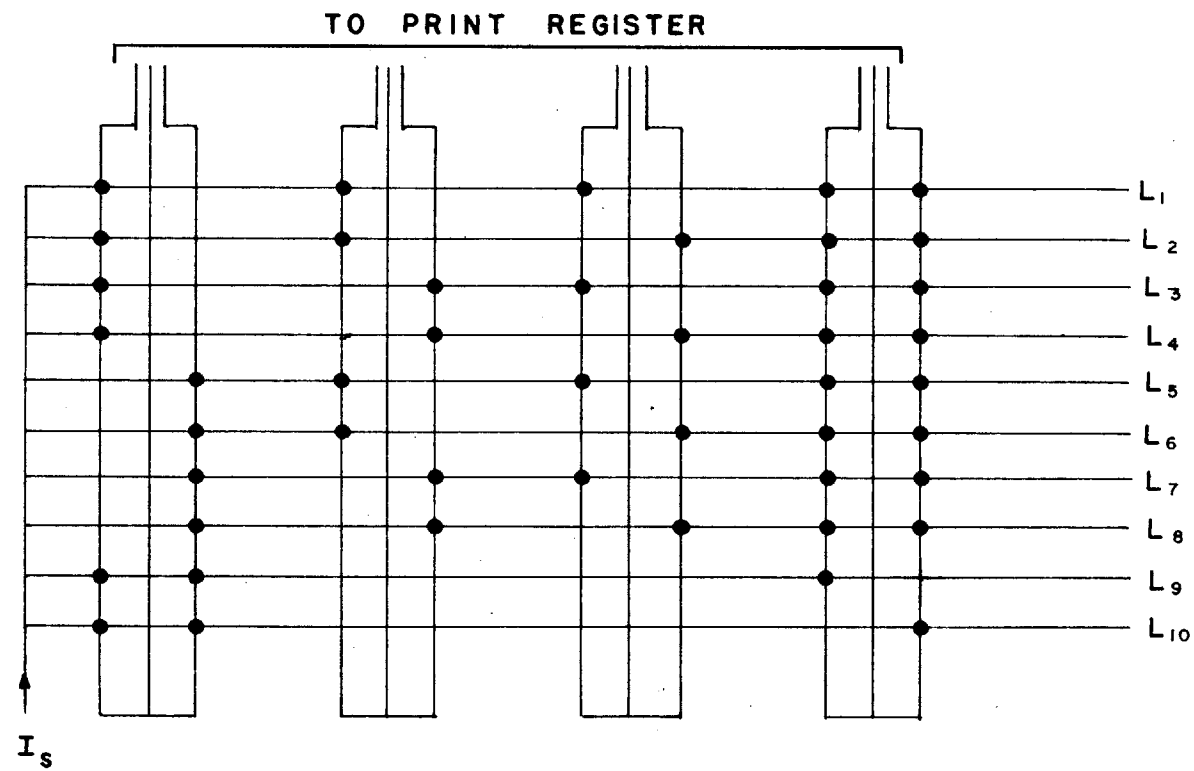FIGURE 11   PRINT REGISTER FOR OCTAL PRINTOUT WITH SIGN

TO PRINT REGISTER

I_s

FIGURE 12   TEN POSITION SWITCH FOR PRINT TRANSLATION MATRIX

4.23   THE PRINT TRANSLATION MATRIX

The PRINT TRANSLATION MATRIX, Figure 13, performs the operation of translating the digits of a word, including the sign digit, into the Flexowriter code. The inputs L_1 to L_{10} come from the ten position switch of section 4.22. The outputs of the matrix labeled CR_{20} to CR_{25} go to the respective controls of the gates driveing the core transformers, as shown in Figure 14.

4.24   FLEXOWRITER PRINT ROUTINE CIRCUIT

The circuit for the Flexowriter routine is shown in Figure 14. The Flexowriter is prepared to accept and print data supplied by the computer by depressing the START-READ switch on the body of the Flexowriter. This has the effect of locking up relay RMA, which is driven by the Flexowriter. I_2 will enter the circuit via normally open (NO) contacts of RMA, switching CR_2 to the normal state. The source current I_s has the choice of output gates on FF_1 depending on the state of the FF. Assuming that a ONE is stored in FF_1, the source current must go to the delay, and then through the gate of CR_1 (CR_2 is normal) and thus set FF_1 to ZERO. The output current of FF_1 is therefore switched to FF_2, which is initially set to NO PRINT (ONE).

If FF_1 is initially in the proper state then the output current of FF_1 is already present at the output gates of FF_2.

During the execution of a print instruction the proper word from the memory is placed in the print register and the counter (Figure 14) set to ZERO. The ZERO output of the counter transfers the SIGN part of the word to be printed to the six coding gates CR_{20} through CR_{25}, which in turn properly set the coding contacts RMC_1 through RMC_6. These contacts are on the respective relays RM_1 through RM_6 which are driven by the read-out amplifiers whose input is from
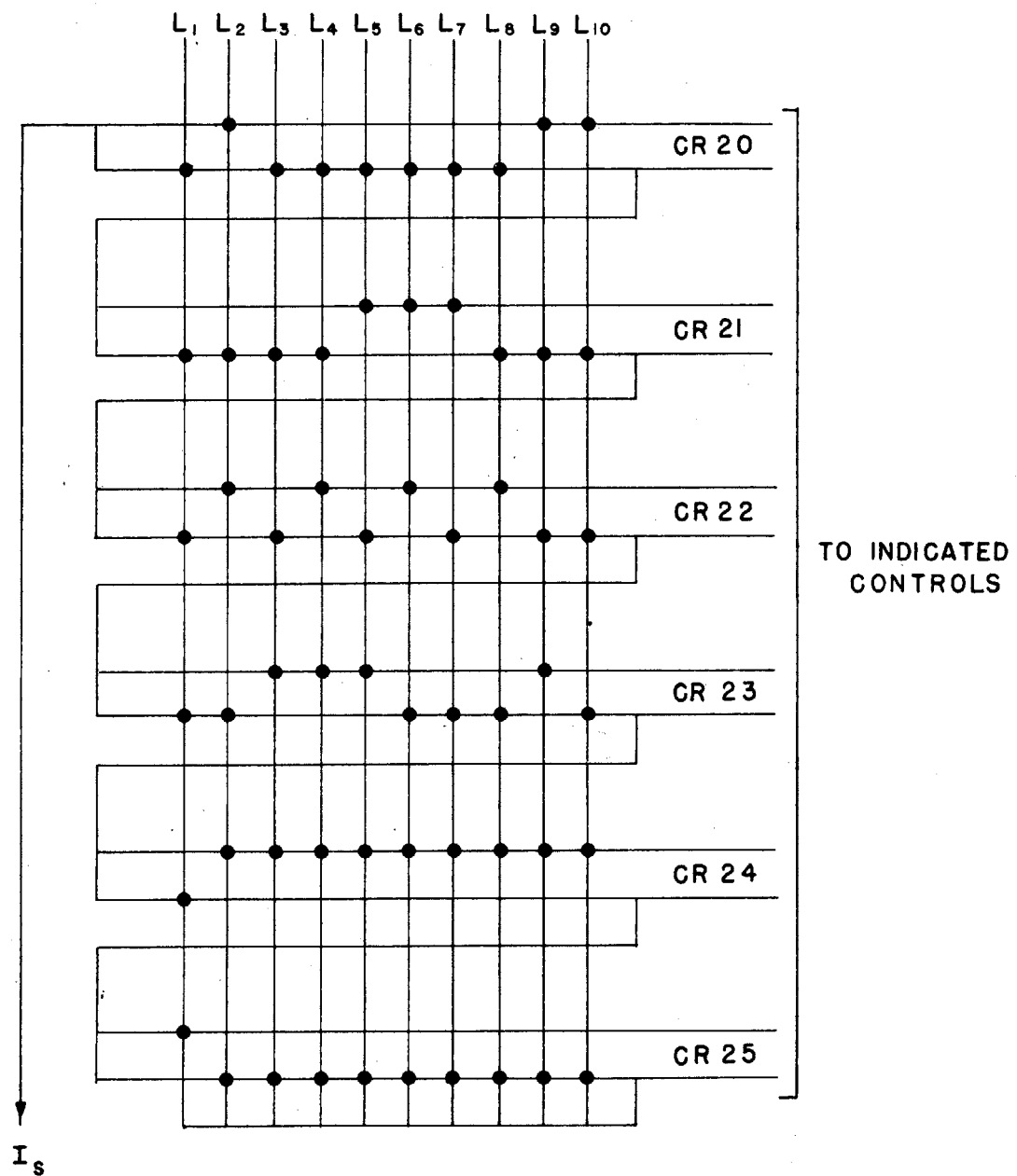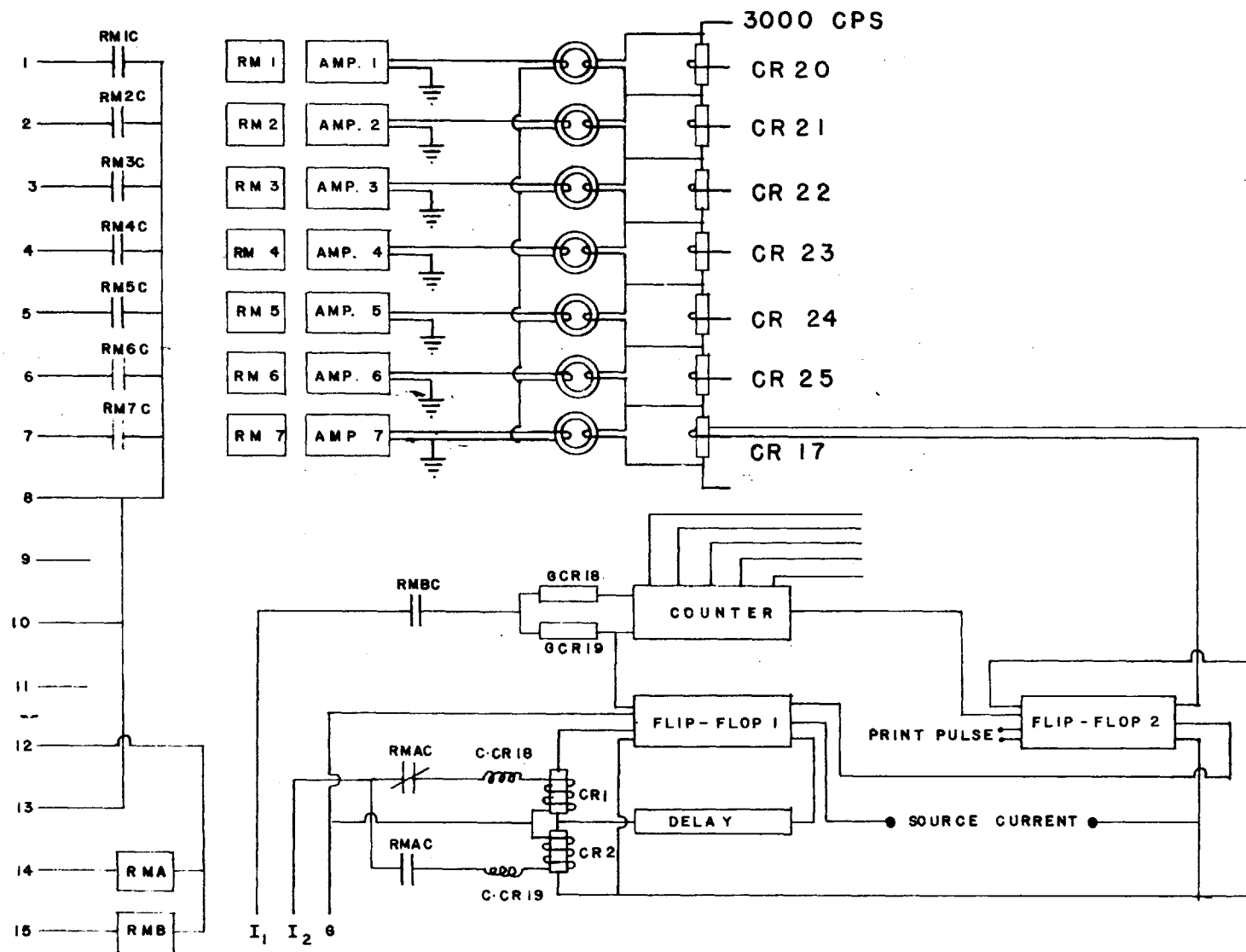
FIGURE 13   PRINT TRANSLATION MATRIX

FIGURE 14   FLEXOWRITER PRINT ROUTINE CIRCUIT

the secondary of the core transformers, the primaries having an input when any of the gates of CR_{20} to CR_{25} is normal. The last pulse from the print instruction sets FF_2 to PRINT (0). I_s must now flow through the control of CR_{17}. The signal across the gate of CR_{17} produced by the 3000-cycle source will close contact RM_7 and the Flexowriter will print the character as determined by the coding contacts. When the Flexowriter printer has started to strike the key and the information as presented by the coding contacts is no longer required, RMB closes for 20 milliseconds, as determined by the Flexowriter. This action allows I_1 to advance the counter through the gate of CR_{18}, setting FF_1 to ONE. I_s is therefore removed from the output gates of FF_2, and the gate of CR_{17} returns to the superconductive state, preventing the printing of another character. The delay is just long enough for RMC_1 through RMC_6 to be reset according to the new character placed in the coding gates before I_s complements FF_1 and again cuts off the gate of CR_{17} enabling the Flexowriter to print the new character.

During the three operations, Carriage Return, Tabulate, and Back Space, RMA releases and I_2 must flow through the gates of CR_1 and CR_{18}. This action will prevent a character being printed during the longer time required for these three characters, since during this time the gate of CR_{17} remains superconductive. When the operation of Carriage Return, Tabulate, or Back Space has ended RMA will again lock-up, and I_1 again flow through the control of $CR_{,2}$.

When the last character has been printed, the output of the counter will pulse FF_2, preventing any further action of the Flexowriter and at the same time send a pulse to start the next INSTRUCTION CYCLE.

4.3   HIGH SPEED FAST ACCESS COUNTER

The design of a pulse counter for use in a digital computer must

have the property of being able to count at a pulse repetition rate at least as high as the maximum frequency at which a single internal command line may be pulsed. In applications where the counter is used to monitor the clock pulses prior to or during the performance of an instruction the counter must be able not only to count reliably at the frequency of the associated clock, but also to present the count to other parts of the computer as quickly as possible. This means that all transients must die as quickly as possible, implying that the propagation time of the carry must either be minimized or completely eliminated. The counter developed for use in the cryotron computer is based on this principle.

Each digit or order, of the counter as shown in Figure 15 consists of two sets of flip-flops. The input pulse enters the counter at the lowest order. Pulse steering is performed by a set of read-out gates in the GATE flip-flops of each order, the steering being dependent on the digit presently stored in the order. If the digit is a ONE, the pulse is steered to the pulse steering gates of the next higher order, but in doing so passes through the zero-set control of the HOLD flip-flop of the order. Alternatively, if the digit stored is a ZERO, the pulse is steered through the one-set control of the order, from which it is returned to the pulse source. Thus an incoming pulse is steered through all orders containing ONE's setting the HOLD flip-flops of these orders to ZERO. At the lowest order containing a ZERO the pulse will return to the pulse source and at the same time set to ONE the HOLD flipflop of the order. The count stored in the higher orders therefore remains unchanged. The HOLD flip-flops of all orders now contain the new count, and prior to the arrival of another pulse the GATE flip-flops must be reset to corespond to the HOLD flip-flops for proper steering of the next pulse. This is achieved by a set of read-out gates in the HOLD flip-flops of each order, arranged so
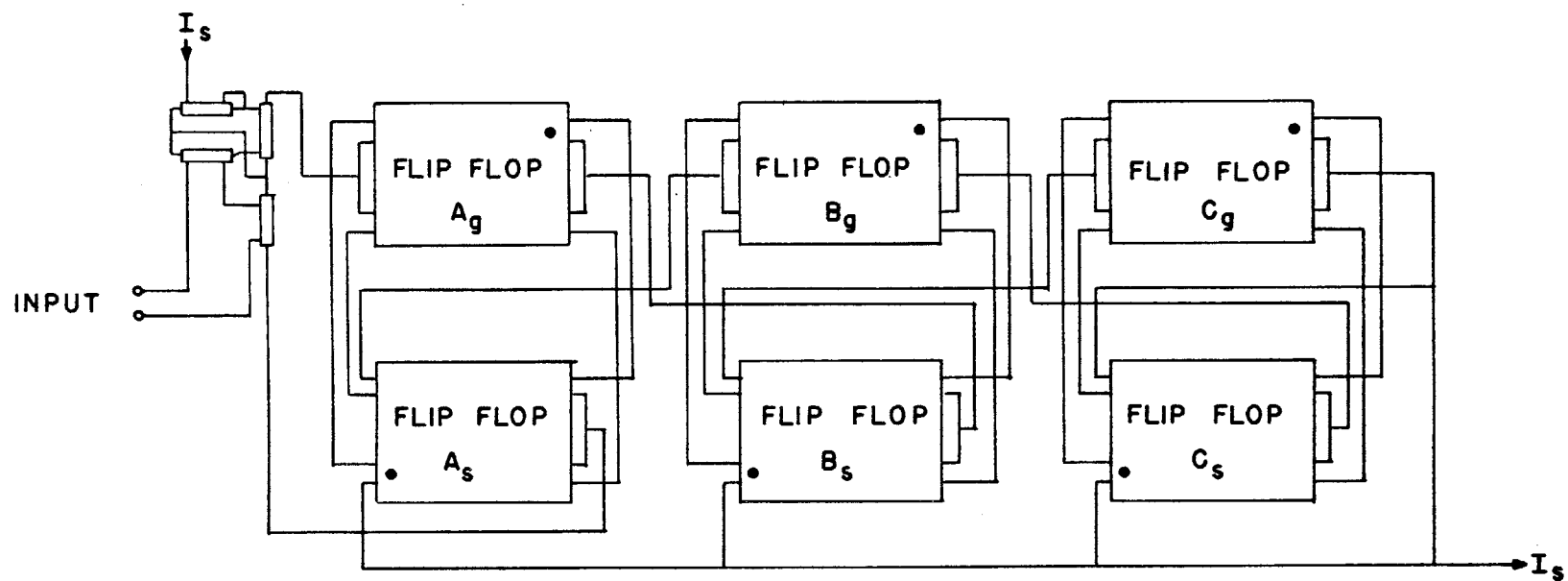
FIGURE 15   HIGH SPEED FAST ACCESS COUNTER

that all orders will simultaneously transfer the count upon initiation of a pulse to the GATE SET LINE. A complementary-output pulse detector as described in section 2.28 of this thesis is used for this purpose, the YES INPUT output being used to drive the counter itself and the NO INPUT output being used to drive the GATE SET LINE.

It is interesting to note that when the input pulse to the counter has ended the proper count is already stored in the HOLD flip-flops. Thus the count is ready for reading into other sections of the computer, the time between pulses being used to properly reset the steering gates. There is no propagation time to delay the availability of the count.

Output gates are not shown but may be placed either in the HOLD flip-flop or the GATE flip-flop depending on the time one wishes the count to change, and this may in some instances obviate the use of a DELAY circuit.

4.4   THE ACCUMULATOR UNIT

The Accumulator unit consists of three registers and an Adder; the A register, the B register, the M register and a separate unit for performing the addition. A set of internal command lines, when pulsed in proper sequence, will perform the arithmetic operations.

4.41   THE A REGISTER

The A register of the computer, of which a single order is shown in Figure 16, is the acting accumulator and is capable of storing and performing the operations of SHIFT RIGHT, SHIFT LEFT, and COMPLEMENT. It has command lines for reading into and out of the various other units of the computer as shown in the Block Diagram of Figure 8.

Separate flip-flops are used for storing the contents during the shifting and complement operations. Two inputs are provided, one
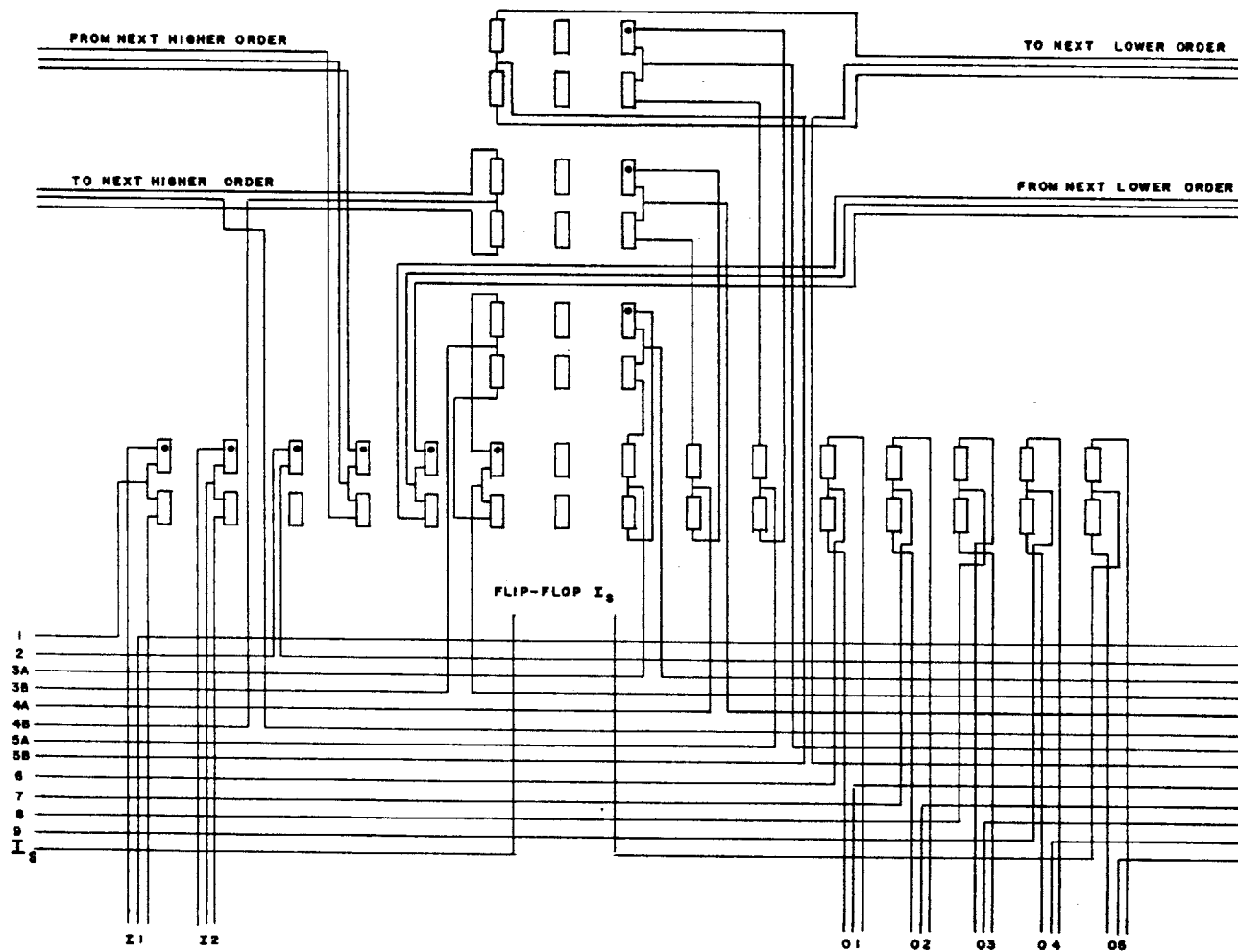
FIGURE 16   SINGLE ORDER CRYOTRON "A" REGISTER

from the Adder, labeled I_1, and the other, labeled I_2 is the input directly from the panel switches. The output lines of the A register are labeled O_1 through O_5 and go to the Bus, the Adder, the B register in complement form, the B register, and the proper amplifier for display on the panel.

The command lines are labeled 1 through 9 and their functions are given in Table IV.

TABLE IV

1   Read Adder into A register
2   Zero set A register
3a, b   Complement A register. A and B are respectively the NO INPUT and YES INPUT outputs of a complementation circuit to which the complement pulse is applied.
4a, b   Shift ONE unit to the left. A and B again as in 3 above except that shift left pulse is applied.
5a, b   Identical to 4 except for shift right.
6   Read A register into Bus
7   Read A register into Adder
8   Read complement of A register into B register
9   Read A register into B register

4.42   THE M REGISTER

The M register is basically the same as the A register except that the sign order is not part of the register itself. The lowest order of the M register has a set of read-out gates which are used to determine whether or not an ADD is to be performed during the multiply operation. The shift and complement lines of the A register continue into the M register, and also perform these operations simultaneously in the M register. The M register has an input line as well as a complement input line from the Bus. In reading the Bus into the M

register that line is chosen which will represent the multiplier in positive form. The original sign is stored in the sign storage register along with the original sign of the multiplicand (A register) to determine whether or not the A register must be complemented at the end of the operation to leave the double length product in correct positive or negative form in the A register.

4.43   THE B REGISTER

The B register holds either the Addend during addition, the Subtrahend during subtraction, or the multiplicand during multiplication. It has inputs and complement inputs from the Bus and the A register, and an output to the Adder. The inputs from the A register are controlled by the A register command lines and the inputs from the Bus are controlled by the Bus command lines.

4.44   THE ADDER

The circuit for the Adder is shown in Figure 17. It is the unit that actually performs the arithmetic operations of addition in the computer.

The inputs are connected as shown in Figure 17a, while the only output gates necessary are placed in the sum flip-flop of the diagram.

The automatic ene-around-carry is achieved by the end-around carry network of Figure 17b, which also has an output for the overflow register.

4.5   THE BUS REGISTER

The function of the Bus register is mainly to distribute the information from and to the memory. It consists of 11 flip-flops each with 3 inputs and 7 outputs which go to the units as shown in the Block Diagram of Figure 8.
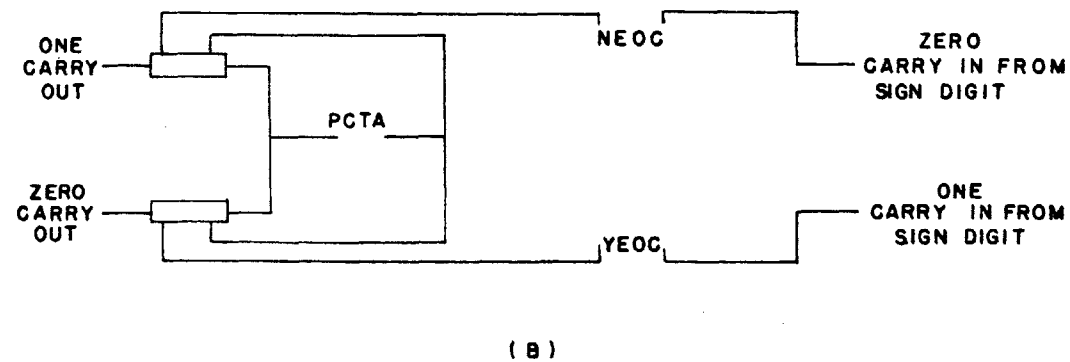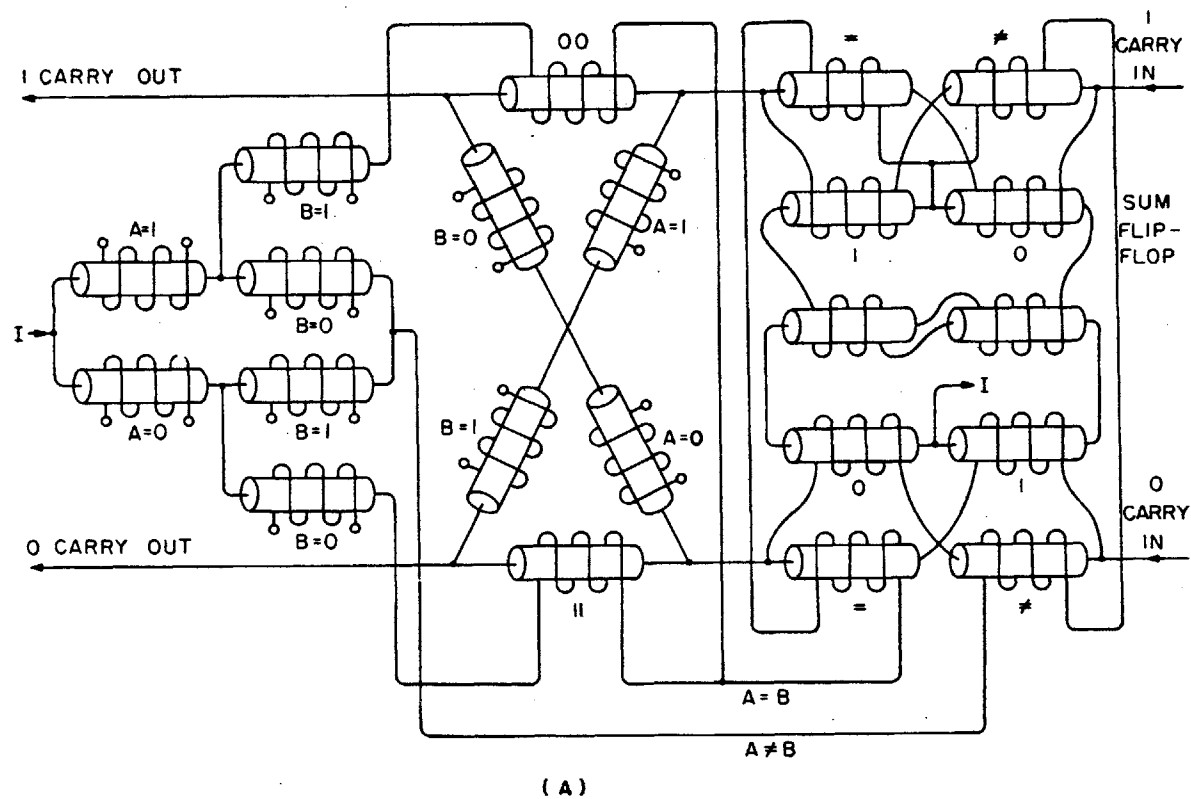
FIGURE 17 (A) ADDER (B) END-AROUND CARRY NETWORK

4.6   THE INSTRUCTION COUNTER

The instruction counter consists of the program counter of the type of section 4.3, and of a pulse distribution counter and matrix for performing the instruction cycle.

The command line pulses ADVANCE INSTRUCTION COUNTER from the execution cycles go to the complementation input of the program counter. The counter is equipped with inputs from the address part of the control for transfer instructions and output gates to read the program counter into the address part of the control during the instruction cycle.

A second counter and a pulse-distribution matrix are used to obtain the command line pulses for the instruction cycle.

4.7   THE CONTROL

The control is a storage register for the instruction and the address during the execution cycle and for the location of the next instruction during the instruction cycle. It consists of 11 flip-flops with read-in from the Bus register, the program counter of section 4.6, and the switches located on the panel. One set of 11 output gates is used for driving the panel indicators. Six read-out gates on the address part of the control go to the inputs on the memory selection matrix. Four read-out gates on the instruction part go to the instruction selection matrix. The sign bit is not used for control purposes.

4.8   THE INSTRUCTION SELECTION MATRIX

The instruction selection matrix as shown in Figure 18, is a 16-position switch, with four inputs from the instruction part of the control. The 16 outputs go to the inputs of the complementation circuits on the various command-line-selection matrices of the various INSTRUCTIONS.
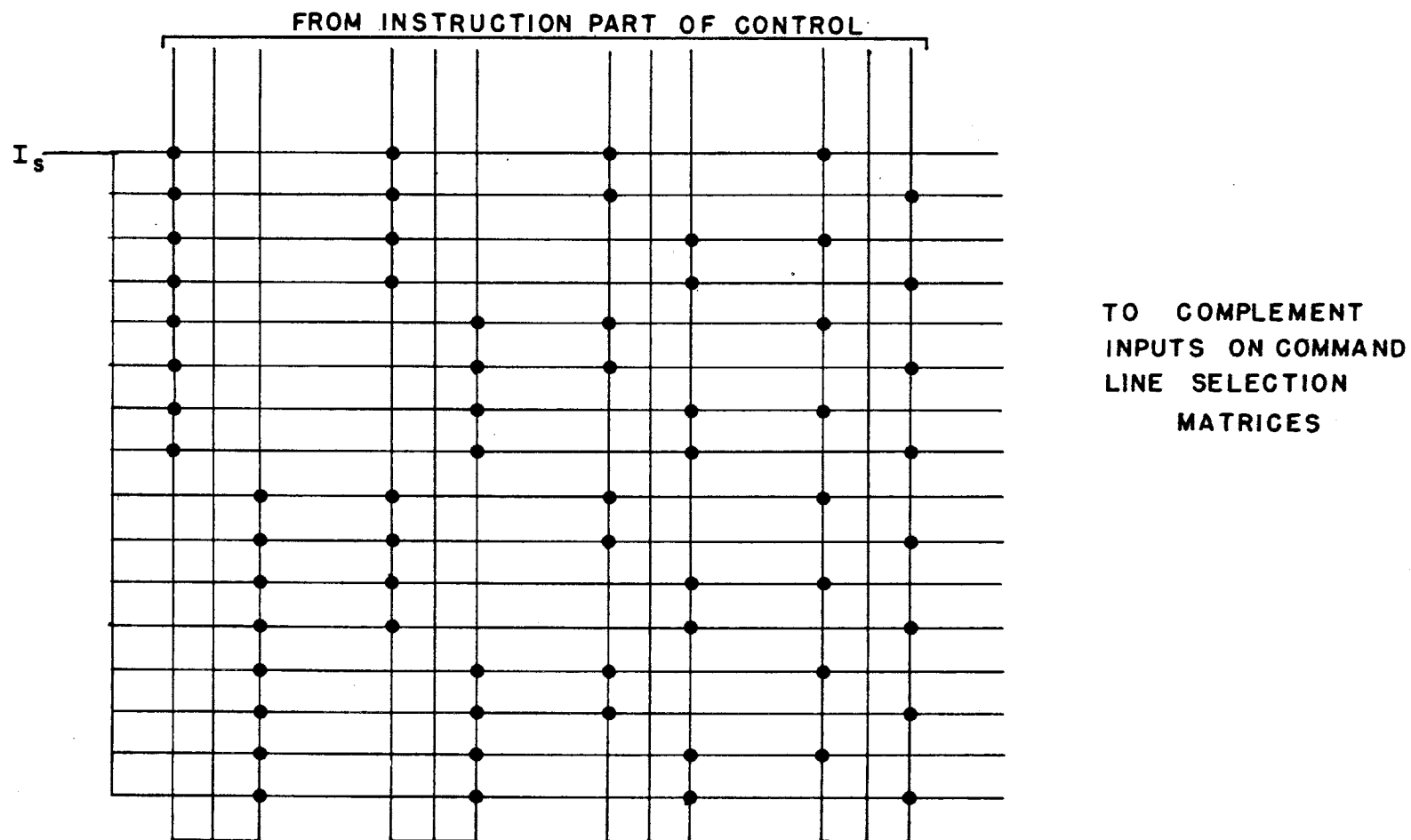
FROM INSTRUCTION PART OF CONTROL

I_s

TO COMPLEMENT
INPUTS ON COMMAND
LINE SELECTION
MATRICES

FIGURE 18   INSTRUCTION   SELECTION   MATRIX

4.9   THE CLOCK

The clock for the computer as shown in Figure 19, consists of a number of flip-flops connected as in the delay circuit of Figure 5, with feedback from the output of the last flip-flop to the input of the first.   In particular the ONE output goes to the ZERO input while the ZERO output goes to the ONE input.   Output pulses are obtained through the use of a pair of cryotrons whose controls are in the feedback loop.   This permits the use of a separate current source I_{sc}, which is used to control the pulse repetition frequency.   Of the pair, one cryotron provides a means of monitoring the frequency, while the other provides the computer with pulses.

4.10   THE CLOCK GATES

The clock gates are shown in Figure 20.   Clock pulses enter on the line marked CLOCK PULSES from the clock itself, and go to the output gates of FF_1, the START, STOP (ST, SP) flip-flop.   The pulses are steered either to the steering gates of FF_2 or to the pulse return line via the stop indicator (SI) line.   The output gates of FF_2, the HALT flip-flop, steer the pulses either to FF_3, the Instruction-Execution-cycle flip-flop, or to the pulse-return line via the HALT INDICATOR (HI) line and the ONE output gate on FF_4. FF_3 steers the pulses either to an instruction cycle (ICP) or an execution cycle (ECP).   If a HALT command occurs, the halt pulse sets FF_2 to the ONE state, diverting the clock pulses to FF_4. OSEC and OSIC are activated from external push button switches and perform Operate Single Execution Cycle and Operate Single Instruction Cycle respectively.   The line labeled CONTINUE (C) is activated by an external push button switch for continuing the program after a halt instruction.
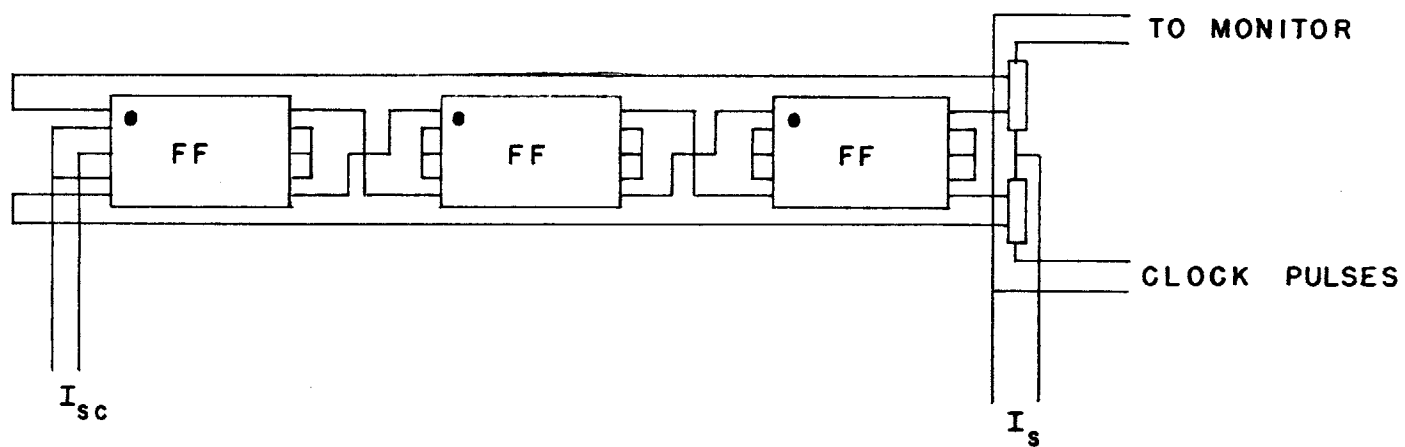
FIGURE 19   CRYOTRON   CLOCK
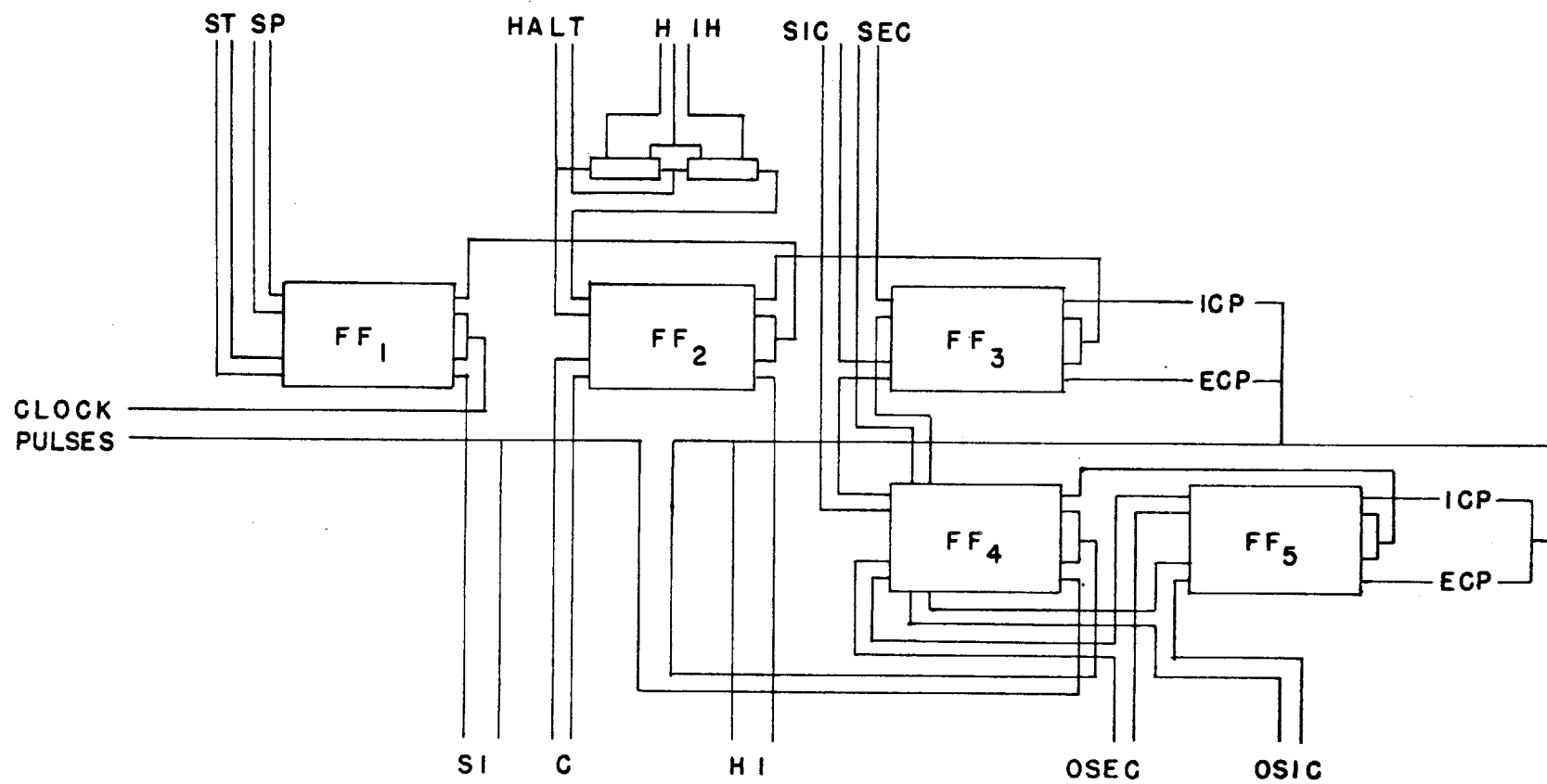
ST SP   HALT   H IH   SIC SEC

FF₁

FF₂

FF₃   ICP
                   ECP

CLOCK
PULSES

FF₄   FF₅   ICP
                            ECP

SI   C   H I   OSEC   OSIC

FIGURE 20   CLOCK   GATES

4.11 THE OVERFLOW REGISTER

The overflow register is the name given the circuit which will give an indication of and store an overflow should it occur. An overflow is detected by checking the sign of the accumulator against the occurance or non-occurance of an end-around-carry in the Adder. The circuit is shown in Figure 21. The sign of the A register and the end-around-carry of the Adder, both of which are d-c levels are fed to the controls of the logic cryotrons. (YEOC stand for YES END AROUND CARRY; NEOC stands for NO END AROUND CARRY) I_s enters at the junction of the sign gates, and accordingly goes to another set of gates to determine the condition of the end-around-carry, from which it then sets the flip-flop to ONE if an OVERFLOW has occured, and ZERO if there was no overflow. There are two input command lines to the register, TRANSFER ON OVERFLOW and TEST FOR OVERFLOW which are labeled 13 and 14 respectively in the diagram. A pulse to the TRANSFER ON OVERFLOW command line goes to a set of output gates on the flip-flop and will either advance the instruction counter or read the ADDRESS in the control into the instruction counter according to whether or not an overflow is stored in the flip-flop. A pulse to the TEST FOR OVERFLOW command line goes to a set of output gates on the flip-flop and will either return to the pulse source or cut the main clock (stop) off.

One set of output gates is used for a visual indication of OVERFLOW on the panel of the computer. This line goes to the overflow indicator amplifier. A third command line labeled 22 in the diagram is used to set the overflow register to ZERO; that is, to set it to the NO OVERFLOW state.

4.12 PRODUCT SIGN DIGIT REGISTER

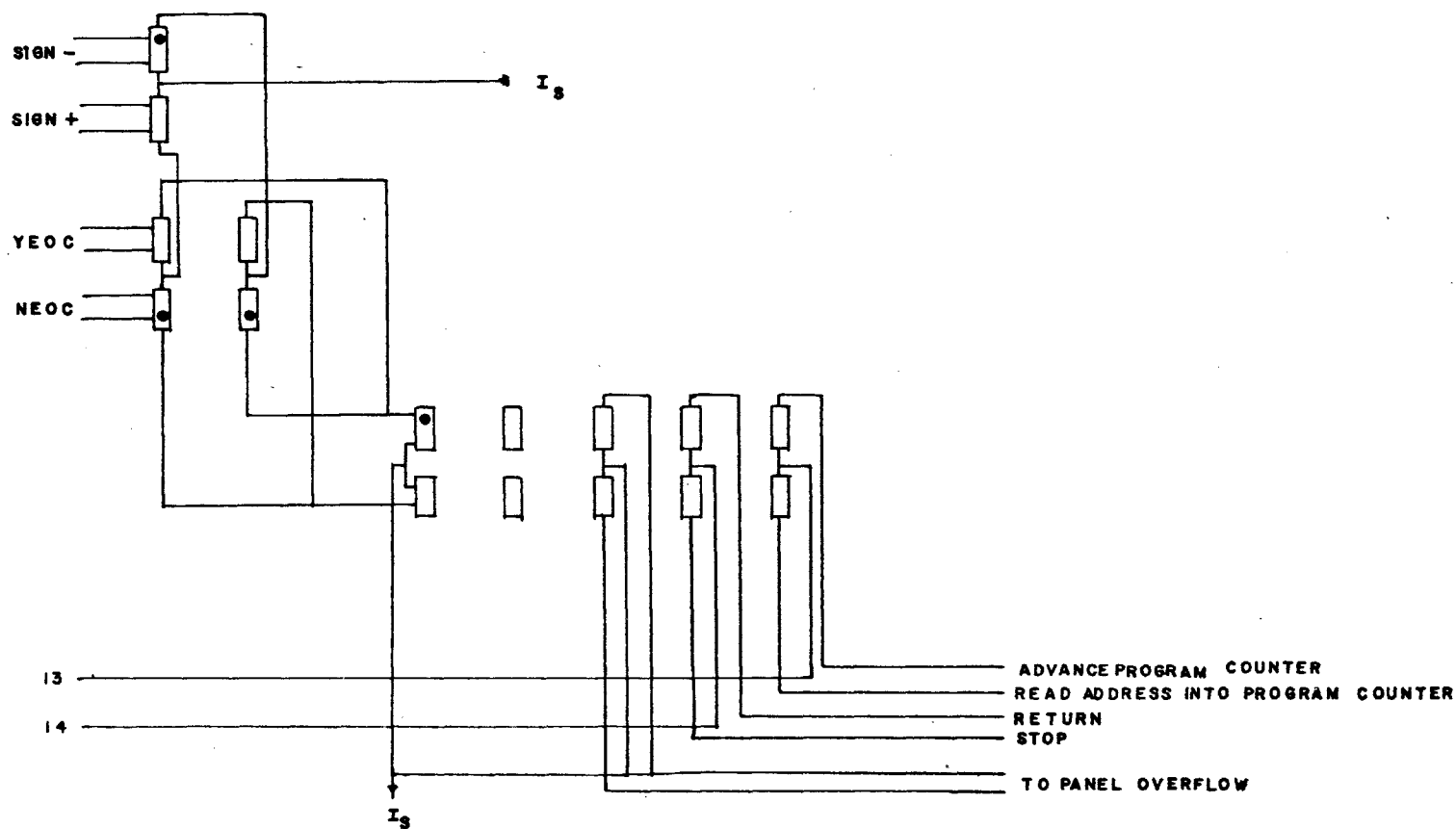The product sign digit register is shown in Figure 22. It

FIGURE 21   OVERFLOW   STORAGE AND CHECKING REGISTER
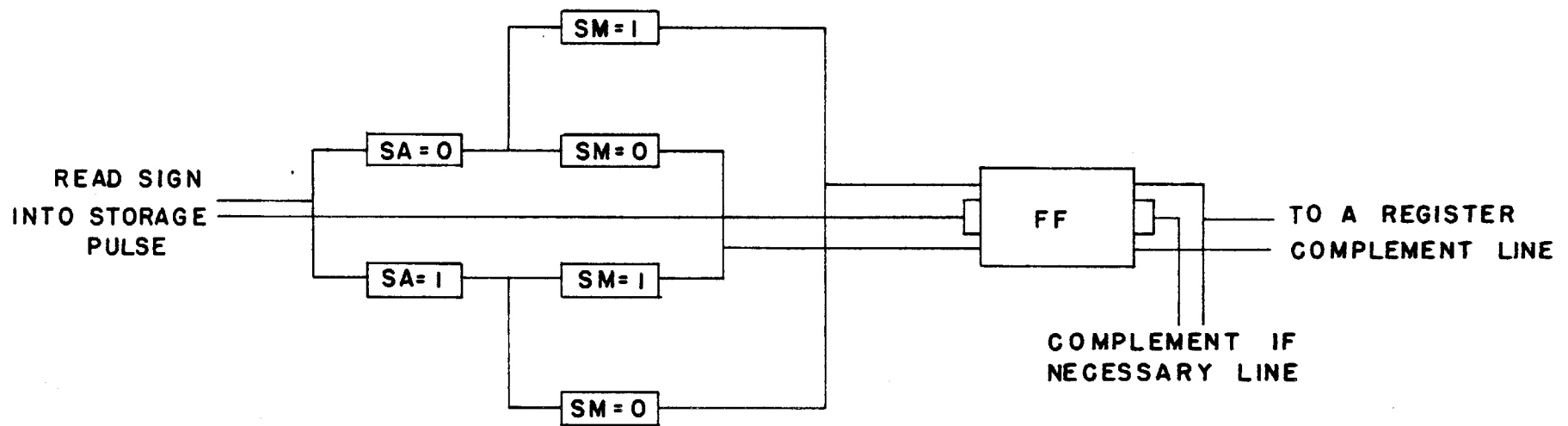
FIGURE 22   PRODUCT SIGN DIGIT REGISTER

consists of a network of gates whose controls are driven by the outputs of the A register sign digit order, and the M register sign digit order. At the occurance of a READ SIGN INTO STORAGE pulse the product sign digit is stored in the flip-flop. At the completion of the multiplication operation a pulse to the output gates of the flip-flop will complement the A register if the product is negative.

4.13 COMMAND LINE SELECTION MATRICES

4.13-1 ADDITION

When a d-c level from the instruction selection matrix is placed on the ADD line as shown in Figure 23, the complementation circuit permits the clock pulses to enter the counter. The counter is initially set to ZERO and while in this state the zero output prevents pulses from other selection matrices from having more than one path. The first count unlocks these lines and source current is applied to CML 14, which tests for overflow. The next count pulses CML 12, which reads the memory into the Bus. The third pulse reads the Bus into the B register. The fourth pulse performs three functions: it reads the A register into the ADDER, the B register into the ADDER, and pulses the Carry Line to perform addition. These are CML 7, CML 17, and CML 18 respectively. The next pulse performs the two operations of reading the adder into the A register, and advancing the instruction counter, which are labeled CML 1 and CML 10 respectively. The last pulse is CML 15 and switches the clock to the instruction cycle. The counter is reset to ZERO during part of the INSTRUCTION CYCLE.

4.13-2 SUBTRACTION

The command line selection matrix for subtraction is identical to that of the addition matrix of section 4.13-1 with the exception of
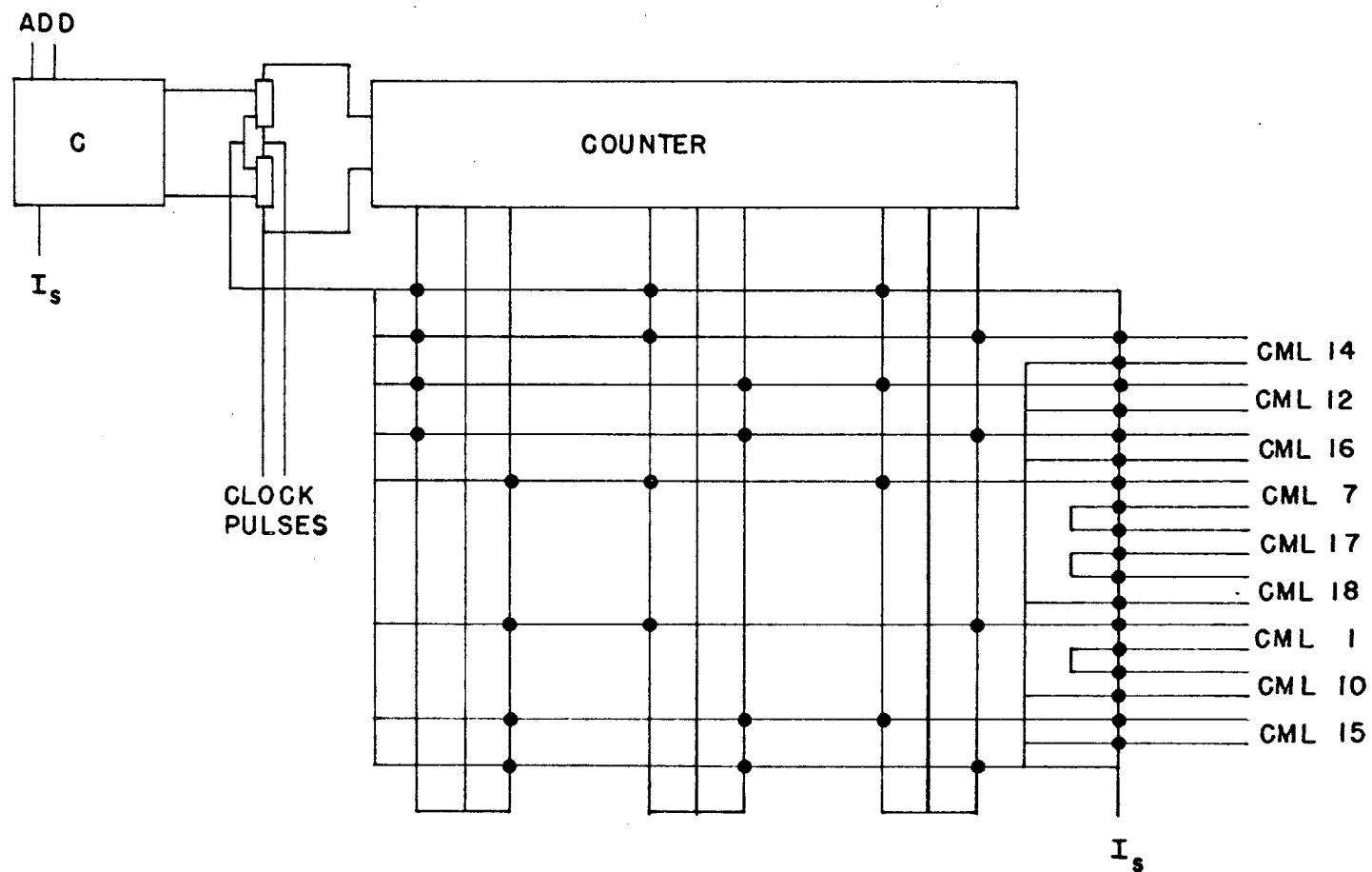
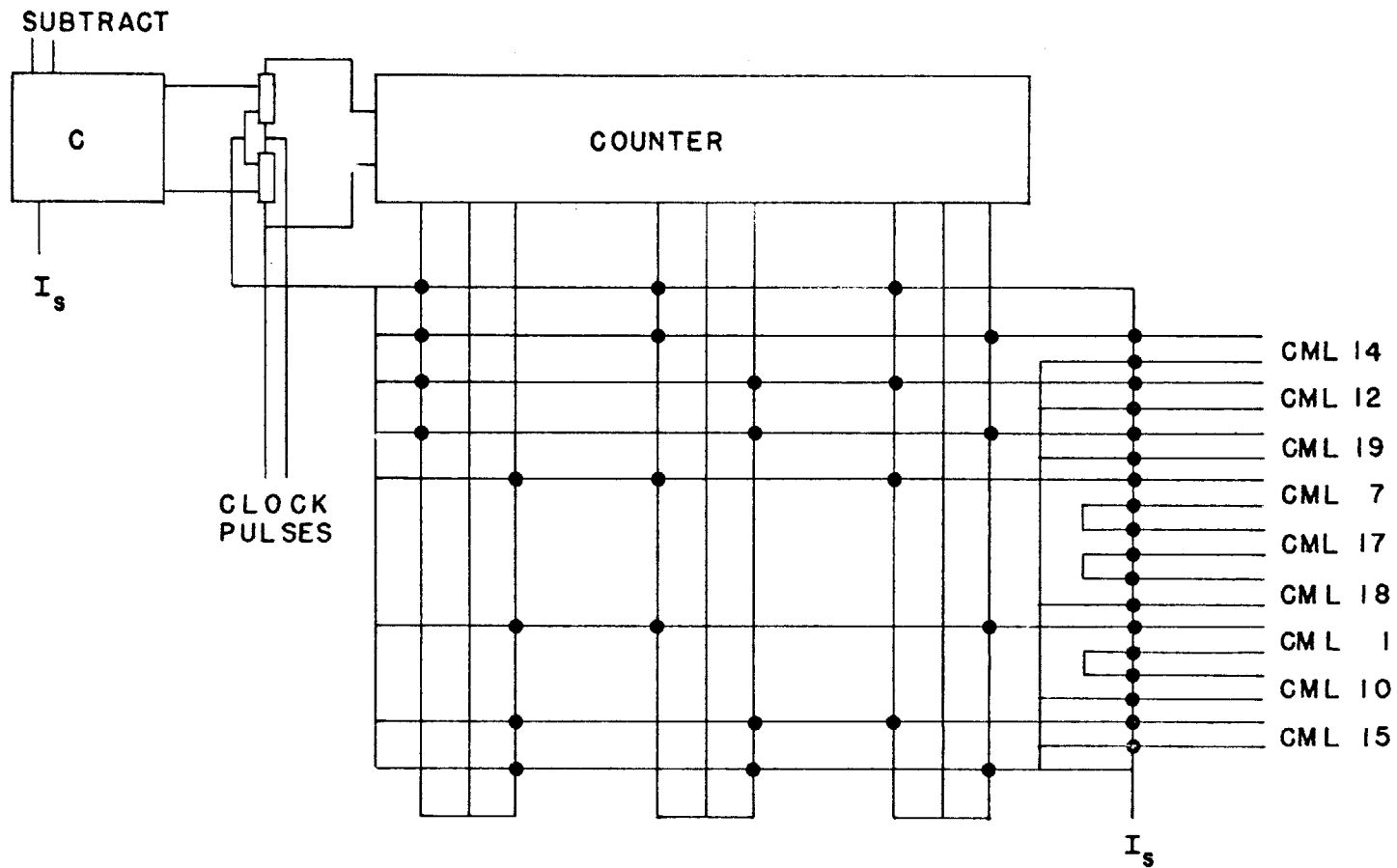FIGURE 23   COMMAND LINE SELECTION MATRIX FOR ADDITION

FIGURE 24 COMMAND LINE SELECTION MATRIX FOR SUBTRACTION

the third pulse which reads the complement of the Bus into the
B register. The matrix is shown in Figure 24.

4.13-3   MULTIPLICATION

At the application of a d-c level to the Multiply line as shown
in Figure 25, the clock pulses enter the counter. The first pulse
tests for overflow, the second reads the memory into the Bus and
the third performs the operations of reading the A register into
the B register complementing if the sign is negative, reading the
Bus into the M register again complementing if the sign is negative,
and storing the sign of the product in the sign storage register.
The next pulse of the counter sets to ZERO the A register and the
Adder. The last pulse switches the clock pulses to the ADD-SHIFT
counter which performs the proper number of add-shift operations
to perform the multiply, performing an actual addition only when
the right-hand order of the M register is ONE. When these op-
erations are complete the product in the A register is complemented
if the stored sign of the product is negative. The last pulse from
the ADD-SHIFT counter switches the clock to the instruction cycle.

4.13-4   CLEAR AND ADD

The command line selection matrix for clear and add is
identical to that of the addition matrix of section 4.13-1 with the
exception that command line 2, which sets the A register to
ZERO, is also activated by the third output of the counter. The
matrix is shown in Figure 26.

4.13-5   STORE

The command line selection matrix for the store instruction
is shown in Figure 27, and is again basically that of the addition
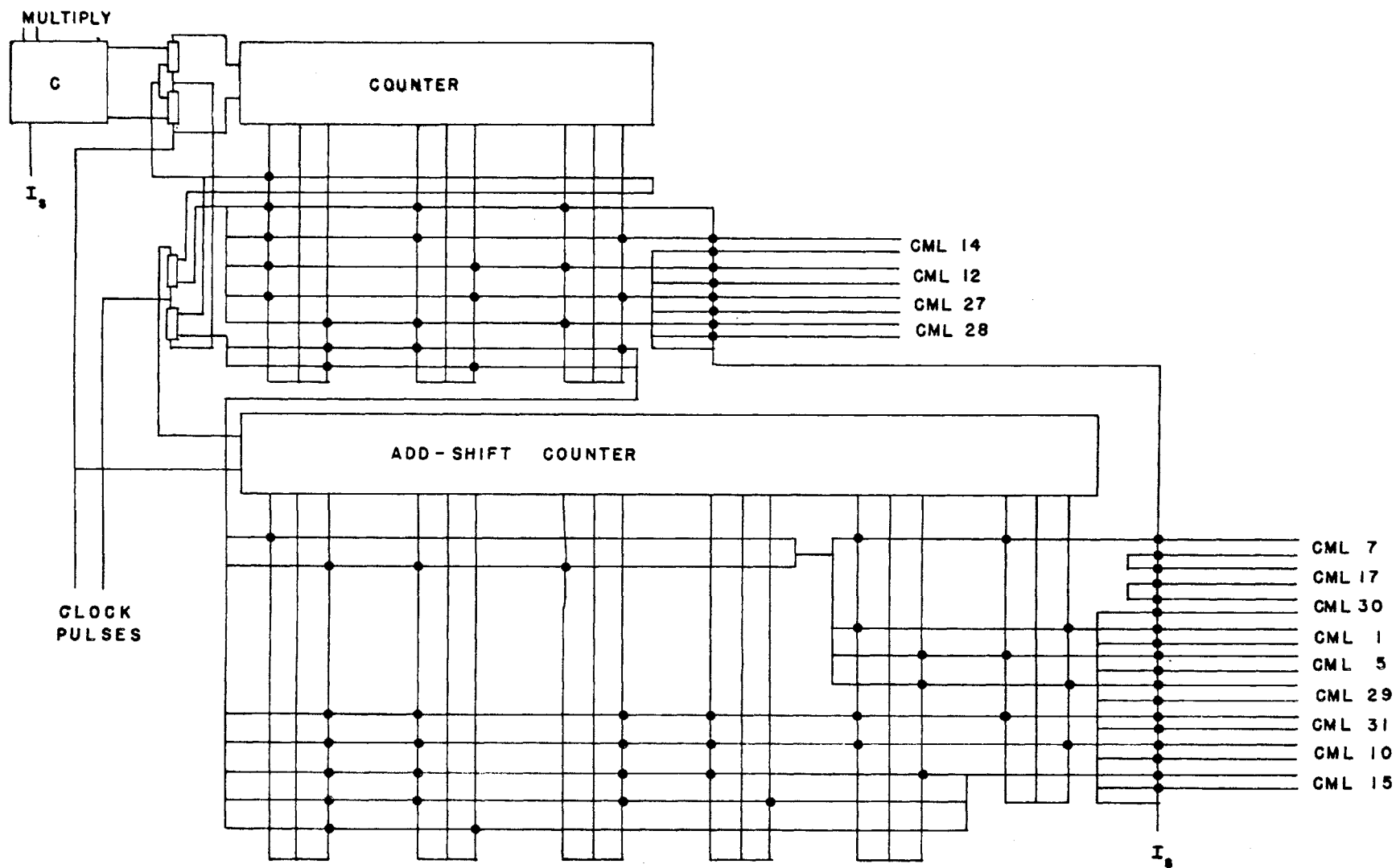
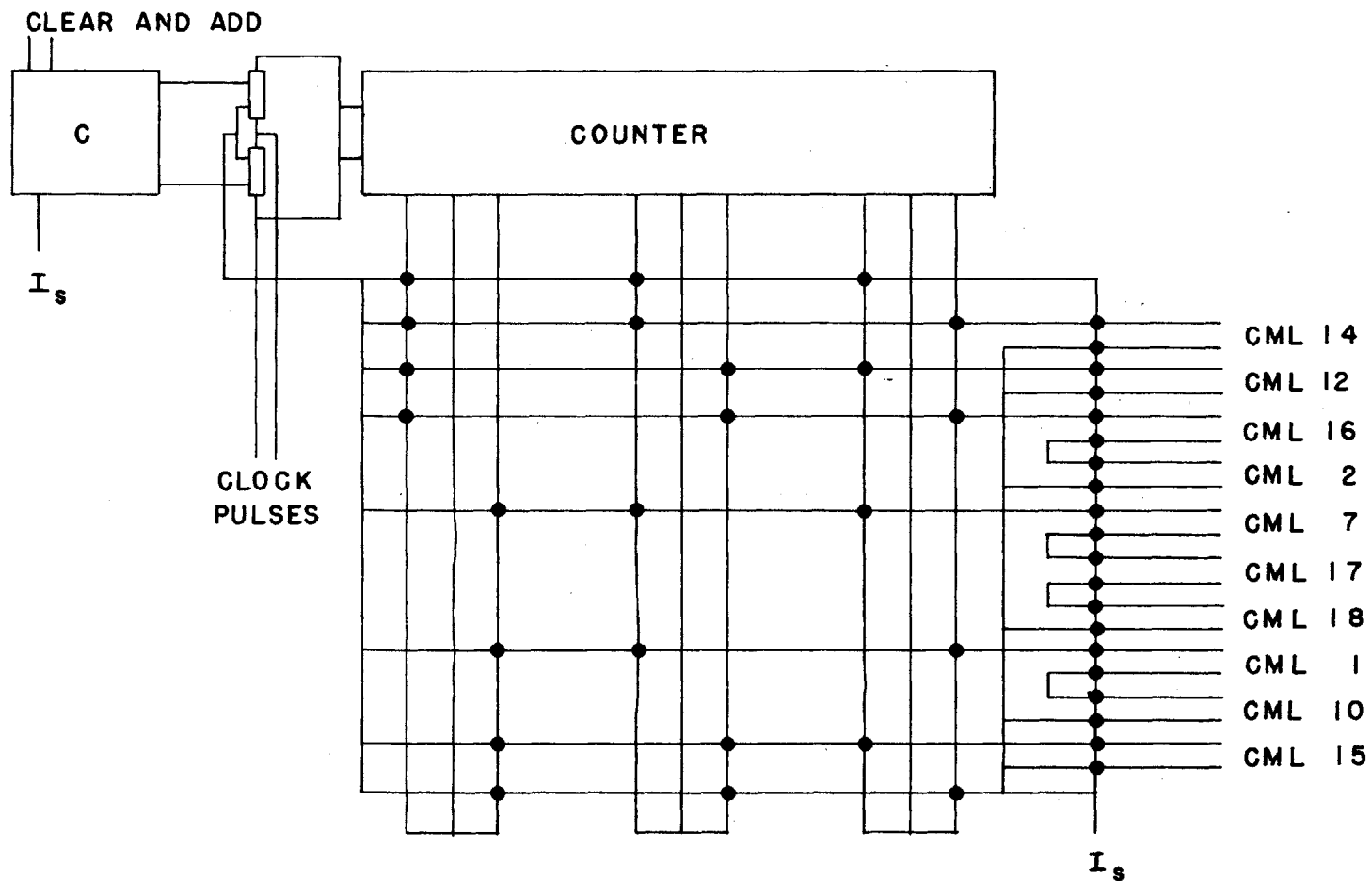FIGURE 25   COMMAND   LINE   SELECTION   MATRIX   FOR   MULTIPLY

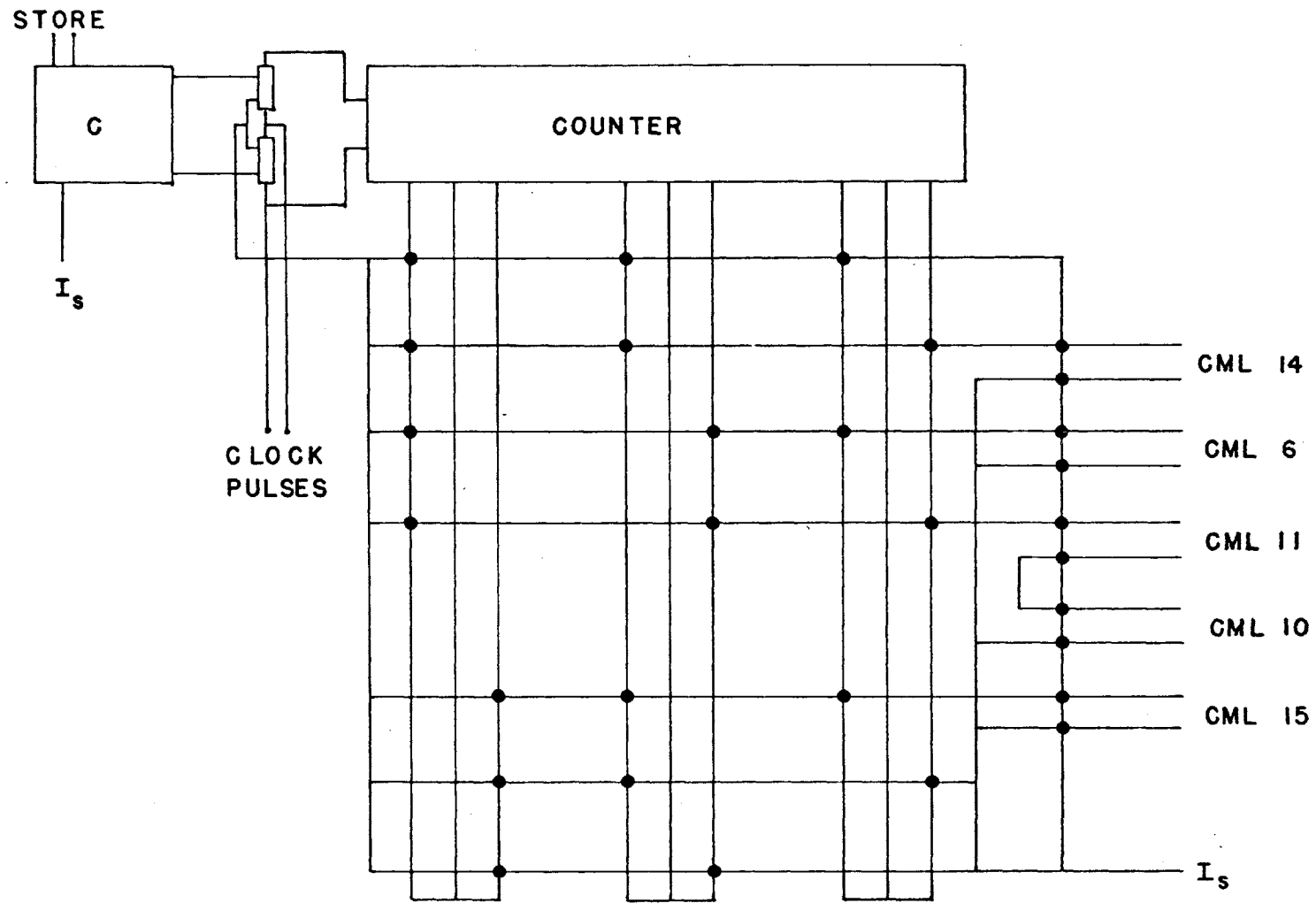FIGURE 26 COMMAND LINE SELECTION MATRIX FOR CLEAR AND ADD

FIGURE 27   COMMAND LINE   SELECTION MATRIX   FOR   STORAGE

matrix of section 4. 13-1, but with the output command lines CML 14, test for overflow; CML 6, read A register into Bus; CML 11 and 10, Read Bus into Memory and Advance Instruction Counter; and CML 15 to switch to the instruction cycle.

4. 13-6   TRANSFER

When a d-c level from the instruction selection matrix is placed on the TRANSFER line as shown in Figure 28, three command lines perform the functions of testing for overflow, reading the address part of the control into the instruction counter and switching back to the instruction cycle.

4. 13-7   TRANSFER IF NEGATIVE

The command line selection matrix for TRANSFER IF NEGATIVE is identical to that of the TRANSFER matrix in section 4. 13-6 except CML 21 is substituted for CML 20, thus reading the address part of the control into the instruction counter only if the sign of the A register is negative. This matrix is shown in Figure 29.

4. 13-8   TRANSFER ON OVERFLOW

The transfer-on-overflow matrix has only three outputs, one to the overflow register of section 4. 11, the second sets the overflow register to ZERO, and the third switches the computer back to the instruction cycle. The matrix is shown in Figure 30.

4. 13-9   SHIFT RIGHT

The command - line - selection matrix for SHIFT RIGHT is of necessity more complex due to the fact that the output is a function of the ADDRESS in the control which specifies the number

TRANSFER

C

I_s

COUNTER

CLOCK
PULSES

CML 14

CML 20

CML 15

I_s
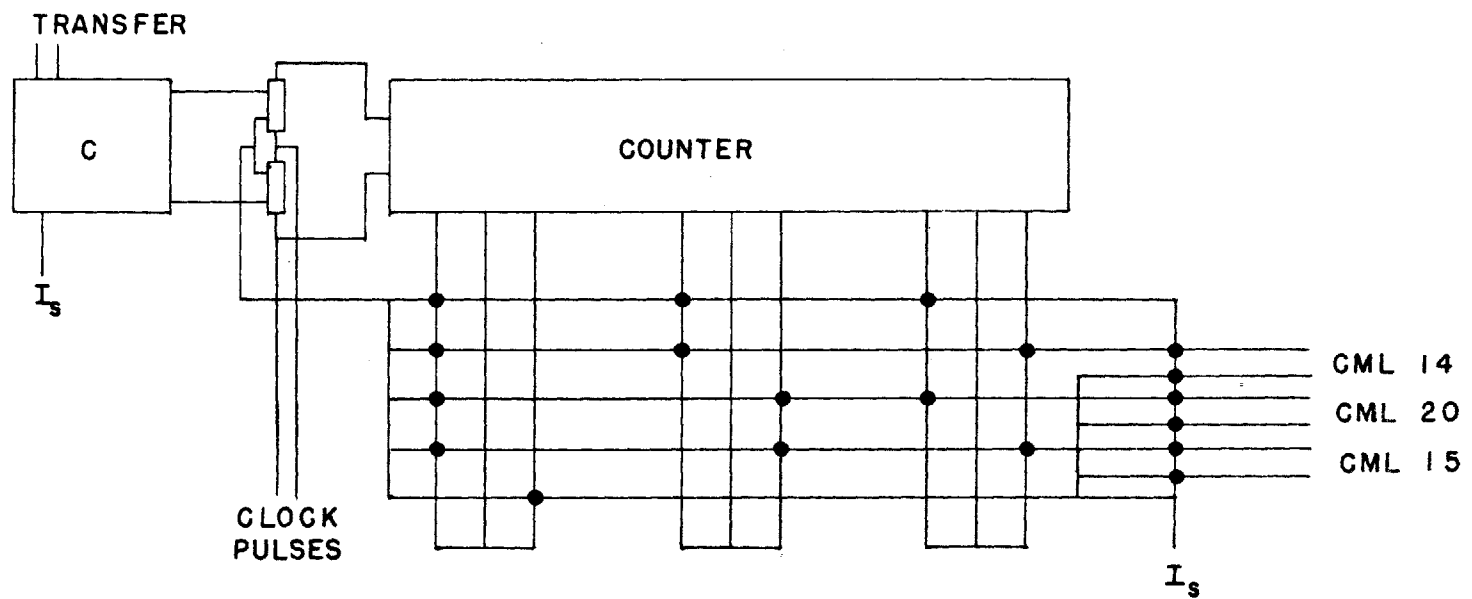
FIGURE 28   COMMAND LINE SELECTION MATRIX FOR   TRANSFER

TRANSFER IF NEGATIVE
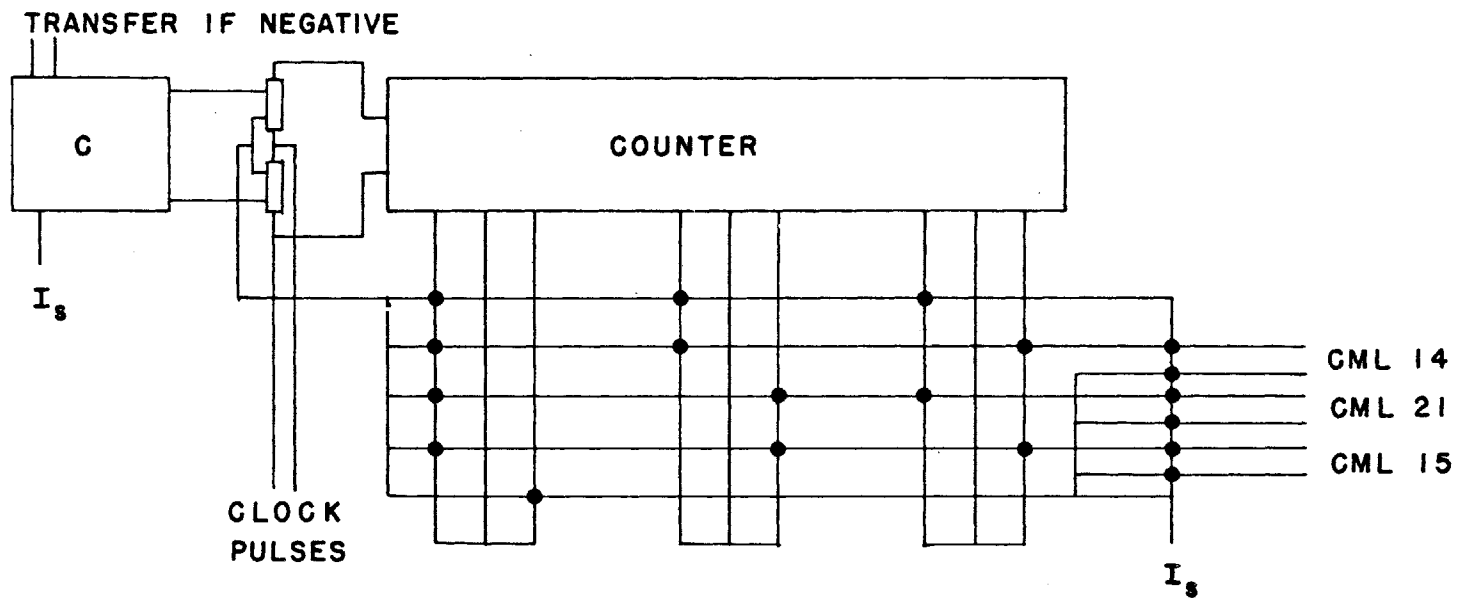
FIGURE 29   COMMAND LINE   SELECTION .MATRIX FOR   TRANSFER   IF   NEGATIVE

TRANSFER ON OVERFLOW

C

I_s

CLOCK
PULSES

COUNTER

CML 13
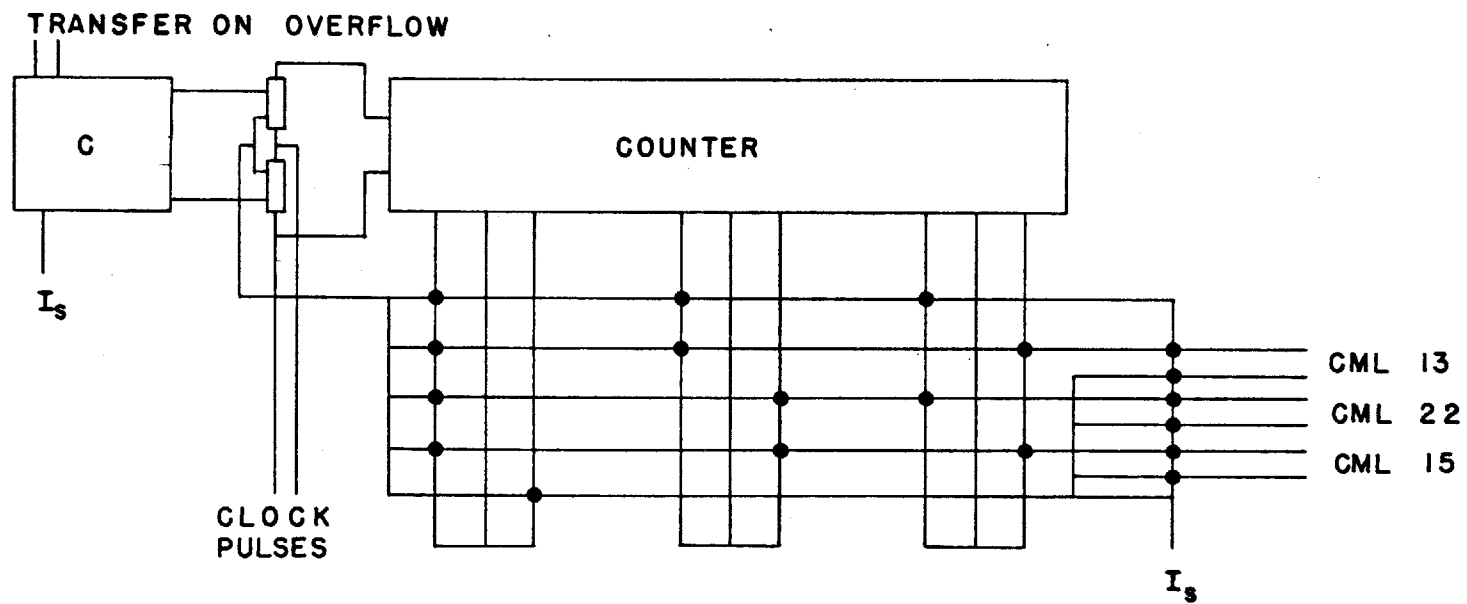
CML 22

CML 15

I_s

FIGURE 30   COMMAND LINE SELECTION MATRIX FOR   TRANSFER ON   OVERFLOW

of shifts to be performed. The matrix is shown in Figure 31. At the application of the d-c level to the SHIFT RIGHT line, the clock pulses enter the counter and in sequence perform the operations of TEST FOR OVERFLOW, READ ADDRESS COMPLEMENT INTO SHIFT RIGHT COUNTER, and ADVANCE INSTRUCTION COUNTER. At this point the clock pulses are switched over to the shift-count counter which now contains the complement of the number of times the shifting operation must be performed. The clock pulses are now also on CML 5 which goes to the A register shift right command line. When the proper number of shift-right pulses have occured the shift-count counter is set to ALL ONES and a pulse is applied to CML 15 to switch back to the instruction cycle.

4.13-10 SHIFT LEFT

The command line selection matrix for SHIFT LEFT is identical to the command line selection matrix for SHIFT RIGHT with the exception that CML 5 is replaced by CML 4, the command line that goes to the A register shift-left line.

4.13-11 PRINT

At the application of a d-c level to the PRINT line as shown in Figure 32, the matrix performs the operations necessary to prepare the PRINT REGISTER for activating the Flexowriter. These operations are: Read memory into Bus, Read Bus into Print register and zero set print counter, advance instruction counter, pulse to the PRINT flip-flop of Figure 14, and the last pulse to a set of gates (not shown) which prevent further pulses from entering the counter. There is no pulse for switching back to the instruction cycle as this is performed by the Print Routine Circuit of Figure 14.
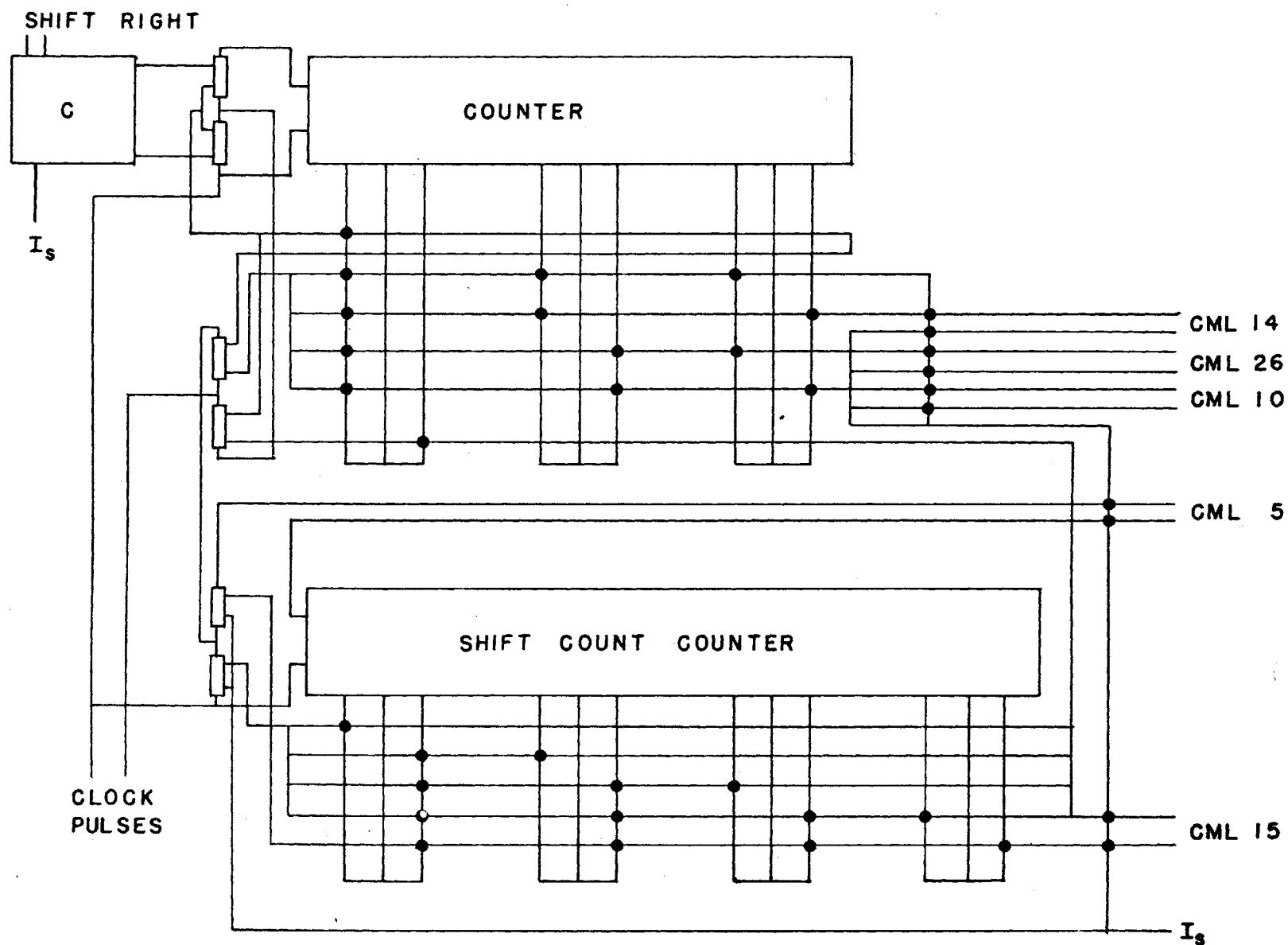
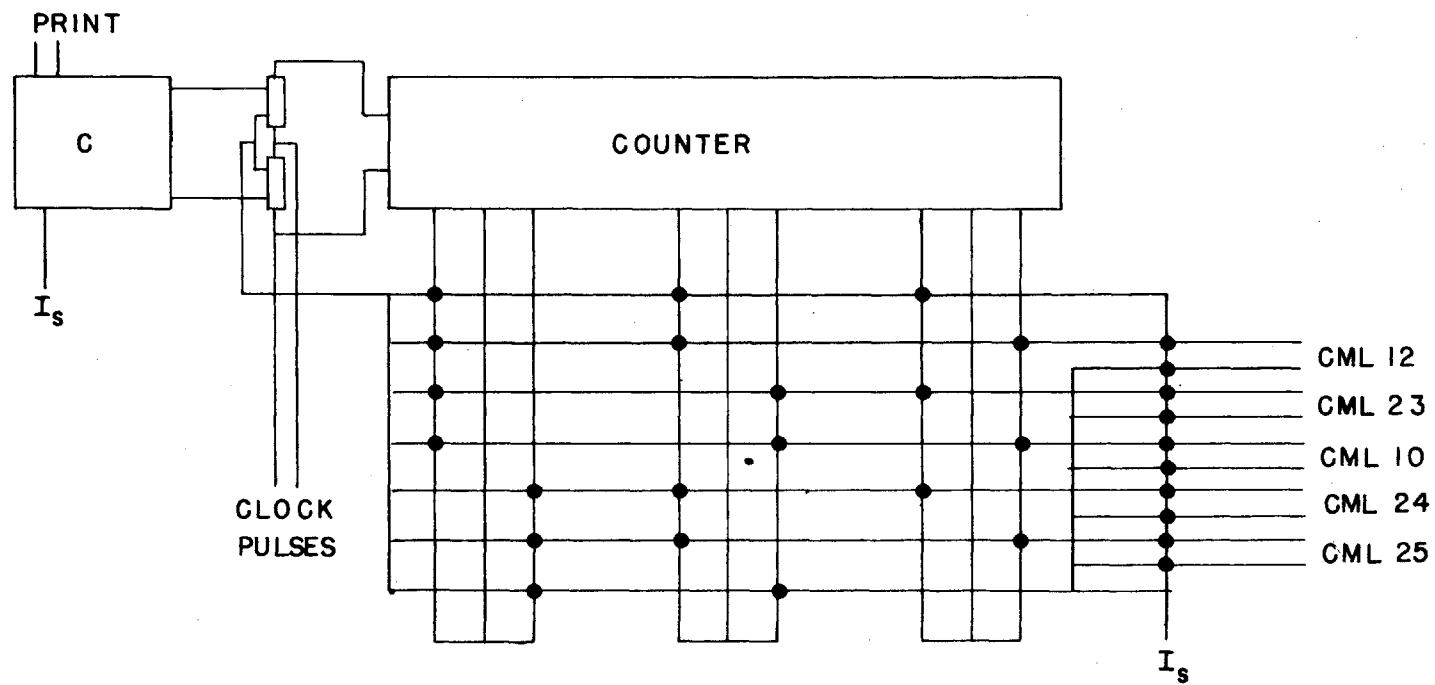FIGURE 31   COMMAND LINE SELECTION MATRIX   FOR   SHIFT RIGHT

FIGURE 32   COMMAND LINE SELECTION MATRIX FOR PRINT

4.14 THE READ-IN UNIT

The read-in unit contains a translation matrix, Figure 33,
to convert the Flexowriter code (6 bits) into 11 separate lines. The
first 8 of these lines are converted into octal code by a second
translation matrix, and represent numbers in octal form. Of the
remaining three lines, onve gives an output when the slash (/) code
is applied at the input, the second gives an output on either the
TAB or CARRIAGE RETURN, while the third is a current continuity
line for those inputs which do not give an output on any of the other
lines.

The octal output of the second translation matrix, Figure 34,
goes to the lowest three orders of an 18 bit shift-left-three-orders
register. The shifting is accomplished through the use of the comple-
mentation circuit. Thus after each letter or number is written on
the Flexowriter and placed in the shift register, a three-place-shift
is performed.

When a slash (/) is written on the Flexowriter the output from
the first translation matrix is used to write the word now in the
shift register into the control. When a TAB or CARRIAGE
RETURN is written a single execution cycle is performed. To
differentiate between instructions and numbers, all instructions are
written with letter symbols in the form:

$$\pm \text{ CLAXX}$$

where XX is octal, and the puls or minus sign the TAG Numbers
are written in the form:

$$\pm \text{ NXXXX}$$

where again XXXX is octal. As shown in Figures 35 and 36, use
is made of the N in the matrix to distinguish numbers and
instructions and convert all instructions into the proper binary
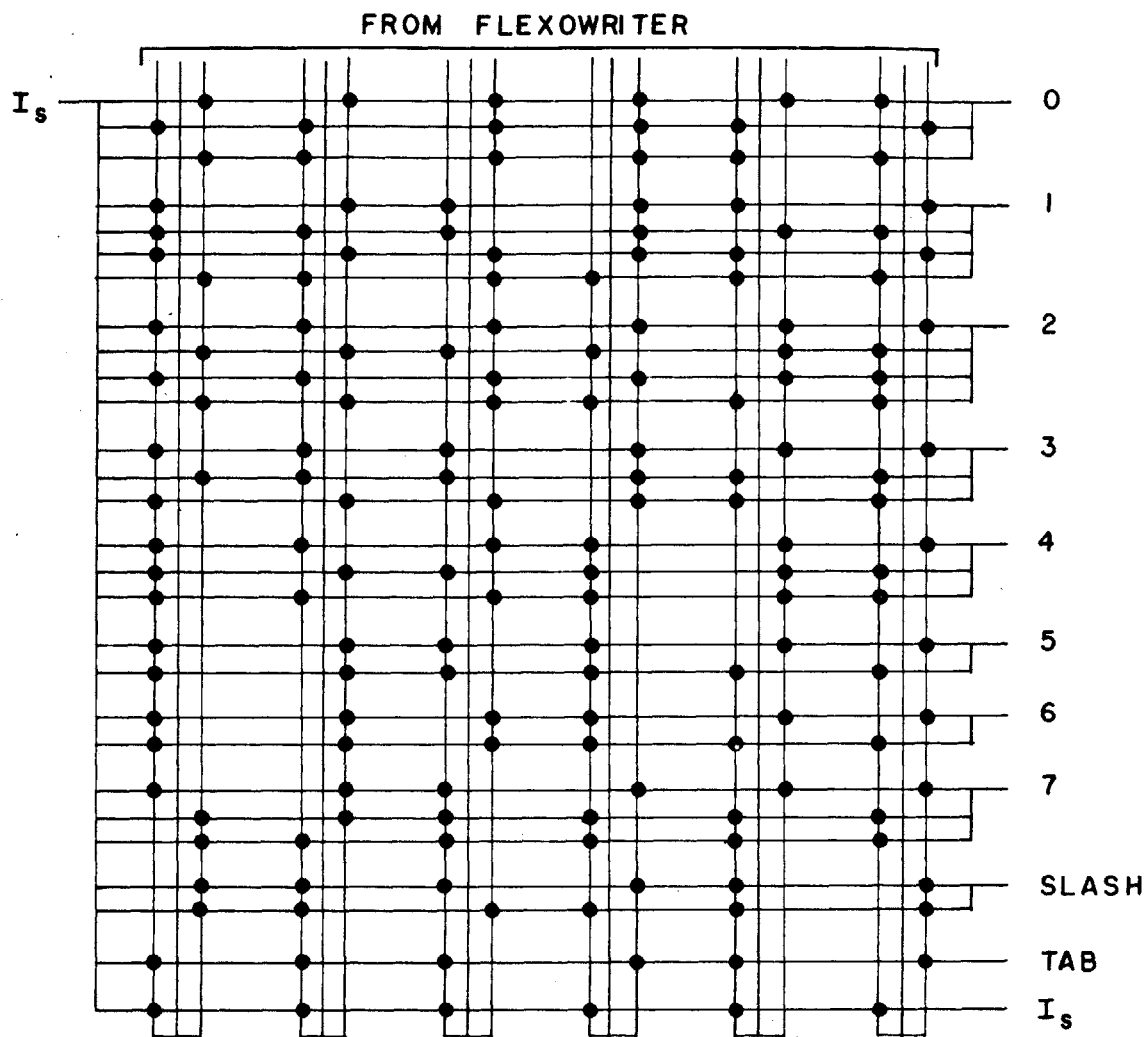
FIGURE 33. FLEXOWRITER TRANSLATION MATRIX 1
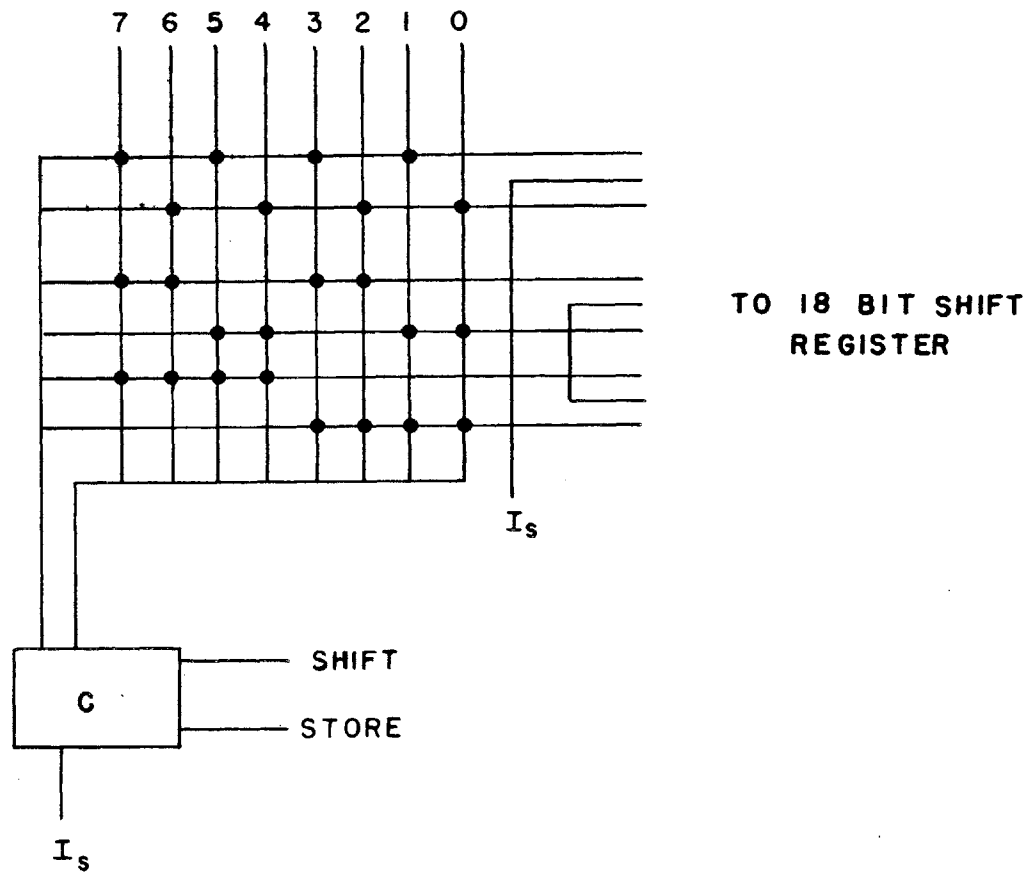
FIGURE 34   FLEXOWRITER   TRANSLATION   MATRIX   2

FROM 2nd 3rd 4th ORDERS OF SHIFT REGISTER

I_s

NUMBER

SYMBOL

NUMBERS

TO CODE MATRIX

FIGURE 35   NUMBER – SYMBOL TRANSLATION MATRIX

I_{symbol} >

I_S <

BINARY CODED
INSTRUCTION

FIGURE 36   CODE MATRIX

code. This distinction between numbers and instructions must be made only in the second, third and fourth orders (each order here is three binary digits, e.i. octal orders), as in all other orders only numbers and the sign occur.

CHAPTER V

TERMINAL EQUIPMENT

5.1   OUTPUT

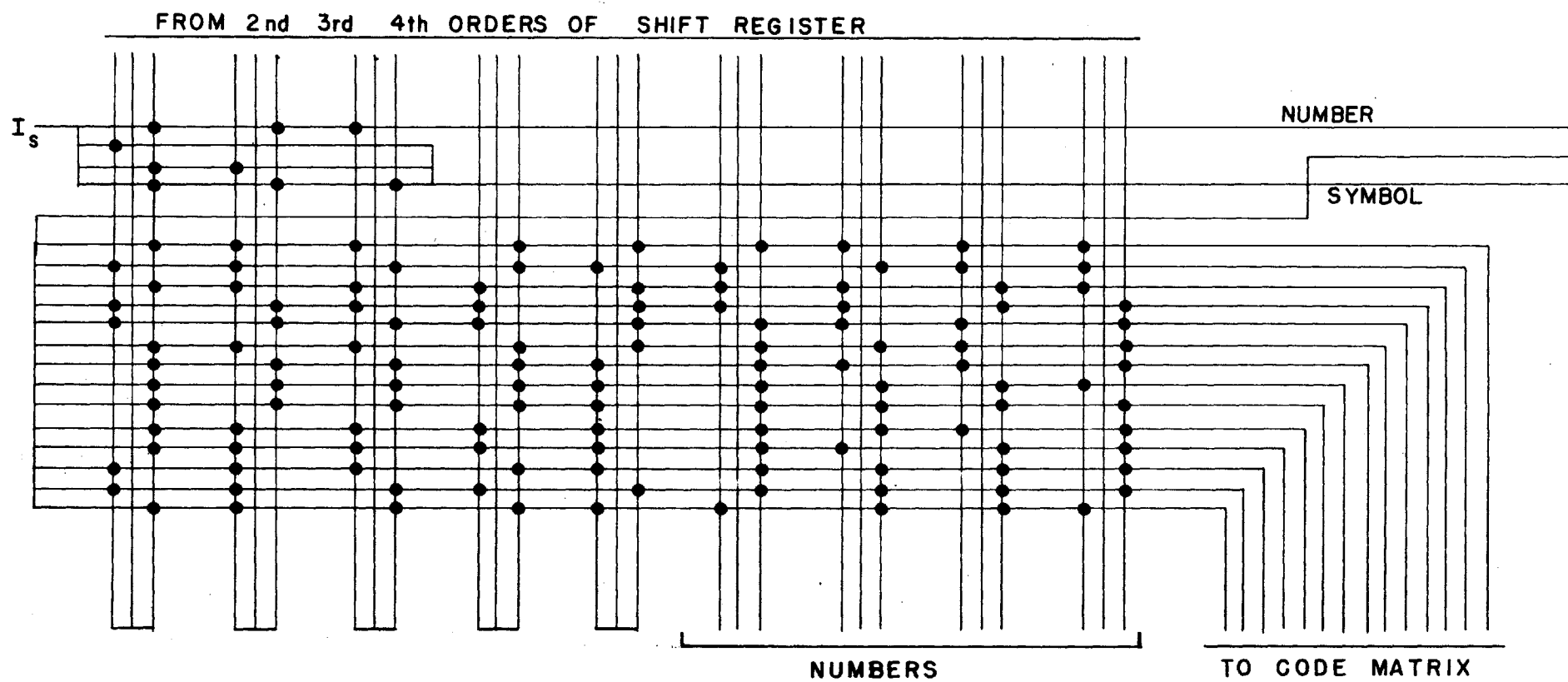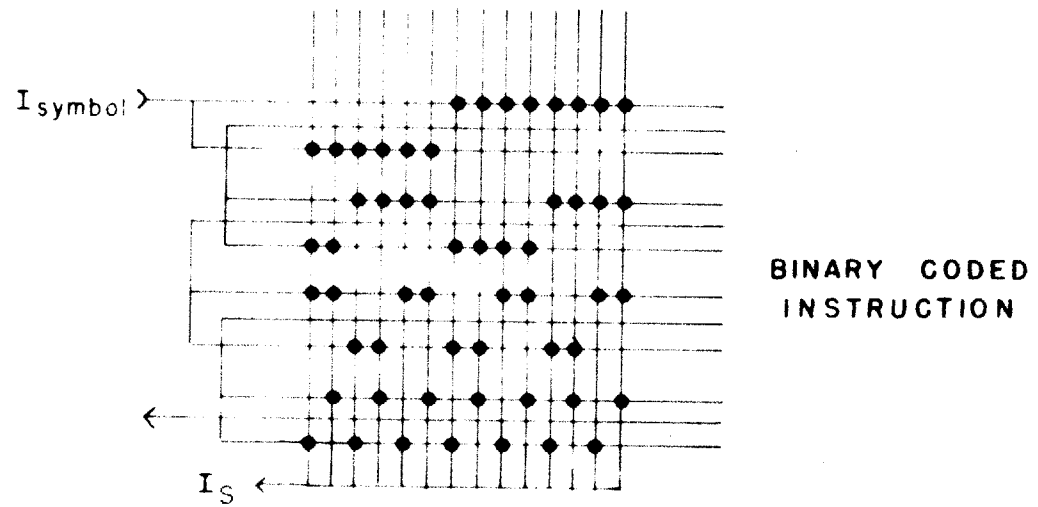The low power and impedance level of cryotrons makes it rather difficult to get information out out of a cryotron system. To detect the state of a cryotron, normal or superconductive, it is usual to use a four - wire measuring technique. A wire-wound cryotron using 0.009 inch Tantalum for the gate and 100 turns of 0.003 inch Niobium for the control winding exhibits a normal gate resistance of approximately 0.001 ohm; with a direct current of 100 milliamperes in the gate the output voltage across the normal gate is 100 microvolts. The resistance of the lead wires coming out of the helium dewar vessel present a series resistance of approximately two to three ohms. Direct matching to the source is therefore not feasable. Detection of such low d-c levels would normally require the use of chopper amplifiers, much space and standby power. To circumvent this problem and yet not deal with pulse circuits for the terminal equipment, it was decided to operate the cryotron read-out gates for the control panel and the Flexowriter from an a-c source. While this does not change the level of the signal to be detected, it simplifiers the d-c drift stabilization and coupling of the required amplifiers. A four-stage transistor amplifier consisting of three stages of amplification and an output switching transistor was designed, and the circuit is shown in Figure 37. The switching stage drives the control panel indicators as well as the relays which operate the Flexowriter printer. A bias threshold control is made available which has a twofold purpose: First, to control the change in input signal necessary for complete switching and second, to provide a master level setting control. The non-linearity of the detector diode forward resistance forms the threshold.
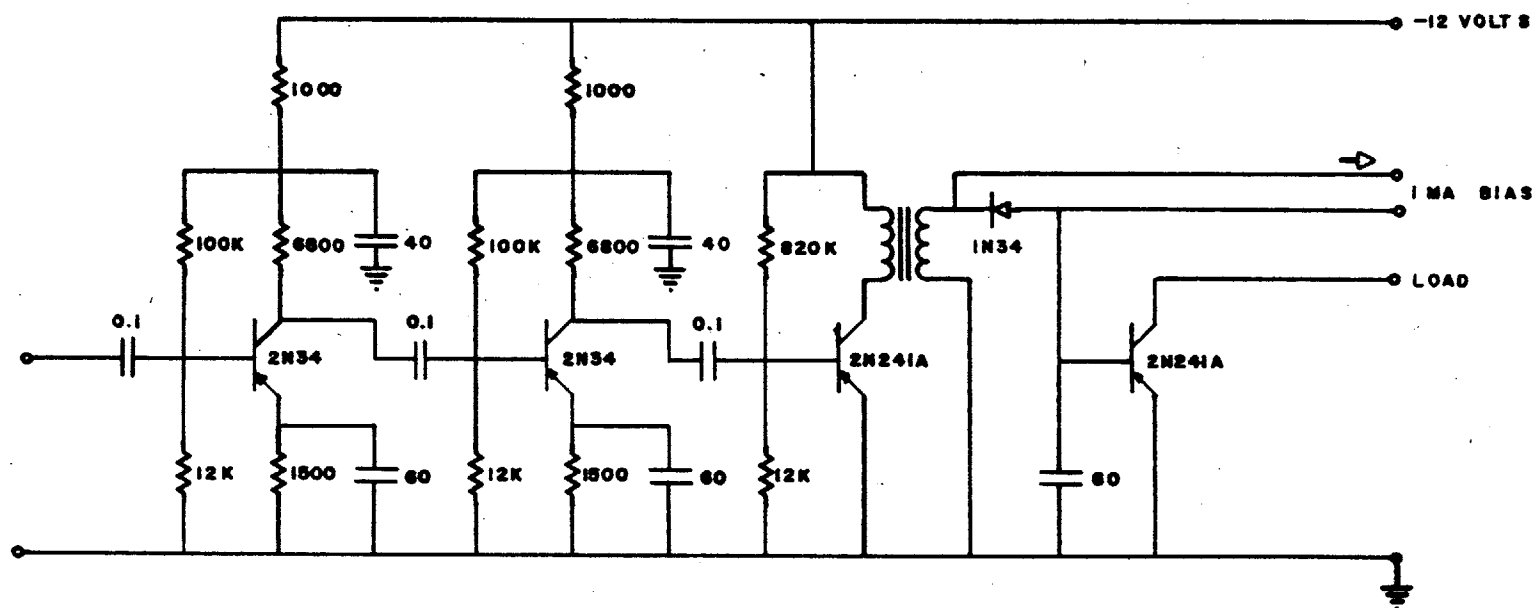
FIGURE 37   READ-OUT AMPLIFIER

The current source which forward biases the diode holds it off and any signal appearing across the transformer is shunted to ground through a capacitance of 60 microfarads, which at 3000 cycles per second represents only 0.8 ohm of reactive impedance. When the signal level rises and the current through the diode in the reverse direction equals that of the bias, the diode turns on, rectification of that part of the signal larger than the bias, I_s, occurs producing a negative potential at the base of the switching transistor. During the no-signal condition the small drop across the diode biases the base positive, preventing a runaway. With the bias the slope to the right of the breakpoint is much steeper, resulting in a much more rapid transition from the OFF state to the ON state of the switching transistor.

The amplifier of Figure 37 was constructed and tested in an experimental cryotron circuit. An input of 50 microvolts was required to achieve switching with the forbidden region (due to power dissipation) 10 db. with no bias, and only 1.5 db. with a bias of 1 milliampere.

The amplifiers are built as plug-in units, two amplifiers per unit, back to back as shown in Figure 38. The plug board, also shown in Figure 38, holds 6 such plug-in amplifiers as well as the individual bias adjusting potentiometers. The particular plug board shown in Figure 38, also has the Flexowriter relays, for reading to the Flexowriter from the computer which are the RM 1 through RM 7 of Figure 14. The two relays mounted near the left edge of the plug board are RMA and RMB of Figure 14, which feed information from the Flexowriter back to the computer during a print operation.

The signals that appear across the output gates which are to be displayed on the panel must be presented to the amplifiers and only one source of 3000 cycles necessary. To permit good shielding for the amplifiers as well as the interconnecting cables it is necessary
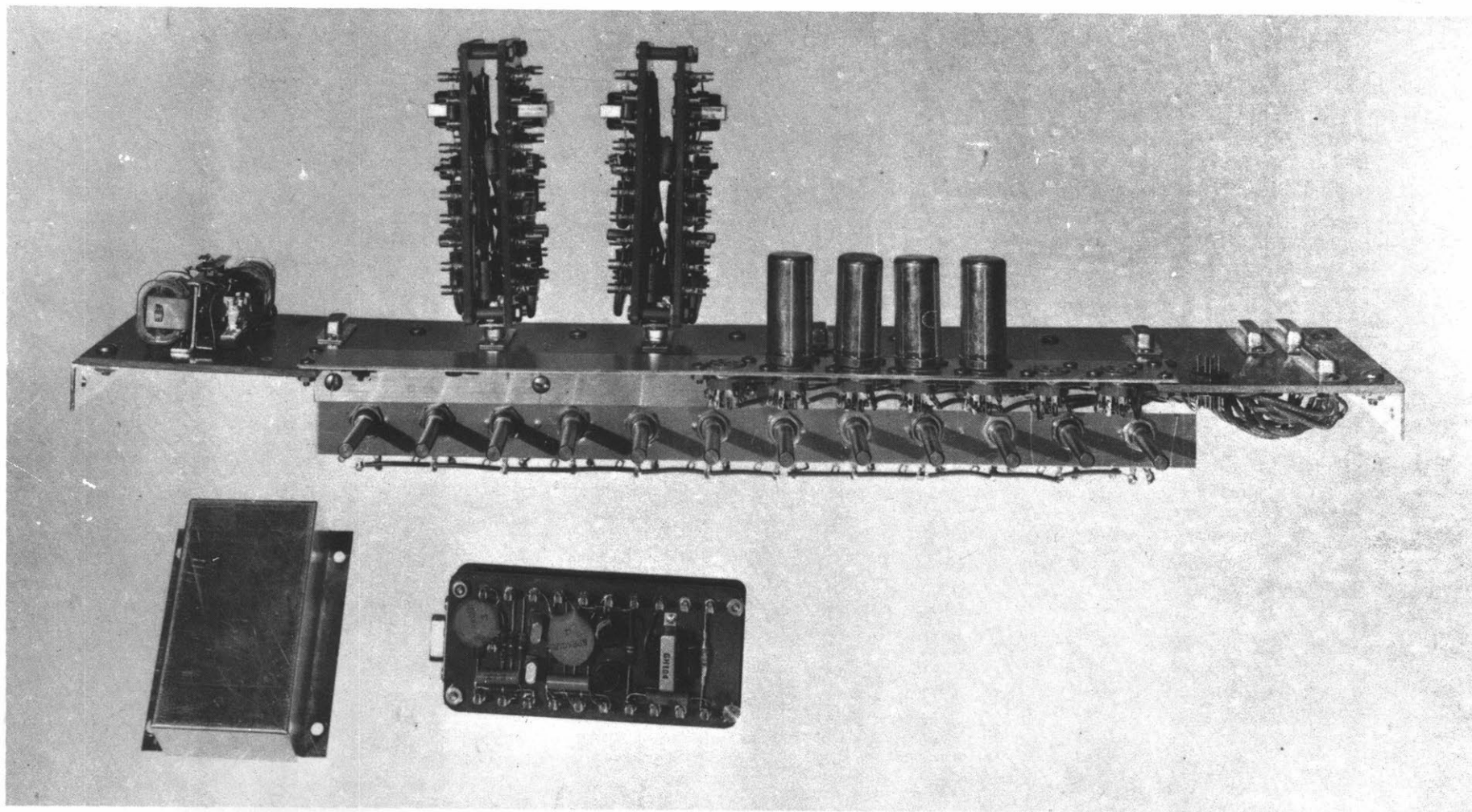
FIGURE 38   AMPLIFIERS AND PLUG BOARD

to have a common ground. The output across each gate is therefore
connected to a small transformer wound on a General Ceramics size
F259 core of Ferramic C. The primary is connected across the gate
which is to be sensed and has 5 turns of 0.003 inch Niobium. The
secondary has 55 turns of A.W.G. 30 copper wire. From the in-
ductance of the primary (0.088 microhenry) and the normal resistance
of the gate the magnitude of the excitation current in the primary
is approximately 1/2 that of the 3000 cycle current source.

5.2   INPUT

Input to the computer presents no problem in that the
Flexowriter printer itself supplies a coded (6 bit) output of 90 volts
which is used to activate a set of 6 relays through the contacts of
which a current goes to the input translation matrix as shown in
Figure 33.

CHAPTER VI

CONSTRUCTION OF CRYOTRON CIRCUITS

6.1   SUPERCONDUCTIVE JOINTS

The construction of wire-wound cryotron circuits using tantalum and niobium, requires superconductive joints between the wires. Several approaches to the problem were attempted without success. It was hoped tha a lead (or other superconductor) plating method could be found and that the many joints could be plated together simultaneously. As yet a superconductive bond between the lead and tantalum or the lead and the niobium has not been achieved.

At the present time inidvidual spotwelding of joints is the only reasonable method available. The quality of the spotweld is very dependent on the discharge time and stored energy of the spotwelder.

Superconductive shorts between the 0.003-inch niobium wire which is used for the control coil, and has a 0.0005-inch insulation of Formvar, and the bare 0.009-inch tantalum used for the gate occured approximately every 300 to 500 turns. Every third or fourth cryotron was therefore a reject. The tantalum was also insulated with 0.0005-inch Formvar with the result that in over 5000 turns of winding not one single short between a gate and a control winding occured.

6.2   MODULAR CONSTRUCTION

Construction of the computer circuits is to be modulized. The modules consist of 1/32-inch linen-base bakelite, approximately 1 inch wide and 8 inches long, with an array of 0.020-inch-diameter-holes. The 0.009-inch tantalum wire is bent down at each end of the control winding and threaded through these holes. Only one source current connection for each module is necessary and these connections need not be superconducting. Information paths however, between

the modules must be superconducting, and in the construction this is achieved through the use of special cryotrons in those places where either the gate or the control wires would normally go to another module. One module has a special control wound as a solenoid with an air core approximately 0.025-inches in diameter, but with no gate wire threading through it. The gate-wire from the other module is doubled back on itself , like a hairpin, and pushed through the control solenoid. Special control solenoids mounted on one module, will then plug into the corresponding doubled-back gate wire of another module. In this manner it is possible to achieve plug-in construction of the cryotron computer, and troublesome units may be easily replaced.

CHAPTER VII

CONCLUSIONS

7.1 SUMMARY

The material presented in this thesis may be classified into four catagories. First, the analysis of the basic switching functions usual to computer circuitry; second, a presentation of the general organization and specifications of the computer; third, the design of the individual circuits; and last, the methods of construction.

The analysis of the basic circuits in Chaper II is intended to aquaint the reader with the general form of cryotron circuits in their various realizations.

The general organization and specifications of the computer are presented in Chapter III Decisions as to whether particular circuits were to be pulse or d-c , synchronous or asynchronous, parallel or series were made in such a way as to achieve fast operation without extremely complex logic.

Chapter IV presents the computer circuits. Boolean Algebra was used in the design of some of the matrices, all other circuits having been designed without its use.

Chapter V treats the terminal equipment that is used to read-into and out of the cryotron computer. The amplifiers and the ferrite-core transformers have been constructed and tested with cryotron circuits. One series of tests on the output equipment extended over several hours with flawless operation.

In Chapter VI methods are given for modulizing the computer circuits into plug-in units, which couple information magnetically, thereby obtaining superconcuctive transfer of information without requiring permanent (as for example spot-welds) joints between modules.

7.2 SUGGESTIONS FOR FURTHER RESEARCH

This thesis presents and solves only a few of the problems associated with the design and construction of a large-scale cryotron system. A few of the areas where further work is required are listed below.

(a) Topological investigation of cryotron circuits for minimum crossovers of non-interacting paths.

(b) Investigation of the metals tantalum and niobium to find a method which will permit easy electroplating of lead onto the materials, with good superconducting bonds.

(c) An investigation to find a superconductor, the critical H field of which is independent of temperature in the region of operation.

APPENDIX I

COMMAND LINES

Command Line Number	Function
1	Read Adder into A register
2	Zero set A register
3	Complement A register
4	Shift left
5	Shift right
6	Read A register into Bus
7	Read A register into Adder
8	Read complement of A register into B register
9	Read A register into B register
10	Advance instruction counter
11	Read Bus into Memory
12	Read Memory into Bus
13	Transfer on Overflow
14	Test for Overflow
15	Switch clock to instruction cycle
16	Read Bus into B register
17	Read B register into Adder
18	Pulse carry to Add; Store overflow in overflow register
19	Read complement of Bus into B register
20	Read Address into Instruction counter
21	Read Address into Instruction counter if sign of A register is negative
22	Zero set overflow register
23	Read Bus into Print Register and zero set Print counter
24	Pulse to Print Flip-Flop
25	Pulse to deactivate clock
26	Read complement of address into shift-count counter
27	Read A register into B register via complement if negative
28	Zero set A register; Zero set Adder
29	Zero set Sign-order of A register
30	Pulse carry to add if right hand M register in state ONE
31	Complement A register if necessary via Sign storage register

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