A 28nm FDSOI integrated reconfigurable switched-capacitor based step-up DC-DC converter with 88% peak efficiency

A 28nm FDSOI Integrated Reconfigurable Switched-Capacitor based Step-Up DC-DC Converter with 88% Peak Efficiency

Avishek Biswas, *Student Member, IEEE,* Yildiz Sinangil, *Student Member, IEEE,* and Anantha P. Chandrakasan, *Fellow, IEEE*

***Abstract*—This paper presents a fully integrated, reconfigurable switched-capacitor based step-up DC-DC converter in a 28nm FDSOI process. Three reconfigurable step-up conversion ratios (5/2, 2/1, 3/2) have been implemented which can provide a wide range of output voltage from 1.2V to 2.4V with a nominal input voltage of 1V. We propose a topology for the 5/2 mode which improves the efficiency by reducing the bottom-plate parasitic loss compared to a conventional series-parallel topology, while delivering the same amount of output power. Further, the proposed topology benefits from using core 1V devices for all charge-transfer switches without incurring any voltage overstress. The converter can deliver load current in the range of 10 μA to 500 μA, achieving a peak efficiency of 88%, using only on-chip MOS and MOM capacitors for a high density implementation.**

***Index Terms*—Reconfigurable, Step-up DC-DC Converter, Switched Capacitor, Bottom-plate Parasitic Capacitance, Voltage Overstress Limitation, FDSOI, Body Biasing**

I. Introduction

With increasing integration of analog, digital and RF circuits in modern systems-on-chip (SoCs), there is a demand for a wide range of unique power supplies to cater to different functionalities. Hence, an on-chip power management unit (PMU) is necessary to efficiently convert and deliver these diverse power supplies from a single source. With the progress of CMOS scaling, the nominal supply voltage (V_{dd}) of the transistors has substantially decreased. For modern CMOS processes V_{dd} is around 1V, at which typical circuits operate. However, certain functionalities can necessitate generating voltages that are higher than V_{dd}. One such example is body-biasing [1]. It is well-known that the threshold voltage (V_t) of a transistor can be modulated by applying an appropriate body-bias voltage. This effect is more prominent in FDSOI (Fully Depleted Silicon On Insulator) transistors, for which we can apply a wide range ($>> V_{dd}$) of body-bias voltage. A step-up converter is necessary for generating these body-bias voltages. Another application for step-up converters is non-volatile memory [2], e.g. ReRAM, FeRAM etc., which operates at voltages higher than V_{dd}. Furthermore, applications like energy harvesting [3], [4] need to boost the source voltage to generate a higher output voltage. Thus, step-up DC-DC converters are an important component in the PMU for these kind of applications.

Fully integrated switched-capacitor (SC) based converters can achieve high conversion efficiency [5]–[7] and power density [8], which are key for on-chip implementation. To benefit from CMOS scaling, SC converters should utilize core transistors as charge-transfer switches, which offer lower on-resistance (R_{on}) with reduced capacitance. However, in order to avoid voltage overstress, these transistors cannot be operated with a gate-to-source/drain voltage of more than V_{dd}. This makes it very challenging [9] to design integrated step-up SC converters that ensure no overstress on transistors. Furthermore, another design challenge for SC converters is reconfigurability [10], [11]. It enables the same converter to be efficiently used to generate a wide range of output voltages, rather than using separate converters for each output voltage.

In this work we implement a reconfigurable step-up SC converter with 3 conversion ratios of 5/2, 2/1 and 3/2. This converter provides a wide range of output voltage from 1.2V to 2.4V, with a fixed input supply voltage of 1V. The step-up converter has been designed to obviate the need of using high voltage I/O transistors which otherwise would have degraded the efficiency owing to their higher R_{on} and capacitance, along with increasing the area. Additionally, a topology is proposed for the 5/2 mode which improves efficiency by reducing the bottom-plate parasitic loss as compared to a conventional series-parallel topology [12]. The converter was implemented in a 28nm FDSOI process [13]–[15] using only on-chip MOS and MOM (Metal-Oxide-Metal) capacitors that do not require any extra fabrication steps, unlike MIM (Metal-Insulator-Metal) [6] and trench capacitors [5].

This converter is designed specifically to generate body-bias voltages for SRAMs. Body-biasing is used to modulate threshold voltage (V_t) of transistors. This effect is more pronounced for FDSOI transistors [1], where the change in V_t is linear with the amount of body-bias applied. In SRAMs body-biasing can be used to improve read/write margins. To generate a wide range of body-bias voltage this reconfigurable step-up converter can be used. Since body-biasing can be dynamic, hence, the converter needs to supply some load current (typically a few 100 uA's).

This paper is organized as follows. Section II discusses the operation of the various conversion modes and also presents a performance comparison of the proposed topology for the 5/2

This work was funded by DARPA. The views and conclusions contained herein are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Government.

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mode as compared to the conventional series-parallel topology. In section III, the MOS implementation of the converter is described along with the required driver circuitry. Section IV illustrates the overall architecture of the step-up converter along with the necessary auxilliary circuits. Section V presents the measured performance of the converter for various operating modes and load currents. Concluding remarks are discussed in section VI.

II. Reconfigurable Step-up SC Module

Fig.1 shows the switch level schematic of a single module of the reconfigurable step-up converter. A module is comprised of two identical sub-modules (A and B) which are connected by switch S_8. Each sub-module consists of 7 switches ($S_1 - S_7$), 2 charge-transfer capacitors (C_1, C_2) and is driven by two non-overlapping, complementary clocks (CLK_1, CLK_2). Additionally, sub-module A operates out-of-phase with sub-module B. This design strategy allows us to reuse simple 2/1 sub-modules to design a more complex 5/2 conversion module.

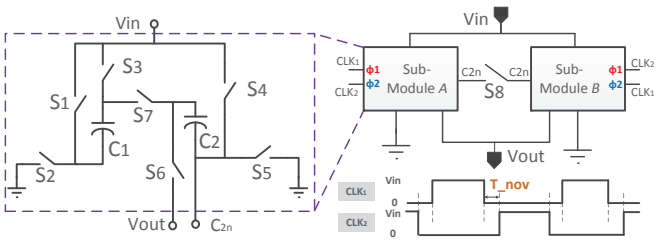


Fig. 1. Reconfigurable step-up switched capacitor module.

Fig. 2(a) shows the operation of the converter in the 5/2 mode for the proposed topology. As shown in the figure, during phase Φ_1, capacitors C_{1a} and C_{2b} are charged from the input node, V_{in}, while capacitors C_{2a} and C_{1b} transfer charge to the output node, V_{out}. On the other hand, during phase Φ_2, C_{1b} gets charged from the input node and C_{2a} gets charged by C_{1a}, while C_{2b} transfers charge to the output node. Also shown in the figure are the voltages across the different charge-transfer capacitors for the no-load case. Using charge balance, it is easily seen that the voltage across each capacitor is identical during the two phases Φ_1 and Φ_2 which proves that, in the steady state, this mode will generate a no-load output voltage $V_{out,NL} = 5/2 \times V_{in}$. Fig. 2(b) shows the operation of a conventional series-parallel topology [12] implementing a 5/2 mode. In this case, all the capacitors get charged from the input in phase Φ_2 and transfer charge to the output in phase Φ_1. Although both the topologies require the same number of capacitors and switches to implement a 5/2 mode, the proposed topology offers two significant benefits compared to the conventional topology.

Firstly, for the proposed implementation, charge is delivered to the output in both the clock phases, Φ_1 and Φ_2. However, in the conventional topology, charge is delivered to the output in only phase Φ_1. Hence, the droop in the output voltage during one clock period is lesser for the proposed implementation. Fig. 3(a) shows the simulated result for the ideal converter in 5/2 mode. As can be seen from the figure, the proposed topology reduces output voltage ripple by $2\times$ compared to the conventional case.

Second and more importantly, the proposed topology offers better performance in terms of reducing bottom-plate parasitic loss, which is a significant component of the overall loss for on-chip implementation of the charge-transfer capacitors [11], [16]. On-chip capacitors offer a much higher energy density compared to their off-chip counterparts, but they suffer from having considerably more parasitic capacitance (associated with their bottom or top plate and the substrate). This parasitic can be as high as 5-10% [16] of the actual capacitance for the MOS capacitors used in this design. In SC converters, this parasitic capacitor gets charged in one phase and loses that energy by discharging in the other phase. The bottom (or top)-plate parasitic loss associated with this voltage swing (V_{par}) can severely degrade the efficiency of the converter especially for low output power levels [11], [17]. This charge-discharge loss can be calculated for each parasitic capacitor as: $P_{bot} = C_{par}V_{par}^2 f_{sw}$. The proposed implementation for the 5/2 mode significantly decreases this loss component by reducing the swing of the bottom (or top) plate of the charge-transfer capacitors. It can be observed from Fig. 2 that,

$$P_{bot}(prop.) = \alpha C_f \left(V_{in}^2 + \left(\frac{V_{in}}{2}\right)^2 + V_{in}^2 + \left(\frac{V_{in}}{2}\right)^2 \right) f_{sw}$$
$$= 2.5\alpha C_f V_{in}^2 f_{sw} \quad (1)$$

where α denotes the ratio of the bottom-plate parasitic capacitor and the corresponding charge-transfer capacitor (C_f) and f_{sw} denotes the switching frequency of the converter. The four components for calculating P_{bot} in (1) arise from the parasitic capacitances associated with the four charge-transfer capacitors, C_{1a}, C_{2a}, C_{1b} *and* C_{2b} respectively. For the conventional series-parallel implementation, this loss can be similarly calculated as

$$P_{bot}(conv.) = \alpha C_f \times$$
$$\left(\left(\frac{3V_{in}}{2}\right)^2 + \left(\frac{V_{in}}{2}\right)^2 + \left(\frac{3V_{in}}{2}\right)^2 + V_{in}^2 \right) f_{sw}$$
$$= 5.75\alpha C_f V_{in}^2 f_{sw} \quad (2)$$

Hence we get a 2.3X reduction in bottom-plate parasitic loss which significantly improves the efficiency. As seen from Fig. 3(b), for the ideal converter with 2% bottom-plate parasitic ($\alpha = 0.02$), we can get an efficiency improvement as high as 15%. This comparison assumes that the total amount of charge-transfer capacitance, the load capacitance and the load resistance are the same for both topologies. It should be noted that the efficiency improvement in the proposed topology is not at the expense of power-density. Fig. 3(a) shows that both the topologies offer similar output impedance, R_{OUT} ($= \frac{1}{Cf_{sw}}$, Appendix), and hence they can deliver similar amount of load power.

The operation in the other two modes (2/1 and 3/2) is illustrated in Fig. 4. It may be noted that in mode 2/1 the capacitors C_1 and C_2, in each sub-module, work exactly in

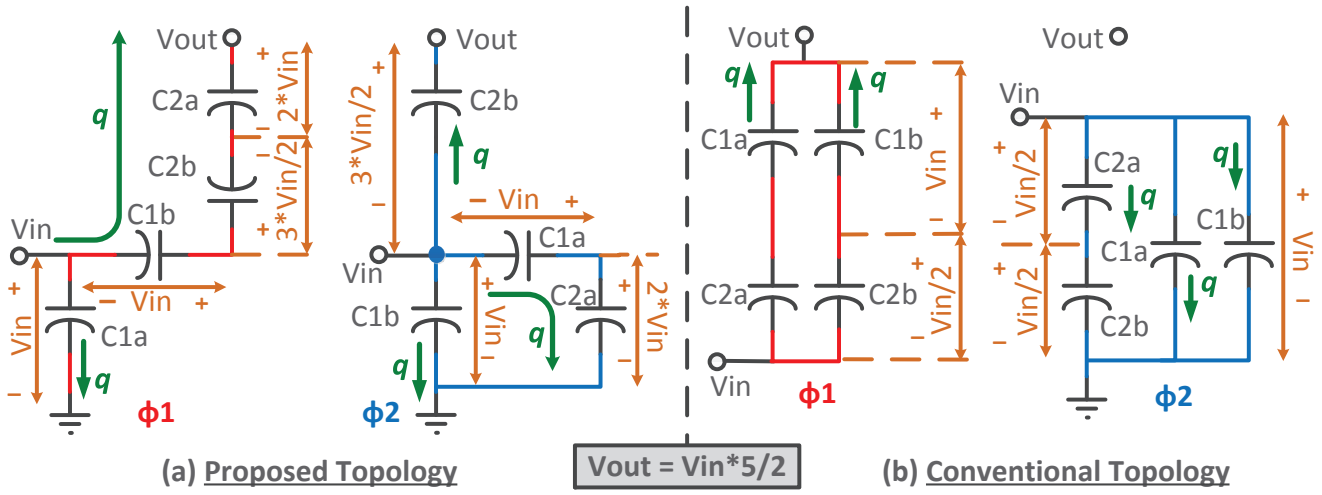


Fig. 2. Operation of the proposed and conventional topologies in 5/2 mode.

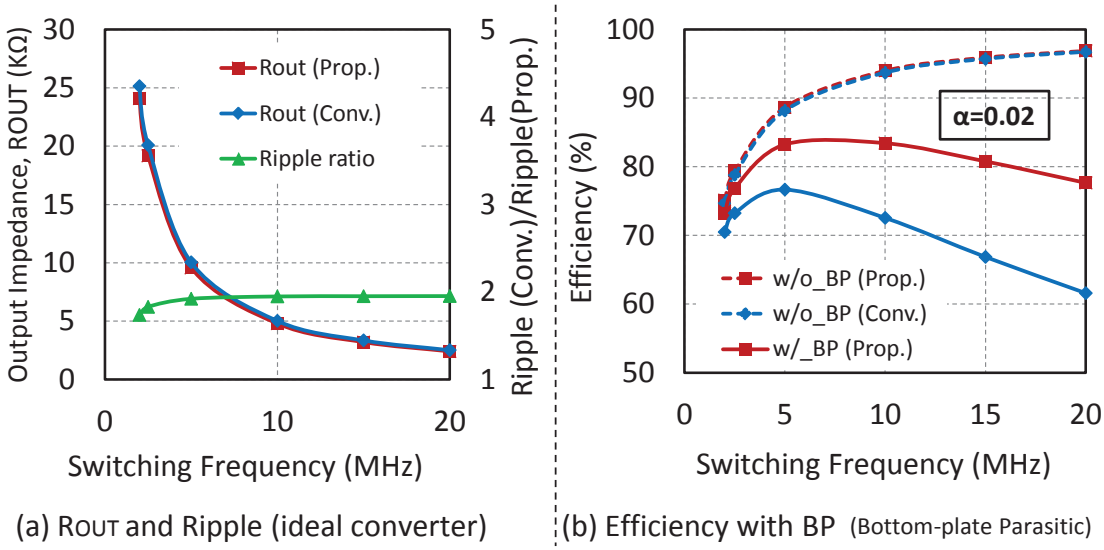


Fig. 3. Simulated performance comparison of the ideal converter for the proposed and conventional topologies in 5/2 mode.

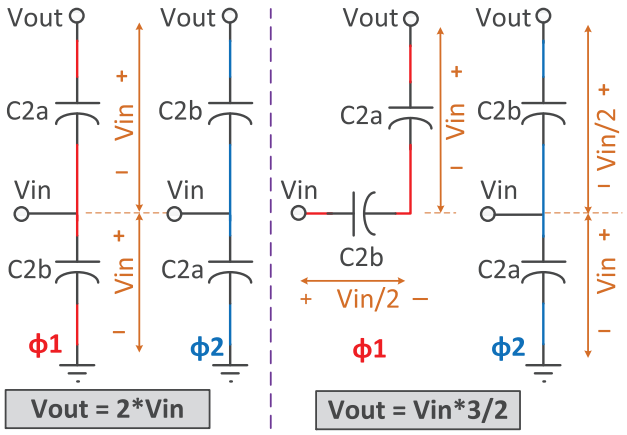


Fig. 4. Operation of the converter in 2/1 and 3/2 modes.

the same manner. Hence, for clarity, only one (C_2) is shown in Fig. 4. The bottom-plate loss for the modes 2/1 and 3/2 can be calculated as follows:

$$P_{bot}(2/1) = \alpha C_f \left(V_{in}^2 + V_{in}^2 + V_{in}^2 + V_{in}^2\right) f_{sw} = 4\alpha C_f V_{in}^2 f_{sw} \quad (3)$$

$$P_{bot}(3/2) = \alpha C_f \left(\left(\frac{V_{in}}{2}\right)^2 + \left(\frac{V_{in}}{2}\right)^2\right) f_{sw} = 0.5\alpha C_f V_{in}^2 f_{sw} \quad (4)$$

The switch configuration for the two sub-modules in the 3 different modes is shown in Table.I. As seen from the table, the ON phase of each switch in sub-module A is opposite to that in sub-module B. This greatly simplifies the design of the converter, since the same sub-module and its associated control and gate-drive circuitry can be reused by just flipping the 2 clock inputs.

TABLE I
SWITCH CONFIGURATION OF THE TWO SUB-MODULES IN THE 3 DIFFERENT MODES

Switch	S_1	S_2	S_3	S_4	S_5	S_6	S_7
Mode 5/2	Φ_2	Φ_1	Φ_1	OFF	Φ_2	Φ_1	Φ_2
Mode 2/1	Φ_1	Φ_2	Φ_2	Φ_1	Φ_2	Φ_1	Φ_2
Mode 3/2	OFF	OFF	Φ_2	OFF	Φ_2	Φ_1	Φ_2

(a) Sub-module A

Switch	S_1	S_2	S_3	S_4	S_5	S_6	S_7
Mode 5/2	Φ_1	Φ_2	Φ_2	Φ_2	OFF	Φ_2	Φ_1
Mode 2/1	Φ_2	Φ_1	Φ_1	Φ_2	Φ_1	Φ_2	Φ_1
Mode 3/2	OFF	OFF	Φ_1	Φ_2	OFF	Φ_2	Φ_1

(b) Sub-module B

The power delivered to the load ($P_{out} = I_{load} \times V_{out}$) in the 3 different modes can be calculated as follows:

$$P_{out}(5/2) = \left(\frac{5V_{in}}{2} - V_{out}\right) C_f f_{sw} \times V_{out} = I_{load} \times \left(\frac{5V_{in}}{2} - \frac{I_{load}}{C_f f_{sw}}\right) \quad (5)$$

$$P_{out}(2/1) = 4\left(2V_{in} - V_{out}\right) C_f f_{sw} \times V_{out} = I_{load} \times \left(2V_{in} - \frac{I_{load}}{4C_f f_{sw}}\right) \quad (6)$$

$$P_{out}(3/2) = 2\left(\frac{3V_{in}}{2} - V_{out}\right) C_f f_{sw} \times V_{out} = I_{load} \times \left(\frac{3V_{in}}{2} - \frac{I_{load}}{2C_f f_{sw}}\right) \quad (7)$$

where I_{load} denotes the load (i.e. output) current, V_{out} denotes the output voltage, and C_f denotes each of the four charge-transfer capacitors in a single module. The I_{load} in equations (5)-(7) is calculated from the summation of the charge transferred (Appendix) to the output node by each flying capacitor, i.e. $I_{load} = \sum_i q_{out,C_i} \times f_{sw} = \sum_i C_i \Delta V_{C_i} \times f_{sw}$. As seen from the above equations, maximum power can be delivered to the load in the mode 2/1. Equivalently, a given amount of load current can be delivered with a lower switching frequency in the 2/1 mode as compared to the other two modes.

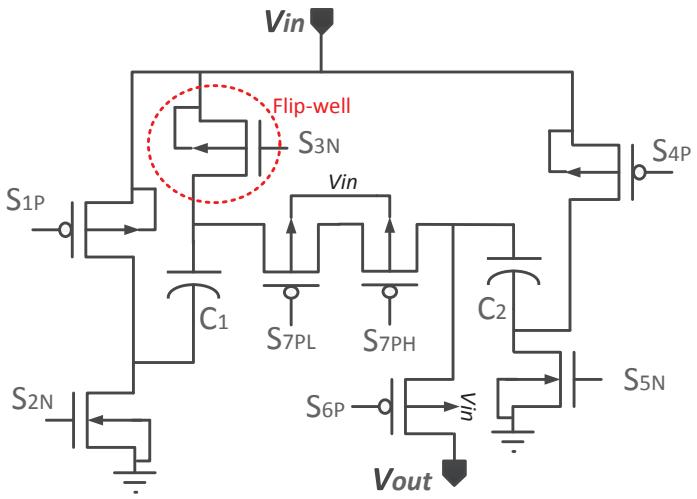
III. MOS IMPLEMENTATION OF THE SUB-MODULE

In this design, all the charge-transfer switches in the main converter module have been implemented with core (1V) transistors. It is important to ensure that none of the transistors are overstressed due to application of a gate-to-source (V_{GS}) or drain-to-source (V_{DS}) voltage higher than the nominal supply voltage, V_{dd}. Fig. 5 shows the MOS implementation of the switches for a sub-module and the associated gate-drive levels for them. The bottom-plate of both the capacitors C_1 and C_2 remain within the voltage range of 0 to V_{dd}. Hence the switches (S_1, S_2, S_4, S_5) which are connected to the bottom-plates of C_1 and C_2 have been implemented with regular PMOS (S_{1P}, S_{4P}) and NMOS (S_{2N}, S_{5N}) transistors. Although not shown in the figure, these transistors are driven by buffers in the voltage range 0 to V_{dd}.

Switch S_3 connects the top-plate of capacitor C_1 to V_{dd} and is turned OFF when the top-plate of C_1 goes to $2V_{dd}$. Hence, it is implemented with an NMOS transistor (S_{3N}) with a gate drive between V_{dd} and $2V_{dd}$, to avoid V_{GS} overstress. It may be noted that the body terminal of S_3 is connected to V_{dd}, which is also its source terminal. This is done to avoid the increase in its threshold voltage due to reverse body-biasing if the body terminal was connected to ground. Hence, a flip-well device (NMOS on n-well) is used for this switch. Flip-well devices [15] are a standard feature for FDSOI technology. In a regular bulk-CMOS technology, this can be achieved by using a triple-well transistor.

Switch S_6 needs to connect the top-plate of the capacitor C_2 to the output voltage node V_{out} and is OFF otherwise. Hence, it is implemented with a regular PMOS transistor (S_{6P}) but with a gate drive between $(V_{out} - V_{dd})$ and V_{out}, so that the maximum V_{GS} applied is V_{dd} and the transistor is not overstressed. The body-terminal of this PMOS transistor is connected to $V_{in}(= V_{dd})$, which is lower than its source potential $(= V_{out})$. Thus a forward body-bias (FBB) is applied to this PMOS, which reduces its V_t and helps in improving its overdrive voltage $(= V_{SG} - V_t)$. The gate-drive of S_6 is provided by the '$V_o - V_i$ $shifter$' circuit shown in Fig.6.

Switch S_7 operates in a wide range of voltage levels, which depend on the conversion mode. It needs to block a voltage of $(V_{out} - V_{dd})$ across it, which can be as high as $2.5 - 1 = 1.5V$ in 5/2 mode. Hence, to avoid a V_{DS} overstress, it is implemented with a cascode of two 1V regular PMOS transistors (S_{7PL} and S_{7PH}). Fig.7 shows the gate voltages required to drive this cascode switch structure in the 3 different modes, while ensuring that V_{SG} and V_{SD} of both the PMOS transistors are $\leq V_{in}(= V_{dd})$. Conventionally [18] a



Switch	Gate-drive Voltage Range
S1P	**0** to **Vin**
S2N	**0** to **Vin**
S3N	**Vin** to **2Vin**
S4P	**0** to **Vin**
S5N	**0** to **Vin**
S6P	**(Vout-Vin)** to **Vout**
S7P_L	**Variable**
S7P_H	**Variable**

Fig. 5. MOS implementation of the switches in a sub-module and their corresponding gate-drives.

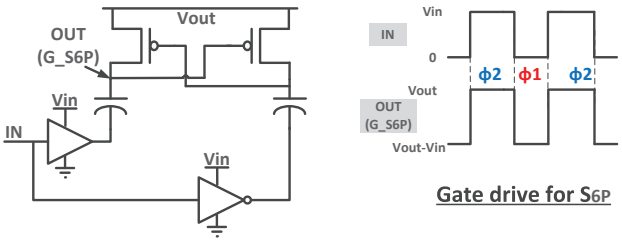


Fig. 6. $V_o - V_i$ shifter circuit for driving switch S_6.

suitable DC voltage needs to be generated to bias this cascode switch structure. In this design, the need for a separate DC voltage is obviated by dynamically biasing the gate of both the transistors, S_{7PL} and S_{7PH}, to turn them ON and OFF simultaneously. It may be noted that the dynamic biasing is also dependent on the conversion mode. Hence it needs to be reconfigurable to work across all the three conversion modes (5/2, 2/1, 3/2).

Fig. 8 shows the reconfigurable gate-drive structures for switches S_{7PL} and S_{7PH}. The LS_EN circuit shown in Fig.8a is a modified 1-to-2 level shifter circuit with enable (EN). When EN = '1', the bottom NMOS stack is cut-off, and the circuit behaves as a 1-to-2 level shifter with the capacitor C_c providing the ac coupling. However, when EN = '0' the top PMOS is cut-off. Hence, with IN = '0' the OUT node is pulled down to ground by the bottom NMOS stack. And when IN becomes '1' both the top and bottom stacks are cut-off and the OUT node is pulled up to V_{in} by the coupling action of the capacitor C_c.

Fig.8b shows the reconfigurable level shifter circuit to drive the switch S_{7PH}. It consists of an inverter structure formed by P_1 and N_1, whose gate and source terminals are biased dynamically to generate the required voltage level at its output node (OUT). In mode 5/2, the source of N1 (V_{S_N}) is biased at V_{in}. When IN = '1', the gate of N1 is at $2V_{in}$; hence it turns ON and passes V_{in} to the output. During this time the PMOS P1 is OFF, since its source voltage $V_{S_P}(= V_{out} - V_{in})$ is less than its gate voltage ($= V_{out}$). On the other hand, when IN = '0' the NMOS N1 is turned OFF since its V_{GS} is zero. Whereas, the gate of P1 is biased at $V_{out} - V_{in}$ while its source is at V_{out} and hence, it passes V_{out} to the output node. The operation of this circuit in mode 3/2 is similar to mode 5/2, except that the low voltage level is at ground instead of V_{in}. This is done by biasing V_{S_N} to ground by a static inverter. In mode 2/1 the operation of this reconfigurable gate-drive circuit is a little different. In this mode, the PMOS P1 is always kept OFF by making sure its gate and source voltages are the same and hence its $V_{SG} = 0$. On the other hand, the NMOS N1 is ON in both the phases (Φ_1 & Φ_2). This is done by dynamically changing its gate and source voltages, such that V_{GS} is always equal to V_{in}. And hence, only N1 is used to pass both the voltage levels V_{in} and 0 to the output node. The '$V_o - V_i$ $Shifter$' block, shown in Fig.8b, is the same circuit as described in Fig.6. The logic works out such that the source of the PMOS P1, i.e. V_{S_P}, in a sub-module (e.g. A) can be driven from the gate-drive of switch S_{6P} of the other sub-module (B, which operates out of phase with A). Whereas, the source node of N1, i.e. V_{S_N}, is driven to either V_{in} or ground by an inverter with the associated logic circuit. Thus, the same level-shifter circuit can be reconfigured to provide different voltage levels for the gate-drive of switch S_7, which leads to an area-efficient implementation.

The switch S_8, connecting the two sub-modules, was implemented with regular 1V PMOS and NMOS transistors in a tramsission gate structure, since it needs to pass a voltage of $V_{in}/2$.

The charge-transfer capacitors were implemented on-chip with high density MOS capacitors along with MOM capacitors stacked on top to improve density. 1V regular MOS transistors were used for C_{1a} & C_{1b}. Whereas, high voltage I/O devices were used for C_{2a} & C_{2b}, which need to support a maximum voltage of $2V_{in}$ across them. For MOS capacitors soft connection of the n-well [16], [12] was adopted. As shown in Fig.9, the n-well of the MOS transistor is biased with a high resistance to the output node V_{out}. This reduces the

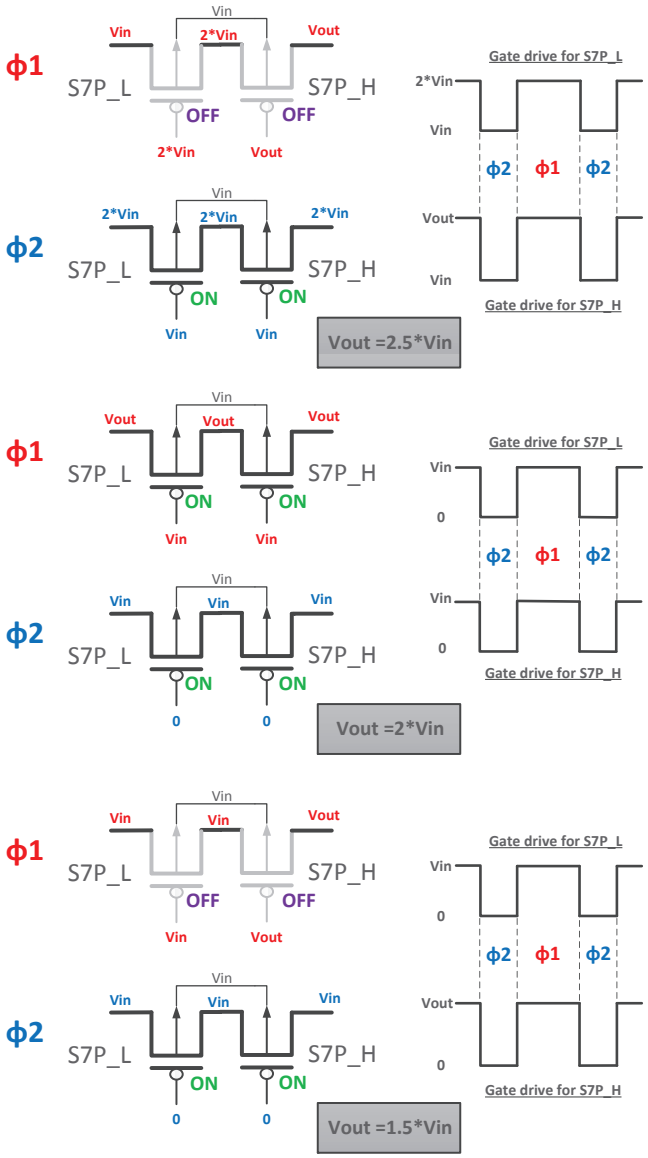
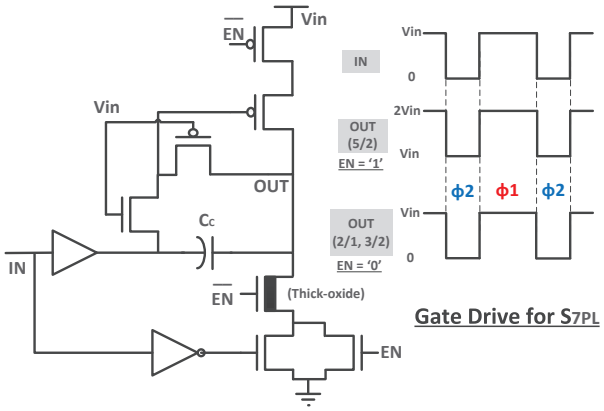
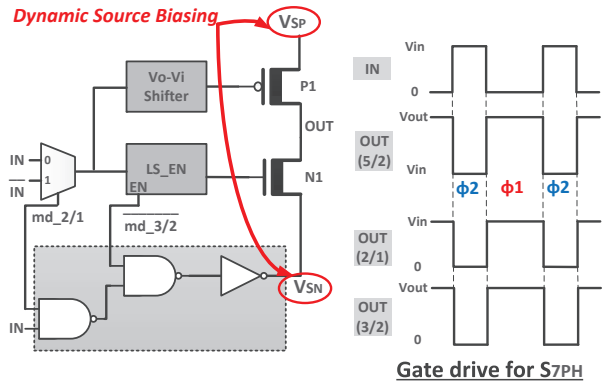


Fig. 7. Gate-drive for the cascode switch structure S_{7PL} and S_{7PH} in the 3 different modes.



(a) Level Shifter with Enable (LS_EN), also used for driving S_{7PL}



(b) Gate-driver for switch S_{7PH}

Fig. 8. Reconfigurable gate-drive circuits for the cascode switch structure S_{7PL} and S_{7PH}.

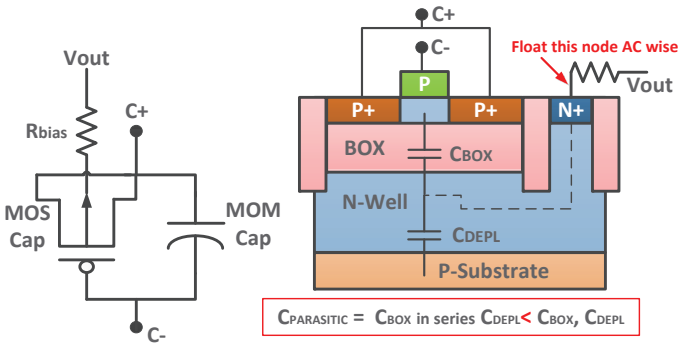


Fig. 9. Implementation of charge-transfer capacitors with parasitic reduction technique.

parasitic capacitance to substrate in two ways. Firstly, the DC bias of the n-well node is set at the highest voltage in the circuit, namely V_{out}. This reduces the n-well to substrate capacitance (C_{DEPL}), which is inversely proportional to the bias voltage across it. Secondly, the n-well node is at high impedance because of the resistor R_{bias}. Hence, the two parasitic capacitors, C_{DEPL} and C_{BOX} (due to the buried oxide layer [13] in FDSOI transistors), are effectively in series. Therefore, the overall top(or bottom)-plate parasitc capacitance to the substrate is:

$$C_{parasitic} = C_{top/bot} = \frac{C_{DEPL}C_{BOX}}{C_{DEPL} + C_{BOX}} < C_{DEPL}, C_{BOX} \tag{8}$$

Hence, this technique significantly reduces the parasitic capacitance to ground and improves efficiency of the converter in all the 3 modes.

IV. Overall System Architecture

Fig. 10 shows the overall architecture of the converter. This work implements 4-phase interleaving in order to reduce output voltage ripple. The 4-phase clock generator, shown in Fig.11, uses a cascade of D-flip-flops to divide an external clock (frequency f_{sw}) into 4 phases (frequency $f_{sw}/4$), each shifted by $45°$. Each phase generates two complementary non-overlapping clocks, which drive a single converter module. A tunable circuit, shown in Fig.12, has been implemented to control the non-overlapping delay, which is crucial to reduce shoot-through current loss. Reconfigurable switch drivers, as

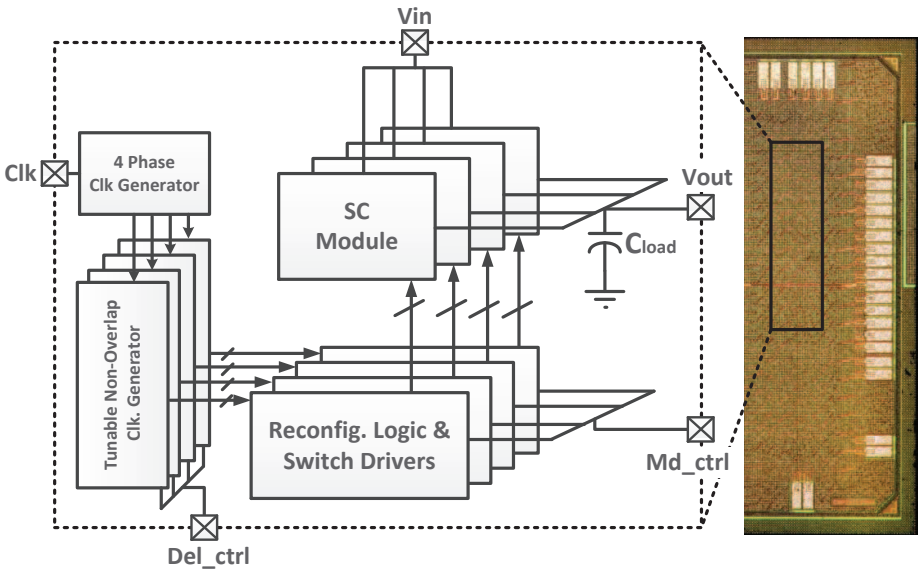


Fig. 10. Overall system architecture with die photo.

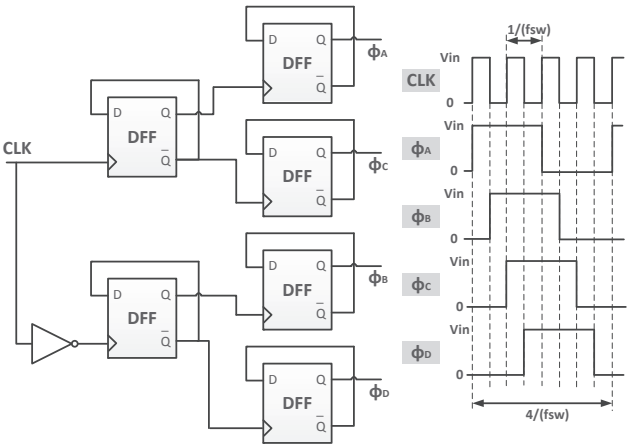


Fig. 11. 4 phase clock generation for interleaving.

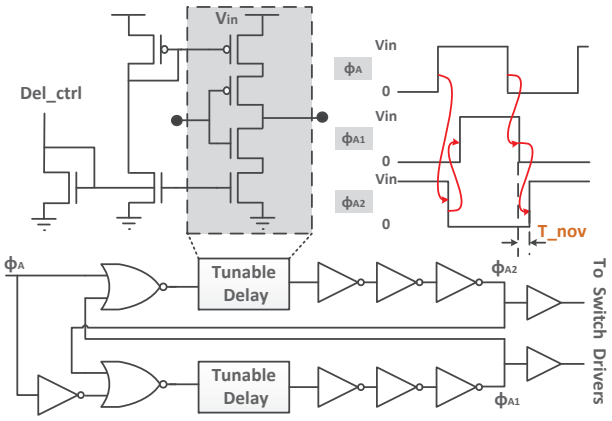


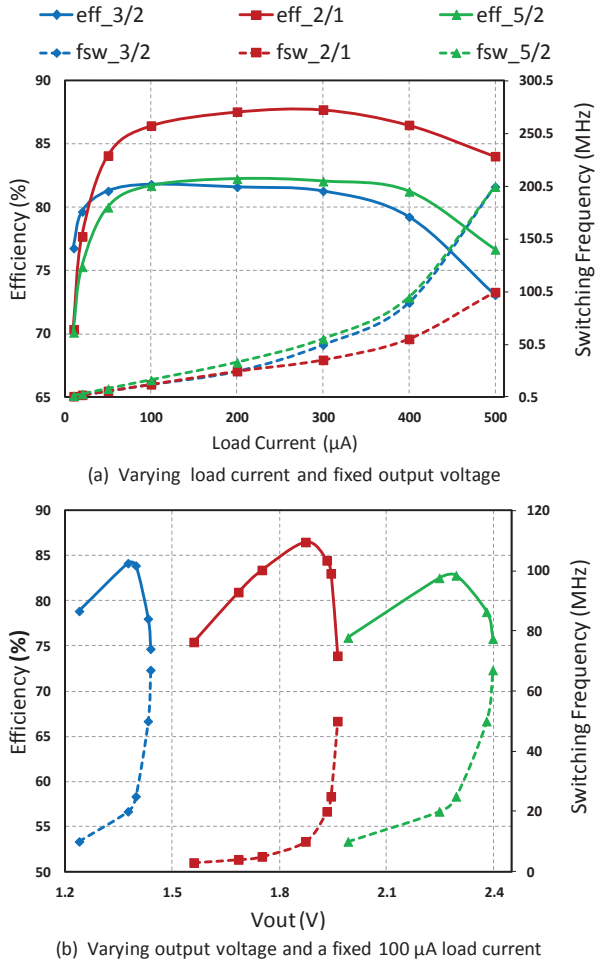
Fig. 12. Tunable non-overlapping clock generation circuit.

explained in the previous section, provide the gate drives for all the switches in each module. An on-chip load capacitor (300pF) provides further necessary ripple reduction at the output.

V. Results

The fully integrated step-up converter was implemented in a 28nm FDSOI process occupying a core area of $0.054mm^2$. An additional $0.06mm^2$ area was used to implement an on-chip load capacitor. Fig. 10 shows the die photo of the converter. The measured efficiency (η) of the converter with varying load current (I_{load}) and $V_{in} = 1V$ is plotted in Fig. 13(a). The output voltage was kept constant at approximately $2.2V$ (mode 5/2), $1.9V$ (mode 2/1) and $1.3V$ (mode 3/2), by changing the switching frequency $(f_{sw}/4)$ of the converter, where f_{sw} denotes the switching frequency of the main (external) clock. As seen from the figure, the converter can supply a load current in the range $10 - 500\ \mu A$ while maintaining an efficiency of more than 70%. It achieves a peak efficiency (η_{peak}) of 88% for the 2/1 mode at $P_{out} = 0.56mW$ and 82% for the 5/2 mode at $P_{out} = 0.66mW$. The efficiency at low load currents of a few 10's of μA is also quite high $(> 70\%)$. This can be mainly attributed to the fact that the bottom-plate parasitic loss is highly reduced in this implementation by careful design of topology (to minimize the bottom-plate swing) as well as by reducing the value of the parasitic capacitance. Fig. 13(b) shows the measured performance with a fixed load current of 100 μA and varying output voltage for the 3 modes. The converter provides an output voltage ranging from $\approx 1.2V\ to\ 2.4V$ with more than 70% efficiency $(V_{in} = 1V)$. Modes 3/2, 2/1 and 5/2 are used to generate V_{out} in the ranges 1.2V to 1.4V, 1.4V to 1.9V and 1.9V to 2.4V, respectively. It can be observed that increasing the switching frequency of the converter increases the output voltage by decreasing the output impedance (R_{OUT}) of the converter. However this effect saturates for higher frequencies, since the converter enters the fast-switching-limit (FSL) mode in which

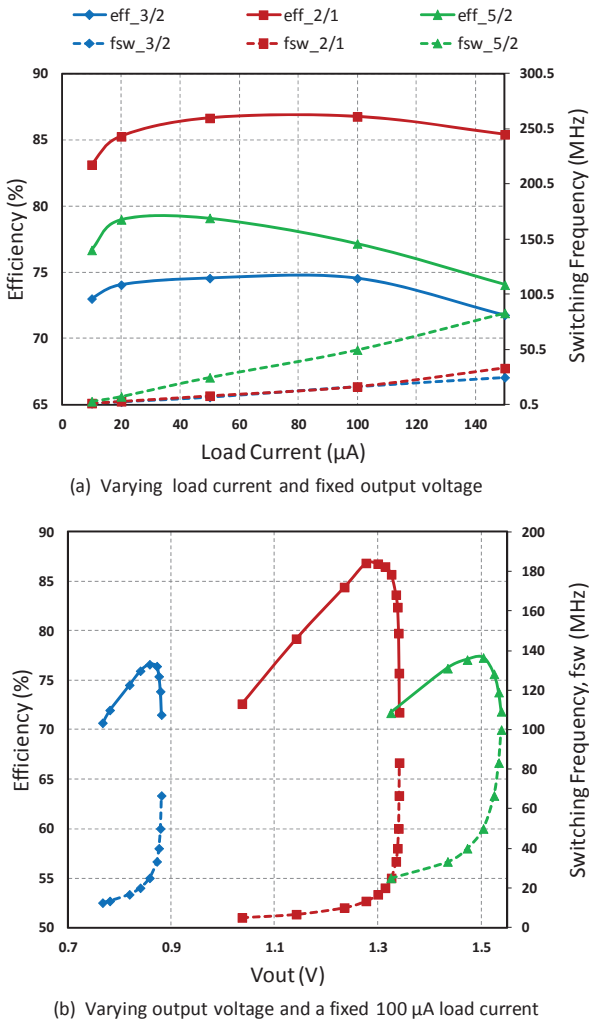
the non-zero resistance of the MOS switches limit R_{OUT}.



(a) Varying load current and fixed output voltage

(b) Varying output voltage and a fixed 100 µA load current

Fig. 13. Measured performance of the converter with $V_{in} = 1V$.



(a) Varying load current and fixed output voltage

(b) Varying output voltage and a fixed 100 µA load current

Fig. 14. Measured performance of the converter with $V_{in} = 0.7V$.

The converter functions properly even at lower V_{in} values. Fig.14 shows the measured performance of the converter with $V_{in} = 0.7V$. As seen from the figure, the converter can deliver currents from $10\mu A$ to $150\mu A$, while maintaining more than 70% efficiency. For Fig.14(a), the output voltage was kept constant at approximately $1.5V$ (mode 5/2), $1.3V$ (mode 2/1) and $0.8V$ (mode 3/2), by changing the switching frequency (f_{sw}) of the converter. The converter achieves a peak efficiency of 86.8% in the 2/1 mode and at $Pout = 0.13mW$. Fig.14(b) shows the performance of the converter with a fixed load current of $100\ \mu A$. The converter provides V_{out} from 0.75V to 1.5V while maintaining more than 70% efficiency, even with a low V_{in} of 0.7V.

Table.II shows the performance comparison with previous works on step-up switched-capacitor DC-DC converters. This work achieves a peak-efficiency as high as 88% even with using MOS capacitors, which have a much lower density and higher parasitic capacitance as compared to MIM [6] and trench capacitors [5]. Furthermore, the output voltage range is much higher than previous works, thanks to the reconfigurability of the converter. The (unoptimized) area of the proposed converter is higher as compared to [5] and [6]. This is because a large portion of the area is occupied by the load capacitor, which has to be implemented with a low density MOM capacitor to support a high output voltage of 2.4V. Also, some of the charge-transfer capacitors have to be implemented with low density I/O transistors to support a high voltage $(> V_{dd})$ across them in the 5/2 mode. If the maximum output voltage requirement is not that high, the converter area can be hugely reduced by utilizing low-voltage denser capacitors. In addition, the number of interleaving stages could be increased to reduce the amount of load capacitance needed.

As seen from Table.II, [5] achieves a slightly higher peak efficiency (90%) because of the use of highly dense (200 fF/μm^2) trench capacitors, which also have a much lesser bottom-plate parasitic capacitance as compared to a capacitor implemented with regular MOS transistors. Bottom-plate parasitic loss is a major loss component for the power levels we are dealing with. Therefore, use of trench capacitors would improve both the efficiency and the power density of the converter, even if everything else in the design is kept the same. This work achieves a higher peak efficiency $(88\%\ @P_{out} = 0.56mW)$ than [6] $(82\%\ @P_{out} = 1.5mW)$, which uses MIM capacitors. As seen from Table.II, the efficiency of the proposed converter is still high (83%) even at a

higher output power level of $1.73mW$. Furthermore, since the proposed converter is reconfigurable it provides a much wider output voltage range $(1.2V - 2.4V)$ as compared to [6], while occupying similar area (taking into account the technology scaling factor).

VI. Conclusion

This paper presents a fully integrated, reconfigurable SC step-up DC-DC converter in a 28nm FDSOI process. The converter uses only on-chip MOS and MOM capacitors, which do not require extra fabrication steps unlike MIM and trench capacitors. It implements three conversion ratios, 5/2, 2/1 and 3/2, to provide a wide range of output voltage $(1.2V - 2.4V)$, from a fixed input voltage of $1V$. A topology was proposed for the 5/2 mode which reduces parasitic bottom-plate capacitor loss and improves efficiency compared to a conventional series-parallel topology. The design uses core 1V transistors for all charge-transfer switches with reconfigurable gate drive circuits, to eliminate steady-state voltage overstress. The converter maintains over 70% efficiency even at a low load current of $10\ \mu A$, achieving a peak efficiency of 88% at an output power level of $0.56\ mW$ in the 2/1 mode.

Appendix
R_{OUT} calculation for the proposed and conventional 5/2 topologies

A. Proposed 5/2 topology

Referring to Fig.2, for phase Φ_1 let us denote the common top-plate node voltage of the capacitors C_{1b} and C_{2b} as V_x and the common bottom-plate node voltage of the capacitors C_{2a} and C_{2b} as V_y. Additionally, for phase Φ_2 let us denote the common top-plate node voltage of the capacitors C_{1a} and C_{2a} as V_z.

Now, using charge-balance for each of the capacitors C_{1a}, C_{2a}, C_{1b} and C_{2b} in the two phases we get:

$$q = (V_{in} - (V_z - V_{in}))C_f \tag{9a}$$

$$q = (V_z - (V_{out} - V_y))C_f \tag{9b}$$

$$q = (V_{in} - (V_x - V_{in}))C_f \tag{9c}$$

$$q = ((V_x - V_y) - (V_{out} - V_{in}))C_f \tag{9d}$$

Solving the above equations we get:

$$V_x = V_z = \frac{2V_{out} + 3V_{in}}{4} \tag{10a}$$

$$V_y = \frac{V_{in}}{2} \tag{10b}$$

Therefore,

$$I_{load} = I_{out} = q_{out} f_{sw} = 2q f_{sw} = 2(2V_{in} - V_x)C_f f_{sw} = 2\left(\frac{5V_{in}}{4} - \frac{V_{out}}{2}\right) C_f f_{sw}$$

$$\implies I_{out} = \left(\frac{5V_{in}}{2} - V_{out}\right) C_f f_{sw} \tag{11}$$

Hence,

$$R_{OUT_{prop}} = \frac{1}{C_f f_{sw}} \tag{12}$$

B. Conventional series-parallel 5/2 topology

Referring to Fig.2, for phase Φ_1 let us denote the common node voltage of the capacitors C_{1a} and C_{2a} (which is same as that of C_{1b} and C_{2b} by symmetry) as V_x. Additionally, for phase Φ_2 let us denote the common node voltage of the capacitors C_{2a} and C_{2b} as V_y.

Now, using charge-balance for each of the capacitors C_{1a}, C_{2a}, C_{1b} and C_{2b} in the two phases we get:

$$q = (V_{in} - (V_{out} - V_x))C_f \tag{13a}$$

$$q = ((V_{in} - V_y) - (V_x - V_{in}))C_f \tag{13b}$$

$$q = (V_{in} - (V_{out} - V_x))C_f \tag{13c}$$

$$q = (V_y - (V_x - V_{in}))C_f \tag{13d}$$

Solving the above equations we get:

$$V_x = \frac{2V_{out} + V_{in}}{4} \tag{14a}$$

$$V_y = \frac{V_{in}}{2} \tag{14b}$$

Therefore,

$$I_{load} = I_{out} = q_{out} f_{sw} = 2q f_{sw} = 2(V_{in} - V_{out} + V_x)C_f f_{sw} = 2\left(\frac{5V_{in}}{4} - \frac{V_{out}}{2}\right) C_f f_{sw}$$

$$\implies I_{out} = \left(\frac{5V_{in}}{2} - V_{out}\right) C_f f_{sw} \tag{15}$$

Hence,

$$R_{OUT_{conv}} = \frac{1}{C_f f_{sw}} \tag{16}$$

Therefore, it is observed that both the topologies offer the same output impedance in the 5/2 mode (in the slow-switching limit (SSL)).

Acknowledgment

The authors would like to thank ST Microelectronics and Andreia Cathelin for chip fabrication.

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TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS WORKS

Design	**[6]**	**[8]**	**[5]**	**This work**
Technology	130nm Bulk	32nm Bulk	45nm SOI	28nm FDSOI
Topology	Step-up 2/1	Step-up 2/1	Step-up 2/1	Reconfigurable Step-up: 5/2, 2/1, 3/2
Capacitor	MIM	Metal finger	Deep Trench	MOS and MOM
Interleaved phases	**16**	**32**	**1**	**4**
Cout	**400 pF**	**0**	**Yes**	**300 pF**
Area (with C_{load})	2.25 mm^2	0.0067 mm^2	0.0012 mm^2	0.114 mm^2
V_{in}	1-1.2V	1-1.2V	1V	1V
V_{out} (@V_{in}=1V)	1.8V	1.3 - 2V	1.6 - 2V	1.2 - 2.4V
η_{peak} (@V_{in}=1V)	82% @P_{out}=1.5 mW	64% @P_{out}=2.9 mW	90% @P_{out}=2.3 mW	**88%** (2/1 mode) @P_{out} = 0.56 mW
Power density @ η_{peak}	0.67 mW/mm^2	0.43 W/mm^2	1.9 W/mm^2	4.9 mW/mm^2
I_{load}(max.) (@V_{in}=1V)	1.5 mA @V_{out}=1.8V, η = 81%	6.8 mA @V_{out}=1.4V, η = 56%	4.8 mA @V_{out}=1.6V, η = 77%	1 mA (2/1 mode) @V_{out} = 1.73V, η = 83%

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