InGaAs/InAs heterojunction vertical nanowire tunnel FETs fabricated by a top-down approach

InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs Fabricated by a Top-down Approach

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Abstract

We demonstrate for the first time InGaAs/InAs heterojunction single nanowire (NW) vertical tunnel FETs fabricated by a top-down approach. Using a novel III-V dry etch process and gate-source isolation method, we have fabricated 50 nm diameter NW TFETs with a channel length of 60 nm and EOT=1.2 nm. Thanks to the insertion of an InAs notch, high source doping, high-aspect ratio nanowire geometry and scaled gate oxide, an average subthreshold swing (S) of 79 mV/dec at V_{ds}= 0.3 V is obtained over 2 decades of current. On the same device, I_{on}= 0.27 μA/μm is extracted at V_{dd}= 0.3 V with a fixed I_{off}= 100 pA/μm. This is the highest ON current demonstrated at this OFF current level in NW TFETs containing III-V materials.

Introduction

In light of the increased emphasis on energy efficiency in electronics, the tunnel FET (TFET) has become attractive due to its potential for low voltage operation [1]. In TFETs, InGaAs-based heterojunctions promise a combination of steep slope, high ON-current due to the reduced tunnel barrier height [2], and a well passivated surface. To enable continued scaling, a nanowire (NW) transistor geometry with wrapped-around gate is highly favorable due to the strong charge control and its robustness to short-channel effects [3]. To date, vertical NW TFETs with III-V materials have only been demonstrated through bottom-up techniques with complex manufacturing issues [4-8]. In this work, for the first time, we demonstrate InGaAs/InAs heterojunction vertical NW TFETs fabricated via a more manufacturing relevant top-down approach. Devices with a diameter (D) of 50 nm and EOT= 1.2 nm exhibit I_{on}= 0.27 μA/μm at a fixed I_{off}= 100 pA/μm, and V_{dd}= 0.3 V. This is the highest ON current demonstrated at this OFF current among NW TFETs based on III-V materials.

Fabrication Process

Fig. 1(a) shows a schematic view of the transistor fabricated in this work. The starting heterostructure, grown by MBE on an InP wafer, is similar to that in [2]. The tunneling junction consists of a p^+-i $In_{0.53}Ga_{0.47}As$ heterostructure in which a 2 nm i-InAs/8 nm i-$In_{0.7}Ga_{0.3}As$ "notch" has been inserted to reduce the tunnel barrier height and yield steeper subthreshold characteristics and high ON current [2]. The p^+ source and n^+ drain have a nominal 10^{20} cm^{-3} C and 6×10^{19} cm^{-3} Si doping, respectively. In Fig. 1(b), the energy band diagram along the nanowire is simulated with *Nextnano3* by solving Schrodinger-Poisson self-consistently in a double-gate geometry (V_{ds}=0 V, V_{gs}=0.5 V). The efficacy of the InAs/$In_{0.7}Ga_{0.3}As$ notch to lower the tunnel barrier is evident [2].

The process flow is described in Fig. 2. We leverage process and etching technologies used in our previous work [9]. One major change is an improved RIE technology [10] to define the NW. Fig. 3 shows a comparison of D= 60 nm InGaAs NW etched in [9] and in this work. By increasing the substrate temperature during etch and optimizing the etching conditions, we are able to realize more vertical and smooth sidewalls. This improvement ensures tighter control of the NW diameter and yields better scalability. An exponent of the capabilities of this technology is shown in Fig. 4 which features a D=15 nm scale InGaAs NW with an aspect ratio greater than 15.

After NW formation, we introduce a spin-on glass (SOG) planarization and etch back step. This forms a 50 nm SOG layer that covers the bottom p^+ source on which the gate stack is deposited. In this way, we reduce the source-to-gate leakage current that affected our previous NW-MOSFETs [9], and are able to scale the gate dielectric thickness. Our process proceeds with a digital etch [11] to smooth the NW sidewalls and reduce its diameter to 50 nm. 2.5 nm ALD Al_2O_3 (EOT=1.2 nm) and W metal are deposited as gate stack. A 30 min 350°C forming gas anneal is performed. Mo is sputtered as contact metal to both p^+ source and n^+ drain. All devices have a final diameter in the intrinsic region of 50 nm and a channel length of 60 nm given by the undoped InAs/InGaAs layer thickness.

Results and Discussion

Fig. 5 shows subthreshold characteristics of one of the best performing single-NW TFETs. A subthreshold swing of 75 mV/dec averaged over I_d from 10^{-9} to 10^{-7} A/μm is obtained at V_{ds}= 0.3 V. ON current of 0.27 μA/μm is extracted with I_{off}= 100 pA/μm and V_{dd}= 0.3 V (V_{ds}=0.3 V, ΔV_{gs}=0.3 V). Interestingly, S slightly improves at higher V_{ds} [4]. The ON/OFF current ratio exceeds 10^5 in this device. The gate leakage current is below 10^{-12} A/μm in the subthreshold regime. The drain current fluctuations are attributed to the single NW nature of the device [4]. As a result, we report average values for the figures of merit. Hysteretical behavior is observed in the subthreshold characteristics. Measurements in a narrower V_{gs} range from -0.2 to 0 V yield S=79 mV/dec when averaging both sweeping directions.

The transfer characteristics (g_m obtained after smoothing due to current fluctuations) at V_{ds}= 0.3 V are shown in Fig. 6. A peak g_m value of 8 μS/μm is obtained. The output characteristics of

the same device are shown in Fig. 7. Triode-like characteristics are observed [5] with a typical low V_{ds} super-linear behavior characteristics of TFETs [12]. Fig. 8 shows the output characteristics in a semilog scale including the reverse regime. Clear negative differential resistance (NDR) is observed for $V_{ds}<0$ and high V_{gs}, confirming the tunneling nature of the device operation in the ON regime. At V_{gs}=0.8 V, we observe a peak-to-valley ratio in I_d of 6.2. This is the highest value reported at room temperature in III-V NW TFETs.

Across the sample a spread of device characteristics is observed. Fig. 9 presents subthreshold characteristics of three different single-NW TFETs including the one shown in Figs. 5-8 (black curve) at V_{ds} = 0.3 V. The device with the most positive V_t shows the steepest subthreshold regime. Output characteristics of these devices in an identical scale are presented in Fig. 10. Devices with positive V_t show triode-like characteristics but devices with negative V_t exhibit saturating behavior and significantly more current. While low-V_{ds} super-linear behavior is observed at all V_{gs} values in devices with the most positive V_t, devices with more negative V_t only show super-linear onset at high V_{gs}. At low V_{gs}, MOSFET-like turn-on with V_{ds} is observed. The reasons for the wide distribution of device characteristics are not clear at this moment, but the high sensitivity of TFET characteristics to small geometrical variations is likely a contributing factor.

To further understand the physics of device operation, temperature (T) dependent measurements on another device (with relatively negative V_t) are performed. Fig. 11 shows the I_d-V_{ds} characteristics at V_{gs}= 0.5 V and different T in a semilog scale. NDR is clearly seen at all T in the reverse regime. I_d in the low $V_{ds}<0$ region shows little T dependence, confirming direct band-to-band tunneling (BTBT) current conduction. In the positive V_{ds} region, I_d increases slightly with T, which can be attributed to bandgap reduction with increasing T [13].

In Fig. 12, subthreshold characteristics at different T and V_{ds} =0.05 V are shown. A T-independent leakage current floor below pA/um range is reached, a unique feature of the NW geometry not seen in planar TFETs [13]. Another observation in Fig. 12 is the sharp saturation of I_d at high V_{gs}, which could be due to high interface states (D_{it}) density inside InGaAs conduction band or the depletion of p+ source in the overlapping region with the gate. The subthreshold current is very sensitive to T, which is not expected from a pure BTBT conduction mechanism. This suggests that a thermal process is involved. The average S at V_{ds}=0.05 V is shown as a function of T in Fig. 13, indicating that ideal behavior is never reached. The Arrhenius plot [ln ($I_d/T^{3/2}$) vs. (1/kT)] at several V_{gs} in the subhtreshold regime is shown in Fig. 14. As observed in Fig. 15, the extracted thermal barrier height ($q\Phi_B$) from the Arrhenius plot is linearly dependent on V_{gs}. T-dependent gate efficiency due to interface states (D_{it}) alone is unlikely to be the root cause as a different T signature due to D_{it} is observed on MOSFETs on similarly etched InGaAs surfaces [14, 15]. A Poole-Frenkel (PF) mechanism described in [13] involving field-enhanced thermal excitation of carriers from trapped states in the bandgap seems inconsistent with the linear dependence of $q\Phi_B$ on V_{gs}.. A possible explanation is that the subthreshold current is bottlenecked by a thermal-assisted tunneling process of electrons from the valence band of the p+ source into the lowest states available in the conduction band at the InAs notch. Simulations of the energy band diagram at different V_{gs} in Fig. 16 allow us to estimate the thermal energy ΔE between the bottom of the InAs notch and the Fermi level at the source $E_{F,S.}$ that is required for this process. The inset confirms a linear relationship between V_{gs} and ΔE with values that are broadly consistent with measurements. Further analysis is needed to fully identify the responsible mechanism.

Fig. 17 benchmarks I_{on} vs. I_{off} among published vertical NW TFETs based on III-V materials at V_{dd}= 0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V). Compared to other vertical III-V NW TFETs, our devices exhibit an excellent combination of steep slope and ON current, delivering high I_{on} at low I_{off}. This is testimony to the increased flexibility and precision heterostructure growth that is afforded by a top-down fabrication approach.

Conclusions

InGaAs/InAs heterojunction NW TFETs have been fabricated via a top-down approach for the first time. With improved InGaAs RIE technology and a thin SOG layer isolating source from gate, we have been able to obtain near vertical-sidewall NWs and scale the EOT to 1.2 nm. An average S of 79 mV/dec at V_{ds}=0.3 V is obtained over 2 decades of current in our best performing devices. I_{on}= 0.27 μA/μm is extracted at V_{dd}=0.3 V and a fixed I_{off}=100 pA/μm. This demonstrates an excellent combination of steep slope and ON current compared to other NW TFETs with III-V materials.

Acknowledgement

Research funded in part by NSF E3S STC (Award #0939514). Devices fabricated at MIT's Microsystems Technology Laboratories and Scanning Electron Beam Laboratory. The authors thank T. Yu, J. Lin, W. Lu and W. Chern for valuable discussions.

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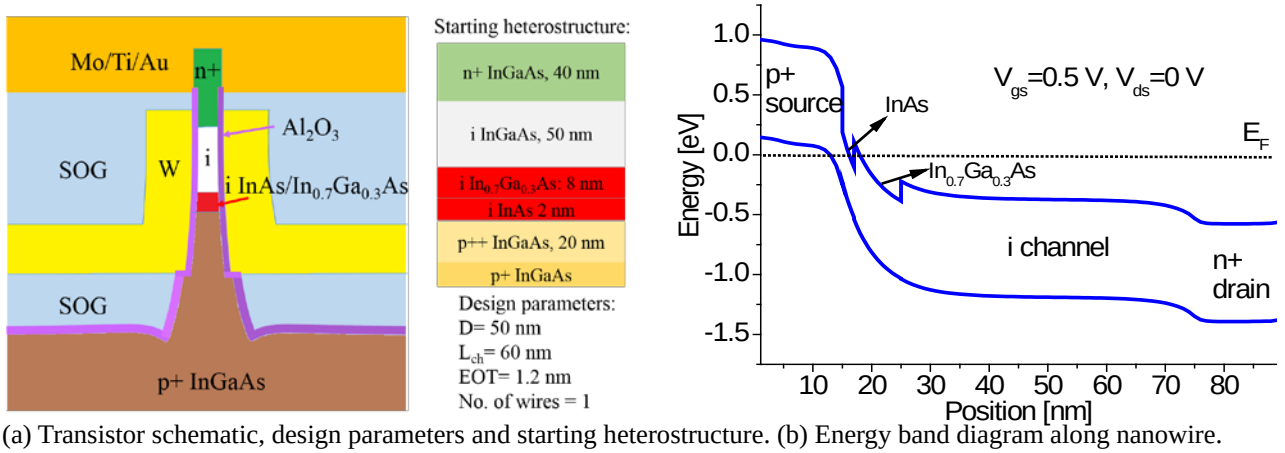

Fig. 1 (a) Transistor schematic, design parameters and starting heterostructure. (b) Energy band diagram along nanowire.

- Nanowire formation by dry etch
- ALD 4 nm Al_2O_3 as protection
- Planarization and etch back to isolate gate metal from p^+ source
- Digital etch
- ALD 2.5 nm Al_2O_3 gate dielectric
- Sputter 40 nm W gate metal
- 30 min forming gas anneal at 350°C
- Gate/top electrode isolation by planarization and etch back (2 times)
- Contact via opening by dry etch
- Sputter Mo as contact metal and S/G/D pad formation

Fig. 2 Process flow for InGaAs/InAs heterojunction vertical nanowire (NW) tunnel TFETs.

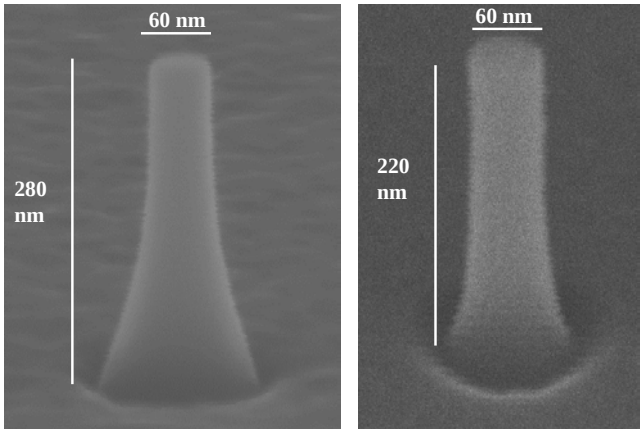

Fig. 3 D= 60 nm InGaAs NW used in NW MOSFETs [9] (left) and this work (right).

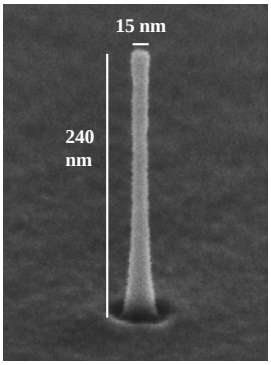

Fig. 4 D=15 nm InGaAs nanowire defined by optimized RIE technique.

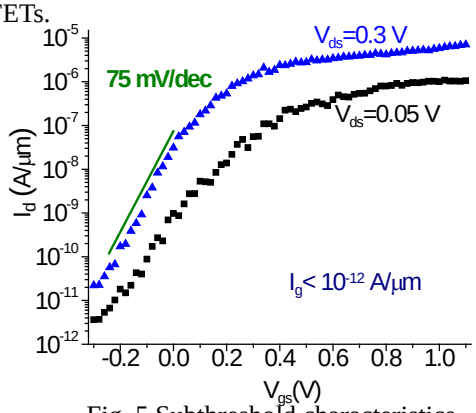

Fig. 5 Subthreshold characteristics of a D= 50 nm single-NW TFET.

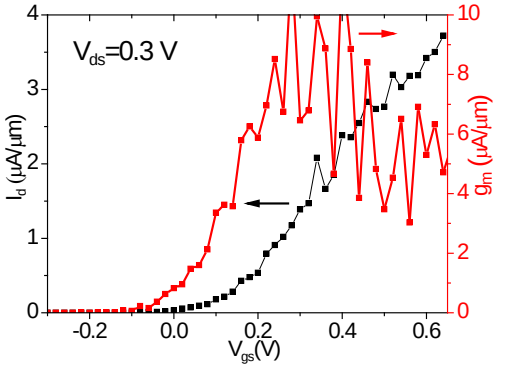

Fig. 6 Transfer characteristics at V_{ds}=0.3 V of the device shown in Fig. 5.

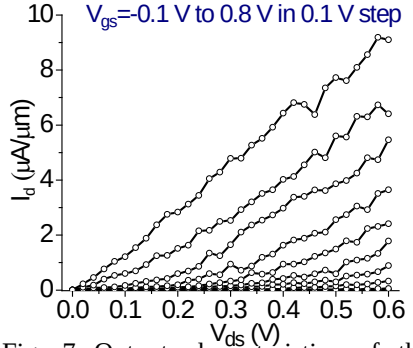

Fig. 7 Output characteristics of the device shown in Fig. 5.

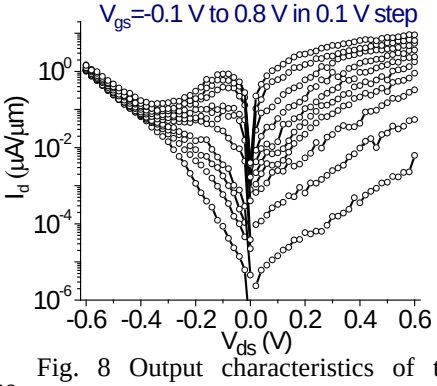

Fig. 8 Output characteristics of the device shown in Fig. 5 in semilog scale for positive and negative V_{ds}.

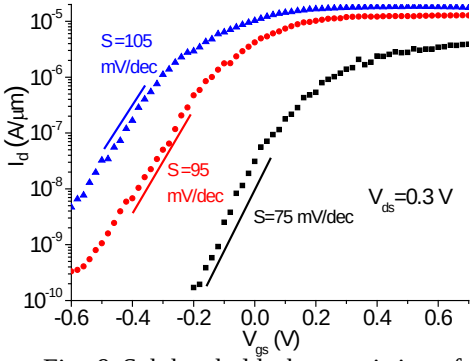

Fig. 9 Subthreshold characteristics of three single-NW TFETs at V_{ds}=0.3 V indicating device-to-device variability.

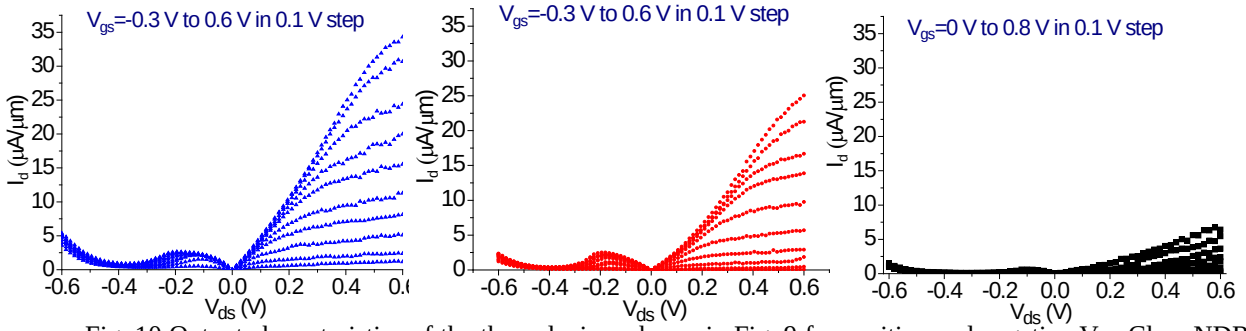

Fig. 10 Output characteristics of the three devices shown in Fig. 9 for positive and negative V_{ds}. Clear NDR is observed in all 3 devices.

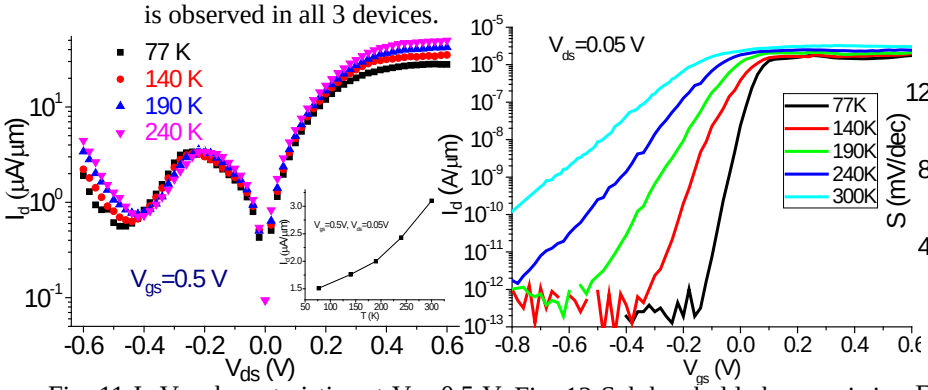

Fig. 11 I_d-V_{ds} characteristics at V_{gs}= 0.5 V of a single-NW TFET in semilog scale at different temperatures from 77 to 240 K. Inset: I_d vs. T at V_{ds}=0.05 V, V_{gs}= 0.5 V.

Fig. 12 Subthreshold characteristics of the device shown in Fig. 11 at V_{ds}=0.05 V and T = 77 to 300 K.

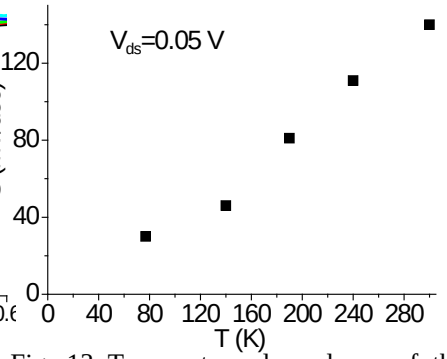

Fig. 13 Temperature dependence of the average S at V_{ds}=0.05 V of the device shown in Figs. 11 and 12.

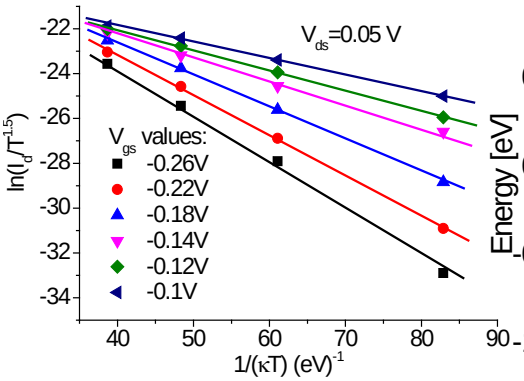

Fig. 14 Arrhenius plot of the subthreshold current at various V_{gs} values versus inverse thermal energy. The slope of the linear relationship is the thermal barrier height.

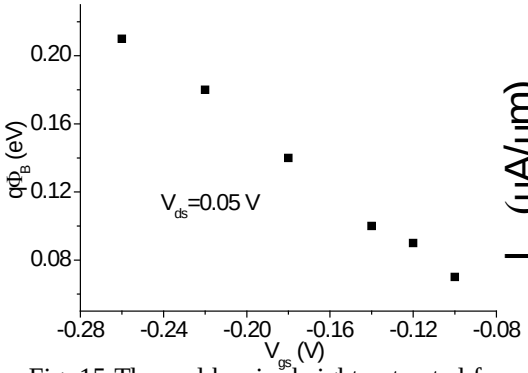

Fig. 15 Thermal barrier height extracted from the slopes in Fig. 14 as a function of V_{gs}.

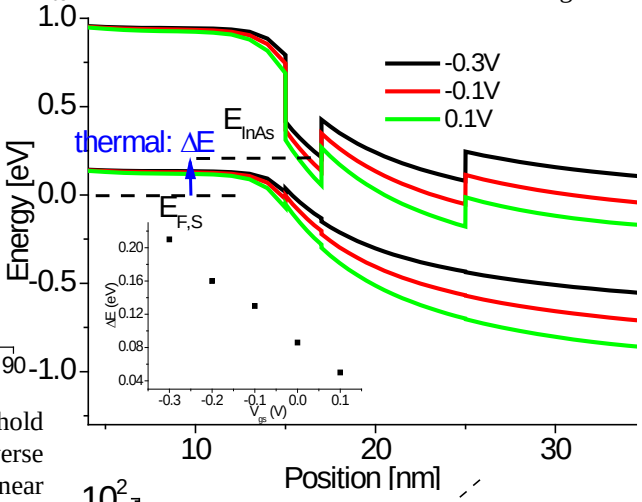

Fig. 16 Energy band diagram at V_{ds}=0 V and various V_{gs}. Thermal energy is needed for subthreshold tunneling between the source Fermi level and the lowest conduction band states at the InAs notch. Inset: thermal barrier ΔE varies linearly with V_{gs}.

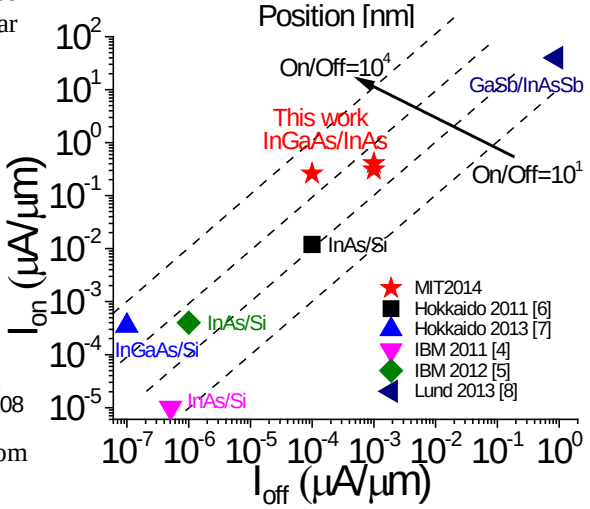

Fig. 17 I_{on} vs. I_{off} at V_{dd}=0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V) for recently published vertical NW TFETs containing III-V materials. All devices but the present ones are fabricated through bottom-up techniques.