Circuits and Protocols for Low Duty Cycle Wireless Systems

by

Arun Paidimarri

B.Tech., Indian Institute of Technology Bombay (2009)
S.M., Massachusetts Institute of Technology (2011)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science
at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2016

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Abstract

IoT devices are helping improve efficiency and expanding capabilities in an increasing number of applications including industrial, home and personal fitness. Device lifetimes are still a concern, and improved energy efficiency is needed. Additionally, aggressive duty cycling is needed to operate these IoT devices in severely energy-constrained applications.

Wireless communication, which consumes a large fraction of the power in these devices, is the primary focus of this thesis. We present circuit (active RF, leakage management and timing) and protocol (medium access and coding) techniques for total power minimization in low duty cycle systems.

First, we present a Bluetooth Low Energy (BLE) transmitter optimized for low duty cycles. It maintains a high efficiency >40% while delivering +10dBm. At the same time, aggressive power gating brings the leakage down to <400pW, giving an on/off power ratio of 7.6×10^7.

Second, we look at protocols for low duty cycle wireless communication. The tradeoffs between network capacity and sensor node power consumption are considered and a fully asynchronous protocol is proposed. Additionally, we look at two coding techniques, Digital Network Coding (DNC) and Spinal coding, to enhance the intrinsic range of communication.

Finally, for systems requiring accurate clocks, the standard is to use crystal oscillators. However, in order to reduce cost and board area, we propose a fully-integrated RC oscillator architecture that achieves high stability while maintaining low power.

Overall, the techniques explored in this thesis aim to expand operation of IoT devices to ever more energy constrained situations and with increased lifetimes.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Joseph F. and Nancy P. Keithley Professor of Electrical Engineering
Acknowledgments

My life so far has been characterized by tremendous love, privilege, support, inspiration, friendship and help. As I finish my PhD, this is a great opportunity to reflect back, and thank everyone that has had a positive impact on my life, especially the past 6 years at MIT.

Firstly, I would like to thank Prof. Anantha Chandrakasan, who has been an excellent adviser. He has been super supportive to me, and has always looked at my best interests, and has pushed me to aim high and work hard. As I think about the range of things on his plate, I find it so inspiring to see how he always responds to emails so quickly, and always finds the time for meetings. It is also so very inspiring to see his excitement for new ideas, and research in such a wide range of topics! I can only aspire to be as effective with my time as he is. It has been a great fortune of mine to have gotten this opportunity to be his student!

I would like to thank Prof. Dave Perreault and Prof. Ruonan Han who have been the best thesis committee I could have asked for. They have been accommodating with schedules, have always been very encouraging, and discussions in the meetings have helped refine the thesis and its presentation.

My work has been funded by the Interconnect Focus Center (IFC), Shell, Texas Instruments. And chip fabrication has been kindly provided by TSMC’s university shuttle program and Texas Instruments.

It has been a privilege to work with some awesome collaborators. Many of the ideas presented in this thesis were a result of discussions. The whole process has been rewarding, and I would love to be able to continue working with you all. Phillip Nadeau and I started together in Ananthagroup, doing wireless systems, and it has been a great privilege to work closely on a few projects, and to discuss regularly various aspects of our projects, or any topic whatsoever. I am amazed at his attention to detail, and focus on the fundamental understanding. Patrick Mercier, was the best mentor I could have asked for during the first few years at MIT. Recently, it was a great experience working on the book chapter with him.

Working with Georgios Angelopoulos and Prof. Muriel Médard on the Digital Network Coding project was a great experience. The elaborate day-long packet error rate experiments in Candlewood were a great learning experience. The work on protocols and Spinal codes was in collaboration with Prof. Hari Balakrishnan and Peter Iannucci. I enjoyed our discussions.

My internships at Texas Instruments were a great learning experience. I would like to thank Gangadhar Burra for allowing such freedom in the work, Danielle Griffith for great discussions and ideas, and Alice Wang in particular for helping get everything done so quickly during the three months, whether it was meeting with experts, arranging tapeout, regularly scoping out the project goals and reevaluating them.

In the Shell/TI microsensor project, it was nice to have the biweekly meetings with Xiaoxue Wang, Frank Yaul and Nathan Ickes and to get feedback from Brian.
de Vuijst, George Zolkiewski, Terry Sculley, Chris Link and others. It has been an honor to have been able to work with Nathan on multiple occasions through the years, including the IFC demos and the Shell project. It is inspiring to see the scale of his projects, and to see the final execution of it. I had a lot of fun working with Tiantian Han, Elizabeth Schell and Nathan on vibration energy harvesting. Later, extending the work with Dennis Buss, Mohammed Araghchini and Sheng Zhao was good fun!

Ananthagroup has been where I have spent an enormous amount of time, and it wouldn’t have been as much fun if not for the awesomeness of the people. All students past and present have been amazing, and it is inspiring to see the great work. Everyday has been a learning experience, and given the wide range of works there is always more to learn! In particular, I would like to thank Mehul and Gilad for the great work on the group wiki and shared resources and to everyone else for all the contributions over the years. I would also thank Chiraag, Masood, Mehul, Nachiket, Phil and Saurav for all the long and late discussions on research and otherwise. Ananthagroup sports clubs have been intermittent, but a lot of fun. The procrastination circle and lunch outings have been much more regular, and have resulted in great discussions. And to Margaret, who has always been perfect with helping us figure out all administrative stuff, ordering parts, getting reimbursements, setting up meetings, reserving spaces.

All of MTL, EECS and MIT in general, including the staff, students, professors who help make thee environment so very collegial. In particular, Janet, Alicia in the graduate office and Debb, Valerie in MTL are always smiling and supportive. The classes that I have taken over the years have been wonderful, and it is inspiring to see the confidence, depth and breadth of the teaching staff!

I enjoyed my time as a teaching assistant for 6.374, and working with Duke Xanthopoulos. His perspectives and experience helped add great insights in the lectures. Teaching the course also greatly helped my own understanding of digital circuits!

Outside of work, I have been very lucky to have a great friend circle. It has been a lot of fun hanging out, eating out, watching movies, taking road trips, hiking, celebrating birthdays etc. It is always nice to have such company, both in good and hard times. I should definitely mention the badminton club and in particular, Tapovan, for all the great games! I have been lucky to have great roommates over the years, in particular, Swapnil, Tapovan, Nachiket and Sagar! Also, a special mention to the CS101 group for all the long conversations about nothing and everything.

And, of course, family! My brother, Kashyap, has been one of my greatest inspirations in life. I would like to acknowledge the help and support from him and my sister-in-law Kuntal. My niece Krishala has been a bundle of joy for everyone in the family ;). My parents, PSN Murthy and Rama Devi, are the greatest ever. They have always encouraged my brother and I to follow our dreams, always supported every activity we have taken up, provided us with everything, and have sacrificed greatly for our cause. They always know when there is a problem, and always know exactly how to cheer me up ;). This thesis is for them!
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Chapter 1

Low Duty Cycle Wireless Systems - Challenges and Opportunities

With the convergence of ever-improving wireless technologies and energy management circuits, Internet-of-things (IoT) devices for home, industrial and environmental monitoring have brought significant improvements to lifestyle, safety and efficiency [1, 2]. Home automation devices such as smart thermostats [3], energy meters [4], and smart-lighting [5] greatly improve the energy efficiency of buildings. Personal fitness devices help users lead healthier lifestyles [6]. Monitoring of industrial environments can help improve safety as well as efficiency.

Some of these IoT devices such as smart thermostats have wired connections to power, and can have a wider set of capabilities. Among battery operated devices, some devices such as personal fitness trackers are typically built for lifetimes of a few days. Quick response times here are a priority. In these applications, wireless communication has a high activity, and thus, active power optimization of the wireless is important.

On the other hand, some other devices, such as in industrial monitoring, are at the extreme low end of energy budgets. These devices might monitor, for example, presence of toxic or combustible gases, or structural stability of a building, or health of
CHAPTER 1. LOW DUTY CYCLE WIRELESS SYSTEMS

Chemical Vapor Detection
- “Fugitive emissions”
- VOCs, H₂S

Mechanical Monitoring
- “Balance of plant” equipment
- >5k pieces per plant

Figure 1-1: Example industrial applications that require ultra-long lifetimes, but also operate at low duty cycles.

rotating equipment in a factory. Some of these industrial applications are illustrated in Fig. 1-1. In many of such cases, it might be infeasible or prohibitively expensive to send wired power, necessitating battery or energy harvested operation. Lifetimes of the order of tens of years are needed in order for them to be useful and not require regular replacement of batteries. This thesis focuses on these extreme use cases.

Depending on the system and configuration, wireless communication can dominate the energy budgets, for example in [7, 8]. Or, depending on the amount of local processing, the power consumed by wireless might vary from being dominant at some times, to being negligible at other times. For example, in [9], the amount of local processing is varied depending on the amount of available power. This can vary the transmit data rates from 200kbps down to a few kbps while trading off data fidelity. Overall, wireless communication is a key component of an IoT device from an energy perspective and improved efficiency can greatly enhance device performance. In addition, the radios are typically the highest peak power consumers [7, 9, 10], presenting challenges for power management and batteries [11]. In this thesis, we aim to improve energy and power efficiency of the wireless communication.

Most of the long lifetime, extreme use cases described above also have an associ-
ated characteristic of low activity or low duty cycles. For example, the wear and tear of rotating equipment is a process with long time constants of the order of hours or days, and thus, updates can be infrequent. Some applications, such as gas sensors, require quick response time once detected, but in normal operation, they only need to send a few updates per day.

1.1 Challenges and Opportunities

In order to find challenges and opportunities, we start by modeling the average power consumption of a duty cycled wireless link, expressed below as:

\[
P_{\text{avg}} = \alpha_{\text{essential}} \cdot P_{\text{active}} + \alpha_{\text{overhead}} \cdot P_{\text{active}} + (1 - \alpha_{\text{essential}} - \alpha_{\text{overhead}}) \cdot P_{\text{standby}} \quad (1.1)
\]

\[
= \frac{t_{\text{essential}} P_{\text{active}}}{t_{\text{interval}}} + \frac{t_{\text{overhead}} P_{\text{active}}}{t_{\text{interval}}} + \frac{(t_{\text{interval}} - t_{\text{essential}} - t_{\text{overhead}}) P_{\text{standby}}}{t_{\text{interval}}} \quad (1.2)
\]

where \( \alpha_{\text{essential}} \) is the intrinsic duty cycle of the application, and captures the essential packets of communication. \( \alpha_{\text{overhead}} \) captures the contribution of overhead in communication protocols that lead to extraneous packets, which in turn lead to increase in power consumption. The duration \( t_{\text{interval}} \) is the time between consecutive transmission of the essential packets, which are each of duration \( t_{\text{essential}} \). \( t_{\text{overhead}} \) is the duration for which the radios are turned on for protocol overhead reasons. This overhead duration can be a function of the \( t_{\text{interval}} \) itself.

At low duty cycles, \( t_{\text{interval}} \rightarrow \infty \), and the average power can be written as:

\[
\lim_{t_{\text{interval}} \rightarrow \infty} P_{\text{avg}} \approx P_{\text{standby}} + \lim_{t_{\text{interval}} \rightarrow \infty} (\alpha_{\text{overhead}} \cdot P_{\text{active}}) \quad (1.3)
\]

where the limit of the second term is a function of the protocol.

Equation 1.2 is plotted for varying \( t_{\text{interval}} \) in Fig. 1-2 for a typical +10dBm Bluetooth Low Energy radio \( (t_{\text{essential}} \text{ of } 200\mu s) \) such as [12]. This chip consumes 75mW in active and 3\( \mu \)W in standby, and operates with a 500ppm accurate sleep-mode timer.
Figure 1-2: Performance of existing BLE radios at low duty cycles, highlighting the various opportunities for power reduction.

The following observations can be made:

1. At low duty cycles (or high values of $t_{\text{interval}}$), the power is limited by protocol overhead. The power consumption tapers off at packet intervals of only ten seconds. The system shows no benefit at low duty cycles. This implies that with an optimized protocol with minimal overhead, the protocol component of the average power can be significantly reduced. Assuming the standby power is low, significant overall power reduction could be obtained.

2. At high duty cycles (or low values of $t_{\text{interval}}$), the performance is dependent on active RF power consumption. Improvements in RF circuits can bring the knee of the curve further left, and even more strongly motivate protocol optimizations.

3. The ultimate limit to power consumption is the standby power, $P_{\text{standby}}$, as
indicated in Eqn. 1.3. This is comprised of leakage power of all the circuits, as well as always-on circuits. One of the key always-on circuit is the timer, whose accuracy requirements are set by the protocol. Reduction in leakage power as well as relaxed timing requirements from protocol choices can significantly bring down $P_{\text{standby}}$.

4. These are in addition to previous works which emphasize the importance of low startup energy for RF circuits [13, 14], especially for the short-packet scenarios in IoT devices. The startup energy is typically dominated by the PLL startup and appears as an overhead through increase in $t_{\text{essential}}$.

Thus, we see that the key challenges for power reduction in wireless systems at low duty cycles are in the joint optimization of protocols, RF circuits, leakage management and sleep-mode timing. In this thesis, we address the following questions:

1. What is the minimum overhead that can be achieved for wireless protocols operating at low duty cycles? For example, can a sensor operate in a (predominantly) transmit-only mode where it only transmits its data when it needs to and is in sleep at all other times? What are the tradeoffs of such a design?

2. Can we design leakage management circuits that present no overhead to active operation? What is the highest on/off power ratio achievable while maintaining high efficiency?

3. Can low-voltage RF circuits be designed to co-optimize on-efficiency and off-state leakage power?

4. What are the tradeoffs for sleep-mode timing generation in terms of frequency, power consumption and accuracy? For example, are crystal oscillators necessary?

5. How do coding schemes interact with low-duty cycle communications? How can an asymmetric energy budget be exploited in the design of link budgets?
6. Overall, can the low duty cycling be translated to sub-nW average power while maintaining high performance?

These questions motivate the work explored in this thesis. The rest of this chapter summarizes the main ideas along with providing context for each of these. The following chapters expand on these ideas in more detail.

1.2 Thesis Outline and Contributions

Table 1.1 summarizes the main contributions in this thesis, including active RF design, leakage management, protocol choices, sleep-mode timing as well as coding techniques.

1.2.1 Low Leakage RF Transmitter and PLL

As discussed above, low leakage in the RF can help reduce average power at low duty cycles. This, in turn, would make energy harvested operation more robust, and enable very long lifetimes for the deployed IoT devices. Previous work on ultra-low leakage wireless [7, 15, 16] have looked at short range communication of a few meters for medical applications, with low output power levels (below −10dBm). In this work, we consider longer range communication with output power around +10dBm, and consider the joint problem of achieving high efficiency at the higher output powers while simultaneously minimizing leakage.
Table 1.1: Summary of contributions in this thesis

<table>
<thead>
<tr>
<th>Theme</th>
<th>Regime of Interest</th>
<th>Key Contributions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active RF</td>
<td>Peak power, communication range, knee of average power</td>
<td>Low voltage operation for reduced switching power, including a low voltage PLL design, a high efficiency +10dBm PA and low-voltage assist circuits with a voltage doubler</td>
</tr>
<tr>
<td></td>
<td>versus duty cycle</td>
<td></td>
</tr>
<tr>
<td>Leakage</td>
<td>Standby power, floor of average power</td>
<td>Extensive power gating, negative gate biasing, efficient negative voltage charge pumps and low leakage logic design techniques to maximize on/off ratio of RF circuits</td>
</tr>
<tr>
<td>Protocols</td>
<td>Average power floor for low duty cycles, network capacity</td>
<td>Analysis of existing protocols and their modes for power and network capacity, a predominantly transmit-only protocol that minimizes protocol overhead</td>
</tr>
<tr>
<td>Timing</td>
<td>Standby power floor, timing accuracy and receiver guard times for synchronous protocols</td>
<td>Gate-leakage based oscillator for asynchronous protocols, and an RC oscillator with comparator offset compensation as crystal oscillator replacements for synchronous protocols</td>
</tr>
<tr>
<td>Coding</td>
<td>Communication range, peak power reduction, asymmetric energy budget</td>
<td>Digital Network Coding as a packet erasure code, Spinal coding for rateless operation, low-power encoder implementations along with digital basebands</td>
</tr>
</tbody>
</table>
These are addressed in a testchip through the following techniques:

1. Low voltage operation (0.68V) helps reduce active switching power as well as short-circuit power. Digital circuits have long benefited from low-voltage operation where energy per operation is minimized [17]. Analog front-ends [18] as well as RF circuits [19,20] have been shown to operate at low voltage, and some of these techniques are borrowed in this work.

2. The PLL, operating at 2.5GHz, is a significant bottleneck for low voltage operation. A low-voltage PLL is developed with focus on the frequency divider, VCO and charge pump circuits.

3. A voltage doubler charge pump is used to generate a 1.2V rail for powering some circuits that consume low power, but aid the low-voltage operation of other higher power RF circuits (for example, high-Q digitally tunable capacitors).

4. Standby power reduction schemes that minimize RF performance degradation are explored. A negative gate biasing technique is used to strongly cutoff power gating switches, exponentially decreasing leakage currents for the same on-performance [16].

5. A minimum leakage bias point is shown for negative biasing in the presence of gate leakages. Such a biasing schemes is used in the PA to result in leakage reduction without efficiency degradation. Efficient negative voltage charge pumps are demonstrated to enable this.

6. A 10pW gate leakage-based 32Hz oscillator is developed for running the negative voltage charge pump.

The test-chip, manufactured in a 65nm CMOS process has an efficiency of 43.7% while delivering a power of +10.9dBm. It has an off-state leakage of 370pW, for an on/off ratio of 7.6×10^7, showing the feasibility of a high efficiency, low leakage RF
transmitters capable of relatively long distance communication. Chapter 2 describes the detailed chip architecture [21], circuit design and measurements of the transmitter, while Chapter 3 describes the design and measurement results for the PLL [22].

1.2.2 Protocols for Low Duty Cycles

We look at the protocol aspects of low duty cycle wireless communication. A full wireless communication protocol includes transmission, reception of both data and acknowledgments, and timing synchronization. The average power in Eqn. 1.3 motivates the need for low overhead protocols, allowing the average power to be limited by chip leakage. The key tradeoffs in the protocol are:

1. Timing synchronization is typically required in wireless networks for the base-station to time-division multiplex the various sensor nodes and to avoid collisions. Protocols typically achieve this through periodic beacons. All sensor nodes wake up to receive these beacons and resynchronize their local clocks. Due to inaccuracies in their clocks, the sensor nodes wake up for a “guard-time” period to ensure reception. This leads to a fixed receiver duty-cycle on the sensor node, dictated by its clock accuracy, and thus prevents it from reaching leakage power levels. The trade-off here is between the power of an accurate clock and the power consumed by the receiver in the guard-time.

2. One approach to overcoming timing synchronization overhead is to employ asynchronous connections in the style of ALOHA [23]. Here, we find that we trade-off network utilization\(^1\) (to avoid collisions of unsynchronized packets) with power consumption.

3. Quality of service and reliability is typically ensured with the use of ACKs and retransmissions, along with the timing synchronization to avoid collisions.

\(^1\)Network utilization is another important metric, and is formulated as the number of nodes supported by the network.
in the first place. However, this comes at the cost of power. We note that some packets could be more important than others (for example “temperature is normal” versus “temperature exceeds 105°C”) and thus, a protocol could provide various grades of reliability and enable tradeoffs with power.

4. Associated with the quality of service is another metric of response time. In beacon-based systems, the response time from sensor to basestation is dictated by the beacon interval. In asynchronous systems, it can be lower, but is dictated by current network conditions including channel path loss and probability of collisions.

Chapter 4 analyzes existing protocols (such as BLE, 802.15.4) and their modes of operation at low duty cycles and discusses how they navigate the above tradeoffs. It also proposes some improvements that achieve minimal protocol overhead through a predominantly transmit-only approach. It results in significant improvement in network utilization in ultra-low duty cycle scenarios.

1.2.3 Oscillators for Protocol Timing

The timer is one of the only always-on blocks, and consumes a large portion of the sleep power [10,12] in various systems. If the protocol allows for low accuracies, pW-level oscillators such as the one developed for the charge pump in the low leakage transmitter above (Sec. 2.4.2 for details) can suffice.

However, in some applications, the protocol is fixed due to compatibility reasons. In some of these protocols, timing synchronization needs to be maintained. When a large number of applications operate at low duty-cycles (such as a heart rate monitoring system with packet transmissions every few seconds), the power of the wireless could be dominated by the timing circuits and the receiver guard-time, as in the example plotted in Fig. 1-2. Optimized high-accuracy timers are thus needed. Though crystal oscillators [24] provide excellent accuracy (better than 500ppm) and
low power consumption (as low as 6nW), in order to avoid the cost and size of these bulky external components, we explore fully-integrated replacements.

Silicon-based resonator integration with CMOS chips have been shown to achieve an excellent $\pm 2$ppm temperature accuracy and only $0.4 \mu$W power [25]. Other approaches have been to explore fully-integrated RC-based oscillator topologies for minimal cost. In Chapter 5, we describe an RC oscillator topology [26]:

1. RC time constants are used to set the period of oscillation, while active circuits like comparators and current sources set the overall performance of the oscillator. We use an offset-cancellation architecture to improve the power consumption versus accuracy tradeoff.

2. When nominally-temperature compensated resistors are used, the measured temperature accuracy of the oscillator is improved $4 \times$ to $25 \times$ to give $\pm 0.18\%$ to $\pm 0.55\%$ variation in $-40^\circ C$ to $+90^\circ C$ range. Most of the residual variation appears to arise from the intrinsic resistor variation.

3. The offset-cancellation scheme also improves the noise performance, with the flicker noise of the comparator getting canceled as well. This improves the long term stability (or Allan deviation) by about $10 \times$ to under $20$ppm for time measurements beyond 0.5 seconds.

1.2.4 Coding Techniques to Enhance Communication Range

In addition to the architecture, circuit and network protocol design aspects discussed so far, certain PHY-layer aspects of communication can greatly influence system performance.

1. Modulation formats are usually of simple, binary type (FSK, OOK, BPSK) since they provide the longest range and simplest modulation circuits, and highest efficiency due to reduced PA-linearity requirements.
2. Data rate, in conjunction with the output power, set the SNR at the receiver of the base-station through the following equation:

\[
P_{\text{IN,RX}} = P_{\text{OUT,TX}} - \text{PathLoss} = -174\text{dB} + 10\log(\text{DataRate}) + \text{NF}_{\text{RX}} + \text{SNR} \\
\therefore \text{SNR} = P_{\text{OUT,TX}} - \text{PathLoss} + 174\text{dB} - 10\log_{10}(\text{DataRate}) - \text{NF}_{\text{RX}}
\]

(1.4)

(1.5)

If the channel is good, the transmitter could reduce its output power. However, at the maximum distance, with the maximum transmit output power, the datarate of the protocol must be set to meet the required \(\text{SNR}_{\text{min}}\) for detection. Different standards choose different nominal datarates as suited for their application. For example, BLE is designed for short ranges (tens of meters) and has a bitrate of 1Mbps while a long-range standard such as Sigfox [27] can communicate over a few kilometers and has data rates as low as 100s of bps.

3. In addition to simply adjusting the datarate, or increasing the output power of the transmitter on the sensor node, communication range can be extended through coding techniques. For example, 802.15.4 [28] uses rate 1/8 spreading codes. This could be advantageous over increasing output power since the corresponding transmitter leakage is lower, making such techniques more attractive for low duty cycles.

Thus, we can enhance range without increasing output power and corresponding chip leakage through the use of coding. Also, since the energy budgets of the sensor node and base-station are asymmetric, coding techniques that take advantage of this with simple encoders and potentially complex decoders can be considered. In this thesis, we look at two new coding techniques, Digital Network Coding (DNC), and Spinal coding.
1.2. THESIS OUTLINE AND CONTRIBUTIONS

Digital Network Coding

DNC is a cross-packet encoding scheme where redundancy is spread across packets. While DNC has been shown to have great benefits to adhoc networks [29], as will be discussed in Chapter 4, star networks are the most energy efficient at low duty cycles. Hence, we consider only the application of DNC in star networks.

In particular, we use DNC to overcome packet losses due to collisions in a congested spectrum, as well as due to channel noise. We find that DNC applied in conjunction with channel codes such as convolutional codes perform well because they complement each other. Chapter 6 describes DNC in detail [30]. It shows the hardware encoder designed to work with a low power -10dBm transmitter. RF measurements demonstrate the SNR improvements of DNC versus, as well as in conjunction with, convolutional coding.

Spinal Coding

A second channel code considered is Spinal codes [31]. Spinal codes use hash functions to spread the input data in the encoded space. They have been shown to approach the Shannon limit in a rateless scheme. We propose to develop a Spinal encoder for use in the context of ultra-low power sensor nodes. For this purpose, we consider simple binary modulation (as opposed to n-QAM and OFDM). At low SNRs, acquiring synchronization is an additional challenge, and so, we explore spreading codes such as in [28]. This synchronization overhead could be significant, especially for short packets in low SNR regimes. Hence, we consider only the fixed-rate versions of the codes to minimize this overhead. Chapter 7 describes this, along with the design of a digital baseband that supports BLE, 802.15.4 along with a Spinal encoder. The optimized spinal encoder design minimizes on-chip memory requirements.
1.3 Summary

We have presented some key challenges for low duty cycle wireless communications, along with some of the opportunities available for power reduction. The key contributions of the thesis can be summarized by Fig. 1-3 and in Table 1.1
Chapter 2

A High Efficiency Low Leakage Bluetooth Low Energy Transmitter

As we saw in Sec. 1.1, at low duty-cycles, leakage power of the system sets the minimum power limit once protocol optimizations are made. Simultaneous RF-mode power optimization helps improve average power at higher duty cycles, also reducing peak current requirements on the energy-delivery subsystems. In this chapter, we present an RF transmitter designed to operate in an extremely low duty-cycle industrial monitoring system with joint optimization of the off-state leakage and on-efficiency. An output power of +10dBm is chosen to extend operation to approximately 100m in industrial environments, while Bluetooth Low Energy (BLE) is chosen as the PHY protocol.

2.1 Background and Related Work

Previous work on RF transmitters has focused primarily on the active performance. Constant-envelope modulations such as OOK, FSK or GFSK (as in BLE) have enabled high efficiency transmitters. For example, [32,33] achieves high efficiency with an FBAR-based LO and an optimized PA-antenna structure. Works such as [12,34]
shows high efficiency Bluetooth architectures with PLL-based frequency references as well as I/Q modulation. Finally, power-hungry I/Q modulators and associated mixers etc. have been replaced with 2-point modulation within the PLL in [35, 36] or with direct modulation of the VCO [37]. In this work, the transmitter includes direct modulation of the VCO and a high-efficiency PA.

Transmitter leakage has been optimized in space-constrained implantable applications such as in [7, 15, 16]. These transmitters radiate low output power $< -10$dBm and have relatively low efficiency ($< 1\%$ because of the low radiation efficiency of the loop-antennas used). However, they show the efficacy of power gating techniques for RF circuits in achieving leakage less than a few nW. Commercial transmitters such as [38] have better efficiency at 5\%, but are limited to a leakage of 50nW. In this work, we look to improve the efficiency-leakage tradeoff.

The $+10$dBm BLE transmitter in this work achieves high on-state efficiency of 43.7\% and an off-state leakage of 370pW for an on/off ratio of $7.6 \times 10^7$. This is achieved through 1) low voltage design (0.68V) for switching power and short-circuit power reduction [20], 2) extensive power gating [16] and 3) a negative-$V_{\text{GS}}$ biasing technique for PA leakage reduction without affecting on-performance. The following sections describe the architecture, circuit design and the measurements from a testchip.

Some of these previous works and their key contributions are summarized in Table 2.1.
## 2.1. BACKGROUND AND RELATED WORK

Table 2.1: Summary of previous work and their key contributions

<table>
<thead>
<tr>
<th>Reference</th>
<th>Key Contributions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chee, VLSI '06 [32]</td>
<td>FBAR-based 2 channel transmitter directly connects the tank of an oscillator to the PA input capacitance for a high efficiency transmitter architecture outputting 0.8dBm</td>
</tr>
<tr>
<td>Paidimarri, JSSC '13 [33]</td>
<td>FBAR-based 3-channel transmitter optimized for −10dBm output power. It uses a resonant buffer to resonate the input capacitance of the PA for high efficiency.</td>
</tr>
<tr>
<td>Liu, ISSCC '13 [35]</td>
<td>A multi-standard capable transceiver architecture. It uses a PLL-based two-point modulation scheme in order to avoid the need for I/Q mixers.</td>
</tr>
<tr>
<td>Chakraborty, VLSI '14 [36]</td>
<td>A digital PLL using a Time to Digital Converter (TDC) is used in this work with two point modulation scheme, avoiding I/Q mixers. It includes a DC/DC converter for direct-battery operation.</td>
</tr>
<tr>
<td>Masuch, TMTT '12 [37]</td>
<td>This Bluetooth transmitter demonstrates an approach with direct modulation of the VCO, where the PLL is on open-loop during packet transmission. It demonstrates that the center frequency stays stable for the packet duration.</td>
</tr>
<tr>
<td>Chow, ISSCC '10 [15]</td>
<td>A space-constrained transmitter radiates less than −45dBm in a biomedical implant application. Power gating leads to sub-nW leakage.</td>
</tr>
<tr>
<td>Mercier, JSSC '14 [16]</td>
<td>An inner-ear implantable transmitter is optimized for low leakage below 40pW and low active power below 400µW. Power gating with negative $V_{GS}$ is demonstrated for reduced leakage operation. The transmitter is built in combination with energy-harvesting from the inner-ear for indefinite operation.</td>
</tr>
<tr>
<td>Yu, ISSCC '07 [20]</td>
<td>This 0.65V PLL demonstrates the feasibility of low-voltage RF circuits.</td>
</tr>
</tbody>
</table>
2.2 Architecture of the BLE Transmitter

Fig. 2-1 shows the architecture of the BLE transmitter. The RF signal path includes a 12MHz crystal oscillator (XOSC) which feeds a 1MHz clock to an integer-N PLL. The PLL provides the 2MHz-spaced BLE channels at 2.4GHz. 1Mbps GFSK modulation is applied through direct modulation of the VCO control voltage. The 12MHz crystal frequency is also divided to 6MHz to clock the digital baseband. Here, a 6× oversampled Gaussian FIR filter generates the GFSK data. The digital baseband also includes an SPI interface and BLE packet generation, including CRC, preamble and synchronization word. The VCO output is buffered onto a +10dBm power amplifier. The PA is fully integrated and interfaces to a 50Ω antenna, and the VCO buffering includes a resonant buffer stage. In order to aid low-voltage operation of the chip at 0.68V, the chip includes a voltage doubler charge pump that runs at 3MHz and...
generates a $V_{\text{DOUB}}=1.2\text{V}$ output. Sec. 2.5 describes the operation of the RF circuits in detail.

In the sleep mode, leakage reduction is achieved through power gating of all the blocks, as shown in Fig. 2-1. Leakage reduction of the high-power PA is implemented without efficiency degradation with a negative voltage biasing scheme. The optimal biasing is described in detail in Sec. 2.3. A $-\frac{1}{2}$ charge pump that runs from a 32Hz is used to generate the negative voltage $V_{\text{NEG}}$ around $-200\text{mV}$. These circuits, along with the power switch management circuits are described in detail in Sec. 2.4. The detailed design of the RF circuits are discussed in Sec. 2.5. Chapter 3 presents in-depth discussion and measurement results for the PLL, and Chapter 7 presents the design of the digital baseband.

2.3 Minimum Leakage Biasing of a Single Transistor with Gate Leakage

The power amplifier is typically one of the highest power consumer in a transmitter, especially so when the output power is $+10\text{dBm}$, as in this work. A simplified implementation of the PA (details in Sec. 2.5.1) is shown in Fig. 2-2. It is implemented as a NMOS-only style with a RF choke bias in order to aid low voltage operation [33,39]. In particular, the transistor is a thin-oxide minimum-length device sized for best efficiency. As a result, the leakage power is significant, with simulations indicating as high as 40nA (at fast corner, room temperature).

The goal for PA leakage reduction is, thus, to minimize the leakage of such a transistor, given by:

$$I_{\text{Leakage}} = I_o \cdot 10^{(V_G-V_S-V_t)/S} + I_{DG}$$  \hspace{1cm} (2.1)

where the first component is the sub-threshold current and the $I_{DG}$ term is the gate leakage current. While this is non-negligible in the 65nm CMOS process used in this
work, the sub-threshold component is still dominant in nominal conditions ($V_G=0$, $V_S=0$). The leakage is a strong function of process and temperature variations [40]. In order to reduce the sub-threshold leakage, the knobs available are the three voltage terms $V_S$, $V_G$ and $V_t$, and Fig. 2-3 shows these options:

**Positive $V_S$:** This is the most commonly used power gating technique, where a thick-oxide high-$V_t$ power switch $M_1$ defines the leakage by making $V_S$ of the low-$V_t$ active circuits positive. Significant leakage reduction can be achieved [7], however, the large active RF current passes through the power switch, leading to efficiency degradation in the PA. Simulations indicate that even with boosted gate voltage applied to the power switch (1.2V from charge pump), the PA efficiency degrades by 6 percentage points while achieving sub-nA leakage across corners.

**Increase $V_t$:** Body biasing using negative $V_B$ increases $V_t$ which then exponentially reduces sub-threshold leakage [40]. However, $V_t$ is a weak function of $V_B$, and requires large negative bias voltages, as low as $-0.6V$, to achieve sub-nA leakage in the PA across process corners. In addition, even with negative body biasing,
2.3. MINIMUM LEAKAGE BIASING

Figure 2-3: Three techniques for leakage reduction of a low-\(V_t\) device: a) High-\(V_t\) thick-oxide power gating switch in series (M\(_1\)), b) Negative body biasing to increase \(V_t\) and c) Negative gate biasing to strongly cut-off device

temperature variation of the leakage current is large.

**Negative \(V_G\):** A third alternative is to apply negative gate bias in the sleep-mode. Leakage is a strong function of gate voltage, and significant leakage reduction can be achieved with small negative voltages (for example, 100× sub-threshold current reduction with \(-200\text{mV}\) assuming \(S=100\text{mV/dec}\)). Previous work, such as \([16, 41]\) have explored negative \(V_{GS}\) biasing of high-\(V_t\) power switches. But in this work, we explore direct biasing of the thin-oxide, low-\(V_t\) PA transistor. The gate-biasing is not in the direct path of active PA current, thereby eliminating efficiency degradation. However, \(I_{DG}\) increases with negative \(V_G\), and thus needs to be carefully examined to determine the optimal bias point where total leakage power is minimized. The optimum negative bias voltage has been experimentally demonstrated previously for power gates in digital circuits \([42]\). The theoretical analysis of the minimum leakage bias point along with the robustness analysis to temperature and process variation is explored below.

Fig. 2-4b shows the measured drain current \((I_{D,PA})\) and gate current \((I_{G,PA})\) of the PA transistor as a function of the negative gate bias applied. The red curve shows the achievable total PA leakage assuming the negative bias is supplied by an ideal \(-\frac{1}{2}\) charge pump \((I_{\text{LEAK}} = I_{D,PA} - \frac{1}{2} I_{G,PA})\). This clearly shows a minimum leakage bias point in the presence of gate leakage.
2.3.1 Robustness to Temperature and Process Variations

Comparing the three leakage reduction schemes of Fig. 2-3, we see that the body and gate biasing are the most attractive because they present zero impact on on-performance. A third alternative is to simultaneously apply body and gate biasing. Fig. 2-5 compares the three schemes as a function of process and temperature variations. The simulation results are normalized.

These results indicate that negative gate biasing provides the best performance at nearly all process corners and across temperature (up to 10× better than body-only biasing and 100× better than the intrinsic leakage of the device). In addition, there is increased robustness with lesser overall variation of the minimum leakage point. For example, gate biasing leads to 4.5× variation across process corners while the intrinsic variation of the drain current is as high as 10×. Also, simultaneous gate and body biasing provides only minimal additional benefits (<10%). This is because of the weak dependence of $V_t$ on body bias as well as the effect of body diode leakage.

2.3.2 Optimum Negative $V_{GS}$ Biasing with Gate Leakage

Consider the single transistor in Fig. 2-4a. The sub-threshold current and gate leakage current are given by the following simplified equations with only the gate voltage dependence shown:

$$I_{\text{sub-threshold}} = I_S = I_{S,0} \cdot 10^{V_G/S}$$  \hspace{1cm} (2.2)
$$I_{\text{gate leakage}} = I_G = I_{G,0} \cdot 10^{-V_G/S_G}$$  \hspace{1cm} (2.3)

where $S$ is the sub-threshold slope, typically around 100mV/decade. $S_G$ is the gate-leakage slope, and is higher, about 400mV/decade or higher [43]. $I_{S,0}$ and $I_{G,0}$ are the sub-threshold and gate leakage currents when $V_G = 0$. The gate-leakage is predominantly $I_{DG}$, while the source to gate component $I_{SG}$ is negligible in comparison because $V_{SG} = V_{DG} - V_{DD}$. The drain current is thus $I_D = I_S + I_G$. The total leakage
2.3. MINIMUM LEAKAGE BIASING

(a) Leakage paths in a thin-oxide low-\(V_t\) transistor

(b) Measured leakage of a transistor with negative gate biasing (arbitrary units). The total current is plotted assuming as ideal \(-\frac{1}{2}\) charge pump.

Figure 2-4: Measured operation of a thin-oxide device with negative gate biasing
CHAPTER 2. HIGH EFFICIENCY LOW LEAKAGE BLE TX

Figure 2-5: Simulation results comparing the effect of gate and body biasing across corners and temperature. Currents are normalized.
power with varying negative gate bias is given by:

\[ P_{\text{leakage}} = V_{\text{DD}} \cdot (I_S + I_G) - V_G \cdot I_G \]  

(2.4)

Assuming that the negative gate bias is produced by a \(-\frac{1}{2}\) charge pump, as seen in Fig. 2-1:

\[ P_{\text{leakage}} = V_{\text{DD}} \cdot (I_S + I_G) + V_{\text{DD}} \cdot \left( \frac{1}{\eta} \cdot 0.5 \cdot I_G \right) \]

\[ = V_{\text{DD}} \cdot \left( I_S + \left(1 + \frac{1}{2\eta}\right) \cdot I_G \right) \]

\[ = V_{\text{DD}} \cdot \left( I_{S,0} \cdot 10^{V_G/S} + I_{G,0} \cdot (1 + \frac{1}{2\eta}) \cdot 10^{-V_G/S_S} \right) \]  

(2.5)

where \( \eta \) is the charge transfer efficiency of the charge pump. The factor 0.5 comes from the fact that an ideal \(-\frac{1}{2}\) charge pump produces an output current of \(2\times\) the input current. Since the sub-threshold component reduces with \( V_G \) while the gate-leakage component increases, there is an optimum \( V_G \) at which the total is minimized.

Minimizing Eqn. 2.7 as a function of \( V_G \):

\[ \frac{\partial P_{\text{leakage}}}{\partial V_G} = 0 \text{ at } V_G = V_{G,\text{opt}} \]  

(2.8)

\[ 0 = V_{\text{DD}} \cdot \left[ \frac{I_{S,0}}{S} \cdot 10^{V_G/S} - \frac{I_{G,0}}{S_S} \cdot \left(1 + \frac{1}{2\eta}\right) \cdot 10^{-V_G/S_S} \right] \text{ at } V_G = V_{G,\text{opt}} \]  

(2.9)

\[ \Rightarrow V_{G,\text{opt}} = -\frac{S \cdot S_S}{S + S_S} \log \left[ \frac{S_S \cdot I_{S,0}}{S \cdot I_{G,0}(1 + \frac{1}{2\eta})} \right] \]

(2.10)

and

\[ \frac{\partial^2 P_{\text{leakage}}}{\partial^2 V_G} > 0 \text{ at } V_G = V_{G,\text{opt}} \]  

(2.11)

\[ \Rightarrow P_{\text{leakage,\text{opt}}} = V_{\text{DD}} \cdot \left[ I_{G,0} \left(1 + \frac{1}{2\eta}\right) \left(\frac{S + S_S}{S_S}\right) \right] \left[ \frac{S_G \cdot I_{S,0}}{S \cdot I_{G,0}(1 + \frac{1}{2\eta})} \right]^{\left(\frac{S}{S_S}\right)} \]  

(2.12)

At the optimal negative bias point, we now calculate the ratio of sub-threshold
current to the gate leakage current, along with the ratio of drain leakage power to the $-\frac{1}{2}$ charge pump power:

$$\frac{I_{S,\text{opt}}}{I_{G,\text{opt}}} = \frac{S}{S_G} \cdot \left( 1 + \frac{1}{2\eta} \right)$$ \hspace{1cm} (2.13)

$$\frac{P_{D,\text{opt}}}{P_{G,\text{opt}}} = \frac{V_{DD} \cdot (I_{S,\text{opt}} + I_{G,\text{opt}})}{V_{DD} \cdot (\frac{1}{2\eta} \cdot I_{G,\text{opt}})}$$ \hspace{1cm} (2.14)

$$= 2\eta \cdot \left( 1 + \frac{I_{S,\text{opt}}}{I_{G,\text{opt}}} \right)$$ \hspace{1cm} (2.15)

$$= 2\eta + \frac{S}{S_G} (1 + 2\eta)$$ \hspace{1cm} (2.16)

The following conclusions can be made from the analysis above:

1) **Temperature stability:** Gate leakage has been shown to have low temperature dependence when compared to sub-threshold current \([44,45]\), because, to the first order, gate leakage is related to the probability of tunneling across a fixed potential barrier, while sub-threshold current is related to diffusion. From Eqn. 2.12, we see that:

$$P_{\text{leakage, opt}} \propto \left( \frac{S}{S+2S_G} \right)$$ \hspace{1cm} (2.17)

Thus, any temperature variation in sub-threshold current is reduced exponentially by the factor $\frac{S}{S+2S_G}$.

Taking typical values of $S = 100\text{mV/decade}$ and $S_G = 400\text{mV/decade}$, and sub-threshold current variation with temperature of $1000\times$, we see that at the optimal gate bias, the temperature variation is reduced to $1000^{1/5} = 4\times$ only (similar to Fig. 2-5). In reality, the sub-threshold slope $S$ itself has linear temperature dependence and $I_{G,0}$ has variation as well.

2) **Process variation stability:** Process variation of gate leakage occurs primarily due to variations in the gate oxide thickness. While gate-oxides are well controlled in modern CMOS processes, variations still exist. Simulations indicate variation of
about 4×, much lower than 18× for sub-threshold current (Fig. 2-5). Based on Eqn. 2.12, the optimal gate bias cannot compensate process-dependent variations of gate leakage, but reduces variations in the sub-threshold current.

3) Need for efficient charge pump: The optimal gate bias voltage, in simulations, varies from $-100mV$ to $-300mV$ across process and temperature. Thus, the choice of a $-\frac{1}{2}$ charge pump is good. As can be seen from Eqn. 2.16, the ratio of leakage power consumed at the drain of the PA to the power consumed by the charge pump is low. Assuming $\eta = 0.9$, the ratio is only 2.2×. This motivates an efficient $-\frac{1}{2}$ charge pump operating in the 100s of pA (Sec. 2.4.1).

4) Supply voltage constraints: The voltage across the gate oxide in the sleep mode, $V_{DD} - V_{G,opt}$, needs to be lower than the process-specified maximum, 1.2V in the 65nm CMOS process used in this work. This is safely ensured with the low-voltage RF design at 0.68V.

5) Negative voltage generation accuracy: As seen in Fig. 2-4b, the minimum leakage point is a shallow optimum. For example, $\pm 25mV$ in accuracy leads to less than 10% increase in the total leakage current. This relaxes the accuracy requirements on the charge pump circuits and its associated oscillator (implementation in Sec. 2.4).

The measurements, discussed in Sec. 2.6.2, confirm the theoretical analysis as well as the simulation results, and confirms the effectiveness of the negative biasing scheme for leakage reduction in the presence of gate leakage.

2.4 Leakage Management Circuits

2.4.1 $-\frac{1}{2}$ Charge Pump

The $-\frac{1}{2}$ charge pump provides the negative voltage used to bias the PA transistor in its minimum leakage bias point. The power delivered by charge pump can be as high as one-third of the total PA leakage power at the minimum leakage point (Eqn. 2.16). This indicates that a high-efficiency charge pump is needed to maximize power sav-
ings. The charge pump needs to nominally generate \( V_{\text{OUT}} = -200\text{mV} \) with a load current of \( I_{\text{OUT}} = -300\text{pA} \). The optimal voltage \( V_{\text{OUT,\text{opt}}} \) can vary from \(-100\text{mV}\) to \(-300\text{mV}\). Only switched-capacitor circuits are considered so as to avoid large external inductors. The key challenge is extremely low quiescent current and high efficiency.

Fig. 2-6 shows the implemented \(-\frac{1}{2}\) charge pump and associated control circuits. In phase \( \phi_1 \), the switched capacitors \( C_{\text{sw}} \) are connected in series and charged to \( V_{\text{DD}/2} \) each. In phase \( \phi_2 \), they are connected in parallel with the top-plates connected to ground, thereby charging the output node \( V_{\text{NEG}} \) to a negative voltage. An external 10nF capacitor is used to filter the output ripple. The body connections shown ensure that body diodes never turn on. Thick-oxide devices with long length are used in all control circuits to minimize sub-threshold currents and to avoid gate leakage. The switches are driven between \( V_{\text{DD}} \) and \( V_{\text{NEG}} \) so as to fully turn them off. A non-overlapping phase generator eliminates short-circuit current losses. A single level converter converts the clock input, running at the switching frequency \( f_{\text{sw}} \), to the \( V_{\text{DD}}-V_{\text{NEG}} \) domain.

In spite of using \( V_{\text{NEG}} \) as part of the control circuits, there are no startup issues. Since \( V_{\text{NEG}} \) is connected to bodies of NMOS switches in the converter, the body diodes prevent the voltage from rising above 0V. Simulations indicate that, even without any load circuits, \( V_{\text{NEG}} \) has a startup value less than 100mV and the charge pump always starts up on application of a clock.

The output current and input current of the charge pump is given by:

\[
I_{\text{OUT}} = 2 \cdot C_{\text{sw}} \cdot f_{\text{sw}} \cdot \left( \frac{V_{\text{DD}}}{2} + V_{\text{NEG}} \right) - I_{\text{ctrl,NEG}}
\]

\[
I_{\text{IN}} = 1 \cdot C_{\text{sw}} \cdot f_{\text{sw}} \cdot \left( \frac{V_{\text{DD}}}{2} + V_{\text{NEG}} \right) + I_{\text{ctrl,DD}}
\]

where \( I_{\text{ctrl,NEG}} \) and \( I_{\text{ctrl,DD}} \) are control circuit currents. Ideally, the output current is \( 2 \times \) the input current, and the current efficiency \( \frac{I_{\text{OUT}}}{2I_{\text{IN}}} \) is 100%, while the power efficiency is ideally \( \frac{-2V_{\text{NEG}}}{V_{\text{DD}}} \). The sources of inefficiency are the control circuit leakage
and switching. This is minimized when $f_{sw}$ is minimized, and correspondingly $C_{sw}$ is increased at the expense of circuit area [46]. In this work, we chose $C_{sw}$ of 80pF and $f_{sw}$ of 16Hz where the charge transfer efficiency is greater than 90% when delivering the nominal load of 300pA at an output of $-200mV$. The capacitors are implemented as MIMs, to minimize bottom-plate parasitics. The entire quiescent current of the control circuits operating at 16Hz is less than 20pA.

Previous work:

In [41], a negative voltage charge pump ($<-150mV$) was developed for strongly turning off power-gating switches with a quiescent power under 1pW. The circuit, however, is not designed to deliver power to the negative rail, as we need in our work,
since the process does not have gate leakage. Similar to our work, the low quiescent power is achieved with low frequency operation of the charge pump (20Hz).

### 2.4.2 32Hz Gate leakage referenced timer

As described above, the charge pump requires an input clock at 16Hz nominally to bias the PA at its minimum-leakage point. As seen in Sec. 2.3.2, the minimum leakage point is a shallow optimum, allowing for inaccuracies in the bias voltage and consequently, the clock frequency. However, it is critical that the power of this oscillator doesn’t dominate the sleep power.

One recent approach to low-frequency oscillators has been to exploit the gate-leakage of deep-submicron transistors as the current source [47]. This helps generate very small currents in the pA regime without large resistors [46]. The circuit implementation of the oscillator is shown in Fig. 2-7a. It oscillates at 32Hz and consumes 14pA, and is divided to get the 16Hz. Nodes V₁ and V₂ alternately charge up to the switching threshold of an inverter. The frequency is:

\[
f = \frac{I_{GATE,avg}}{(2C \cdot V_{TH,INV})}
\]

where \(V_{TH,INV}\) is the switching threshold of the first inverters. Given the low supply voltage, shoot-through current is negligible, enabling the low power consumption in spite of slow rise times on nodes V₁ and V₂. Fig. 2-7b shows simulation waveforms. As the current ramps the voltage on V₁ and V₂, the current value reduces due to lower voltage across the gate leakage device. In order to prevent significant slow down of the oscillator and thus keep \(I_{GATE} \approx I_{GATE,avg}\), \(V_{TH,INV}\) is skewed to be low, around 200mV. As opposed to [47], this oscillator only has 2 stages and operates off a single low-voltage supply. Using only two stages reduces power consumption for the same frequency.

The frequency of the oscillator varies linearly with gate leakage current as well.
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(a) Implementation of the 32Hz gate-leakage based oscillator

(b) Simulated waveforms showing operation of the gate leakage oscillator (50Hz)

Figure 2-7: Circuit and simulated waveforms for the gate leakage oscillator
as the switching threshold. Process variations and temperature variations of these
directly affect the frequency. Simulations indicate up to 6× variation in the absolute
frequency with process (from SS corner to FF corner), with a majority of this vari-
tion attributable to the variation of the gate leakage current. Digitally tunable gate
leakage current source transistors are used to compensate this variation, with further
frequency tuning provided by tunable capacitance $C$. Overall, 10× frequency tuning
is provided to overcome the process variation. Since gate leakage current is constant
with respect to temperature [47], the frequency is nominally temperature indepen-
dent. However, unlike in [47], no additional temperature compensation scheme is
implemented in this work, because of the low accuracy requirements of the $-\frac{1}{2}$ charge
pump.

2.4.3 Power gating choices for all other blocks

We now describe the design choices for power gating all other blocks in the design
other than the PA. Since these circuits have a large number of transistors, we consider
high-$V_t$ power gating switches. This comes at the expense on on-efficiency degrada-
tion, but these circuits only consume a small fraction of the total power (<10%).
Hence, the overall impact on TX efficiency is reduced. The design target for the
power switches is to have < 5% degradation in power, which translates to an $I\cdot R$
drop of < 5% of $V_{DD}$, or about 30mV, in the worst case corners.

The various supplies available in the system need to be utilized to the best extent
possible to get the best tradeoff between leakage and $I\cdot R$ drop. The rails available
are $V_{DD}$, GND, $V_{NEG}$ at all times, and $V_{DOUB}$ in active modes. Fig. 2-8 shows the
implementation of PMOS and NMOS power gating that uses the optimal choice of
supply rails.

The NMOS power switch is driven strongly with $V_{DOUB}$ in active mode, giving
> 10× on-resistance improvement in the worst case. It is turned off strongly with
$V_{NEG}$ biasing in sleep mode, again providing > 10× leakage reduction. On-resistance
2.4. LEAKAGE MANAGEMENT CIRCUITS

![Circuit Diagram](image)

Figure 2-8: Implementation of a) NMOS and b) PMOS power gating along with the voltage applied in active and sleep modes.

...improvement is particularly strong because of the low value of $V_{\text{DD}}$ that is close to the $V_t$ of these power switches. The leakage of the switch at $V_{\text{NEG}}$ is limited by Gate Induced Drain Leakage (GIDL) effects [40].

The PMOS power switch has on-resistance improvement by $10\times$ by turning on strongly using the $V_{\text{NEG}}$ rail instead of using 0V. However, since $V_{\text{DOUB}}$ is unavailable in sleep mode, there is no further leakage reduction feasible. Overall, the NMOS power switches offer higher on/off performance, but there are some scenarios where the PMOS power switch is necessary:

**Standard cell-based circuits**

If the standard cell library does not include cells with triple-Well (or deep n-Well) design, it is infeasible to power gate with an NMOS power switch. Hence, the digital baseband, programmable dividers in the PLL and XOSC are PMOS-power gated.

**Special cases with spurious gate leakage**

Consider the design of high-$Q$ RF capacitor banks. Fig. 2-9 shows one switchable capacitor $C_1$. INV$_1$ drives M$_1$ to connect / disconnect capacitor $C_1$. M$_1$ is chosen...
Figure 2-9: Example of spurious gate leakage paths that are not suppressed by NMOS power switches. The switched-capacitor is part of a high-Q RF capacitor bank.

to be a thin-oxide device in order to minimize resistance (and thus maximize Q) for a given parasitic capacitance. If INV\_1 were NMOS power-gated, the gate leakage of M\_1 would go through spuriously, leading to a leakage as high as 2.5nA (FF corner simulation). On the other hand, adding a power switch in series with M\_1 itself would lower the Q of the capacitor bank. Instead, the PMOS power switch M\_2 shown in Fig. 2-9 cuts off the spurious gate-leakage paths and keeps leakage below 5pA.
Figure 2-10: Implementation of the fully-integrated +10dBm PA with negative-gate biasing-based leakage reduction
2.5 RF Circuits

2.5.1 Power Amplifier Design

The PA in this work is designed for an output power of +10dBm in order to provide long communication range. The challenge is to maintain high efficiency while delivering +10dBm from a low supply voltage. Fig. 2-10 shows a detailed circuit diagram of the fully integrated PA signal chain that also makes use of the minimum leakage biasing technique described in Sec. 2.3.

Main PA

In order to maximize the output power at low $V_{DD}$, an NMOS-only RF choke-based PA architecture is chosen. This allows the drain node to swing above and below $V_{DD}$, thereby maximizing swing at low supply voltages [33,39]. This results in an output power of:

$$P_{OUT} = \frac{V_{DD}^2}{2 \cdot R_{PA}}$$  \hspace{1cm} (2.21)

An on-chip π-matching network transforms the 50Ω antenna impedance down to $\approx 20\Omega$ so as to achieve the required +10dBm output power. The main PA transistor $M_0$ is biased at $V_{B,PA} \approx V_{t,M0}$ in order to trade-off on-resistance and shoot-through current losses. This DC bias is provided through $R_0$. It can be seen that in the sleep-mode, a single near minimum-sized switch $M_1$ biases the gate of $M_0$ to its minimum-leakage negative bias point ($V_{NEG}$), and this presents near-zero loading to the RF, and thus has near-zero efficiency degradation.

The matching network is fully integrated, and expects a 50Ω load. Tuning for the matching network components to compensate for process variations is achieved with digitally controlled capacitor banks, where the switches are powered from the boosted $V_{Doub}$ rail to maximize $Q$.

RF from the previous stage is ac-coupled onto $M_0$. The PA is driven in saturated...
class-B/class-C in order to operate at peak efficiency for the constant-envelope GFSK modulation. A large swing from the previous stage ensures maximum drive of the PA, which minimizes on-resistance, and thus maximizes efficiency. As a corollary, large swing input reduces switch size for the same $R_{on}$, thus reducing sleep-mode leakage as well as reducing loading on the previous stage.

In schematic simulations, the PA has an efficiency of 54% at +10dBm output power. The losses in the transistor $M_0$ is 22%, close to the theoretical loss in an ideal class-B PA, thus indicating that the PA operates in saturated class-B/class-C mode. The choke inductor has a loss of 7.5% predominantly from DC losses, while the inductor in the pi-match has a loss of 14%. The remaining 2.5% is dissipated in the tunable capacitors in the pi-match, which reflects the high-Q ($>60$) implementation. After RC extracted simulations, the efficiency drops to about 50%, while measurements show further degradation down to 46.4%, owing to unmodeled losses.

**PA input resonant buffer and VCO buffer**

As indicated above, the PA works best when driven with the maximum swing possible. However, the PA also presents close to 1pF of capacitance. Inverter drive is precluded by the power considerations, and thus, a resonant buffer structure is chosen [33] where transistor $M_2$ only needs to provide power to replenish the losses in the tank circuit. NMOS-only structure with inductor to $V_{DD}$ also ensures that the output swings close to $2V_{DD}$, thus maximizing the swing to the PA in a low-$V_{DD}$ circuit.

Similar to the main PA transistor $M_0$, strong drive of the resonant buffer transistor $M_2$ can lead to significant decrease in device size, and thus, the loading on its driver. In order to prevent frequency pulling effects, an inverter buffer chain is used as a VCO buffer. This inverter chain is powered from $V_{DOUB}$. Strong drive ensures that the fanout of the inverter chain is close to $4 \times$. Thus the VCO is only loaded with a minimum-sized inverter ($M_4$-$M_5$). For a given on-resistance of $M_2$, the device sizing
and VCO buffer power consumption are given by:

\[
W_{M2} \propto \frac{1}{V_{DD,\text{VCOBuf}} - V_t}
\]

\[
P_{\text{VCOBuffer}} \propto \frac{V_{DD,\text{VCOBuf}}^2}{V_{DD,\text{VCOBuf}} - V_t}
\]

Thus, when designed across process corners, for low supply voltages (close to \(V_t\)), the power of the VCO buffer is optimized when \(V_{\text{DOUB}}\) is used to power it.

Overall, strongly driven inverters and resonant load lead to the resonant buffer transistor \(M_2\) to be \(25\times\) smaller than \(M_0\). The VCO buffer only draws 100\(\mu\)W from the doubler. In sleep mode, the VCO buffer and resonant buffer are gated with thick-oxide NMOS switches \(M_3, M_6\).

### 2.5.2 PLL and Frequency Modulation

The detailed design of the PLL is explained in detail in Chapter 3, along with the circuits for FSK modulation. The PLL is an integer-N PLL. It achieved the 2MHz BLE channel-spacing with the use of a 1MHz reference, itself generated from the 12MHz crystal oscillator. Low voltage operation results in reduced static and dynamic power in all blocks. The entire PLL consumes 0.68mW.

### 2.5.3 Doubler Charge Pump

A boosted 1.2V supply is needed to power the VCO buffer such that the resonant buffer is strongly driven. Also, this boosted supply is used to improve the quality factor of digitally-tuned capacitor banks in the VCO and the PA matching network. These circuits do not consume any static current except and thus do not add to the power requirements of the charge pump. Finally, this voltage is also used to overdrive the power-gating switches to reduce their size (Sec. 2.4.3).

The load requirement of this boosted supply is 100\(\mu\)W. Fig. 2-11 shows the im-
2.5. RF CIRCUITS

Figure 2-11: The voltage doubler charge pump that generates 1.2V in active mode.

plementation of the switched-capacitor charge pump [46,48]. It uses $C_{\text{DOUB}}=100\text{pF}$ and a $\approx 100\text{nF}$ external decoupling capacitor. On-chip MIM capacitors are used to minimize bottom-plate parasitics. The charge pump is operated at 3MHz using a divided version of the 12MHz crystal oscillator.

In sleep mode, the inverters are power gated. And since the load circuits are also power gated and the load current on the $V_{\text{DOUB}}$ is negligible, the rail settles to $\approx V_{\text{DD}}$, and doesn’t collapse. Thus, any sleep-mode signals and state elements in the $V_{\text{DOUB}}$ domain stay valid.

Overall, the circuits powered by the doubler only consume a small fraction of the total power, while helping reduce the supply voltage of the higher power circuits.
2.6 Measurements

Fig. 2-12 shows the die photo of the transmitter fabricated in a 65nm LP CMOS process. The die area is $2.5 \times 2.5\text{mm}^2$ while the core area is $1.6\text{mm}^2$. The testboard is shown in Fig. 2-13. The transmitter is on a daughter board, and a FPGA board is used to control the design though the SPI bus.

2.6.1 RF Performance

The power consumption of all the active circuits excluding the PA is $1.8\text{mW}$ from a $0.68\text{V}$ supply. The distribution of power is shown in Fig. 2-14. The crystal oscillator, VCO, and remaining PLL circuits consume $32\mu\text{W}$, $510\mu\text{W}$ and $132\mu\text{W}$ respectively. The VCO buffer consumes $102\mu\text{W}$ from the $1.2\text{V}$ output of the doubler, which consumes an additional $21\mu\text{W}$ generating the $1.2\text{V}$ rail. The resonant buffer draws $1\text{mW}$.

The PA delivers an output power ranging from $+10.9\text{dBm}$ down to $-5\text{dBm}$ with varying bias voltage and PA supply. The bias voltage is applied from $0.3\text{V}$ up to about $0.65\text{V}$ while the PA supply is varied from $0.25\text{V}$ up to the nominal $0.68\text{V}$. Fig. 2-16a shows the measured PA efficiency. System efficiency, defined as the ratio of output power to the power consumption of the entire transmitter, is plotted in Fig. 2-16b. At PA supply of $0.68\text{V}$, the PA has a peak efficiency of $46.4\%$ outputting $+10.9\text{dBm}$. The TX efficiency is $43.7\%$. At a lower PA supply voltage of $0.25\text{V}$, the PA has a peak efficiency of $47.2\%$ when delivering $+2.6\text{dBm}$, while the TX efficiency is $31.6\%$. All these efficiency measurements are performed with the calibration procedure described in Appendix A.
Figure 2-12: Die photo of the transmitter in 65nm LPCMOS

Figure 2-13: Test board for the transmitter. The chip is placed on a daughter board, and an FPGA controls the SPI interface.
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VCO=510μW
PLL=132μW
XOSC=32μW
Doubler=21μW
VCO Buffer=102μW
Digital=7.5μW
Res. Buffer=1mW
Total Active = 1.8mW (excluding PA)

Figure 2-14: Distribution of active power consumption excluding the PA.

Figure 2-15: Measured current efficiency of the voltage doubler as a function of load current, and the corresponding charge pump frequency
2.6. MEASUREMENTS

(a) PA efficiency

(b) Transmitter Efficiency

Figure 2-16: Measured PA and transmitter efficiencies as the PA supply and bias voltage are changed.
Efficiency of the voltage doubler charge pump is shown in Fig. 2-15 along with the frequency of the charge pump. This is plotted for $V_{\text{DOUB}}=1.2\text{V}$. The current efficiency is 95%, while the power efficiency is 84% ($\eta_{\text{power}} = \eta_{\text{current}} \cdot \frac{V_{\text{DOUB}}}{2V_{\text{DD}}}$).

The PLL has a phase noise of $-110\text{dBc/Hz}$ at 1MHz offset. Detailed measurements of the PLL are in Sec. 3.3. The spectrum for 1Mbps FSK/GFSK modulation is shown in Fig. 2-17 with the output power at +5dBm. The frequency deviation is $\pm 250\text{kHz}$. The adjacent channel power for 1Mbps GFSK is $-44\text{dBm}$ in a 1MHz band at 2MHz offset, and $-46\text{dBm}$ at 3MHz offset. This is well below the BLE spec.

Comparison with BLE Spectral Requirements

<table>
<thead>
<tr>
<th>Offset frequency</th>
<th>2MHz</th>
<th>3MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLE Spec</td>
<td>$-20\text{dBm}$</td>
<td>$-30\text{dBm}$</td>
</tr>
<tr>
<td>Measured GFSK</td>
<td>$-44\text{dBm}$</td>
<td>$-46\text{dBm}$</td>
</tr>
</tbody>
</table>

Figure 2-17: The spectrum of 1Mbps FSK and GFSK modulation, and comparison to the BLE mask.
2.6.2 Leakage Performance

The $-\frac{1}{2}$ charge pump is characterized in Fig. 2-18. The current transfer efficiency is $>90\%$ in generating $-200\text{mV}$. Optimal value of $V_{\text{NEG}}$ was around $V_{\text{NEG}}=-220\text{mV}$ with the charge pump run at 16Hz (with output of the gate leakage oscillator).

Fig. 2-19 shows measured waveforms for $V_{\text{NEG}}$. The signal is buffered, ac-coupled and averaged (using the clock as the trigger). External clock is used for this measurement in order to avoid jitter and improve the averaging. The DC-value of the signal is around $-220\text{mV}$ and the ripple is clearly seen to be around 15mV. On the falling edge of clock (phase $\phi_2$ of Fig. 2-6), $V_{\text{NEG}}$ has a step change, and it is discharged slowly until the next cycle. In Fig. 2-4b, the minimum-leakage bias point was plotted assuming a 100% efficient charge pump. The percentage increase in the total leakage as $V_{\text{NEG}}$ is swept is plotted in Fig. 2-20. It shows that the 90% current efficiency only results in a 3.5% increase in the total leakage at minimum leakage bias point. This is also consistent with the analysis of Eqn. 2.12, where, to the first order, $\eta = 0.9$ also results in 3.6% increase in $P_{\text{leakage,opt}}$.

The total leakage of the transmitter is 370pW (550pA). The distribution of the leakage power is given in Fig. 2-21. The drain leakage of the PA is 211pW, and $-\frac{1}{2}$ charge pump consumes 90pW. This ratio, which comes to $2.3\times$ is consistent with the analysis of Eqn. 2.16. The gate-leakage oscillator consumes 9.5pW. All the remaining circuits have a leakage of 47pW.

Fig. 2-22 shows the measured chip leakage as a function of temperature. Both the minimum leakage point as well as the leakage at $V_{\text{NEG}}=0$ are plotted. At each temperature, the output of the $-\frac{1}{2}$ charge pump is set to the optimal value by adjusting the frequency of operation. At 25°C, the leakage reduction is $30\times$. At 80°C, the leakage reduction is $100\times$. The total variation of leakage over $-40\text{°C}$ to $+80\text{°C}$ reduces from $1000\times$ to only $10\times$ with the optimal negative gate biasing. This is close to the analysis of Sec. 2.3. The optimal negative bias varies from $-300\text{mV}$ at 80°C to $-50\text{mV}$ at $-40\text{°C}$. The optimal charge pump frequency varies from 100Hz
CHAPTER 2. HIGH EFFICIENCY LOW LEAKAGE BLE TX

Figure 2-18: Performance of the $-\frac{1}{2}$ charge pump.

Figure 2-19: Oscilloscope measurements showing ripple on $V_{\text{NEG}}$
Figure 2-20: Plot showing the impact of 90% charge transfer efficiency on the minimum leakage bias point. As $V_{\text{NEG}}$ is swept, the percentage increase in the total current when compared to Fig. 2-4b is plotted. At the minimum leakage bias point, the 10% inefficiency only has a 3.5% impact on the total.

Figure 2-21: Distribution of leakage power consumption in all the blocks of the system.
CHAPTER 2. HIGH EFFICIENCY LOW LEAKAGE BLE TX

Figure 2-22: Leakage of the full chip as a function of temperature in three operating modes a) No negative gate biasing b) Fixed frequency operation of charge pump and c) Minimum leakage biasing with optimal charge pump frequency down to 4Hz. Fig. 2-22 also shows the leakage power if a fixed charge pump frequency of 50Hz is used across all temperatures (for example, if a temperature sensor is not available in the system). This leakage is $2.2 \times$ higher than optimal at $-40^\circ C$, $1.25 \times$ at $25^\circ C$ and only $1.06 \times$ at $80^\circ C$.

Fig. 2-23a shows a histogram of the PA leakage, $I_{D,PA} - \frac{1}{2}I_{G,PA}$, at $V_{NEG}=-200mV$ for 25 chips. This is measured with a source meter supplying the negative voltage to speed up measurements. $-200mV$ is chosen to be approximately the minimum leakage bias point. The measured variation using the $-200mV$ bias is only $\pm 13\%$. However, it increases to $\pm 27\%$ when $V_{NEG}=0$. This further confirms the robustness of the negative gate biasing scheme (discussed in Sec. 2.3.1).

2.6.3 System Measurements, Demo and Comparison

The measured startup of the chip from sleep-mode is shown in Fig. 2-24. It shows the $EN_{TX}$ enable signal, output of the 12MHz crystal oscillator (after on-chip division by 12), and the doubler output $V_{DOUB}$ voltage. In sleep-mode, it can be seen that $V_{DOUB}$ maintains itself at $V_{DD}$ of 0.68V, as explained in Sec. 2.5.3. The crystal oscillator starts up in about 2ms, at which point the doubler starts functioning. $V_{DOUB}$ settled
2.6. MEASUREMENTS

Figure 2-23: Measured histogram of PA leakage with and without negative gate biasing.
Figure 2-24: Startup transient of the transmitter, with XOSC and $V_{DOUB}$ settling.
in an additional 4ms, at which point the chip is ready to turn on the PLL, and start RF transmission. The total startup time is large (6ms), however, the energy in the startup is:

\[ E_{\text{startup}} = 6\text{ms} \cdot 32\mu\text{W} + 4\text{ms} \cdot 21\mu\text{W} = 276\text{nJ} \quad (2.24) \]

This translates to only about 11\(\mu\text{s}\) of the power consumed by the entire transmitter when on. Typical BLE packets are about 200\(\mu\text{s}\) long, and thus, the startup energy is negligible.

The TX was able to successfully communicate with commercial BLE radios from Texas Instruments \cite{12}, as well as to Android and iOS devices. Fig. 2-25 shows the demo board and Fig. 2-26 shows the screenshot of a custom Android app showing received packets. The app shows details of the last packet as well as a plot showing the RSSI (Received Signal Strength Indicator) for the last 10 packets received from each sensor node. Table 2.2 compares this work with previous work. It highlights the design of high efficiency RF circuits simultaneously with low off-state leakage. The on/off power ratio, at \(7.6 \times 10^7\), is the highest of these works.

### 2.7 Conclusions

In conclusion, a 2.4GHz BLE-compatible transmitter architecture for use in ultra-low duty cycle applications has been presented. Low voltage operation, extensive power gating and a negative gate biasing technique help in achieving a peak TX efficiency of 43.7% at an output power of +10.9dBm while reaching a leakage power of 370pW, for an on/off ratio of \(7.6 \times 10^7\).
CHAPTER 2. HIGH EFFICIENCY LOW LEAKAGE BLE TX

Figure 2-25: Photos showing the front and back of the demo board and the chip antenna.

Figure 2-26: App screenshot shows BLE communication between the transmitter and an Android device. The graph is a plot of RSSI for the last 10 packets.
Table 2.2: Comparison to previous transmitters

<table>
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<th>Ref</th>
<th>Tech.</th>
<th>(V_{DD}) (V)</th>
<th>(P_{OUT}) (dBm)</th>
<th>TX Eff. (%)</th>
<th>(P_{Leak}) (pW)</th>
<th>On/Off Ratio</th>
<th>Comment</th>
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<td>[7]</td>
<td>180nm</td>
<td>4</td>
<td>−10</td>
<td>0.2</td>
<td>3300</td>
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<td>−45</td>
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<tr>
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<td>&gt; −29</td>
<td>&gt; 0.7</td>
<td>39.7</td>
<td>4.8 (\times) 10^6</td>
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<tr>
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<td>0.8</td>
<td>46</td>
<td>-</td>
<td>-</td>
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<td>[34]</td>
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<td>1.8</td>
<td>6</td>
<td>10.1</td>
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<td>-</td>
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<td>5</td>
<td>5</td>
<td>54000</td>
<td>1.2 (\times) 10^6</td>
<td>802.15.4 with PLL, I/Q</td>
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<td>-</td>
<td>-</td>
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<td>-</td>
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<td>17.4</td>
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<td>-</td>
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<td>10.9</td>
<td>43.7</td>
<td>370</td>
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Chapter 3

A Low Voltage Phase Locked Loop with Direct Modulation of VCO

This chapter discussed the design and measurement results for the low voltage phase locked loop (PLL) used in the transmitter of Chapter 2. Low voltage operation of the PLL results in power reduction through reduced switching power. It is enabled by optimization of the VCO, charge pump and frequency divider. The PLL also includes a capability for direct modulation of the VCO, which is used for GFSK modulation.

3.1 Background and Previous Work

Narrowband RF systems rely on stable, accurate LO generation to function reliably. PLLs operating from a crystal reference provide these stable LOs, but typically consume a large amount of power and set limits to the overall RF power. However, since communication costs dominate wireless sensor systems’ power budgets, schemes to reduce PLL power can lead to significant battery life improvements. One approach has been to eliminate the PLL and use RF resonators such as FBARs [33]. Significant power reduction is feasible, but compatibility with standards such as Bluetooth Low Energy (BLE) is compromised because of insufficient frequency coverage.
In this work, we aim to address LO power generation, in the 2.4GHz ISM band, through a low-voltage PLL optimized for power consumption. Previous low-voltage PLLs such as [49] and [20] have shown operation down to as low as 0.5V, but the implementations still consume significant power (> 2mW). On the other hand, works such as [50] and [51] demonstrate low power PLLs operating at nominal voltages such as 1V, leaving room for further reduction through voltage scaling. For example, a recent work presented a 0.3V PLL architecture that also has ultra-low 780µW power consumption [52].

The PLL is co-optimized for RF and leakage performance for use in ultra-low duty cycle applications. The PLL functions down to 0.68V and has a power consumption of 680µW. The following sections discuss the PLL architecture and circuit optimizations along with measurements from a testchip.

### 3.2 PLL Architecture and Circuit Blocks

Figure 3-1 shows the architecture of the integer-N PLL. A 12MHz crystal oscillator is divided down to 1MHz, allowing the PLL to provide 2MHz channel spacings, as required by BLE. The 12MHz crystal output is also used by the digital baseband in the full system. The divider in the feedback path includes a fixed divide-by-2 operating at 2.4GHz and a 32/33 dual-modulus prescaler [53] running at 1.2GHz, followed by a programmable divider.

True Single Phase Clock (TSPC) flip-flops are used to enable low-voltage operation. The 32/33 prescaler is the largest value feasible to achieve complete channel coverage in the integer-N architecture. This minimizes the operating frequency of the programmable divider to 37MHz which is easily achieved at 0.68V using standard static logic-based synthesis.
Figure 3-1: Block diagram showing the detailed implementation of the PLL used in this work. The PLL includes direct modulation of the VCO for GFSK and extensive power gating.
It should be noted that all 802.15.4 channels (with 5MHz spacing) can also be produced by simply replacing the crystal with a 15MHz one (making the PLL reference 1.25MHz). The feedback loop is designed for a phase margin of 40° and a bandwidth of 50kHz. Values of $R_1 = 400k\Omega$, $C_1 = 14pF$, $C_2 = 1.2pF$, $R_3 = 250k\Omega$ and $C_3 = 2pF$ are used in the third-order loop filter.

### 3.2.1 Charge Pump

Low voltage operation of the Charge Pump gives a linear reduction in power consumption, but limited output voltage range is a significant challenge at low supply voltages [52]. For example, even with sub-threshold operation, at a supply of 0.68V, the linear output range is only 380mV (assuming 150mV saturation). Since some of this linear range is required to accommodate overshoot in the transients, the usable output range is only about $0.2 - 0.3V$.

A second challenge for low power operation of the charge pump is filtering of reference spurs arising from charge sharing. This is typically mitigated by analog voltage buffers that, when $UP = 1$ or $DN = 1$, bias the current mirror at the charge pump output voltage. To avoid significant energy overhead of an analog buffer, [50] proposed a biasing scheme using diodes. This is shown in Fig. 3-1 with transistors $MN_1$ and $MP_1$. The current mirrors are now biased at fixed voltages set by the diode-connected transistors. At low supply voltages, with the low inherent output voltage range of the charge pump, this fixed-voltage biasing reduces reference spurs by 15dB.

### 3.2.2 VCO

The small voltage range of the Charge Pump imposes design constraints on the VCO. For a 300mV range, simulated $C_{Max}/C_{Min}$ of the varactors is only 1.2×. Hence, using a single varactor to cover the entire 2.4GHz band would lead to a large fixed capacitance, which would reduce the inductance required for resonance, thereby increasing power. In addition, the VCO gain would be $> 300MHz/V$ and lead to degraded output
spectrum due to noise and coupling onto the VCO control voltage. We mitigate this problem by including a closely-spaced digitally tuned coarse capacitor bank (Fig. 3-2) that centers the VCO close to the required frequency and lets the PLL settle around that. Figure 3-3 shows the measured VCO response. With a 14.4MHz coarse frequency step and an 87MHz/V varactor gain, 200mV of the charge pump linear output range is utilized, satisfying the constraints.

A cross-coupled inverter architecture is chosen for the low-voltage VCO to minimize power. The oscillator swings rail-to-rail and power consumption is lower than a NMOS-only architecture and does not suffer adversely from shoot-through current due to the low supply voltage. However, one challenge of operating this at 0.68V is that the transistors are biased in sub-threshold, leading to large sizes and associated parasitic capacitance. In order to mitigate this, body-biasing is applied to the transistors to increase current for the same transistor size, thus leading to smaller transistors. But, providing the bias voltages for the NMOS and PMOS separately is a challenge with a limited power budget. We propose a self-body-biasing scheme (Fig. 3-2) where bodies of the NMOS and PMOS are tied together. The body diodes self-bias at $V_{BODY} \approx V_{DD}/2$ (<20mV variation across corners). Since $V_{DD}$ is low, the forward current in the body diodes is negligible, including across corners. Simulations show a 1.5× reduction in the transistor sizes, thereby significantly reducing parasitic capacitance.

### 3.2.3 Divider

Low voltage dividers require careful design to achieve functionality at RF. To achieve the best programmability, a flip-flop-based architecture such as a dual-modulus divider is necessary, as opposed to an injection-locked divider such as in [52]. Since static flip-flops in our process do not work at 2.5GHz below 0.9V, we apply a dynamic TSPC logic style (such as done in previous PLLs in [50,53]). Power savings are achieved through both voltage scaling and lower switching capacitance in the
CHAPTER 3. A LOW VOLTAGE PLL

Figure 3-2: Implementation of the low-voltage VCO with self-body-biasing and coarse frequency tuning.

Figure 3-3: Measured VCO tuning characteristics show coverage of the 2.4GHz ISM band.
3.2. PLL ARCHITECTURE AND CIRCUIT BLOCKS

Figure 3-4: Implementation of the True Single Phase Clock (TSPC) flip-flop used in the low-voltage 2.5GHz frequency divider.

smaller dynamic flip-flops. Figure 3-4 shows the 2.5GHz divide-by-2 circuit with the TSPC flip-flop and the relative sizing of the devices used to achieve functionality at 2.5GHz across corners. The same flip-flop is used in the 32/33 prescaler. An alternative is to use CML logic styles, which have been shown to achieve even lower voltage operation [20, 49], but could have higher power consumption.

3.2.4 Frequency Modulation

1Mbps GFSK modulation is achieved by direct modulation of the VCO [37] in order to avoid a high-power I/Q mixer. Once the PLL has settled, the integrating charge-pump is turned off by making EN_{PLL} low (see Fig. 3-1). The PFD is placed in reset where no UP/DN pulses are generated. Simultaneously, the loop filter is disconnected so that the varactor control voltage V_{VCO} is held on capacitor C_3. This is held constant for the duration of the packet (< 0.5ms in BLE), keeping the center frequency fixed. The switch is carefully designed to have minimal leakage. The design is aided by the fact that it is in series the large loop filter resistor R_3 (250kΩ).
The main VCO varactor is 170fF (single-ended) and provides a 87MHz/V gain. For modulation, a second, 5× smaller varactor (35fF single-ended) and has a gain of about 17MHz/V. The varactor is controlled by a capacitive DAC to generate the 1Mbps GFSK modulation. The DAC is driven by the digital baseband. Fig. 3-5 shows the implementation of the capacitive DAC used.

The FSK control voltage $V_{FSK}$ is precharged to $V_{DD}$ initially, and the Frequency Control Word (FCW) is held at the mid-point of 64. When $EN_{PLL}$ is low, $V_{FSK}$ is high impedance, and the only DC leakage path is through the switch $EN_{PLL}$, which is designed to be low-leakage. When the FCW changes, the capacitor bank couples a voltage onto $V_{FSK}$ which then modulates the frequency through the varactors. The voltage step of the DAC and the resulting frequency step is:

![Figure 3-5: Capacitive DAC used to generate GFSK modulation](image)
3.2. PLL ARCHITECTURE AND CIRCUIT BLOCKS

\[ V_{\text{FSK,step}} = V_{\text{DD}} \cdot \frac{C_{\text{sw}}}{C_o + 127C_{\text{sw}}} \]  \hspace{1cm} (3.1)

\[ \Delta f_{\text{step}} = 17\text{MHz}/V \cdot V_{\text{FSK,step}} \]  \hspace{1cm} (3.2)

\[ = 17\text{MHz}/V \cdot V_{\text{DD}} \cdot \frac{C_{\text{sw}}}{C_o + 127C_{\text{sw}}} \]  \hspace{1cm} (3.3)

In this design, \( C_{\text{sw}} = 5\text{fF}, C_o = 4.5\text{pF} \), giving a voltage step of 0.7mW and a resulting in a nominal frequency step of 11kHz (4ppm of 2.5GHz) and a nominal total FSK tuning range of \( \pm 0.7\text{MHz} \) resulting from a total voltage range of only 85mV. Such fine tuning of the frequency helps generate an accurate GFSK modulation waveform. The key advantage of this technique for FSK modulation is that relatively large capacitors are switched to generate small frequency steps. For example, the effective amount of capacitance change seen by the tank of the VCO is about 10aF. In addition, a small total voltage range ensures linear response. This is in contrast to the approach of [54], where a thermometric coded capacitor bank with non-uniform capacitor sizes is used to ensure linear response for generation of aF-level capacitance changes.

The capacitive DAC also requires binary weighted buffers and resistors in order to ensure that all bits have the same rise time and fall time. This is important when switching multiple bits simultaneously. This requirement is one disadvantage of this approach, in comparison to the thermometer-coding in [54].

3.2.5 Leakage Management

Since this PLL has been designed for use in the ultra-low-leakage transmitter of Chapter 2, power gating has been applied to all blocks, as shown in Fig. 3-1. Thick oxide NMOS switches are used in most cases, with PMOS switches used to gate standard cell-based circuits (tradeoffs discussed in detail in Sec. 2.4.3). The resulting leakage power of the PLL is 170pW without \( V_{\text{NEG}} \). When strongly cutoff with \( V_{\text{NEG}} \), the total PLL leakage reduces to 27pW.
3.3 Measurements

Figure 3-6 shows the zoomed-in die photo of the transmitter from Chapter 2 with the PLL blocks identified. The PLL occupies a core area of 0.2mm².

All core circuits operate at 0.68V. A 1.2V rail, generated by a charge pump running from the crystal, powers various switches in the design, including the power gating switches. This 1.2V rail consumes < 2µW in active mode. The total power consumption of the PLL is 680µW. The distribution of power in the various blocks is shown in Fig. 3-7. A majority of the power is consumed by the VCO.

The far out 50MHz wide spectrum of the PLL output is plotted in Fig. 3-9a. The spurs from the 1MHz reference is better than −50dBc. The −55dBc spur at 12MHz comes from coupling from the XOSC. A close-in view in Fig. 3-9b shows a 15dB reduction of spurs at 1MHz and 2MHz (first and second harmonic spurs) when enabling the Charge Pump spur reduction technique.

The phase noise of the PLL is plotted in Fig. 3-8. It shows a phase noise of −110dBc/Hz at 1MHz offset and −120dBc/Hz at 3MHz offset. This gives a VCO
3.3. MEASUREMENTS

VCO = 510 $\mu$W

\[ VCO = 510 \, \mu W \]

\[ \text{LF Dividers + PFD} = 3 \, \mu W \]

\[ \text{LF Dividers} = 82 \, \mu W \]

\[ \text{XOSC} = 32 \, \mu W \]

\[ \text{Charge Pump} = 48 \, \mu W \]

\[ \text{Total PLL Power} = 680 \, \mu W \]

Figure 3-7: Distribution of power in the various blocks of the PLL.

\[ f_{\text{center}} = 2.414 \, \text{GHz} \]

\[ -110 \, \text{dBc/Hz at 1 MHz} \]

\[ -120 \, \text{dBc/Hz at 3 MHz} \]

Figure 3-8: Measured phase noise of the PLL at 2.414GHz.
Figure 3-9: Measured spectrum of the PLL output showing a) spurs are lower than $-50\text{dBc}$ and b) spurs are reduced by $>15\text{dB}$ by the charge pump bypass circuit.
phase noise FOM of $-182\text{dB}$. The FOM is defined as below and captures the power consumption phase noise trade-off in the white noise limited regime:

$$\text{FOM} = 10 \log \left[ \left( \frac{\omega_{o}}{\Delta\omega} \right)^{2} \frac{1}{L(\Delta\omega) \cdot P_{DC}} \right]$$ \hspace{1cm} (3.4)

Figure 3-10 shows the transient response of the PLL. The startup time is 130$\mu$s for 20ppm settling. This reduces to 70$\mu$s for a step-frequency change of +2MHz. Both are below the requirements for BLE and 802.15.4. Figure 3-11 shows how the settling time can be reduced further by up to 2× with higher charge pump current (and correspondingly higher total power). Similarly, the startup time of the PLL can be reduced down to 90$\mu$s.

In Fig. 3-12, we plot a time domain waveform showing FSK modulation. The instantaneous frequency is measured through post-processing of oscilloscope data, and in this example, 1Mbps data is modulated with a frequency deviation of $\pm 350\text{kHz}$.

Table 3.1 compares this work to recent PLLs in both the low voltage and low power space.
Figure 3-10: Measured 20ppm settling time of the PLL in a) Startup at 2.452GHz and b) Frequency step from 2.452GHz to 2.454GHz
3.3. MEASUREMENTS

Figure 3-11: Effect of increased $I_{CP}$ on settling time.

Figure 3-12: Example time domain measurement of FSK modulation. This example shows 1Mbps data modulated with $f_{dev} = \pm 350$kHz.
### Table 3.1: Comparison to recent PLLs

<table>
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<tr>
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<td><strong>27</strong></td>
<td>/</td>
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* Value read from Fig. 5
3.4 Conclusions

An integer-N PLL has been presented with ultra-low power operation at 680µW. It operates at a low voltage of 0.68V in a 65nm LPCMOS process. The VCO, charge pump and a TSPC dynamic flip-flop-based frequency divider were all optimized for the low voltage low power regime. The PLL achieves a phase noise of $-110\text{dBc/Hz}$ at 1MHz offset and has a startup time of 130µs. Extensive power gating bring down the leakage power of the PLL to 27pW allowing operation in extremely low duty cycle applications. The PLL includes a direct modulation of the VCO for frequency modulation required by BLE. This PLL enables the low-voltage operation of the transmitter in Chapter 2. Additionally, if this PLL is combined with a low power $-10\text{dBm}$ PA such as in [33], it could result in a sub-mW Bluetooth Low Energy (BLE) transmitter for short-range applications.
Chapter 4

Protocol Considerations for Ultra-low Duty Cycles \(^1\)

As discussed in Chapter 1, a lot of industrial monitoring applications are inherently low duty cycle, and are also among the most energy constrained. Long lifetimes as high as 20 years is desirable, calling for minimizing power consumption. Recent work has shown energy harvesting that works at the nW power levels \([55, 56]\), extending operation of sensor nodes to more stringent environments. Similarly, analog sensor front-ends \([57]\), processors \([58]\) have been shown to operate at nW power levels. Finally, we have seen in Chapter 2 that sleep-mode power of radios can be brought down to sub-nW levels.

In this context of a sensor node operating at very low average power consumption, we take a look at existing RF communication protocols and analyze their operation in very low duty cycles. In particular, we look to keep the average power of the sensor node as close to the sleep-mode power as is possible.

\(^1\)The work presented in this chapter is in collaboration with Peter Iannucci, Nathan Ickes and Prof. Hari Balakrishnan
4.1 Protocol Requirements

The wireless network parameters include the communication range, data rate, channel bandwidth, modulation and coding, and the number of supported nodes. In power-constrained sensor nodes, most standards employ simple modulation schemes (for example binary FSK in Bluetooth Low Energy or at most 4-QAM in 802.15.4), and thus, the data rate is about the same as the channel bandwidth. The communication range is set by the combination of output power of the sensor nodes, and the coding applied. These are low-level parameters, but when coupled with the higher level communication protocols, and the average datarate requirements of each node, the maximum number of nodes supported by the network can be determined.

However, given the varied data rates and coding applied, a useful way to compare protocols is to look at the ratio of transmission time of useful information and the complete channel time used for the communication. This has implications on both average power consumption and the number of nodes supported.

In this chapter, we are thus looking at power consumption and “protocol network utilization” as the key comparison points, in the context of low duty cycle communication.

4.2 Existing Protocols and Limitations

For discussion of power consumption, in this section, we use the power consumption values of a commercial radio such as CC2540 from Texas Instruments [12]. It has a transmit power of 75mW, receiver power of 50mW and leakage power of 3µW. For a research radio, we use a transmit power of 25mW, leakage of less than 1nW (Chapter 2) and receiver power of 4mW [59].
4.2. EXISTING PROTOCOLS AND LIMITATIONS

4.2.1 Mesh Protocols

Mesh networks like Contiki [60] and Zigbee [61] have the advantage of extending range of the network through relaying. But, in order to coordinate with other nodes to find paths to the base-station, and to find new nodes in the system, the protocols incur significant overhead. The nodes wake up a lot more frequently than their intrinsic datarates suggest. For example, Contiki requires the nodes to have duty cycles of about 0.1 to 1% [60]. Even if the intrinsic datarate of a node approaches 0bps, the average power consumption of the radio is much higher than the leakage. This is dominated by the overhead of forwarding packets in the network and other protocol overhead. The average power is about 50µW in commercial radios (17× higher than leakage) and 4µW in research radios (1000× higher than leakage).

If, instead, we look at point-to-point links, each node doesn’t have to relay information from other nodes. Hence, they will potentially scale well for low duty-cycle applications. The issue of communication range can be addressed in, potentially three ways:

1. Adding the required number of access points/base stations to cover the region of interest.

2. Taking advantage of the asymmetric energy budgets of the sensor nodes and base-stations to enhance range. This implies the use of high power, high sensitivity receivers and high output power transmitters at the base-station.

3. Coding techniques to enhance the sensor-node to base-station links. This takes advantage of the energy asymmetry between encoding and decoding for most error-correction codes.

We will now look at a few currently available standards and consider their operation in ultra-low duty cycles.
Figure 4-1: Bluetooth Low Energy communication is scheduled by a basestation with a Beacon. The sensor node needs to wake up with a guard time proportional to the packet interval.

4.2.2 Bluetooth Low Energy (BLE)

The Bluetooth Low Energy (BLE) [62] is a common standard used in consumer electronics and a host of new IoT devices. There are multiple modes of operation of a sensor node in BLE:

Connected Mode

This is the default mode in which sensors communicate their data to the base-station. Each communication transaction is initiated by a periodic beacon from the base-station, followed by a reply from the sensor node and an acknowledgment from the base-station, as shown in Fig. 4-1. Since the communication is initiated by the base-station, the sensor needs an accurate timer that wakes up the RF at the right time. In order to compensate for the timing inaccuracy of its clock, the sensor node needs to turn on its receiver early to accommodate a guard time. The energy spent by the sensor node in each beacon interval is given by:

\[
E_{interval} = E_{sleep} + E_{guard} + E_{beacon} + E_{TX} + E_{ack} \\
= P_{sleep} \cdot T_{sleep} + P_{RX} \cdot \alpha \cdot T_{sleep} + P_{RX} \cdot (T_{beacon} + T_{ack}) + P_{TX} \cdot T_{data} \quad (4.1)
\]
Figure 4-2: A reconnected mode of Bluetooth Low Energy. Communication starts with an advertisement from a sensor node, which results in no guard time requirements.

where $\alpha$ is the fraction of the sleep time that is needed for the guard time. This is set by the temperature and noise characteristics of the oscillator used. At very low duty cycles, or very long packet intervals ($T_{\text{sleep}}$), the average power tends towards

$$\lim_{T_{\text{sleep}} \to \infty} P_{\text{avg}} = P_{\text{sleep}} + \alpha \cdot P_{RX}$$

Hence, we can see that the average power is limited by the receiver power and the sleep timer accuracy, and not by the leakage power (sleep). For example, commercial radios with 500ppm accurate sleep timers would have an average power of $25\mu W$ ($8 \times$ higher than leakage) and research chips even with 100ppm accurate clocks would consume $400nW$ ($400 \times$ higher than leakage)

It should also be noted that the BLE standard limits the maximum $t_{\text{sleep}}$ period to 32s. This limits the maximum duty cycling. This implies that in the final implementation, depending on the sleep mode power and the receiver power consumption, the above limit may not be feasible.

**Reconnect Mode**

The key problems with the connected mode of BLE is that the timing is set by the energy-abundant base-station while the sensor-node needs to handle guard timing. So, below a certain duty cycle, it is beneficial for the sensor node to disconnect and
reconnect from the base-station. The absolute time of reconnection is set by the
sensor node, and hence no guard time is required. The sensor node advertises itself,
the base-station sets up a connection. With the sensor node connected now,
the base-station sends a beacon, the sensor node sends its data and a request to
disconnect, and then the base-station acknowledges the data and the disconnection.
The timing of a complete transaction is shown in Fig. 4-2. The energy per interval is:

\[
E_{\text{interval}} = E_{\text{sleep}} + E_{\text{adv}} + E_{\text{connect}} + E_{\text{beacon}} + E_{\text{data}} + E_{\text{ack}}
\]

\[= P_{\text{sleep}} \cdot T_{\text{sleep}} + P_{\text{RX}} \cdot (T_{\text{connect}} + T_{\text{beacon}} + T_{\text{ack}})
\]

\[+ P_{\text{TX}} \cdot (T_{\text{adv}} + T_{\text{data}})\]  

(4.5)

\[\lim_{t_{\text{sleep}} \to \infty} P_{\text{avg}} = P_{\text{sleep}}\]  

(4.6)

This solves the problem that the average power settles to the leakage power.
However, the following limitations need to be addressed.

1. There is a lot of overhead in the connection setup and close protocols. At least
five packets are communicated in one transaction.

2. A majority of the sensor nodes are now assumed to be connecting and dis-
connecting, which implies that a majority of the communication is happen-
ing asynchronously, thereby leading to the chance for packet collision. Such
packet collisions can be partially alleviated with Carrier Sense Medium Access
(CSMA). In this scheme, before transmission of the advertisement, each node
measures the energy in the channel to estimate if there are other nodes trans-
mitting. However, the node is not be in the receive range of all nodes in the
network, which implies that there will still be collisions\(^2\).

3. The connection procedure, as defined in the protocol is probabilistic, because

\(^2\)This is called the “hidden terminal problem”. In an asymmetric network where the sensor nodes
have poor receive sensitivity with respect to the base station, this problem is even more severe.
both the base-station and sensor search over the three advertisement channels. Even though, in the best case, the base-station connects to the sensor after the first advertisement, it might not happen because of a missed packet reception. All these can potentially increase the energy consumed by the sensor every packet interval. Even though, in the limit the power is limited by leakage, this overhead causes the break-even point to occur at lower duty cycles.

4.2.3 802.15.4 in Star Topology

Communication in 802.15.4 is scheduled by a common beacon from the base-station addressed to all the sensors. The beacon interval is fixed by the network designer. Each interval has Time Division Multiple Access (TDMA) scheduled sections used by nodes with a large amount of data. The rest of the interval is set aside for Carrier Sense (CSMA) access by all other nodes.

Similar to in BLE, nodes with low duty cycles should not schedule future communications and incur guard time power loss. They must wake-up with their own local clocks and send their data during the carrier-sense periods. In order to accomplish this, the overhead incurred by the sensor node are:

1. The sensor needs to wait for the next beacon to synchronize and know the next CSMA period, thereby wasting energy. However, the timing uncertainty (the \( \alpha \cdot T_{sleep} \)) doesn’t translate to an unbounded energy draw, since the maximum wait time is bounded by the beacon period, which can be set small (for example <100ms) to reduce this loss.

2. Packet collisions between other nodes in the CSMA period.

The issues are similar to the BLE reconnect-mode of operation. Section 4.3 provides some ideas to improve these protocols and reduce overhead.


4.2.4 ETSI Low Traffic Network (LTN) Standard

European Telecommunications Standards Institute (ETSI) has a working committee drafting a standard for very low traffic networks (tens of bytes per day) \cite{63}. In the PHY, they propose Ultra Narrow Band (UNB) communication (100 to 600 bps) or Orthogonal Sequence Spread Spectrum (OSSS) at similarly low rates in order to achieve long range. They operate in the 900MHz ISM bands\(^3\). Sigfox \cite{27} is a company that has a commercial implementation of such a UNB network.

On the medium access front, the standard talks about asynchronous transmission from the sensor node, with optional windows for downlink data from the base-station. This approach essentially removes the overhead of synchronization, thereby potentially reducing power consumption down to the leakage. Optionally, the standard allows for periodic synchronization (every 128 seconds) through beacons from the base-station. The asynchronous approach is similar to the CSMA transmission in 802.15.4 and BLE advertisements. It is also the idea that we propose in Section 4.3, where we analyze its effectiveness, along with analysis of network capacity and packet collision, which are potential problems when all nodes are asynchronous.

The Sigfox implementation achieves an average power consumption of 50\(\mu\)W.\(^4\)

4.2.5 Weightless.org

Weightless SIG \cite{64} is a competing Ultra Narrow Band (UNB) machine-to-machine communication standard that is under development. They propose low datarates (down to 200bps) and operation in 900MHz ISM bands in order to achieve long range. This standard requires synchronization (beacon period of 15 minutes) and has a total active time of about 100ms every beacon period. However, the standard is not public, and the details of the synchronization protocol and transmission is not

\(^3\)This is compliant with spectrum allocations in USA, Europe, China and Japan

\(^4\)It is not clear from \cite{27} as to which mode of the protocol is used for the power measurement, and under what duty cycle conditions it is specified.
available. The expected average power consumption is about 25 to 50\(\mu W\) [64].

### 4.2.6 Wake up Radio Based Systems

Wake up receivers are always-on radios that listen in for a wake-up signal from a base-station in order to wake up the full system. These receivers are typically simpler, and may operate at reduced bit rates in order to save power consumption or to enhance sensitivity. In [65], a wake-up receiver that consumes only 116nW is presented. This is one of the lowest power consumption reported. It operates at a data rate of 125kbps but has a sensitivity of only −46dBm. On the other hand, receivers such as [66] achieves an excellent sensitivity of −97dBm. This design also operates at 10kbps, and consumes 99\(\mu W\). These wake up receivers can potentially be duty cycled to reduce average power, at the cost of response times. Overall, if base-station control of sensor-node timing is necessary, wake-up receivers are a good solution, and can compete with the fully synchronized approaches such as the connected-mode of the BLE. But, implementing sub-nW wake-up receivers that maintain long range is a hard problem.

### 4.3 Proposed Protocol for Ultra-Low Duty Cycles

The protocols discussed above are all efficient in their PHY specifications, with short headers, allowing for efficient transmission of short packets. The differences in terms of instantaneous datarates sets the communication range. 802.15.4 or BLE, with 250kbps and 1Mbps rates respectively are good for dense networks with a large number of nodes, for example in a factory, monitoring various equipment. On the other hand, the UNB protocols with the very low datarates are useful for sparse networks such that the base-stations can be placed far apart, reducing installation costs. This is useful for networks such as farm and crop monitoring, or smart meters for water,

\(^5\)The duty cycle conditions are not specified.
electricity and gas.

In this section, we only consider the medium access aspects of protocol and suggest an approach for ultra-low duty cycles. This amounts to minimizing synchronization overhead, connection setup etc. Hence, for the rest of the section, unless specified, we assume the BLE PHY. The results are not exclusive to BLE, and can be extended to all of the protocols, and can potentially be implemented in all the standards with minor modifications.

### 4.3.1 Asynchronous Transmission Protocol

As we saw in Section 4.2, synchronization overhead can lead to power consumption not scaling down to the leakage/sleep power of the radios, providing an opportunity for $10 \times$ (in commercial) to $1000 \times$ (in research radios) reduction in average power consumption.

The reconnect-BLE approach requires no synchronization, but has connection setup and closing overhead. Our approach is to use an asynchronous essentially-transmit-only protocol with hooks for improved Quality of Service (QoS). This is essentially an unslotted ALOHA protocol and the literature on this can be used to analyze it. The high-level protocol is as follows:

1. **Asynchronous Transmit**: The sensor node sends out its data in an asynchronous fashion. The time of transmission is determined by a local timer that is unsynchronized with the base-station, leading to lower accuracy specifications, saving power. For example, the timer shown in Sec. 2.4.2 could be used as a sleep-mode timer. The base-station is always listening on the channel, and is guaranteed to pick up the transmitted packet unless there is packet collision or interference.

2. **Optional ACK**: The sensor node, depending on the perceived importance of a packet can optionally not request an ACK from the base-station. This reduces
4.3. PROPOSED PROTOCOL FOR ULTRA-LOW DUTY CYCLES

the number of packets in the air by $2 \times$ and also saves power in the sensor node. An example of a situation with no-ACK is a temperature sensor in a factory that is reporting normal behavior.

3. **Repeat Transmission:** For important packets with high QoS requirements, the ACK is requested. If no ACK is received, the packet was lost either because of noise or packet collision. The sensor node retransmits its packet after a random time offset in order to avoid repeat collisions. This ensures the packet reception. In addition, if there is an event that causes multiple sensors to be triggers simultaneously, the randomized time offsets improve packet reception.

4. **Long Payloads:** Certain sensors might need to send a long stream of data to the base station. In this case, operation in the same channel is problematic because the long stream might collide with multiple other sensors. In this case, the first packet only sends a request for a dedicated communication window in a separate channel, and the ACK allots this. The actual payload is then communicated in the separate channel. This is essentially the connected mode of BLE or the TDMA scheduled slots of 802.15.4

Frequency Division Multiple Access (FDMA) is also typically used in wireless systems to make use of the full bandwidth of the available spectrum. One use of FDMA is to spread the sensor nodes across the various channels in the band, thereby reducing collisions in each individual channel. Protocols such as BLE apply frequency hopping in order to overcome channel fading (where some channels have higher path loss). Thus, FDMA can also be applied in the asynchronous transmission protocol to reduce both collisions and to overcome fading.

5. **Node Reconfiguration:** The sensor node periodically sets its ACK flag in order to ensure some guaranteed packet transmission. The sensors can also get feedback from the base-station about its channel characteristics in order to ad-
just output power, as well as other node reconfiguration commands. Depending
on the size of the communication, this might occur in a separate channel, or as
part of the ACK itself.

4.3.2 Average Power Consumption Comparison

The energy consumed and average power of a typical sensor node in each interval is
given by:

\[ E_{\text{interval}} = P_{\text{sleep}} \cdot T_{\text{sleep}} + P_{\text{TX}} \cdot T_{\text{data}} \]  \hspace{1cm} (4.7)

\[ P_{\text{avg}} = P_{\text{sleep}} + P_{\text{TX}} \cdot \frac{T_{\text{data}}}{T_{\text{interval}}} \]  \hspace{1cm} (4.8)

where \( T_{\text{sleep}} \approx T_{\text{interval}} \) at low duty cycles.

Figure 4-3 shows the modeled power consumption of commercial BLE radios with
various packet intervals (proxy for duty cycle) with the various protocols. Figure 4-4
shows the power consumption for a system using performance from research chips
(Chapter 2 and [59]). In addition to the power of transmission and reception, the
model also includes power consumed in frequency settling and calibration.

It can be seen that the 32 second limit on \( T_{\text{sleep}} \) in the connected mode of BLE
doesn’t affect the power for commercial radios. This is because the knee of the curve
occurs at around 10 second packet intervals. On the other hand, with the research
radios, the knee of the curve is at packet intervals around 200 seconds. Here, removing
the 32 second restriction can give about 33% reduction in power at low duty cycles.

However, overall, the transmit only protocol, being asynchronous is very effective
in reducing power across all duty cycles, reaching the leakage power levels of the
chips. In addition, timing accuracy requirements of the timer is relaxed.

In Figure 4-5, we analyze the case of an 802.15.4 style packets built using research
prototype specifications. The individual packets are longer because of the lower bit
rate (250kbps). For the baseline 802.15.4, a beacon interval of 100ms is chosen, and
the nodes transmit data using a CSMA scheme. The node waits for the beacon to synchronize, it then transmits at a random time in the beacon interval, and receives an acknowledgment. Majority of the energy is consumed for synchronization. We see than the transmit-only approach can save about $10\times$ in power.

Finally, Figure 4-6 considers an ultra narrowband (UNB) application built with research-prototype specification. We consider a datarate of 1kbps. As discussed in Section 4.2.4, such low datarates are useful for sparse networks requiring very long range. As shown in the figure, due to the long packet lengths (200ms in this plot), the average power is not affected by the guard intervals even for long packet intervals (up to 1hr). Hence, in these UNB use-cases, a connected mode of operation might be preferable, since it allows for larger number of nodes as well (as will be shown in Section 4.3.3)
Figure 4-4: Comparison of power consumption of a sensor node using research radios using BLE in connected mode, reconnect mode and a transmit-only protocol.

Figure 4-5: Comparison of power consumption of a sensor node using research radios using 802.15.4 style packets.
4.3. PROPOSED PROTOCOL FOR ULTRA-LOW DUTY CYCLES

Figure 4-6: Comparison of various protocols in a long range, low datarate UNB system

4.3.3 Network Capacity Comparison

The network capacity is limited by the packet collisions. The probability of successful packet reception is given by:

\[ p_{\text{success}} = \exp\left(-2 \cdot N \cdot \frac{t_{\text{packet}}}{t_{\text{interval}}} \right) \]  \hspace{1cm} (4.9)

where \( N \) is the number of nodes. Therefore, for a given required probability of success, the number of nodes supported by the network is given by

\[ N_{\text{max,tx-only}} = \frac{\log(1/p_{\text{success}}) \cdot t_{\text{interval}}}{2 \cdot t_{\text{packet}}} \]  \hspace{1cm} (4.10)

The calculation is similar for reconnected-BLE approach, but with longer \( t_{\text{packet}} \).

For the connected-BLE protocol and similar fully-scheduled protocols, the network
can be continually scheduled, leading to

\[ N_{\text{max,connected}} = \frac{t_{\text{interval}}}{3 \cdot t_{\text{packet}}} \]  (4.11)

where the factor 3 comes from the combination of a beacon, data packet and acknowledgment.

The network utilization for the asynchronous protocols, is:

\[ \text{Util} = \log(\frac{1}{p_{\text{success}}}) \]  (4.12)

This comes out to about 5% for 0.9 probability of success and 11% for 0.8 probability of success for each individual transmissions. Given these network utilization numbers, it can be seen that pruning down the communication from a full “reconnect-BLE” approach to an asynchronous transmit-only scheme can be greatly beneficial (for not just the power consumption of the node).

The connected-BLE protocol, and similar fully-scheduled protocols, can theoretically occupy the network continuously. But, this doesn’t translate to a network utilization of 100%, since each transaction involves three packets, including the beacon, sensor data and the ACK. Thus, the network utilization is at most 33%. But, in the baseline BLE protocol, this is only true if the restriction on the maximum \( T_{\text{sleep}} \) is removed. When \( T_{\text{sleep}} \) is limited to values lower than 32 seconds, the duty cycling is limited, and leads to a saturation on the number of nodes supported. The network utilization then tends to zero if the intrinsic application duty cycle reduces.

Figure 4-7 compares various protocol options in terms of the number of supported nodes. The calculations assume 1Mbps communications using BLE packets. It also assumes that only two BLE channels are used. For the connected and reconnected BLE case, one channel is used for advertisements while the other is used for data communications. For the TX-only protocol, both channels are used for asynchronous communication. It is also interesting to note that in the reconnected-BLE case, only
4.4 Conclusions

In this chapter, we considered wireless sensor applications operating at very low duty cycles. We looked at various existing wireless protocols and analyzed power consumption and network capacity. One of the key efforts is to minimize protocol overhead at low duty cycles, and reach an average power consumption limited by standby power. This is achieved by avoiding the need for accurate clocks in the sensor node and eliminating guard time requirements. In addition, a predominantly

![Comparison of network capacity for various protocols](image)

Figure 4-7: Comparison of network capacity for various protocols

the advertisements and initial connection request packets are asynchronous, while the rest of the communication happens in a scheduled time slot on a separate channel.

For UNB protocols, this analysis will be similar, but the number of nodes will be a scaled version because of the low datarates. But, they also occupy lesser bandwidth.
transmit-only protocol is shown to help reduce power by further reducing the duration for which the sensors are active.
Chapter 5

An RC Oscillator with Comparator OffsetCancellation

For low duty cycle systems operating with fully asynchronous protocols such as the transmit-only approach discussed in Chapter 4, oscillators such as the gate-leakage oscillator of Sec. 2.4.2 or transistor-$V_t$-based oscillators like [67] are sufficient and result in power consumption under 10pW. On the other hand, if the application needs a high-accuracy kHz-range oscillator dictated by the use of beacon-based protocols, other alternatives are needed.

5.1 High Accuracy Oscillators for Protocol Timing

The necessity for high-accuracy oscillators are made clear in the operation of slave sensor nodes in connected-modes of Bluetooth Low Energy (BLE) or 802.15.4 networks, especially at low duty cycles. These sensor nodes wake up periodically to receive beacons to synchronize transmissions. However, due to the potential inaccuracy of its clock, the receiver needs to be turned on for a guard time before the actual

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1The work presented in this chapter is in collaboration with Danielle Griffith, Alice Wang and Gangadhar Burra
beacon in order to ensure reliable reception. This guard time $t_{\text{guard}}$ is given by:

$$t_{\text{guard}} = p \cdot t_{\text{interval}}$$  \hspace{1cm} (5.1)$$

where $p$ is the fractional frequency inaccuracy in the timer and $t_{\text{interval}}$ is the packet interval. Since the full receiver is on during this guard time, at low duty cycles (or large $t_{\text{interval}}$), the energy is dominated by this guard time. This limits the average power of the system [68]. There is a tradeoff between spending higher power towards a more accurate oscillator (resulting in lower guard time) on the one hand and spending lower power in a less accurate oscillator (resulting in higher guard time) on the other hand. Wireless systems typically use 32kHz crystal oscillators since they provide some of the best tradeoffs, with high accuracy and low power, with some recent works such as [24] showing power consumption below 6nW. However, the external component results in significant board area and cost concerns, motivating the need for a fully-integrated replacement. One potential solution was demonstrated in [25] where a silicon-based resonator is integrated with the CMOS circuits to achieve an excellent $\pm 2$ppm temperature accuracy and $0.4\,\mu$W power. In this work, however, we explore fully-integrated RC oscillators as an alternate low-cost solution.

### 5.1.1 Oscillator Requirements

In Eqn. 5.1, timing inaccuracy of the timer, $p$, has three main sources. a) temperature, b) supply voltage and c) timing noise. Only transient sources of inaccuracies are considered since process variation related inaccuracies can be removed with a one-time calibration. Overall, $p$ can be expressed as:

$$p_{\text{total}} = p_{\text{temperature}} + p_{\text{voltage}} + p_{\text{Allan-at-}t_{\text{interval}}}$$  \hspace{1cm} (5.2)$$

where the timing noise component is captured by the Allan deviation [69] at the given measurement duration (or averaging time) $t_{\text{interval}}$. Allan deviation improves
5.1. HIGH ACCURACY OSCILLATORS FOR PROTOCOL TIMING

with increasing averaging of the white noise process. Eventually, at large averaging times, the Allan deviation stops improving and is limited by flicker noise.

Before discussing the core-oscillator design, we first consider system-level techniques that can improve on the intrinsic voltage and temperature inaccuracies of the oscillator. Supply voltage variation can be mitigated through the use of voltage regulators, either explicitly, or implicitly in the oscillator structure itself [70]. Temperature variations can be mitigated by the use of temperature sensors and look-up-table based frequency compensation [47]. A second approach to mitigate temperature variation is to periodically wake up a higher-accuracy (and higher power) oscillator to measure and compensate the lower power oscillator [71, 72]. Timing noise, being random, however, cannot be calibrated out.

In this work, we present a fully-integrated RC oscillator particularly focusing on improvements to intrinsic temperature and noise performance.

5.1.2 Integrated RC Oscillators, Design Tradeoffs and Previous Work

Fig. 5-1 shows the basic architecture of an RC oscillator [73]. The scheme shown has a key advantage that it doesn’t rely on absolute accuracy of the current source, which nominally eliminates a key source of uncertainty from the system. The period is equal to $RC + t_{\text{delay}}$ where $t_{\text{delay}}$ is the delay of the comparator. The key tradeoffs for low-power and high accuracy design are: a) The voltage swing can be reduced with low $I$, but, in the face of comparator offset, which is temperature dependent, a given offset affects the period by a larger fraction. This leads to worse temperature variation. b) Similarly, the input-referred noise as well as current source noise also leads to a larger effective timing noise. c) Low power consumption of the comparator, especially with offset constraints, results in finite speed, and variation in this speed due to temperature can now result in variation in the period. d) At low values of current source $I$, the temperature dependent leakage currents in the switches can
Figure 5-1: A basic RC oscillator topology and associated timing diagram.

have larger fractional effect on the period.

Alternate RC oscillator topologies use the exponential RC-time constant-settling response [70, 74, 75], and have similar tradeoffs with respect to power consumption, voltage swing, comparator offsets, delays as well as noise.

Offset has been previously identified as the key bottleneck in the tradeoffs discussed above [75–78]. If offset is canceled, low swing operation is made feasible, and comparator design is eased, ultimately reducing power. The voltage-averaging feedback scheme of [75] is effective for MHz oscillators, but will require very large passive filters if scaled down to the kHz range. The self-chopped offset compensation schemes in [76] and [78] result in excellent performance, but consume higher power due to biasing circuits. The offset and delay compensation of [77] has an excellent scheme for compensating comparator offset and delay and also operates at low power (400nW at 33kHz), but requires two comparators, presenting the opportunity for further savings. In this work, we present an RC oscillator architecture with a new offset cancellation scheme that requires only a single comparator, allows low swing, low power operation and achieves 4× to 25× temperature variation reduction. The architecture also has noise canceling properties, resulting in about 10× Allan deviation reduction.

An additional tradeoff is the choice of resistor. Temperature variation of the
resistor results in variation of the period. Works such as [74,77,79,80] have shown that two resistor types with opposing temperature coefficients can be combined to achieve high overall accuracy. In this work, we use nominally temperature compensated polyresistors provided by the process itself.

Finally, the design and tradeoff in the current reference used in an oscillator can vary depending up on the value of the required currents. Higher frequency oscillators that consume power in the µW range might use bandgap-based current and voltage references [81]. However, lower power oscillators avoid these by, for example, making the frequency nominally independent of these factors as in [73]. For currents in the tens of nA and higher, constant-$g_m$ current sources (such as in [76]) and threshold-referenced bias circuits (such as in [77]) are used. As the current values decrease, the values of the resistor used in the reference increases. Thus, to avoid area penalty, at even lower currents in the sub-nA regime, higher valued current references are duty-cycled (in the tens of pA regime in [82]), or gate leakage in thin-oxide devices is used (as in [47] and in the 32Hz oscillator design in Sec. 2.4.2). In this chapter, the oscillator is designed for the tens of kHz regime for wireless protocol timing applications, and the power budget allows the use of a simple constant-$g_m$ current reference, and will be shown in Sec. 5.3.4.

These previous oscillator designs and their performance are tabulated in Tab. 5.1.

5.1.3 Outline of Chapter

In Sec. 5.2, the architecture along with its operation are presented. Analysis of the offset and noise cancellation properties are discussed along with analysis of the effects of component matching. Sec. 5.3 discusses the design and tradeoffs of individual circuit blocks in the oscillator. Sec. 5.4 presents measurement results for a testchip fabricated in a 65nm CMOS process.
5.2 Offset Cancellation Oscillator Architecture

Fig. 5-2 shows the architecture of the offset-canceling oscillator. It has a timing circuit, a continuous time comparator and a Schmitt trigger. The timing circuit includes two matched current sources $I$, two matched capacitors $C$ and a resistor $R$. We first describe the nominal operation and then discuss process variation, temperature stability and noise performance.

5.2.1 Nominal Operation

Fig. 5-3 shows the nominal timing. The circuit operates in two phases. In phase $\phi = 0$, node $V_2$ sets a reference voltage of $I \cdot R$ at the negative terminal of the comparator. Node $V_1$ ramps up and triggers the comparator when the voltage crosses $I \cdot R$ which then flips the phase of operation, making $\phi = 1$. Small glitches at the output of the comparator during phase change are eliminated with the Schmitt trigger. The operation during phase $\phi = 1$ is symmetric, with $V_2 = I \cdot R$ and $V_1$ ramping. The
duration of each phase, and the total period of oscillation is given by:

\[ t_{\text{phase}} = R \cdot C + t_{\text{delay}} \]

\[ t_{\text{period}} = 2R \cdot C + 2t_{\text{delay}} \]

where \( t_{\text{delay}} \) is the delay of the comparator and Schmitt trigger circuits. In order to ensure that the passives determine the period and the temperature stability for the oscillator, it is desirable to have high-speed operation of the comparator, by minimizing \( t_{\text{delay}} \).

### 5.2.2 Effect of Mismatch and Process Variation

Process variation in the values of \( R \) and \( C \) can directly affect the period based on Eqn. 5.4, but can be compensated with a one-time calibration. Process variation in \( I \) does not nominally impact the period, however it can affect voltage swings \((= I \cdot R)\) and comparator bandwidth, and can again be one-time calibrated. Mismatch variations in the values of \( C \) and \( I \), however, need to be considered carefully. Finally, mismatch in the comparator leads to offset, which also affects period. All these mismatch and process variation effects are analyzed below.

Fig. 5-4 shows the circuit diagrams for two phases of operation in the presence of mismatch. Fig. 5-5 shows the waveforms and timing for this. The two current sources
are \( I_1 \) and \( I_2 \), the capacitors are \( C_1 \) and \( C_2 \) and the comparator offset is \( V_{os} \). The duration of the two phases, and the total period are:

\[
\begin{align*}
  t_{\phi=0} &= (I_2 R + V_{os}) \cdot \frac{C_1}{I_1} + t_{\text{delay}} \\
  t_{\phi=1} &= (I_1 R - V_{os}) \cdot \frac{C_2}{I_2} + t_{\text{delay}} \\
  t_{\text{period}} &= \left[ \frac{RC_1 I_2}{I_1} + \frac{RC_2 I_1}{I_2} \right] + V_{os} \left[ \frac{C_1}{I_1} - \frac{C_2}{I_2} \right] + 2t_{\text{delay}}
\end{align*}
\] (5.5)

(5.6)

(5.7)

Now, rewriting this assuming mismatch fractions of \( \pm \alpha, \mp \beta \) around nominal values of \( C, I \) [or, \( C_1 = C(1 + \alpha) \) and \( C_2 = C(1 - \alpha) \), \( I_1 = I(1 - \beta) \) and \( I_2 = I(1 + \beta) \)]:

\[
\begin{align*}
  t_{\phi=0} &\approx RC \left[ 1 + \alpha + 2\beta + 2\alpha\beta + \frac{V_{os}}{IR} (1 + \alpha + \beta + \alpha\beta) \right] + t_{\text{delay}} \\
  t_{\text{period}} &\approx 2RC \left[ 1 + 2\alpha\beta + \frac{V_{os}}{IR} (\alpha + \beta) \right] + 2t_{\text{delay}}
\end{align*}
\] (5.8)

(5.9)

Thus, we see that with well matched components, the effect of offset on the overall period is significantly attenuated as compared to the durations of the individual phases, where offset directly affects them without any attenuation. For example, even with modest mismatch numbers such as \( \alpha + \beta = 5\% \), the effect of offset is attenuated by \( 20\times \). Simulations of the implemented circuit at nominal operation indicate up to \( 100\times \) reduction in offset-dependence. This demonstrates the offset canceling timing architecture.

Because \( R \) is shared between the two phases, there is no mismatch term for this, improving robustness of the oscillator. Using a single shared resistor also saves die area. In addition, for processes where low temperature coefficient resistors are not available, a single external resistor is sufficient. Resistor sharing between the two phases is feasible because, during phase-change, only the current needs to be switched between \( I_1 \) and \( I_2 \) (which are themselves well matched).

Capacitor mismatch \( \alpha \) directly affects offset cancellation, and it could be desirable to use the same capacitor for both phases of oscillations. However, unlike with resistor, during change of phase, the capacitor needs to be discharged to \( 0V \) before the current
Figure 5-4: Operation of the RC oscillator under mismatch, showing the circuit for the two phases
sources are switched. This requires more complex timing with separate small-time-
constant pulse generation circuits, as done in [73]. Such an alternative was not chosen,
in order to avoid extending \( t_{\text{delay}} \) and its temperature and process dependencies. In
addition, because of the use of large capacitors, and with common-centroid layout,
the mismatch \( \alpha \) can be kept small.

### 5.2.3 Temperature Variation

The sources of temperature variation for the oscillator are the temperature variation of
the resistor, the capacitors, switch matrix \((S_1 - S_6)\), comparator offset and comparator
delay. Capacitors are implemented as metal-oxide-metal (MOM) capacitors, and thus
have negligible temperature variation. The on-chip resistors in this work have a
special zero-temperature coefficient design, where the linear temperature dependence
is removed, giving low overall temperature dependence. An alternative is, as shown in
previous work such as [77,79], to use two resistors of different temperature coefficients
and cancel their effects. A third alternative is to use one low temperature coefficient
external resistor.

The switches \( S_1 - S_6 \) have finite on-resistance and off-leakage, which in turn change
with temperature and can thus affect the period of oscillations. Sec. 5.3 will discuss
the detailed design considerations for the switches in this design.

Given low temperature coefficient of the intrinsic RC time constant, it is critical to ensure that the rest of the circuit does not start to dominate the overall performance. The comparator is designed with constant-\(g_m\) biasing in order to achieve constant bandwidth across temperature and thus, constant comparator delay. The delay of the Schmitt trigger and buffers is designed to be much smaller than the delay of the comparator itself. Temperature variation in the comparator offset is attenuated by the factor \((\alpha + \beta)\) through the offset cancellation scheme. This significantly relaxes the requirements for offset in the comparator design, making it easier to build a low-power high-speed comparator. More of the circuit design is described in Sec. 5.3.

The impact of offset in Eqn. 5.9 is also a function of the swing \(I \cdot R\), where larger swing implies more robustness. However, because of the offset cancellation architecture, a low-swing design is feasible\(^2\), thus significantly reducing power consumption. For example, in this work, a swing of only 150mV is used. If offset varies by 10mV across temperature, when no offset-cancellation is applied, the frequency varies by as much as 6%. However, with offset-cancellation, simulations indicate that this is attenuated by 100\(\times\) to 0.06\%\(^3\).

### 5.2.4 Noise and Allan Variance

Long-term variations in the period of oscillation occur due to the low frequency noise sources in the current sources \(I_1\) and \(I_2\), in the comparator and the resistor. Flicker noise in \(I_1\) and \(I_2\) result in variation of \(\beta\)\(^4\). The duration of each phase of the oscillator offers no attenuation to the noise (Eqn. 5.8), but its effect on total period variation is attenuated by the capacitor mismatch factor \(\alpha\). Flicker noise in the comparator trans-

\(^2\)The impact of offset on the total period in Eqn. 5.9 is a factor \((\alpha + \beta)\) lower than the impact of offset on the phase duration in Eqn. 5.8. Thus, the oscillator can now be operated with low swings.\(^3\)Simulations are performed with artificially applied offset to an ideal comparator in order to capture only the offset-cancellation aspects of the design. In reality, temperature dependence of \(R \cdot C\) delay as well as \(t_{\text{delay}}\) will limit amount of cancellation.\(^4\)This results from flicker noise in the current mirror transistors. Flicker noise in the PTAT reference itself manifests as common-mode variation in \(I\), and has a negligible effect on the period.
lates to long-term variation of the offset of the comparator $V_{os}$, which is attenuated by the offset-cancellation scheme. Resistor noise results in variation in the $i_{\text{noise,rms}} \cdot R$ reference noise, but, this is not differential between the two phases, and is thus not canceled by the offset cancellation scheme. However, since the noise is white, this is averaged out, and long-term Allan deviation is unaffected.

Thus, overall, the architecture is robust to noise sources, and can result in excellent long-term Allan deviation results.

### 5.2.5 Summary of Design Considerations

The architecture of the oscillator allows significant power reduction as a result of the following design choices:

1. The architecture requires only one comparator.

2. The design of the comparator requires optimization of gain and bandwidth with only weak constraints on the offset and flicker noise performance. This results in low-power comparator implementations.

3. Given the attenuation of offset and its variation with temperature, the architecture allows low swings ($I \cdot R$), thereby allowing operation at low currents.

### 5.3 Circuit Design and Tradeoffs

In this design, $R=5\,\text{M}\Omega$ and $C=5\,\text{pF}$ for an RC time constant of $25\,\mu\text{s}$, giving a nominal frequency around 20kHz (Eqn. 5.4). The charging current $I$ is 30nA, for a swing of only 150mV.

#### 5.3.1 Switch Matrix

We now look at the design of the switch matrix $S_1 - S_6$. Discharge switches $S_5 - S_6$ discharge the capacitors. These switches are sized for low leakage, while the resistance
requirement $R_{sw} << R (=5M\Omega)$ is easily met since $V_{GS, on, S_{5-6}} = V_{DD}$. Leakage of $S_{5-6}$ is important because this leakage, which is exponential with temperature, diverts current from charging the capacitor $C$, affecting timing.

Switches $S_{3-4}$, when off, operate at $V_{GS, off, S_{3-4}} = -I \cdot R$, thus have reduced leakage (by up to $30\times$), which is thus negligible. However, when on, $V_{GS, on, S_{3-4}} = V_{DD} - I \cdot R$, and the comparator trigger voltage has an error of $I \cdot R_{S_{3-4}}$. Temperature variation of this voltage error can lead to frequency variation.

Switches $S_{1-2}$ are the most stringent in their design. When off, $V_{GS, off, S_{1-2}} = 0$, and when on, they have a voltage error arising from the finite switch resistance. Overall, if the voltage error from $S_{1-2}$ is equal to the voltage error of $S_{3-4}$, timing is unaffected, but switch resistance differences as low as $5k\Omega$ can lead to a frequency error of $0.1\%$. Similarly, if the leakage of $S_{5-6}$ is equal to the leakage of $S_{1-2}$, timing is unaffected, but, leakage mismatch as low as $30pA$ can lead to frequency error of $0.1\%$. Thus, the switches need to be optimally sized and matched.

Since $V_t$ varies with device length and width [40, 83], careful sizing can be used to help meet the switch resistance and leakage requirements described above. This is in addition to the use of the various device flavors available in the process. In this work, the technology chosen was able to provide the necessary switch matrix design such that their resistance and leakages do not affect timing.

However, an alternate switch matrix design using a 4-point probe (or Kelvin connection) as shown in Fig. 5-6 could be utilized to relax the requirements and ease the design process. The resistance constraints on switches $S_{1-4}$ are eliminated. Switches $S_{7-10}$ multiplex voltages onto the comparator and do not conduct current\(^5\).

\(^5\)This technique was brought to our attention during the Q and A session at the conference presentation of this work at [26]
5.3.2 Comparator

The comparator used in this design is shown in Fig. 5-7. The primary requirements are low current, high bandwidth and constant delay across temperature, while secondary requirements are low-offset. The comparator needs to handle low common-mode voltages around 150mV.

A PMOS input pair topology is chosen due to the low input common-mode voltage required. Sub-threshold operation and constant-$g_m$ biasing (with PTAT current biasing) leads to nominally constant bandwidth across temperature, and consequently, constant delay. The nominal delay of the comparator is designed to be about 100ns, or 0.4% of the period. The comparator consumes about 50nA, with 30nA in the first differential stage, and the average current of the second stage about 20nA. In addition. Additionally, both statistical and systematic variations in the offset are minimized through common-centroid layout and careful sizing of the second stage, respectively.
5.3. **CIRCUIT DESIGN AND TRADEOFFS**

5.3.3 **Schmitt Trigger and Buffers**

The Schmitt trigger and inverter-chain buffers make the edge from the comparator sharp, and give strong rail-to-rail outputs. The delay of these is about 10ns, and is much smaller than the comparator delay, and thus doesn’t affect overall oscillator performance. The current consumption of these buffers is also lower than 10nA.

During the change of phase, when nodes $V_1$ and $V_2$ switch roles, in order to prevent potential glitching, the Schmitt trigger stage is used. Shown in Fig. 5-7, weak high-$V_t$ transistors are added to provide a small hysteresis (10s of mV in simulations).

5.3.4 **Current Source**

The PTAT current reference for the oscillator is shown in Fig. 5-8a [84]. This current reference is designed to supply currents to other blocks in the system including LDOs, and thus operates from the I/O supply voltage of 1.65V to 3.3V. It includes a 5MΩ reference resistor and has a quiescent current of 25nA, while generating an output current of 10nA. Long-length, and wide devices are used to improve matching, and results in a Monte-Carlo mismatch variation of ±0.5nA.
25 nA Quiescent

(a) Implementation of the current reference

(b) Mismatch-only Monte Carlo simulations showing 1nA accuracy in current source. Plotted is the current in each branch of the reference.

Figure 5-8: Implementation and Monte Carlo simulations for the PTAT current reference
5.4 Measurements

The oscillator was fabricated in a 65nm CMOS process. The die photograph is shown in Fig. 5-9. The RC oscillator occupies an area of 0.032mm² while the current reference occupies as additional 0.073mm². The PCB used for testing is shown in Fig. 5-10.

5.4.1 Nominal Performance

The oscillator core operates from a 1V supply. The current reference is designed to operate off a battery voltage of 1.5V–3.3V in order to supply currents to other blocks of a wireless SoC, including battery management blocks and LDOs etc. The current reference draws 25nA, and provides a PTAT current reference with a nominal output of 10nA. Fig. 5-11 shows the measured PTAT performance of the current source in the −40°C to +90°C range.

The oscillator core itself consumes 130nA, with 30nA each consumed by the cur-
CHAPTER 5. RC OSCILLATOR WITH OFFSET CANCELLATION

Figure 5-10: Testboard for the RC Oscillator. It includes on-board regulators, level-shifters and connection to an FPGA board.

Figure 5-11: Measured current source output as a function of temperature showing PTAT behavior.
rent sources charging the R and C, 50nA in the comparator, 10nA in the Schmitt trigger and the buffers and 10nA in the current mirror from the current reference.

Fig. 5-12 shows the period of the oscillator as the on-chip R and C are tuned digitally. It shows linear relationship of the period to linear increase in R or C. The frequency can be tuned from 9kHz up to about 30kHz. The nominal frequency of the oscillator is chosen at the mid-range, at 18.5kHz. All temperature and noise measurements are performed at this operating point.

The voltage variation of the oscillator is plotted in Fig. 5-13 for 4 measured chips. The chips have variation around 0.4%/V up to about 5%/V for the worst-case chip. However, since the total variation is lower than ±0.12% across 50mV, only a coarse-regulated LDO/power supply is needed to maintain constant frequency. For example, the architecture of [70] includes a coarse voltage regulator to significantly improve the voltage accuracy of the oscillator.

Because there are no long time-constant bias voltages in the oscillator, the startup-time is low. Fig. 5-14 shows the measured startup transient of the oscillator. Both the current source and oscillator enable signals are turned on simultaneously. The oscillator period settles in 4 cycles. If the current source is already enabled, the settling time reduces to 2 cycles.

### 5.4.2 Temperature Variation

Experiments for temperature variation were performed for 4 chips to characterize the resistor temperature variation and the offset cancellation. All measurements were performed across the temperature range of −40°C to +90°C unless otherwise specified.

Fig. 5-15 shows the performance with on-chip temperature compensated resistors, while the temperature variation of replica resistors is plotted in Fig. 5-16a. The resistors have very low temperature variation, below ±0.19% across the full temperature range. The temperature variation of the period of oscillation of the 4 chips are
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Figure 5-12: Measured tuning range of the oscillator period with digitally tuned R and C. The frequency tunes from 9kHz up to 30kHz.

Figure 5-13: Variation in period of oscillator with supply voltage for 4 chips.
Figure 5-14: Startup time of the oscillator shows the period settling in 4 cycles. Both the current source and oscillator enables are turned on simultaneously.

Figure 5-15: Temperature variation of oscillator period measured for 4 chips
CHAPTER 5. RC OSCILLATOR WITH OFFSET CANCELLATION

Figure 5-16: Measured contribution due to the resistors variation as well as the contribution of the rest of the circuits.
±0.18%, ±0.225%, ±0.25% and ±0.55%. If the temperature variation of the resistor is subtracted from that of the period, the resulting temperature variation is plotted in Fig. 5-16b. We see that the residual temperature variation is still about the same (±0.19% to ±0.6%), though the shape changes. This indicates that this variation is intrinsic to the oscillator structure itself.

Fig. 5-17 compares the temperature variation of the total period versus the variation of the positive phase of the oscillator. This shows the effect of offset cancellation technique (Eqn. 5.8 versus Eqn. 5.9). Again, 4 chips are measured. The duration of each phase of the oscillator has a variation as large as ±7%. The improvement due to offset cancellation varies from 4× to as high as 25× between the chips. This strongly shows the benefit of the offset cancellation scheme, especially at the low swings (and current levels) used in this design.
Finally, a copy of the oscillator with Nwell resistors instead of the temperature compensated resistor is characterized in Fig. 5-18. The variation is as high as ±2.6%. This shows the importance of temperature compensation of the resistor itself.

5.4.3 Allan Deviation

Typically, Allan deviation measurements are carried out using specialized frequency counter equipment such as [85]. These have high accuracy, with Allan deviation noise floor as low as 1ppb or 0.01ppb at averaging time \( \tau = 1s \). For this work, we implement a custom FPGA-based solution for continuous capture of frequency measurements at programmable averaging time values. The implementation is shown in Fig. 5-19. The oscillator from the DUT, Osc\textsubscript{IN}, is retimed to the reference clock CLK\textsubscript{HF} (either the 48MHz system clock or a 288MHz PLL output). A synchronous divider creates the measurement intervals, each of \( 2^{N\text{div}} \) cycles of Osc\textsubscript{IN}. A 26-bit counter counts the
5.4. MEASUREMENTS

Figure 5-19: FPGA-based design for Allan deviation measurement. Continuous timing windows are measured with a high frequency counter and the data is post-processed in Matlab.

The number of CLK$_{HF}$ cycles in each measurement window, and pushes the count value to a FIFO. At the same time, the counter is reset in order to start counting for the next window, thereby ensuring continuous measurements. In addition, the system provides a means for gating the counter during the 0-phase of the oscillator. This mode allows the measurement of the Allan deviation of the oscillator without offset cancellation.

Fig. 5-20 shows the measured noise floor of the Allan measurement setup. It uses a 48MHz crystal oscillator as CLK$_{SYS}$ and a 1MHz crystal oscillator as the input Osc$_{IN}$. When the 288MHz PLL output is used, the Allan deviation floor at low values of $\tau$ are $6\times$ lower, but the long term stability, at 30ppb is determined by the crystal oscillators. This noise floor can be improved by using more accurate frequency references such as OCXO (oven-controlled crystal oscillator), but is sufficient for the
Figure 5-20: The Allan deviation measurement noise floor for the setup in Fig. 5-19 is 30ppb.

Figure 5-21: Allan deviation for the oscillator with and without offset compensation shows that the circuit attenuates noise as well.
5.4. MEASUREMENTS

RC oscillator measurements to follow.

The long-term Allan deviation of one of the chips is plotted in Fig. 5-21. For short averaging intervals, the white frequency noise process is apparent ($\tau^{-0.5}$ trend) while flicker frequency noise leads to flattening ($\tau^0$ trend). For the full period (capturing offset cancellation) at averaging intervals $\tau > 1s$, the Allan deviation is better than 20ppm. However, for just one phase of the oscillator, due to no offset cancellation, the flicker frequency noise flattens out at around 200ppm. As discussed in Sec. 5.2.4, the oscillator is more resilient to current source noise as well as comparator flicker noise, leading to the $10\times$ improvement.

Shorter-term Allan deviation measurements were performed for the 4 chips across temperature, from 0°C to +90°C. Fig. 5-22 plots it for averaging interval of $\tau=2s$. It shows that the Allan deviation stays below 35ppm across the 4 chips and across the temperature range, indicating high accuracy timing measurements for wireless systems.

![Figure 5-22: Allan measurements for 4 chips across temperature at $\tau=2s$](image-url)
Finally, jitter measurements using an oscilloscope are correlated with Allan deviation to verify the measurements. Fig. 5-23 shows the $1\sigma$ jitter at various averaging times and the value estimated from the Allan deviation, showing good match. The estimate was calculated using:

$$1\sigma \text{ jitter} \approx \tau \cdot \text{Allan deviation} \quad (5.10)$$

### 5.4.4 Comparison

Table 5.1 summarizes this work and compares it with previously published integrated oscillators operating in various frequencies. In addition to RC oscillators, also compared are alternate oscillator topologies that are referenced to electron mobility [86], ring oscillators with special biasing [71, 81], and ultra-low-frequency oscillators that use gate leakage [47].
Table 5.1: Comparison to previous fully integrated oscillators

<table>
<thead>
<tr>
<th>Ref</th>
<th>Tech. (nm)</th>
<th>Area (mm$^2$)</th>
<th>Freq. (kHz)</th>
<th>Power (nW)</th>
<th>Temp. Accu. (%)</th>
<th>Temp. Range (°C)</th>
<th>Volt. Accu. (%/V)</th>
<th>Allan Floor (ppm)</th>
<th>Start up Cycles</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>[87]</td>
<td>350</td>
<td>0.09</td>
<td>5000</td>
<td>20000</td>
<td>±0.7</td>
<td>−20 / +60</td>
<td>4</td>
<td>-</td>
<td>10$^7$</td>
<td>RC-based linear-ramp</td>
</tr>
<tr>
<td>[73]</td>
<td>350</td>
<td>0.1</td>
<td>3.3</td>
<td>11</td>
<td>±1.2</td>
<td>−20 / +80</td>
<td>6</td>
<td>-</td>
<td>-</td>
<td>RC-based linear ramp</td>
</tr>
<tr>
<td>[74]</td>
<td>65</td>
<td>0.03</td>
<td>6000</td>
<td>66000</td>
<td>±0.5$^a$</td>
<td>0 / 120</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Dual poly temp compensation</td>
</tr>
<tr>
<td>[82]</td>
<td>130</td>
<td>0.019</td>
<td>0.011</td>
<td>0.100</td>
<td>±3</td>
<td>0 / +90</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>Duty-cycled current source</td>
</tr>
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<td>[70]</td>
<td>65</td>
<td>0.015</td>
<td>33</td>
<td>190</td>
<td>±0.21</td>
<td>−20 / +90</td>
<td>0.09</td>
<td>4</td>
<td>-</td>
<td>RC-exponential-based Local voltage regulation</td>
</tr>
<tr>
<td>[47]</td>
<td>130</td>
<td>0.01</td>
<td>0.0004</td>
<td>0.66</td>
<td>±0.13$^a$</td>
<td>−20 / 60</td>
<td>420</td>
<td>50$^b$</td>
<td>-</td>
<td>Self-chopped offset compensation</td>
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<td>[76]</td>
<td>60</td>
<td>0.048</td>
<td>32.768</td>
<td>4500</td>
<td>±0.1</td>
<td>−20 / 100</td>
<td>0.12</td>
<td>-</td>
<td>-</td>
<td>Gate-leakage based</td>
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<td>[79]</td>
<td>90</td>
<td>0.12</td>
<td>100</td>
<td>280</td>
<td>±0.68</td>
<td>−40 / +90</td>
<td>5.7</td>
<td>-</td>
<td>1</td>
<td>Dual poly temp compensation</td>
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<td>[77]</td>
<td>180</td>
<td>0.105</td>
<td>32.55</td>
<td>470</td>
<td>±0.84</td>
<td>−40 / 100</td>
<td>1.1</td>
<td>-</td>
<td>3</td>
<td>Offset, delay compensation Dual resistor temp compensation</td>
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<td>[86]</td>
<td>65</td>
<td>0.11</td>
<td>100</td>
<td>40800</td>
<td>±1.1 (3σ)</td>
<td>−22 / +85</td>
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<td>-</td>
<td>1000</td>
<td>Mobility-based reference</td>
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<td>31.25</td>
<td>360</td>
<td>±25$^a$</td>
<td>−45 / +80</td>
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<td>-</td>
<td>-</td>
<td>RC-based linear-ramp</td>
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<td>[78]</td>
<td>130</td>
<td>0.073</td>
<td>3200</td>
<td>38200</td>
<td>±0.25</td>
<td>20 / 60</td>
<td>4</td>
<td>140</td>
<td>-</td>
<td>Self-clocked offset cancellation</td>
</tr>
<tr>
<td>[75]</td>
<td>180</td>
<td>0.04</td>
<td>14000</td>
<td>45000</td>
<td>±0.19</td>
<td>−40 / 125</td>
<td>1.6</td>
<td>&lt;26$^c$</td>
<td>14</td>
<td>Offset compensation with voltage-averaging feedback</td>
</tr>
<tr>
<td>[81]</td>
<td>250</td>
<td>-</td>
<td>7000</td>
<td>1500000</td>
<td>±0.84</td>
<td>−40 / 125</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>Ring oscillator with temperature compensation</td>
</tr>
<tr>
<td>[80]</td>
<td>350</td>
<td>0.162</td>
<td>130</td>
<td>3700</td>
<td>±0.5</td>
<td>−20 / 100</td>
<td>0.4</td>
<td>-</td>
<td>-</td>
<td>Dual poly temp compensation</td>
</tr>
<tr>
<td>[71]</td>
<td>130</td>
<td>0.25</td>
<td>100</td>
<td>150</td>
<td>±0.035$^a$</td>
<td>20 / 70</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Low power ring oscillator periodically calibrated</td>
</tr>
<tr>
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<td>65</td>
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<td>18.5</td>
<td>130</td>
<td>±0.18 to ±0.55</td>
<td>−40 / +90</td>
<td>&lt;5</td>
<td>20</td>
<td>4</td>
<td>Offset cancellation and temp. compensated resistor</td>
</tr>
</tbody>
</table>

$^a$ Estimated from ppm/°C  
$^b$ Estimated from 1 hour timing uncertainty  
$^c$ Estimated from jitter data
5.5 Conclusions

In conclusion, an offset cancellation scheme has been presented that helps achieve temperature stability of $\pm 0.18\%$, ultra-low power operation at 130nW and long-term stability of better than 20ppm, advancing the state of fully-integrated timers for wireless sensors.
Chapter 6

A Low Power Transmitter with Digital Network Coding

Coding techniques improve the reliability of communication and enhance range. In low duty cycle systems, coding can be applied to help reduce the output power requirements of the transmitters, which results in reduced leakage power, assuming a fixed on/off ratio (see Chapter 2). Coding involves introduction of redundancy in order to recover from errors.

Depending on the type of errors, there are two commonly used coding techniques. Forward Error Correction (FEC) codes [89] are a physical layer (PHY). Here, a packet of $k$ information bits is mapped to an $n$-bit packet, resulting in an effective code rate of $r = k/n$ and a lower packet error rate. An example of FEC codes is convolutional codes. Typically, FEC can correct random errors arising from channel noise. However, if there are bursty errors, packets might not be recoverable.

Apart from FEC codes, communication reliability can be further improved by the use of erasure codes [90]. Classical erasure schemes, which were initially introduced for the binary erasure channel, can be applied for packet-based correction techniques as well. According to this coding approach, cross-packet redundancy is introduced.

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1This work is in collaboration with Georgios Angelopoulos and Prof. Muriel Médard
For instance, $K$ packets are encoded into $N$ coded packets, resulting in an effective transmission rate of $R = K/N$. As long as any set of $K$ out of the $N$ packets are received, the initial information can be recovered. These schemes are usually implemented in the network layer. In this chapter, we consider Digital Network Coding [91] along with its interplay with FEC codes in the form of Random Linear Network Coding (RLNC) and Joint Channel and Network Coding (JCNC).

## 6.1 Network Coding for Star Networks

Previous work on network coding techniques have shown bandwidth reduction in multihop networks. Routing of multicast data flows, in particular, have been shown to benefit from network coding at the intermediate nodes in the network [91]. As discussed in Chapter 4, multihop networks are energy inefficient for low duty cycle systems because of the protocol overhead. In this chapter, we consider network coding benefits for single-hop communication in star network topologies.

One such work is [92], which shows that network coding can help minimize the number of acknowledgments to be received by the sensor node. This was shown in contrast to Automatic Repeat Request (ARQ) schemes. A second work, such as [93], uses network coding as a basis for a rateless code for broadcast transmissions. In this chapter however, only unicast transmissions are considered.

We consider the use of redundancy provided by network coding as a channel code, and thus its use in star networks. We experimentally evaluate how it can be used to improve communication reliability at low SNRs. In particular, we demonstrate a low-power digital baseband that includes a network coding engine. This is co-designed with an ultra-low power $-10\text{dBm}$ transmitter for short range wireless systems such as Body Area Networks (BANs). All the experimental evaluations are performed in indoor environments.
In the RLNC scheme used in this work, encoded packets are produced as linear combinations of the initial packets, where the coefficients are randomly selected. When enough linearly independent coded packets are received at the destination node, the decoding process can be done, and the initial packets recovered. Clearly, if there are packet erasures, as long as enough packets are received, all the packets are recovered.

Assume that $K$ packets have to be transmitted ($P_1, P_2, ..., P_K$), each of them containing $L$ bytes\[^2\] of data ($P_1 = \{p_{11}, p_{12}, ..., p_{1L}\}$), as shown in Fig. 6-1. The encoding process creates $N$ coded packets ($P'_1, P'_2, ..., P'_N$), where $N \geq K$, according to the equation:

$$p'_l = \sum_{j=1}^{K} p_{jl} \times c_{ij},$$  \(\text{Eq. (6.1)}\)

where $1 \leq l \leq L$ and $1 \leq i \leq N$ and $c_{i,j}$ are randomly selected coefficients, appended in headers of transmitted packets. Using matrix notation, the encoding process is

---

\[^2\]In this case, the finite field $GF(2^8)$ is used. In general, a packet can be segmented into symbols of $q$ bits each, making use of $GF(2^q)$. 
described as:

\[ P' = C \times P. \] (6.2)

where \( P \) is the matrix of initial packets, \( C \) the matrix composed of the sets of coefficients and \( P' \) the matrix of coded packets. At the destination, receiving any \( K \) out of the \( N \) transmitted packets is enough to recover the initial packets. The decoding process consists of the inverse process; inverting the coefficients matrix \( (C') \) and multiplying it by the coded packets. Receiving any \( K \) out of the packets is sufficient, as long as the coefficient matrix is invertible. For large finite fields, this is true with a very high probability. In this work, only the fixed-rate versions are considered, as opposed to rateless schemes [93].

6.2.1 Choice of \( K \) for RLNC

The probability of successfully decoding a packet in RLNC equals the probability of receiving at least \( K \) coded packets. Assuming \( p_e \) is the erasure probability, the packet error rate can be calculated as:

\[
PER_{RLNC} = 1 - \sum_{i=K}^{N} \binom{N}{i} p_e^{N-i} (1 - p_e)^i
\] (6.3)

According to Eqn. (6.3), for given \( p_e \) and code rate, \( PER_{RLNC} \) reduces exponentially with increasing \( K \). However, delay constraints and memory requirements of low-power sensors dictate that \( K \) cannot be made large. Larger memories on the sensors increase power consumption as well as the cost of the system. In addition, the overhead of the coefficients in each transmitted packet is \( 1 + \frac{K}{L} \), and thus, higher \( K \) can start to effect overall rate, as well as worsen \( p_e \).

For the design of our custom implementation of an RLNC accelerator, \( K \) of value 4 is chosen.
6.3. LOW POWER TRANSMITTER WITH FEC/RLNC/JCNC ENCODER

6.3.1 RLNC Encoder

The block diagram of the RLNC encoder, implementing equation (6.1), is shown in Fig. 6-3. It is a fully parallel implementation, calculating one symbol of a coded
packet every clock cycle. In this case, four packets are coded together \((K = 4)\). The incoming symbols are multiplied with the coefficients, produced by Linear Feedback Shift Registers (LFSRs). The LFSRs are initialized by appropriate values in order to ensure that the generated coded packets are linear independent. The coded output symbol is directly connected to the next block, ready for additional FEC coding or transmission.

All operations of RLNC are performed over finite fields or Galois Fields \((GFs)\). This propriety guaranties that the result of any operation has the same length as the initial operands; thus the coded packets will have the same length as the initial ones. Assume \(A(x)\) and \(B(x)\) are two \(GF\) elements; their sum is equivalent of the bit-wise
6.3. LOW POWER TRANSMITTER WITH FEC/RLNC/JCNC ENCODER

XOR of their polynomial representation:

\[ S(x) = A(x) \oplus B(x) \]  \hspace{1cm} (6.4)

Multiplication is a two step operation composed by polynomial multiplication followed by modulo reduction:

\[ P(x) = (A(x) \times B(x)) \mod g(x) \]  \hspace{1cm} (6.5)

where \( g(x) \) is the primitive polynomial of the field. In our design, we implement a bit-parallel low-power multiplier using the standard representation basis and primitive polynomial \( g(x) = [1, 0, 0, 0, 1, 1, 0, 1] \).

6.3.2 Packetizer and FEC Encoder

The next block after the RLNC engine is the packetizer. In this block, the RLNC coded packet is further encoded by a multi-rate FEC convolutional encoder of constraint length 4 at one of the coding rates: 1, 3/4, 1/2 and 1/3. Before the FEC, a 16-bit CRC is calculated and attached to the packet along with the appropriate trellis termination bytes. Finally, the packet is interleaved and a sync word and preamble are added before it is passed to the RF block for transmission. The design generates one bit per cycle. The parameters for CRC, preamble and sync word are compatible with CC2511 [94] in order to perform over-the-air experiments.

Fig. 6-4 shows the packet format. The packet length is configurable up to 64 bytes of payload. Also, since the RLNC encoder and packetizer/FEC encoder are in series, JCNC is obtained by simply configuring both blocks appropriately.


6.3.3 Low Power Digital Design

Low power design techniques are used in order to achieve minimum energy operation. Near-threshold voltage scaling is applied. In order to ensure such low-voltage operation for the entire design, the 2Kb memory needed for the 4 packets are designed using flip-flops instead of SRAMs. The encoder is measured to be functional down to 0.35V, resulting in \( \times 10 \) power savings. In addition, clock gating is used to reduce dynamic power and custom level-shifters are implemented to interface with other voltage domains, including the RF block and IO.

6.3.4 RF Transmitter

The transmitter used in this work is a single-channel version of [33]. It uses a single high-Q Film Bulk Acoustic Resonator (FBAR) to define a single channel of operation in the 2.4GHz ISM band. The resonator is configured as an oscillator, and the high-stability of the resonant frequency eliminates the need for a PLL. The transmitter also includes a PA optimized for low output power around \(-10\)dBm. Overall, the transmitter consumes 550µW from a 0.7V supply. The transmitter supports up to 1Mbps FSK modulation, since the FBAR-oscillator supports a tuning range of 600kHz. A 6-bit capacitor bank is used to perform the frequency modulation with a step-size of 9.5kHz.
6.3. LOW POWER TRANSMITTER WITH FEC/RLNC/JCNC ENCODER

Figure 6-5: Architecture for the pulse shaping block.

Figure 6-6: The impulse response of the Gaussian filter used and error from the ideal filter.

6.3.5 Pulse Shaping for GFSK

However, since FSK modulation produces side-bands in the spectrum, it is highly desirable to reduce this emission to improve interoperability in the busy 2.4GHz ISM band. At the same time, in a low-power TX, it is important to keep the energy overhead of the pulse shaping low. Fig. 6-5 shows the implemented architecture for Gaussian pulse-shaped FSK (GFSK) with BT product = 0.3. Fixed coefficients are used to reduce the FIR filter to simple shift and add operations. The coefficients
and the $5 \times$ oversampling speed are chosen as a trade-off between power and spectral efficiency through Matlab simulations. Fig. 6-6 shows the coefficients used, along with the error with respect to an ideal $5 \times$ oversampled filter. The sum of coefficients is designed as a power of 2 (512 in this case) so that the inputs to the FIR filter can be the required max and min capacitor bank settings. The lower bits of the FIR filter are dropped before driving the oscillator.

### 6.3.6 Block Level Measurements

The chip is implemented in 65nm CMOS. The $2\text{mm} \times 1.3\text{mm}$ chip is co-packaged with an FBAR resonator in a 44-pin QFN package. The chip die photo is shown in Fig. 6-7.

The DNC engine and packetizer consume only $15 \mu W$ for 1Mb/s data rate, when operating at 0.4V. The RF section consumes $550 \mu W$ for FSK modulation with -10dBm output power for an energy efficiency of 550pJ/bit at 1Mb/s. The FIR filter for 1Mb/s GFSK consumes $15 \mu W$ from a 1V supply, running off a 5MHz clock.
6.3. LOW POWER TRANSMITTER WITH FEC/RLNC/JCNC ENCODER

![Spectrum Diagram]

Figure 6-8: Spectra for 1Mbps FSK and GFSK showing 28dB reduction in the second side-lobe.

Table 6.1: Summary of measurements

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>65nm</td>
</tr>
<tr>
<td><strong>Datarate</strong></td>
<td>1Mb/s</td>
</tr>
<tr>
<td><strong>Modulation</strong></td>
<td>FSK, GFSK</td>
</tr>
<tr>
<td><strong>DNC and Packetizer</strong></td>
<td></td>
</tr>
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<td><strong>Supply</strong></td>
<td>0.4V</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>15µW</td>
</tr>
<tr>
<td><strong>Pulse Shaping</strong></td>
<td></td>
</tr>
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<td><strong>Supply</strong></td>
<td>1V</td>
</tr>
<tr>
<td><strong>Power</strong></td>
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</tr>
<tr>
<td><strong>RF</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Supply</strong></td>
<td>0.7V</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>550µW</td>
</tr>
</tbody>
</table>
Fig. 6-8 shows the spectra of 1Mb/s FSK and GFSK. The first side-lobe is reduced by 11dB and the second by 28dB. The much improved spectral efficiency occurs with only 15pJ/b overhead.

Table 6.1 summarizes the circuit measurement results.

6.4 Experimental Setup for Over-the-air Measurements

The experimental evaluation and performance comparison of PHY-layer FEC, RLNC and JCNC is done through careful and controlled experiments. The setup is shown in Fig. 6-9. The transmitter IC with the encoder circuits is used as the sensor node. It is controlled by a Matlab program on a PC through an FPGA. A generic commercial transceiver (Texas Instruments CC2511 [94]) is used to receive the data from the transmitter. A transmission data rate of 500 kbps is used for all our measurements, which is limited by the maximum supported data rate of the CC2511 receiver. FSK modulation is employed for data transmission and coherent demodulation is performed at the receiver; hard Viterbi decoding and an interleaver of 4 bytes length are also used.

A PC-based packet sniffer software transfers the data from the CC2511 over a USB interface. This software then sends the received data over to the Matlab program which then computes the packet error rate.

The CC2511 chip provides the Received Signal Strength Indicator (RSSI), which is a good proxy for the SNR on the channel. In the rest of this section, improvements in RSSI and improvement in SNR values will be used interchangeably\(^3\).

\(^3\)This is reasonable because an improved SNR due to coding leads to an improved RSSI at which reliable communication is measured. This is because RSSI is the measurement available.
6.4. EXPERIMENTAL SETUP FOR OVER-THE-AIR MEASUREMENTS

Erasure Coding
Channel Coding
RF
Digital Attenuator
CC2511 Commercial RX

Data
SNR Setting

FPGA

Matlab PER Calculation
Packet Sniffer Application

PC

Figure 6-9: Simplified block diagram of our experimental setup. The transmitter IC with integrated JCNC encoder transmits data to a commercial receiver dongle, connected with a PC for decoding and statistics collection.
In order to perform detailed PER measurements and estimate coding gains, the SNR of the received signal needs to be changed. The intrinsic output power tuning on the transmitter is limited (about 7 dB), and it is not possible to physically move the devices apart in a repeatably accurate manner. To overcome this issue, a digitally controlled RF attenuator is connected between the transmitter IC and the antenna. A 31 dB dynamic range, with 1 dB/step [95] provides a very repeatable method of sweeping the SNR of the channel. For each setting of the attenuator and code rate, $10^3$ packets are transmitted, each of 48 bytes length.

### 6.5 Over-the-air Packet Error Rate Measurements

In this Section, the performance of the PHY-layer FEC, RLNC and JCNC schemes based on our measurement in a typical indoor environment is presented and discussed.

#### 6.5.1 Performance of PHY-layer FEC and RLNC Operating Separately

The error correction performance of the PHY-layer FEC code is shown in Fig. 6-10. The measured PERs for different code rates are plotted. A PHY-layer FEC of code rate 3/4 provides only a marginal improvement over uncoded data transmission, while FEC of code rate 1/2 provides approximately 2.25 dB SNR improvement. Use of a PHY-layer FEC code with rate 1/3 offers only a small additional coding gain compared to the rate 1/2 code; as expected, increasing the redundancy of the FEC code provides diminishing returns in the coding gain.

Fig. 6-11 shows the performance of RLNC for several code rates, when no PHY-layer FEC code is used. At a PER of $10^{-2}$, its effective SNR improvement is 2.5 dB and 3.4 dB for the 4/6 and 4/8 code rate, respectively. For reference, the PER curve of the PHY-layer FEC of rate 1/2 is also plotted in the same figure with dashed line. Comparing the PER curves of the two coding schemes in Figs. 6-10 and 6-11, a very
6.5. OVER-THE-AIR PACKET ERROR RATE MEASUREMENTS

![Figure 6-10: Measured packet error rate (PER) curves for a convolutional (FEC) code of rate = 3/4, 1/2 and 1/3 compared with uncoded packets’ transmission.]

The difference in the PER curves for the two coding schemes can also be explained by examining the behavior of the wireless channel in typical indoor environments. For a
AWGN channel with fixed and known SNR, PHY-layer FEC codes can be designed to communicate packets reliably, as long as their transmission rate is below the capacity of the channel. In that case, packet-level erasure codes are not necessary. On the other hand, for an erasure channel, in which packets are either received entirely correct or completely erased, a packet-level erasure code (such as RLNC) can be sufficient to provide the necessary reliability, making a physical layer code unnecessary.

In reality, although noise is always present in the wireless channel causing random bit errors within a packet, its effects are more pronounced in the low SNR regime and these random errors are better corrected by the convolutional codes. At higher SNR levels, the intrinsic bit error rate is negligible. However, interference from nearby networks operating at the same frequency band becomes the dominant limiting factor, creating packet collisions with large burst errors and making the channel behave like a block fading channel. This is particularly true in the 2.4GHz ISM band, where a large variety of networks coexist, including WiFi (802.11), BLE, 802.15.4. In addition, indoor environments also see interference from appliances such as microwave ovens. In this case, RLNC performs better by introducing a longer dependency across packets.

Interference itself could be reduced through techniques such as carrier-sense, but because the transmitter is optimized for ultra-low power sensor applications, it does not include this capability. Additionally, because of the varied range of standards and communication ranges, carrier-sense may not be as effective in eliminating interference. For example, 802.11 uses output powers as high as +15dBm while our transmitter only does –10dBm for short-ranges.

Ultimately, we thus see that depending on the SNR levels and the environment, the channel sees a combination of random noise based bit errors and interference-based packet erasures. This motivates the Joint Channel and Network Code (JCNC) as a means to tackle both and significantly improve performance.
6.5. OVER-THE-AIR PACKET ERROR RATE MEASUREMENTS

Figure 6-11: Measured packet error rate (PER) curves for random linear network coding (RLNC) of rate = 4/5, 4/6 and 4/8 compared with uncoded packets.

6.5.3 Performance of JCNC

The performance of the joint channel-network coding (JCNC) scheme is shown in Fig. 6-12. According to our measurement results, JCNC of effective rate 1/3 performs better than the PHY-layer FEC code of the same rate by approximately 1 dB at PER of $10^{-2}$. However, at the very low SNR regime, the PHY-layer FEC code has the best performance because, as explained earlier, use of RLNC requires successful reception of at least $K$ packets for a block to be decoded. This graph confirms the synergy between PHY-layer FEC codes and RLNC in a joint coding scheme. As is shown, the coding gain of joint PHY-layer FEC and RLNC is 5.6 dB for an effective code rate 1/4. Table 6.2 summarizes the effective SNR improvements for different PHY-layer FEC and RLNC code rates at two target PERs.
Figure 6-12: Measured packet error rate (PER) curves for the joint channel-network coding (JCNC) scheme.
Table 6.2: Effective SNR improvement for the JCNC scheme.

<table>
<thead>
<tr>
<th>FEC Rate</th>
<th>RLNC Rate</th>
<th>SNR improvement</th>
<th>PER= 10^{-1}</th>
<th>PER=10^{-2}</th>
</tr>
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<tr>
<td>1</td>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
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<td>1.5dB</td>
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<td>2.25dB</td>
<td>4dB</td>
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<td>4/8</td>
<td>3.5dB</td>
<td>5.6dB</td>
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6.6 Summary

Modern low power indoor sensor networks have to communicate their information under strict resource constraints, usually operating in the overpopulated ISM frequency band. In this chapter, we study the use of random linear network coding (RLNC) in sensor applications as an erasure code for improved data reliability. RLNC introduces redundancy across several packets and can offer a significant advantage to sensor networks operating in severe interference environments. However, in the low SNR regime, random bit errors overwhelm this packet-level erasure code and the use of a PHY-layer FEC becomes important. For this reason, we also study a joint channel-network coding (JCNC) scheme, examining the synergy between a convolutional code and RLNC. We perform measurements in a typical office environment using a custom sensor node, integrating on-chip a low power 2.4 GHz transmitter and an accelerator implementing both PHY-layer FEC and RLNC. The results show that RLNC provides an effective coding gain of 3.4 dB, outperforming the PHY-layer FEC code of the same code rate, at a PER of 10^{-2}. In addition, it performs well when used in conjunction with the PHY-layer code as a JCNC scheme, offering an overall
coding gain of 5.6 dB.
Chapter 7

A Digital Baseband supporting Spinal Coding, BLE and 802.15.4

Spinal coding is a recent error correcting scheme developed at MIT [31] and has been shown to perform close-to-Shannon capacity. They spread apart the code words with hash functions, and operate as a rateless code. The hash function is sequentially applied to \( k \)-bits of the input message at a time, and this produces a randomization of the resulting coded output. For example, any mistake in decoding of one of the bits will result in a statistically independent result for all the output bits to follow.

In this chapter we present a hardware implementation of fixed-rate Spinal Codes for use in low-power wireless systems employing simple modulation schemes such as FSK/OOK. This spinal encoder hardware has been integrated with a complete transmit-PHY digital baseband for BLE and 802.15.4. The entire baseband has been designed as part of the complete transmitter described in Chapters 2 and 3. This chapter explores the design of this complete baseband.

Previous work in hardware implementation of Spinal codes has been on FPGAs [96] and for WiFi-like OFDM modulation-based systems. Previous work in fully

\[1\]

The work presented in this chapter is in collaboration with Peter Ianucci, Nathan Ickes and Prof. Hari Balakrishnan
integrated digital baseband designs include [97], where both the transmit (60μW) and receiver (140μW) baseband circuits are implemented for BLE, 802.15.4 and 802.15.6 standards. In this chapter, the design of the transmit portions of the digital baseband for BLE, 802.15.4 and Spinal coding are presented.

### 7.1 Spinal Coding

Fig. 7-1 explains the concept of spinal coding and how the hash function is successively applied to the input bits $k$-bits at a time. These hash outputs are called the spine. In this implementation, the hash-function output is a 32-bit number. In the rateless-mode, bit-slices of the spine are transmitted one after the other until successful communication. Thus, in this base-mode, the various rates feasible are:

$$\text{rate} = \frac{k}{n}, \quad n \in [k+1, 32] \quad (7.1)$$

In our implementation, $k$ is either 2 or 4, thereby giving spinal code rates up to 1/16 or 1/8. Fig. 7-1 also shows the scalability of the encoding to add even more redundancy. This is accomplished by using the spine as a seed for a Random Number Generator (RNG), which is itself a slight modification of the same hash function. In
our implementation, we support one application of the RNG to obtain spinal code rates up to $1/32$.

### 7.1.1 Fixed-rate Mode of Operation

According to simulations performed in [31], the fixed-rate schemes perform worse than rateless versions of the spinal codes with about 2-3dB SNR degradation for a given bit rate. However, for very short packets, typical of sensor nodes, if rateless modes are used, the overhead of a worst-case synchronization and preamble size could be large. But, with fixed-rate modes, an optimally sized synchronization word and preamble could be chosen. In addition, as will be shown in Sec. 7.2.3, the fixed-rate version leads to significant reduction in memory requirements for the encoder.

### 7.2 Digital Baseband Design

The digital baseband design is implemented for integration with the BLE transmitter from Chapter 2. In addition to BLE, the digital baseband supports 802.15.4 transmit-PHY and also incorporates a fixed-rate Spinal Encoder. The complete specifications of the two standards can be found in [62] and [28]. The complete block diagram is shown in Fig. 7-2.

The data memory holds up to 64 bytes of the input data. The data is read out by one of two encoders. The convolutional encoder implements rates 4 rates 1, 2/3, 1/2, and 1/3. The spinal encoder encodes at rates from 4/5 down to as low as $1/32$. A Cyclic Redundancy Check (CRC) block snoops memory reads and calculates the CRC of the data. Two CRC polynomials, corresponding to BLE (24-bit value) and 802.15.4 (16-bit value) are computed. This CRC output is read in by the spinal/convolutional encoders at the end of the blocks/packets for encoding before sending out to the next block. The CRC initialization register is configurable depending on the standard used.
BLE requires a data whitener block that XORs the input data with a known pseudo-random sequence in order to eliminate long stretches of ones or zeros. The PRBS is generated by a fixed 7-bit LFSR polynomial, however, the initialization is a function of the channel number used. The data whitener block does not change the length of the bit stream.

Next, preamble and sync word bit sequences are added to the bit stream. BLE uses an 8-bit preamble (either 10101010 or 01010101) while 802.15.4 uses a 32-bit preamble of all zeros. BLE includes a 64-bit sync word, while 802.15.4 only uses a 8-bit sync word. BLE uses the sync word for packet type identification (in advertisement packets) or for the unique-ID of the transmitter (in the connected mode). On the other hand, 802.15.4 uses header data to encode such information. Our implementation optionally includes up to 256 bits of LFSR-based preamble and sync word for use with spinal codes in low-SNR regimes.

The next block in the system is for spreading codes. 802.15.4 uses a rate 1/8 spreading code where 4 bits of the input stream are encoded to a 32-bit sequence through a look-up table. BLE doesn’t use any spreading codes. The chip provides
configurability in the spreading factor with rates 1, 1/2, 1/4 and 1/8 implemented. This spreading code provides the effective whitening of the bit stream for 802.15.4. For use with Spinal codes, our implementation supports separate spreading factors for the preamble and payload components of the packet. Thus, synchronization accuracy can be improved with spreading while payload accuracy can be improved by the spinal coding.

For modulation, BLE uses Gaussian Frequency Shift Keying (GFSK). For the direct modulation transmitter of Chapter 2, the data is directly passed onto a Gaussian filter, similar to the design of Sec. 6.3.5. The output can be passed on to the transmitter. On the other hand, 802.15.4 uses Offset Quadrature Phase Shift Keying (O-QPSK) with half-sine pulse shaping. This modulation has been shown to be equivalent to Minimum Shift Keying (MSK)\(^2\) [98]. Thus, with a transformation of the O-QPSK bitstream into the equivalent FSK bitstream, the same direct modulation transmitter can be used. This transformation is done by the Modulation block.

Finally, the pulse shaping block (enabled for BLE, disabled for 802.15.4) filters the data before connection to the DAC in the direct modulation transmitter. This block is similar in design to the design in Sec. 6.3.5

### 7.2.1 Interconnection Between Blocks

Table 7.1 shows the rates for each of the blocks in the system. It shows the minimum and maximum rate, and the rate for BLE and 802.15.4. It shows that each block sees widely varying amounts of activity and speed of generations of output bits. Thus, it is hard to build a hand-calculated timing schedule for the blocks. Instead, a FIFO-based back-pressure technique is applied [99]. The modulation block sets the rate of output bits (for example, 1 bit every 6 cycles for 1Mbps with 6MHz clock frequency), and pulls bits from its input FIFO. Each block computes as long as there is input

\(^2\)Minimum Shift Keying (MSK) is FSK with the minimum deviation frequency that maintains orthogonality between the two symbols. If the datarate is \(D\), the frequency deviation is \(\Delta f_{\text{MSK}} = \pm D/4\)
data available for it, and there is space in its output FIFO. This way, each block computes data when necessary and automatically operate at the correct rate. The FIFO signals are used to clock gate each individual block, thereby saving power.

Table 7.1: Rates of each block in the digital baseband

<table>
<thead>
<tr>
<th>Block</th>
<th>Min. Rate</th>
<th>Max. Rate</th>
<th>BLE</th>
<th>802.15.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Convolutional Code</td>
<td>1/4</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Spinal Code</td>
<td>1/32</td>
<td>4/5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Data Whitener</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Preamble / Sync Word</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Spreading</td>
<td>1/8</td>
<td>1</td>
<td>1</td>
<td>1/8</td>
</tr>
<tr>
<td>Modulation</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Pulse Shaping</td>
<td>1</td>
<td>6</td>
<td>6</td>
<td>1</td>
</tr>
</tbody>
</table>

7.2.2 System Clock Frequency

In order to support BLE, the digital baseband needs to operate at 6MHz, for 6× oversampled Gaussian filtering of 1Mbps FSK data. Thus, the system clock can be any multiple of 6MHz. For 802.15.4, the datarate is 2Mbps, but doesn’t require filtering, and thus, multiples of 6MHz is still sufficient. In Chapter 2, the system clock is 12MHz, as required by this design.

7.2.3 Spinal Encoder with Low Memory Requirements

The key block for implementation of the spinal encoder is the computation of the hash function. In general, it involves 6 XORs, 16 bit shifts and 10 additions. For the case of \( k = 2 \) or \( k = 4 \), it reduces to 7 additions. The circuit implementation is shown in Fig. 7-3. It uses a single adder, and performs the computation over 7 cycles.
and uses an extra cycle to load data to the whitener block. This is sufficient in this design because of the access to the higher frequency (due to the $6 \times$ clock in the pulse shaping block). Because the spinal coder outputs at least 3 bits per hash, the design uses less than 3 cycles per bit. The use of a single 32-bit adder reduces area.

The scheduling is as shown in Table 7.2.

### Table 7.2: Scheduling of the hash function calculator.

<table>
<thead>
<tr>
<th>Cycle</th>
<th>$Sel_1$</th>
<th>$Sel_2$</th>
<th>$Sel_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

When the fixed-rate spinal code is used, after each hash computation, all the output bits are sent out to the next block, the whitener. And when more than the 32 bits are needed, a second hash is computed (with slightly modified input to the same hardware). No separate memory of the hashes is needed as the entire encoding is performed in a streaming fashion. However, if the rateless version of the spinal codes is used, the hashes need to stored in memory in order to send out various slices when needed. Thus, the fixed-rate spinal code enables a architecture with minimal memory requirements.

### 7.2.4 Low Power, Low Voltage Operation

The baseband is synthesized and place-and-routed using a 1.2V standard cell library. Since the baseband is designed for use in the transmitter architecture of Chapter 2, it
Figure 7-3: Circuit implementation of the hash function used in the Spinal encoder.
7.3. MEASUREMENTS

needs to operate at low voltages (below 0.7V). The place-and-route is performed at
1.2V, 100MHz with a target hold slack of 0.25ns. Later, the standard cells were re-
characterized for 0.65V supply, and timing was verified using Primetime static timing
analysis tools.

Clock gating is enabled in the synthesis tool to ensure that all inactive blocks are
gated. Synthesis reports indicate that clock gating reduces power consumption by
$2 - 3 \times$.

Additionally, in order to ease low-voltage operation, similar to the design of Chapter 6, we use registers to implement the small memory required.

7.3 Measurements

Fig. 7-4 shows the layout of the digital baseband, incorporated into the Transmitter
from Chapter 2. It occupies an area of $300 \mu\text{m} \times 150 \mu\text{m}$. The relative sizing of the
various blocks are shown. The design uses 21k Nand-gate equivalents of logic, a third
of which is occupied by the memory blocks including Data and the Config, indicating
the importance of minimizing the memory requirements of the Spinal encoder. The
spinal encoder itself consumes 3k gates.

Fig. 7-5 shows the power consumption and maximum frequency of operation as a
function of supply voltage. The worst-case operating point is chosen where the spinal
coding rate is highest, and the spreading factor is the lowest. This is the operating
point with the highest number of hashes calculated per unit time. For the target
frequency of 12MHz, the minimum $V_{DD}$ of operation is 0.55V. At 0.7V, the design
works up to a frequency of 30MHz. The power consumption increases from $11 \mu\text{W}$ up
to $45 \mu\text{W}$.

In Fig. 7-6, we show the variation of power consumption with decreasing spinal
coding rate and varying spreading code rate. These experiments are performed with
$k = 2$, and thus the spinal coding rate varies from $2/3$ up to $2/64$, and the mea-
measurements are for $V_{DD}=0.55V$. When the code rate switches from 2/32 to 2/33, all 4 curves see a bump in power consumption. This is because of the extra hash computation in the RNG-stage of the coding. Everywhere else on the graphs, the power reduces with increasing ‘1/spinal rate’ because of the amortization of the hash computations. As the spreading code rate decreases, the power again reduces because the hash computation in the spinal code is more power hungry than the simple look-up table outputs of the spreading encoder block. Overall the power consumption of the block is small (below 11$\mu W$) and shows the efficiency of spinal encoding operations, especially in the fixed-rate modes.
7.3. MEASUREMENTS

Figure 7-5: Power consumption and maximum frequency versus $V_{DD}$. Plotted for spinal rate of 2/3 and with spreading disabled.

Figure 7-6: Power consumption at 12MHz, 0.55V, for varying spinal coding and spreading rates.
7.4 Conclusions

In this chapter, we considered Spinal coding, a new class of error correcting codes that achieve high performance across a wide range of SN Rs. Previous work has shown spinal coding in the rateless mode of operation. In this work, we propose the use of fixed-rate versions of the spinal codes for use in ultra-low-power transmitters. Here, it was shown that fixed-rate implementations have minimized memory requirements. The spinal encoder is incorporated in a highly-configurable digital baseband that also includes support for BLE and 802.15.4. Low power low voltage techniques ensure that the design functions down to 0.55V while operating at the desired frequency of 12MHz. The design consumes less than 11µW.
Chapter 8

Conclusions and Future Directions

This thesis presented various techniques that improve the performance of the wireless communications for Internet of Things (IoT) devices with particular focus on the extremely energy-constrained devices, for example, in industrial monitoring systems. A large number of these systems have also been identified to have low communication duty cycle requirements. In this context, a number of opportunities for power reduction, and consequently lifetime enhancement, have been identified:

1. At low duty cycles, protocol-related overhead is identified as a major bottleneck. Optimizations to wireless protocols can help drive this overhead to a minimum, allowing the devices to only turn on their radios for as little time as possible, which is the amount of intrinsic rate of information production. Even in the context of existing protocols, choice of parameters and modes of operation are shown to have significant effect on RF activity levels.

2. Once protocol overhead is eliminated, chip standby power is the limiting factor. One of the major components of standby power is typically the sleep-mode timer, and depending on the accuracy requirements for the timing, there is great potential for power/cost reductions.

3. The second major component of chip standby power is the intrinsic leakage.
Techniques for leakage reduction in RF circuits that do not effect on-efficiency can thus greatly improve standby power, and hence, average power at low duty cycles.

4. Active power reduction techniques can help reduce peak power requirements on power management circuits and batteries, easing system design.

5. Low voltage RF design can help reduce both RF (switching) power as well as leakage. However, there are significant challenges in the design of blocks such as PLLs and PAs.

6. Wireless coding techniques can help enhance range and reliability of communication systems and can thus reduce peak output power specifications, thus helping reduce leakage (assuming a fixed on/off power ratio). Integration of energy-efficient implementations of state-of-the-art encoders can help demonstrate their applicability in IoT devices.

8.1 Conclusions

8.1.1 Protocol

Analysis of Existing Protocols indicates that the choice of modes of operation can significantly affect power consumption, network utilization, quality of service and maximum number of nodes supported. It is critical to optimize the protocols before making further modifications. At low duty cycles, protocol optimizations can provide up to $10 \times$ power reduction in commercial-off-the-shelf radios and $>100 \times$ improvement when research-prototypes are used.

The (predominantly) Transmit-Only Protocol developed in Chapter 4 has further optimized the protocol with modifications to the baseline protocols. This is achieved with tradeoff between quality of service and power. Power consumption
is linked to the importance of the transmitted data. This shows that existing protocols can be further improved under additional assumptions. Our results indicate up to $4 \times$ increase in network throughput, and up to $4 \times$ decrease in the knee of the power versus duty cycle curve.

8.1.2 Low Power Timers

High Accuracy RC Oscillators have a tradeoff between temperature performance and power consumption. This has been shown to be strongly dictated by the tradeoffs of designing a comparator with high speed, low offset and low power. An offset-cancellation scheme has been developed to break this tradeoff. Temperature variation of the oscillator period was measured to have improvements between $4 \times$ to $25 \times$ among 4 measured chips. Even though the ultimate temperature variation of $\pm 0.18\%$ over $-40^\circ C$ to $+90^\circ C$ is larger than for crystals, elimination of the external component results in cost reductions. The oscillator consumes 120nW for 18.5kHz operation.

If there are guarantees on the range of feasible temperatures at the sensor node, the frequency inaccuracy of the oscillator will have better bounds, making protocol-timing feasible (for example, below the 500ppm requirement of BLE)

A 10pW Gate-Leakage-based Oscillator operating at 32Hz has been presented for use in the sleep-mode for driving the $-\frac{1}{2}$ charge pump for leakage reduction. Such ultra-low power timers can be used for sleep-mode timing as well, if fully asynchronous approaches such as the transmit-only protocol are used. This highlights the great opportunity that exists for power reduction through protocol choices that greatly relax circuit specifications.
8.1.3 High Efficiency, Low Leakage RF

**Low Voltage RF Operation** of the BLE transmitter has been achieved through a combination of techniques. Resonant drives of the PA input as well as resonance in the output matching network help achieve large swing (nearly $2 \times V_{DD}$), thereby maximizing drive and thus, efficiency. Some RF blocks are operated off a 1.2V voltage doubler in order to assist the low-voltage operation of the remaining blocks. For example, 1.2V drive in the digitally tunable capacitor banks helps improve Q for the same parasitic capacitance. Overall, this doubler rail only consumes 100µW (less than 1% of the total power). Finally, the PLL circuits are optimized for low voltage operation through body biasing (for reduction of VCO parasitic capacitance) and dynamic logic design (for the frequency divider).

Ultimately, all the techniques help bring the supply voltage low, enabling power savings through reduced switching power. The lower supply voltage also results in lower leakage power, further aiding low-duty cycle operation.

**Leakage Reduction** for the transmitter has also been achieved through a mix of methods. The PA, being the most power hungry active block, requires the most careful design in order to minimize or avoid any on-performance degradation. Negative voltage biasing of the thin-oxide PA transistor has been identified as the optimal scheme for leakage reduction because of minimal parasitics. Additionally, a minimum-leakage bias point has been identified, at approximately $-200$mV where the tradeoff between decreasing subthreshold current and increasing gate leakage current is optimized. Overall, this scheme can achieve $30\times$ leakage reduction and also shows superior resilience to process and temperature variations. This is mainly attributed to the tighter control of gate leakage as compared to subthreshold current.

All other blocks in the system are power gated with thick-oxide high-$V_t$ power switches. Here, optimal choice of the voltage rails ($V_{NEG}$, $V_{SS}$, $V_{DD}$ and $V_{DOUB}$)
8.1. CONCLUSIONS

available in the system can lead to significant leakage reduction.

An Efficient \(-\frac{1}{2}\) Charge Pump that operates in the hundreds of pA range is
designed to provide the gate leakage current for the PA at the minimum leakage
bias point. Low frequency operation and large charge transfer capacitors are used
to achieve a high current efficiency > 90%.

Overall, a combination of low voltage operation and low leakage design leads to
the BLE transmitter achieving an efficiency of > 43\% when delivering +10dBm
and a standby power of 370pW. This gives an on/off ratio of \(7.6 \times 10^7\), one of the
highest reported for RF circuits.

8.1.4 Coding Techniques

Coding techniques help enhance communication range while keeping the peak power
consumption constant. For point-to-point communication systems with asymmetric
energy budgets, coding techniques with simple encoders, but potentially complex
decoders can be used. In this thesis, we considered Network Coding and Spinal
coding.

Network Coding is implemented as a Random Linear code (RLNC). Over-the-
air packet error rate experiments are performed to compare RLNC, convolutional
codes and a joint code. Measurements show that RLNC can correct for packet
losses due to bursty errors or interference, while convolutional codes correct for
random errors. Overall, measurements show that the joint code performs the best.
Peak SNR improvement of 5.6dB was demonstrated.

Spinal Coding is a hash-function based code, and has previously been shown
to achieve performance close to the Shannon-limit. In this work, an encoder in a
rated-code-mode was developed with optimized on-chip memory requirements to
result in a power consumption of under 11\(\mu\)W.
8.2 Future Directions

We envision plenty of avenues for interesting research in wireless communication for IoT devices including at low duty cycles:

**Wide-Dynamic Range Power Delivery:** The RF transmitter presents a very challenging load to a power delivery system. It draws sub-nA load current in sleep, and draws as high as 36mA in active for a dynamic range close to $10^8$. In order to leverage such a wide dynamic range in the TX, it is critical for the power management to maintain high efficiency over the whole range. Converters such as [100, 101] present techniques for high efficiency over a dynamic range of $10^4$ to $10^5$, and methods to enhance these can be explored.

**Low Leakage RX Implementation:** A receiver is essential for a complete wireless system, and in the context of low duty cycles, it will be interesting to explore low-leakage designs for RX circuits such as LNAs. Again, minimal to no on-performance degradation is desired!

**Integrated Medium Access Control (MAC):** Typical wireless systems employ a microcontroller to run the full protocol stack of, say, BLE or 802.15.4 [12]. This is done in order to support the various modes and corner cases better. However, there is a significant power penalty to this. A potential research avenue is to build an application-specific hardware implementation. For example, for one of the asynchronous modes of BLE or even the TX-only approach of Chapter 4.

**Timing Calibration:** Explore fundamental limitations of timing with the RC oscillator, with added duty-cycled temperature sensor and calibration with high-accuracy RF frequency reference. While systems such as [71, 72] implement such schemes, a theoretical analysis of the the guarantees that such a scheme can provide in terms of long-term stability would be valuable.
8.2. *FUTURE DIRECTIONS*

**Over-the-air System Exploration of Spinal Codes:** The work on Chapter 7 only presented hardware implementation of a very modular digital baseband including a spinal encoder. Experimental verification of the effectiveness of Spinal codes for low-SNR environments when using simple modulation schemes such as FSK/OOK needs to be done. Optimal preamble and sync word choices for the various rates supported by the baseband also can be explored.

Overall, there are tremendous opportunities in the design of system architectures, circuits and protocols for ultra-low duty cycle IoT devices!
Appendix A

Calibrated Measurement of PA Output Power

Measuring output power of the PA accurately is critical for correctly calculating efficiency. The sources non-uniformity of measurements arise primarily due to non-idealities of the cable and connectors connecting the PA output to the spectrum analyzer. Losses in the cable lead to lower power values read by the spectrum analyzer, which leads to underestimated efficiencies. Impedance non-idealities in the cable and connectors lead to non-50Ω presented to the PA. Depending on the length of the cable, this impedance changes, and makes the efficiency measurements not repeatable. Thus, we need a good procedure to calibrate losses and to present a more repeatable impedance to the PA.

Figure A-1: Measurement setup and data for $S_{11}$ shows the effectiveness of the attenuator in presenting an ideal 50Ω load.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>2.4GHz</th>
<th>2.5GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$ w/ Attenuator</td>
<td>−28dB</td>
<td>−28.3dB</td>
</tr>
<tr>
<td>$S_{11}$ w/out Attenuator</td>
<td>−18dB</td>
<td>−19dB</td>
</tr>
</tbody>
</table>
We use a 30dB attenuator [102] with good $S_{11}$ to ensure a known 50Ω input impedance. A three feet SMA cable is used. This is captured by the setup and measured data of Fig. A-1. A network analyzer measured the $S_{11}$ to be better than $−28$dB in the 2.4GHz ISM band. Without the attenuator, the $S_{11}$ was measured to be only about $−18$dB.

The use of the attenuator before the cable ensures $S_{11}$, but the losses need to now be calibrated. This is done by the setup shown in Fig. A-2 where a signal generator outputs a known power level which is then measured by the spectrum analyzer. The data shows a uniform loss of about $−32.8$dB across the 2.4GHz band as well as across input power levels from 0dBm to +10dBm.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>2.4GHz</th>
<th>2.5GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path Loss</td>
<td></td>
<td></td>
</tr>
<tr>
<td>($P_{IN}=0$dBm)</td>
<td>$−32.84$dB</td>
<td>$−32.87$dB</td>
</tr>
<tr>
<td>($P_{IN}=10$dBm)</td>
<td>$−32.87$dB</td>
<td>$−32.89$dB</td>
</tr>
</tbody>
</table>

Figure A-2: Measurement setup for calibration of path loss through the attenuator and cable. The path loss in the 2.4GHz band is $−32.8$dB. The same setup is used for measuring output power of the DUT.

Measurements of the Device Under Test (DUT) are done with same setup, replacing the signal generator with the DUT. True output power is then 32.8dB higher than that reported by the spectrum analyzer, while the $S_{11}$ presented to the DUT is better than $−28$dB.
# Appendix B

## List of Equipment Used

Table B.1: List of key equipment used for the measurements in this thesis

<table>
<thead>
<tr>
<th>RF Equipment</th>
<th>Power Supplies</th>
<th>Oscilloscopes</th>
<th>Miscellaneous</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Generator</td>
<td>Regular Keithley 2400 Sourcemeter</td>
<td>High Speed (up to 2.5GHz)</td>
<td>FPGA platform Opal Kelly XEM3001 and XEM6001</td>
</tr>
<tr>
<td>Spectrum Analyzer</td>
<td>Regular Keithley 2602A Sourcemeter</td>
<td>Low Frequency (500MHz)</td>
<td>Thermal Chamber TPS Tenney Series 942</td>
</tr>
<tr>
<td>Network Analyzer</td>
<td>Leakage Measurement Keithley 6430 sub-fA Sourcemeter</td>
<td>Low Frequency (500MHz) Tektronix TDS5054B</td>
<td>GPIB to USB Keithley KUSB-488B</td>
</tr>
<tr>
<td>Phase Noise</td>
<td></td>
<td>Digital Phosphor Tektronix TDS3054B</td>
<td></td>
</tr>
</tbody>
</table>
Appendix C

List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWGN</td>
<td>Additive White Gaussian Noise</td>
</tr>
<tr>
<td>BLE</td>
<td>Bluetooth Low Energy</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>CSMA</td>
<td>Carrier Sense Multiple Access</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DNC</td>
<td>Digital Network Coding</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>ETSI</td>
<td>European Telecommunications Standards Institute</td>
</tr>
<tr>
<td>FBAR</td>
<td>Film Bulk Acoustic Resonator</td>
</tr>
<tr>
<td>FCW</td>
<td>Frequency Control Word</td>
</tr>
<tr>
<td>FEC</td>
<td>Forward Error Correction</td>
</tr>
<tr>
<td>FIFO</td>
<td>First In First Out</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency Shift Keying</td>
</tr>
<tr>
<td>GFSK</td>
<td>Gaussian Frequency Shift Keying</td>
</tr>
</tbody>
</table>
APPENDIX C. LIST OF ACRONYMS

GF  Galois Field
GIDL Gate Induced Drain Leakage
IoT Internet of Things
ISM Industrial Scientific and Medical
JCNC Joint Channel and Network Code
LO Local Oscillator
LTN Low Throughput Network
MAC Medium Access Control
MIM Metal Insulator Metal
MOM Metal Oxide Metal
MSK Minimum Shift Keying
O-QPSK Offset Quadrature Phase Shift Keying
OCXO Oven Controlled Crystal Oscillator
OFDM Orthogonal Frequency Division Multiplexing
OOK On Off Keying
OSSS Orthogonal Sequence Spread Spectrum
PA Power Amplifier
PER Packet Error Rate
PFD Phase Frequency Detector
PHY Physical layer
PLL Phase Locked Loop
ppb Parts per billion
ppm Parts per million
PTAT Proportional To Absolute Temperature
QAM Quadrature Amplitude Modulation
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN</td>
<td>Quad Flat No Lead</td>
</tr>
<tr>
<td>QoS</td>
<td>Quality of Service</td>
</tr>
<tr>
<td>RLNC</td>
<td>Random Linear Network Code</td>
</tr>
<tr>
<td>RNG</td>
<td>Random Number Generator</td>
</tr>
<tr>
<td>RSSI</td>
<td>Received Signal Strength Indicator</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System on a Chip</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time Division Multiple Access</td>
</tr>
<tr>
<td>TSPC</td>
<td>True Single Phase Clock</td>
</tr>
<tr>
<td>UNB</td>
<td>Ultra Narrowband</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>XOSC</td>
<td>Crystal Oscillator</td>
</tr>
</tbody>
</table>
APPENDIX C. LIST OF ACRONYMS
Bibliography


[38] “CC2520: Second generation 2.4 GHz ZigBee/IEEE 802.15.4 RF transceiver,” Texas Instruments, 2007.


