Highly Scaled Silicon Field Emitter Arrays with Integrated Silicon Nanowire Current Limiters

by

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To my Poppy.

[Quantum mechanics] describes nature as absurd from the point of view of common sense. And yet it fully agrees with experiment. So I hope you can accept nature as She is – **absurd.**

– Richard P. Feynman

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Abstract

Field emitter arrays (FEAs) are a promising class of cold electron sources with applications in RF amplifiers, terahertz sources, lithography, imaging, and displays. FEAs are yet to achieve widely implemented because of serious challenges which have limited their viability in systems that require advanced electron sources. We identified four major challenges that posed significant barriers to the application of field emitter arrays in systems. These challenges are (1) charge injection and breakdown of the insulator between the emitter and the extraction gate, (2) thermal runaway due to Joule heating or micro-plasma discharge, (3) back-ion bombardment resulting in emitter tip damage (4) large capacitance between the gate and the substate that limits switching performance.

In this thesis, we address these challenges with a new device architecture that consists of a sharp silicon emitter atop a silicon nanowire embedded in a dielectric matrix of SiO_2 and SiN_x. The 10-μm tall, 200-nm diameter silicon nanowire limits current and improves reliability through velocity saturation and the pinch-off of majority carriers. The 2-μm thick SiO_2 insulator between the gate and the substrate and the conformal dielectric matrix that embeds the nanowire current limiters prevents charge injection and minimizes the capacitance between the gate and the substrate. Since the nanowire current limiter is fabricated directly underneath each field emitter, we maintain an emitter density of 10^8 emitters/cm^2, enabling high current density. The design of the anode prevents tip erosion from back-streaming ions.

These arrays demonstrate consistent current scaling of array sizes from a single emitter to 25,000 emitters, low voltage ($V_{GE} < 60V$), high current density ($J > 100$ A/cm^2), and long lifetime ($t >$ 100 hours at 100 A/cm^2, $>$ 100 hours at 10 A/cm^2, and $>$ 300 hours at 100 mA/cm^2). The current density enabled by our device structure is an improvement of $> 10\times$ over state-of-the art ($\approx 1 - 10$ A/cm^2) for Si field emission cathodes operated in a direct current mode. Our devices demonstrated a turn-on voltage as low as 8.5 V. This low-voltage enabled operation in a 500 Torr He ambient with an anode-emitter voltage below the first ionization potential of He ($\sim$ 19 V). These high current, high current density, long lifetime cold cathodes could enable new approaches to x-ray imagers, RF amplifiers, THz sources, and deep UV sources.

Thesis Supervisor: Akintunde I. (Tayo) Akinwande
Title: Professor

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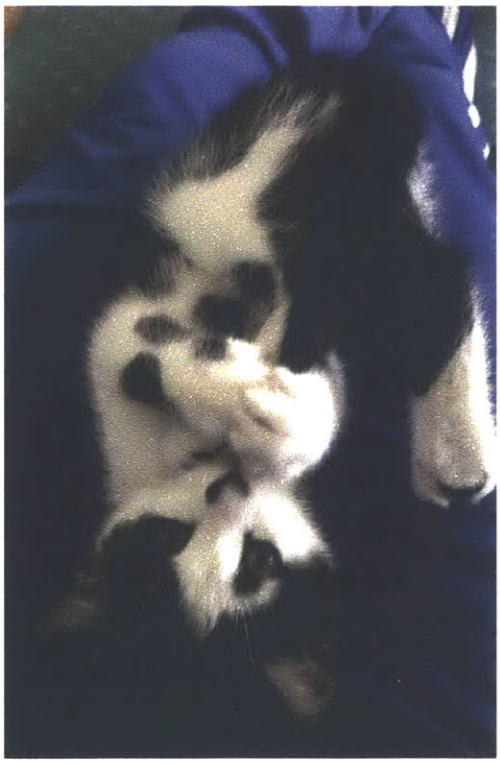
Also, because there is precedent for this, here is a picture of my kitten, Franklin:



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Chapter 1

Introduction

1.1 Problem Statement

Semiconductor electronic devices have become ubiquitous since the integrated circuits revolution in the 1960s, displacing vacuum electronics in all but a small number of niche applications. As the frequency and power performance of solid state transistors increased and their cost to manufacture plummeted exponentially according to Moore's Law [90], vacuum electronics could not compete with integrated circuits in a vast number of applications in terms of size, weight, power, or cost.

In some applications, however, creating electronic devices with increasing power output, frequency performance or smaller size becomes much more challenging using semiconductor devices. This may be due to environmental constraints, such as very high temperatures that cause the failure of metal-semiconductor contacts or the intrinsic carriers to dominate the extrinsic doping and thus breaking p-n junctions. Another area where solid-state electronics struggle are in high radiation environments (*i.e.* space), where cosmic rays can generate carriers that change the behavior of logic and memory circuits, leading to errors. Cosmic rays are photons that can have energy > 1 GeV, thus shielding electronics from them is an extreme challenge.

Building high frequency and high power electronic devices is a particular challenge due to carrier transit delays and breakdown of the device. These carrier transit delays set a fundamental limit to the switching frequency of a device and arise from effects of transport in a

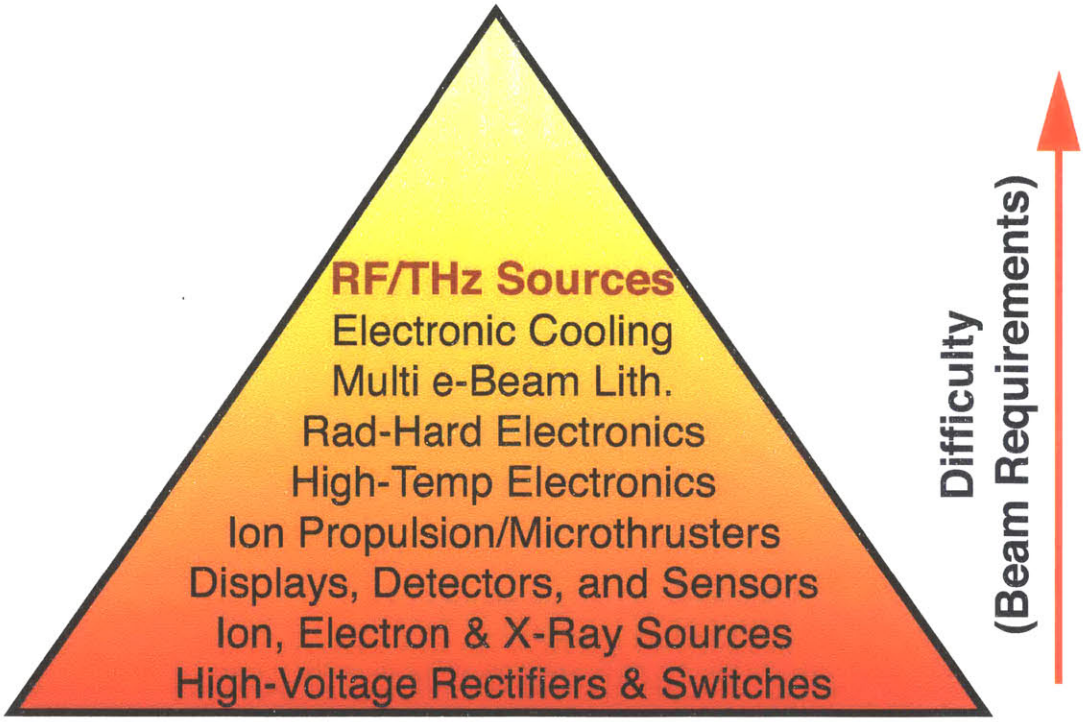


Figure 1-1: Applications for Gated Electron Field Emitters

semiconductor crystal and include electron-phonon interactions and ionized impurity scattering [85]. To combat the carrier transit problem, the channel length is reduced, however, by reducing the channel length, the maximum voltage that can be applied between the drain and the source (V_{DS}) is also reduced. A measure of the high frequency and high power performance of a material system or device architecture is given by the Johnson Figure of Merit ($JFOM$) [71]

$$JFOM = \frac{E_{br} v_{sat}}{2\pi} \tag{1.1}$$

where E_{br} is the breakdown field of the channel material, and v_{sat} is the saturation velocity of the electrons in the channel.

Because there are no atoms for electrons to interact with in vacuum, they may be accelerated to velocities approaching the velocity of light, c, without scattering. The challenge in this case is designing high voltage systems.

Terahertz radiation is considered the sub-mm wave frequency band between 300 GHz and

	Si	GaAs	4H-SiC	GaN	Diamond	Vac.
E_g (eV)	1.1	1.42	3.26	3.39	5.45	∞
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}	1.6×10^{-27}	0
μ_n (cm^2/Vs)	1350	8500	700	1200 (bulk) 2000 (2DEG)	1900	$\simeq \infty$
v_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	2.7	$\simeq 300$
E_{br} (MV/cm)	0.3	0.4	3.0	3.3	5.6	> 100 [130]
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20	≈ 0
$JFOM$	1	2.7	20	27.5	50	> 4000

Table 1.1: Properties related to power performance at high frequencies, based on [89]

30.0 THz. The energy of a 1 THz photon is 4 meV, which is near the energy gap between molecular bands [2]. For this reason, THz is particularly exciting for applications investigating the structure and composition of materials, including radar medical imaging (tomography), biological and chemical sensing, and spectroscopy. In addition, while the atmosphere absorbs radiation in the THz regime quite readily, the bandwidth available is enormous, making it a promising band for high-bandwidth satellite-satellite or satellite-aircraft communications. Room-temperature photonics also struggle in the "THz gap". Photonic devices rely on population inversion, and at room temperature, kT is the energy of a 6 THz photon. Because of that, it is a serious challenge for operation below that frequency. Vacuum electronics are an exciting technology because it does not suffer from either of these problems. For a relativistic beam, slow wave interaction structures for 1 THz are approximately 300 μm: not a particular fabrication challenge using state-of-the-art MEMS technologies.

For an example of a THz system that could benefit from high current, high current density cathodes, Basten et al. recently demonstrated the operation of a 0.85 THz power amplifier using a folded wave guide slow-wave interaction structure Shown in Fig. 1-2[8]. They used a thermionic cathode that required a large permanent magnet for beam forming and compression to obtain 3.1 mA of circuit current and 311 A/cm^2 circuit current density. If this beam performance could be achieved without large permanent magnets, there could be a dramatic reduction in the size and weight of these systems.

With the *possible* exception of carbon nanotube cathodes for x-ray sources[45, 56], cold

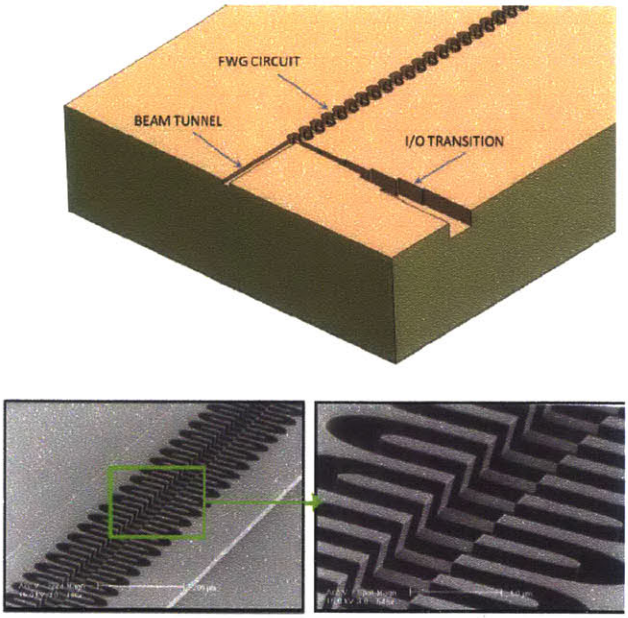


Figure 1-2: 0.85 THz Vaccum amplifer, reprinted with permission from [8]. ©2012 IEEE

cathode electron sources have yet to fully deliver on their promise of a high-performance cathode adequate for integration into commercial systems. The performance requirements of these applications include beam quality (*low energy dispersion, high brightness, small spot size*), current (*high current, high current density*), uniformity (*spatial uniformity and stability*) and lifetime (*long lifetime*). While electron sources based on field emission have had promise, they have not met the performance goals required for systems.

Through careful examination of the literature, it has become clear that there are four main challenges that have thus far prevented afield emission source from achieving the required metrics:

1. large capacitance between the gate and the emitter electrodes that has limited switching and high frequency performance [117, 99];

2. insulator breakdown due to injection of charge from either the silicon substrate into the dielectric spacer between the gate and the emitter substrate or the gate electrode pad into the substrate, or flashover of the dielectric where the desorption of gas molecules adsorbed in the dielectric leads to a plasma on the dielectric surface and vaporization of the dielectric [5, 50]

3. erosion of field emitter tips due to bombardment by back streaming ions emanating from impact ionization of neutral gas molecules desorbed form the anode or the gate that may include the formation of a plasma

4. emitter tip melting due to Joule heating and thermal runaway or cathodic arc. [13, 12].

Temple *et al.* reduced the capacitance between the gate and the substrate of field emitter arrays in order to increase the unity current gain cut-off frequency, f_T.

$$f_T = \frac{g_m}{2\pi C_{GE}} \tag{1.2}$$

where C_{GE} is the gate-emitter capacitance and g_m is the transconductance i.e. $\partial I_A / \partial V_{GE}$. They used silicon pillar structures with aspect ratios of 2.5:1 (column height: pillar diameter). The pillar diameter has an impact on the minimum gate aperture which in turn has an impact of the field factor, β, and consequently the slope of the Fowler-Nordheim plot, b_{FN}. To reduce C_{GE}, further, the aspect ratio of the field emitter arrays need to be increased further.

Holland *et al.* reduced charge injection into the oxide between the gate and the emitter by increasing the insulator thickness to 4 μm while keeping the gate aperture at a diameter of 1 μm. Using this structure; they reported a reduction in the electrostatic field across the insulator between the gate electrode and the substrate leading to a dramatic decrease in charge injection and device reliability. Furthermore, the increase in the insulator thickness while keeping gate aperture the same made the structure more amendable to field ionization at relatively low voltage, a physical process that requires more intense electrostatic fields at the tip [114, 40]. In this work, the aspect ratio is increased to >50:1 while the gate aperture is reduced to 350 nm and oxide thickness increased to 10 μm dramatically reducing the electrostatic field across the gate insulator thereby reducing time dependent dielectric breakdown (TDDB) and hence increase lifetime [87].

Takemura *et al.* showed that a vertical current limiter connected in series to a small array of field emitters could improve reliability while not having any significant impact on the voltage drop across the field emitter and hence the field emission current. They showed that the vertical current limiter improved lifetime of cathodes in traveling wave tubes (TWTs) [120]. Browning et al. had earlier shown that cathodic arcs could be arrested or quenched if a high valued

resistor is placed in series with the emitter or gate of the field emitter with the central idea of limiting the current in the gate/emitter circuit [13, 12, 3]. Velasquez-Garcia *et al.* improved emission current uniformity [55, 124, 125] by incorporating high aspect ratio silicon vertical current limiters [tip-to-tip spacing 10 μm, column diameter 1μm, column height 100 μm] in series with each emitter tip. The inclusion of a silicon vertical current limiter with current source behavior in series with each emitter tip improved uniformity, severely reduced under-utilization of tips in the arrays and also improved lifetime/reliability.

While Velasquez-Garcia *et al.* were successful in improving emission current uniformity and reliability; their device required high operating gate-to-emitter voltage and only $\approx$ 1% of the emitted electrons were collected by the anode. This is because they needed to use an external gate electrode that is not self-aligned to the emitter leading to significant interception of the emitted electrons but more importantly high gate-to-emitter distance leads to low field factor and hence high operating voltages. They could not fabricate proximate self-aligned gates because they could not embed their high aspect ratio silicon columns that form the basis for the current limiter in a dielectric matrix.

In this work, the tip density was increased by a factor of 100× compared to Velasquez-Garcia *et al.*, and also the operating voltage was reduced by a factor of 10× allowing the attainment of very high current per tip and current density of 100 A cm^{-2} at low operating gate-to-emitter voltages (V_{GE} < 75 V) while also achieving long lifetimes (>100 hours @ 100 A cm^{-2}). The presence of a current limiter in the emitter circuit improves both emission current uniformity and lifetime/reliability.

None of the previous work of integrating silicon pillars into field emitter arrays has been able to simultaneously achieve high current, high current density, and low voltage while maintaining long lifetime due to the lack of a fabrication process that could simultaneously build, dense, high aspect ratio silicon nanowires with sharp emitter tips, and integrated, self-aligned extraction gates.

This thesis addresses all of the challenges that have prevented field emitters from being viable sources in a holistic manner as follows:

- The silicon nanowire (diameter = 200 nm, column height 10 μm) embedded in a dielectric matrix proposed here increases the aspect ratio to 50:1 (and potentially 100:1) and

thus dramatically reduces C_{GE} and improves switching performance.

- Emission current uniformity is improved because the emission current from sharper tips which turn-on at lower voltages (due to of the higher field factor of sharper emitters) are regulated by the current limiter while the duller tips turn-on at higher voltages and emit lower currents.

- Reliability is improved because the current limiter prevents a tip from ever attaining a current level that is sufficient to result in thermal runaway and melting. The current limiters also help to prevent cathodic arcs or plasma formation by preventing the current runaway needed to sustain the arc or plasma.

- The lifetime is improved because the electrostatic field across the insulator is significantly reduced leading to reduction in time dependent dielectric breakdown (TDDB) and hence longer lifetime.

- The final piece of the puzzle is tip erosion from back ion bombardment or arc formation due to desorption of gas molecules from the anode. For our device characterization, we used a hollow anode structure that prevents desorption of gas molecules from the anode upon energetic electron impact and subsequent ionization of the desorbed molecules. The tip, which is often biased at the lowest potential, is bombarded by the ions generated from gas molecules desorbed from the andoe. The current limiters based on silicon nanowires connected in series with tips also prevent plasma formation and thus increase lifetime.

To address these failure mechanisms, in this thesis we report the design, fabrication process, and characterization of silicon field emitter arrays with integrated silicon nanowire current limiters and self-aligned gate apertures. The field emission cathode has tip radii less than 10 nm integrated with silicon nanowires ($\approx$ 100 nm diameter), high aspect ratio (10 μm tall), and dense (1 μm pitch) silicon nanowire arrays. Our solution to the problem results in devices that span three length scales and seven orders of magnitude, creating a number of challenges both in fabrication and in modeling:

- Emitter tip radius — on the order of 1 nm

- Gate diameter and nanowire length — on the order of 1 μm.
- Emitter-Anode separation — on the order of 1 cm.

These devices have demonstrated current > 10 mA, current density > 100 A/cm^2, $V_{GE,ON}$ < 60 V. These results demonstrate that these devices could become an enabling electron source for applications that require high current density cathodes.

1.2 Objectives of This Work

The objectives of this thesis can be summarized as follows:

- Develop a fabrication process for creating silicon nanowire current limiters with silicon field emitter arrays with integrated, self-aligned extraction gate apertures.
- Demonstrate that the integration of the silicon nanowire current limiters results in a cathode with significantly improved performance (current, current density, and reliability) over the state-of-the-art.
- We demonstrated current > 10 mA, current density > 100 A/cm^2, and lifetime > 100 hours at 100 A/cm^2.

1.3 Structure of Thesis

The outline of this dissertation is as follows:

Chapter 2 of this dissertation reviews the physics of electron emission, with particular emphasis on field emission. It describes field emission as a two step process, where first electrons are transported to the surface barrier, and then they tunnel through the deformed barrier into vacuum. This concept is central to the hypothesis that by controlling the supply of electrons, we can build more uniform and reliable electron sources.

Chapter 3 introduces the silicon pillar/nanowire current limiter as an attractive option to controlling the supply of electrons. These silicon pillars act as an ideal current source for field emitters, providing simultaneously high current and high dynamic resistance due to velocity

saturation and pinch off in the channel. Because they are located directly underneath each emitter tip in an array, the emitters may be packed densely. This chapter also describes thermal modeling and the second-order effects and non-idealities of silicon nanowire current limiters, such as surface states and 3-D effects.

Chapter 4 presents a proof-of-concept structure that demonstrates that a scaled silicon field emitter array with silicon nanowire current limiters is feasible. This structure is the first to demonstrate saturation effects of a scaled silicon field emitter array with silicon nanowire current limiters. Due to the distance between the gate and the emitter tip, emitter-to-emitter pitch was limited to 5 μm. SEM imaging of the completed structure revealed that the fabrication process achieved a tip radius < 6 nm with a standard deviation of 1.2 nm.

Chapter 5 presents the gated field emitter array with silicon nanowire current limiters. First, it explores in detail a structure that demonstrates a successful method for simultaneously embedding the silicon nanowires in a high quality dielectric matrix while allowing for an integrated gate with a gate aperture that is self-aligned to the emitter tip. However, this structure suffered from several significant drawbacks including large gate leakage. To combat these problems, a new device design that addressed these problems and attained breakthrough device performance in regards to current density and device lifetime was developed.

In Chapter 6, the lifetime and reliability of the field emission arrays with integrated gates and silicon nanowire current limiters is investigated. Our device characterization shows that the Si nanowire current limiter enables long lifetime operation, with lifetime >10 days @ 100 mA/cm^2, and >100 hours @ 100A/cm^2. The I-V characteristics show that there is increase in gate-emitter voltage to achieve the same current with time, but that by allowing the device to relax in a ultra-high vacuum environment, the original I-V characteristics can be restored, indicative of charge trapping at the Si/SiO_2 interface.

Chapter 7 explores some novel device structures and applications that are enabled by the technology developed in this thesis. These include field emission operation in high pressure helium ambient environments and low-voltage transmission of electrons through a graphene window.

Chapter 8 presents a summary of this thesis, lists the contributions, and offers some suggestions for future work.

Chapter 2

Field Emission Theory and Technology

2.1 Objectives

This chapter provides an introduction to the theory of cold field emission, and some of the challenges of field emission. It also introduces the most-researched technologies for microfabricated emitters with self-aligned extractor gates. It covers the advantages and disadvantages of these different methods of building field emitter arrays with self-aligned gates, and it introduces the concept of using supply limitation to improve the reliability and uniformity of field emitter arrays.

Electrons in a metal or semiconductor can overcome the energy barrier at the surface (work function) and be ejected from the metal or semiconductor into vacuum by two different methods. In the case of thermionic emission or photoemission, the electrons are either imparted with thermal energy or photo-energy so they can overcome the potential barrier into vacuum [Fig. 2-1a]. In the case of field emission, however, the potential barrier is deformed by the application of an electric field to the point where electrons can tunnel *through* this barrier and leak into vacuum [Fig. 2-1b].

2.2 Fowler-Nordheim Model

The tunneling current density for electrons through a triangular barrier is given by (For a full derivation, please see Appendix D):

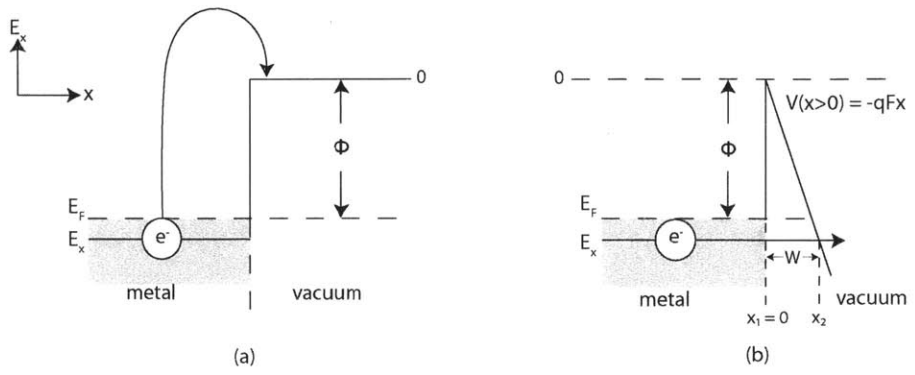


Figure 2-1: Two methods of emission of electrons from a metal. (a) Thermionic or photo emission. (b) Field emission.

$$J_{tnl} = q\frac{4}{3}\frac{16\pi m^* \sqrt{\phi/E_F}}{h^3 B^2(\phi + E_F)} F^2 \exp\left[-B\frac{\phi^{3/2}}{qF}\right] \tag{2.1}$$

here q is the electronic charge, m^* is the effective mass, ϕ is the work function, E_F is the Fermi energy, F is the electric field, and B is a constant ($B = 4\sqrt{2m_e}/3\hbar q \approx 6.87 \times 10^7$). While the above equation gives a simple quantum mechanical model for the tunneling current for a triangular barrier, additional considerations must be taken into account [46] to account for image forces that lowers the energy barrier at the surface. Near the surface, the electrons see an image potential V_{im} due to their proximity to the conducting surface, given classically by $V_{im} = -q^2/4x$ [98]. This gives a total potential term of

$$V = -q\left[Fx + \frac{q}{4x}\right] \tag{2.2}$$

This new energy barrier at the surface, while rounded at the top, is still almost triangular, with a maximum height of $\sqrt{\phi - yF^{1/2}}$ and a tunneling width of ϕ/qF. The area under the curve $\sqrt{V(x) - E_x}$ from 0 to W is different from the uncorrected area by a factor of $\alpha = \sqrt{1-y}$, where $y = 3.79 \times 10^{-4} qF^{1/2}/\phi$

The corrected potential term is inserted into the tunneling probability expression to compute the integral in eq. D.12. The result is the Fowler-Nordheim equation.

$$J = \frac{AF^2}{\phi t^2(y)} \exp\left[-B\frac{\phi^{3/2}}{F} v(y)\right] \tag{2.3}$$

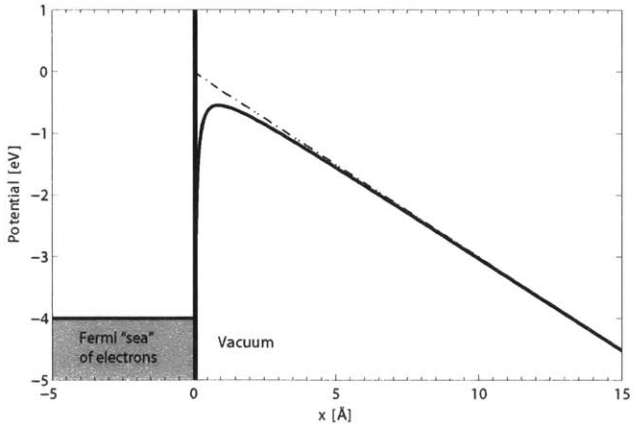


Figure 2-2: Comparison of the barrier with image charge correction (solid line) to the uncorrected barrier (dashed line)

Where $t^2(y)$ and $v(y)$ are elliptic functions that take into account the image charge barrier rounding effects, $A = q^3/8\pi h \approx 1.54 \times 10^{-6}$, $B = 4\sqrt{2m_e}/3\hbar q \approx 6.87 \times 10^{-7}$ and $y = \sqrt{q^3F/\phi} \approx 3.79 \times 10^{-4}F^{1/2}/\phi$.

The Fowler-Nordheim model is not without its limits. First, the above section assumes that the charge cloud terminates abruptly at the surface of the emitter. Instead, the electron cloud extends part way into vacuum. Because of this, the potential step is not as abrupt as depicted.

In the case of a semiconductor, there is also the issue that the electric field penetrates into the material some distance, resulting in band-bending and a potential at the surface, ϕ_s, which makes the surface barrier different from the work function of the bulk. At high fields, the semiconductor will be driven into accumulation, and a lower-dimensionality electron gas will form at the surface.

Generally, the Fowler-Nordheim equation is only valid for planar, metallic surfaces at 0 K. In the case of a nano-fabricated semiconducting field emitter at room temperature, none of these approximations are exactly true. For example, depending on the geometry of the emitter and the material used to fabricate it, the assumption that the electrons are in a 3-dimensional electron gas (3DEG) may not be valid. For example, in a semiconductor, a sheet charge, a line charge, or a point charge may form at the field emitter, resulting in a 2-D, 1-D, or 0-D electron gas. There has been work from Patterson et al. [100] and Qin *et al.* [105] to extend the model to different geometries and different materials. While these solutions are more correct, applying

them to experimental data is much more challenging, and their analytical complexity tends to obfuscate the meaning of the results.

Despite some of these drawbacks, if we continue to use the Fowler-Nordheim model instead of one of the more advanced models, several approximations could be made to make the Fowler-Nordheim model analytically solvable and applicable to nanofabricated field emission triode structures. In order to apply the theory to experiments, the Fowler-Nordheim model must be translated from current density and surface electric field to the experimentally observable quantities of measured current and applied voltage. To translate the current density, J to current, I, we can approximate the emission current as constant over an effective area of emission, α, and make the substitution $J = I/\alpha$.

To translate the field, F to applied voltage, V, we can make the approximation that the surface electrostatic field is proportional with gate voltage, V_G through a constant β, such that $F = \beta V_G$. β is known as the field factor and depends on the geometry of the emitter structure. A large β implies that the effective electric field at the surface of the apex of the emitter tip will be much larger than the macroscopic electric field (i.e. $\beta V_G \gg V_G/(R-r)$). β is described in more detail in Section 2.3 below.

Because the elliptical functions are slowly varying, they can be approximated as $t^2(y) = 1.1$ and $v(y) = 0.95 - y^2$ [11]. With these simplifications, Equation 2.3 becomes:

$$I = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B(1.44 \times 10^{-7})}{\phi^{1/2}}\right] V_G^2 \exp\left[-\frac{0.95 B \phi^{3/2}}{\beta V_G}\right] \tag{2.4}$$

This equation can be further simplified by the introduction of the FN coefficients commonly found in the literature [116], a_{FN} and b_{FN}:

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\phi} \exp\left[\frac{B \cdot 1.44 \times 10^{-7}}{\phi^{1/2}}\right] \tag{2.5}$$

$$b_{FN} = \frac{0.95 B \phi^{3/2}}{\beta} \tag{2.6}$$

Making the appropriate substitutions results in a simplified version of the FN equation that could be used in interpreting experimental data:

$$\boxed{I = a_{FN}\, V_G^2\, \exp\left[-\frac{b_{FN}}{V_G}\right]} \tag{2.7}$$

2.3 The Field Factor, β

The field factor β is an important approximation for microfabricated, non-planar emitter geometries because it allows us to apply the Fowler-Nordheim model to a wide variety of emitters, instead of just the planar geometry that Fowler and Nordheim first considered. The potential at every point in this system, Φ is a boundary value problem governed by the Laplace equation. A simple analytical solution is found through the approximation of the tip as a hard "ball" and the gate as a spherical shell. The Laplace equation (assuming no space charge in the vicinity of the emitter tip):

$$\nabla^2 \Phi = 0 \tag{2.8}$$

is trivial to solve in spherical coordinates to find the electric field at the surface of the "ball" [68] While the tip is not truly a spherical ball, nor is the gate not a spherical shell, it gives a quick approximation for the field factor:

$$\beta \approx \frac{1}{r}\frac{d}{(d-r)} \tag{2.9}$$

Where Φ is the potential at each point. Typically, r is several orders of magnitude smaller than d (~5 nm compared to ~200-300 nm for an integrated gate electrode. If not integrated, d may be many orders of magnitude larger), so the approximation that $d \gg r$ is valid, resulting in:

$$\beta \approx \frac{1}{r} \tag{2.10}$$

Hence to first order, β is inversely proportional to tip radius. To check the validity of the ball-in-sphere model, 3-D electrostatics simulations of both the ball-in-sphere model and a conical emitter tip with tip radii, r = 10 nm and gate aperture radius d = 175 nm were performed, as shown in Figure 2-3. The top figures depict equipotential surfaces of a quadrant

of the 3-D models used. The bottom figures are 2-D cross-sections at the apex of the emitter with equipotential lines drawn. The ball-in-sphere model tends to slightly overestimate the field at the apex of the emitter. With 50 V applied to the gate, the numerical ball in sphere model predicts an electric field at the apex of the emitter of 5.3×10^7 V/cm, the conical tip model predicts 3.9×10^7 V/cm, and the $\beta = 1/r$ approximation predicts 5×10^7 V/cm.

More careful modeling of the electrostatics have resulted in new analytical and semi-numerical models of field enhancment, including the "bowling pin model" and the "Saturn model," [37, 70, 32]. These models increase the validity of the approximations used and introduce an angular dependence of the field at the emitter tip, which is lost with the ball-in-sphere model. These models suggest that the field factor β can be modeled as varying with tip radius r in $\beta \approx k/r^n$, where k and n are geometry dependent. The exact calculation of these coefficients varies depending on the model used, however, typically for real devices with a gate aperture > 250 nm in diameter and tip radius, r between 1 nm and 10 nm, n is typically close to 0.7 and k is approximately 10^6.

Examining the geometry of field emission tips fabricated out of silicon using transmission electron microscopy (TEM) imaging, as performed by Pflug [103] in Fig. 2-4, shows that the radius of the field emitters that were fabricated followed log-normal distribution, with radii ranging from 1.4-14nm. Nilsson et. al. have suggested that the field enhancement factor, β follows a Poisson distribution [97], and by implication, that a similar distribution can be deduced for tip radius.

Because of the limits of fabrication at these small scales, it is impossible for a FEA to be completely uniform even across a single die, and large spatial distributions may exist across a wafer. This distribution of tip radius will result in an even larger distribution of emission currents, due to the exponential dependence on tip radius that exists in the FN tunneling model. Thus, even while some tips do have enough electric field to turn on, other tips may have enough electric field are current such that the joule heating could lead to tip destruction.

Fig. 2-5 illustrates the effect of tip radius distribution on emission current. The large, central plot show emission currents for different emitters of a typical field emitter device, assuming an average tip radius $r_0 = 5$ nm and a standard deviation of ~ 1 nm. Within one standard deviation of tip radius, the emission current changes by over 2 orders of maginude at 30 V. For this typical

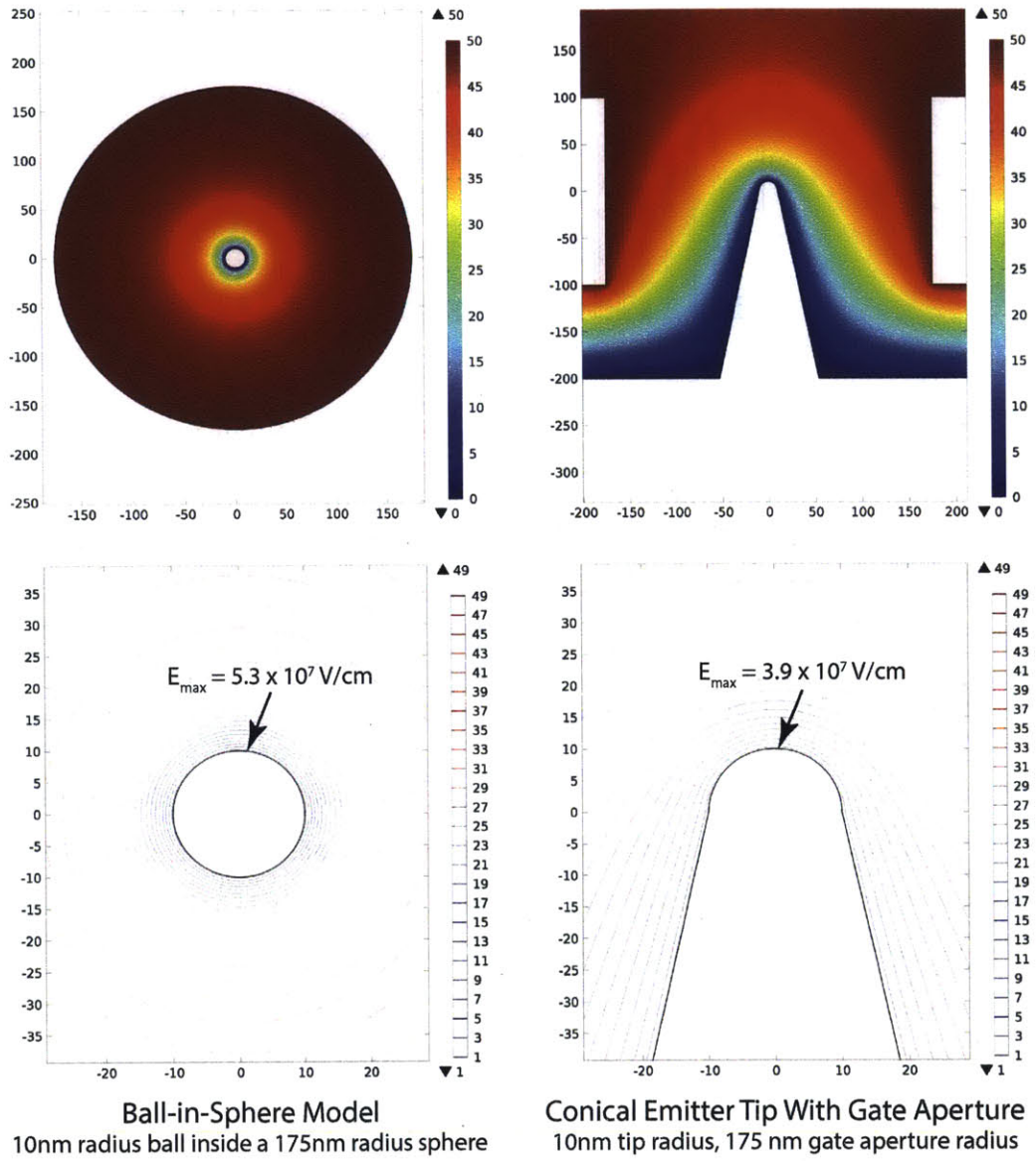


Figure 2-3: Comparison of simulations of the Ball-in-sphere model and a conical emitter tip with tip radii, $r = 10$ nm and gate aperture radius $d = 175$ nm. The top figures depict equipotential contours of a 2-D cross-section of the 3-D models used. The bottom figures are 2-D cross-sections at the apex of the emitter with equipotential lines drawn. The ball-in-sphere model tends to slightly overestimate the field at the apex of the emitter.

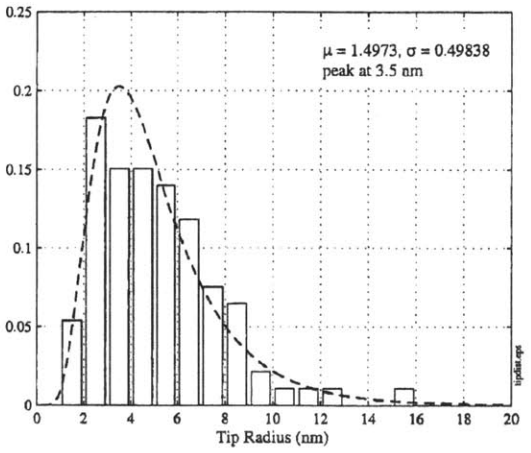


Figure 2-4: Tip radius exhibits a log-normal distribution [103]

emitter tip size distribution, it is possible for the sharpest emitters to burn out before the dullest emitters even turn on, thus limiting the overall performance and utilization of the array.

2.4 State of the Art Field Emitter Arrays

Field emitter arrays are very attractive as a replacement for thermionic cathodes, however they suffer from stability and uniformity problems arising from the exponential dependencies of tip emission current on surface electrostatic field as indicated by the Fowler-Nordheim model presented in Section 2.2. Because emission current has an exponential relationship to the emitter radius, it is difficult to make the emission current uniform over large area. In addition, when not operating in a perfect vacuum, gas molecules from the operation environment may absorb onto the surface of the emitter and change the local work function, resulting in large current fluctuations over time.

It is a significant microfabrication challenge to build a patterned gate in close proximity of field emitter tips. To keep the required voltages small, the gate must be as close as possible to the emitter tip. However, to prevent an electrical short between the gate and substrate, as well as dielectric breakdown of the insulator, thick dielectrics must be used. In addition, if the gate aperture is not precisely aligned with the emitter tip in the center of the aperture, the electric field around the tip will be distorted, resulting in an increased transverse force on the emitted

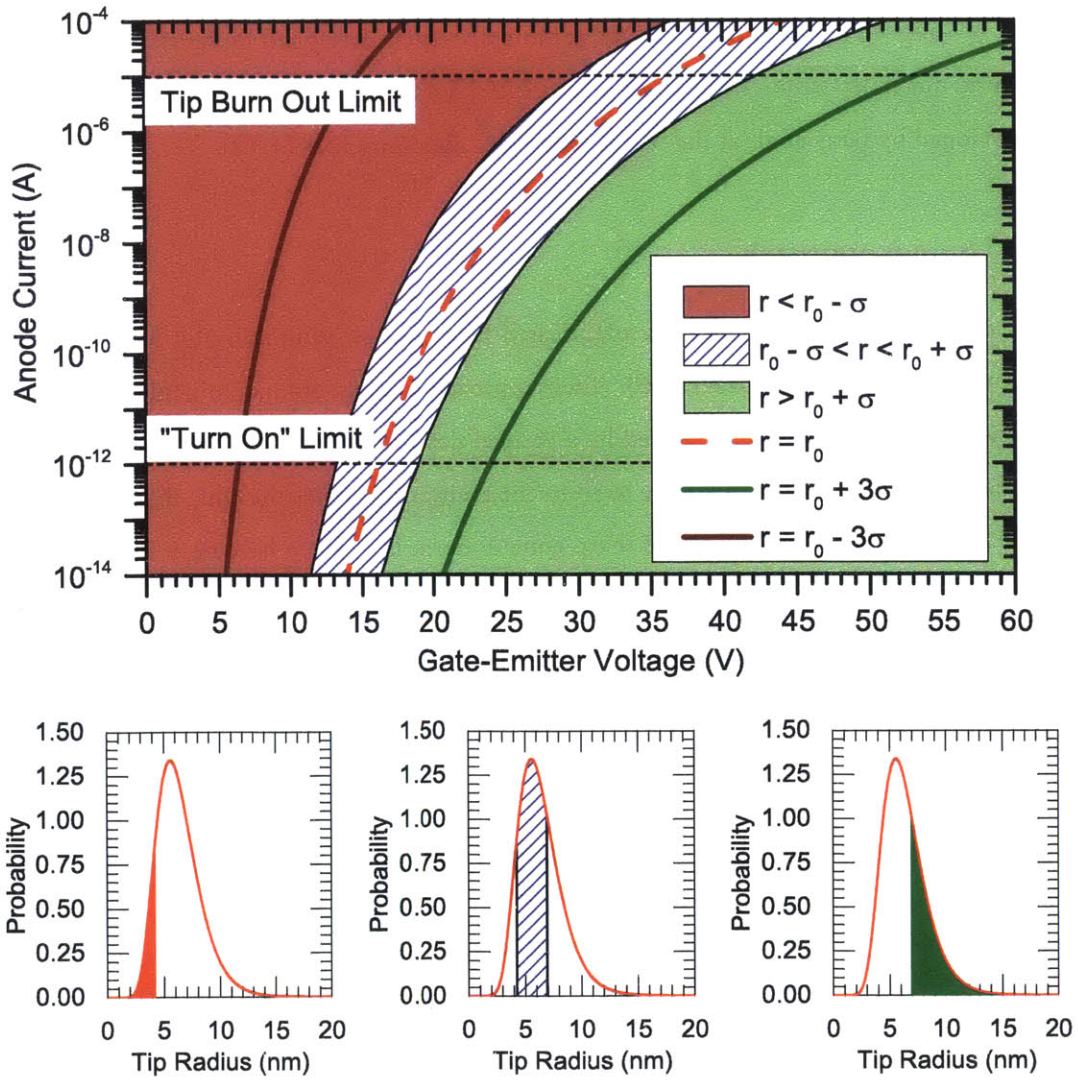


Figure 2-5: The effect of tip radius distribution on emission current. The large, central plot show emission currents for different emitters of a typical field emitter device, and the effect of that the modeled statistical variation in tip radius has on emission current. For this typical emitter tip size distribution, it is possible for the sharpest emitters to burn out before the dullest emitters even turn on, thus limiting the overall performance and utilization of the array.

electrons resulting in interception of the electrons by the gate. Hence, the gate aperture must be self-aligned to the emitter.

There are two main approaches for the microfabrication of field emitter arrays with integrated, self-aligned gates: the additive patterning approach developed by Spindt et al. [116] which uses metal deposition through an aperture and the substractive patterning approach that was developed by Gray et al. at the Naval Research Laboratory (NRL) [51].

2.4.1 Spindt approach

Spindt et al. first demonstrated a microfabricated field emitter using thin film Molybdenum cones in their seminal 1976 paper [116]. Their approach revolves around an angled incidence deposition of a sacrificial layer followed by a vertical deposition of a refractory metal, usually molybdenum, through a gate aperture to form the emitter tip. After the cone deposition, the sacrificial layer is etched, releasing the sharp cone underneath. There have been many refinements to the Spindt process, including 2-step depositions of different materials and different deposition conditions to make for higher aspect ratio emitter cones with thicker dielectrics, and the formation of double gated structures. The Spindt process is the most heavily researched form of field emitter array. The base process for forming Spindt emitters is as follows:

1. Oxidize low resistivity, n-type Si wafer to the desired dielectric thickness (≈ 1 μm)
2. Deposit molybdenum gate through e-beam evaporation
3. Coat with poly-methyl-methacrylate (PMMA) resist
4. Use electron beam (e-beam) lithography to to expose PMMA to write gate apertures of approximately 1 μm
5. Develop PMMA in isopropyl alcohol and expose underlying molybdenum
6. Selectively etch the molybdenum down to the SiO_2 layer
7. Strip remaining PMMA, then etch through the SiO_2 in hydrofluoric acid (HF)

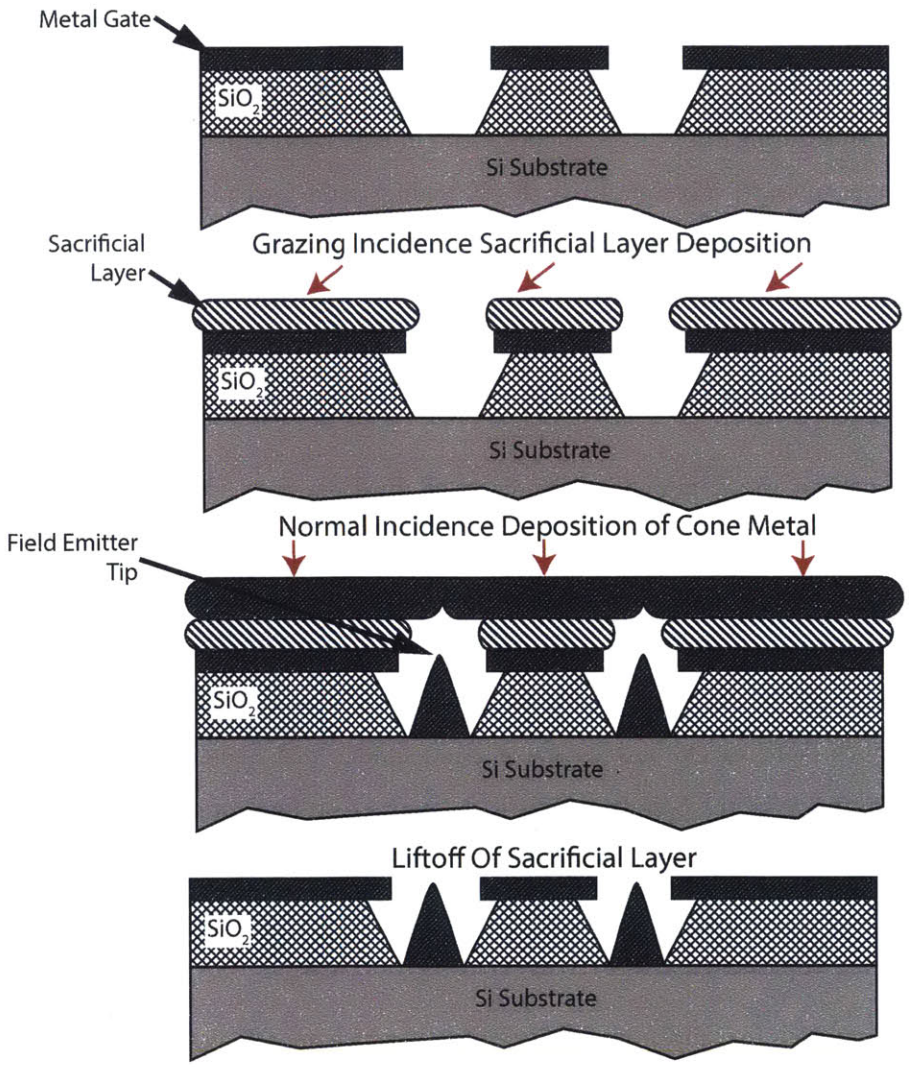


Figure 2-6: Schematic diagram of key processing steps in the Spindt approach for the fabrication of field emitter tips with self-aligned gates uses the deposition and lift-off of refractory metals, traditionally Molybdenum.

8. Deposit aluminum sacrificial layer at a grazing incidence while rotating the sample. The sacrificial layer also serves to reduce the diameter of the holes that will form the emitter cones

9. deposit molybdenum through the partially closed via e-beam deposition using a small source with long throwing distance at normal incidence. The size of the hole continues to shrink during this process. A cone forms in the cavity as the Mo vapor condenses on a smaller area until it is completely closed, leading to the formation of the tips and making the tips relatively uniform

10. Etch aluminum and lift-off excess molybdenum

11. Clean sample and mount in vacuum system

The benefits of the Spindt approach are that all the depositions occur at room temperature, allowing for a variety of different substrate materials to be used. Because the metals are evaporated, many different emitter materials may be employed in addition to refractory metals, such as low-work function materials. Low work function materials are interesting for field emission because they have the potential to emit more current at lower electric fields, however, they are typically much more reactive and less stable than materials with higher work functions.

A disadvantage of the Spindt process is the emitter tip uniformity that can be achieved through deposition in large area devices.

2.4.2 Self-aligned gate apertures through etching

The other approach for fabricating extraction gates which are self-aligned to the emitter tips uses a combination of deposition etching, and chemical-mechanical polishing (CMP). The use of chemical-mechanical polishing in the fabrication of field emitter arrays was first demonstrated by Cathey and Browning at Micron [18, 14]. There have been further enhancements by groups since, including multiple gates [38, 21], electrostatic lenses[92], and extension to different materials[22].

In the CMP approach, shown schematically in Figure 2-7, emitter tips are either etched (in the case of silicon emitters) or grown (in the case of carbon nanotube emitters). A conformal

dielectric material is then deposited which buries the emitter tips, however, due to the conformal nature of the deposition process, "bumps" are formed where the emitter tips are located. A conducting gate is then comformally deposited. Using chemical mechanical polishing, both materials are removed isotropically, exposing the underlying dielectric where the emitters are. This dielectric then can be removed, exposing the emitter surface.

A simple process for forming sharp silicon emitter tips with is as follows:

1. Deposit photoresist on an n-type silicon wafer.
2. Expose photoresist "dots" which become the etching mask for silicon tips
3. Perform an isotropic etch of the silicon to form rough tips
4. Sharpen tips by thermally oxidizing the silicon using traditional semiconductor processing techniques
5. Perform CVD deposition of silicon dioxide for the insulator between the emitter and the gate
6. LPCVD deposition of *in situ* doped polysilicon gate material
7. Polish the device using a timed chemical-mechanical polishing step to form the gate apertures
8. etch the underlying dielectric in hydrofluoric acid to expose the emitter tips
9. Load the sample into vacuum chamber for operation

Advantages of the CMP approach are that using silicon emitters or carbon nanotubes, the emitter tip radius may be incredibly sharp[36] [32, 88], and the deposition and CMP process leverage years of technology development and experience in the semiconductor industry on these processes for good uniformity and repeatability.

The primary disadvantage of this approach is that there is added complexity and processing steps.

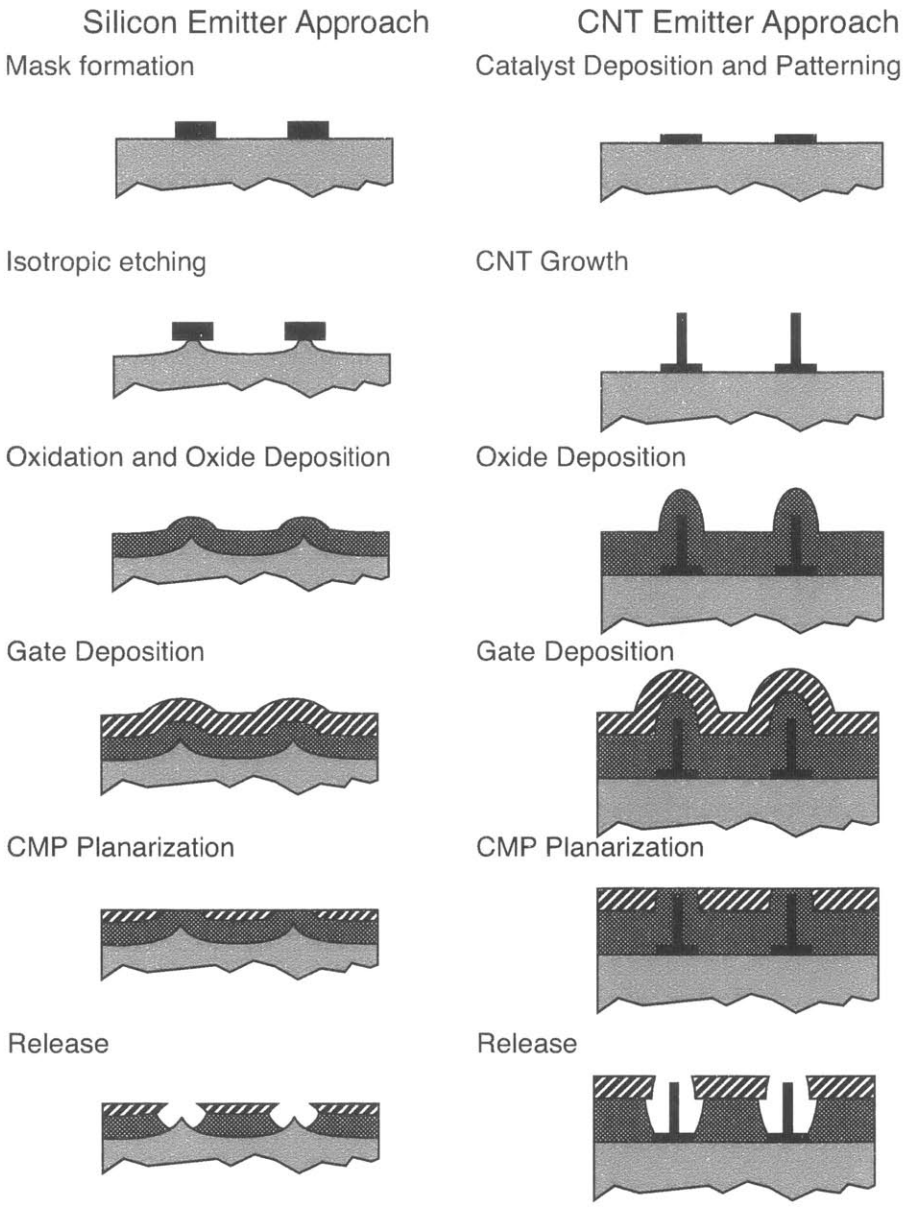


Figure 2-7: Schematic diagram of key processing steps in two different materials for using chemical-mechanical polishing (CMP) to form emitters with self-aligned gates, (Left) Silicon and (Right) Carbon Nanotubes. In both cases, a conformal oxide deposition forms a "bump" that later becomes the gate aperture when excess material is removed during the polishing step.

2.4.3 Controlling the Electron Supply

Field emitters typically operate in a regime where the current is controlled by the probability of electrons tunneling through the barrier from the metal or semiconductor into vacuum. This is because the number of available carriers at the surface is large, and there is a quasi-neutral bulk nearby with an electrical contact to replenish electrons that are transmitted, as is the case with a metallic or heavily-doped n-type semiconductor. This tunneling-probability regime is extremely sensitive to the tip radius and the work function of the emitter. The introduction of a current limitation element changes the system to make the transport process from the bulk to the emitter surface the dominant process in controlling the current and to reduce the sensitivity of the current to tip radius and work function.

Field emission can be treated as a two-step transport process shown in Figure 2-8. First, electrons are transported to the surface barrier. This is included in the Fowler-Nordheim derivation shown in Appendix D as the supply function $N(E)$, but is often obfuscated in simplifications of the Fowler-Nordheim equation. This supply function gives a number of electrons that are impinging on the surface barrier. At the surface barrier, there is a probability that the electrons impinging on the barrier will be transmitted through the surface barrier instead of being reflected.

Most prior work on limiting the supply of electrons to the surface of field emitters focused on using high-resistivity substrates [3, 64] to approximate a current source. The effect of adding

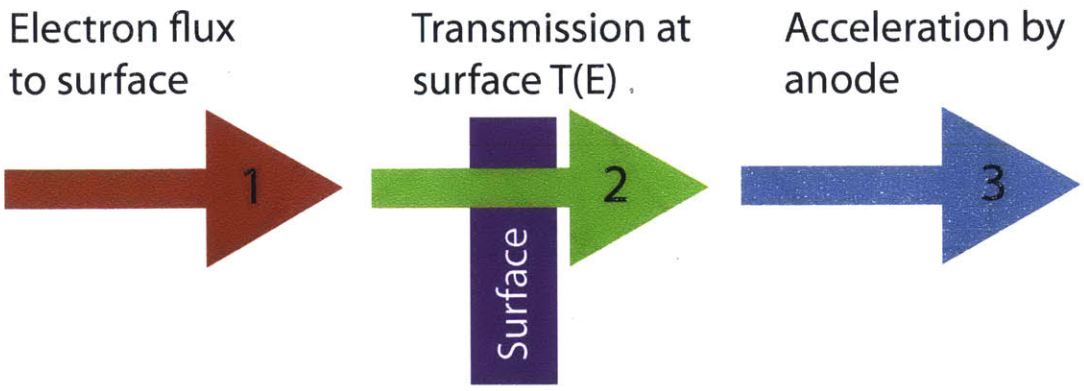


Figure 2-8: Block diagram of the factors involved with field emission. A field emitter may be limited by either the transmission at the surface, or the flux to the surface

a large resistance in series with the emission results in the load line shown in fig 2-9 with respect to tip radius variation. Increasing emission current results in a voltage divider, with part of the voltage dropping across the resistor, reducing the gate-to-emitter voltage and resulting in lower emission current. Adding this resistance improves emitter reliability and reduces cathodic arcs by quenching the formation of a microplasma [13], but it is at the cost of operating voltage and efficiency. In order to reduce sensitivity, the resistance must be large, however, with a linear resistor, it is impossible to simultaneously achieve high current and low sensitivity to tip radius.

To address the non-idealities of the resistive element in series with the FEAs and and closer approximate an ideal current source, MOSFET structures have been integrated into FEAs to control individual [67] or small groups of emitters [62] [74]. The variation of emission current is much less when a MOSFET that is in saturation is used as a current control element compared to when limited by a resistor (provided that the FET output resistance is much less than the

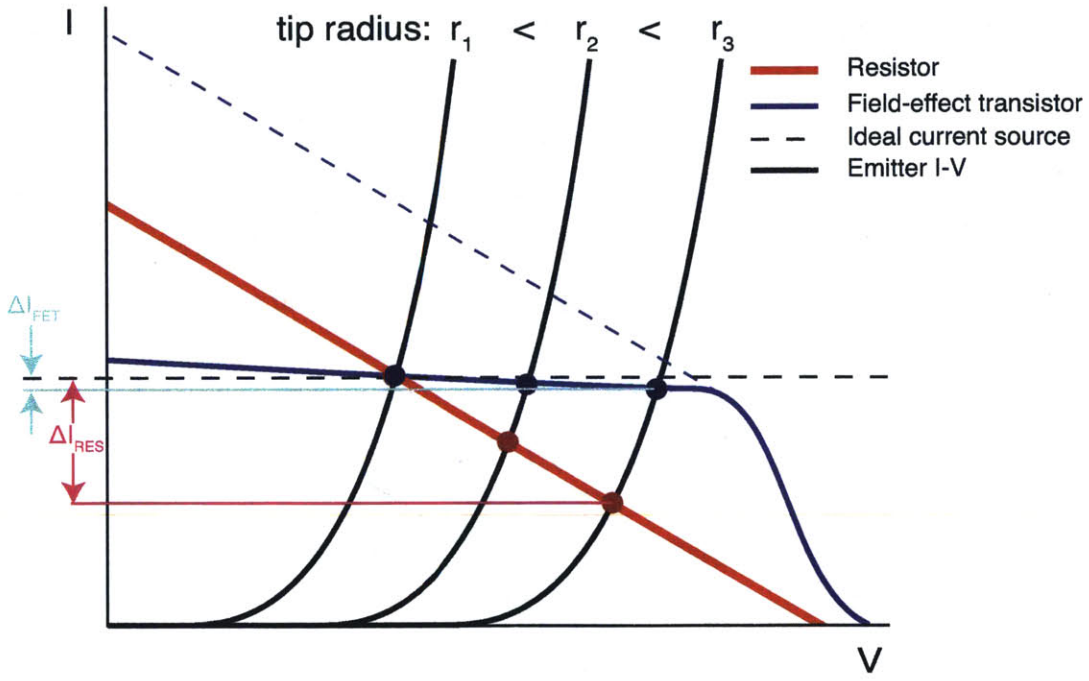


Figure 2-9: Qualitative load lines of different types of current sources connected in series with each individual field emitter, demonstrating the variation of emission current for different tip radii. The dashed blue line shows that even if the output resistance of the FET equaled the that of the resistor, the FET would provide more emission current

linear resistance, *ie.* $g_{out} \ll 1/R$) [Fig. 2-9]. The sensitivity of the current S is given by:

$$S = \frac{I_0}{\Delta I} \tag{2.11}$$

where I_0 is the current, and ΔI is the derivative, i.e. dI/dt at $I = I_0$. Hence, a MOSFET with higher current, I_0, will have a lower sensitivity than a linear resistor.

This combination of high conductance at low V_{DS} and high dynamic resistance in the saturation regime is precisely the behavior required to implement a good current source. The drawback of using a MOSFET to approximate current sources is that planar MOSFETs require significant area in the array, reducing the packing density and hence the attainable current density of the array. A possible trade-off is to use a MOSFET to drive a small number of emitter elements, such as was implemented by Hong et al. and Itoh et al. [62, 67]. In this scheme, however, emission non-uniformity will still occur in the smaller set of emitters controlled by the same transistor. To control each individual emitter with a conventional lateral MOSFET is not advantageous because the relatively large area of the MOSFET will result in a greatly reduced packing density.

Through careful design of the current limiting element, the performance of the array can be improved when compared to that of unlimited arrays. If the limited current is high enough while still preventing burnout, higher current may be obtained than without limitation. Figure 2-10 demonstrates by plotting the hypothetical current of an ideal array, the performance of an array whose emitters burnout at 10 μA, and an array whose current is limited to slightly below burnout $I_{limit} = 5$ μA. Note the hysteresis of the simulation of the array with burnout. During the initial sweep, as the voltage is increased, the anode current decreases due to the burnout of more and more emitter tips. On the down sweep, and on subsequent sweeps, the burnt out emitters do not participate in field emission, and the emission current is several orders of magnitude lower than on the initial sweep.

2.5 Technical Approach

A suitable current limiter has been recently demonstrated: the vertical silicon pillar current limiter. This two-terminal device utilizes velocity saturation of carriers in semiconductor ma-

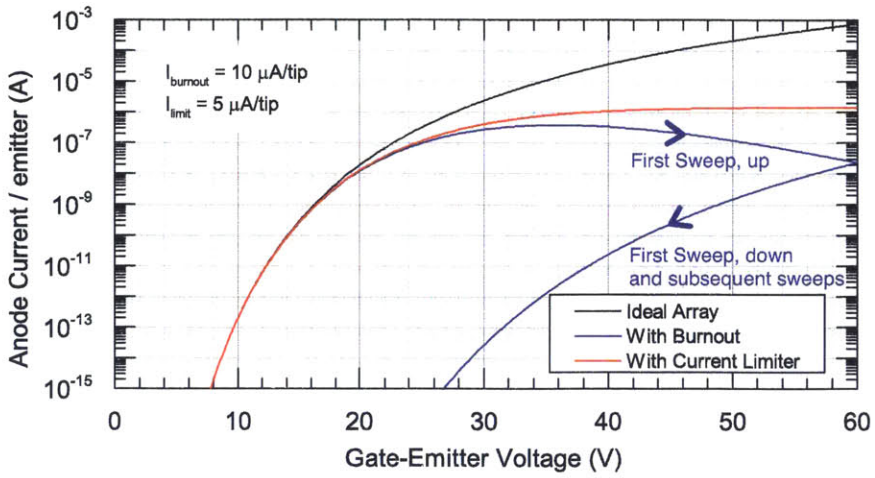


Figure 2-10: The effect of tip burnout on current performance. By limiting the current to each individual emitter in an array, the overall performance of the array can be improved. Note the hysteresis of the simulation of the array with burnout. During the initial sweep, as the voltage is increased, the anode current decreases due to the burnout of more and more emitter tips. On the down sweep and on subsequent sweeps, the burnt out emitters do not participate in field emission.

terials at sufficiently high fields to create a large dynamic resistance. This device was motivated by early work in GaAs by Baek *et al.* where a voltage difference applied between two contacts separated by a distance L generated the required field for velocity saturation [7]. At low fields, the device behaves like a linear resistor. Above a critical voltage, the velocity of carriers in the channel saturates, resulting in pinch-off and current saturation. A schematic diagram of the the device in GaAs reported in [7] is shown in Figure 2-11, and their obtained current-voltage characteristics are shown in Figure 2-12.

In the proposed device, the contacts are spaced much further apart with a small cross-sectional area, resulting in a high aspect ratio structure. The silicon pillars are embedded in an oxide, which passivates the surface and reduces the density of interface traps. When a voltage is applied to the drain end of the channel with respect to the source, the drain electric field creates a channel electric field. The drain potential also depletes the surface of the silicon column at the drain end, narrowing the channel width. The channel becomes narrower as the drain potential increases, eventually resulting in pinch-off. The current saturates due to a combination of the

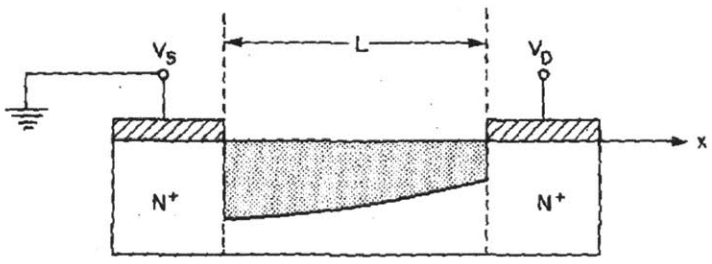
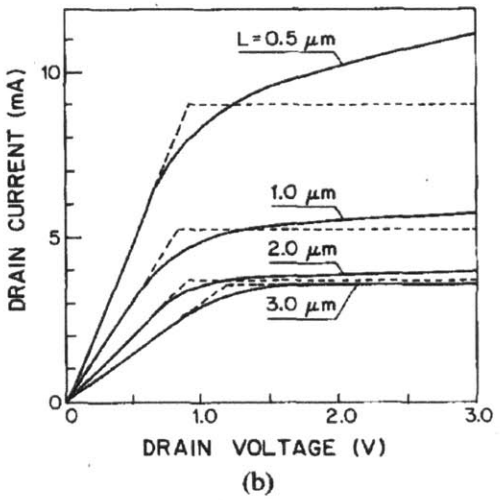


Figure 2-11: Schematic cross-section diagram of the ungated FET current limiter by Baek. Reprinted with permission from [7]. ©1985 IEEE.



(b)

Fig. 8. Comparison of the theoretical results with the experimental data (solid line-experiment; dashed line-theory):

$W = 20 \times 10^{-6}$ m, $A = 1.25 \times 10^{-7}$ m,
$N_d = 1.74 \times 10^{23}$ m^{-3}, $\mu_n = 0.35$ m^2/V-s
(a) $V_{Sbi} = 0.47$ V, $v_s = 1.21 \times 10^5$ m/s, $R_c = 0.74$ Ω-mm
(b) $V_{Sbi} = 0.46$ V, $v_s = 1.20 \times 10^5$ m/s, $R_c = 0.88$ Ω-mm.

Figure 2-12: Measured and simulated I-V characteristics from Baek et al. Reprinted with permission from [7]. ©1985 IEEE.

pinch-off and the saturation of electron velocity under large electric fields. If a lower aspect ratio were used, a higher drain-source voltage is required to pinch off the channel.

Velásquez-García *et al.* demonstrated a 1 cm^2 array with 10μm pitch (*i.e.* emitter density of 10^6 cm^{-2} for an array of 1000 × 1000 emitters). Each field emitter is atop a vertical silicon pillar that is 1 μm in diameter and × 100 μm tall [125]. The tip radius was measured to be

$\simeq$ 30 nm. These arrays lacked an integrated gate electrode, and thus the voltages required for field emission were > 200 V. They demonstrated current saturation at gate-emitter voltage of 1600 V.

These field emitter arrays showed very good stability and uniformity and prevent the destructive heating of the sharpest tips, however, the 1 μm pitch limits the current density that may be obtained from this device. The highest current and current density reported from these device are 0.6 A and 0.6 A/cm^2. The gate was not integrated with the emitter substrate and aligned by hand. Consequently the alignment of the emitters to the gate apertures was poor resulting in an anode efficiency (I_A/I_E) that was less than 1 %.

Numerical simulations, presented in detail in Chapter 3 indicate that the pillar dimensions can be scaled from 100 μm tall, and 1 μ diameter to 10 μm tall and 100 nm diameter, and that by increasing the doping density, the current per tip can remain constant (analogous to Dennard scaling rules for CMOS [27]).

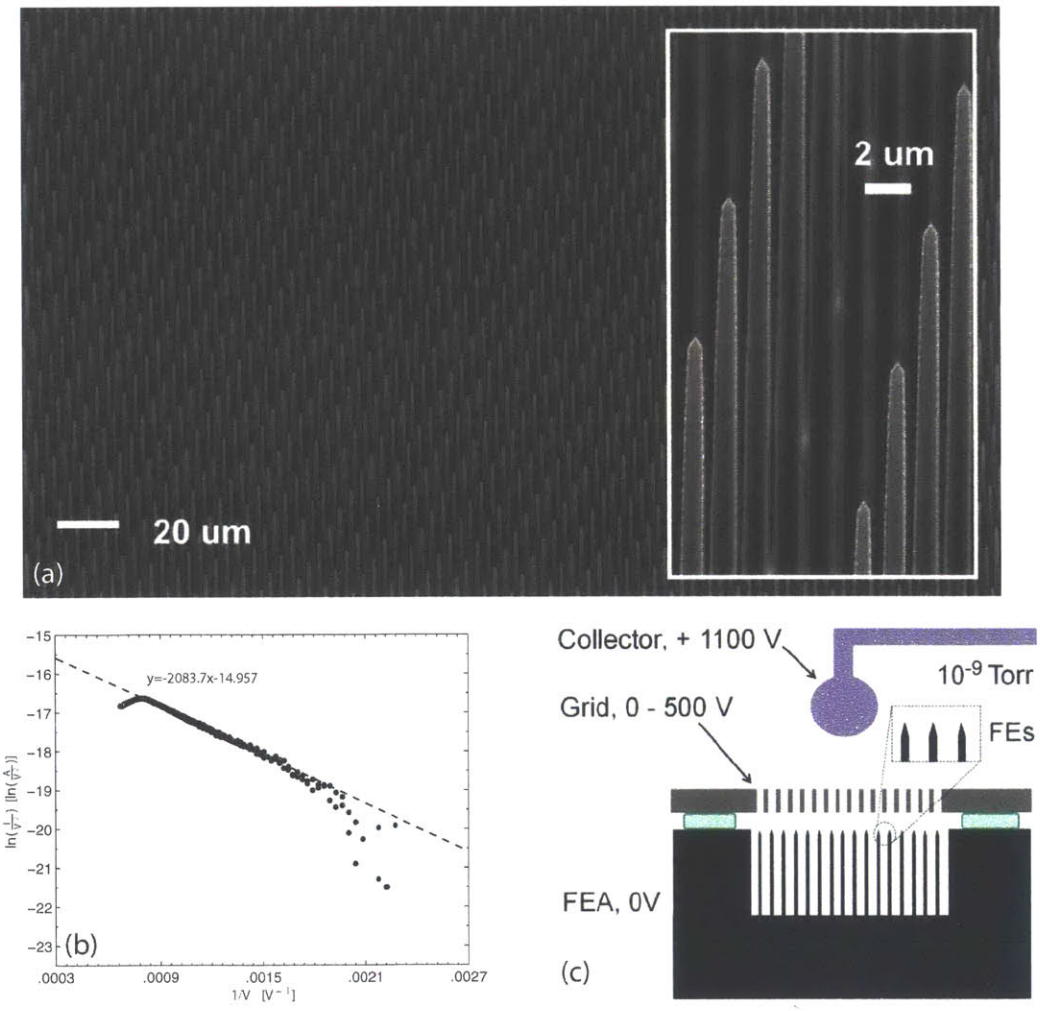


Figure 2-13: (a) Array of field emitters with 10 μm pitch, 1 μm diameter, and 100 μm tall Si pillar current limiters. (b) Characterization setup (c)Fowler-Nordheim plot of a field emitter array with individual silicon pillar current limiters that demonstrates current control by the current limiter. Due to the dependencies of the FN equation, if $\ln(\frac{I}{V^2})$ is plotted against V^{-1}, the graph should be a straight line if the emission mechanism is field emission. This device shows a clear deviation from linear behavior at large voltages. Reprinted with permission from [125]. ©2011 IEEE.

Chapter 3

The Vertical Silicon Nanowire Current Limiter

3.1 Introduction

The objective of this chapter is:

1. Introduce the Silicon nanowire current limiter as a means to regulate the supply of current to individual field emitters
2. Build an intuitive model of the operation of silicon nanowire current limiters
3. Measure the current-voltage characteristics of Si nanowire current limiters, and compare experimental data with models
4. Develop device physics models for surface traps of silicon nanowires as a means to explain the current obtained from silicon nanowires and develop methods to mitigate them
5. Model the interactions between Si nanowire current limiters when operated in parallel in arays, as in FEAs

In Figure 3-1, a schematic drawing (Figure 3-1a) and equivalent circuit diagram (Figure 3-1b) of the FEA and current limiter are shown. The nanowire current limiter has a current source-like I-V characteristic when biased at voltages larger than its saturation voltage [7, 9].

Due to the geometry, the drain region pinches off and the electron velocity saturates, resulting in current saturation.

When vertical current limiters are connected in series with individual field emitters, they limit the current from each field emitter in the array, allowing for uniform emission without thermal runaway or burnout, provided their saturation current is below the burnout limit as demonstrated by Velásquez-Garcá *et al.* [125]. This current limitation is consistent with the operation of the device in the electron supply controlled regime instead of the electron transmission controlled regime as observed by Ding et al. for Si field emitter arrays [62, 31] allowing for reliable operation of FEAs at high currents.

The combined current limiter-FEAs reported by Velásquez-García et al. [125] had Si pillars with a diameter of 1 μm, height of 100 μm, and 10 μm pitch, resulting in a density of 10^6 tips/cm^2. The FEAs are capable of high and uniform current emission (0.5 A and 0.5 A/cm^2). As mentioned in Section 2.5, the arrays reported by Velásquez-García et al. demonstrated stable and uniform emission, and regulation of the emission current by the silicon pillar. Their arrays had pulsed current and current density up to 0.5 A and 0.5 A/cm^2, and the current that they were able to obtain was limited by interception of electrons by the gate electrode, resulting in heating of the gate leading to reflow and failure of the polymer spacer used to separate the gate from the emitter tips. Because the gate was not integrated with the emitters, and aligned by hand, the anode efficiency ($I_A/I_E \times 100\%$) was less than 1 %. With a gate-emitter voltage of > 1000 V and current of 0.5 A, the gate must — in ultra-high-vacuum — dissipate a power of > 500 W (and > $500 W/cm^2$), > 5× higher than the power dissipated by current microprocessors. Hence, to limit the power dissipated, the characterization at gate voltages higher than 1000 V the arrays were pulsed with a duty cycle of 10^{-5}, lowering the average power dissipation to 50 mW.

By spacing the emitters closer together and the making the tips sharper, the operating voltage can be reduced and the current density increased. However, without including an integrated gate, the electric field at the surface of the emitter is reduced due to electrostatic screening of adjacent emitters (For modeling of this effect, please see Section 4.2). Hence, if the distance between emitter tips is to be reduced, a gate must be much closer to the emitter tip (*i.e.* integrated and self-aligned to the emitters). In order to form a self-aligned gate, the gaps between

adjacent pillars must be filled in with a dielectric, and the filling of voids that are 100 μm deep is an unsolved problem. In addition, if the emitter-to-emitter spacing were to be reduced, deep reactive ion etching (DRIE) limits how closely the emitters may be spaced. DRIE of holes is limited to aspect ratios of $\approx 20:1$[129]. Finally, forming emitter tips that are less than 10 nm in radius with this structure uniformly due to etching and oxidation rate variations presents a challenge due to the size of the etching mask used in the fabrication process.

For these reasons, we decided to scale the current limiter demonstrated by Velásquez-García et al. by an order of magnitude, replacing the 1 μm diameter, 100 μ tall Si pillar with a 100 nm diameter, 10 μm tall Si nanowire. Reducing all of the dimensions of the current limiter-FEA structure provides several benefits. By shrinking the pitch of the emitters, the tip density is increased. Because the pillar cross-sectional area is smaller, the saturation current for a given doping density is lower; however, by increasing the doping in the pillar, the current density increases, allowing the same current per emitter to be obtained from narrower pillars. In addition, the gate aperture scales with the pillar diameter. Thus, by decreasing the pillar diameter — and

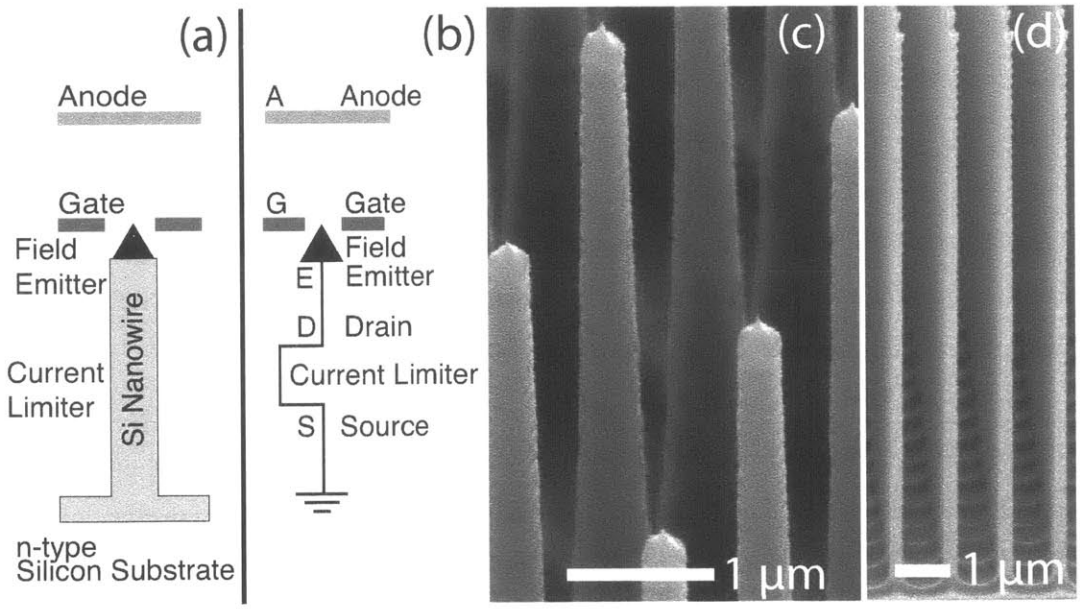


Figure 3-1: (a) Schematic diagram of a single field emitter in series with a current limiter. (b) Circuit diagram of the current limiter-FEA structure. (c) SEM of the completed current limiter-FEA structure. (d) Cross-sectional SEM of a Si nanowire current limiter without a field emitter with oxide removed to show the pillar. This chapter focuses on modeling and characterization of the Si Nanowire current limiter.

by implication the gate aperture — the field factor, β (cm^{-1}), which relates the gate voltage to the electrostatic field at the tip surface increases, resulting in lower turn-on and operating voltages. In practice, Pflug et al. demonstrated gate apertures as small as 70 nm, resulting in a turn-on voltage of 8.5 V [102].

A possible consequence of using current limiters to regulate FEAs is the potentially larger energy spread of the emitted electrons when compared to un-regulated FEAs. In an unregulated FEA, each emitter in the array has the same gate-emitter voltage bias. However, when a current limiter controls the current through each emitter, the gate voltage, V_G, is divided between the gate-emitter voltage, V_GE, and the drain-source voltage, V_{DS}, of the vertical current limiter, i.e. $V_G = V_{GE} + V_{DS}$. Because each emitter is biased at a different gate-emitter voltage, electrons from each emitter are accelerated by different voltages, resulting in a wider energy distribution. The energy spread of the FEA current could potentially be reduced by shrinking the gate aperture, and thus increasing β, while keeping its uniformity constant. Using an FEM simulation platform, we estimated that by increasing β by a factor of 5 while keeping the same tip radius statistics, the energy spread across the FEA decreased from 5 eV to 2 eV.

3.2 Modeling the Si Nanowire Current Limiter — An Intuitive Model

Figure 3-2 shows a typical I-V transfer characteristic for a vertical current limiter, with different regions of operation highlighted. In the following section, we will explore the physics that give rise to the current saturation shown in this graph.

The carrier flow in electronics is most generally described by the Boltzmann Transport Equation (BTE). However, for the purpose of developing a simple analytical model for the description of the operation of the current limiter, beginning with drift-diffusion equation will suffice (although, it is important to note that the drift-diffusion equation can be derived from the BTE). For this discussion, the hole current will be neglected, as the substrate used to fabricate the Si nanowire current limiters is n-type, and the device is operated in the dark, so that there are no photo-generated minority carriers. The substrate is uniformly doped so that there are neither junctions nor large electron concentration gradients, so the diffusion term may also

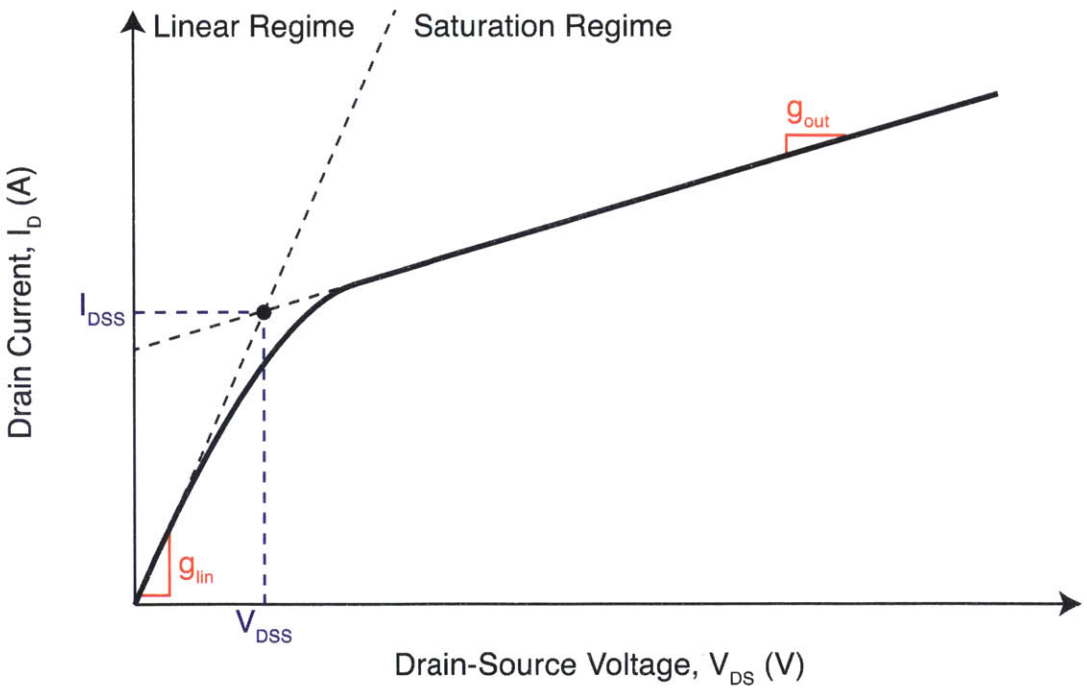


Figure 3-2: Schematic transfer characteristic for the vertical current limiter.

be safely neglected. The problem may be even further reduced by noting that all of the carrier flow will be along the axial direction of the pillar, resulting in a one-dimensional problem.

$$J \approx -q n v_e^{\,drift}(\mathscr{E}) \tag{3.1}$$

At low fields, the current density is proportional to the electric field through the electron mobility, μ_e.

$$J = -q n \mu_e \mathscr{E} \tag{3.2}$$

Where q is the fundamental charge, n is the carrier concentration, v_e^{drift} is the drift velocity of the electrons, and $\mathscr{E}$ is the electric field. Assuming that the pillar has a cross-sectional area, A, and a length, L, the total current supplied to the field-emitter may be obtained. At low voltages, the voltage drop is expected to be linear along the length of the pillar, that is $\mathscr{E} = -\nabla V = -dV(x)/dx$ is a constant, yielding the following expressions for the drain current, I_D

and the linear resistance, G_{LIN} [S]:

$$I_D = qAn\mu_e \frac{dV(x)}{dx} \approx \frac{qAn\mu_e V_{DS}}{L} \tag{3.3}$$

$$g_{lin} = \frac{qAn\mu_e}{L} \tag{3.4}$$

However, at higher electric fields, the velocity of electrons begins to saturate. In silicon, the saturation velocity, v_{sat} is $\approx 1 \times 10^7$ cm/s. To describe the saturation effect, no longer can a linear relationship between current density and electric field be assumed. The drift velocity must now be replaced by the following simple analytic expression:

$$v_e^{drift} = \frac{\mu_e \mathcal{E}}{\sqrt{1 + \left(\frac{\mu_e \mathcal{E}}{v_{sat}}\right)^2}} \tag{3.5}$$

In addition to the field-dependent mobility, the source depletion layer increases from the source to the drain end of the nanowire, resulting in a cross-sectional area, $A(x)$, that decreases along the length of the channel. The full drain current expression is:

$$I_D = \frac{qA(x)n\mu_e}{\sqrt{1 + \left(\frac{\mu_e}{v_{sat}}\right)^2 \left(\frac{dV(x)}{dx}\right)^2}} \frac{dV(x)}{dx} \tag{3.6}$$

Above a certain V_{DS}, the velocity of the electrons reaches v_{sat}, and the electron concentration in the drain end of the channel drops off substantially. Defined as V_{DSS}, it is at this voltage that the channel is pinched off and the current reaches its saturation value, I_{DSS}. Increasing V_{DS} beyond this value causes the overdrive voltage $\Delta V_{DS} = V_{DS} - V_{DSS}$ to be dropped across the depletion region. As ΔV_{DS} is further increased, the depletion region widens, effectively shortening the length of the channel by an amount, ΔL. This effect, known as channel length modulation, can be modeled as a linear increase in the drain current for $V_{DS} > V_{DSS}$. Figure 3-3 illustrates the effect of increasing V_{DS} beyond V_{DSS} on the equipotential lines in the device. For the illustration, it is assumed that the electric field at the edges of the illustration normal to that surface is 0. The current in the saturation regime is thus:

$$I_D \cong I_{DSS}[1 + \lambda V_{DS}] = I_{DSS} + g_{out}\Delta V_{DS} \tag{3.7}$$

where λ [V^{-1}] is the channel length modulation parameter and $g_{out} \approx \lambda I_{DSS}$ [s] is the resulting output conductance. While the behavior of channel length modulation in Si nanowire current limiters is largely analogous to its behavior in standard planar MOSFETs, the channel pinch-off in the current limiter is a 3-D effect, as the extension of the depletion region varies in both orthogonal directions perpendicular to the axial direction.

Another consideration is that the dependence of I_D on V_{DS} beyond V_{DSS} could be explained by drain induced barrier lowering (DIBL). DIBL is a short channel effect in MOSFETs where increasing the drain voltage affects the barrier at the source end of the channel, increasing the injection of charge into the channel. For our devices, it seems unlikely that DIBL plays a major role. The silicon nanowire is long (≈ 10 μm, and the voltages applied are moderate, so that the electric field at the source end of the channel remains low. Finally, because there is no junction in our device, there is no barrier to the injection of carriers into the silicon nanowire.

3.3 Numerical Modeling

To estimate the performance of the vertical current limiters and serve as a guide to their fabrication, process and device simulations were performed using the SILVACO toolset (Silvaco International, Santa Clara, CA). For these simulations, the Si pillar cross-sectional area was fixed at 100 nm × 100 nm. The area surrounding the pillar was filled with SiO_2, and both the top drain contact and substrate source contact were assumed to be perfect ohmic contacts. No interface states or fixed charge at the Si/SiO_2 interface were included in these simulations.

Once the structure was obtained, ATLAS was used to simulate the current-voltage characteristics of a single current limiter. These simulations solved Poisson's equation self-consistently with the carrier flow and continuity equations. To explore the functional dependencies on channel length and doping, the doping density, N_D, was varied between 10^{13} cm^{-3} and 10^{16} cm^{-3}, and the channel length, L, was varied between 1 μm and 10 μm. For the simulations where N_D was varied, the channel length was fixed at 10 μm, and for the simulations where L was varied, N_D was fixed at 5×10^{14} cm^{-3}. Figure 3-4 shows a representative I-V characteristic

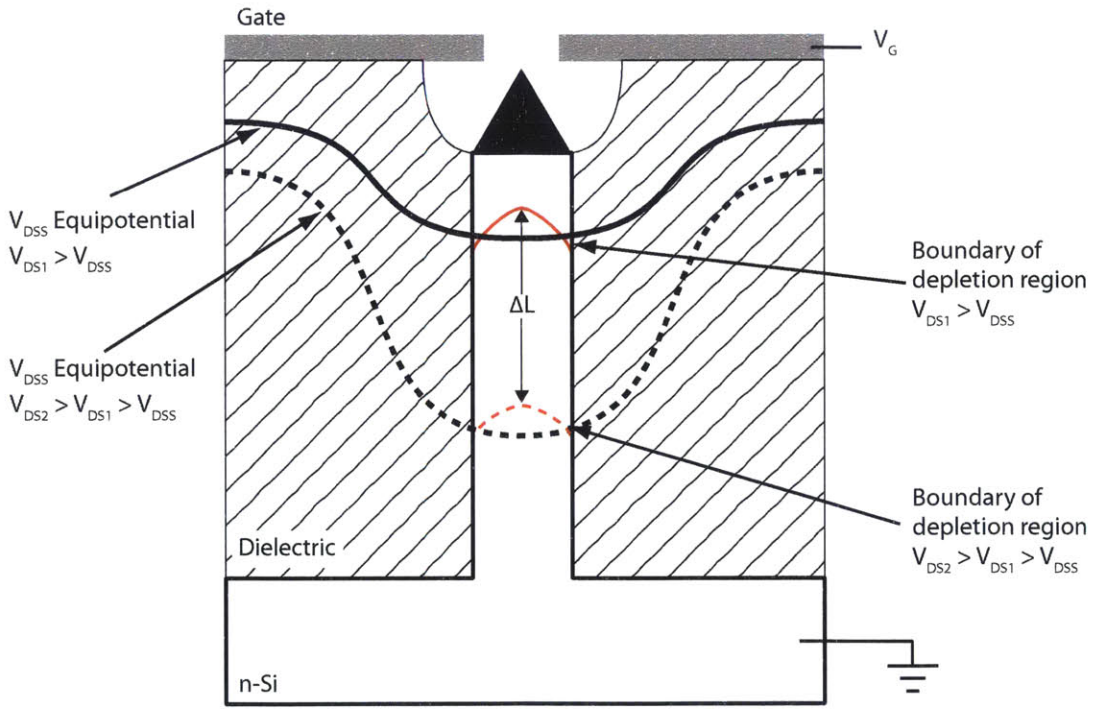


Figure 3-3: Schematic device cross-section showing the evolution of the equipotential lines and depletion width.

from the simulation framework.

The linear conductance (g_{lin}), the output conductance, (g_o), and the drain saturation current per pillar (I_{DSS}) were extracted from the simulations. The dependence of g_o, and g_{lin} on the doping density is plotted in Figure 3-5(a). In Figure 3-5(b), the ratio of g_{lin}/g_{out} is plotted. This metric is an indicator of how well a device with given doping density saturates. In general, nanowires with doping density < 10^{15} can have a linear conductance that is > 1000× larger than their dynamic conductance. In Figure 3-5(c), the dependence of g_o and g_{lin} on the channel length are shown. An aspect ratio greater than 50:1 is required to obtain a sufficiently large dynamic resistance while simultaneously providing the large current per tip required for high performance field emitter arrays. The saturation current is shown in Figure 3-6.

We followed the sensitivity analysis approach originally proposed by Hong et al. [60] and adopted by Velásquez-García et al. [125] to determine the dynamic resistance ($r_o = 10^{11}\ \Omega$) required for uniform emission current. Increasing the aspect ratio much beyond 100:1, however, gives diminishing returns, with the output conductance, linear conductance, and saturation current approaching asymptotic values. In addition, current limiters with aspect ratios larger

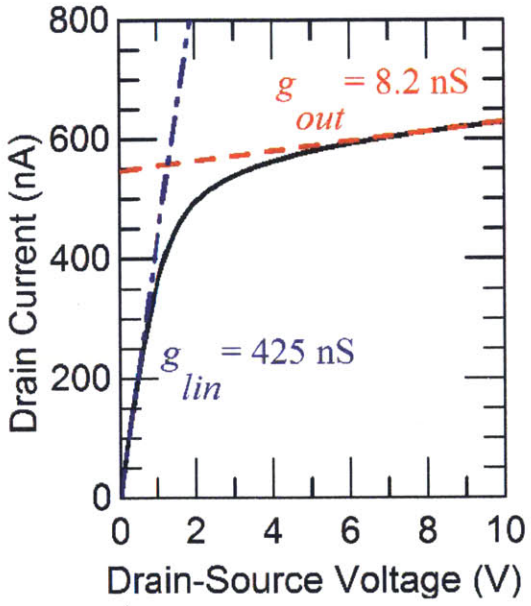


Figure 3-4: Representative simulation of a silicon nanowire current limiter with 200 nm diameter, length of 8 μm, and $N_D = 5 \times 10^{15}$ cm^{-3}.

than 100:1 further complicate fabrication. Based on these simulations, wafers with doping density of 2×10^{14} cm^{-3} and a target pillar height of 10 μm (corresponding to a pillar aspect ratio of 100:1) were chosen to theoretically obtain devices with a saturation current of 1 nA/pillar and an output resistance $> 10^{11}$ Ω.

Our simulation results predicted the saturation current, output conductance, and linear conductance that were about a factor of 30 larger than what was extracted from I-V characterization of the fabricated devices. There are several important phenomena in the fabricated Si nanowire devices that these simulation models did not capture. The first is that doping tends to follow a Poission distribution. With a doping density of 2×10^{14} cm^{-3}, assuming a Poisson distribution of dopant atoms, there are approximately 35 donor atoms in the entire 10 μm long channel. Because of the small number of dopant atoms, we expect random dopant fluctuations (RDF) to result in large variations from nanowire to nanowire. Additionally, due to the electrostatics of the nanowire, the effective doping can be even lower due to incomplete donor ionization [29, 28].

Interface traps at the Si/SiO_2 interface, D_{it} have a substantial impact on the silicon nanowire current limiters. For a complete treatment of the effect of interface traps on the Si nanowire, see Section F. While RDF and interface traps typically manifest themselves as threshold voltage shifts in MOS devices [59, 76, 112]; in the nanowire, both RDF and interface traps directly affect the channel conductivity, and in large part explain the variation of saturation currents and linear conductivities measured in the actual devices. With low doping and moderate interface trap density, the models suggest that it is possible to fully deplete the nanowire without any voltage applied.

3.4 I-V Characteristics

I-V characterization took place in a probe station using an Agilent 4156C semiconductor parameter analyzer. During the measurement, the substrate (and the source end of the channel) was held at 0 V, and a positive voltage, V_{DS}, was applied to the drain contact. Table 3.1 is a summary of experimental I-V measurements performed. In general, the devices demonstrate excellent current saturation, with a saturation current (I_{DSS}) of approximately 15 pA/pillar and

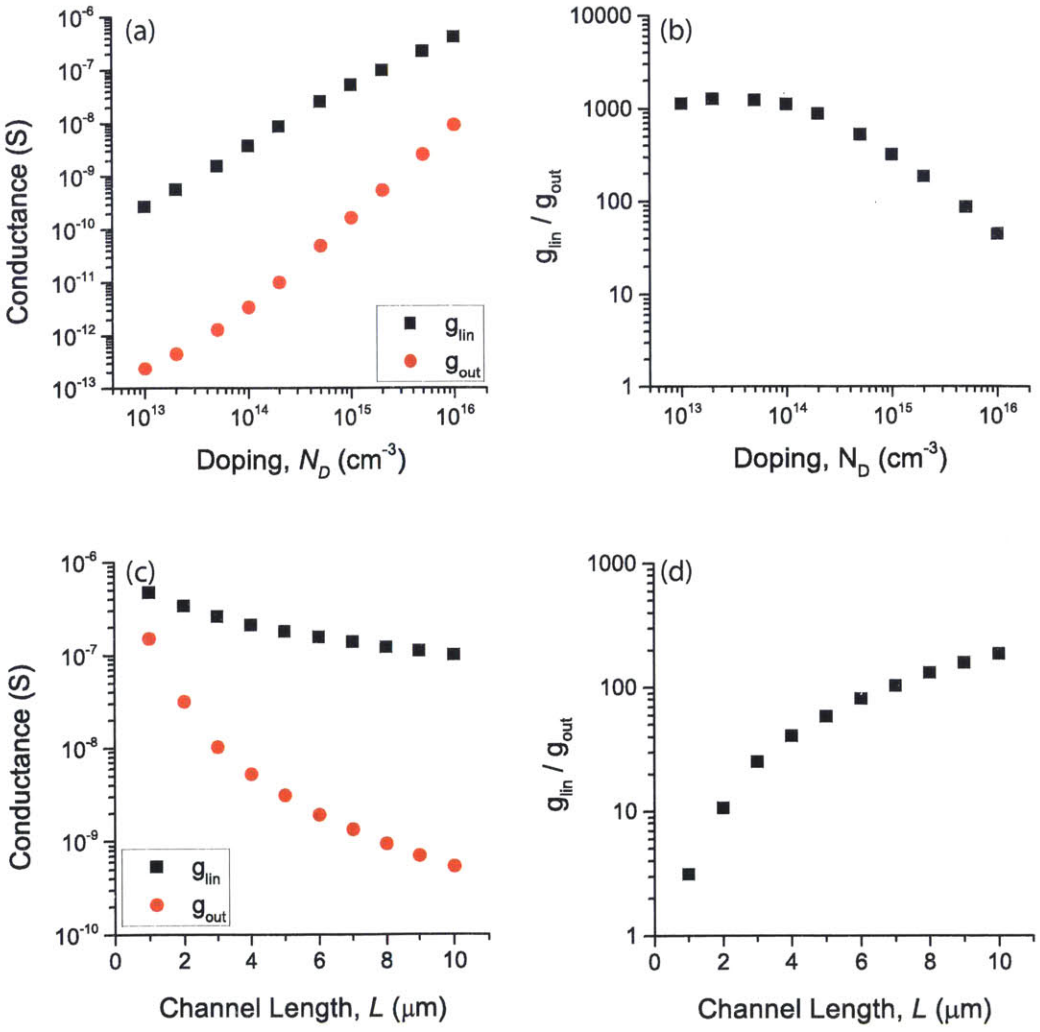


Figure 3-5: (a) Effect channel doping has on linear and output conductances with a channel length of 10 μm. (b) g_{lin}/g_o vs. doping. (c) Effect channel doping has on linear and output conductances with a channel doping of 5×10^{14} cm^{-3}. (d) g_{lin}/g_o vs. channel length.

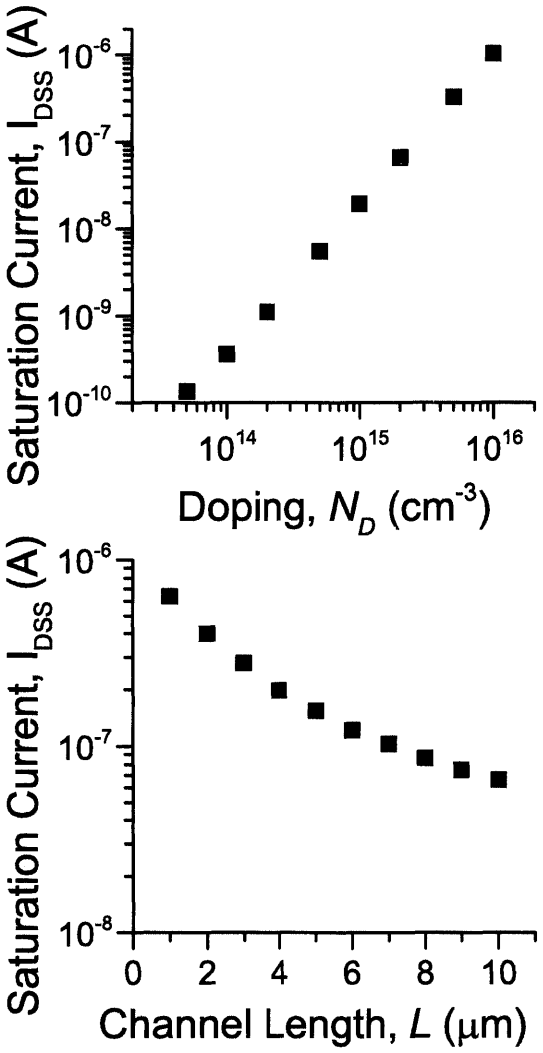


Figure 3-6: (top) Effect channel doping has on saturation current with a channel length of 10 μm. (bottom) Effect channel length has on saturation current with a channel doping of 5×10^{14} cm^{-3}.

an output conductance (g_{lin}) less than 1.8×10^{-13} S/pillar. The current saturates at a drain-to-source saturation voltage (V_{DSS}) under 0.2 V. A linear conductance ($g_l in$) of up to 2.6×10^{-10} S/pillar was measured.

To ensure that the resistance was not a direct result of contact resistance, transfer length measurements (TLM) were performed. From the TLM structures, a specific contact resistance was 3.2×10^{-3} Ω/cm^2 was obtained, resulting in an estimated contact resistance of 3.80×10^7 Ω

to the pillar, several of orders of magnitude less than the linear resistance. The above extraction of contact resistance likely underestimates the contact resistance to the pillars, as the contact openings in the TLM test structures were 300 μm × 10 μm, whereas the pillar cross-section is 100 nm × 100 nm.

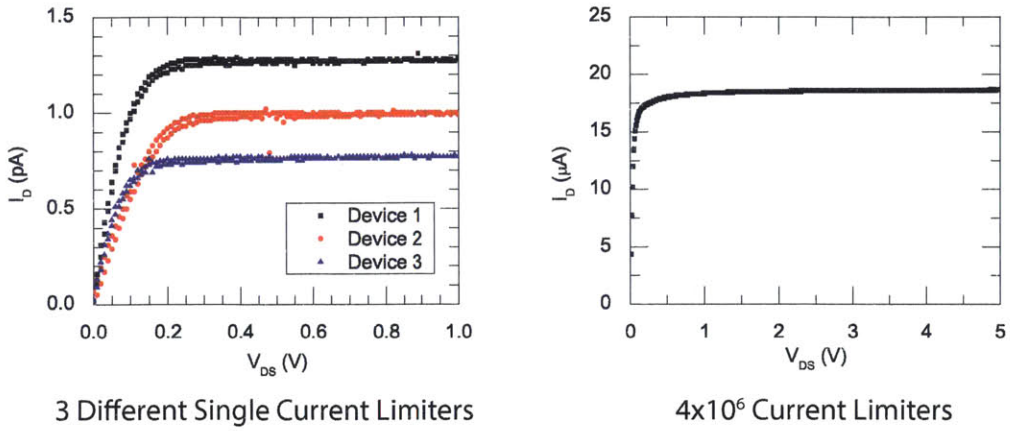


Figure 3-7: I-V Characteristics of single current limiters (left) and an array of 4×10^6 current limiters (right).

Figure 3-7 shows the I-V characteristics for several single current limiters in a single array and an array of 4M current limiters, and Table 3.1 summarizes the I-V characterization for many different array sizes. These I-V characteristics demonstrate the current limiting capabilities of the scaled current limiter structure.

The measured current/nanowire is much lower than the both the analytical model and the numerical simulations predict. Two non-idealities that could impact the electrical characteristics and ultimate performance of silicon nanowires are the effect of the Si/SiO_2 interface along the surface of the nanowire and the incomplete donor ionization that results in silicon nanowires. For a discussion of incomplete donor ionization, please see Appendix E. The effect of interface states is covered in detail in Appendix F. Briefly, as the diameter of the nanowire is reduced, the surface-to-volume ratio increases and surface effects can become a limiting factor to performance. Incomplete donor ionization does not appear to be a factor in the current limiters, but for the doping density and device geometry chosen, the interface charge Q_{it} that arises from a moderate interface trap density could fully deplete the Si nanowires.

Size of Array	IDSS/pillar [pA]	VDSS [V]	glin/pillar [pS]	gout/pillar [pS]
1	8.5	0.06	150	0.33
4	0.50	0.20	6.7	0.18
5	1.3	0.20	12	0.061
8	2.2	0.80	28	0.096
62.5k	2.6	0.01	23	-
125k	1.8	0.08	22	-
250k	1.9	0.06	33	-
500k	2.1	0.06	38	0.0060
1M	15	0.15	250	0.090
2M	10	0.08	42	0.022
4M	4.7	0.05	99	0.0065

a. Indicates negative resistance in the saturation regime

Table 3.1: MEASURED CURRENT-VOLTAGE CHARACTERIZATION DATA

To explore the effect of temperature on current-voltage relationship of silicon nanowire current limiters and explore the trap occupancy/density, we collected several $I_D - V_{DS}$ sweeps of a silicon nanowire current limiter at different temperatures, ranging from 274 K to 403 K. The current-voltage characteristics are shown in Figure 3-8. The linear conductance, g_{lin} and saturation current I_{sat} were extracted from the I-V characteristics, and plotted on a semilog scale. The activation energy of both the saturation current and the linear conductance varies with $\simeq E_g/2$.

In a semiconductor that is extrinsically doped, the majority carrier concentration and thus the current-voltage characteristics of majority carrier devices devices should not shift very much over this temperature range. This strong temperature dependence of the I-V characteristics with activation energy $\simeq E_g$ suggests that perhaps the nanowire is fully depleted, consistent with the modeling of interface states. The temperature dependence of the intrinsic carrier concentration n_i can be modeled near room temperature as:

$$n_i = \sqrt{n_0 \cdot p_0} = \sqrt{N_c N_v}\left(\frac{T}{300}\right)^{3/2} \exp\left(-\frac{E_g(T)}{2kT}\right) \tag{3.8}$$

Where n_0 and p_0 are the equilibrium electron and hole concentrations, respectively, N_c and N_v are the effective density of states in the conduction and valence bands at 300 K, respectively, and E_g is the band gap of silicon. Around 300 K, the temperature dependence of E_g is roughly

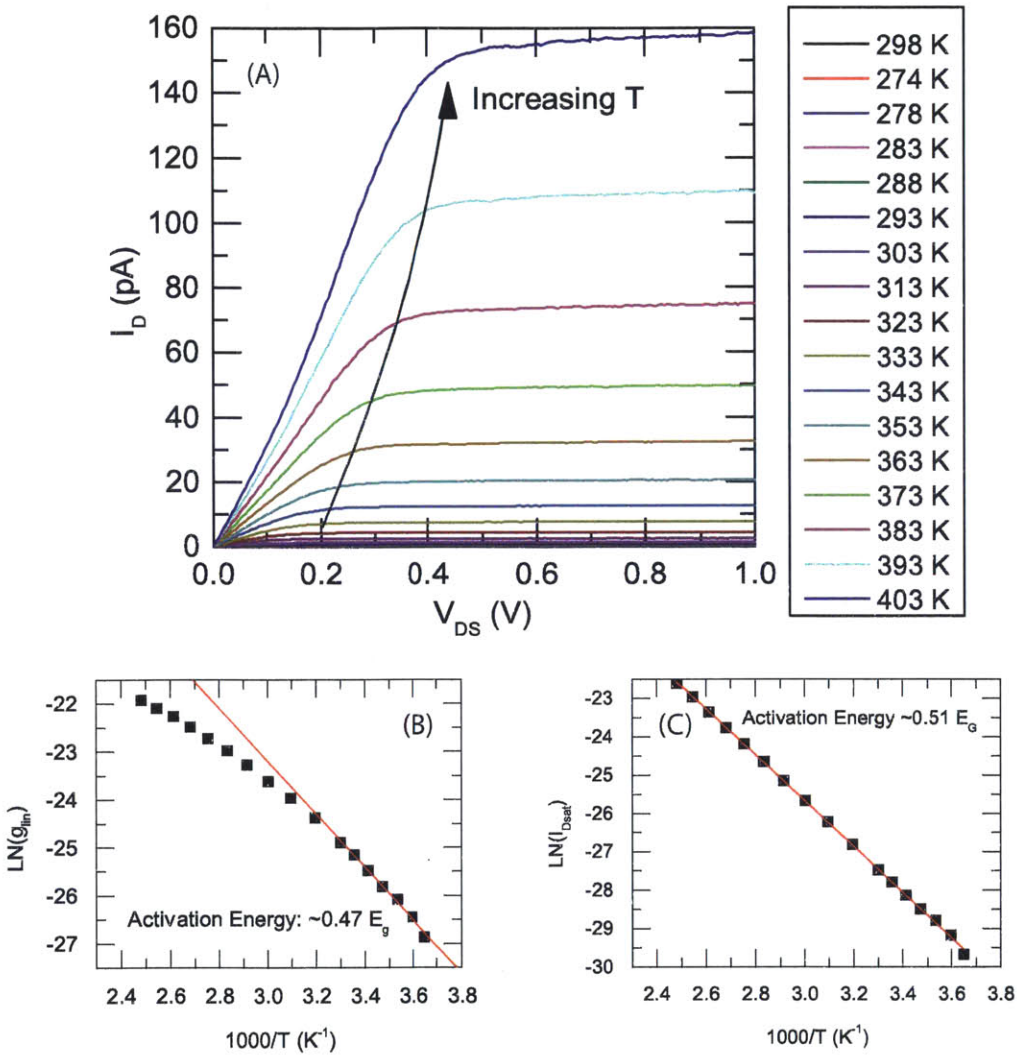


Figure 3-8: (A) Current-voltage characteristics of a single SiNW at a variety of different temperatures. (B) Arrhenius plot of linear conductance, g_{lin} shows a nearly linear relationship, with an activation energy of $\sim E_g/2$ (C) Arrhenius plot of saturation current, I_{sat} shows linear relationship, with an activation energy of $\sim E_g/2$.

linear, and can be modeled as $E_g(T) = E_{go} + C\,T$ where $E_{g0} = 1.206$ and $C = 2.73 \times 10^{-4}$ [26]. If we assume that the nanowire is fully depleted due to interface traps, the saturation current is:

$$I_{sat} = qA_{NW}n_i v_{sat} \tag{3.9}$$

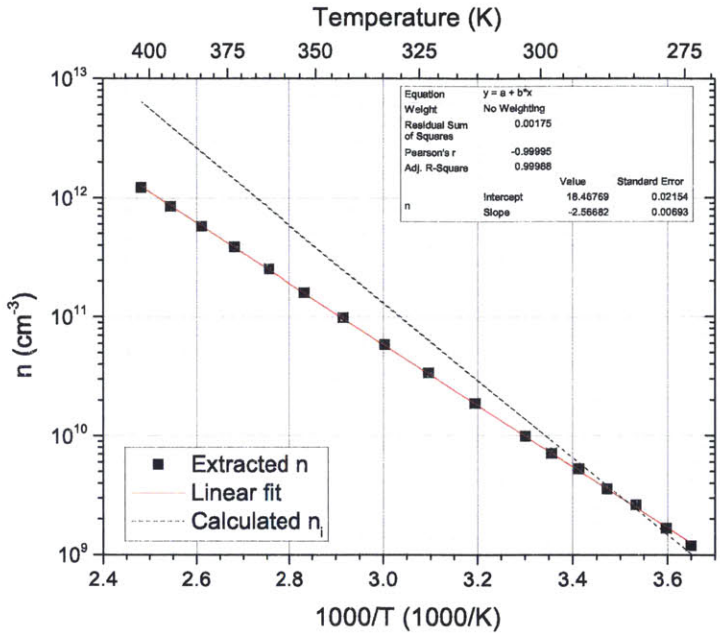


Figure 3-9: Comparison of the n_i extracted from the saturation current to a model for intrinsic carrier concentration, assuming a nanowire radius of 50 nm.

Where n_i is the intrinsic carrier concentration and v_{sat} is the saturation velocity of electrons. A comparison of the n_i extracted from the saturation current to the model in Equation 3.8 is shown in Figure 3-9. Using the current to extract the intrinsic carrier concentration tends to underestimate the temperature dependence at $T > 300$ K. A possible explanation for this difference is that a fraction of the carriers injected into the depleted Si nanowire are recombining at the Si/SiO_2 interface. The interface traps have a surface recombination velocity (SRV) S associated with them which depends on the interface trap density D_{it} and the capture cross-section σ. The recombination velocity gives rise to a recombination current:

$$I_{rec} = A_{surf} q S n_i \tag{3.10}$$

where A_{surf} is the surface area of the nanowire ($A_{surf} = 2\pi r L$). It has been suggested in the literature that the surface recombination velocity, S, has a temperature dependence[44]. If the difference in the intrinsic carrier concentration extracted from the I-V characteristics and the model is due to surface recombination, we can estimate S from the difference between the two.

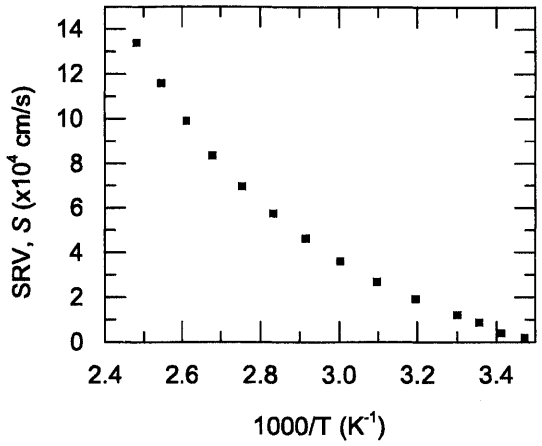


Figure 3-10: Estimation of surface recombination velocity from the I-V characteristics

Figure 3-10 shows the estimated surface recombination velocity as a function of temperature. The estimated surface recombination velocity ($\sim 10^4 - 10^5$ cm/s) is higher than expected for a well-passivated Si/SiO_2 interface.

These results suggest that the lower than expected drain current of the nanowire current limiters is likely due to a combination of depletion by the interface trap density and recombination at the silicon nanowire surface.

3.5 Array Effects

Another phenomenon not taken into account by previous simulations is the effect of neighboring nanowires when they are arranged in an array. In the case of the simulations of the single nanowire, the area surrounding the nanowire is etched and a region of quasi-neutral silicon spaced about half a micron away from the nanowire remains. When a positive voltage is applied to the top of the nanowire, using the gradual channel approximation, the drain end of the nanowire will be at V_{DS}. The substrate, some distance away, will remain approximately ground. This substrate acts like the gate in a MOSFET and will form a depletion region in the nanowire. Depending on the doping and the geometry of the nanowire, this effect may cause channel pinchoff earlier than velocity saturation.

To explore this effect, we will analytically examine the electrostatics of two situations:

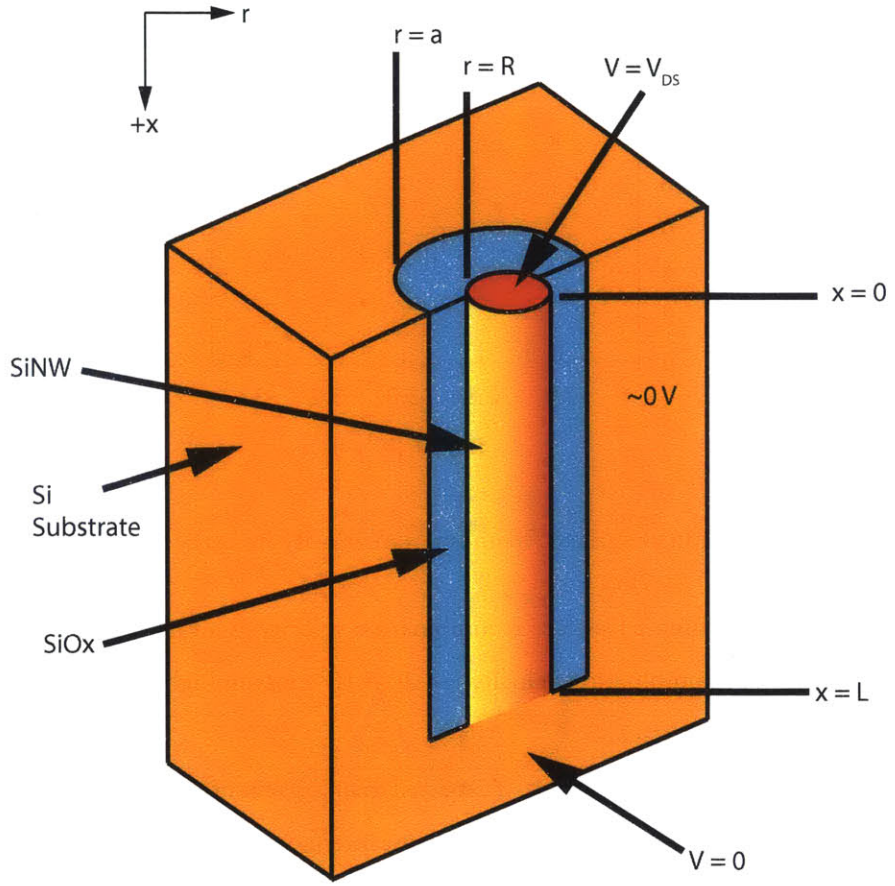


Figure 3-11: Schematic drawing of a silicon nanowire surrounded by oxide and a neutral substrate. the substrate/oxide/nanowire structure forms a parasitic, unwanted MOS structure.

1. A cylindrical nanowire surrounded by the substrate (Figure 3-11)

2. a cylindrical nanowire buried in oxide with the substate very far away

Following the analytical treatment of this problem, we will present numerical, 3-D device simulations. To treat this problem analytically, we will make arguments similar to those used when treating 2-D planar MOSFETs, but solving Poisson's equation in cylindrical coordinates as was performed in the treatment of traps at the nanowire/SiO_2 interface. We consider a nanowire that is uniformly doped and cylindrical, with radius R. The uniform doping in the semiconductor is equal to the substrate doping. The oxide is uniform, and has thickness $t_{ox} = a - R$. The nanowire is L microns long. We make (1) the gradual channel approximation,

where we assume that the the vertical electric field along the channel varies much slower than the radial electric field i.e. $\partial E_x/\partial x \ll \partial E_r/\partial r$ (2) The full depletion approximation, in that space charge $\rho(x,y) = 0$ when the semiconductor is quasineutral, and $\rho(x,y) = qN_D$ where depleted. (3) Neglect any interface states or fixed charge at the Si/SiO_2 interface.

Consider this structure with a voltage V_{DS} applied between the drain of the nanowire and the substrate. At the drain end of the nanowire, the channel potential is thus:

$$V(x) = V(0) = V_{DS} \tag{3.11}$$

With the surrounding silicon substrate essentially at ground, this V_{DS} will give rise to a depletion region at the surface of the nanowire. We will denote the radius of the edge of the depletion region as r_d. From the charge neutrality condition, a corresponding accumulation layer will from in the substrate surrounding the nanowire. The charge in this accumulation layer must be equal to the space charge inside of the nanowire. These charges are denoted Q_{Acc} and Q_{NW}, respectively. Thus:

$$Q_{NW} = -Q_{Acc} \tag{3.12}$$

where:

$$Q_{NW} = q\pi N_D(R^2 - r_d^2) \tag{3.13}$$

Let us consider the case where the nanowire is on the onset of being fully depleted, i.e. $r_d = 0$. In this case, that we will define as "pinch-off", the potential at the very center of the channel is $V_{DS,sat}$, and the surface potential, ϕ_s at pinch-off is found through the solution of Poisson's equation:

$$\phi_s(x=0) = V_{DS} - \frac{qN_D R^2}{4\epsilon_{Si}} \tag{3.14}$$

The voltage drop across the oxide can be calculated with the capacitance per unit length and the charge per unit length in the semiconductor through $V = Q_s/C_{ox}$. The capacitance of the oxide is the capacitance of a coaxial structure with inner radius R and outer radius $a = t_{ox} + R$:

$$C_{ox} = \frac{2\pi\epsilon_{ox}}{\ln\left(\frac{a}{R}\right)} \tag{3.15}$$

Thus, the voltage at which pinch-off occurs is:

$$\boxed{V_{DS,sat} = \frac{qN_D R^2}{2}\left(\frac{1}{2\epsilon_{si}} + \frac{\ln\left(\frac{t_{ox}+R}{R}\right)}{\epsilon_{ox}}\right)} \tag{3.16}$$

Figure 3-12 plots $V_{DS,sat}$ against doping and t_{ox} to examine the trend of when the channel pinches off. We see that for moderately doped silicon nanowires, even with an oxide thickness $> 1\ \mu$m, the channel can pinch-off at $V_{DS} < 1V$ due to the logarithmic dependence of $V_{ds,sat}$ on $t_o x$. This suggests that even without surface states, for a pillar that is surrounded by neutral silicon at ground, the current may be less than what is expected from the intuitive model.

Based on this modeling of individual nanowires, when the silicon nanowire current limiters are in 2-D arrays surrounded by a neutral Si substrate, the current in nanowires at the corner or edge of the array will saturate at a lower drain-source voltage than those in the center of an array. The devices on the edge are at least partially surrounded by Si virtually at ground, whereas devices inside of the array will be surrounded by nanowires that have approximately the same

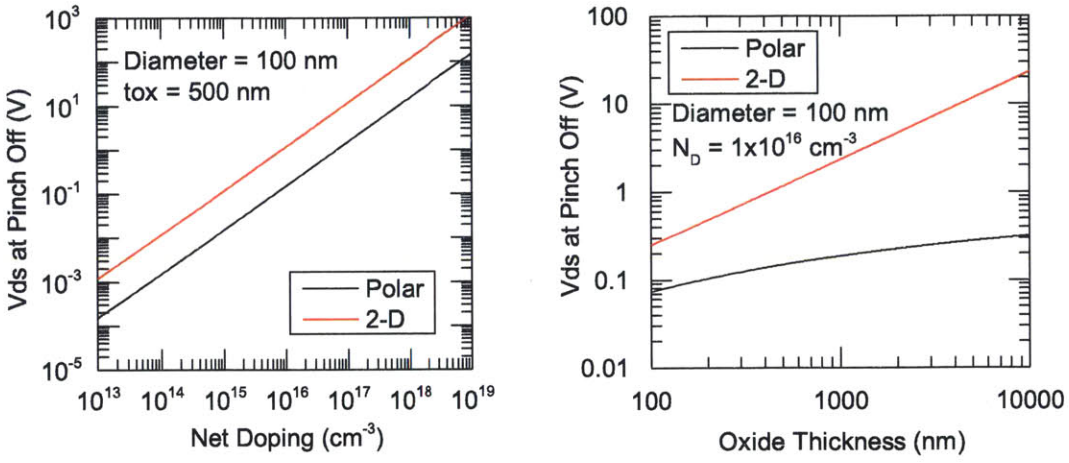


Figure 3-12: The effect of doping (left) and oxide thickness (right) on the voltage at which the channel pinches off due to the parasitic MOS structure formed by the substrate surrounding a single nanowire.

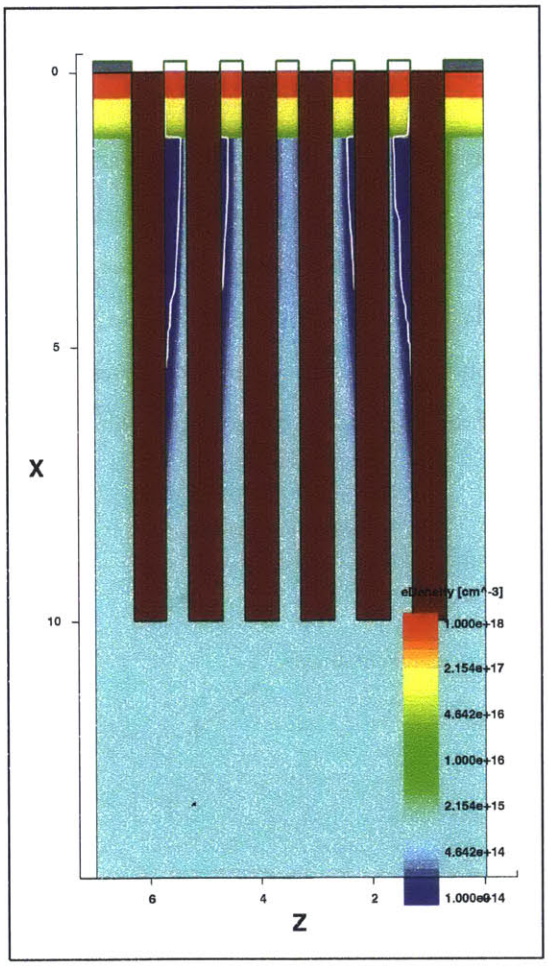


Figure 3-13: Cross-section of a simulation of a 5x5 array at $V_{DS} = 10$ V. This cross-section shows the electron concentration in the nanowires, and the depletion edge is highlighted in white, defined as electron concentrations less than 10% of the value in thermal equilibrium. This simulation demonstrates the effect of the surrounding substrate on the I-V characteristics of the nanowires.

potential distribution along their length, reducing the transverse electric field that might serve to deplete the nanowire.

To model this effect, we performed fully 3-D device simulations in Sentaurus, a Poisson equation and continuity equation solver, similar to SILVACO, but with better handling of 3-D structures and simulation domains with many nodes. We generated 5x5 and 10x10 arrays of Si nanowires, and swept the drain-source voltage, measuring the current in each individual nanowire. The electron concentrations in the various pillars across a cross-section cut through the center of the 5x5 array at $V_{DS} = 10$ V is shown in Figure 3-13. As expected based on the analytical calculations of individual nanowires above, the pillars at the edge of the array saturate at a lower voltage and at lower currents due to the gate effect of the surrounding neutral semiconductor. The depletion region forms on the side closest to the edge of the array, and extends towards the center of the array as the drain-source voltage in increased.

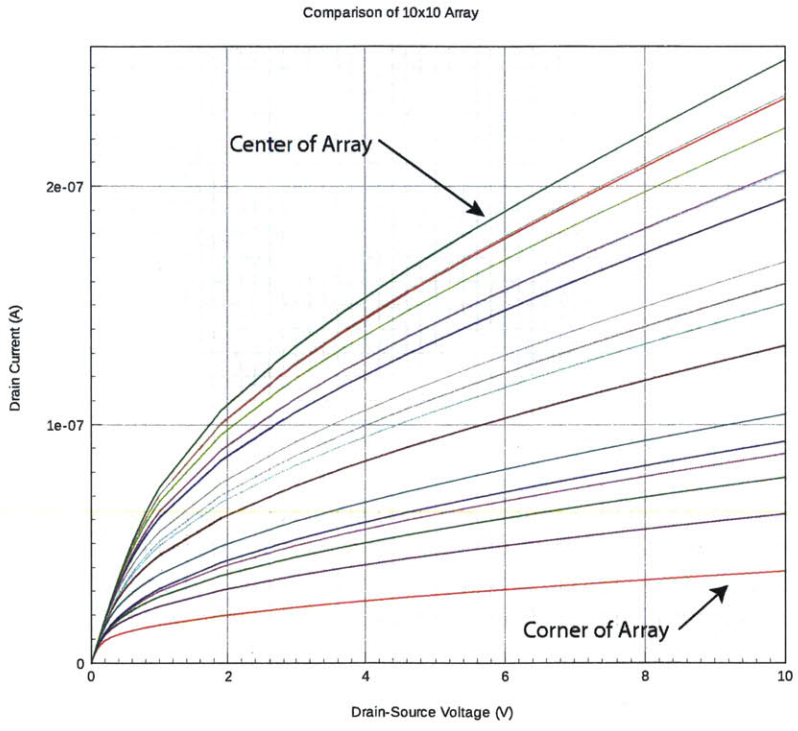


Figure 3-14: Comparison of I-V Characteristics across a 10x10 Array, demonstrating the effect of the substrate on the current limiter. The current limiters along the periphery saturate at lower currents than those in the center.

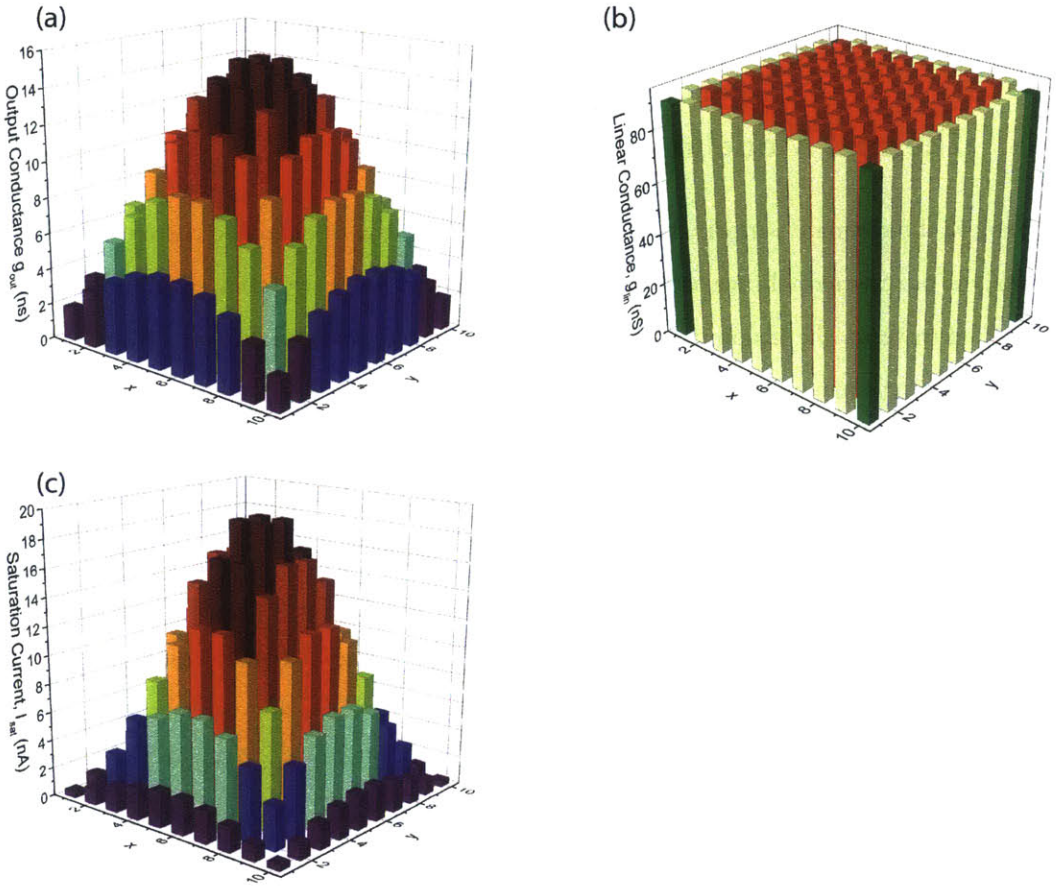


Figure 3-15: Comparison of output conductance (a), linear conductance (b), and saturation current (c) for each position in the 10x10 array.

Figure 3-14 shows the individual I-V characteristics of current limiters in a 10x10 array as simulated in Sentaurus. The emitters are all connected in parallel, and their currents measured individually as the drain-to-source voltage is ramped from 0-10 V. While linear conductance does not appear to be sensitive to position in the array, between the edge and the center there can be as much as a factor of 5 variation in saturation current I_{DSS} from this effect, and a factor of 6 difference in output conductance, g_{out}. These results are summarized in Figure 3-15.

It may be possible to mitigate this effect by varying the diameter of the nanowire based on its position in the array, making the nanowires closer to the edge larger than the nanowires in the center, however a remaining challenge is to keep the emitter tip radius uniform while changing the nanowire diameter. To enable uniform emitters with varying nanowire, it may be

possible and necessary to decouple the emitter formation from the nanowire formation.

3.6 Thermal Modeling and Analysis

To explore the ultimate performance and failure mode of the Si nanowire current limimters, an analysis of the thermal breakdown of the silicon pillars was performed. Experiments were conducted to verify the maximum possible current sourced before failure of the current limiter. Several single nanowire current limiters were characterized under conditions where current was varied and voltage was measured until thermal runaway and device failure occurred. Figure 3-16 shows a representative voltage-current characteristic, which exemplifies the failure that occurred. I-V characteristics of the device were taken before and after stressing. Before stressing, the device had a saturation current of 8 pA. At a bias current of 11 pA, impact ionization in the high-field region of the channel was observed, resulting in a large change in current with small increase in voltage. At a current level of 200 nA, the device failed and the measured voltage hit compliance, indicating that an open circuit has formed. The inset of Figure 3-16 shows an optical micrograph of the metal contact pad after stressing, showing physical damage resulting from the destructive testing: a large crater in the metallization centered on the location of the single pillar contact.

Following the analysis of the thermal limits of field emitters presented by Utsumi in [122], the maximum current density at burn-out due to Joule heating approximated by:

$$i_{max} = \frac{\sqrt{2T_m\tilde{\sigma}k}}{h} \tag{3.17}$$

where h is the height of the structure, T_m is the melting temperature of silicon, $\tilde{\sigma}$ is the average value of electrical conductivity, taken between room temperature and T_m, and k is the thermal conductivity of silicon. Using the thermal conductivity and electrical conductivity values for n-type silicon with a donor concentration of 2×10^{14} cm^{-3}, a value of 100 nA for I_{max} ($I_{max} = i_{max} \times$ cross-sectional area) is obtained for a 100 nm diameter column, agreeing with the experimental value of 200 nA to within a factor of 2.

To perform more rigorous thermal modeling, we switched to finite element analysis. To model the breakdown and heating in Si nanowires, a hydrodynamic model [118] implemented

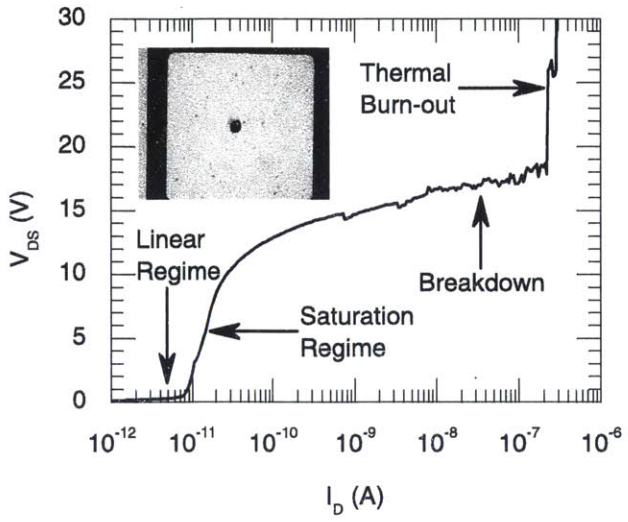


Figure 3-16: Schematic drawing of a silicon nanowire surrounded by oxide and a neutral substrate. the substrate/oxide/nanowire structure forms a parasitic, unwanted MOS structure.

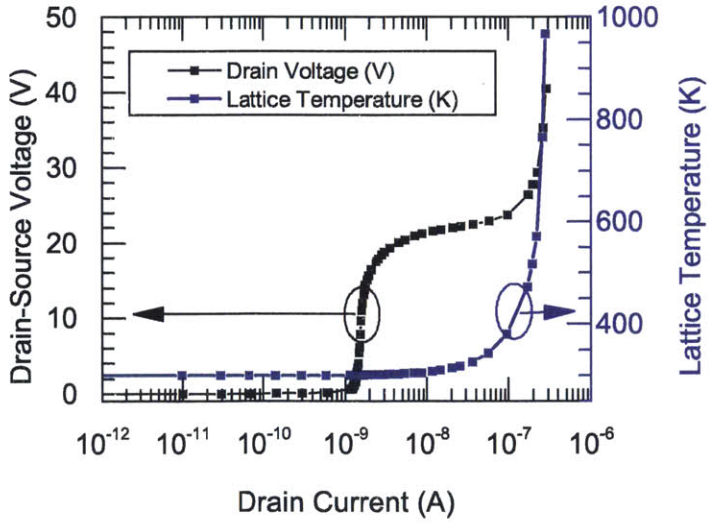


Figure 3-17: Simulation of heating and avalanche breakdown in a silicon nanowire using the hydrodynamic models.

in Sentaurus was used. The hydrodynamic model is a set of three energy balance equations that are solved self-consistently with the Poisson equation and the carrier continuity equations in the semiconductor to give impact ionization rates and heating of the semiconductor lattice. The boundary conditions were set so that that the backside of the wafer was a perfect thermal

conductor, and the top of the nanowire was a perfect thermal insulator. The sides of the simulation domain were set to be reflecting boundaries (*i.e.* $\nabla T_{\perp} = 0$). The results of the simulation are shown in Figure 3-17. A nanowire diameter of 100 nm, a length of 10 μm, and doping of $2 \times 10^{1}5$ cm^{-3} were used.

The simulation accurately predicts that breakdown of the device occurs at approximately 2×10^{-7} A, and the model predicts a breakdown voltage of $\sim$ 23 V, compared to the actual breakdown voltage of 19 V. The model has its limitations, however. It does not accurately predict the saturation current of the nanowire. This is expected, as surface states were not included in the simulation model.

3.7 Summary

This chapter presented analytical models, numerical simulations, and measured I-V characteristics of silicon nanowire current limiters. Analytical results and numerical modeling gives insights into the effect of the silicon nanowire surface on current limiter performance and shows that the surface depletion layer that arises from interface traps could have a large effect on device performance. 3-D simulations show that the saturation current depends on the position of the nanowire in the array, and that current limiters towards the edges of the array saturate at lower voltages and lower currents than devices in the center of the array from a gate-effect of the surrounding substrate. Through understanding these effects, methods of minimizing rheir impact on the performance of the field emitter array can be developed.

Chapter 4

Ungated Silicon Field Emitter Arrays with Nanowire Current Limiters

4.1 Introduction

The purpose of this chapter is to present a proof-of-concept structure that demonstrates that a scaled silicon field emitter array with silicon nanowire current limiters is feasible. This device is the first to demonstrate current saturation in scaled silicon field emitter arrays with silicon nanowire current limiters. Due to the distance between the gate electrode and the emitter tip, electrostatic screening limited the emitter-to-emitter to 5 μm. SEM imaging of the completed structure demonstrated a tip radius < 6 nm with a standard deviation of 1.2 nm. The result is shown to be consistent with both analytical and finite element models.

4.2 Design

During the design process, we performed numerical simulations to guide the design of emitter and extractor gate geometry. DC steady-state simulations were performed using the COMSOL Multiphysics simulation package. In the simulations, a 100-nm diameter, 10-μ tall pillar that is topped with a cone with 15° half-angle. Emitter tip radius was fixed at 5 nm. A diode configuration was employed, where an equipotential surface was placed a distance x away from the emitters with tip-to-tip spacing of y. The emitter-anode separation was varied from 0.1

μm < x < 20 μm, and the tip-to-tip separation was varied from 1 μm < y < 20 μm. The simulation is a 2-D simulation, thus it is expected that the field factor extracted from this simulation will be slightly lower than would be the case in a full 3-D simulation; however, the simulation still gives valuable insight into the expected screening effects of the ungated array. Figure 4-1 shows the details of the simulation structure.

At the simulation boundary on the right side, a symmetry boundary condition was enforced. This boundary condition sets the normal electric field equal to zero (i.e. $d\Phi/dy = \mathcal{E}_{\perp} = 0$) and the charge at the interface equal to zero (i.e. $\rho_s = 0$). This boundary condition allows for the simulation to cover half the size, and still include appropriate interactions. 5 emitters are simulated, and by measuring the maximum electric field at the emitter furthest from the edge, perimeter effects are much reduced approximating what the field at the center of the array is expected to be. Because the simulation was a two-dimensional (2-D) simulation, the field enhancement at the tip may be somewhat lower than in the 3-D case; however, valuable insight may still be gleaned from these results.

During the simulation, the potential at the top of the simulation area was set to 1 V, and then the highest electric field at the tip of the furthest emitter from the edge of the array. This electric field is the field factor, β. From β, the Fowler-Nordheim slope b_{FN} is extracted using

$$b_{FN} = \frac{0.95 \cdot 6.87 \times 10^7 \cdot \chi_{Si}^{3/2}}{\beta} \tag{4.1}$$

Where χ_{Si} is the electron affinity of silicon (4.05 eV). b_{FN} has important implications for the performance of field emitters, and a lower b_{FN} implies lower voltage operation. $b_{FN} \approx 5000$ V implies a turn-on voltage, $V_{ON} \sim 200$ V. Figure 4-2 shows the effect of varying the emitter pitch and the tip-anode spacing on b_{FN}.

Examining the field lines shown in Figure 4-1A, due to the prominence of the emitters in the periphery of the array, the curvature of the potential is higher around these emitters resulting in a higher surface electric field.

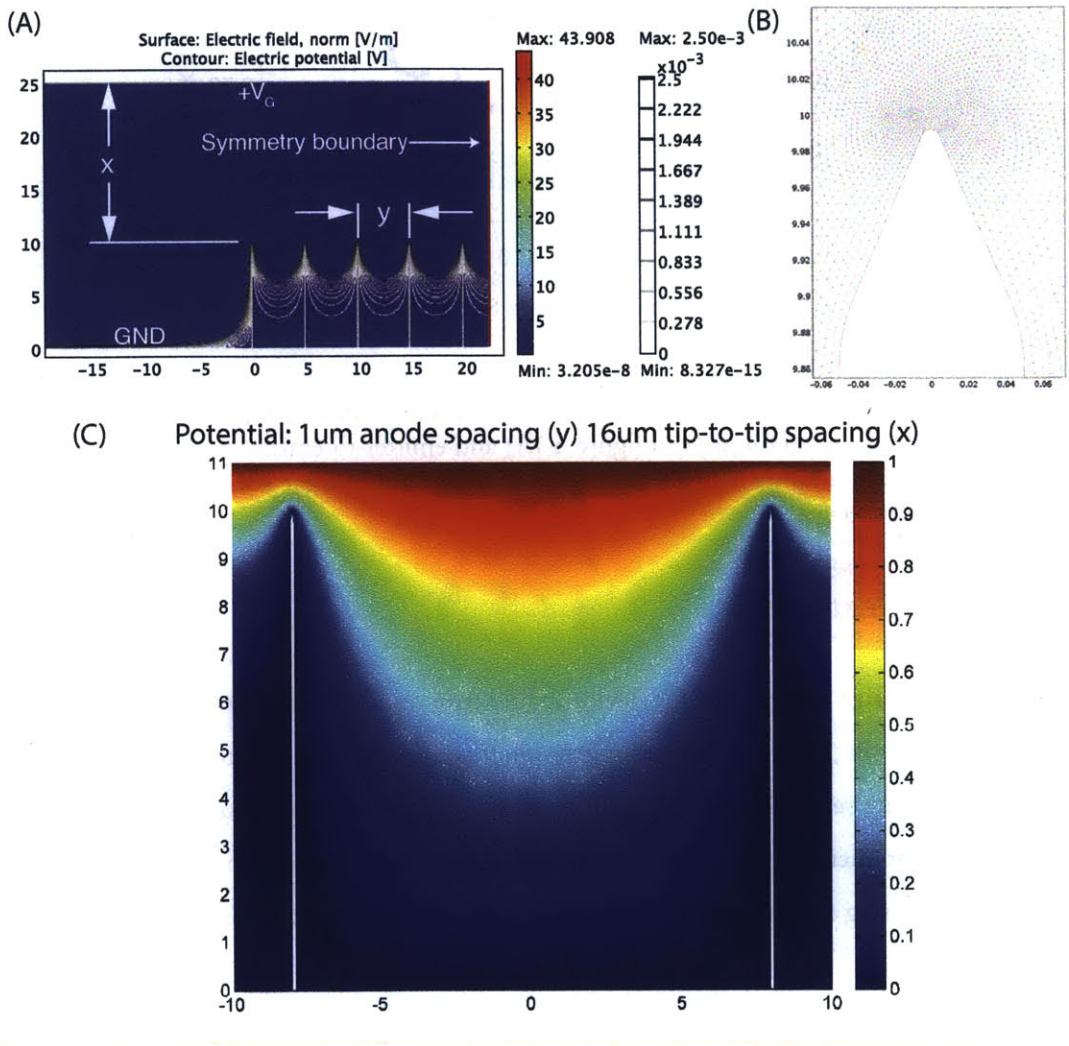


Figure 4-1: (A) Simulation structure for the exploration of the screening effects of adjacent emitters. The simulation shows the electric field as shaded colors, and the equipotential lines. Units of all of the axes in this figure are in microns. (B) Detail of the emitter tip meshing used in this simulation. (C) Detail of the normalized potential (shaded) surrounding 2 emitter tips in a simulation structure. The anode-emitter spacing is $x = 1$ μm and the emitter-to-emitter pitch is $y = 16$ μm.

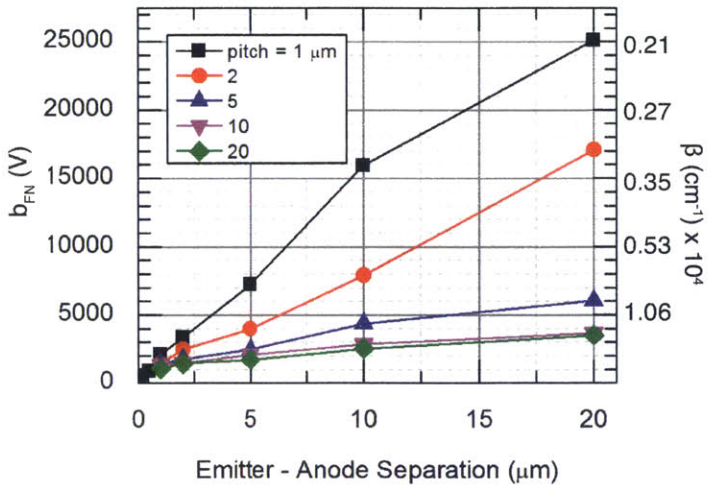


Figure 4-2: screening effect of adjacent tips on the Fowler-Nordheim slope, b_{FN} as a function of different tip-anode separations (x in figure 4-1A) and emitter-to-emitter pitches (y in figure 4-1A). A higher b_{FN} implies a smaller field factor and hence a larger effective tip radius and a higher turn-on voltage.

4.3 Fabrication

Based on the design criteria that the device should turn on at a gate-emitter voltage under 200 V, a structure with 5 μm emitter-to-emitter pitch and a substrate-to-gate separation of $\sim$ 25 μm (emitter-gate separation of $\approx$ 15 μm) was chosen. These design choices were a trade-off that allowed for microfabrication of the field emitter array, and hand-assembly of the extraction gate structure using commercially available polymer spacers as standoffs for the extraction gates.

The combined silicon nanowire current limiter-FEA structure was fabricated with 5 μm pitch and hexagonal packing, and the device was expected to turn on at a gate-emitter voltage of approximately 200 V. Thermal oxide was grown, and photolithography was performed to define "dots" that would define the emitter locations. After the patterning of the oxide with reactive ion etching, the initial formation of the emitter cones is performed using a plasma etch with SF_6/O_2 chemistry. The partial pressure of oxygen changes the lateral etch rate, while barely changing vertical etch rate, allowing for control over the etch profile.

The undercutting step needed to be precisely controlled to obtain a sharp tip after the oxidation to reduce the pillar diameter. After the tip formation, the pillar is etched using the

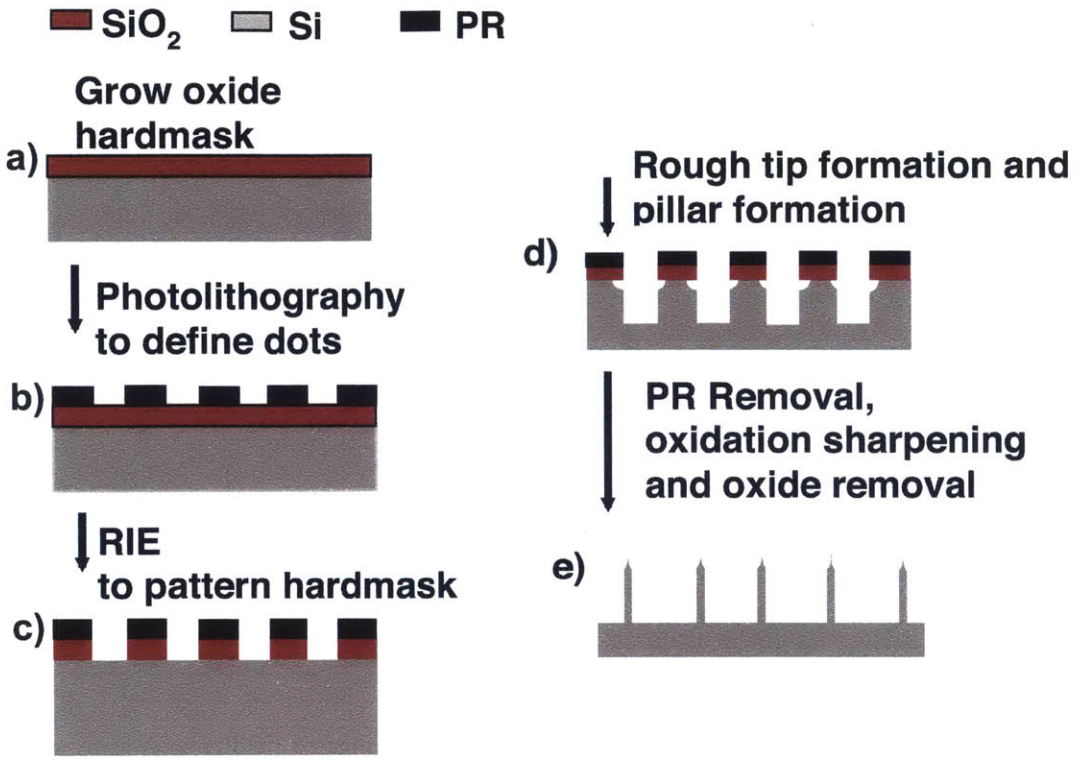


Figure 4-3: Schematic cross-section of the fabrication steps for building ungated field emitter arrays with integrated nanowire current limiters.

same DRIE process as in the vertical current limiter process. Following the DRIE step, the structure was oxidized at 1000°C using dry O_2 to simultaneously form sharp emitter tips while reducing the pillar diameter. Finally, the thermally grown oxide is removed using 10:1 diluted HF. An SEM image of the completed structure is shown in Figure 4-4. The pillars are 10 μm tall, with a diameter of 110 nm and a tip radius under 10 nm. Figure 4-6 shows representative SEM images of the emitter tips after field emission testing. Figure 4-5 is a plot of the radii of 209 tips and Figure 4-6 shows some representative SEM images of the emitter tips. The statistics follow a log-normal distribution with a mean of 5.6 nm and a standard deviation of 1.3 nm. The tip radius measurements were made using SEMs taken after the device characterization; hence they are representative of the actual device dimensions.

The full fabrication process flow for the fabrication used for these devices is included in Appendix H.

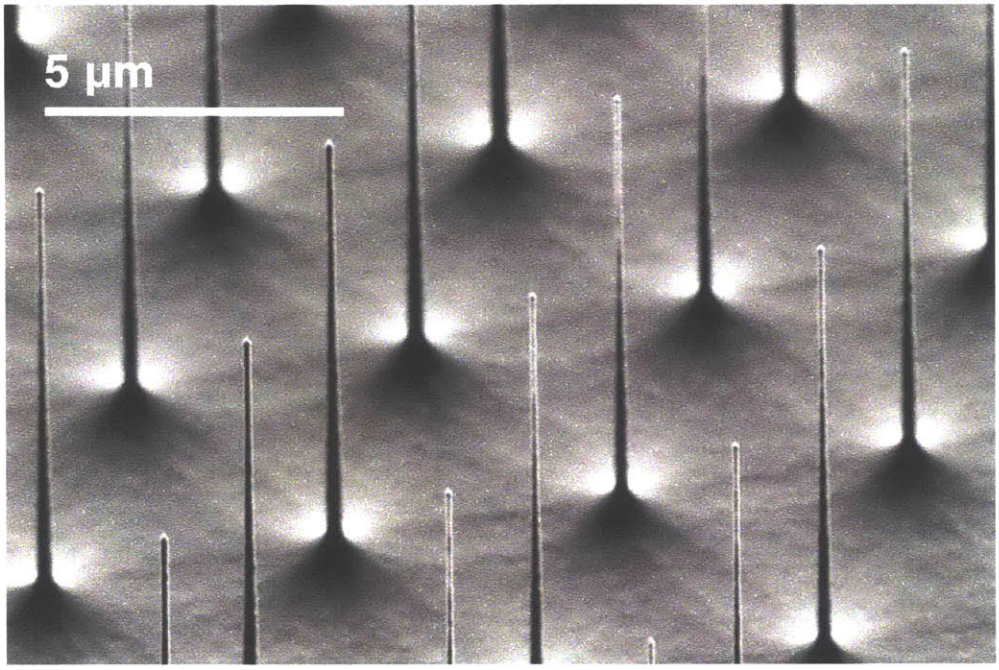


Figure 4-4: Scanning electron micrograph of the completed ungated field emitter array with integrated silicon nanowire current limiters. The device has 5 μm pitch, and the current limiters are 100 nm diameter and 10 μm tall.

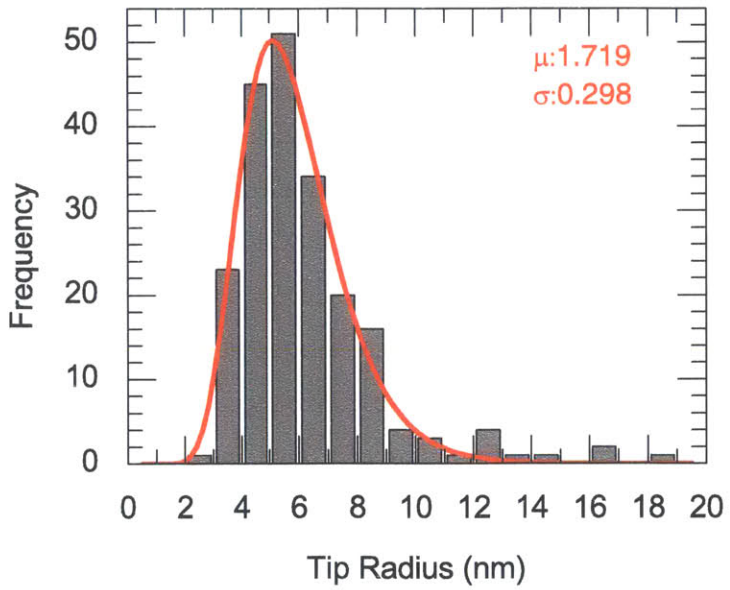


Figure 4-5: Tip Radius statistics for 209 emitters measured with SEM. The distribution is log-normal with a mean of 5.6 nm and a standard deviation of 1.3 nm.

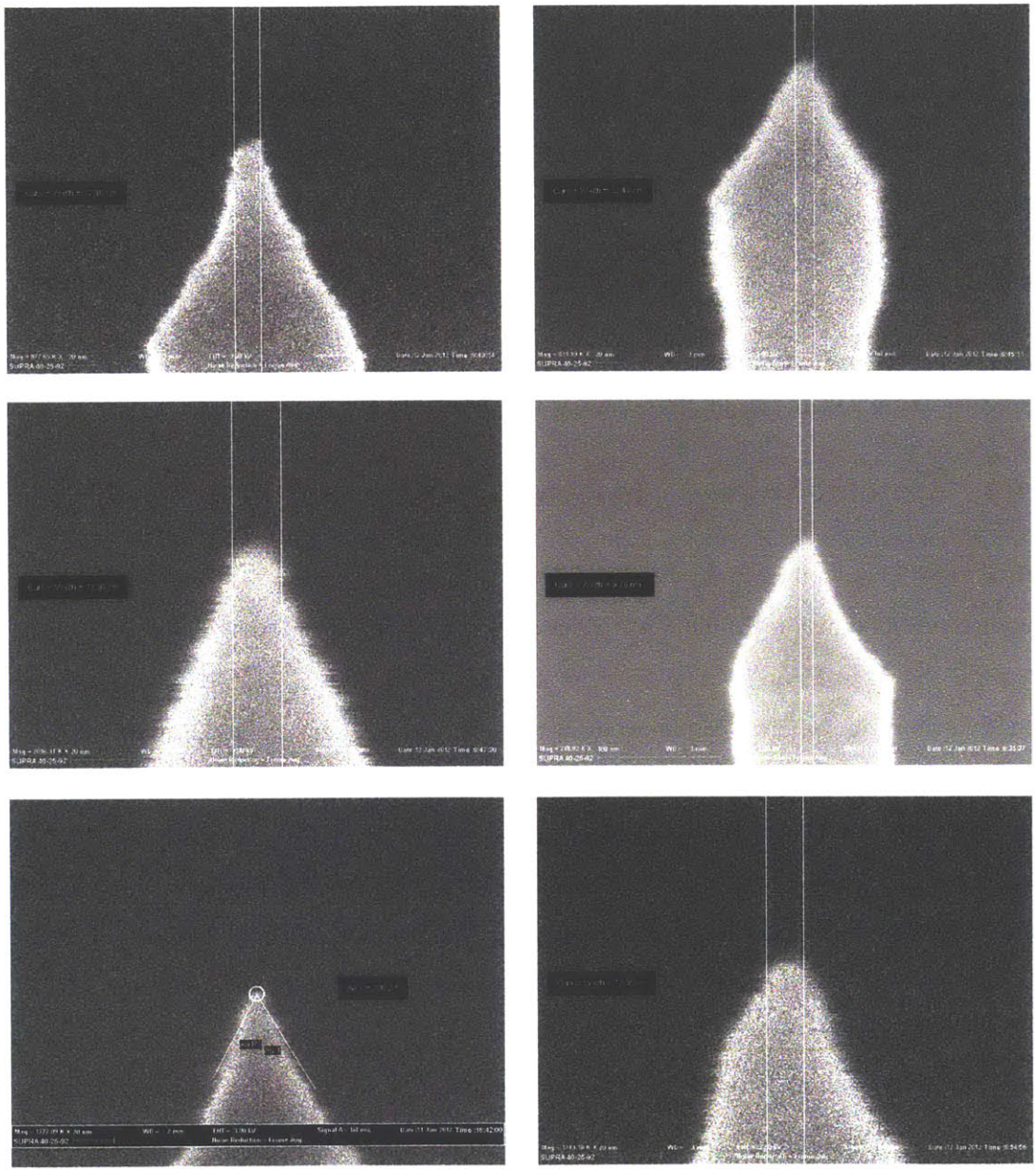


Figure 4-6: Representative SEM images of emitter tips used to generate the statistics shown in Figure 4-5

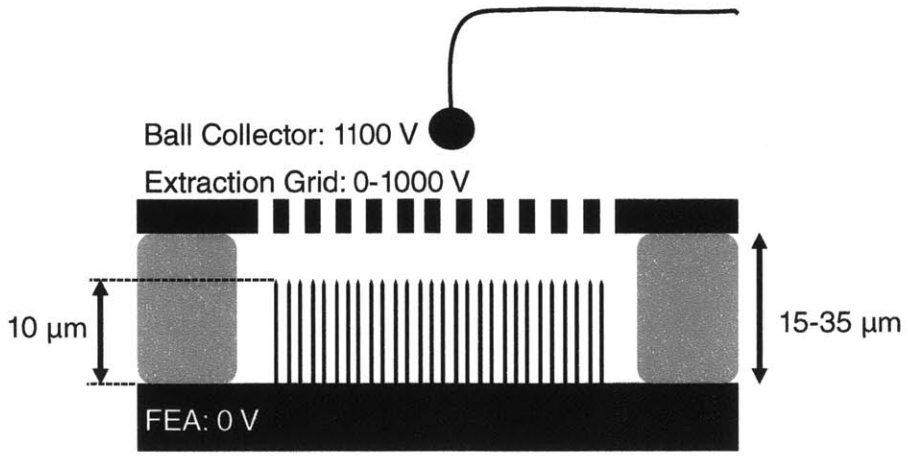


Figure 4-7: Schematic of the triode configuration used to test the ballasted FEAs. A nylon polymer gasket acts as a stand-off between the FEA and the extraction gate.

4.4 Current-Voltage Characterization

Arrays of 1.36 million emitters were fabricated following the process described in Section 4.3 using n-type Si wafers with a nominal donor concentration of $\simeq 10^{15}$ cm^{-3}. The experimental setup is shown in Figure 4-7. A 25 ± 10 μm thick nylon spacer was used to insulate the emitters from an unaligned perforated extraction grid, resulting in a tip-grid distance of 5–25 μm. When electrons are emitted from the sample, a fraction of the electrons pass through the grid and are collected by a suspended ball-shaped anode biased at +1100 V, allowing us to determine whether the source of the current is leakage through the dielectric spacer ocesr electron field emission current. The linear relationship between the current collected at the grid and the suspended anode suggests that the origin was field emission. At higher voltages, this linearity does not hold. It is likely that the polymer spacer is beginning to break down at these voltages, resulting in significant leakage current in addition to the field-emission current.

I-V characterization was conducted in an ultra-high vacuum testing chamber at a pressure of 9×10^{-10} Torr using three commercially available high voltage source measure units (Keithley model 237 SMUs). Figure 4-8 shows the typical I-V characteristics of a 1.36-million tip FEA for electrons collected by both the extraction gate and the anode. The anode efficiency, *i.e.* the transparency of the extraction gate was about 1 %. The Fowler-Nordheim (FN) plot, also shown in Figure 4-8, is a common technique for plotting field emission data. Ideally, there is a

linear relationship between the natural log of the current over the square of the gate voltage and the inverse of the gate voltage [46]. At high extraction gate voltages, if the emission current is limited by the vertical current limiters, the FN plot should deviate from the linear relationship and the slope should become less negative at higher voltages. At a bias voltage of approximately 600 V, the FN characteristic in Figure 4-8 begins to deviate from its linear characteristics.

The tip radius may be estimated empirically from I-V characteristics by extracting the slope of the Fowler-Nordheim curve, b_{FN} and using

$$\beta \approx \frac{0.95 \cdot 6.87 \times 10^7 \cdot \phi^{3/2}}{b_{FN}} \tag{4.2}$$

and

$$r \approx \frac{1}{\beta} \tag{4.3}$$

where $\beta$is the field factor in cm^{-1} ϕ is the work function barrier in eV, assumed to be 4.05 eV for n-type Si, and r is the emitter tip radius in cm. The slope extracted from the F-N gate current characteristic shown in Figure 4-8 was 2942, resulting in a β of 1.80×10^5 cm^{-1}, and an r of 55 nm. This result is not consistent with the experimental measured tip radii shown in Figure 4-5, and will be examined further below.

4.5 Discussion

The current-voltage characterization of the individually ballasted FEAs presented in the preceding section are consistent with the results obtained by Velásquez-Garcá et al. [125] and the characterization of the vertical current limiter pillars without field emission structures reported in Chapter 3. Using the data presented in Table 1 and assuming that the emission current is limited to 10 pA/emitter the expected array current is 13.6 μA. From Figure 4-8, at a gate-to-source bias voltage of 550 V, we observe the transition of the F-N plot from the regime where the current is limited by the transmission of electrons through the barrier to a supply limited regime. The corresponding emission from the FEA is 11.1 μA. This result is consistent with our suggestion that the vertical current limiter controls emission current.

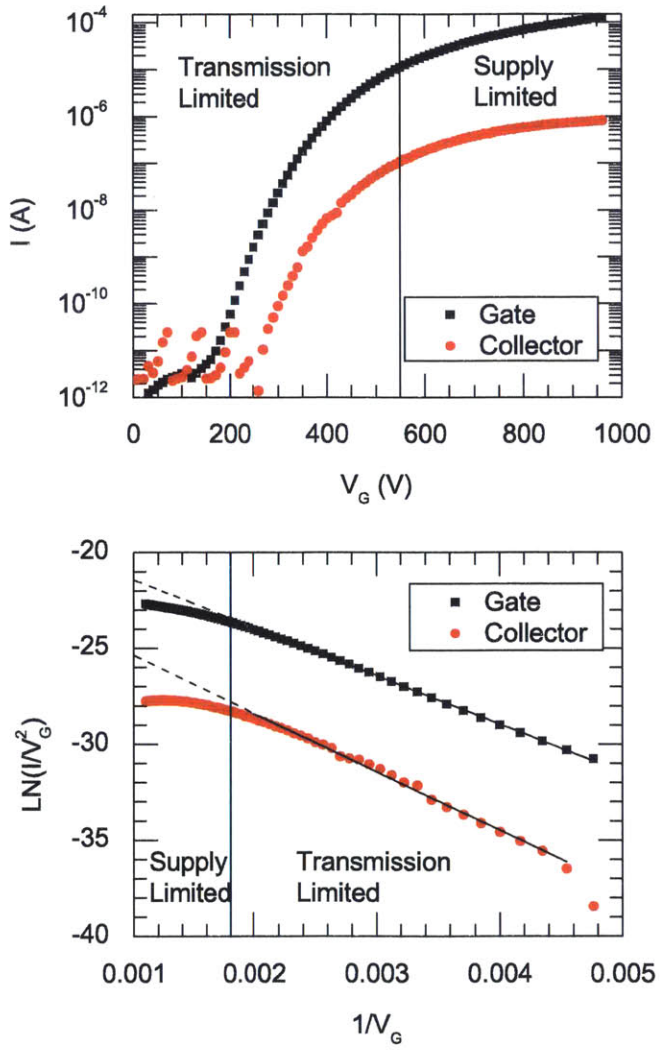


Figure 4-8: (top)I-V Characteristics for an array of 1.36 million individually ballasted field emitters. At gate voltages over 550 V, the FEA enters a regime where the current is limited by the supply of electrons to the field emitters by the vertical current limiter, rather than the transmission through the barrier. (bottom) F-N Plot for an array of 1.36 million individually ballasted field emitters, demonstrating the different regions of operation.

We note that the surface of these current limiters are covered by thin oxides that are not carefully processed and hence may be effected by a higher interface trap density. This increased trap density will have an impact on the saturation current of the current limiters however, based on the experimentally obtained saturation characteristics of the FEAs reported above, we do not believe this had a major impact on the ability to use this structure for the current limitation of field emission arrays.

An explanation for this difference in extracted tip radius is that the models that describe the electrostatics of a microfabricated field emitter with a self-aligned gate that is very close to the tip [123, 37] do not translate well to structures where the gate is perforated and located about 25 microns away with tip-to-tip separation of 5 μm and an aspect ratio of 100, as we have in this case. Screening of the tip electrostatic field by proximal tips has been suggested in the literature, especially when the tip-to-tip distance is far less than the tip-to-gate distance [96]. A 3-D finite element model of the emitter with the gate electrode positioned 12 μm above the emitter tips, shows that the field factor, β is about an order of magnitude lower than predicted by the ball-in-sphere model for an emitter with the same radius. The model accounts for screening by nearest neighbor emitters on the electric field at the apex of the tip. A comparison of the field factors for the ball-in-sphere model and the simulation results are shown in Figure 4-9. Using the field factor measured in the I-V characteristics (1.8×10^5 cm^{-1}), from this model we estimate the tip radius to be $\approx$ 6 nm, agreeing very well with the tip radius statistics measured using SEM (mean = 5.6 nm).

Another possible explanation of this difference could be the presence of a thin native oxide could manifest itself as a lower field factor, which translates into an implied higher workfunction. However, assuming a work function increase from 4.05 eV to 4.5 eV changes the extracted tip radius by less than 20 %. Hence, this is not very likely.

The current saturates at $\simeq$ 10 μA, corresponding to $\simeq$ 7.36 pA/emitter. This number agrees very well with the measured saturation current of individual silicon nanowires presented in Chapter 3, 8.5 pA. Because there is no thermal SiO_2 to passivate the surface of these nanowires, we expect that the density of interface traps to be large, $D_{it} > 10^{11}$ cm^{-2} eV^{-1}. Combinded with the small diameter and the low to moderate doping ($\simeq 10^{15}$ cm^{-3}), it is likely that the Si nanowire are fully depleted. Assuming $n_{eff} \approx n_i = 10^{10}$ cm^{-3} and a diameter of 100 nm, we

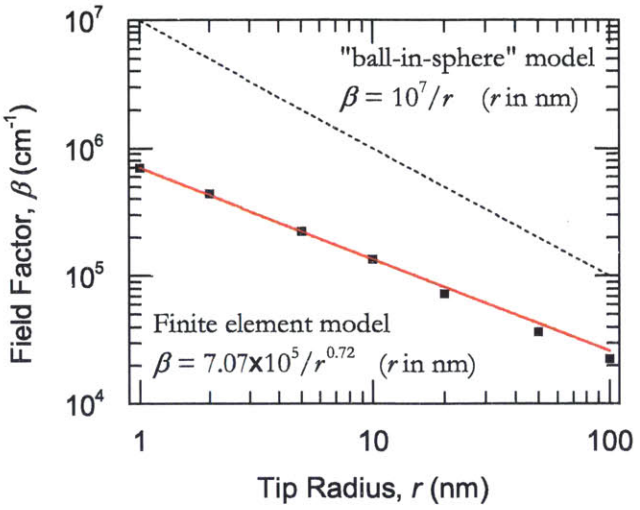


Figure 4-9: 3-D finite element simulation of the ungated emitter structure taking into account screening of the electric field from nearest neighbors. emitter pitch is 5 μm, the gate is 12 μm above the emitters.

find that the saturation current is 1.7 pA/emitter. This discrepancy could be explained by either the pillar diameter being slightly larger than 100 nm, or that the effective carrier concentration is slightly higher.

4.6 Summary

This chapter demonstrated the design, fabrication, and characterization of ungated Si field emitter arrays with Si nanowire current limiters. We verified that the FEAs function as intended, and successfully limited the current, as evidenced by a "bending over" of the F-N plot. The measured saturation current was consistent with the measured I-V characteristics of the nanowire current limiters, and the tip radius statistics measured with SEM were consistent with the tip radius extracted from the Fowler-Nordheim plot of the data, using a finite element model for the field factor, β.

Chapter 5

Gated Silicon Field Emitter Arrays

5.1 Introduction

This chapter presents gated field emitter arrays with silicon nanowire current limiters. First, it explores in detail several key process steps method for forming silicon nanowires and filling the gap between nanowires with a conformal dielectric. This conformal dielectric is required to support an integrated gate with a gate aperture that is self-aligned to the emitter. However, this first structure suffered from several significant drawbacks including large gate leakage. To combat these problems, a new device architecture was developed that addressed the problems and the fundamental problems of FEAs. Through addressing these challenges, the new device design attained breakthrough device performance with regards to current density and device lifetime.

5.2 Numerical Modeling

A simple silicon FEA with vertical nanowire current limiter fabrication process was created and simulated in ATHENA, resulting in the structure shown in Figure 5-1. In this simulation the donor concentration was 2×10^{15} cm^{-3}. To create a sharp tip ($r \approx 2$ nm) on top of the silicon pillar, a short isotropic etch to begin rough tip formation was performed continuing with the deep anisotropic etch to form the pillar. When performing the oxidation, the time was carefully controlled to produce a sharp emitter. After the oxidation, the gaps were filled in with LCPVD

oxide, Si_3N_x, and polysilicon was deposited. To create a self-aligned gate, a polishing step was used to pattern the gate aperture, stopping just before the emitter tip was damaged. Finally, the oxide encasing the emitter was removed with a wet etch step.

The structure created in ATHENA was then imported into DevEdit, software which allows for arbitrary editing of structure files generated by SILVACO tools. The meshing around the tip was made much finer to be able to simulate the high gradient at the emitter surface required to model field emitters. The grid constraints in the rest of the simulation domain were relaxed to keep the number of grid points manageable and allow subsequent device simulation in ATLAS to converge.

ATLAS provides a framework for modeling Fowler-Nordheim tunneling through gate oxides that solves the tunneling current at the semiconductor-dielectric interface directly with the current continuity equations, setting a current boundary condition at the emitter tip surface. This model is typically used by CMOS designers for modeling tunneling into the floating gate in Flash memory. The model uses a version of the Fowler-Nordheim equation to calculate the current density at the tunneling interface:

$$J_{FN} = A_{FN} E^2 \exp\left(-\frac{B_{FN}}{E}\right) \tag{5.1}$$

E is the magnitude of the electric field in the dielectric. By default, A_{FN} and B_{FN} are Fowler-Nordheim coefficients for tunneling through a trapezoidal oxide barrier, but can be easily modified in the code to use appropriate F-N parameters for tunneling into vacuum that include image charge effects i.e. $A_{FN} = 4.752 \times 10^{-5}$ and $B_{FN} = 5.268 \times 10^{8}$.

The simulated I-V Characteristics and F-N plot are shown in Figure 5-2 and summarized in Table 5.1. The emitter reached a current of 1 pA at $\approx$ 28 V, and the onset of saturation is at a current of 1.5 μA @ $V_{GE} \approx 70$ V. From the F-N plot in Figure 5-2, we find that the slope is 600, corresponding to a β of $\approx 8.8 \times 10^5$ and a tip radius of 11 nm using $\beta \approx 1/r$. The effective tip radius for this simulation was limited by the meshing at the apex of the emitter.

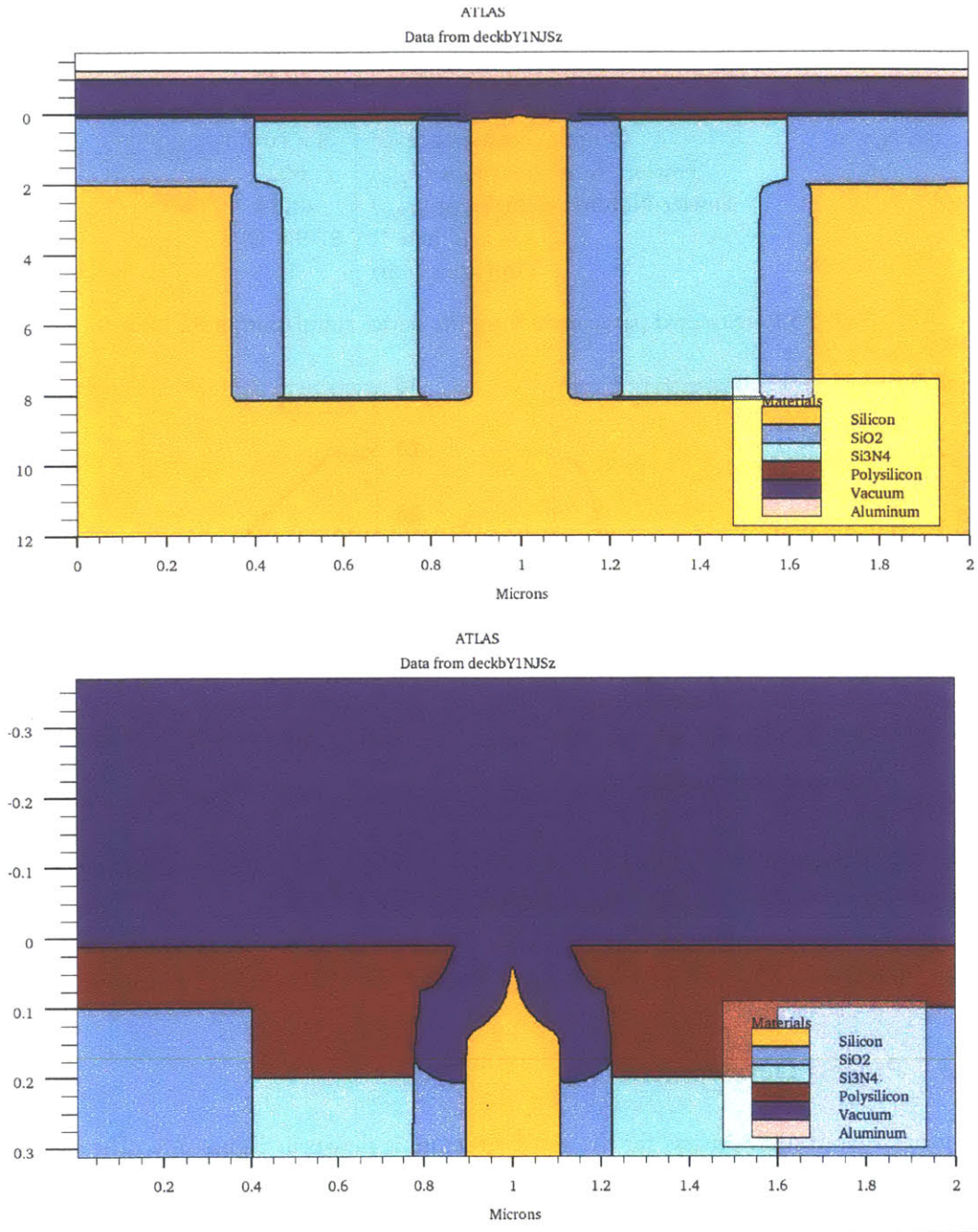


Figure 5-1: The structure of the numerical simulation

Parameter	Value
Doping Density, N_D (cm^{-3})	2×10^{15}
NW Diameter (nm)	200
Turn-on voltage (V)	20 V
Gate-Emitter Saturation Voltage (V)	70 V
Saturation Current (A)	1.5 μA
Output conductance (S)	8×10^{-9}
Fowler-Nordheim Slope (b_{FN})	602
Fowler-Nordheim Intercept (a_{FN})	-11.24
β (cm^{-1})	8.79×10^5
Tip radius (nm)	11

Table 5.1: Extracted parameters from the device simulation in ATLAS

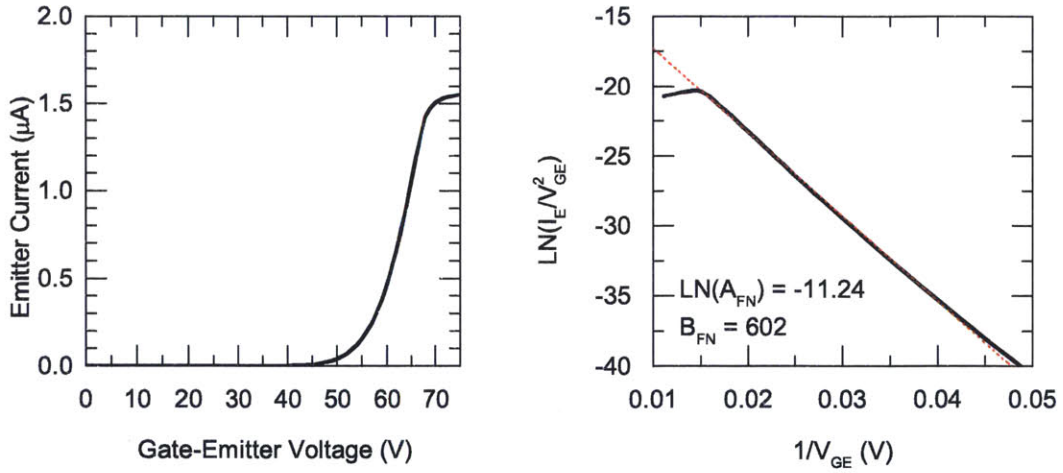


Figure 5-2: Simulated IV and FN Characteristics for a device with a 200-nm diameter, 8 μm tall nanowire current limiter, and doping density $N_D = 2 \times 10^{15}$ cm^{-3}.

5.3 Process Development and Proof-of-Concept Devices

5.3.1 Process Development

The general fabrication process for the gated structure is shown in Figure 5-3. The process begins identically to the ungated device presented in Chapter 4 with patterning an oxide hard mask followed by reactive ion etching to form the emitter tips and deep reactive ion etching to form the silicon nanowire current limiters. The tips are sharpened and the SiNW diameters is reduced to $\sim$ 100 nm with thermal oxidation at 950 °C. After the oxidation, a multistep fill process is used to fill in the gaps between adjacent pillars with SiO_2 and Si_3N_x. The Si_3N_x is

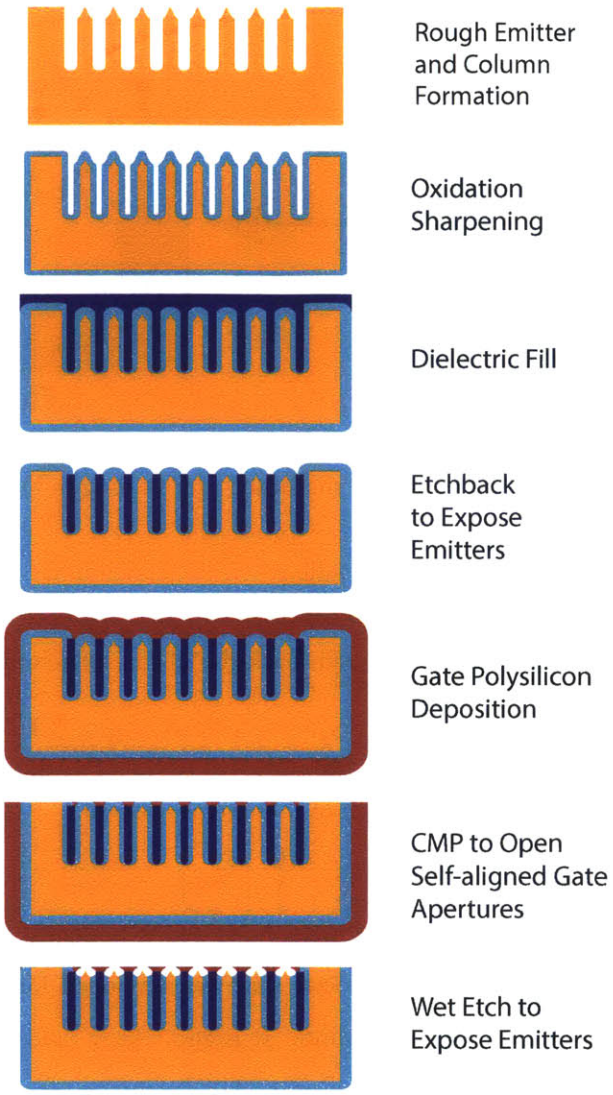


Figure 5-3: Schematic of the process for gated FEAs.

then etched back to expose the oxide domes, which will form the self-aligned gate apertures. An *in situ*-doped poly-Si gate is then deposited, and thinned using CMP to form the gate apertures. Finally, a wet etch in buffered-oxide etchant (7:1 HF:NH_4F) is used to release the emitters.

To successfully build these FEAs, three key processing steps needed to be well-understood and optimized those processing steps were:

1. Deep reactive ion etching to form the Si nanowire current limiter

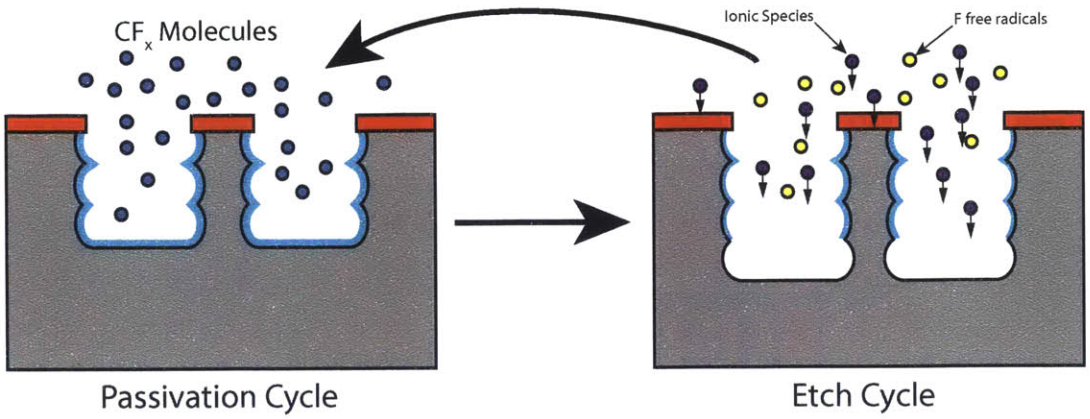


Figure 5-4: Schematic of the Bosch process used in DRIE.

2. Filling in the gaps between adjacent pillars

3. Chemical mechanical polishing to etch back the silicon nitride used to fill in the gaps between pillars.

The following sections will go into each of these steps in detail.

Deep-Reactive Ion Etching

Deep reactive ion etching (DRIE) is a process that was developed for the MEMS industry for the creation of high-aspect-ratio structures. It is also widely used in the semiconductor industry to fabricate deep trenches for capacitors used in dynamic memory (DRAM) [109], and though-silicon vias (TSVs) [35]. DRIE uses the Bosch process to achieve extremely anisotropic features and vertical sidewalls. The Bosch process is a time-multiplexed process where the etcher switches an inductively coupled plasma (ICP) between two modes to achieve vertical sidewalls:

1. An isotropic SF_6 plasma etching step in which ions are directed vertically towards the substrate, and free fluorine excited radicals react with the silicon on the surface to form volatile SiF_2 which is then removed

2. A passivation step, in which C_4F_8 which decomposes to CF_x reacts with the exposed silicon surface to form a polymer substance similar to Teflon.

Etch Parameter	Value
Bosch Process Gasses	SF6 and C4F8
Pressure (mTorr)	24
Etch Cycle Time (s)	5 (start on etch cycle)
Passivation Cycle Time (s)	**5.8-7.5**
SF6 Flow Rate (sccm)	**80-110**
C4F8 Flow Rate (sccm)	45
Etch/passivation Power (W)	800/600 W
Platen Power during Etch/Passivation (W)	120/60

Table 5.2: Etch Parameters

The passivation layer protects the sidewalls from further etching, but the polymer at the bottom of the feature being etched is sputtered away by energetic, directional ions. The process is shown schematically in Figure 5-4.

A challenge of using DRIE for high-aspect-ratio structures is that the etch profile is geometry dependent, and very sensitive to processing conditions. Hence, for challenging (i.e. high-aspect-ratio, high density structures) careful process development and optimization are absolutely critical to attain uniform and repeatable results. If a non-optimized process is used, small changes in the starting mask or processing conditions can result in poor etches with problems such as significant undercut, mask erosion, or black silicon formation. Examples of problems that resulted from non-optimized DRIE processes are shown in Figure 5-5.

To optimize the DRIE etch in order to improve the profile of the silicon nanowire current limiters, we conducted a 2-parameter design of experiments. A series of initial experiments to explore the parameter space and determine which parameters had the biggest impact on the etch were conducted. The parameters that were explored include RF power, platen power, pressure, and gas flow rates. After the exploration phase, the SF_6 flow rate and the ratio of etching time to passivation time were found to have the largest effect on on etch selectivity. Here, we define etch selectivity as the ratio of the vertical etch rate to the lateral etch rate. The parameters for the etch are summarized below in Table 5.2.

The SF_6 flow rate and passivation time were varied using a circumscribed central composite experimental design, which is a box circumscribed by "star points" and a center point that is measured multiple times to demonstrate repeatability and lend confidence to the values mea-

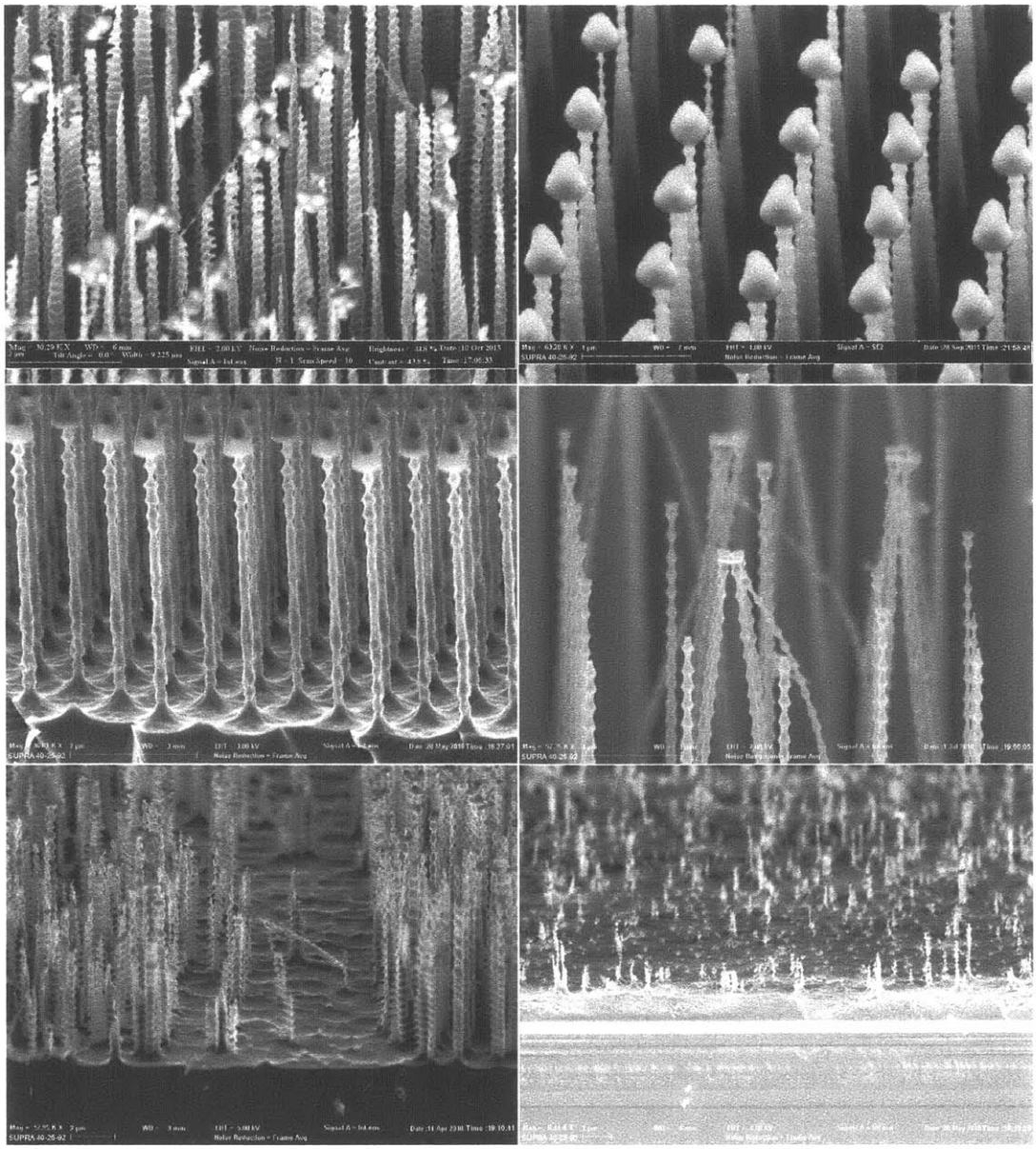


Figure 5-5: Some of the challenges of DRIE.

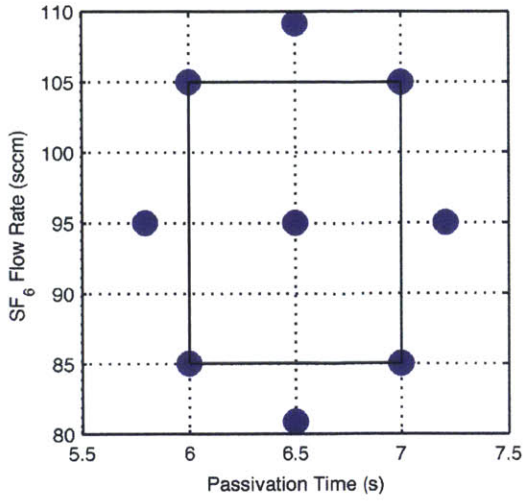


Figure 5-6: Exploration space for the design of experiments

Run	Passivation Time (s)	SF6 Flow (sccm)
1	7.2	95
2	6.5	95
3	6.5	81
4	6	105
5	6.5	109
6	6.5	95
7	5.8	95
8	6.5	95
9	7	105
10	7	85
11	6.5	95
12	6.5	95
13	6.5	95
14	6	85

Table 5.3: Summary of etching conditions used in the circumscribed central composite design of experiments

sured. The experimental design space is shown in Figure 5-6 and Table 5.3. A consequence of using a central composite design of experiments is that the response surface modeling is limited to linear and quadratic terms, and cannot model higher order interactions between the variables. To model these higher order terms, a full factorial design, with many more data points would need to be implemented. These interactions can be safely neglected for our purposes.

From the experiments, a response surface was fitted to the data in MATLAB using RSTOOL, an interactive response surface modeling tool included in the statistics and machine learning toolbox of MATLAB. This tool allows for the mapping of linear, quadratic and higher order response surfaces to an experimental design. In this case, a quadratic model with no interactions was used. The results are summarized in Figure 5-7.

In general, both the lateral etch rate and the vertical etch rate increase with increasing SF6 flow rate and decreasing passivation time. This makes intuitive sense. With a shorter passivation time, a higher porportion of the total time is spent etching, thus the etch rate is expected to be higher. In addition, a shorter passivation time implies that there will be less passivation polymer to etch through, and thus the etch rate will be faster.

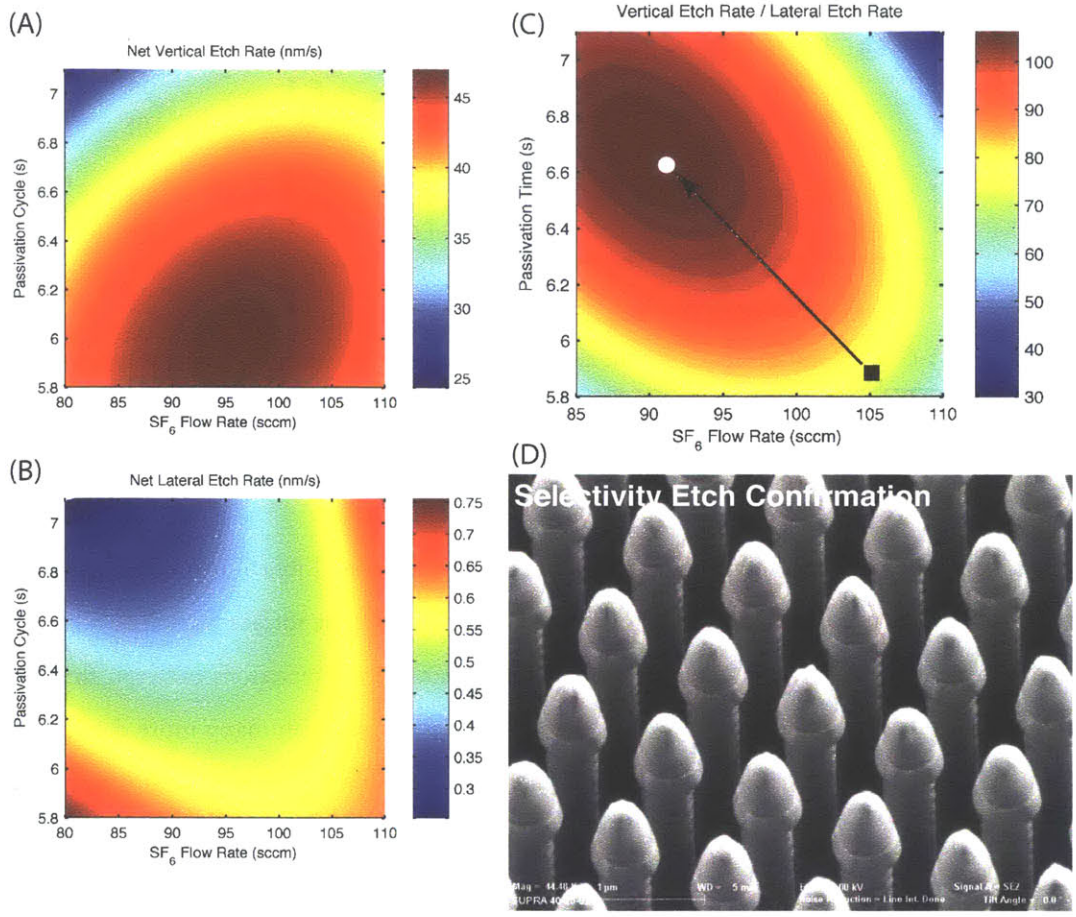


Figure 5-7: (A) the response of vertical etch rate to SF6 flow rate and Passivation cycle time (B) response of lateral etch rate to the same (C) Selectivity demonstrating the shift from the original etch [denoted by black square] to the optimized etch [denoted by white circle] (D) Confirmation of etch selectivity.

A higher SF_6 flow rate means that the residual C_4F_8 will be flushed from the chamber faster, and there will be a higher concentration of SF_6 in the chamber. In addition, reacted products will have a shorter dwell time in the chamber because while the pressure remains constant, the flow into the vacuum chamber increases, which implies that the flow out of the vacuum chamber must increase by the same amount.

Because the lateral etch rate and the vertical etch rate do not have the same dependence on these parameters, a local selectivity maximum occurs at a flow rate of $\approx$ 90 sccm and a passivation time of 6.6 s.

5.3.2 Dielectric Fill Process

Developing a process to fill in the gaps between the SiNWs was a significant fabrication and materials challenge. A variety of different techniques were employed before a feasible combination of techniques was developed.

The first attempts to fill in the gaps used a liquid spin-on-glass (SOG). SOG is hydrogen silsesquioxane (HSQ) or methylsiloxane-based material where the wafers are spun-coated with SOG, and then cured at $\approx$ 450°C. During the curing process, solvent is removed from the film and the liquid becomes a glass. SOG is commonly used as an inter-level dielectric and to planarize topology, however, even low-shrinkage SOG materials were found to result in cracking in our structure.

Low temperature oxide (LTO) deposition was also used to fill the gaps. LTO deposition is an LPCVD reaction using SiH_4 and O_2 at $\approx$ 425°C. After deposition, the oxide needs to be densified at a higher temperature (> 800°C to remove hydrogen from the film and to improve the dielectric qualities of the oxide. LTO deposition has several drawbacks that makes the process unsuitable for this application. The low-temperature of the deposition causes the deposition to be not very conformal, forming large"keyhole voids" where the top of the gaps close before the bottom of the gap is filled. In addtion, the high temperature densification causes the oxide film to shrink 1 – 2 % and cracking results.

Undoped poly-Si deposition and oxidation was tried to fill the gaps between SiNWs. We found when using only poly-Si deposition and oxidation, the deposition was unable to be controlled enough. It was impossible to attain simultaneously filled gaps and complete poly-Si

consumption during the oxidation process.

After this series of experiments, a process consisting of Si oxidation, poly-Si deposition, poly-Si oxidation, and Si_3N_x deposition was developed to create a conformal dielectric fill. The multi-stop process is shown in Figure 5-8.

This stack consists of silicon dioxide and silicon nitride formed through a combination of deposition of undoped poly-silicon films, oxidation of the poly-silicon films, and silicon nitride deposition. The undoped poly-silicon is deposited at 625 °C using low-pressure chemical vapor deposition (LPCVD). At this temperature, the polysilicon shows columnar growth and large grains [73] . In addition, due to the elevated temperature at which the deposition takes place, the deposition is reaction-rate limited [72] and the poly-silicon has high surface diffusion [72], allowing for conformal deposition into the deep voids between nanowires. The thickness of this deposition is controlled so that after subsequent oxidation, a gap of < 50 nm remains between adjacent nanowires, and preventing the oxidation fronts from meeting. If the oxidation fronts do meet, they form keyhole voids or leave unoxidized polysilicon.

The remaining void is filled by 1-μm of low-stress, silicon-rich silicon nitride deposited in a vertical tube reactor via LPCVD at 800 °C. The deposition reaction to form SiNx is also rate-limited and has high surface diffusion so that the nitride fills in the remaining gaps between pillars. Subsequent cross-section shows that this process creates a reproducible, consistently

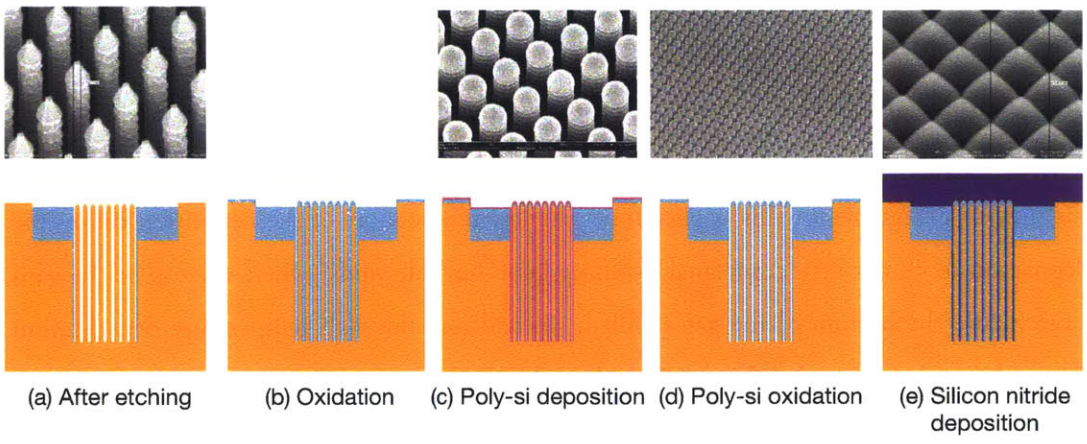


Figure 5-8: Process for filling in the voids between adjacent silicon nanowires with a dielectric matrix.

void-free dielectric matrix that completely surrounds the nanowires. A cross-section of the void free fill after planarization is shown in Figure 5-9.

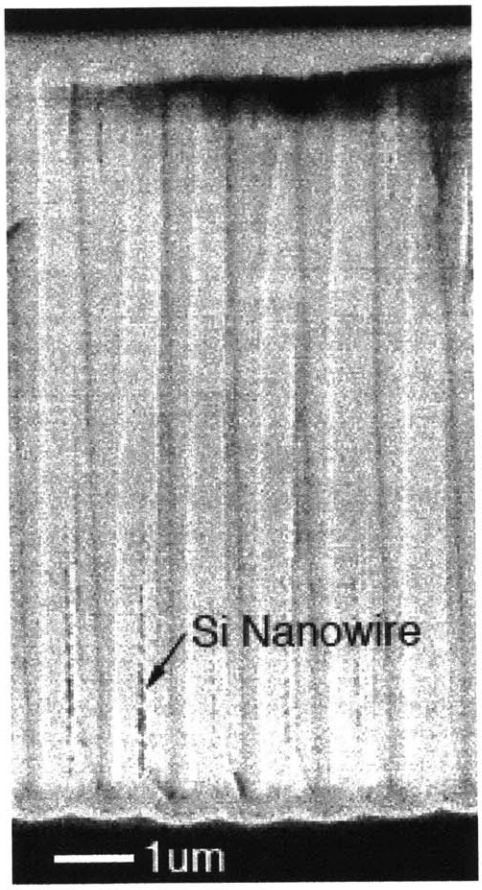


Figure 5-9: Void-free dielectric matrix with vertical silicon nanowires embedded in them after CMP planarization.

Chemical-Mechanical Polishing (CMP)

?? Chemical mechanical polishing (CMP) is a process technology for creating smooth surfaces on semiconductor wafers though a combination of abrasive polishing and wet chemical etching. A typical CMP tool, such as the one shown schematically in Figure 5-10 uses a large, pliable polishing pad attached to a solid metal platen. The wafer is attached to a chuck, held in place with a retaining ring and vacuum, and is placed in intimate contact with the pad. The pad deforms to conform to the wafer surface, to account for wafer bow and long-range "waviness."

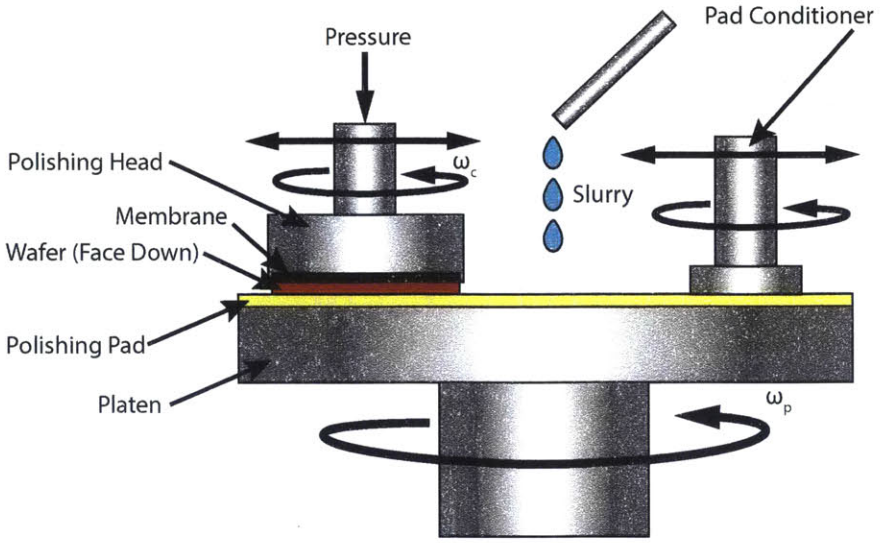


Figure 5-10: Schematic of a CMP process

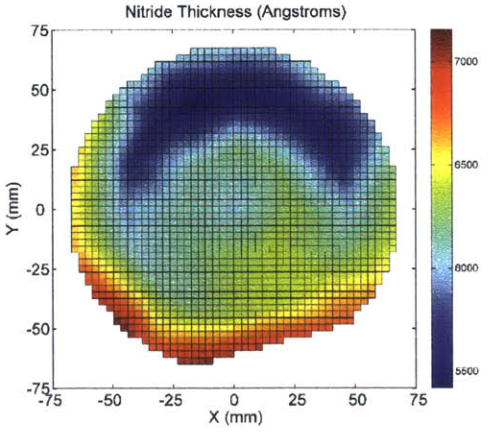
A slurry, in this case a colloidal suspension of fine silica particles (mean size $\approx 0.1 - 0.2$ μm [83]) in deionized (DI) water and potassium hydroxide (KOH) is used. The silica particles are the abrasive, and the KOH enhances the polishing rate by causing silica dissolution [33]. The solution is alkaline, with a pH ≈ 10.

Chemical mechanical polishing is widely used by the semiconductor industry. Originally, the process was only used in back end-of-line (BEOL) processing for the planarization of metal layers and inter-level dielectrics (ILDs) [75], and the damascene process for Cu interconnects [128]. Now, CMP is widely used in shallow-trench isolation (STI) [94] and to pattern metal gates for transistors in advanced technology nodes.[63].

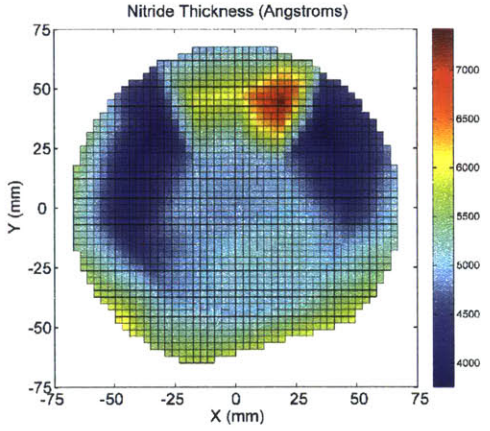
CMP is an important processing step for building field emitter arrays with self-aligned gates as explained in Chapter 2. The preferred method of forming self aligned gates in Si FEAs is to use an oxide deposition to define the aperture of the device, deposit the gate material, and then polish the structure, timing the polishing step so that it removes the gate material to expose the oxide that embeds the emitter tip but before the tip is exposed. This process takes advantage of the fact that "bumps" polish faster than planar surfaces, however if the polishing step goes too long, the tip may be damaged, resulting in blunt tips.

The process for fabricating self-aligned gated FEAs with vertical Si nanowire current limiters

1600 s



2400 s



3400 s

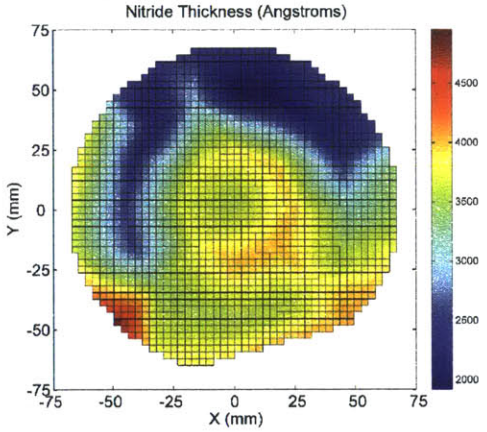


Figure 5-11: Wafer thickness maps for three different times to extract the etch rate and uniformity of the polishing. 49 points across the wafer were measured using spectroreflectometry.

utilizes two CMP steps (three with the inclusion of the mesa structure). Polishing the silicon nitride is critical to both planarize the film and to thin it so that the nitride/oxide interface is within $\approx$ 200 nm of the surface. This step is required to achieve uniformity during the wet etchback to expose the oxide domes. A thick nitride is required to fill in the gaps, however, when wet etching thick films spatial non-unformities become worse. Silicon nitride is a very hard material (hardness $\sim$ 30500 MPa) and etches extremely slow or not at all in most chemical etchants. This section will only go into depth into the process of CMP of silicon nitride. The CMP of polysilicon for the gate apertures is also an important step that was well characterized.

To characterize the polishing rate of the silicon nitride, a number of bare silicon wafers were coated with nominally 1-μm of low-stress silicon-rich silicon nitride deposited using a low-pressure chemical vapor deposition (LPCVD) in a vertical tube reactor. These wafers were then polished for different times, and then 49 measurements of the film thickness across the wafer were taken using spectroreflectometry (DBS) using a UV1280 spectrophotometer/ellipsometer. DBS uses a spectroreflectometer that exposes a wafer to light (220-830 nm) and determines the film thickness or refractive index based on the reflected spectrum (reflected intensity as a function of wavelength) and a known standard (a clean bare silicon wafer) [1]. The wafer maps for several different polishing times are shown in Figure 5-11.

From the wafer maps of the film thickness, the thickness of the nitride has a clear spatial dependence, with the nitride on the outside edge of the wafer etching faster than the center of the wafer. This distribution can be explained by the fact that the wafer is spinning, and hence the edge of the wafer is moving faster across the surface of the pad than the center of the wafer. This non-uniformity is mitigated somewhat by the fact that the platen and the wafer chuck co-rotate and the wafer chuck oscillates back and forth on the platen, however it cannot be eliminated.

From the slope of the plot of film thickness vs. polishing time, we can extract the polishing rate of silicon nitride. The etch rate of the nitride is linear, as shown in Figure 5-12 and $\approx$ 24 nm/min. Compared to the etch rate of SiN_x in 165 °C Phosphoric acid – the typical method of etching silicon nitride films – 4 nm/min.

The plot of nitride thickness was created over multiple days starting with a bare silicon wafer coated with 1 μm of nitride each time, so the CMP tool is exhibiting very good uniformity and

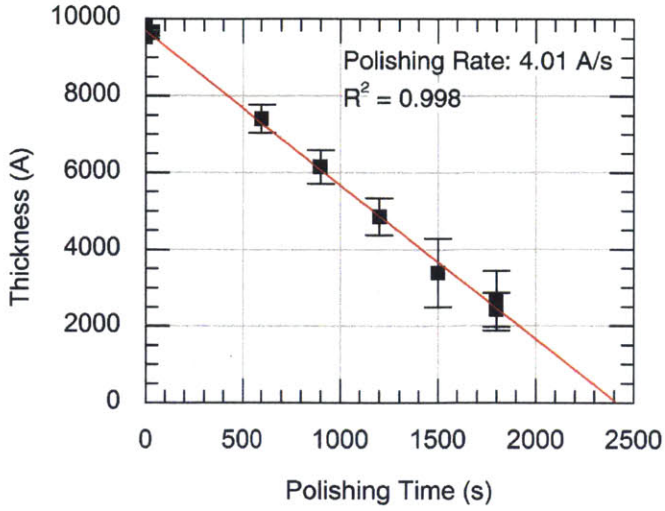


Figure 5-12: Extraction of nitride polishing rate from thickness measurements. The error bars show the standard deviation of the measurments made on a single wafer, showing the spatial variation in film thickness.

stability over the short term. The time point at 1800 s was repeated over 2 different days with good agreement to verify polishing stability. Over long periods of time, however, the polishing rate has drifted by as much as a factor of 5, so care must be taken to measure the actual polishing rate prior to processing important device wafers.

Using these results, we then polished wafers with silicon field emitter tips on top of nanowire current limiters. Due to the topology of the nitride film, the polishing rate was faster initially, but then slowed once a planar surface was formed. Figure 5-13 shows the emitter tips buried in SiO_2 and SiN_x, and Figure 5-14 shows the resulting oxide domes after the etchback in hot phosphoric acid.

5.3.3 I-V Characterization

Figure 5-15 shows the testing setup used to characterize these devices. Due to the lack of probe pads, contact needed to be made directly to the gate over the active area of the field emitter array. Two different methods of making contact were used, a sharp tungsten probe and a stainless steel ball electrode. The tungsten probe would short the emitter to the gate, either because it would punch through the thin polysilicon to the gates, or it would make

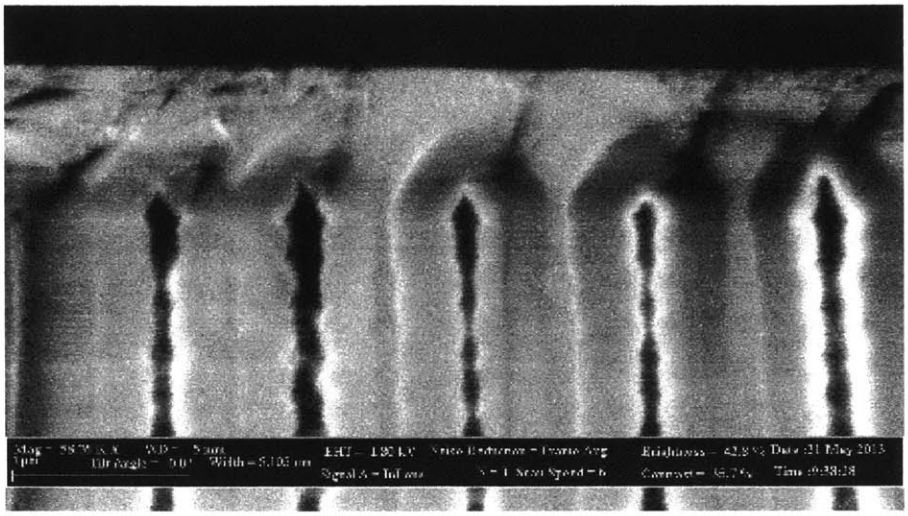


Figure 5-13: Cross-section SEM of a device after nitride polishing. There is about 200 nm of nitride remaining on top of the oxide bumps.

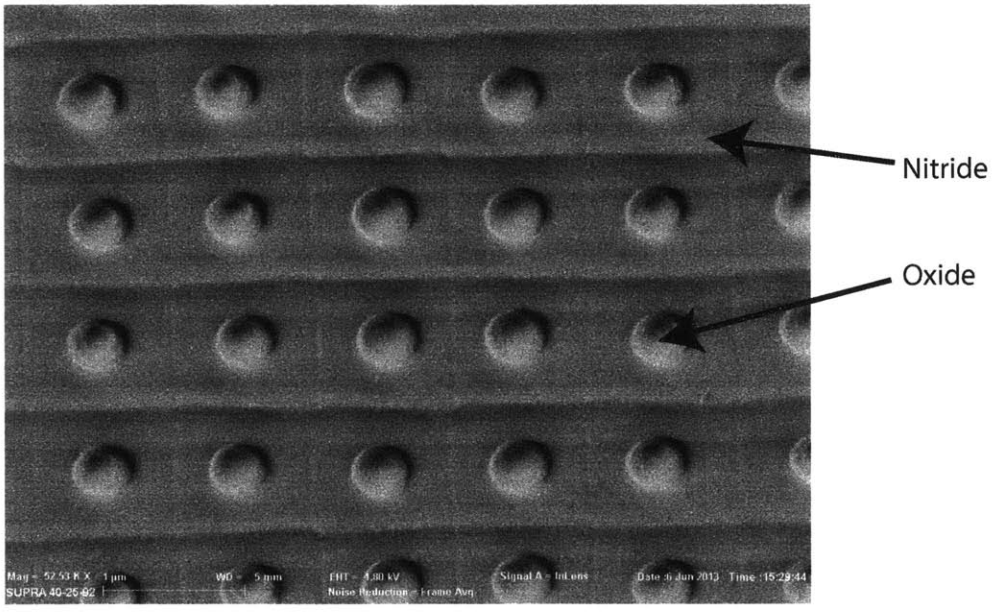


Figure 5-14: SEM image of the oxide domes after nitride etchback in 160 C phosphoric acid.

contact to the emitter tip by lodging itself into gate apertures. Thus, the ball electrode was the better method of making contact to the gate. While the large surface area of the ball prevented shorting between the gate and the emitter tips, a sizable percentage of the array was occluded by the ball and the ball deformed the electric field over the FEA, resulting in a high fraction of the current being intercepted by the ball itself. The I-V characteristics and Fowler-Nordheim plot of a representative device are shown in Figure 5-16.

The field emitter array turns-on at a gate-emitter voltage of 20 V, and exhibits a Fowler-Nordheim slope of < 300. If we approximate the field factor as $\beta \approx 1/r$, this implies that the tip radius is 5.2 nm. However, this approach typically overestimates the tip radius of sharp emitters (see Section 5.4.4), so the average tip radius is likely sharper than 5 nm.

At gate-emitter voltages of 35 V, the Folwer-Nordheim characteristic deviates from its linear regime, suggesting that the nanowire current limiters are controlling the supply of electrons to the emitter surface. The array consists of 10^6 emitters, and the emitter current, $I_E = I_G + I_A \approx 1\ \mu$A, implying a current/tip of approximately 1pA, consistent with earlier results for the saturation current of 100-nm diameter silicon nanowires and the ungated devices.

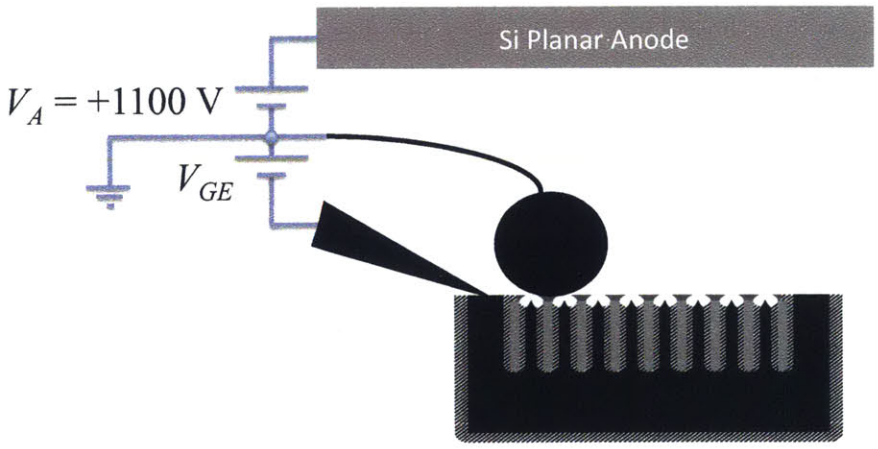


Figure 5-15: Testing setup of the devices

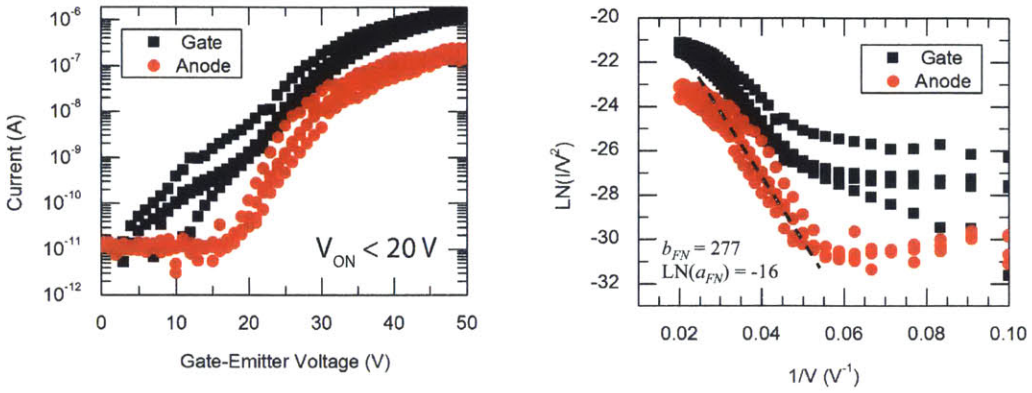


Figure 5-16: I-V characteristics and Fowler-Nordheim plot of the proof of concept gated field emitter array. The device turns on at 20 V demonstrates current saturation at approximately 35 V.

5.4 High Performance Silicon Field Emitter Arrays

5.4.1 Design

The devices presented in the previous section demonstrated a method to fabricate silicon field emitter arrays with silicon nanowire current limiters and self-aligned gate apertures. However, the high gate leakage current of these devices means that they are far from optimized. To prevent the high gate current, a better method of isolating the gate from the substrate needed to be developed to prevent leakage. Furthermore, this isolation needs to be able to withstand a high voltage without breakdown. High quality SiO_2 has a dielectric strength (the electric field at which breakdown of the dielectric material occurs) of approximately 10 MV/cm, however, when the dielectric is biased near its dielectric strength over time, charge injection into the dielectric can cause failure. This type of dielectric failure is called time-dependent dielectric failure (TDDB) [87]. In order to prevent TDDB and ensure long lifetime of the dielectric, the dielectric must be de-rated, and the electric field must be limited to a fraction of its dielectric strength. Usually, limiting the field applied to about 1/10 of the dielectric strength. Thus to support $\approx$ 200 V on the gate, the dielectric spacer between the gate and the substrate needs to be at least 2 μm.

Based on previous results, and in order to attain high current per tip, the Si nanowire must

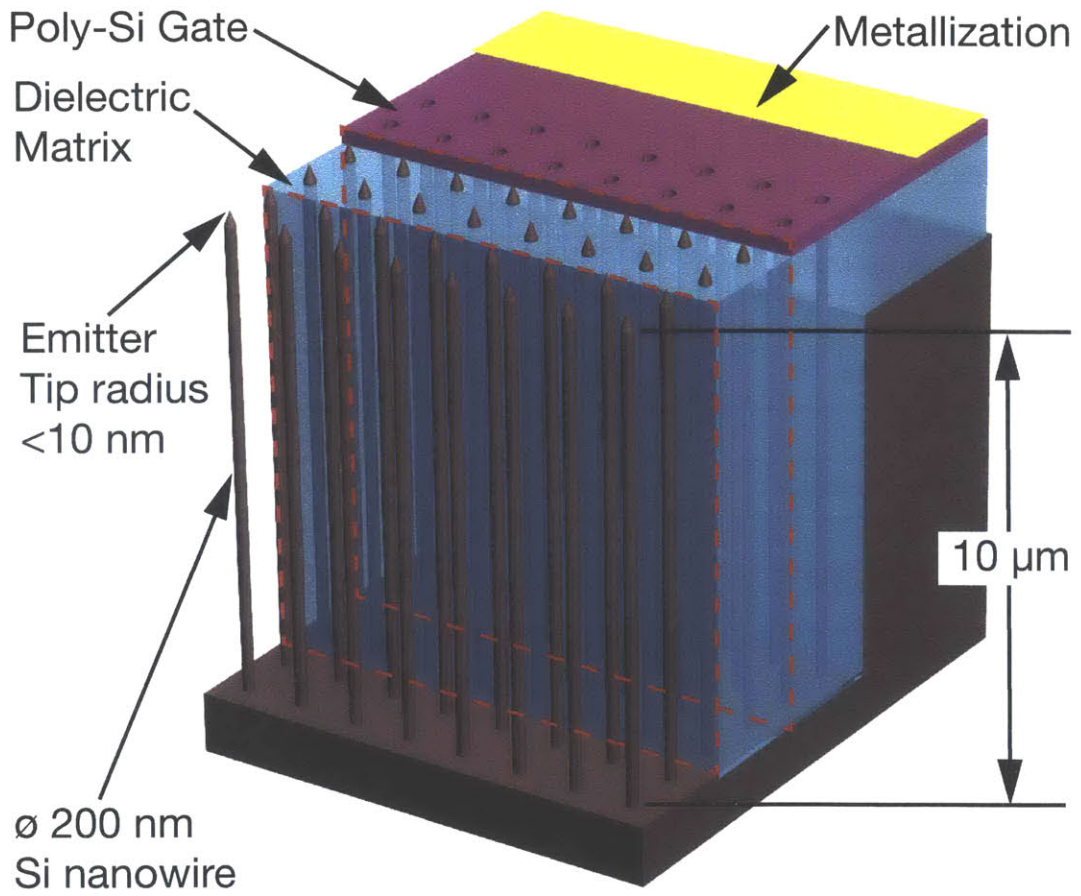


Figure 5-17: A 3-D rendering of the proposed device structure.

not be fully depleted. This implies that the nanowire must have a larger diameter, high quality dielectric passivation, and higher doping than the field emission devices previously discussed. We chose to increase the diameter to 200 nm, and use <100> 150 mm n-type phosphorus doped wafers with resistivity ≈ 3 Ω·cm (Doping density $N_D = 2 \times 10^{15}$ cm^{-3}). A 3-D rendering of the proposed device structure is shown in Figure 5-17.

Assuming that the pillar diameter and doping are high enough that surface states and perimeter effects can be neglected, our simple analytical model predicts that the maximum current/pillar to be limited to $I \approx qA_{eff}N_D v_{e,sat} = 4$ μA/tip.

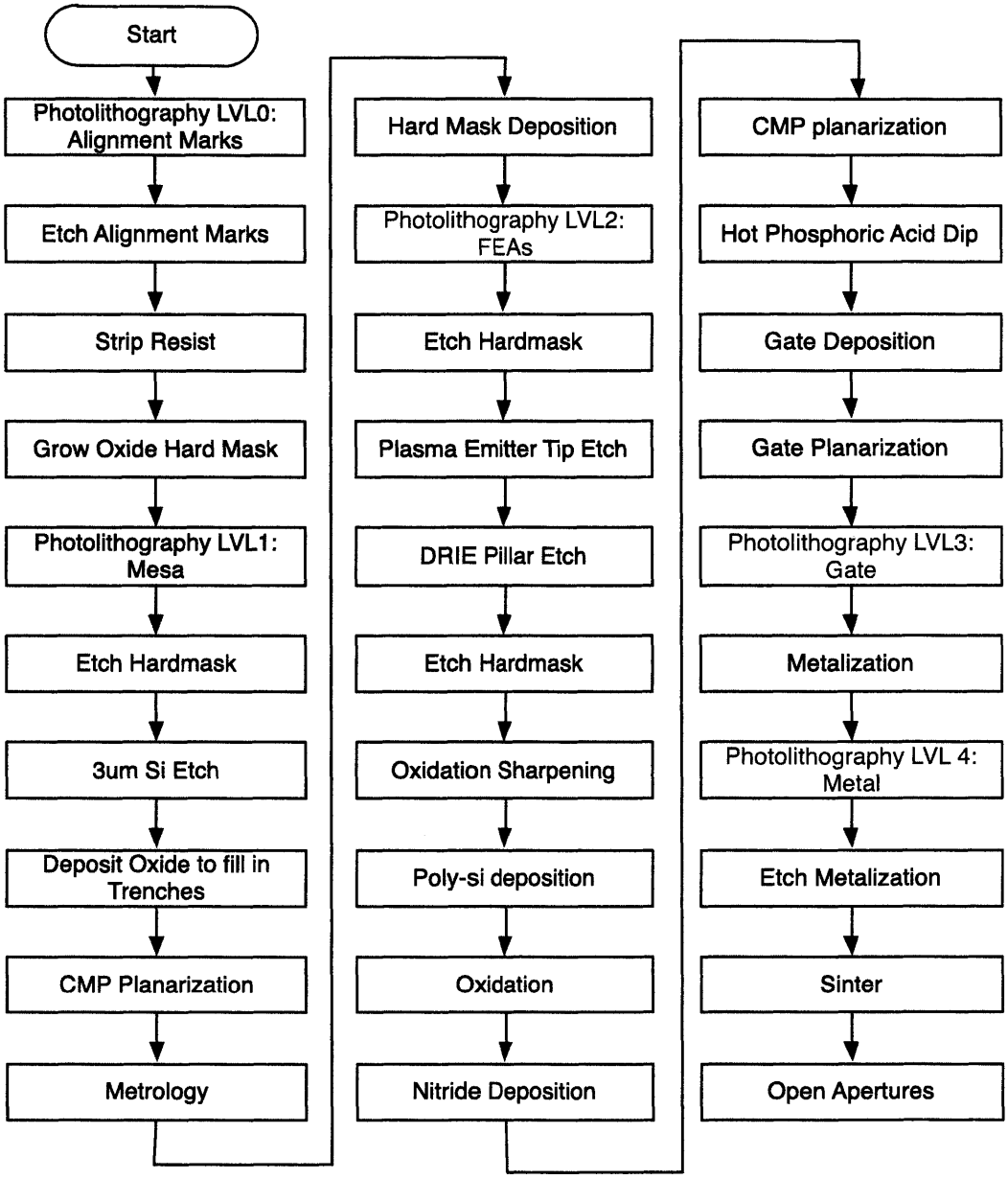


Figure 5-18: The full process for FEAs with integrated SiNW Current Limiters and self-aligned gates.

5.4.2 Fabrication

Arrays sizes ranged from a single emitter to 1000×1000 emitters. Each array has 1-μm emitter-to-emitter spacing. The emitters have tip radius < 10 nm and are on top of a silicon nanowire

that is < 200 nm in diameter and 8 microns tall. A doped polysilicon gate electrode with 350nm diameter surrounds the emitter for applying the electric field to the field emitter tip. Figure 5-18 shows an outline of the fabrication steps.

First, a mesa region on which the array of silicon nanowires capped with field emitter tips will be later be fabricated is defined (Figure 5-19) by etching trenches around the array region. The trench is at least 200 μm-wide and ~ 2 μm-deep.

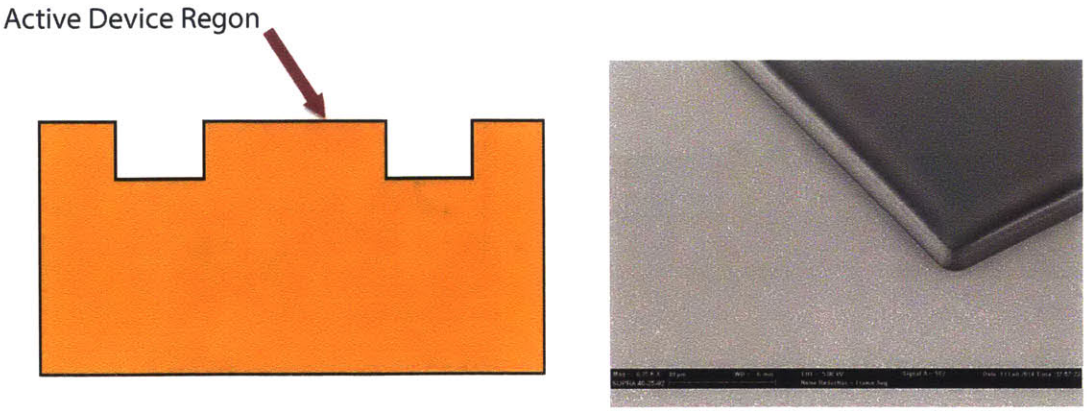


Figure 5-19: Etching the mesa that will form the active device region.

5-μm of plasma enhanced chemical vapor deposited (PECVD) oxide is deposited on both the front and the back of the wafer to fill in the trenches that were formed with dielectric. In order to manage stress and prevent bowing, the deposition was carried out in two steps, with an anneal step in between. Between depositions and after the second deposition, the wafers were annealed at 900 °C in O_2 ambient. Chemical Mechanical Polishing (CMP) is then used to planarize the top surface and expose the bare silicon in the mesa region (Figure 5-20).

A corresponding amount of the oxide film on the backside of the wafer was removed to balance the stress in the oxide films and remove the wafer bow that was resulted after CMP. After planarization, approximately 2-μm of SiO_2 remains only in the trenches around the active regions, and it isolates the gate electrode pad from the substrate and prevents dielectric breakdown of the oxide in the vertical direction from occurring during normal device operation.

Next, 50 nm of thermal oxide is grown followed by the deposition of 250-nm of SiO_2 by PECVD. The oxide layers are an etch mask for patterning the emitters. The patterning and

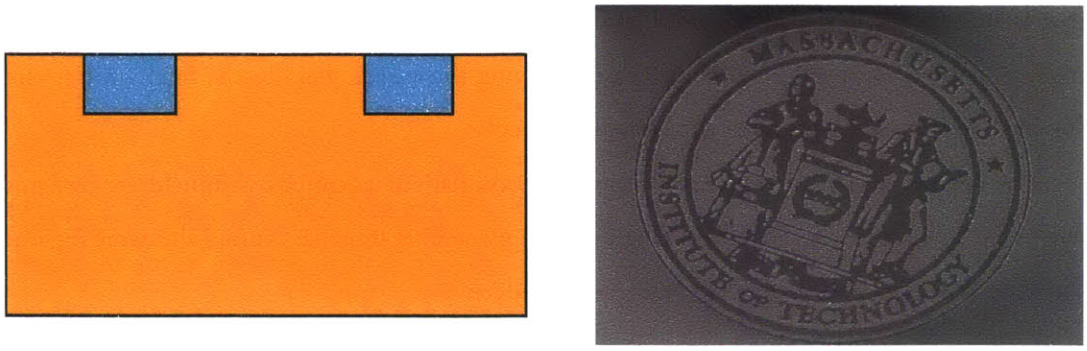


Figure 5-20: filling the trenches surrounding the active device region and planarization.

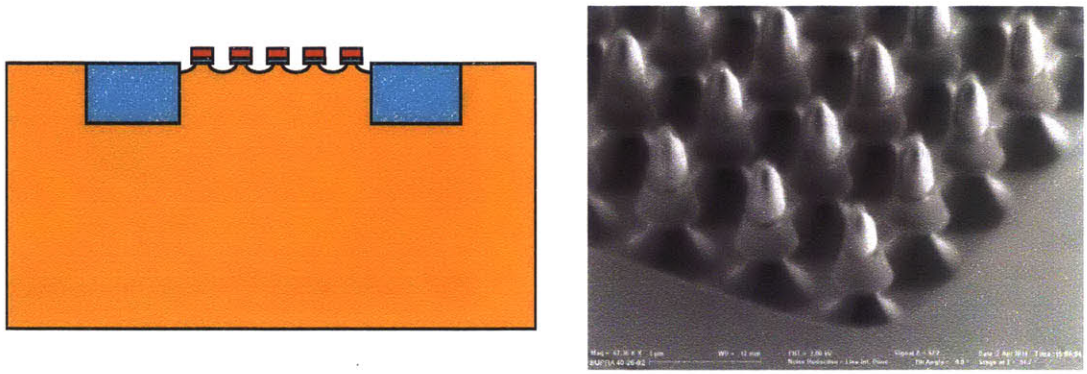


Figure 5-21: Rough emitter tip etch.

etching process to form the nanoscale-sharp silicon tip and the silicon nanowire current limiter begins with an i-line stepper photolithography using a positive photoresist (Shipley SPR-700) to form 1-μm pitch arrays of 0.5 μm photoresist dots. It is critical that the array patterns be well-aligned (misalignment < 50nm) to the mesa regions. The oxide hard mask is patterned by a CF_4/CHF_3/Ar reactive ion etch. After this etch, the tip has a diameter of about 200 nm. An SF_6 plasma is used to etch the silicon isotropically. The result of this etch, shown in Figure 5-21, forms what will become the field emitter tips.

Deep reactive ion etching (DRIE) is used to form the high-aspect-ratio silicon pillars. The pillars after the DRIE step with the SiO_2 hard mask removed are shown in Figure 5-22. The DRIE etch uses the optimized etch parameters as developed in the previous section.

At this point, the pillars have a diameter of 400 nm, and are 10 microns tall. The diameter is somewhat less than the diameter of the hardmask used due to undercutting of the oxide during

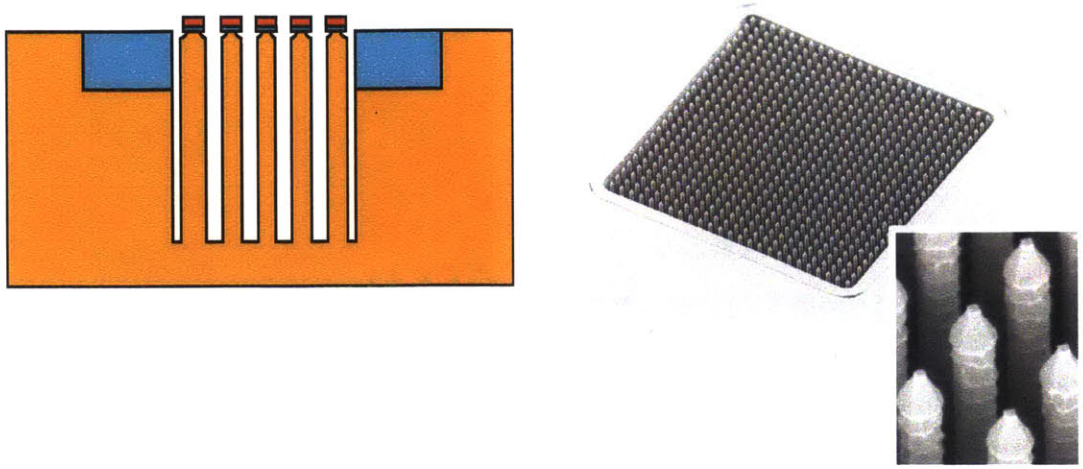


Figure 5-22: Silicon nanowire etch

the DRIE step because the etch is not perfectly anisotropic.

The remaining photoresist and the hard mask are stripped in an O_2 plasma and 7:1 BHF, respectively. To reduce the dimensions of both the pillar and the tip to their final dimensions, the wafer underwent wet oxidation at 950 °C. 950 °C is the temperature above which viscoelastic flow of silicon dioxide occurs, which would deform the shape of the silicon dioxide and potentially result in blunt silicon tips. [61, 86, 60, 39].

A 2-D finite element semiconductor process simulator (Silvaco ATHENA) was used to design the etching and oxidation steps to ensure that the emitter tip would be nano-scale sharp and that the silicon nanowire would be < 200 nm diameter after this oxidation [55, 54]. The silicon nanowire has a diameter of ≈ 200 nm and the column height is ≈ 10 μm. The silicon tip is formed by oxidation sharpening resulting in a tip radius of $\approx 6 - 8$ nm [55].

The deposition of the dielectric stack is, described in detail in Section 5.3.2, resulting in completely filled gaps between Si nanowires as shown in Figure 5-23. A self-aligned polysilicon gate is then defined. To define the gate aperture, first a timed polishing of the nitride is performed using CMP to bring the surface of the nitride to within approximately 100 nm of the top of the oxide domes.

The oxide domes are exposed as shown in Fig. 5-24 through a timed wet etch using phosphoric acid at 160 °C (etch rate $\sim$ 40 Å/min). Phosphoric acid etches silicon nitride with a

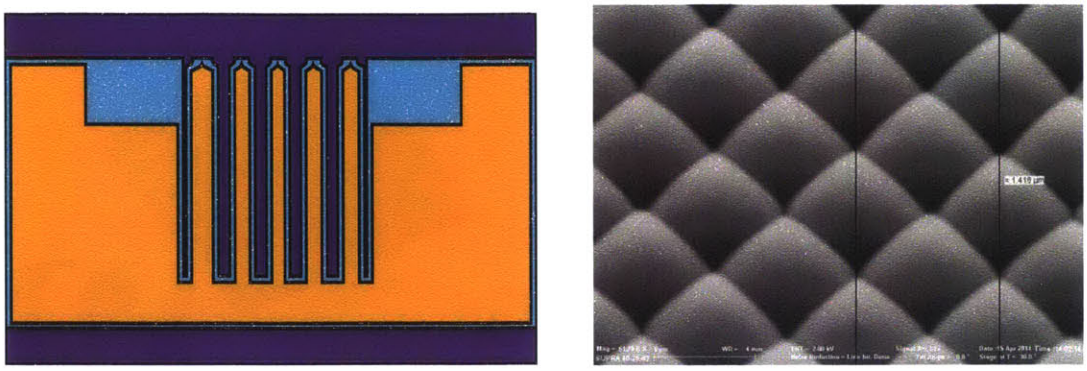


Figure 5-23: Void-free dielectric matrix with vertical silicon nanowires embedded in them.

selectivity of $\sim 20:1$ relative to silicon dioxide. The oxide domes will assist in the formation of the gate apertures by allowing the gate material deposited on the remaining nitride to survive, CMP, but the material deposited on the domes to be removed.

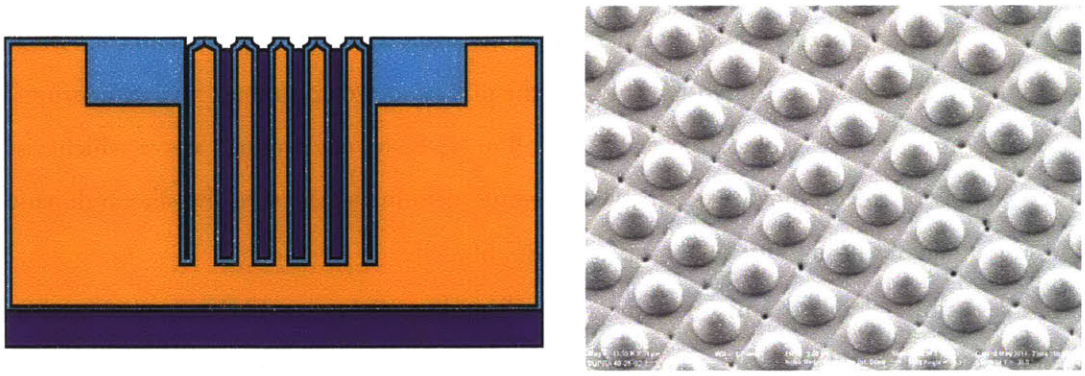


Figure 5-24: Oxide domes that form the gate aperture.

800 nm of poly-silicon gate electrode material that is in situ doped with phosphorus is next deposited as shown in Figure 5-25. A thickness of at least 3× the height of the oxide dome, so that there is full coverage of the gaps between the domes, and that the surface topology is smooth. After polishing, the dopants are activated using rapid thermal annealing (RTA) at 950 C for 30 s.

A third CMP step planarizes the gate, and is timed to stop within 50nm of the emitter tip. The grown and deposited oxide around the emitter tip defines the gate aperture, and the depth of the silicon nitride wet etch determines the gate thickness. Similar to the character-

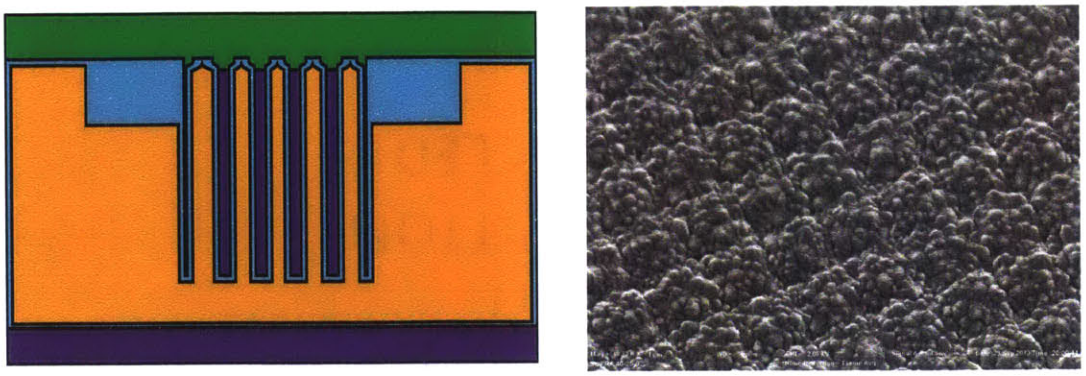


Figure 5-25: Cartoon and SEM of the gate polysilicon deposition

ization of the nitride polishing shown in section ??, characterization of the polishing rate of the polysilicon was performed using spectroreflectometry and confirmed with 4 point probe electrical measurements. Figure 5-26 shows the results of the characterization of the polishing rate of polysilicon. the rate was approximately 47 A/s, and both the optical and the electrical characterization are in agreement. Figure 5-27 shows the gate apertures after CMP.

After gate apertures are formed, the poly silicon gate is patterned with photolithography and a dry etch process. Ni/Ti/Au contact metal is deposited and patterned using a lift-off tech-

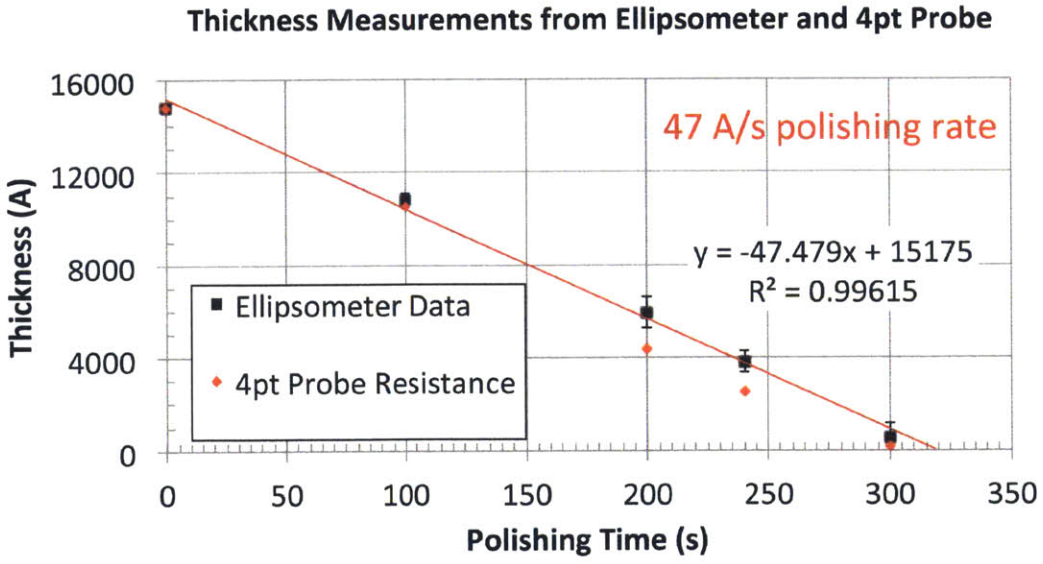


Figure 5-26: Characterization of the polysilicon polishing rate.

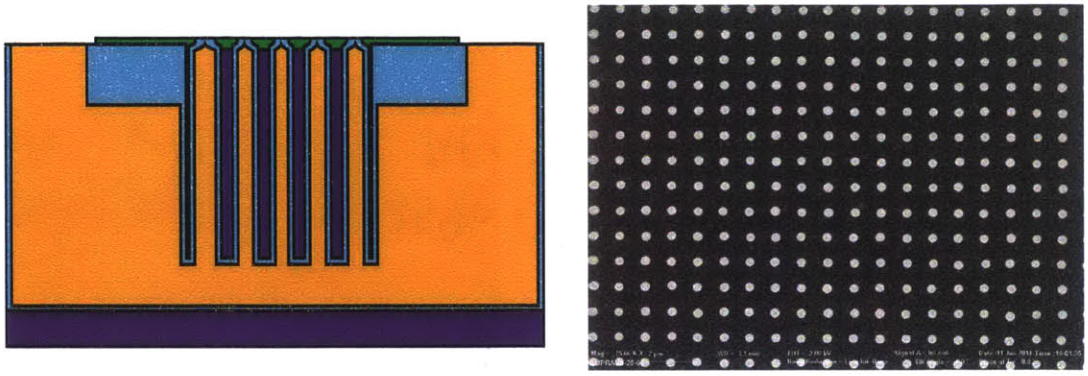


Figure 5-27: The gate apertures after CMP.

nique. The metal stack is sintered at 400 °C under forming gas for 30 minutes. During the sintering process, the nickel reacts with the polysilicon to form a nickel silicide, ensuring low contact resistance. Finally, a commercial pad etchant (Silox Vapox III, Transene Co., Danvers, MA) removes the oxide encasing the tips to expose the tips. The sample immediately is then dried with N_2 and loaded into the ultra-high-vacuum characterization chamber for I-V characterization. A tilted SEM image of the completed and released device is shown in Figure 5-28, and a cross section is shown in Figure 5-29.

As can be seen from the the SEM images, the silicon nanowires are 8 μm tall and < 200 nm in diameter, with the characteristic scalloping from the Bosch process. The emitter tips have a radius < 10 nm and the gate aperture diameter is $\approx$ 350 nm. The oxide outside of the array is 2 μm thick, and the polysilicon gate is $\approx$ 200 nm thick, with the emitter tip recessed from the top by $\approx$ 50 nm. Due to the sidewall slope of the mesa etch, there is a sharp, $\approx$ 1 μm tall ridge around the perimeter of the array, located $\approx$ 1 μm from the poly-Si/SiO_2 interface.

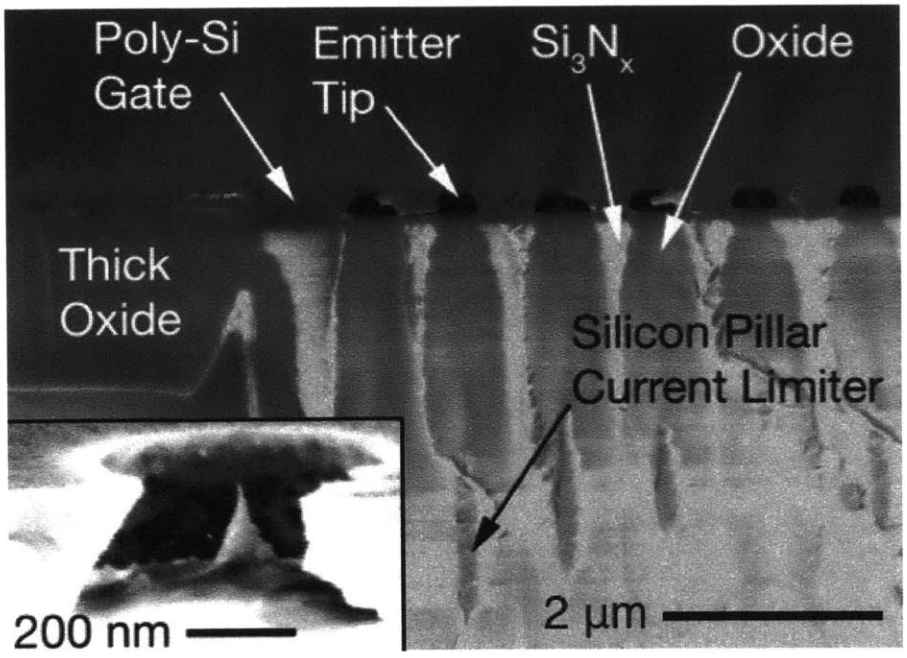


Figure 5-28: SEM cross-section of the completed Device structure.

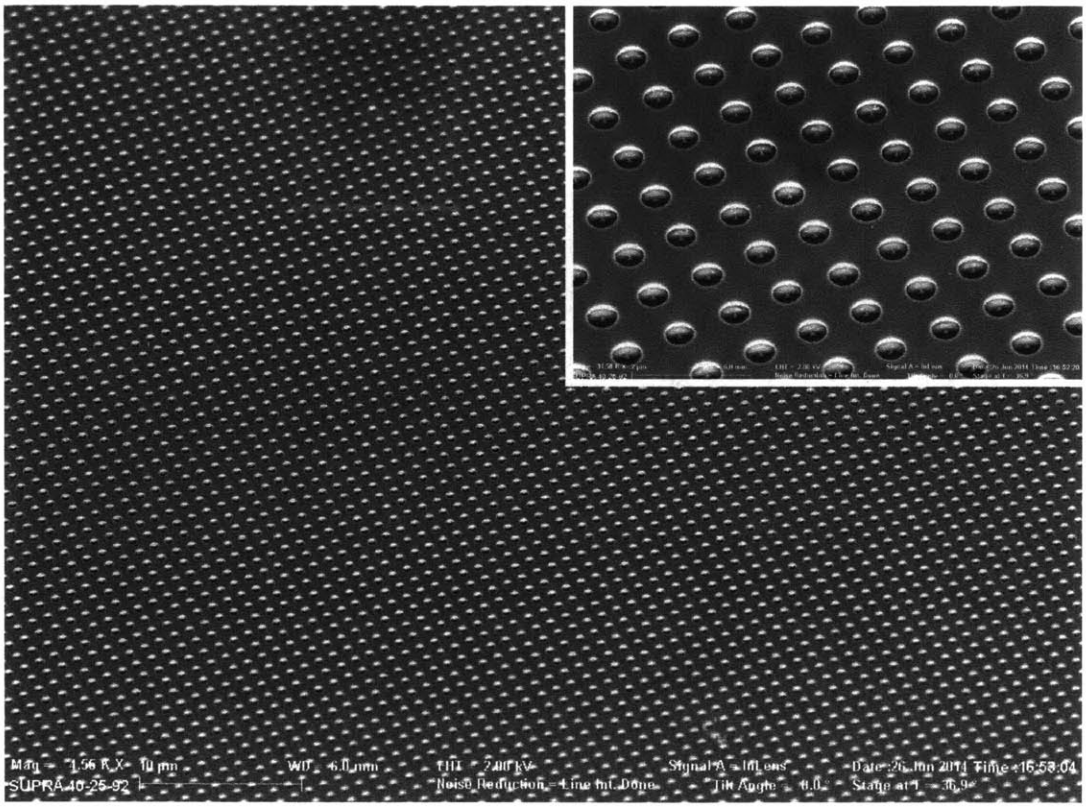


Figure 5-29: SEM of the completed Device structure.

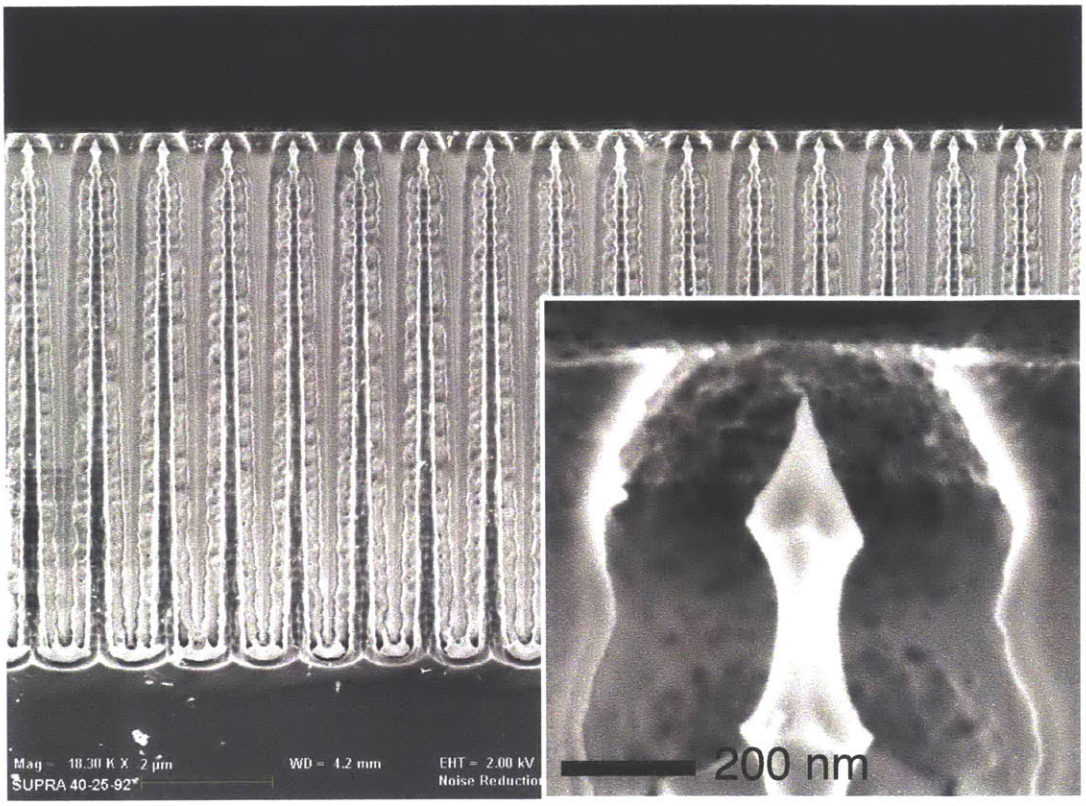


Figure 5-30: SEM of the completed Device structure with oxide removed to show detail of the Si nanowire. Inset: Detail of an emitter tip.

5.4.3 I-V Characterization

During I-V characterization, an ion pump maintained the test chamber under ultra-high-vacuum. The pressure was continually measured to monitor outgassing using the ion pump current and a Bayard-Alpert gauge. The pressure measured is below 3×10^{-10} Torr during the course of the experiments. The electrons emitted by the field emitter array is collected by a stainless steel, bakeable, Faraday cup anode placed approximately 1 cm above the surface of the chip. Three Keithley 237 high voltage SMUs source voltage and measure the emitter, gate and anode currents. These SMUs have ±1100 V range, can source current up to 10 mA, and measure current with resolution < 10 pA. MHV-5 electrical feedthroughs allow for electrical connection to the sample under test. Contact to the cathode was made to the backside through

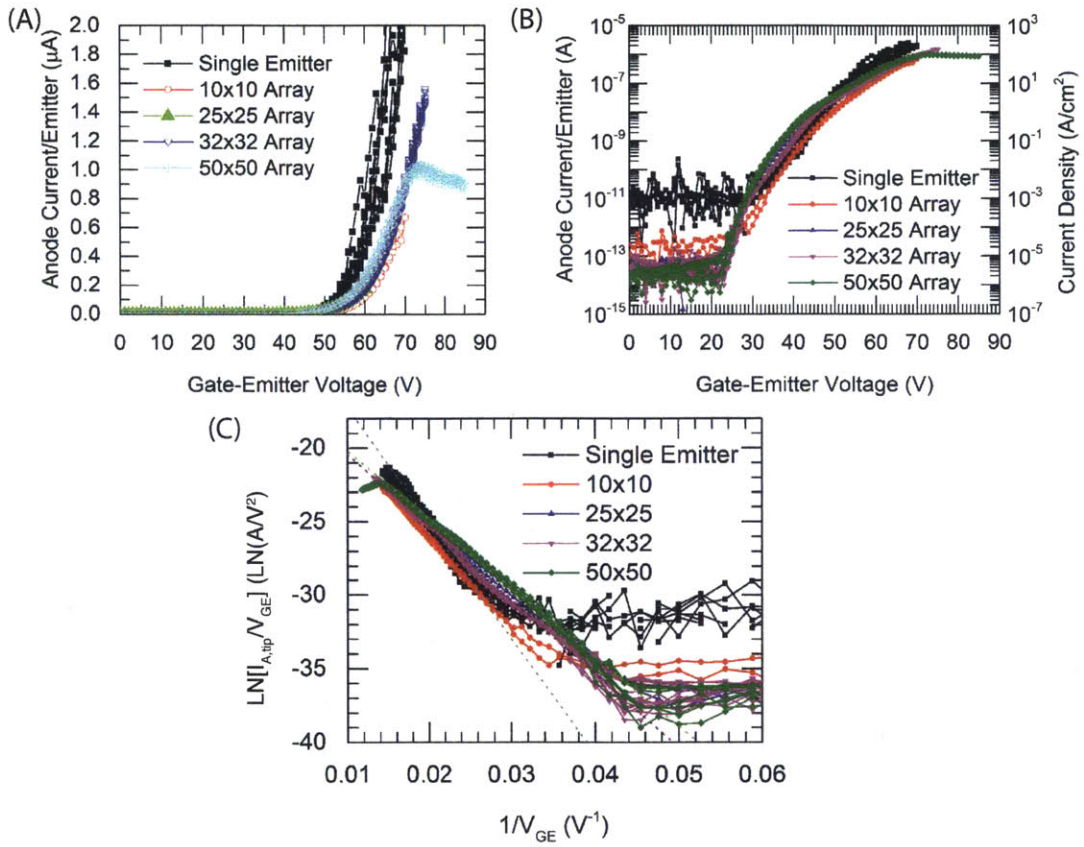


Figure 5-31: (A) I-V Characteristics (current per tip on a semilog scale), (B) IV Characteristics (current per tip on a linear scale), (C) F-N Plot per tip of a variety of different array sizes, demonstrating that current scales with the number of tips. In each of these devices except the 50 × 50 arrays at V_{GE} > 70 V, the total gate interception was less than 5 % of the emission current (anode efficiency > 95%.)

the chuck, and the gate was contacted with a tungsten probe.

Figure 5-31 shows the transfer characteristics for several different array sizes scaled by the number of tips in the array. Multiple sweeps were taken to ensure that the characteristics were stable. From the I-V characteristics, we see that the arrays do show good agreement with each other when scaled by the number of tips in the array. In each of these devices except the 50 × 50 arrays at V_{GE} > 70 V, the total gate interception was less than 5 % of the emission current (anode efficiency > 95%.

Figure 5-31 also shows the Fowler-Nordheim (F-N) plot, wherein $\ln\left(I_{A,tip}/V_{GE}^2\right)$ is plotted against the inverse of gate-emitter voltage. We define the Fowler-Nordheim coefficients in the

Array Size	Turn-on Voltage	Maximum Voltage	Maximum Current	Maximum Current/tip	FN Slope	FN Intercept per tip
Single Emitter	31 V	60 V	2.5 μA	2.5 μA	785	-9.39
10x10	27 V	70 V	67.8 μA	678 nA	610	-15.5
25x25	22 V	60 V	11 μA	176 nA	445	-16.3
32x32	23 V	65 V	1.6 mA	1.55 μA	498	-15.5
50x50	22 V	80 V	2.6 mA	1.04 μA	468	-15.5

Table 5.4: Summary of device performance for the characteristics

following way [116]:

$$\ln\left(\frac{I_A}{V_{GE}^2}\right) = \ln(a_{FN}) + \frac{b_{FN}}{V_{GE}} \tag{5.2}$$

where:

$$b_{FN} = \frac{0.95 \cdot 6.87 \times 10^7 \cdot \chi_{Si}^{3/2}}{\beta} \tag{5.3}$$

and

$$a_{FN} = \frac{\alpha A \beta^2}{1.1\chi_{Si}} \exp\left[\frac{B \cdot 1.44 \times 10^{-7}}{\chi_{Si}^{1/2}}\right] \tag{5.4}$$

where χ_{Si} is the barrier height (eV), assumed to be the electron affinity of silicon (4.05 eV, and β is the field factor (cm^{-1}) that converts the applied gate-emitter voltage to an effective tip surface field.

The Fowler-Nordheim plot is linear when the current is from electrons tunneling through the surface barrier. Small deviations from a linear relationship could be due to quantum effects in the emitter tip [100], a non-triangular tunneling barrier due to emitter geometry [79], or space charge limitation following Child's law [23].

The saturation of the anode current observed in the 50 × 50 array above a gate-to-emitter voltage of 70 V shown in Fig. 5-31 is not due to current limitation by the silicon nanowire, or any of these previously stated effects. We observed that the saturation of the anode current is

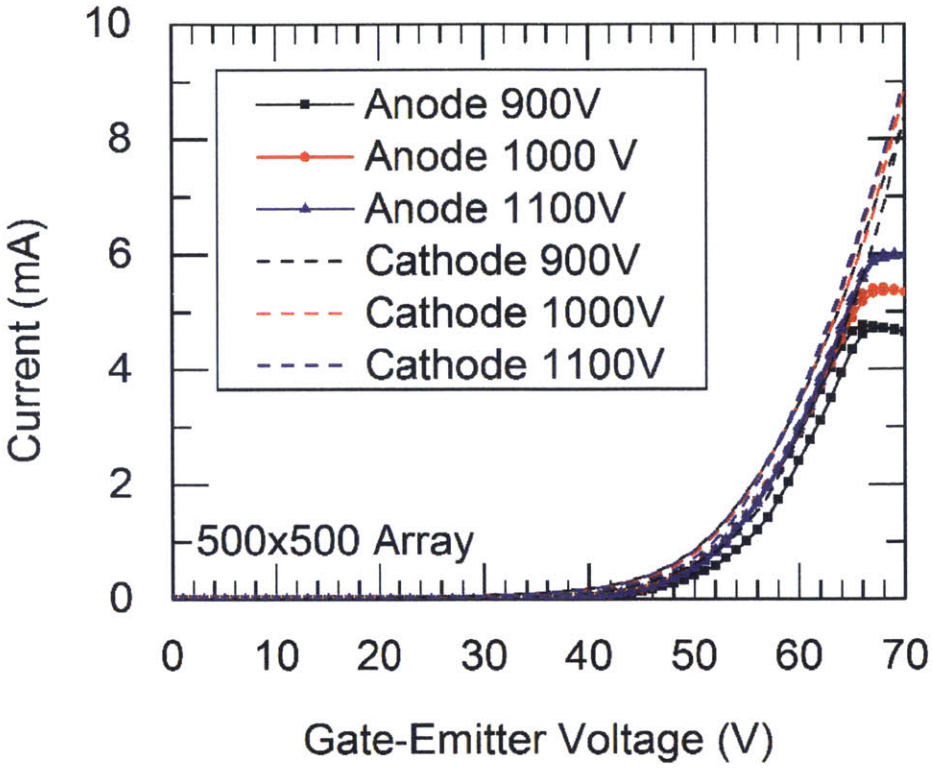


Figure 5-32: The effect of changing the anode voltage on a 500 × 500 array that exhibits current saturation.

accompanied by a corresponding increase of the gate current. Thus, the saturation is likely due to diversion of electrons to the gate after leaving the emitter tip due to insufficient anode field. This phenomenon could be mitigated by bringing the anode physically closer to the surface of the emitter or by increasing the voltage on the anode. Figure 5-32 shows a 500 × 500 array that demonstrated similar saturation as the 50 × 50 array. By modifying the anode voltage by 10 % (i.e. $V_A = 1000 \pm 100$ V, I_A changed by ±10%, accordingly, while the emitter current remained approximately constant.

The devices reported were designed to achieve high current and hence they do not demonstrate clear evidence of current limitation during normal DC operation. They do demonstrate, however, that they are robust, uniform, and their current scales with the number of tips in the array, thus implying that the silicon nanowires prevent catastrophic breakdown and improve uniformity.

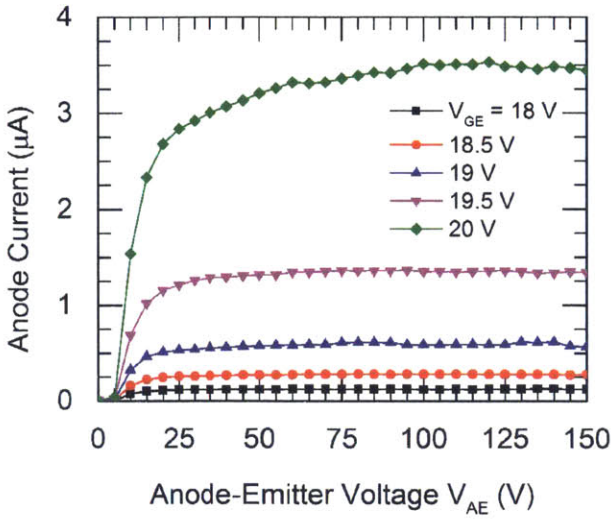


Figure 5-33: Output Characteristics for a 500x500 Array.

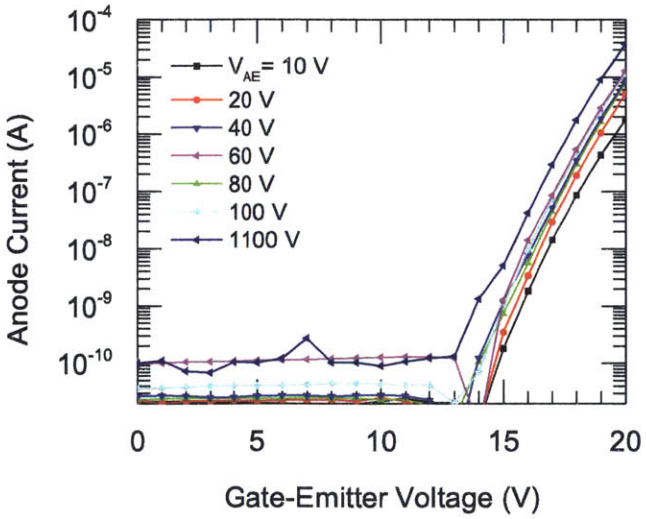


Figure 5-34: Transfer characteristics for the same 500x500 array shown in Figure 5-33

Figure 5-34 shows the output characteristics, and Figure 5-33 shows the transfer characteristic for a 500×500 array (250,000 emitter tips). The device turns on at a gate-emitter voltage of approximately $V_{GE,ON}$ = 14 V, and reaches > 3 μA of current (> 16 pA/emitter) at V_{GE} < 20 V. As expected, for gate voltages > $V_{GE,ON}$ the anode voltage has very little dependence on anode voltage.

Up until this point, we have only considered the effect of the gate-to-emitter voltage on the emission current, but in actuality, the voltage between the anode and teh emitter, V_{AE}, also applies an electric field to the emitter, and the electric field on the surface of the emitter is a superposition of the two, and we can consider an analogous field factor for the anode, which we will call γ [103] such that:

$$E_{surf} = \gamma V_{AE} + \beta V_{GE} \tag{5.5}$$

There is not much variation in emission current at high anode voltages, implying that the magnitude of γ is much less than β. This agrees with the fact that the anode is about 1 cm away from the emitter tip, while the gate directly surrounds the tip and is less than 200 nm away.

When the anode is at 0 V, the current collected by the anode approaches 0. This can be explained through the band diagram shown in Figure 5-35. In field emission, the electron are emitted from near the fermi level, and there is negligible scattering or momentum relaxation in vacuum. If the anode is at 0 V, there is a potential barrier at the anode with the height of barrier equal to the work function of the anode. This barrier repels incoming electrons, and directs them back towards the gate.

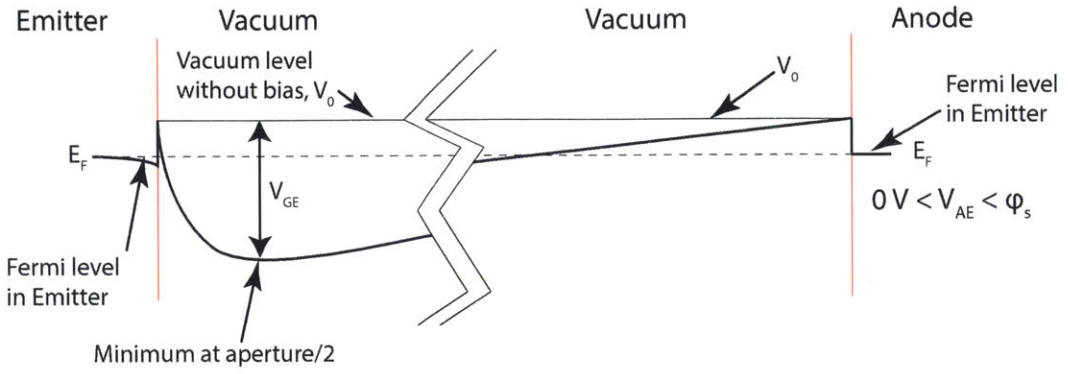


Figure 5-35: Band diagram from the emitter tip to the anode at $V_{AE} = 0$ V

When the anode voltage is increased to the work function of the anode (i.e. $V_{AE} = \phi_A$ as shown in Figure 5-36), electrons are collected by the anode. However, it is not a completely sharp on-off transition. If electrons are emitted from below the Fermi energy, they will not

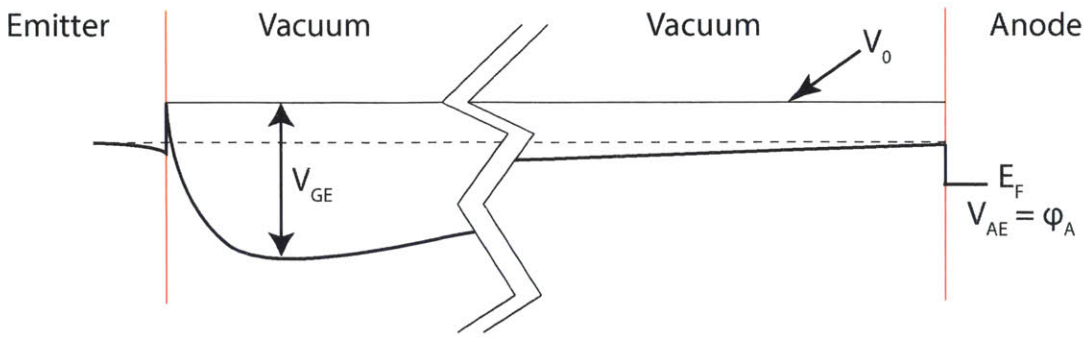


Figure 5-36: Band diagram from the emitter tip to the anode at $V_{AE} = \phi_A$

not have sufficient energy to be collected by the anode. In addition, due to the wave-particle dual nature of electrons, even though classically there should be no reflection of the potential barrier on the transmission of electrons, this is not the case, and a certain fraction of electrons are still repelled by the anode. To model this effect, we assume that the potential near the anode is approximately constant, and equal to $E_F - V_{AE} + \phi_A$ where V_{AE} is the anode-emitter voltage and ϕ_A is the work function of anode. Assuming a workfuction of 4.5 eV, we calculate a collection efficiency by the anode as shown in Figure 5-37. While the collection efficiency is not quite a step function, is it quite abrupt, with $\approx 75\%$ of electrons collected by the anode at 5 V, and $> 90\%$ collected by the anode at 5.5 V.

Although there is still a retarding field to overcome, the electron should attain enough energy through the initial acceleration by the gate field to overcome it. This may not be the case if the electrons are accelerated with a large transverse velocity component. The retarding field could cause the longitudinal velocity to go to zero and reflect electrons.

Increasing the anode voltage beyond the work function of the anode further lowers the potential barrier and allows a higher percentage of electrons to be collected by the anode (Figure 5-38). This can be explained both through the transmission coefficient of the quantum-mechanical barrier increasing, and there being a lower repulsive field that the electrons have to overcome. When we reach the typical regime of operation $V_{AE} \gg V_{GE}$ all of the electrons emitted through the gate aperture are collected by the anode.

Differentiating the transfer curve of $V_{AE} = 1100$ V yields the transconductance (gm) shown in Figure 5-39. At $V_{GE} = 20$ V, the gate transconductance reaches about 30 μS (0.12 nS/tip).

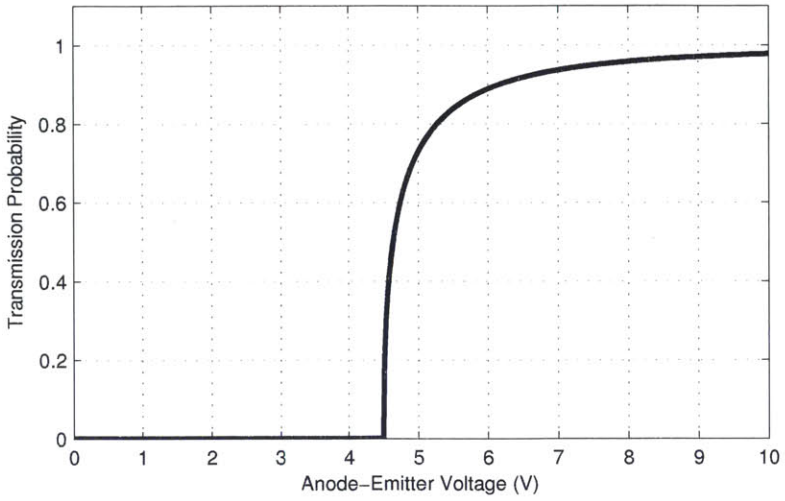


Figure 5-37: Collection probability of the anode as a function of anode-emitter voltage for $\phi_A = 4.5$ eV.

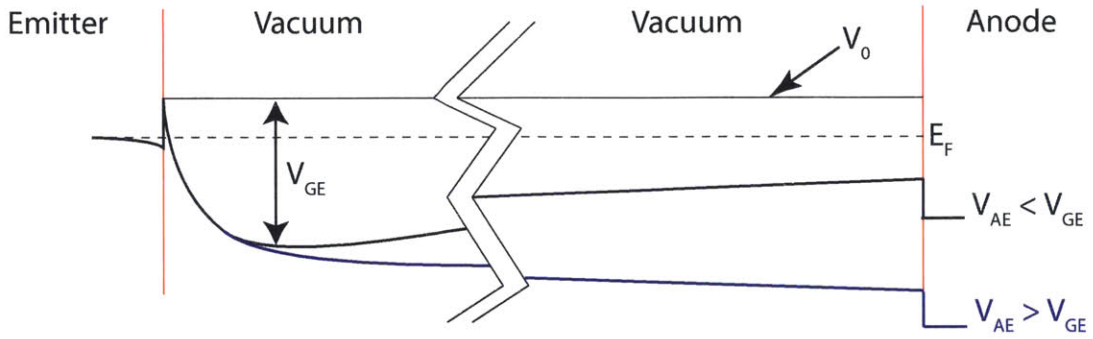


Figure 5-38: Band diagram from the emitter tip to the anode at $V_{AE} < V_{GE}$ and $V_{AE} > V_{GE}$ V

Extension to higher voltages and currents, such as those reported by Whaley et al. [126] would yield similar results, as the transconductance for a cathode scales exponentially with gate voltage, and the currents for which they report transconductance were for $V_{GE} > 60$ V.

Comparing these results to the output and transfer curves for a single emitter shown in Figure 5-41, we see some similarities. The 500x500 array turns on at a much lower voltage than the single emitter. This low turn-on voltage can be attributed to the noise floor of the measurement system, but also to the log-normal statistical variation of tip radius of emitter tips [55], that arises from the fabrication process we employed to make the nanometer-sharp silicon

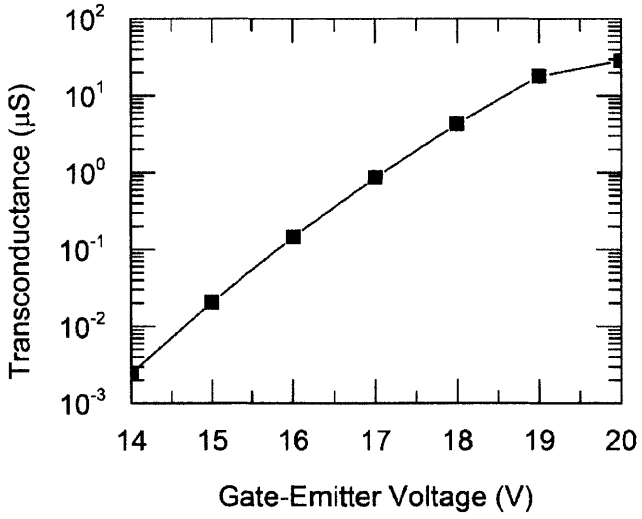


Figure 5-39: Gate Transconductance of the transfer characteristics shown in Figure 5-33.

emitters. Because of the distribution of tip radius, at low voltages, the several very sharp (radius $\approx$ 1 nm) emitters dominate the current characteristics. After prolonged emission or emission at higher voltages, the turn-on voltage shifts to higher voltages, perhaps due to emitter tip becoming blunt or to charging of the insulating oxide.

Ranadive developed an empirical model for the proportion of the emission current intercepted by the gate as opposed to collected by anode [106]. He argued that the anode current can be described as $I_A = \alpha_f I_E$ and that the gate current is $I_G = (1-\alpha_f)I_E$, where α_f is the transmission coefficient. Ranadive made the approximation that $alpha_f$ could be approximated as $1-\exp(-kV_{AE})$ and a linear relationship was discovered when $\ln[1-I_A/I_E]$ was plotted against V_{AE}. This plot for a single emitter with $V_{GE} = 40$ V is shown in figure 5-40. From the plot, we confirm that the relationship is roughly linear, with $k \approx -0.097$.

100 A/cm^2 Devices

In Figure 5-42, the transfer characteristics of 5 different field emitter arrays of different sizes ranging from a single emitter to 2500 emitters are overlaid on each other and scaled by the number of the tips in the array. Quantitatively, the single emitter has a higher turn-on voltage than the other sizes characterized, however, it is likely that the turn-on voltage is limited by the

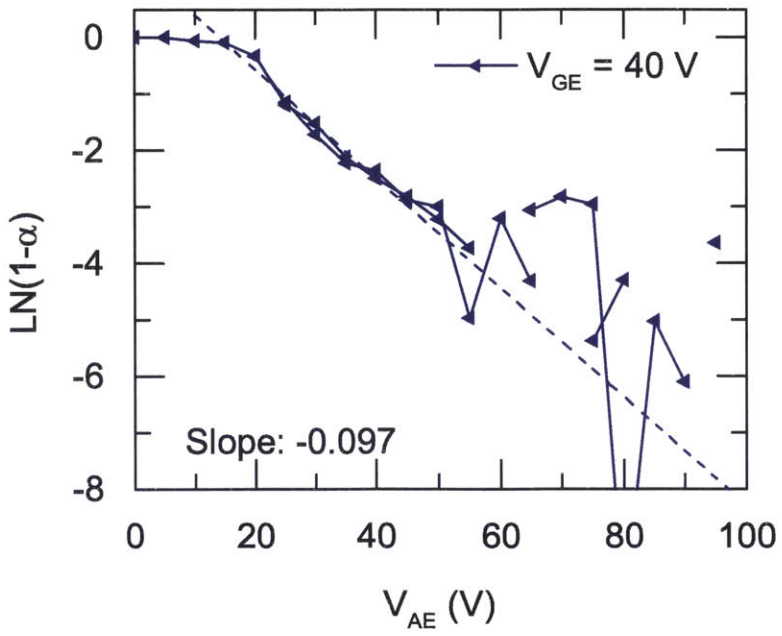


Figure 5-40: The Ranadive gate current model

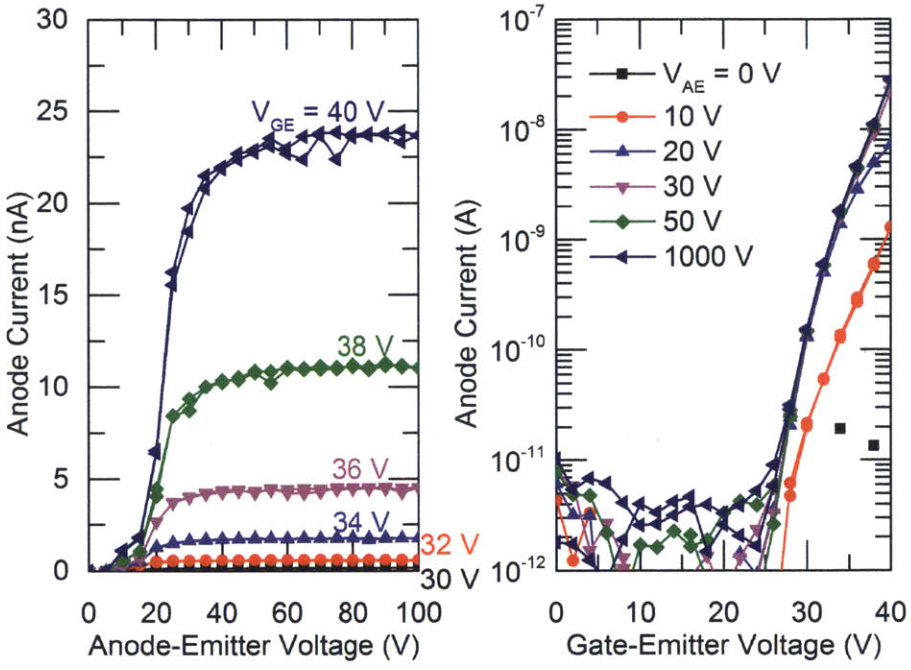


Figure 5-41: Output and transfer characteristics for the single device

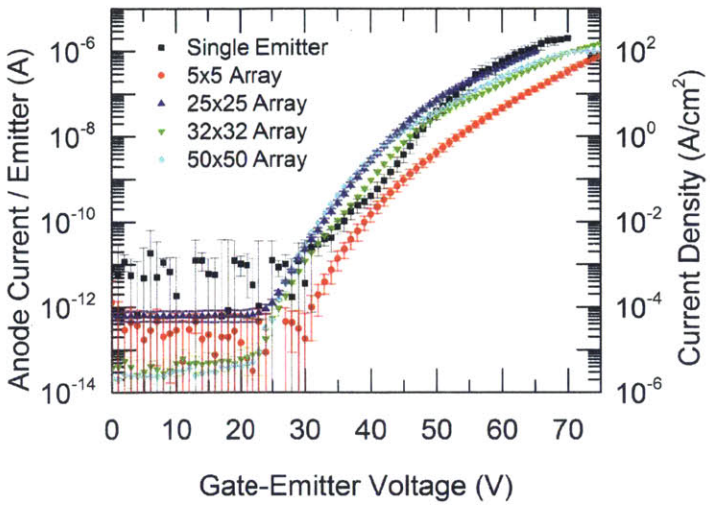


Figure 5-42: Comparison of the transfer characteristics of 5 different devices scaled by the number of emitters.

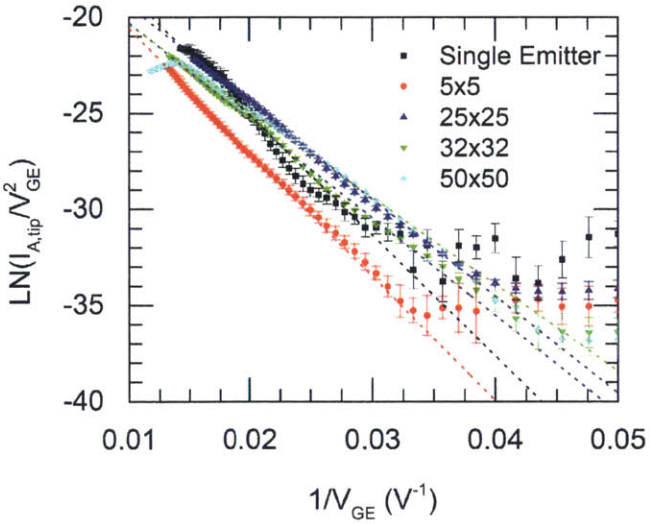


Figure 5-43: Fowler-Nordheim plot of the several different field emission arrays shown in the previous graph

noise floor in our measurement system. These results are summarized in Table 5.5

We find that as the array size increases, the effective tip radius decreases. There are two complementary explanations for this. First, proximity effects during the patterning cause the features in the center of the array to be slightly smaller than the features at the edge of the array, resulting in slightly sharper tips in the center versus the perimeter. The larger arrays have

	Single	5×5	25×25	32×32	50×50
$V_{GE,on}$ (V)	31	30	22	23	22
Max V_{GE} (V)	60	75	60	65	80
Max I_A (mA)	0.0025	0.240	0.655	1.55	2.6
Max I_A/Tip (μA)	2.5	0.96	1.04	1.55	1.04
Max J_A (A/cm^2)	250*	96	104	155	104
FN Slope, b_{FN} (V)	785	645	503	498	468
FN Int., ln(a_{FN}) (ln(A/V^2))	-9.39	-10.93	-7.93	-8.49	-7.72
FN Int./tip, ln(a_{FN})/tip (ln(A/V^2))	-9.39	-14.15	-14.37	-15.42	-15.54
Field Factor, β (cm^{-1} × 10^6)	0.669	0.821	1.054	1.068	1.137
Tip Radius (nm)	6.0	5.0	4.03	3.20	2.93

Table 5.5: Summary of device performance for the characteristics

a smaller number of perimeter emitters, thus there are a higher percentage sharper emitters in the larger arrays. This effect can be mitigated by using a more advanced lithography technology that employs edge proximity correction in the mask layout of subsequent revisions. Another explanation is that the emitter-tip radius follows a well-documented log-normal or Gaussian distribution [69]. As the array size increases, there is an increased likelihood that there are several sharper emitters in the array. These sharper emitters will dominate the performance at lower gate-emitter voltages and decrease the slope of the Fowler-Nordheim plot [95]. It is likely that both effects are contributing to the reduction in tip radius observed in our characteristics for the larger array sizes.

The saturation of the anode current observed in the 50×50 array above a gate-to-emitter voltage of 70 V is not due to current limitation by the silicon nanowire. The saturation of the anode current is accompanied by a corresponding increase of the gate current. The anode current saturation can thus be explained by the diversion of electrons to the gate after leaving the emitter tip. Due to strength of the gate-to-emitter (lateral) electrostatic field relative to the anode-to-emitter (vertical) electrostatic field, the electrons preferentially arrive at the gate instead of the emitter at gate-emitter voltages greater than 70 V due to insufficient anode electric

field. By increasing the voltage on the anode, or by bringing the anode physically closer to the surface of the emitter, the anode electric field can be increased, leading to an increase of the gate-emitter voltage at which the electrons are intercepted by the gate can occur. This effect was measured and is shown in Figure 5-32.

In Figure 5-44, we compare the I-V characteristics of a single emitter with a simulated device in SILVACO. The details of the simulation are given in Section 5.2. A 2.5-D simulation structure was used were considered, where a 2-D axisymmetric structure was generated programmatically in MATLAB so that the tip radius and meshing is precisely defined. We find that using the doping and the tip radius as parameters, we can get good quantitative agreement between the simulation and the current measured for reasonable tip radii and doping densities.

To fit the simulation results to the measured I-V characteristics, a tip radius of 6.5 nm and a doping density of 2.5×10^{16} cm^{-3} were used. A simulation of the wet thermal oxidation used to sharpen the tips and shrink the nanowire suggests that the doping density inside the nanowire is slightly lower, $\sim 1.5 \times 10^{16}$ cm^{-3}. The simulated I-V characteristic had an FN slope of 624, in agreement with the measured FN slope of 626. The FN intercepts of the simulated and measured characteristics were -12.38 and -12.63. Using the model developed in Section 5.4.4 below, we extract a tip radius of 8.3 nm. The experimental FN characteristic appears to deviate from its linear relationship at $V_{GE} \approx 60$ V, and the simulation suggests that the current limiter saturates at $V_{GE} \simeq 60$ V.

5.4.4 New technique for electrical estimation of emitter tip statistics

It is a significant challenge to image the fine structure of the tip with TEM and SEM due to the many different material layers in the field emitter structure, and the high packing density. The particular challenge of imaging the field emitter tip with high resolution SEM is charging of the surrounding oxide layers. With TEM, there is a significant risk of damaging the tip geometry and re-depositing of material onto the tip during sample preparation with focused ion beam (FIB) milling. In the absence of traditional tools of analyzing the uniformity of our field emitter tips, we explore below the extraction of the tip distribution using our current voltage characteristics.

A simple analytical model relating the field factor, β, to the emitter tip radius is the ball-

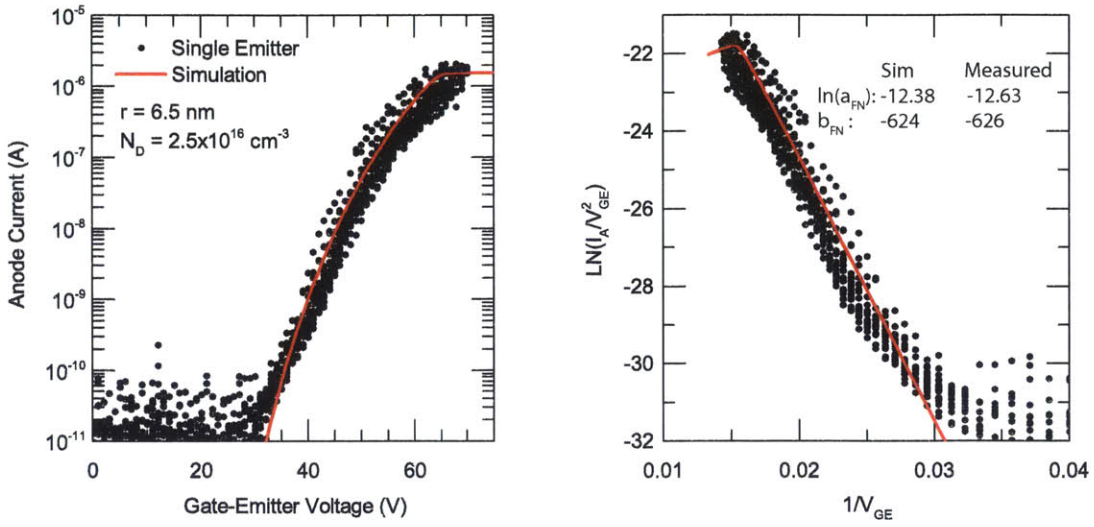


Figure 5-44: Comparison of simulated I-V characteristics (left) and FN chart (right) to experimental data for a single emitter (black dots).

in-sphere model [32]. In the ball in sphere model, the emitter tip is modeled as a hard, metal sphere of radius r in a large, spherical shell of radius R. The relationship of the voltage on the sphere to the electric field at the surface of the sphere is simply given by the solution of Laplace's equation in spherical coordinates.

$$\beta = \frac{1}{r} - \frac{1}{R-r} \approx \frac{1}{r} | r \ll R \tag{5.6}$$

While this model is very simple to use and could give results that are reasonable to within an order of magnitude, it is not very accurate for realistic tip and gate geometries and underestimates the tip radius for emitters that are sharper than 20 nm. To build a better estimate for tip radius for our structure, we developed a finite element model for the silicon nanowires capped with field emitter tips embedded in a dielectric matrix using COMSOL Multiphysics. The element (silicon nanowire capped with silicon tip) is modeled using cylindrical symmetry around the central axis of the emitter (i.e. $r = 0$). The emitter is simulated as having an emitter half-cone angle of 30°. The nanowire diameter is 200 nm, and the nanowire is 8 microns tall. The emitter tip radius is varied between 0.5 nm and 50 nm. The gate aperture is 350 nm, and the gate thickness is 250 nm. Aside from the tip, the pillar is buried in silicon dioxide with relative dielectric constant $\epsilon_{ox} = 3.9$. The surface is assumed to be ideal with no fixed charge or

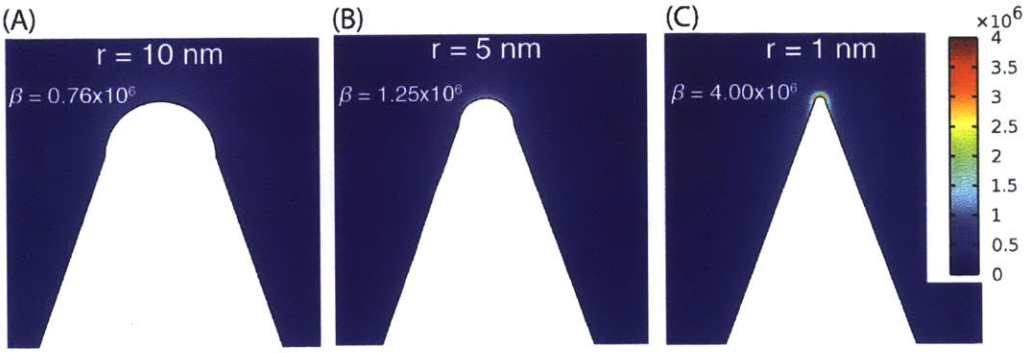


Figure 5-45: Finite element electrostatics simulation to determine the relationship between tip radius (r) and field factor (β) for the silicon nanowire with self-aligned gated tip. The nanowire is 200 nm in diameter and 10 microns tall, with a tip half-cone angle of 30 degrees. (A)-(C) Detail of the electric field around the apex of the tip for tip radii of 10 nm (A), 5 nm (B), and 1 nm (C).

surface states. In addition, it is assumed that there is no current or space charge in the system. The emitter is assumed to be a perfect conductor, that is, the voltage along the emitter surface is set to 0 V. The polysilicon gate is also modeled as a perfect conductor, and the voltage on the gate is 1 V. The boundary condition at $r = 0$ is set to $(\partial E_r)/\partial r = 0$, and the solution of the potential and the electric field in the structure is reduced to a boundary value problem. With these boundary conditions (i.e. $V_{GE} = 1$ V), the maximum electric field at the apex of the field emitter in V/cm is the field factor, β.

The finite element simulation of the tip geometry, shown in Figure 5-45(A)-(C), plots the electric field proximal to tips of various emitter radii. By reducing the emitter tip radius from 10 nm to 1 nm, the field factor is increased from 0.76×10^6 cm^{-1} to 4.0×10^6 cm^{-1}. If we plot the results for emitters in the range $0.5 < r < 50$ nm, we find the result shown in Figure 5-46. Dvorson et al. [37], Jensen et al. [70] and Ding et al. [32] developed analytical models that show that the field factor for conical emitters follow the form $\beta = k/r^n$. By fitting an equation of that form to the field factors extracted from the numerical model, we obtained a very good fit to our data with a $\beta = 4.075 \times 10^6/r^{0.7417}$ cm^{-1} for r in nm.

It is unsurprising that the finite element model indicates that β does not strictly follow $1/r$. for $\beta = 1/r$ to be precisely true, spherical symmetry would need to be maintained. instead, the gate is roughly cylindrical, the emitter tip is a cone, and the gate only subtends a fraction

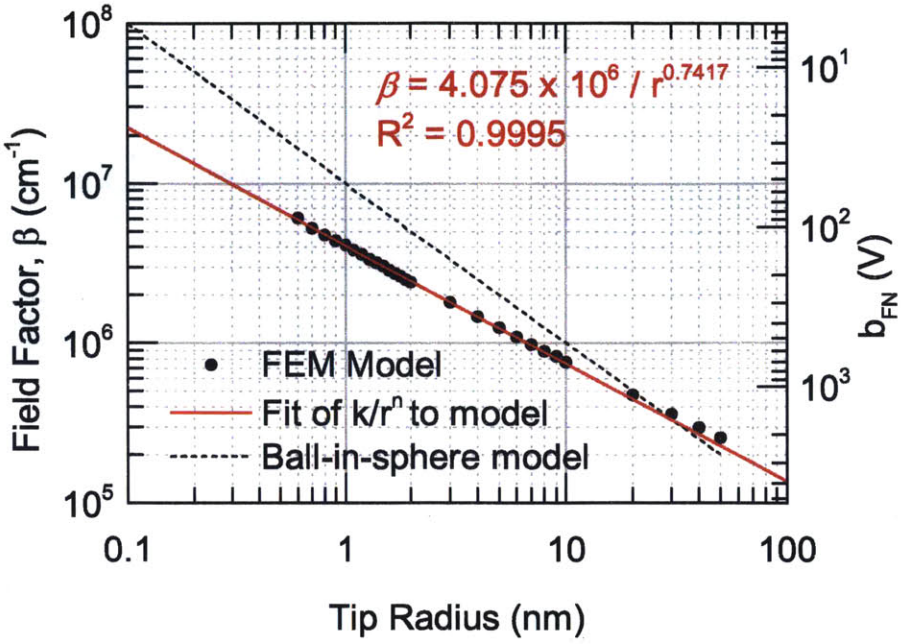


Figure 5-46: Fit of field factors with the model $\beta = k/r^n$ from the finite element electrostatics model shows good experimental agreement for this structure for $r = 0.5 - 50$ nm.

of the angle of the emitter tip surface.

From the relationship between tip radius and the field factor for our structure, we can use the slope of the Fowler-Nordheim plots of our I-V characteristics to estimate the average radius of the emitter tips in the array assuming that the silicon workfunction is its electron affinity. Over 150 plots from 20 different devices were analyzed for their Fowler-Nordheim slopes, and their tip radii were extracted. Table 5.6 shows the number of characteristics used for each device size. The results for the tip radii estimates for the different plots are summarized in the box chart shown in Figure 5-47.

The mean of the average tip radii extracted from the current voltage characteristics of the filed emitter arrays decreases from 8.7 nm for the single emitter to 4.8 nm for the 25×25 array. It is likely that in the smaller arrays, edge effects have a large effect on the tip radius distribution. For example, in the 10×10 array, 36 % of emitters are on the perimeter, and 64% of emitters are either on the perimeter, or nearest neighbors to the perimeter. As the size of the array increases, the percentage of emitters along the perimeter becomes. It is expected that the lithographic

conditions (photon flux distribution) is not symmetric for nanowires/emitters situated on the perimeter. This will result in features that are slightly smaller. During oxidation, these slightly smaller features might have been over-oxidized, resulting in an emitter tip that is not as sharp.

Array Size	Number of Characteristics Used
1	39
100	11
625	28
1024	20
2500	15
10000	25
250000	11

Table 5.6: Summary of device performance for the characteristics

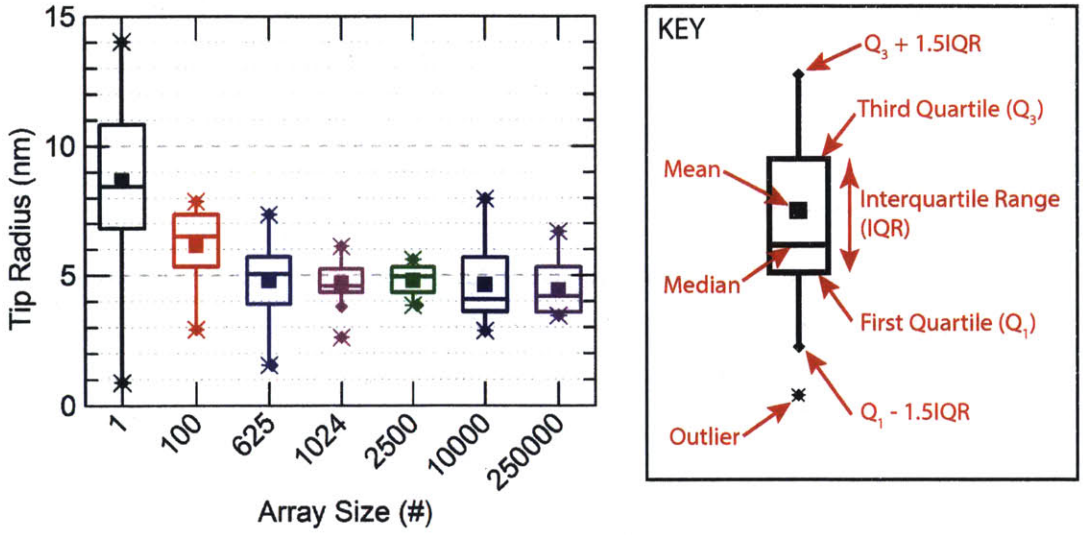


Figure 5-47: Box chart of the distribution of average effective tip radii extracted from I-V characteristics and fitted to tip radius using the extrapolation from the finite element model. The square in the center of each box indicates the mean value of tip radius of the distribution. The horizontal line inside of each box is the median value of tip radius. The upper and lower bounds of the box show the first (Q_1) and third quartiles (Q_3) of the tip radius distribution, the height of the box is the inter-quartile range (IQR). The terminal points of the vertical lines extending from the boxes show approximately $\pm 3\sigma$ (i.e. $Q_1 - 1.5 \times \text{IQR}$ and $Q_3 + 1.5 \times \text{IQR}$). The starred points are outliers.

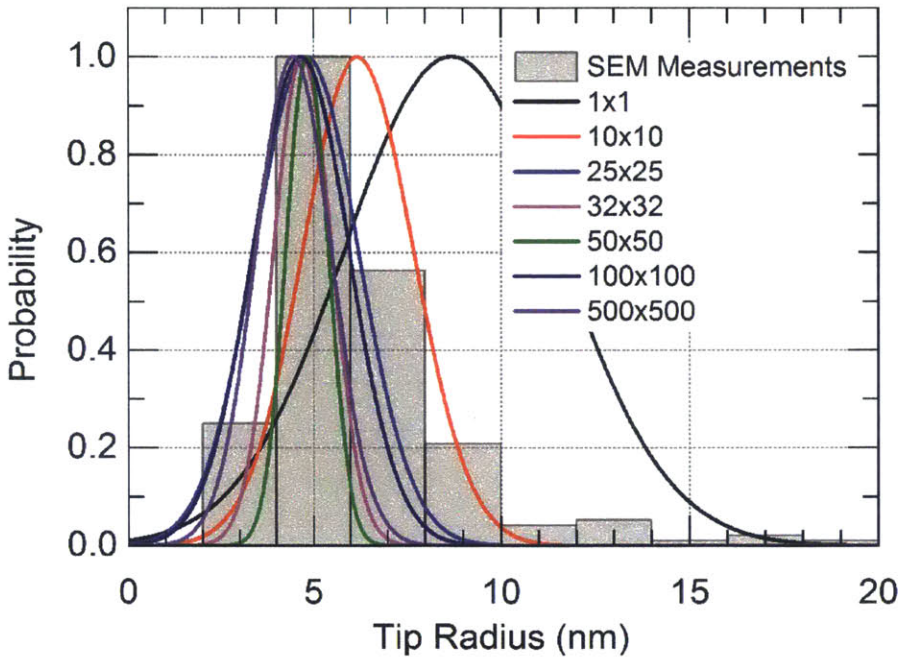


Figure 5-48: Probability density functions of the average effective tip radii of different array sizes based on the statistics of the data summarized in Figure 5-47 superimposed a histogram of 200 tip radii measured on a representative sample.

This effect will be reduced by adding perimeter corrections to the mask.

For arrays larger than 625, the average tip radius tends to be between 4 and 5 nm, consistent with previous work on silicon field emitter arrays. For arrays larger than 1000 emitters, the variation tends to be smaller. This is probably due to the law of large numbers, and the averaging effect that takes place with the large number of emitters. It was expected that there would be a slight trend for the tip radius to decrease with array size due to the presence of a few sharper "hero" emitters dominating the emission at lower voltages; however, this effect does not appear to be present in the data presented. Either the arrays are extremely uniform that there are not many of these very sharp emitters, or the presence of the silicon pillar nanowire prevents them for contributing an overly large percentage of the current. If the statistics obtained from the IV characterization are plotted as Gaussian probability density functions, as shown in Figure 5-48, the larger arrays all converge around 4.8 nm. The distribution is consistent with those obtained from SEM measurements of tips without gates previously reported in Guerrera et al. [55]. We

should add a caveat that the distribution extracted from the IV characteristics would naturally favor smaller tip radius and perhaps tighter distribution principally due to the exponential relationship between the field factor (and hence the tip radius) on the emission current.

5.4.5 Emission Angle Measurements

This section examines the angle of emission of the silicon FEA through the use of a low voltage phosphor screen. From the spot size, we can obtain estimates about the distribution of transverse energy of the electrons that are being emitted and make some estimates about the brightness of our electron source.

Figure 5-49 shows a schematic of the experimental setup used for these measurements. The field emitter array with width a emits electrons. These electrons have a certain transverse velocity v_x that gives rise to a divergence in the beam once it leaves the emitter. A ZnO phosphor screen, biased at 900 V is placed at a height h above the field emitter array. When the emitted electrons impact the phosphor screen, they excite phosphors in a spot on the phosphor screen with width d through cathodeluminescense (CL). In CL, the electrons generate electron-hole pairs called excitons. These excitons transfer energy to an impurity "activator" ion, which is then excited to a higher level, relaxes to a radiating level, and then radiatively transitions back to the lower level to produce light[107]. This light is then collected by a microscope objective, and imaged onto a scientific CCD digital camera (QImaging Retiga camera).

A 25 × 25 array was used for these experiments. The I-V and F-N characteristics of the device are shown in Figure 5-50. The device turned on at $\sim$ 30 V and had an average tip radius of $\sim$ 10 nm based on the Fowler-Nordheim slope of 700 V. During I-V characterization, the phosphor screen anode was kept at $\sim$ 5 mm, and biased at $V_{AE} = 900$ V, while the gate voltage, V_{GE} was ramped from 0 to 60 V. For the imaging of the phosphor screen, the gate electrode was biased at a constant gate-emitter voltage $V_{GE} = 60$ V and the anode at $V_{AE} = 900$ V. The array produced an anode current of $I_A \approx 3.5$ μA. The gate leakage is about 50 nA at 60 V, and follows Fowler-Nordheim behavior. Images of the phosphor screen were collected at various heights between 4.6 mm, and 8.3 mm, as shown in Figure 5-51.

To calibrate the height of the phosphor screen above the sample, the trendline of the width of the spot above the sample was extrapolated back to a separation of 0, and set to the width of

the array, 25 μm. The relative spacing between the different spots is measured by a micrometer and accurate to $\pm$25.4 μm. To obtain repeatable results, care was taken to ensure that each image was collected and processed exactly the same. The anode was kept at a constant bias of 900 V, and the camera used a 90 second exposure with a gain of 8. Such a long exposure was needed because of the low efficiency of low-voltage phosphor screens. Recombination at the surface quenches phosphorescence and reduces the brightness, and because the phosphor screen is not metallized, half of the light that is generated is directed downwards and away from the camera, and more of the light is piped away from the camera in the glass substrate of the phosphor screen due to total internal reflection.

After the image was collected and saved, it was imported into photoshop. An image of the substrate was used to calibrate the size of the pixels to quantitatively measure the spot size. In photoshop, the width of the spot was measured, and the brightness/contrast was changed to +75/-25 respectively to obtain a clear reproduction when printed.

The spot on the phosphor screen appears oblong, with one axis cut off on one end. The end is that is cut-off is likely due to the probe deforming the electric field and occluding the phosphor screen. The spot may be longer in one axis than the other because of non-uniformity

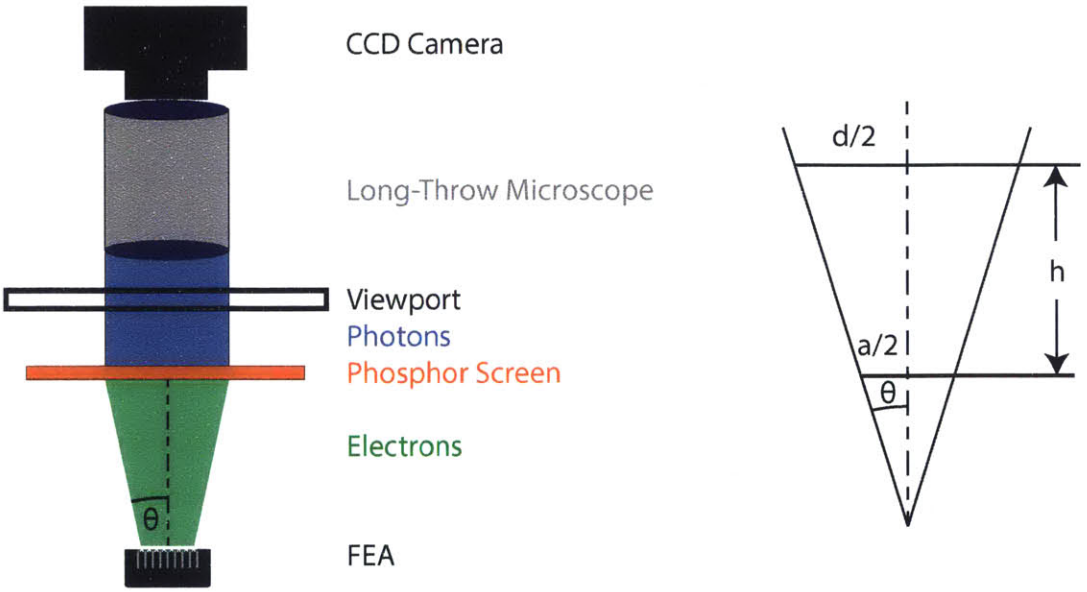


Figure 5-49: Diagram of the measurement Setup

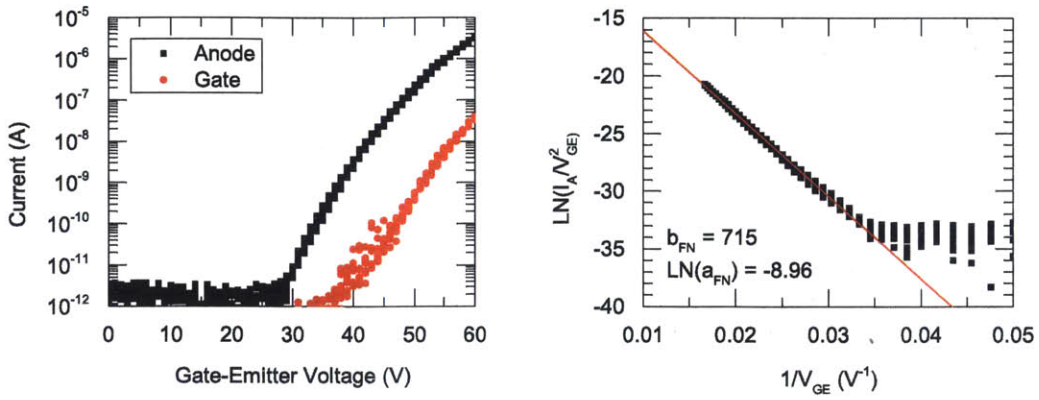


Figure 5-50: I-V characteristics (left) and Fowler-Nordheim characteristics (right) of the device used for emission angle experiments

in the chemical-mechanical polishing, resulting in the top not being exactly in the center of the aperture. Figure 5-52 plots the width of the spot vs. height. While the accuracy of the spacing between the points is ±25 μm, to calibrate the height of the phosphor relative to the substrate, the points were shifted so that the y-intercept of the least squares linear regression was half the array width.

From the spot size, we can calculate the emission half-angle through:

$$\tan\theta = \frac{1}{2}\frac{dx}{dh} \tag{5.7}$$

Where dx/dh is the slope of the half-width of the spot size. We find that the emission angle is ≈ 12.3° (≈ 200 mrad). This number agrees quite well with previous results reported in the thesis of M. Ding, who found that Si FEAs with apertures formed with CMP had an emission angle of 12.6° [30].

From the spot size, we can obtain an estimate of the transverse velocity and transverse energy of emitted electrons. When an electron is emitted at an angle away from the apex of the emitter tip, it will gain some transverse energy due to the roughly spherical gate field profile around the tip. Once the electron is far enough from the gate electrode (approximately several gate diameters), it will be accelerated by the anode field (which is roughly constant and perpendicular to the substrate), but the electrons will retain the transverse velocity they attained from acceleration from the gate field. Hence, the transverse velocity should depend on the gate

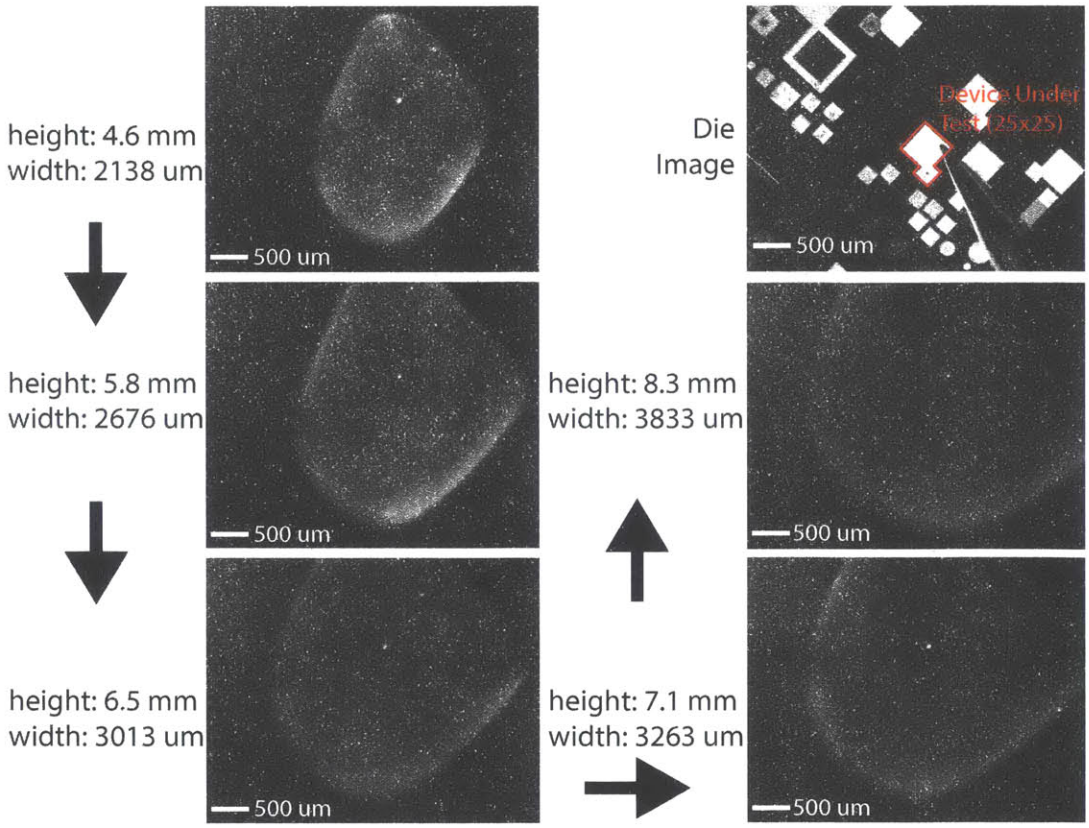


Figure 5-51: Dependence of the spot size on the height of the phosphor screen. Spots produced on the phosphor anode with $V_G = 60$ V, $V_E = 0$ V, $V_A = 900$ V, $I_A \approx 3.5$ μA. The gate leakage is about 50 nA at 60 V, and appears to follow Fowler-Nordheim behavior. The spot size measurement was taken on the short axis of the spot. There was a linear relationship between spot size and the height.

voltage, but not the anode voltage.

From the height, h, we can calculate the travel time Δt by assuming that the force on the electrons is constant and equal to qE where the electric field is approximately equal to the anode voltage divided by the separation between the phosphor screen anode and the FEA, i.e. $E = V_A/h$. With a known travel time, we can then estimate the transverse velocity, v_x given the displacement Δx, assuming that Δx is the half-spot size.

$$h = \frac{1}{2}\frac{qV_A}{mh}(\Delta t)^2 \rightarrow \Delta t = h\sqrt{\frac{2m}{qV_A}} \rightarrow v_x = \frac{\Delta x}{h\sqrt{\frac{2m}{qV_A}}} \tag{5.8}$$

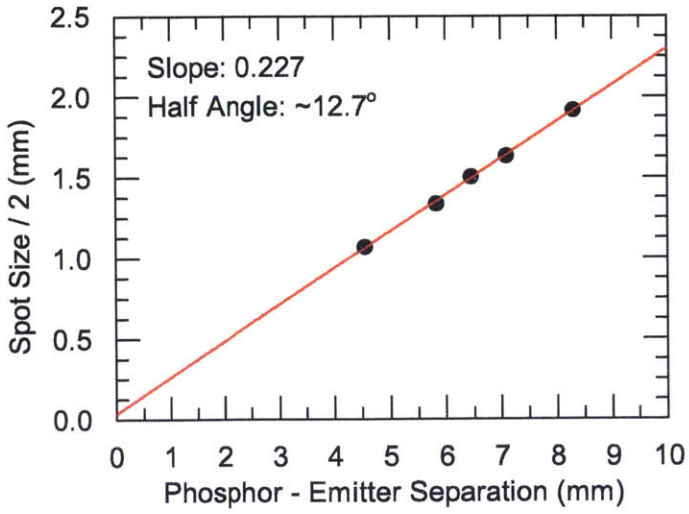


Figure 5-52: Extraction of emission angle from spot size measurements

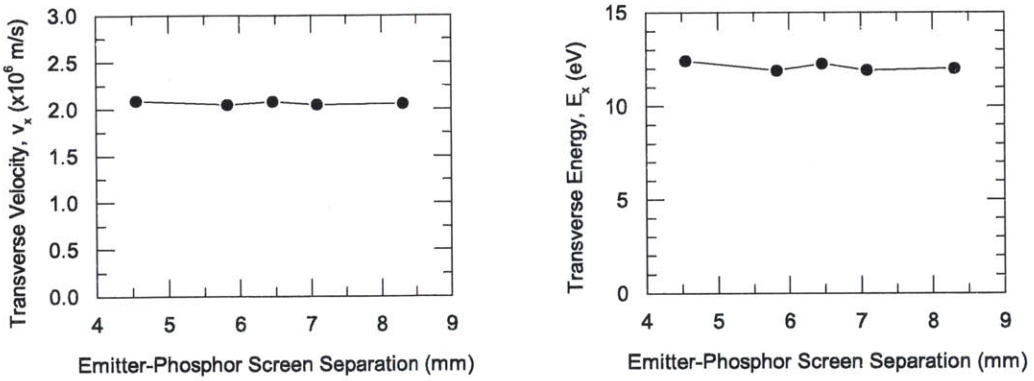


Figure 5-53: Transverse velocity (left) and energy (right) for the different anode-emitter separations measured.

Using this approach, we find a transverse velocity of $\approx 2\times10^6$ m/s. Estimating the transverse energy as $E_x = \frac{1}{2}mv_x^2$, we find that the electrons have a transverse energy of ≈ 12 eV. Figure 5-53 shows the transverse velocity and energy of the different anode heights measured, showing good agreement between the different measurements.

5.4.6 Failure Analysis

When gate-emitter voltages greater than approximately 65-80 V are applied, the devices can sometimes exhibit sudden catastrophic failure. These failures are associated with a sharp pressure rise and a drop in emission current. Figure 5-54 is an example of the I-V sweep of a device that failed at $V_{GE} = 70$ V.

Before failure, the device was emitting approximately 650 nA/emitter, for a current density of 65 A/cm^2. The gate current was $\approx$ 1 μA, less than 1 % of the total current emitted by the anode. During the 6th sweep, emission suddenly ceased, and the pressure increased from $\approx 2 \times 10^{-10}$ Torr to 1×10^{-9} Torr. The gate current characteristic changed: the gate current decreased at higher voltages, but increased at lower voltages.

A plausible explanation for the shift in the gate current is thus: Before failure, the gate current at high voltages is due to interception of emitted electrons by the gate. This is corroborated by the almost linear Fowler-Nordheim characteristic of the gate current at higher gate-emitter voltages. After the sudden failure, the electron emission is "turned off" but a resistive leakage path between the substrate and the gate is formed, causing the gate leakage to be higher at low voltages, but lacking the exponential nature of field emission.

There are several possible causes of this dielectric failure:

1. Charge injection and breakdown inside the oxide

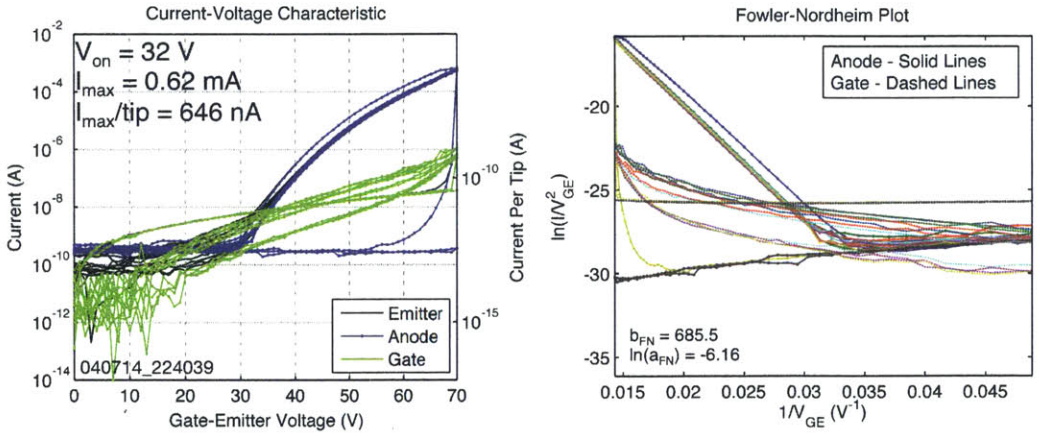


Figure 5-54: I-V and FN plots of a device that demonstrated sudden catastrophic failure at $V_{GE} = 70$ V

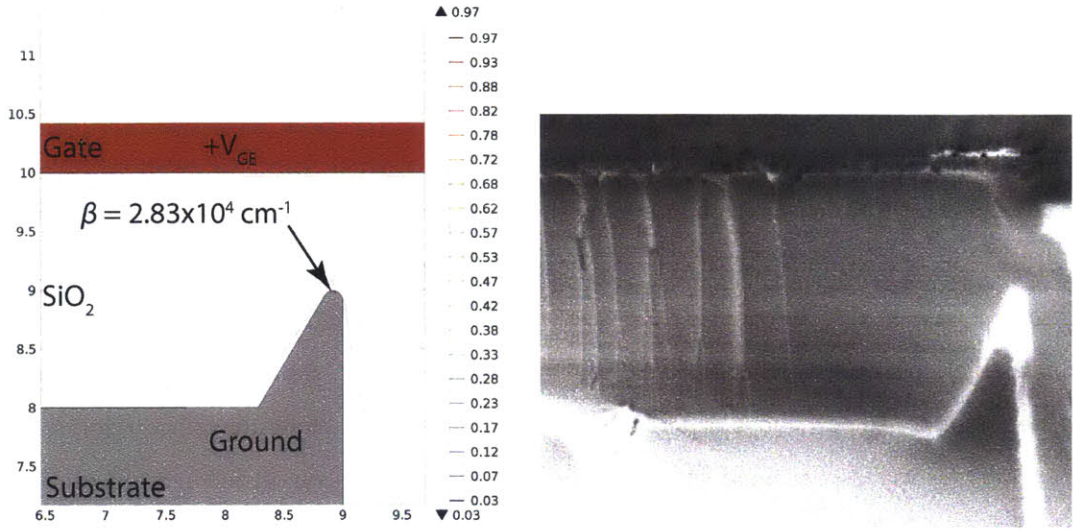


Figure 5-55: Comparison of the finite element simulation of the ridge found at the edge of the array with a cross-section SEM of the ridge. There is a field enhancement of approximately 5 at the apex of the ridge.

2. Flashover and vacuum breakdown at the gate, SiO_2, vacuum triple point [5, 50, 115].

Cross-section SEMs of the completed device revealed a possible failure point is a sharp ridge that formed around the active device region. This ridge was inadvertently created during the mesa etch due to the etch being unoptimized and thus having an isotropic component. This ridge has a prominence of 1 μm above the substrate, and a radius at the tip of approximately 120 nm. Finite element simulations of the ridge indicate that the electric field at the apex of the ridge is > 5× greater than the electric field in the rest of the oxide, and thus is a likely location for failure. Figure 5-55 compares the finite element model (with equipotential lines drawn) with the SEM of the structure.

With 70 V on the gate and the substrate at ground, the electric field at the apex of the ridge is approximately 3 MV/cm. The intrinsic dielectric strength of SiO_2 is often reported at 10 MV/cm [119], however, this SiO_2 has undergone significant plasma processing, as well as CMP. It is possible that some of these processes have introduced defect sites into the oxide, reducing its dielectric strength and causing failure at lower than expected fields.

5.5 Summary

This chapter covered the design, fabrication process development, fabrication, modeling, and characterization of silicon field emitter arrays with self-aligned gates and integrated silicon nanowire current limiters. Exploratory experiments in filling the voids between high-aspect-ratio silicon pillars revealed that it was a significant materials and processing challenge, and extensive work was done to develop a process for the void-free, filling of these gaps with a high quality dielectric material that could support the polysilicon gate. A process that used a combination of undoped polysilicon deposition and oxidation, as well as low-stress silicon nitride was presented, as well as a method that used selective etching of silicon nitride over silicon dioxide to form self-aligned gate apertures. These exploratory experiments yielded functional field emitter arrays, demonstrating a turn-on voltage $\approx$ 20 V and current saturation at 30 V, however, these devices suffered from large gate-substrate leakage current. To address this leakage current, a new device architecture was proposed that incorporates a thick dielectric surrounding the array, and a process to ensure that the gate polysilicon remains outside of the active array after processing.

These new devices exhibit record current density for Si field emitter arrays, with sustained currents > 1 μA/tip and current densities > 150 A/cm^2 @ V_{GE} < 70 V. The results are consistent with numerical simulations and analytical models. A number of different-sized arrays were measured, showing that current scales by the number of emitters in the array, suggesting both that the emitter tip radius distribution is quite uniform, and that the current limiter is preventing the destruction of sharper emitters. From the I-V characteristics, a new technique from extracting the tip radius statistics was developed, and the results of the method agree well with tip radii measured with SEM.in

Chapter 6

Lifetime Characterization of Silicon Field Emitter Arrays

6.1 Introduction

In this chapter, the lifetime and reliability of silicon field emitter arrays with integrated silicon nanowire current limiters and self-aligned gate apertures is explored. Lifetime and reliability are important metrics for some applications of electron sources, with requirements ranging from several minutes to years. To test the lifetime of our FEAs, we operate them with the Keithley 237 that biases the emitter in constant current mode, with the gate power supply set to 0V. The Keithley 237 has an internal feedback loop to maintain the current, and will automatically adjust the voltage should the I-V characteristics change. At regular intervals of every 1 or 5 hours, the measurement is paused and an I-V sweep is taken to monitor the health of the device. After the I-V sweep, the current is ramped up and lifetime test is continued.

During lifetime measurements, the anode was biased at a voltage of 1 kV. The power dissipated by our anode is limited to 1 W to prevent heating of the anode and outgassing, which would have the potential to cause back-ion bombardment and damage the emitter, thus the beam current is limited to 1 mA during lifetime characterization. We tested several different sized arrays, and have achieved up to 100 hours @ 100 A/cm^2, and over 10 days @ 1 mA and 0.1 A/cm^2. Only the 50 × 50 array at 100 A/cm^2 demonstrated irreversible failure when the test was concluded.

Array size	1000 × 10000	100 × 100	50 × 50	Single Emitter
Current (mA)	1	1	2.5	0.001
Current Density(A/cm^2)	0.1	10	100	100
Starting Voltage (V)	43	54.5	71	55
Lifetime (hours)	320	100	6	100
Failed?	n	n	y	n

Table 6.1: Devices Characterized for Lifetime

Table 6.1 Summarizes the lifetime results.

6.2 The S-K Chart

In this chapter, we examine the behavior of a single sample over time, and plot the slope and intercepts from linear fits of different FN-plots. These plots are referred to as Seppen-Katamuki plots or SK-plots for short. An example S-K plot is shown in Figure 6-1. The name Seppen-Katamuki comes from the Japanese words for slope and intercept, following the work and convention of Gotoh et al. [49, 48]. In SK-plots, a linear relationship between the slope and the intercept is often observed, however, this linear relationship cannot be explained assuming only a change in a single parameter, such as the radius or the work function. For a possible explanation using the simple FN-equation, a radial dependency of the emission area must be included [66, 47].

6.3 0.1 A/cm^2 Device

We have demonstrated 10 days of continuous operation of a 1000 × 1000 array (1M emitters) at an anode current of 1 mA (J = 100 mA/cm^2) (Fig. 6-3). During the course of these experiments, the operating voltage increased 4.8%. This voltage increase is likely indicative of charge injection and trapping at the surface of the oxide, resulting in de-biasing of the gate and a reduction in the electric field at the surface of the emitter. The plot of voltage vs. time in Fig. 6-3 shows spikes at regular intervals. These spikes occur each time the lifetime measurement is paused to collect the I-V characteristics.

The S-K chart of I-V characteristics taken during the course of the lifetime characterization

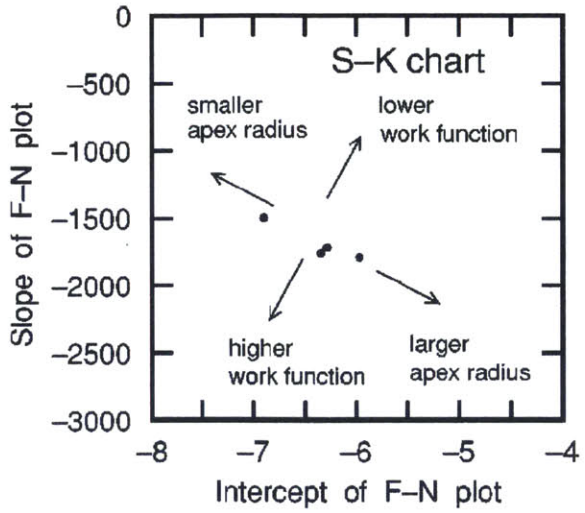


Figure 6-1: Example S-K chart. From [49], reproduced with permission. ©2001 AIP.

is shown in Figure 6-2. One I-V characteristic per day was used to generate the S-K. The S-K chart shows a clear trend towards larger apex radius and duller emitters over the course of the experiment. Although each time the lifetime test was paused for I-V characteristics the voltage required to maintain 0.1A/cm^2 was lower, and the voltage increases back to its previous value. It was initially thought that perhaps this voltage change suggests that it is possible that

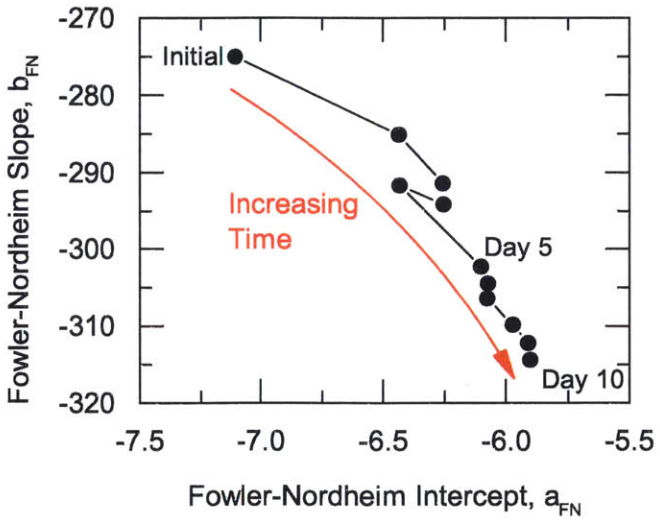


Figure 6-2: S-K Chart of the 0.1 A/cm^2 device.

the degradation may be due to charging of the gate oxide or the gate itself, and that the effect could be reversible, however, the S-K chart indicates that there is also a change in the effective structure of the tips.

6.4 10 A/cm^2 Device

The 100×100 array (10^4 emitters) was operated continuously for 100 hours at an anode current of 1 mA. The results are plotted in Figure 6-7. This current corresponds to a current density $J = 10$ A/cm^2. This device demonstrated a more severe voltage increase of 14.8% over the 100 hours to maintain 10 A/cm^2 current density. Figure 6-4 shows that the voltage shift is worse for the first 10 hours, and then increases linearly at a rate of 0.05 V/hour. Interestingly, by allowing the device to relax for 24 hours, the device recovered and the original I-V characteristics were restored as shown in Figure6-5.

From the I-V characteristics collected every 5 hours, we calculated the Fowler-Nordheim $\ln(a_{FN})$ and b_{FN} parameters and plotted $\ln(a_{FN})$ and b_{FN} to make the Seppen-Katamuki (S-K) chart in Figure6-6. From the S-K plot, we see that over time, the voltage required to achieve emission is increasing, consistent with either work function increasing or de-biasing due to charge trapping. Because the initial I-V characteristics were able to be recovered, it is more likely that de-biasing due to charging is the reason for the shift in characteristics.

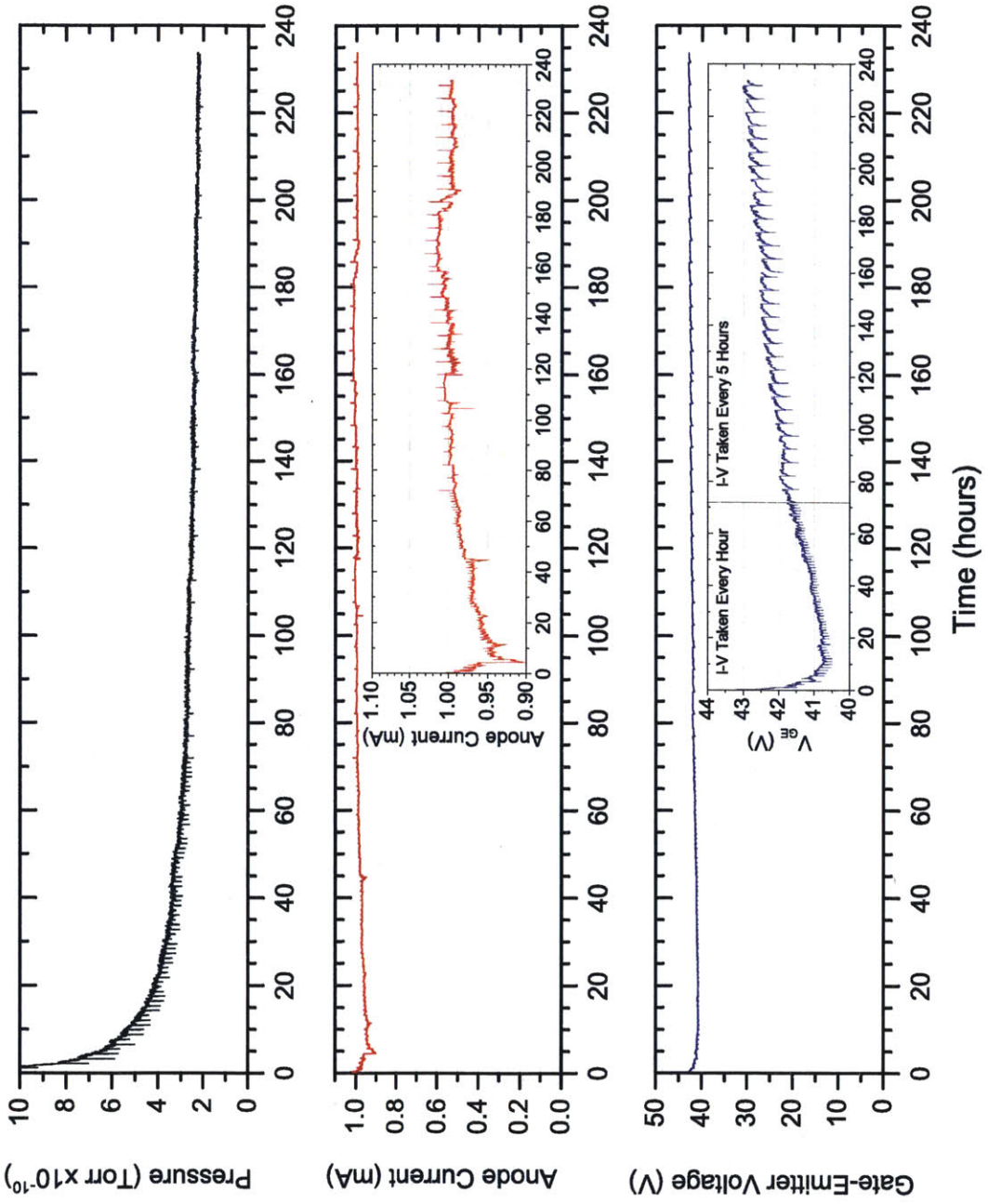


Figure 6-3: Lifetime summary - 1mA, 0.1 A/cm^2, 10 Days after initial 70 hour experiment - 310+ hours total.

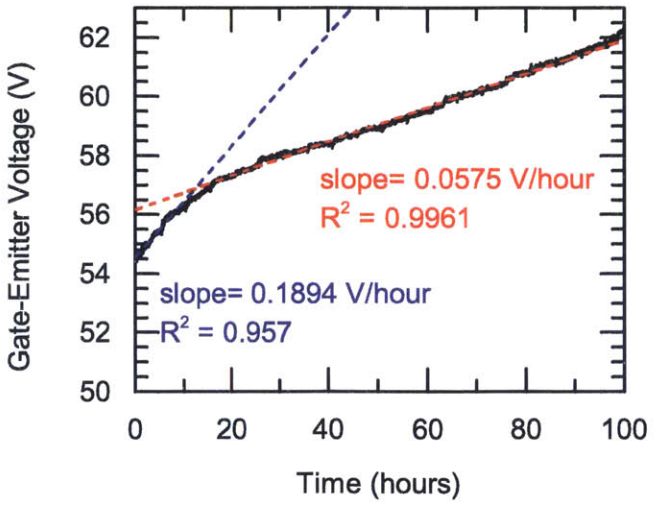


Figure 6-4: The operating voltage of the 100x100 array increased linearly with time.

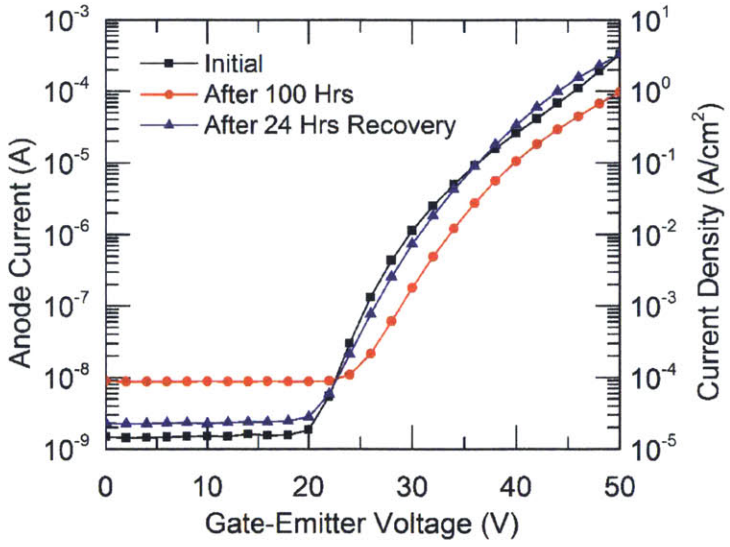


Figure 6-5: I-V characteristics showing the recovery of the 100x100 device.

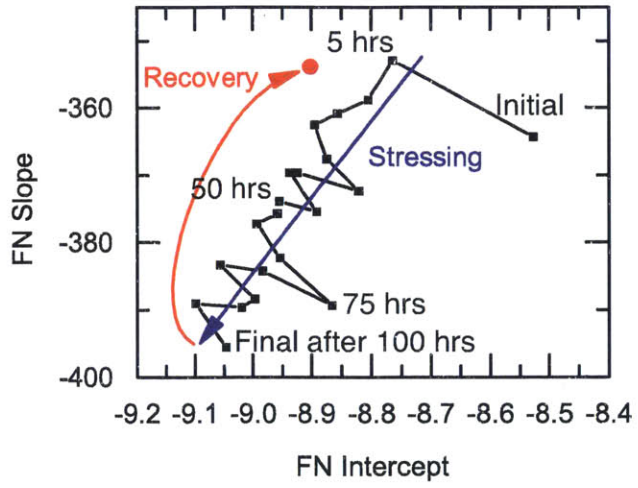


Figure 6-6: S-K chart of the FN characteristics showing the recovery of the 100x100 device.

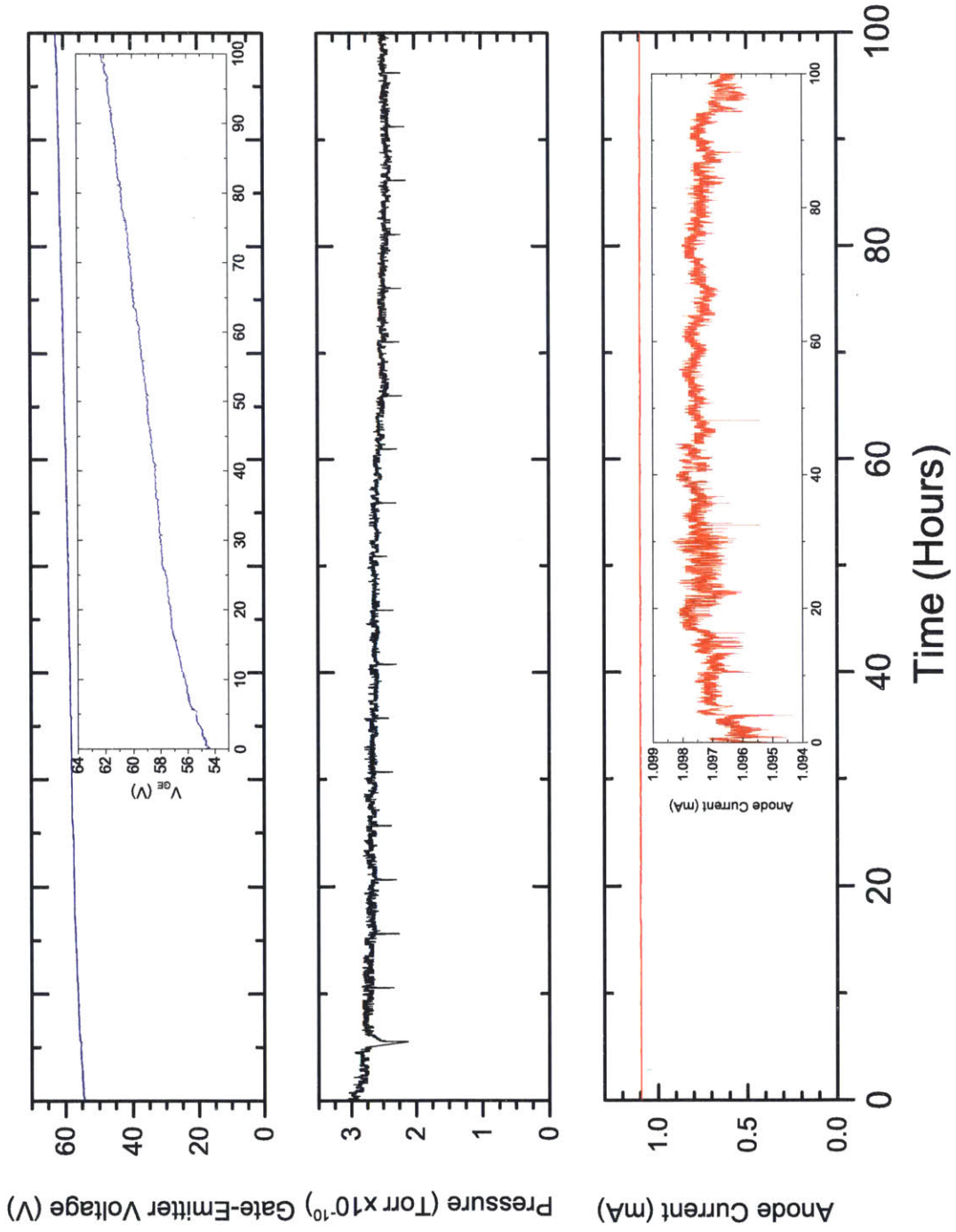


Figure 6-7: Lifetime summary - 100x100 array 1mA, 10 A/cm^2, 100 hours total.

6.5 100 A/cm^2 Devices

A 50x50 array was operated at an anode current of 2.5 mA (Current density, $J = 100$ A/cm^2) for a period of 5 hours before failing. Figure 6-10 shows a summary of the data taken during lifetime characterization. The voltage increased linearly over 6.5 hours of operation, beginning at 70 V until it reached 75 V when a failure occurred. This increase of 0.77 V/hour is more drastic than the voltage increase in the 10 A/cm ^{2} devices and is probably attributed to the higher operating voltage injecting more carriers into the dielectric film. Thus, this event is likely dielectric breakdown which resulted in outgassing which damaged the emitters. Due to the emitter damage, there was a sharp reduction in emission current, increasing the driving voltage to the compliance limit of 90 V. After 5.5 hours at 90 V and anode current between 1 and 1.5 mA, the device demonstrated irrecoverable failure. Both of these failures were accompanied by spikes in the pressure due to arcing and emitter outgassing.

A single emitter operating at an anode current of 1 μA (for an equivalent array current of 100 A/cm^2) maintained that current for over 100 hours with negligible degradation (Fig. 6-11). The 4.4% standard deviation in voltage is likely due to fluctuations in the state of the emitter surface [65], as shown by the S-K chart in Figure 6-9). There is no clear trend in the progression of the F-N characteristics of the 1x1 array, however, these scatter in this S-K characteristic is consistent

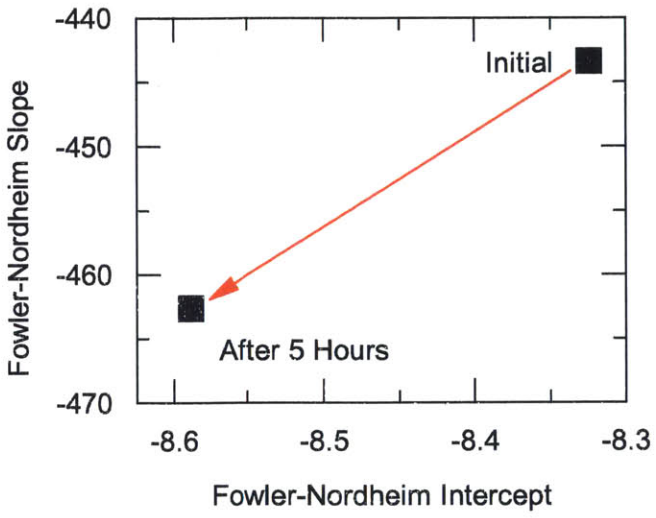


Figure 6-8: S-K chart of the 50x50 Array.

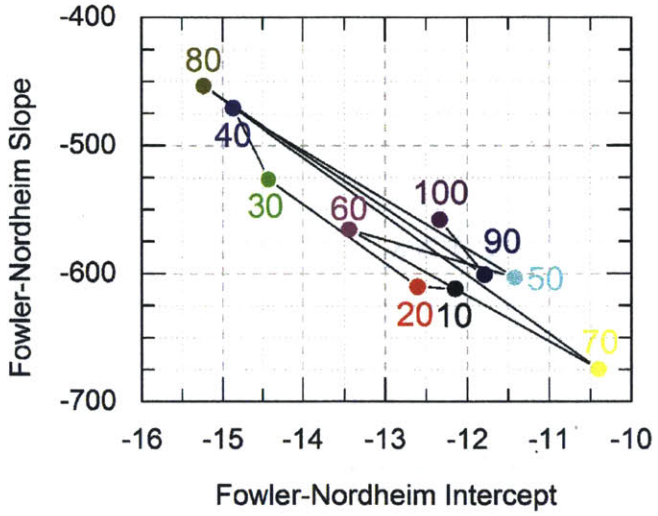


Figure 6-9: S-K Chart of the single emitter shows random walk over time.

with the S-K characteristic of a single Pt Spindt-type emitter demonstrated by Gotoh et al. [48].

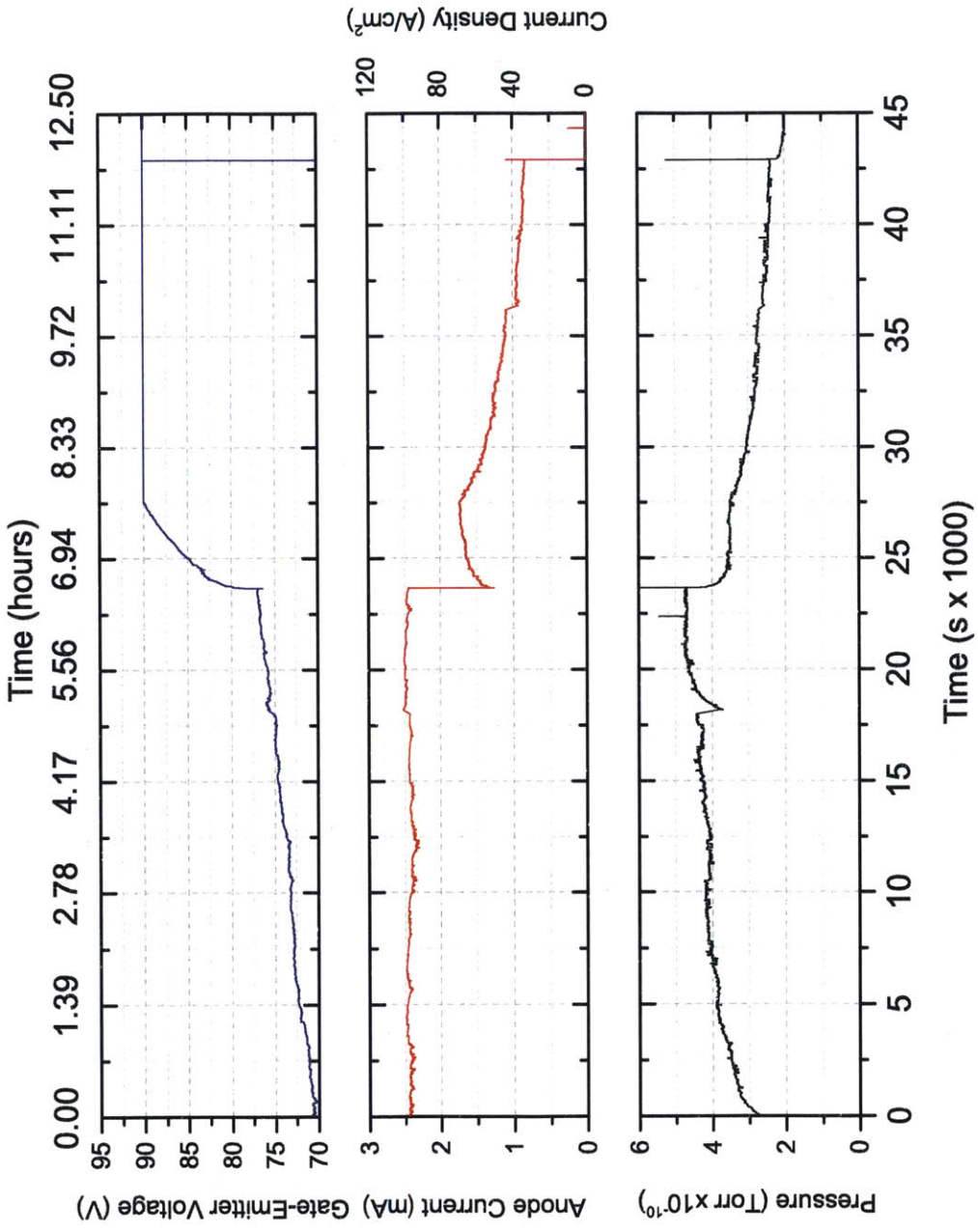


Figure 6-10: Lifetime summary - 50x50 array, 2.5 mA, 100 A/cm^2, 5 hours.

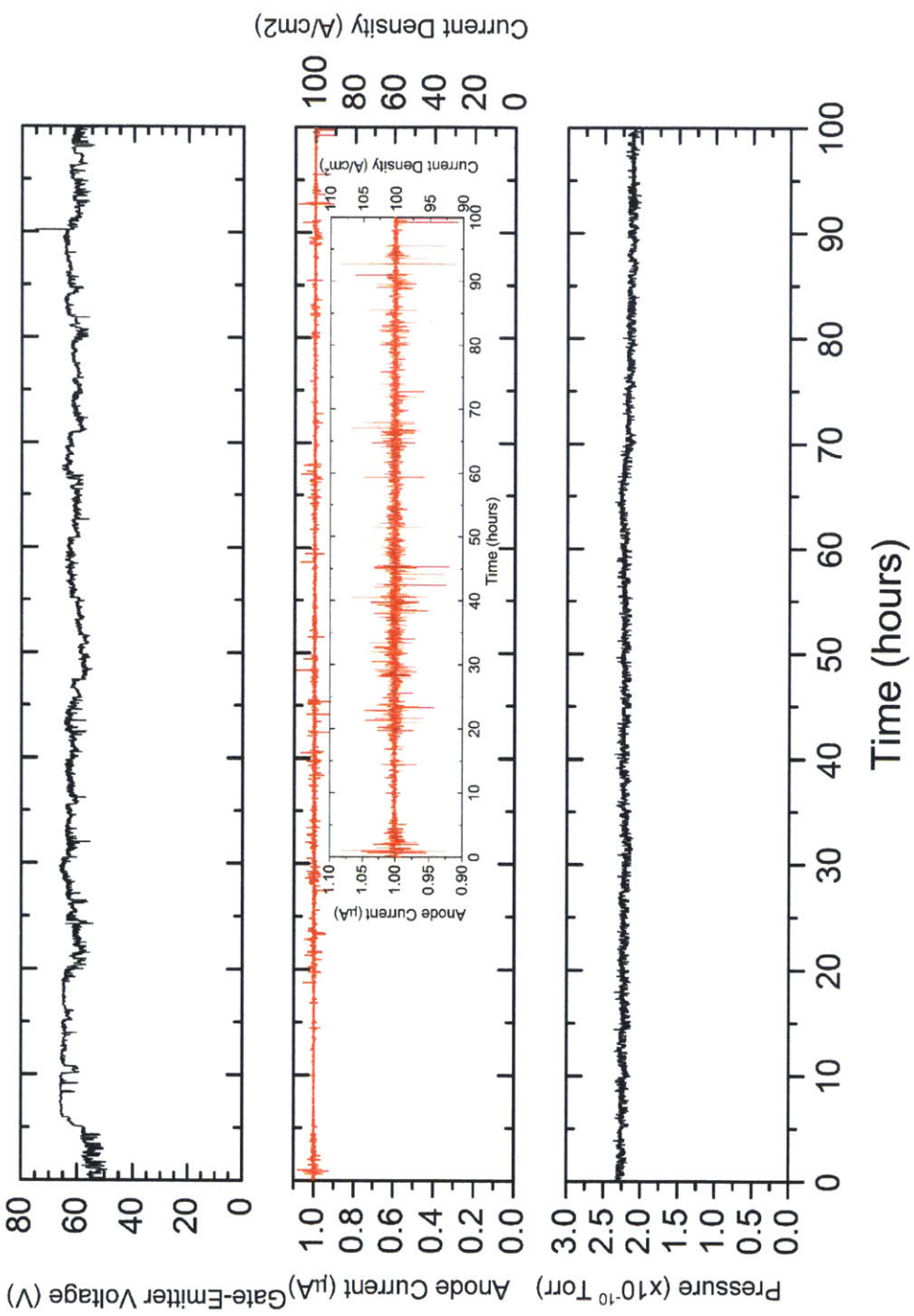


Figure 6-11: Lifetime summary - Single Emitter, 1μA, 100 A/cm^2, 100 hours total

6.6 Discussion

The variation of the S-K chart for single silicon emitters has been observed by several in the literature, however, a satisfactory explanation for the behavior still does not exist. As Persaud observes [101], because the distribution of the points along the line appears random, explaining the data is a challenge. The linear relation shown in the SK-plots seems to be orthogonal to a change in work function. Charbonnier *et al.* also investigated further possible explanations for the linear behavior in SK-plots, and considered whether nano-protrusions on top of a single emitter can be the cause. They found that a single protrusion cannot fit the experimental data but when several protrusions are used, good linear fits to the SK-plots can be obtained [20].

The body of literature that examines the long-term temporal stability of silicon field emitter cathodes is particularly sparse. Most papers that examined temporal stability, only presented short term stability such as those presented by Itoh and Hong[67, 62] and many others. Temple et al. demonstrated 25 hour operation of a 3255 tip array operating at ≈ 100 μA for a current of 30 nA/tip, or a current density of 0.03 A/cm^2 [121]. When we expand our literature search to carbon nanotube and metallic emitters, the picture improves somewhat, but perhaps the only comparable results in terms of lifetime at high current and high current density come from metal cathodes fabricated by SRI, with published reports of operating at 120 mA, 13 A/cm^2, and 2.4 μA/tip for several days [115].

Our results stand apart from the body of literature for silicon FEAs in terms of current density and lifetime. We can attribute this enhanced performance to our device architecture which prevents the failure mechanisms. Further work needs to be done to quantify these lifetime results and demonstrate how this devices will eventually degrade and fail. If these failure mechanisms could be well understood, we could develop approaches for performing accelerated lifetime testing such as is done with transistors.

6.7 Summary

Lifetime characterization demonstrated > 100 hours of operation for a single emitter operating at 1 μA (for an equivalent array current of 100 A/cm^2) and of > 100 hours for a 10 × 10 array operating at 10 A/cm^2. The emission characteristics degraded during this time however, by

allowing the device to relax, the original characteristics could be recovered. Only a very limited subset of devices and potential failure mechanisms have been explored and there is very rich set of issues that can be explored in this area. However, these limited results suggest that a potential degradation mechanism of the 100×100 array could be charging of the insulator between the gate and the emitter.

If the degradation mechanism is indeed dielectric charging, there are several ways that this effect could be mitigated. The first is that the dielectric could be made thicker. Another option is to coat the dielectric with a thin film of conductive, but highly resistive material. This film could prevent the accumulation of charge in the dielectric.

Chapter 7

Potential New Applications of FEAs

In this chapter, experiments in extending the operation of field emitter arrays to challenging applications where a pristine vacuum environment is not available are explored. Two of these experiments include operation in a high-pressure helium ambient, and the use of an electron-transparent graphene gate to isolate the emitters from the ambient environment.

7.1 Operation in Helium Ambient

An alternative to solid-state electronics for high-frequency power application are vacuum electronics; however, the need for vacuum chambers and vacuum pumps limits their utility, particularly in applications where size and weight and power (SWaP) are constrained. In this section, we report an approach that uses a gas channel medium approaching 1 atmosphere (500 Torr) to achieve simultaneously high breakdown field and high electron velocity, without the need for a pristine vacuum.

The operation of the field emitter device in helium can be thought of and modeled as a transistor where the channel medium is a gas rather than a solid state material, i.e. the "He channel transistor." In both a planar MOSFET and in the He channel transistor, a gate electrode modulates a barrier to control the injection of carriers into the channel. In a MOSFET, a thermionic process is used to inject the carriers into the channel. This is because the barrier between the source and the drain is < 1.1 eV, the bandgap of Si, and the gate is only several monolayers of an insulator away from the channel, often a high-$\varkappa$ dielectric. This description of MOSFET

operation is particularly obvious when thinking about the subthreshold region of operation. The thermionic injection of carriers from the source is what gives rise to subthreshold current, and the ideal subthreshold swing of 60 mV/dec.

In a gas channel, the barrier is much higher, closer to the work function of the material, $\approx 4-5$ eV, and it is a significant challenge to engineer materials with a work function low enough to make the injection of electrons into the channel via a thermionic process, as reducing the work function of the material thus increases the reactivity of the material (i.e. the definition of oxidation in a chemical sense is the loss of electrons). Hence, our approach is to inject electrons into a gas channel using the field emission arrays presented in Chapter 6, in which all the bias voltages (gate to emitter voltage for electron injection and anode to emitter voltage for electron extraction) are all below the first excited state energy of the gas to ensure that the only interactions with gas molecules is elastic scattering. Figure 7-1 shows a schematic of the

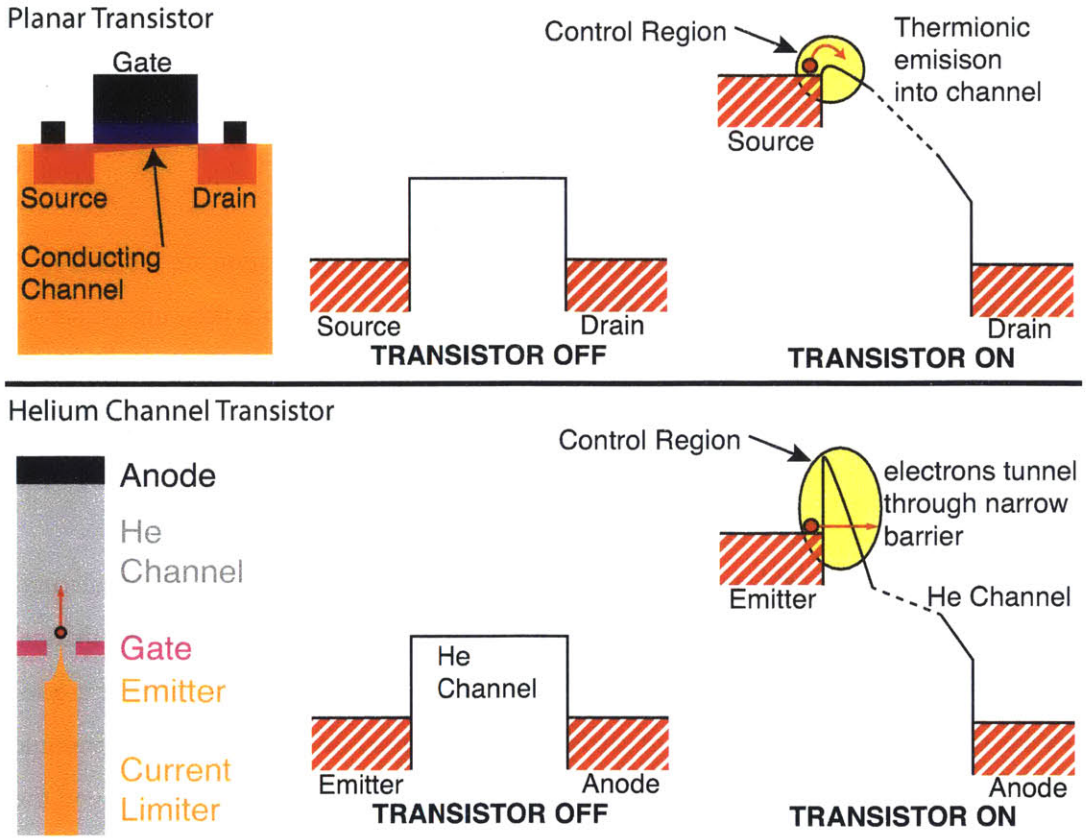


Figure 7-1: Comparision of the helium channel transistor to a planar MOSFET

transistors and their principles of operation, where applying a voltage between the gate and the emitter/source causes the injection of electrons into the channel.

For our channel, we chose helium for its low reactivity and high first ionization energy (≈ 24 eV) due to the tight binding of the valence electrons to the helium nucleus. Furthermore the excited states resulting from electron impact also have very high energy with the lowest having energy greater than 19.5 eV [2]. It is expected that electrons in a helium channel should have a higher mobility than in a solid-state device, as the density of gas molecules is much less than the density of atoms in a solid-state lattice.

To estimate the mobility of electrons in helium, we can use the relaxation time approximation [85], starting with the assumption that the electrons are traveling at a constant drift velocity v_{drift} with no elastic collisions (momentum relaxation), i.e.

$$qF - \frac{m^* v_{drift}}{\tau_m} = \frac{\partial (m^* v_{drift})}{\partial t} = 0 \tag{7.1}$$

where qF is the acceleration force from the electric field applied by the anode, and $m^* v_{drift}/\tau_m$ is the "drag force" from elastic scattering by the gas molecules. m^* is the electron mass, and τ_m is the momentum relaxation time, and is the time required to randomize the momentum. The momentum relaxation time can be thought of intuitively as the average time between scattering events. It is trivial to solve for the drift velocity under this steady state condition:

$$v_{drift} = \frac{q\tau_m}{m^*} F \tag{7.2}$$

and hence the mobility, μ is:

$$\mu = \frac{q\tau_m}{m^*} \tag{7.3}$$

To calculate the time between collisions, we assume that the helium atoms in the gas are evenly distributed with density N_{He}. If the electrons are traveling with velocity v_e i.e. $v_e = \sqrt{\frac{2qE}{m^*}}$, we can use elastic collision cross-section, σ to calculate to find the momentum relaxation rate:

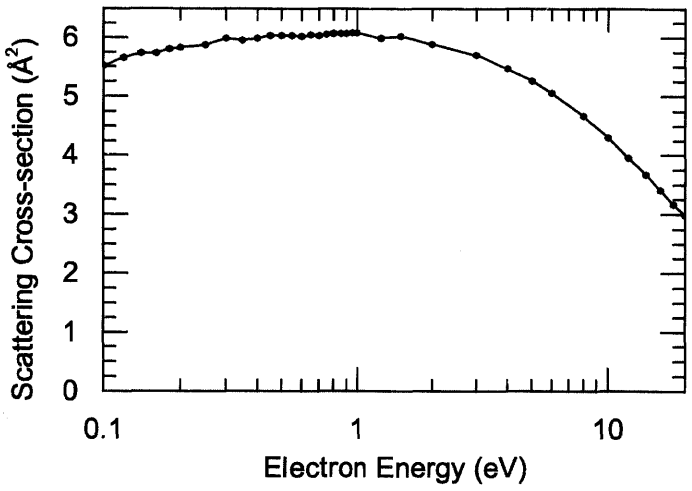


Figure 7-2: Scattering cross-section for low energy electrons in helium, after [16]

$$\frac{1}{\tau_m} = N_{He}\sigma\sqrt{\frac{2qE}{m^*}} \tag{7.4}$$

We use the average value of σ as tabulated in [16] for electrons with energy between 0.1 and 20 eV. Figure 7-2 shows that the scattering cross-section for electrons of energy 0 – 20 eV is relatively constant, with values varying between 3 and 6 $\times 10^{-16}$ cm^{-2}. Not visible in this data is the dip in elastic scattering present at the 19.366 eV due to the $1s^2s^2$ resonance. Note that σ is independent of pressure. The scattering rate, however, depends on the density of gas atoms/molecules in the channel, which obviously changes with pressure.

Thus, assuming the average energy of electrons is 20 eV and the scattering cross-section is 4 Å^2, the mobility of electrons in He at 1 atmosphere is

$$\boxed{\mu_{e,He} \approx 1700 \ \frac{\text{cm}^2}{\text{V}\cdot\text{s}}} \tag{7.5}$$

Surprisingly, this mobility comparable to the mobility numbers for Si and GaAs. A more rigorous calculation of this mobility would take into account the energy dependent nature of the momentum relaxation time and solve the Boltzmann transport equation assuming a uniform electric field, however, the numbers we chose should provide a pessimistic estimate.

Furthermore, we can perform an estimation of the saturation velocity of electrons assuming steady state inelastic scattering with energy transfer to the first excited state of helium under electron impact.

In that case:

$$\frac{\partial \langle E \rangle}{\partial t} = 0 = qFv_e - \nu_u E_{transfer} \tag{7.6}$$

Experiments to measure the differential inelastic cross-section of helium show that that threshold of excitation of the metastable 2^3S triplet state of He is 19.819 eV [4], and it could have a lifetime as long as 8000 s [58, 15]. Thus, from energy balance, the saturation velocity, v_{sat} is given by:

$$v_{sat} \approx \sqrt{\frac{E_{inelastic\ threshold}}{m^*}} \tag{7.7}$$

Using eq. 7.7 and assuming that the energy is 19.812 eV and the electron mass is the free electron mass, we obtain a saturation velocity of 1.8×10^8 cm/s, more than an order of magnitude higher than the saturation velocity numbers obtained in solid state electronics for silicon and gallium arsenide.

As shown in Figure 7-3, He has breakdown voltage of greater than 160 V at atmospheric pressure with a minimum at about 50 microns [3]. Thus, when the electrode is placed at a distance below the mean free path of He at STP, the breakdown voltage will be greater than 160 V. Hence, a way to increase the breakdown voltage is to reduce the spacing between the electrodes so that it is less than the mean free path of electrons in He. At 1 atmosphere, as shown in Figure 7-4, the mean free path is 9.5 μm.

Recall from Chapter 1 that the Johnson Figure-of-Merit is (J-FOM) is a figure of merit of power semiconductor devices, and defined as J-FOM = $\frac{E_{bd} v_{sat}}{2\pi}$. The above calculations imply that the J-FOM of a "helium channel transistor" could be greater than 10^{14} V/s, compared to the Si J-FOM of 4.5×10^{11} V/s or the GaN J-FOM of 9.5×10^{12} V/s [89]. Electronics with J-FOM of 10^{14} V/s without the need for high vacuum could result in a new architecture for devices that require high power amplification at high frequencies with small SWaP requirements.

To move towards a helium channel transistor, we have demonstrated the operation of low-

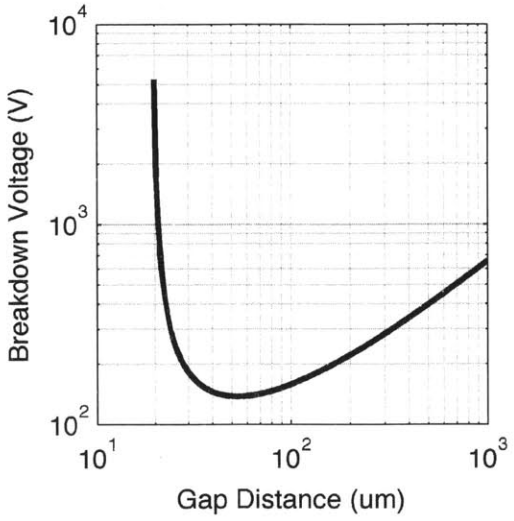


Figure 7-3: Paschen's curve for helium at 1 atmosphere

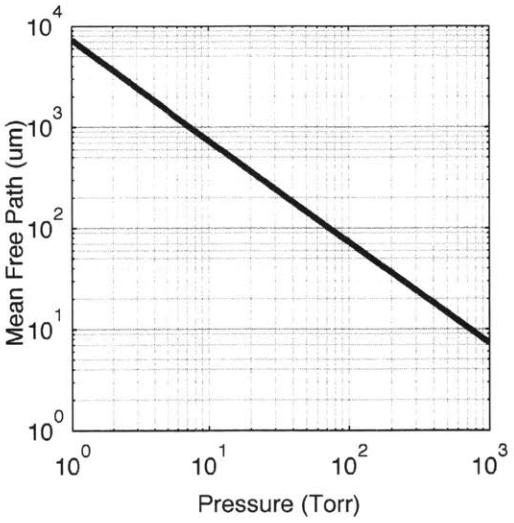


Figure 7-4: Mean free path of electrons in helium as a function of pressure

voltage field emission cathodes suitable for operation in helium. Figure 7-5 shows a 1000 × 10000 field emitter array that turns on at V_{GE} = 8.5 V and emits over 1 nA of current at V_{GE} < 10 V. This device shows a current swing > 2 orders of magnitude with ΔV_{GE} = 1.5 V.

Another cathode emitted over 1 nA of current at V_{GE} < 14 With the anode biased at 19 V, below the first ionization potential to prevent plasma formation and back-ion bombardment.

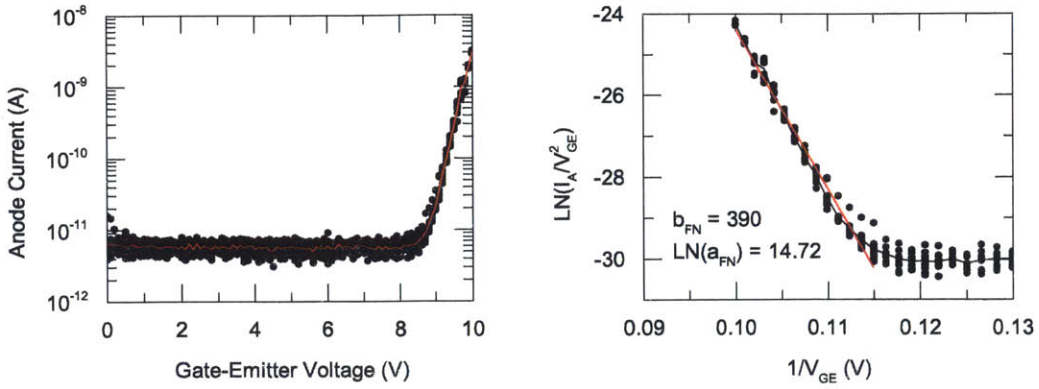


Figure 7-5: I-V and FN Characteristics of a 1000x1000 array that turns on at 8.5 V

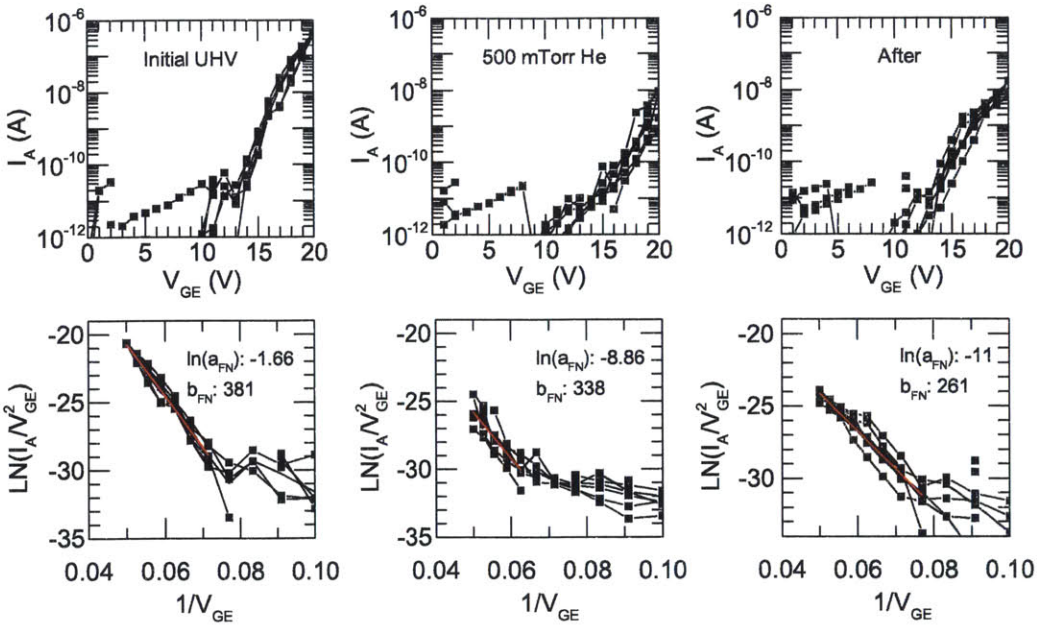


Figure 7-6: I-V (top) and FN (bottom) Characteristics of a 1000 × 1000 array operated in 100 mTorr of helium with V_A = 19 V

After characterizing this device in ultra-high-vacuum, the ion pump was isolated from the rest of the chamber and switched to the turbo pump. Helium was introduced into the vacuum chamber through a needle valve, with the flow rate moderated to set the pressure. I-V characteristics at various pressure have been recorded. Figure 7-6 shows the operation of the device in 100 mTorr of helium.

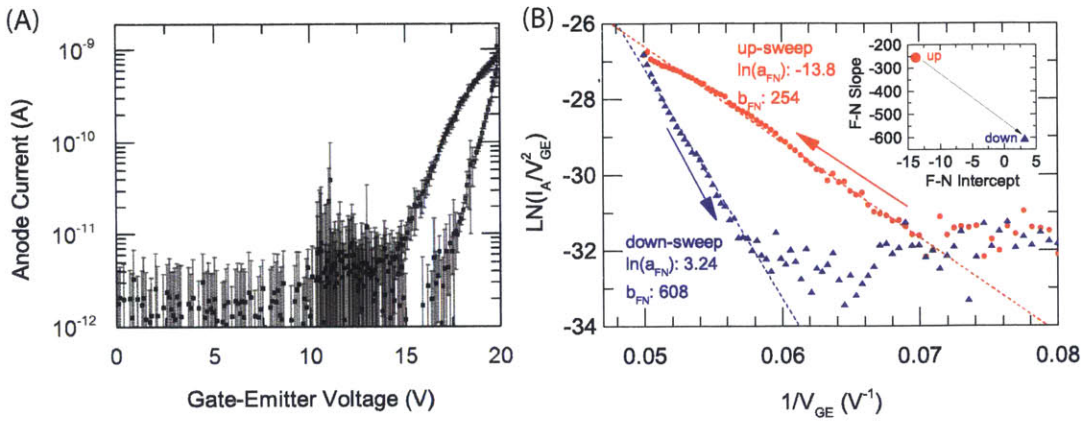


Figure 7-7: I-V (A) and FN (B) Characteristics of a 1000 × 1000 array operated in 500 Torr of helium with $V_A = 19$ V

At pressures greater than $\sim 10^{-7}$ Torr, the emission current begins to be suppressed when compared to the current obtained under UHV. We postulate that this suppression is due to adsorption of helium on the emitter surface, increasing the barrier for emission. Operation of the devices exposed to higher pressures in UHV can cause a subsequent increase in current, similar to the ionizers reported by Fomani et al. [41]. These cathodes have been operated in He pressures up to 500 Torr (Figure 7-7).

When operated in 500 Torr of He, the device characteristics demonstrated significant hysteresis, with the device "turn on" at $V_{GE} \simeq 15$ V and "turn off" at $V_{GE} \simeq 18$ V. This change is too large to be explained by a work function difference. If we assume that the change is only due to work function, the ratio of the work functions between the up sweep and down sweep would be a factor of 3. In addition, the S-K chart shown in the inset of Figure 7-7(B) suggests that the up-sweep characteristic exhibits an smaller effective tip radius compared with the down-sweeps, with β decreasing from 2×10^6 to 8.5×10^5. It appears that as we drive to higher voltages, the slop of the FN plot changes as the emission current from sharper emitters is quenched, and then only larger emitters contribute to the current in the down sweep. It is possible that higher emission current allows helium to better passivate emission sites, and that there are fewer atomic sites contributing to emission in the smaller emitters. We have not been able to ascertain the exact mechanism of this effect.

At higher pressures, the emission current was completely suppressed and there was no ob-

servable emission current at 1 atmosphere. The recovery of the I-V indicates that it is surface adsorption of gas molecules on the emitter surface that is limiting the emitter performance in high-pressure environments. This adsorption-desorption and its effect on emitter stability and lifetime is the primary challenge for this proposed class of devices, and may be mitigated by novel surface coatings or device architectures.

7.2 Electron-transparent Graphene-Gated FEAs

Based on challenge of gas adsorption on the emitter surface when operating the cathode in poor vacuum conditions, it is attractive to develop a method to isolate the cathode from the ambient atmosphere to ensure that the emitter tips remain in a pristine vacuum environment regardless of the ambient environment. One possible way to do this is to encapsulate the cathode, maintaining a pristine ultra-high-vacuum environment in which the emitters to operate. This structure requires an "electron window" that is transparent to electrons, but is impervious to gas molecules. In practice, this window can be a membrane that that is thin enough to allow electrons of a certain energy to be transmitted and thick enough to prevent the percolation of gas molecules in the opposite direction. There are applications for electron transparent windows in microscopy (particularly for the imaging of biological or other "wet" samples), lithography, x-ray sources, ion sources, electron-beam processing, and lasers.

Previous work on electron-transparent materials can be traced back to Lenard windows on cathode ray tubes [81] and Rutherford's experiments measuring the transmission and scattering of β particles by metal foils reported in 1911 [110]. Groups have utilized metal films such as aluminum-coated mylar [19]. Other groups have studied the use of layered organic/inorganic materials [43], silicon [24], and dielectric materials such as alumina [34], silicon nitride [52], and boron nitride [57].

All of these approaches share several drawbacks. First, these structures require a rigid support structure to maintain the integrity and prevent the membrane from tearing when a large vacuum differential is applied across the material. This support structure is necessarily thick, and reduces the transmission efficiency of the window. Next, the membranes range from tens of nanometers to several microns thick, requiring electrons to have energy of $> 1 - 10$ keV

to attain adequate transmission through the electron window. An ideal approach would use a low-Z material to reduce nuclear scattering of the electron beam and would be atomically thin, allowing transmission of electrons with energy < 100 eV.

Graphene, an allotrope of carbon which has garnered lots of publicity recently as an interesting electronic and mechanical material, can be as thin as a single atomic layer. It is a single sheet of graphite, i.e. carbon atoms arranged in an hexagonal pattern and has excellent mechanical properties and thermal properties. The atomic layer thickness ($\sim$ 5 Å)and the low atomic number of carbon ($Z = 6$) guarantees that the scattering cross-section will be small even for low energy electrons. Previous experimental work performing electron holography of graphene has shown that graphene can be transparent to electrons with energy > 100 eV, absorbing or backscattering $\approx$ 27% of the incoming electrons per layer at 66 eV [84]. Following [91], an effective attenuation length (l_{EAL})of graphene can be modeled theoretically or measured experimentally, and transmission can be modeled as an evanescent wave:

$$I_{transmitted} = I_0 \exp\left(-\frac{t}{l_{EAL}}\right) \tag{7.8}$$

At low energies, this effective attenuation length (l_{EAL}) has been shown to be on the order of 5 Å[77]. Graphene has also been previously demonstrated to work as an electron-transparent gate electrode for field emission devices, demonstrating transmission through the triode at $\sim 400V$ [82].

Important for this application is that an atomic layer of graphene has been shown to be impermeable to gas molecules as small as helium [17]. From the measured leak-rate data reported in [17], they have estimated the upper bound of the transmission probability of a helium atom impinging on a graphene membrane to be 10^{-11}. The pressure on either side of the membrane equilibrates in a time on the order of hours or days, and the authors speculate that that it is due to leakage at the graphene-SiO_2 interface, or diffusion of He through the SiO_2.

Given the tensile strength of graphene ($\sim$ 130 GPa [80]), it thus possible to have ultra high vacuum on one side of a atomic layer graphene membrane which has the electron emitter and on the other side have one atmosphere (or greater) of ambient gasses or others. Corroborating this, the results in [17] indicate 4.75 μm x 4.75 μm microchamber sealed with a single layer of

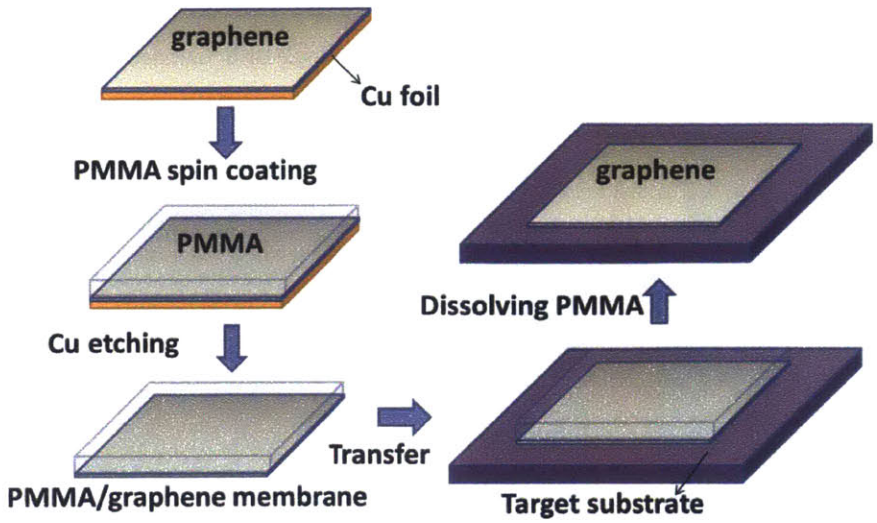


Figure 7-8: Process for transferring graphene from Cu catalyst foil to a device substrate using PMMA. Figure from [78].

graphene was able to withstand several atmospheres of pressure without failure. Above several atm, the failure mechanism was slipping of the graphene film, indicating that perhaps with a better clamping mechanism, an even larger pressure differential can be maintained.

We conducted experiments in which graphene was synthesized by hot-walled thermal chemical vapor deposition (CVD), as similarly reported in detail in [6] 5 sccm CH_4 (99.5% purity) was introduced to a 500-nm-thick physical vapor deposited Cu (and Ni) catalyst on 200 nm thermally oxidized Si, at 1000° C in an Ar: H_2 ballast (960 (99.9997%): 40 (99.9992%) sccm, at 25 mbar. Following the growth phase, samples were quenched using 2000 sccm N_2 (99.99%) to 250° C prior to system venting. The graphene was transferred to our field emitter as shown in Figure 7-8.

To transfer the graphene, PMMA (an electron-beam resist) was spun onto the graphene. By etching the copper catalyst layer in ferric chloride (i.e. PCB etchant), we transferred the graphene layer to the substrate, on top of the polysilicon gate of our our silicon field emitter. The PMMA was dissolved in acetone, leaving the graphene layer in intimate (and electrical) contact with our polysilicon gate. The final structure is shown in Fig 7-9. It should be noted that the tip is recessed from the top of the poly-silicon gate aperture by about 50 – 75 nm.

Figure 7-10 shows the I-V and F-N characteristics for a 100 × 100 array that has been

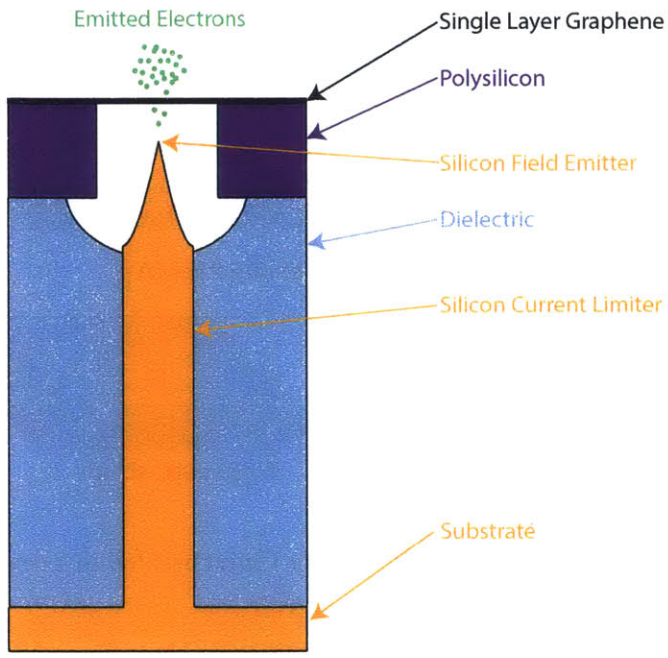


Figure 7-9: Structure of a field emitter device with an electron-transparent graphene gate.

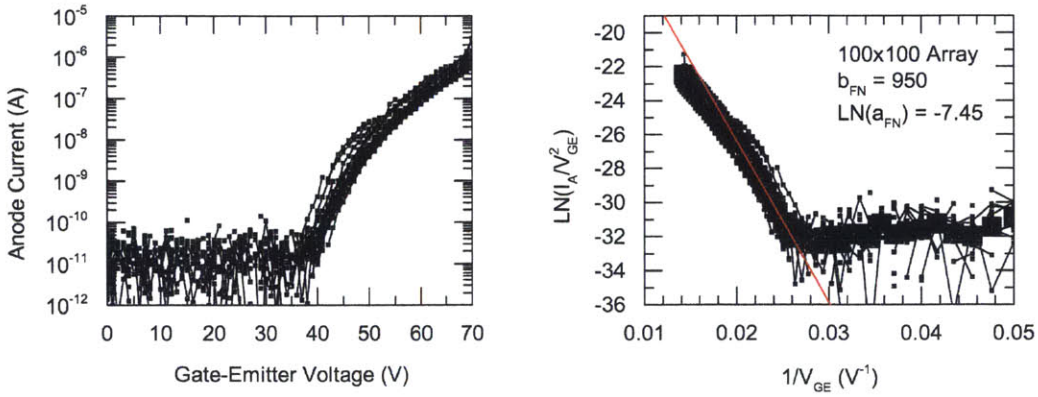


Figure 7-10: I-V (left) and FN Characteristics (right) of a 100 × 100 array with a graphene, electron transparent gate electrode.

covered with single layer graphene. These results demonstrate that the graphene gate layer is transparent to electrons emitted by the tip. The current shown in Fig. 7-10 is collected by the anode placed about 1 cm above the silicon field emitter array with graphene gate layer.

Generally, 100 × 100 arrays turn on at $V_{GE} < 20$ V. With graphene on the sample, the

turn-on voltage has shifted to $\approx$ 40 V. While the graphene could change the electrostatics, it appears that energy transmission through atomically thin graphene sheets is limited by the "bulk" (in as much as an atomically thin layer of material can have a bulk, at least) plasmon excitations in the graphene. In plasmon interactions, the electron excites charge density waves in the ensemble of loosely bound electrons within the graphene. Plasmon interactions are the dominant inelastic scattering mechanism for electrons in solids and typically involves energy losses of 10 to 30 eV [10] hence, the fact that our device seems to strongly turn on between 30 and 40 eV is consistent with plasmon excitation limiting transmission through the graphene at lower energies. This sharp turn on is hence likely more due to the transmission probability through the graphene rather than emission from the tip. The transmission probability manifests itself as an effective higher $b_{FN} \approx 1000\ \mathrm{V}^{-1}$ vs. 300-700 for typical 100 × 100 arrays.

The process is not yet perfected, and one of the consequences is that the gate leakage current is several orders of magnitude higher than the emission current. The high gate leakage current is probably due to the fact that the graphene is unpatterned, and thus shorts to the substrate in areas outside of the active device region (e.g. along the periphery of the substrate). A way to improve this process is to perform photolithography (electron-beam lithography) of the graphene after transferring to the target substrate. Because of the challenges inherent in performing 2-D transfers on large substrates, it may be better to transfer on small pieces, and *after* field emission characterization, to compare the performance of arrays before and after graphene transfer.

Graphene is readily etched in an oxygen plasma, allowing for an simple method for patterning the graphene after lithography to define the regions where the graphene will remain. A solvent clean can remove the resist after the O_2 plasma etch, which should not damage the graphene layer. It is also possible that subsequent annealing of the graphene after the transfer and solvent processing could improve the graphene, or alternative polymer scaffolds yield better quality graphene [127].

There are three potential approaches for using a graphene membrane to protect field emitter tips from their environment, summarized in Figure 7-11. The first, explored above, is where the graphene membrane is in intimate contact with the gate, so that each emitter tip is in its own microenvironment. The second architecture is where the graphene is used as a transparent anode, used to separate the entire cathode from the ambient environment. In this case, the

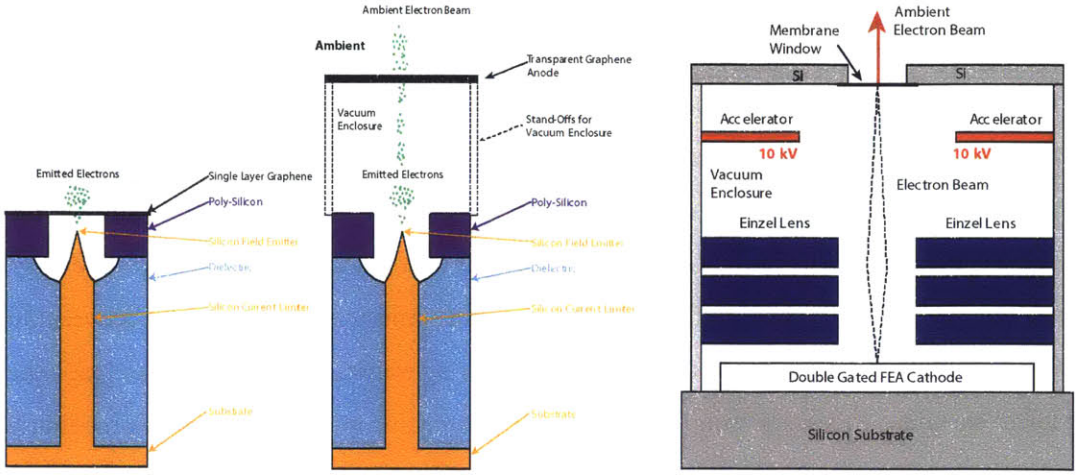


Figure 7-11: Three different approaches for using graphene to separate field emitter tips from there operating envrionment

graphene would be separated some distance from the emitter tips, and a larger volume would be maintained under UHV. The third — and most complex — architecture is similar to the transparent graphene anode, but includes beam-forming electrodes to form a focused or collimated electron beam in the ambient environment. Further work needs to be done to test the viability of each of the architectures.

7.3 Summary

In this chapter we reported experiments to explore extending the operation of field emitter arrays to challenging applications through the operation in high pressures and using an electron-transparent graphene gate. Both of these experiments show promise, however, more work needs to be done to make both technologies higher performance.

The ability to operate field emission cold cathodes in a variety of environments – not just ultra-high vacuum – has considerable implications. First, the cost, size, weight, and power of the systems that they are operated in could be significantly reduced because the need for large, inefficient vacuum pumps and vacuum chambers is lessened. We can also think about using

these cathodes for novel applications such as environmental SEM, food processing, and high throughput processing of semiconductor wafers.

To improve the emission characteristics of emitters in helium, surface coatings that prevent the adsorption of gasses on the emitter surface, while still allowing for electron emission. It could be that higher work function materials could limit the reactivity of the emitter surface and help prevent gas adsorption, however, the emission current will be reduced correspondingly. The operation should be extended to 1 atmosphere.

The electron-transparent graphene gate is exciting, as it is the lowest gate-emitter voltage reported for an electron-transparent triode. Several challenges, particularly the leakage current of the graphene gate needs to be addressed with careful processing. Sealing techniques for thin graphene membranes should be explored. Further analysis of the transmission of electrons through graphene, and experiments measuring the inelastic scattering mechanisms of electrons in graphene at low energies should be performed.

Chapter 8

Summary and Future Directions

8.1 Summary

This thesis reported the design, fabrication, modeling, and characterization of silicon field emitter arrays with self-aligned gates and integrated silicon nanowire current limiters. First, detailed modeling and characterization of the silicon nanowire current limiter was performed, including the role of surface states and recombination in determining the I-V characteristics of the current limiter, the thermal failure and breakdown of the nanowire, and 3-D effects of building arrays of silicon nanowires. This modeling suggests that for high current operation, the Si nanowire must have higher doping and/or larger radius than previously expected to prevent full-depletion due to the silicon interface. Ungated arrays with high-aspect-ratio current limiters verified that the silicon nanowire successfully limits the current to individual emitters, evidenced by the F-N plot deviating from its linear relationship.

Exploratory experiments in filling the voids between high-aspect-ratio silicon pillars revealed that it was a significant materials and processing challenge, and extensive work was done to develop a process for the void-free, filling of these gaps with a high quality dielectric material that could support the polysilicon gate. A process that used a combination of undoped polysilicon deposition and oxidation, as well as low-stress silicon nitride was presented, as well as a method that used selective etching of silicon nitride over silicon dioxide to form self-aligned gate apertures. These exploratory experiments yielded functional field emitter arrays, demonstrating a turn-on voltage $\approx$ 20 V and current saturation at 30 V, however, these devices suffered

from large gate-substrate leakage current. To address this leakage current, a new device architecture was proposed that incorporates a thick dielectric surrounding the array and probe pads outside the active array.

These new devices exhibit record current density for Si field emitter arrays, with sustained currents > 1 μA/tip and current densities > 150 A/cm^2 @ V_{GE} < 70 V. A number of different-sized arrays were measured, showing that current scales by the number of emitters in the array, suggesting both that the emitter tip radius distribution is quite uniform, and that the current limiter is preventing the destruction of sharper emitters. Lifetime characterization demonstrated > 100 hours of operation for a single emitter operating at 1 μA (for an equivalent array current of 100 A/cm^2) and of > 100 hours for a 10 × 10 array operating at 10 A/cm^2. The emission characteristics degraded during this time however, by allowing the device to relax, the original characteristics could be recovered.

The new devices are suitable for a variety of different applications where high performance cold cathodes are required, and we conducted some experiments to try to extend their operation to areas where high-vacuum is no-longer required. We demonstrated that graphene is an interesting material for impermeable, electron transparent windows, and that 40 eV electrons can penetrate graphene. We also demonstrated field emitter arrays that operate in up to 500 Torr of helium at voltages under 19 V, the first ionization potential of He.

8.2 Significant Contributions of This Work

Here is a brief list of the main contributions of this work:

1. Development and demonstration of an original process for the fabrication of silicon field emitter arrays with self-aligned gate and integrated silicon nanowire current limiters. As executed, this process produced current limited field emitter arrays with 100× higher packing density than arrays with current limiters previously reported, and are the first reported arrays to combine both individual current limiters and self-aligned gates.

2. Demonstration of field emitter arrays that demonstrate operation at > 150 A/cm^2 @ 1.5 mA of total current. These are the highest reported Si field emitter array current

densities and represent a > 10× improvement over state-of-the-art semiconductor field emitter arrays.

3. Demonstration of single tip field emission current from silicon FEAs > 2.5 μA.

4. Field emitter arrays that demonstrate > 100-hour lifetimes at a current density > 100A/cm^2, > 100-hour lifetimes at a current density > 10 A/cm^2, and > 320 hours at 0.1 A/cm^2, suggesting that the current limiter addresses failure mechanisms of field emitter arrays.

5. Development of a new technique to electrically estimate the tip radius statistics of field emitter arrays from a series of I-V characteristics.

6. Study of the beam divergence of silicon field emitter arrays with current limiters and self-aligned gate, demonstrating $\simeq 12°$ angular divergence.

7. Study of the electron transparency of graphene, demonstrating that at voltages as low as 40 V, there is transmission of electrons through graphene.

8. Demonstration of turn on-voltages as low as 8.5 V, enabling operation of Silicon field emitter arrays in up to 500 Torr of He. The low turn-on voltage makes it possible to keep all voltages lower than the first ionization potential of He and prevent ionization of the gas and arcing. Devices recovered when re-introduced to UHV and operated at low pressure, indicating surface absorption is causing emission current degradation at high pressures.

9. Developed an approach for self-consistent device simulations of a single emitter were developed that agree with measured I-V characteristics, using only doping density and tip radius as fitting parameters.

10. Explored the effect of operating the current limiters in an array instead of as isolated structures.

8.3 Future Directions

The gated field emitter arrays with integrated nanowires could be further optimized and improved. Perhaps first they should be improved by extending their operation to higher voltages. Typically devices exhibited failure between 60 and 75 V. A systematic study of the reliability of the dielectric, including time-dependent dielectric breakdown studies (TDDB) [87] should be performed, and this study used to optimize the structure and extend operation to higher voltages. An obvious first step is to reproduce the fabrication with careful optimization of the mesa etch to ensure that a sharp ridge does not form around the perimeter of the active area. Second, the dielectric surrounding the arrays could be thickened from 2 to 3 – 5 microns, increasing the breakdown voltage of the device. A better understanding of vacuum breakdown could also help extend field emitter operation to higher voltages without failures.

Now that the modeling of silicon nanowire current limiters has been improved — examining both individual nanowires and the effects of putting them in an array — the models should be coupled and turned into framework to model field emitter arrays with integrated current limiters. As part of this, measuring the interface trap density and recombination velocity of the SiNW surface should be performed. These experiments could include pump-probe techniques [53]. This modeling could better inform field emitter array designers and enable better optimized field emitter arrays with nanowire current limiters.

Of course, the arrays could be further scaled. Gated field emitter arrays with pitch as small as 200 nm have been reported [102]. If these field emitter arrays with Si nanowire current limiters were shrunk to 200-nm pitch, and the current/tip maintained at 1 μA, the current density could be increased to > 2000 A/cm^2. At this scale, it is likely that a more precision deposition technique such as atomic layer deposition will need to be employed to fill in the very small gaps between naowires. Assuming a nanowire diameter of $\sim$ 10nm, height of 1 μm and moderate D_{it}, it is likely that a high doping density of 10^{18} – 10^{19} cm^{-3} will need to be used to prevent the nanowire from being completely depleted.

These devices are approaching the performance required to make them an electron source for systems that require $\approx$ 100 A/cm^2 current density and $\approx$ 1 mA circuit current, such as the 0.85 THz amplifier reported in [8]. In order to make these arrays implementable in systems,

a packaging technology needs to be developed in order to create electrical contact to the gate and the substrate while allowing the beam to be injected into the input of the system.

A systematic study of the operation of cathodes in a high pressure, inert gas ambient, including potential surface coatings to prevent adsorbed gas molecules from quenching field emission should be performed. Electron transparency of graphene at low beam energy should be conducted, and work on developing architectures that separate the cathode from the ambient environment should be performed. The graphene-encapsulated cathode could enable a long-life electron impact ionizer in systems such as portable mass spectrometers. Work should be continued to explore the use of this device architecture in ionization experiments.

Appendix A

Table of Fundamental Physical Constants

Physical Constant	Symbol	Value	
		SI units	"microelectronic" units
Boltzmann constant	k_B	1.38×10^{-23} J/K	8.62×10^{-5} eV/K
Electron charge	q	1.60×10^{-19} C	$1.60 \times 10^{-19} = 1\ e$
Electron rest mass	m_0	9.11×10^{-31} kg	5.69×10^{-16} eV·s^2/cm^2
Planck constant	h	6.63×10^{-34} J·s	4.14×10^{-15} eV·s
	$\hbar$	1.05×10^{-34} J·s	6.58×10^{-16} eV·s
Speed of light in vacuum	c	3.00×10^{8} m/s	3.00×10^{10} cm/s
Permittivity of vacuum	ϵ_0	8.85×10^{-12} F/m	8.85×10^{-14} F/cm

Conversion between both systems:

$$1 \text{ eV} = 1.60 \times 10^{-19} \text{ J}$$

$$1 \text{ kg} = 6.24 \times 10^{14} \text{ eV} \cdot \text{s}^2/\text{cm}^2$$

From [119]

Appendix B

Table of Important Material Parameters of Si and GaAs at 300 K

Physical Parameter	Sym	Si Value	GaAs Value	units
lattice constant	a	0.543	0.565	nm
interatomic distance		0.235	0.245	nm
atomic density	N_a	5.0×10^{22}	4.4×10^{22}	g
density	d	2.33	5.32	$g \cdot cm^{-3}$
linear thermal expansion coefficient	α	2.59×10^{-6}	5.73×10^{-6}	K^{-1}
relative dielectric constant	ϵ_r	11.7	12.9	-
electron affinity	χ	4.04		eV
bandgap energy	E_g	1.124	1.422	eV
DOS electron effective mass	m^*_{de}	1.09 m_0	0.066 m_0	$eV \cdot s^2/cm^2$
DOS hole effective mass	m^*_{dh}	1.15 m_0	0.52 m_0	$eV \cdot s^2/cm^2$
conduction band effective DOS	N_c	2.86×10^{19}	4.21×10^{17}	cm^{-3}
valence band effective DOS	N_v	3.10×10^{19}	9.51×10^{18}	cm^{-3}
intrinsic carrier concentration	n_i	1.07×10^{10}	2.25×10^{6}	cm^{-3}
optical phonon energy	E_{opt}	0.063	0.035	eV
conductivity electron effective mass	m^*_{ce}	0.28 m_0	0.070 m_0	$eV \cdot s^2/cm^2$
conductivity hole effective mass	m^*_{de}	0.41 m_0	0.44 m_0	$eV \cdot s^2/cm^2$
phonon-limited electron mobility	μ_e	1430	8000	$cm^2/V \cdot s$
phonon-limited hole mobility	μ_h	480	320	$cm^2/V \cdot s$
electron saturation velocity	v_{esat}	1.0×10^7	$1.0\text{-}1.5 \times 10^7$	cm/s
hole saturation velocity	v_{hsat}	6.0×10^6		cm/s
optical G/R rate coefficient	r_{rad}	2.0×10^{-15}	7.2×10^{-10}	cm^3/s
electron-electron Auger coefficient	r_{eeh}	1.8×10^{-31}	1.8×10^{-31}	cm^6/s
hole-hole Auger coefficient	r_{ehh}	9.5×10^{-32}	4.0×10^{-30}	cm^6/s
impact ionization threshold energy	E_{ii}	1.12	1.72	eV

From [119]

Appendix C

Table of Important Material Parameters of SiO_2 and Si_3N_4 at 300 K

Physical Parameter	SiO_2 Value	Si_3N_4 Value	units
Structure	Amorphous	Amorphous	
Melting Point	≈ 1600	-	°C
Density	2.2	3.1	g/cm^3
Refractive Index	1.46	2.05	
Dielectric Constant	3.9	7.5	
Dielectric Strength	10^7	10^7	V/cm
Infrared Absorption Band	9.3	11.5 - 12.0	μm
Energy Gap	9	5	eV
Thermal Expansion	5×10^{-7}	-	$°C^{-1}$
Thermal Conductivity	0.014	-	$W\ cm^{-1}\ K^{-1}$
DC Resistivity			
@25 °C	$10^{14} - 10^{16}$	10^{14}	$\Omega \cdot$ cm
@500 °C	-	$\approx 2 \times 10^{13}$	$\Omega \cdot$ cm

Appendix D

Tunneling Through a Surface Barrier

The one-dimensional problem of an electron tunneling through a sharp triangular barrier can be readily solved by applying the Wentzel-Kramers-Brillouin (WKB) approximation to estimate the transmission probability, $T(E_x)$, through the barrier. For a single electron with energy in the direction of the barrier E_x, the one-dimensional time-independent Schrödinger equation is:

$$E_x\psi(x) = -\frac{\hbar^2}{2m}\frac{d^2}{dx^2}\psi(x) + V(x)\psi(x) \tag{D.1}$$

The tunneling distance, W, depends on both the energy of the electron as well as the applied electric field, F. In this section, the vacuum level at $x = 0$ is used as the energy reference.

$$W(E_x) = \frac{\phi + E_F - E_x}{qF} \tag{D.2}$$

First consider a particle incident traveling in the $+x$ direction incident on a barrier with wavefunction ψ_0. The particle inside of the barrier can be modeled as an evanescent wave and ψ inside of the barrier can be approximated as decaying as $\psi_0\, e^{-\alpha x}$. From this model, an expression for the fraction of the wave that is transmitted through the barrier, i.e. the transmission probability is obtained:

$$T(E_x) = \frac{\psi(W)}{\psi(0)} \approx e^{-\alpha W} \tag{D.3}$$

If instead of a square barrier, the barrier height varies as a function of position, the WKB approximation can be used to calculate the transmission probability. Essentially, the WKB approximation breaks up the barrier into a number of barriers win infinitesimal width and calculates the transmission through each. Mathematically, the WKB approximation states:

$$T(E_x) \approx e^{-2\int_{x_1}^{x_2} k(x)\,\mathrm{d}x} \tag{D.4}$$

where x_1 and x_2 are the classical turning points. The x-directed wave vector inside the classically forbidden region, $k(x)$, from the Shrödinger equation, is

$$k(x) = \sqrt{2m[V(x) - E_x]/\hbar^2} \tag{D.5}$$

From this equation, the relation between α and k can be found.

$$\alpha W = \int_{x_1}^{x_2} k(x)dx \tag{D.6}$$

Thus, the transmission probability $T(E_x)$ is:

$$T(E_x) \approx \exp\left[-2\int_{x_1}^{x_2} \sqrt{2m[V(x) - E_x]/\hbar^2}\, dx\right] \tag{D.7}$$

Where the potential difference $V(x) - E_x = -qFx + \phi + E_F - E_x$. From the potential $V(x) = -qFx$, the limits of the classically forbidden region are $0 \le x \le \frac{\phi + E_F - E_x}{qF}$, giving the limits of the integration. The resulting equation is:

$$T(E_x) \approx \exp\left[-2\int_0^W \sqrt{\frac{2m}{\hbar^2}}\sqrt{-qFx + \phi + E_F - E_x}\, dx\right] \tag{D.8}$$

The equation can be readily integrated to find:

$$T(E_x) \approx \exp\left[-\frac{4}{3}\sqrt{\frac{2m}{\hbar^2}}\frac{(\phi + E_F - E_x)^{3/2}}{qF}\right] \tag{D.9}$$

Alternatively, by noting that apart from the factor of $\sqrt{2m/\hbar}$, this area resembles a triangle with base $(\phi + E_F - E_x)/qF$ and height of $\sqrt{\phi + E_F - E_x}$, the same result can be obtained.

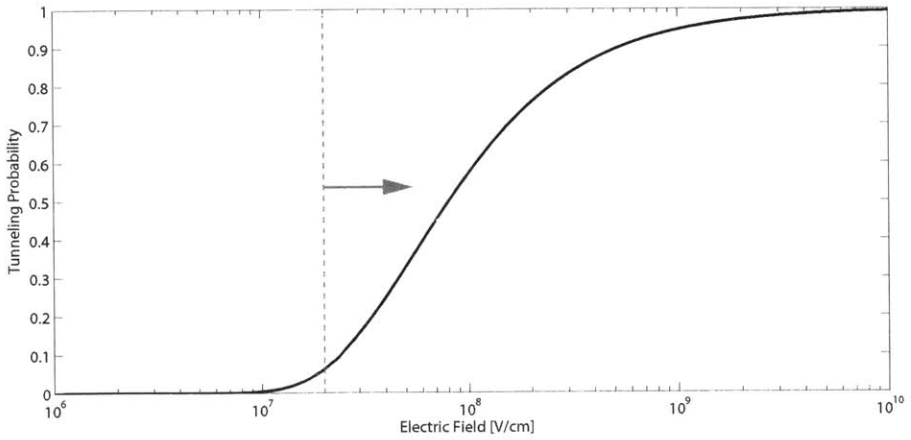


Figure D-1: Tunneling probability through a triangular barrier shows an exponential dependence on electric field. The electron has energy normal to the surface $E_x = E_F$. The dashed line shows where significant tunneling occurs, at 2 V/nm.

Because electrons inside the metal obey Fermi-Dirac statistics and the metal is assumed to be at 0 K, we can assume that there are no occupied states with energy greater than the Fermi energy. In addition, for energies below the Fermi energy, the transmission probability is vanishingly small because. Thus, we can make the approximation that $E_x \approx E_F$, simplifying equation D.9 to:

$$T(E_x) \approx \exp\left[-\frac{4}{3}\sqrt{\frac{2m}{\hbar^2}}\frac{\phi^{3/2}}{qF}\right] \tag{D.10}$$

From the above, the tunneling probability has exponential dependence on the applied electric field, as well as the barrier height. Assuming that the electron with x-directed energy E_x equal to the Fermi energy, the height of the barrier is the work function, ϕ, for n-type Si (~ 4.04 eV). A quick calculation can be performed to understand the field required for significant electron emission to occur. Figure D-1 shows the relationship of the tunneling probability to the electric field. There begins to be significant tunneling probability at roughly 2 V/nm (2×10^7 V/cm), indicating that the width of the potential barrier must be less than approximately 2 nm. This thickness is on the order of several electron wavelengths, which is the same result that is obtained for significant transmission of an evanescent wave.

A more careful calculation of the tunneling probability was performed by Fowler and Nord-

heim [42] with the result:

$$T = \frac{4\sqrt{E_x(\phi + E_F - E_x)}}{\phi + E_F} \exp\left[-\frac{4}{3}\sqrt{\frac{2m}{\hbar}}\frac{(\phi + E_F - E_x)^{3/2}}{qF}\right] \tag{D.11}$$

When considering many electrons, it is more appropriate to consider tunneling current density rather than tunneling probabilities. The tunneling current density can be expressed as the tunneling probability multiplied by the differential arrival rate (flux of electrons per unit energy) $N(E_x)$, called the supply function, and then integrated from $-\infty$ to E_F:

$$J_{tnl} = q\int_{-\infty}^{E_F} T(F,E)\cdot N(E)dE \tag{D.12}$$

where:

$$N(E_x) = \int v(E_x)g(E)f(E_x) \tag{D.13}$$

Here, $v(E_x)$ is the x-velocity of the electrons, $g(E)$ is the density of states (in p-space), and $f(E_x)$ is the Fermi-Dirac distribution. For a 3-D electron gas, the density of states will be:

$$g(E) = \frac{2}{h^3} d\,p_x\, d\,p_y\, d\,p_z \tag{D.14}$$

and the supply function integral is:

$$N(E_x) = \int_{p_y,p_z} \frac{p_x}{m^*}\cdot\frac{2}{h^3} d\,p_x\, d\,p_y\, d\,p_z \cdot \frac{1}{1+\exp(\frac{E_x - E_F}{k_B T})} \tag{D.15}$$

Performing a change of variables and evaluating this integral in cylindrical coordinates results in:

$$N(E_x) = \frac{4\pi m^* k_B T}{h^3}\ln\left(1 + e^{\frac{E_F - E_x}{k_B T}}\right) \tag{D.16}$$

Putting equations D.16 and D.11 together into D.12 yields an approximate expression for the tunneling current.

$$J_{tnl}(E_x)\,dE_x = \frac{16\pi m^* k_B T\sqrt{E_x(\phi+E_F-E_x)}}{h^3(\phi+E_F)}\ln\left(1+e^{\frac{E_F-E_x}{k_BT}}\right) \cdot \exp\left[-B\frac{(\phi+E_F-E_x)^{3/2}}{qF}\right]dE_x \tag{D.17}$$

where

$$B = \frac{8\pi\sqrt{2m^*}}{3h} = 6.87\times10^7\ \mathrm{cm}^{-1}\cdot\mathrm{eV}^{-1/2} \tag{D.18}$$

At moderate temperatures, the following simplification can be made in the calculation of the supply function:

$$k_BT\ln\left(1+e^{\frac{E_F-E_x}{k_BT}}\right) \cong \begin{cases} k_BTe^{\frac{E_F-E_x}{k_BT}}, & \text{for } E_x > E_F \quad \text{(D.19a)} \\ E_F-E_x, & \text{for } E_x \le E_F \quad \text{(D.19b)} \end{cases}$$

The simplification results in the tunneling current becoming:

$$J_{tnl}(E_x)\,dE_x = \frac{16\pi m^*(E_F-E_x)\sqrt{E_x(\phi+E_F-E_x)}}{h^3(\phi+E_F)}\cdot\exp\left[-B\frac{(\phi+E_F-Ex)^{3/2}}{qF}\right]dE_x \tag{D.20}$$

for $E_x > E_F$, and:

$$J_{tnl}(E_x)\,dE_x = \frac{16\pi m^* k_BT\sqrt{E_x(\phi+E_F-E_x)}e^{(E-E_F)/k_BT}}{h^3(\phi+E_F)}\cdot\exp\left[-B\frac{(\phi+E_F-Ex)^{3/2}}{qF}\right]dE_x \tag{D.21}$$

for $E_x \le E_F$. Because this function is peaking at $E_x = E_F$, the approximation that $E_F - E_x \ll \phi$ may be made. In addition, by using the approximation:

$$(B/F)(\phi + E_F - E_x)^{3/2} = (B/F)\phi^{3/2}(1 + (E_F - E_x)/\phi)^{3/2} \cong (B/F)\frac{3}{2}\phi^{1/2}(E_F - E_x) \quad \text{(D.22)}$$

which is valid because $(E_F - E_x)/\phi \ll 1$ and results in an integral of the form $-\int y e^{cy} dy$. The modified version of equation D.20 shown below:

$$J_{tnl} = q\frac{16\pi m^* \sqrt{\phi E_F}}{h^3(\phi + E_F)} \exp\left[-B\frac{\phi^{3/2}}{qF}\right] \int_{-\infty}^{E_F} \exp\left[\frac{3}{2}B\phi^{1/2}(E_F - E_x)/qF\right](E_F - E_x)dE_x \quad \text{(D.23)}$$

Performing the integration, we finally arrive at the Fowler-Nordheim model without image correction in 3-D:

$$J_{tnl} = q\frac{4}{3}\frac{16\pi m^* \sqrt{\phi/E_F}}{h^3 B^2(\phi + E_F)} F^2 \exp\left[-B\frac{\phi^{3/2}}{qF}\right] \quad \text{(D.24)}$$

Appendix E

Donor Ionization Efficiency in Silicon Nanowires

A surprising consequence of the nanowire geometry is that the assumption that all of the donor atoms inside the silicon are ionized is no longer valid, and must be checked. This is because in a bulk silicon lattice, the potential of the ionized impurity is screened by the charge carriers in silicon. In a nanowire, the volume surrounding the impurity is reduced, the medium that the impurity "sees" in no longer isotropic, and an image charge can form at the semiconductor/dielectric interface. The new ionization energy, with respect to the conduction band, can be found through the calculation given by Diarra et al. [29, 28], assuming that the donor atom is sitting directly in the center of the nanowire (the best case scenario):

$$E_I = E_I^0 + \frac{2}{\epsilon_{Si} r} \frac{\epsilon_{Si} - \epsilon_{ox}}{\epsilon_{Si} + \epsilon_{ox}} F(\epsilon_{Si}/\epsilon_{ox}) \tag{E.1}$$

where r is the nanowire radius (in nm), ϵ_{Si} and ϵ_{ox} are the relative dielectric constants of Si and SiO_2, respectively, E_I^0 is the ionization energy for the donor in eV ($E_I^0 = 45$ meV for phosphorus donor atoms in silicon) and $F(x)$ is the following function in (nm·eV):

$$F(x) = \frac{0.0949x^3 + 17.395x^2 + 175.739x + 200.674}{x^2 + 50.841x + 219.091} \tag{E.2}$$

From the modified ionization energy, we can then calculate the density of the ionized impurities as:

$$N_D^+ = \frac{N_D}{1 + g_d \exp\left(\frac{E_F - E_C - E_I}{kT}\right)} \tag{E.3}$$

Where g_d, the degeneracy of donor states, is equal to 2 from spin degeneracy [119]. In a silicon nanowire, we can assume that the charge neutrality condition still holds, i.e.

$$N_D^+(E_F) + p(E_F) - n(E_F) - N_A^-(E_F) = 0 \tag{E.4}$$

where:

$$\exp\left(\frac{E_F - E_C}{kT}\right) = \frac{n}{N_C} \tag{E.5}$$

and assuming that in the case of an n-doped semiconductor $N_A^-(E_F) \approx 0$ and $p(E_F) \approx 0$

$$\frac{N_D}{1 + 2\frac{n}{N_C}\exp\left(\frac{E_I}{kT}\right)} = n \tag{E.6}$$

where N_C is the effective density of states in the conduction band of Silicon, and is unchanged from the bulk value for nanowires larger than $\approx$ 10nm. Solving for n, and assuming that $n = N_D^+$, we find:

$$n = N_D^+ = \frac{N_c}{4} e^{-E_I/kT}\left(-1 + \sqrt{1 + 8\frac{N_D}{N_C}e^{E_I/kT}}\right) \tag{E.7}$$

Putting these all together, Figure E-1 shows the number of ionized donors and the ionization efficiency (N_D^+/N_D) for a silicon nanowire buried in SiO_2. From the graph, we can assume that the donors are completely ionized only until about a doping of 10^{17} for a 100-nm diameter nanowire. For the nanowire current limiters explored in this dissertation, this effect does not appear to be a relevant concern, however, for smaller nanowires or nanowires with higher doping densities, care should be taken to explore this phenomenon.

It is obvious from equation E.1 that the ratio of dielectric constants between the nanowire material (ϵ_{Si}) and the surrounding material (ϵ_{ox}) have a large impact on the incomplete ionization in the nanowire in that the higher the dielectric constant, the lower the effect. Diarra et al. have suggested that a way to mitigate this effect is to bury the silicon nanowire in a high-κ

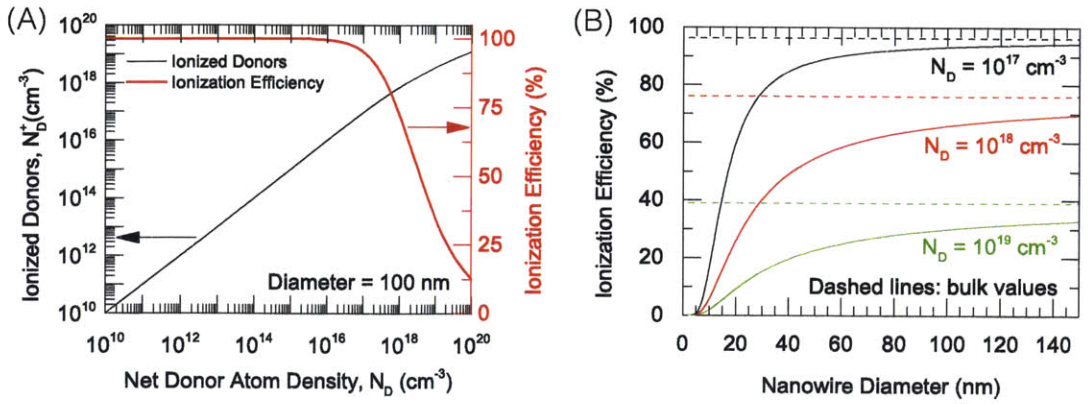


Figure E-1: (A) Ionization Efficiency and Ionized donor concentration vs. Net Doping for a 100-nm diameter silicon nanowire in oxide (B) Ionization efficiency for several different doping densities for vs. nanowire diameter

dielectric such as HfO_2. Another option is to use a metal gate around the nanowire to provide better electrostatics and screen the ionized impurities better.

Appendix F

Modeling of Surface States in Si Nanowire Current Limiters

Two non-idealities that effect the electrical characteristics and ultimate performance of silicon nanowires are the effect of the Si/SiO_2 interface along the surface of the nanowire and the incomplete donor ionization that results in silicon nanowires. This section will focus on the impact of interface states on silicon nanowire current limiter performance. For a discussion of incomplete donor ionization, please see Appendix E. As the size of the nanowire shrinks, the surface-to-volume ratio increases, and surface effects can become a limiting factor to performance. These surface effects need to be properly understood in order to build a model for the silicon nanowire as a current limiter. We will start by examining the effect of charges and traps at the Si/SiO_2 interface.

As in the case of a MOSFET, in a silicon nanowire device there are four types of charges or traps that can have an impact on device performance, using the framework developed by Deal [25]. These are [119]:

1. Interface traps of density D_{it}, and trapped charges Q_{it} which are located at the Si/SiO_2 interface with energy states within the silicon forbidden bandgap and can exchange charges with silicon in a short time. D_{it} has units $ev^{-1}cm^{-2}$. The interface charge density, Q_{it}, is determined by the Fermi level, so it can change with bias. Interface traps can arise from Si dangling bonds, broken Si-H bonds, impurities, excess oxygen, and excess

silicon (trivalent) silicon.

2. Fixed oxide charges, Q_f, which are located at or near the interface and are immobile under an applied electric field.

3. Oxide trapped charges, Q_o. These traps are distributed inside the oxide layer.

4. Mobile ionic charges, Q_m, such as sodium ions. These mobile within the oxide under bias-temperature stress conditions.

Figure F-1 shows a simple schematic depiction of the state of the Si/SiO_2 interface after a hydrogen anneal, such as a 5% H_2:N_2 forming gas anneal at $\sim$ 400 °C. This anneal allows hydrogen to diffuse through the dielectric layer and satisfy dangling bonds at the Si/SiO_2 interface. An anneal such as this can reduce the defects at this interface from about 10^{15} cm^{-2} to about 10^{10} cm^{-2}.

This dissertation will focus mainly on the effect of D_{it} and Q_{it} on device performance. Q_f is always positive and will act to accumulate the surface of the silicon nanowire, increasing

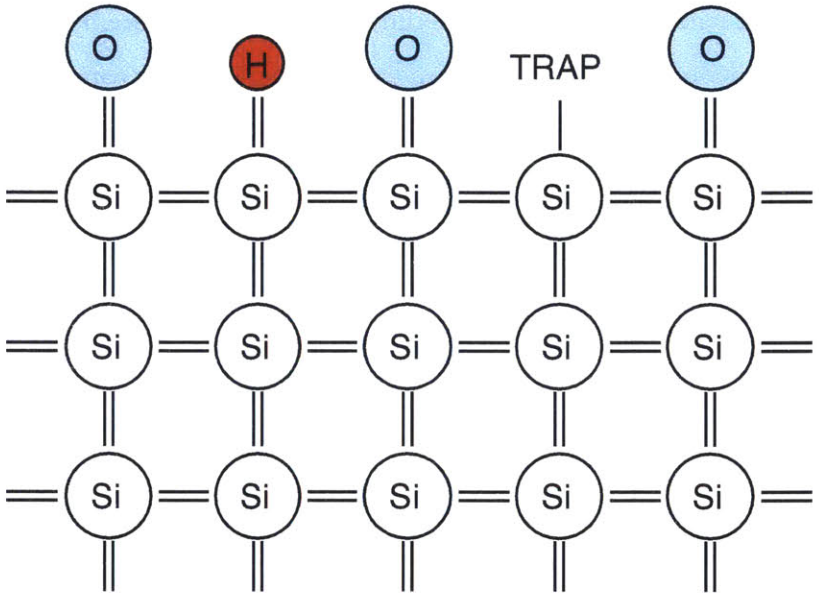


Figure F-1: Schematic depiction of the state of the Si/SiO_2 interface. Dangling bonds give rise to trap sites, which can accept electrons and give rise to interface charge. An anneal in hydrogen can passivate some of the surface traps sites by allowing hydrogen to bond at the dangling sites, reducing the interface trap density.

current at lower V_{DS}, which does not agree with our experimental results. Q_o and Q_m can deplete the silicon nanowire and impact performance, however through careful processing and the fact that we have a high quality thermal oxide on the surface of the nanowire, we expect that the density of Q_o and Q_m to be low. Further, their effect will be simply to shift the electrostatics of the device, whereas D_{it} can directly address the electrons in the silicon, and effect its density.

D_{it} is the density of interface trap states as function of E_s, i.e. $D_{it}(E_s)$, where E_s is an energy (in eV) in the bandgap measured with respect to the intrinsic Fermi level at the Si/SiO_2 interface. This is shown schematically in Figure F-2. Typically, D_{it} is relatively constant near the midgap, but it increases as the energy approaches both the conduction band and valence band edges. However, it is possible for deep traps to be present that manifest in the midgap, giving rise to a parabolic increase in the middle of the bandgap. Both cases are depicted in Figure F-2. These states can be integrated to find the interface charge, Q_{it} through:

$$Q_{it} = -q \int_{E_i}^{E_F} D_{it}(E_s) dE \tag{F.1}$$

While Figure F-2 shows the states in the center of the gap as being symmetric around midgap, this condition is not necessarily nor often the case. In general, interface traps are amphoteric, meaning that they can act as acceptor-like states or donor-like states depending on their position in the gap and the location of the Fermi energy, E_F. Assuming a Fermi level in the upper half of the bandgap, consistent with n-doped silicon, Then then trap sites between the Fermi energy and the middle of the bandgap are negatively charged, and the trap sites above the Fermi level are neutral.

For materials with a Fermi level below the middle of the bandgap, the converse is true. These site act like donors. That is, the trap sites below the Fermi level are neutral, and the trap sites between midgap and the Fermi level are positively charged. As the Fermi level can move with applied bias, the number of active trap sites can change with applied bias. This is shown schematically in Figure F-3.

Figure F-4 shows a schematic representation of the effect Q_{it} has on the silicon nanowire. The outer part of the nanowire is depleted, however there remains an inner quasi-neutral channel. This can be thought of as reducing the effective diameter of the nanowire so that is is less

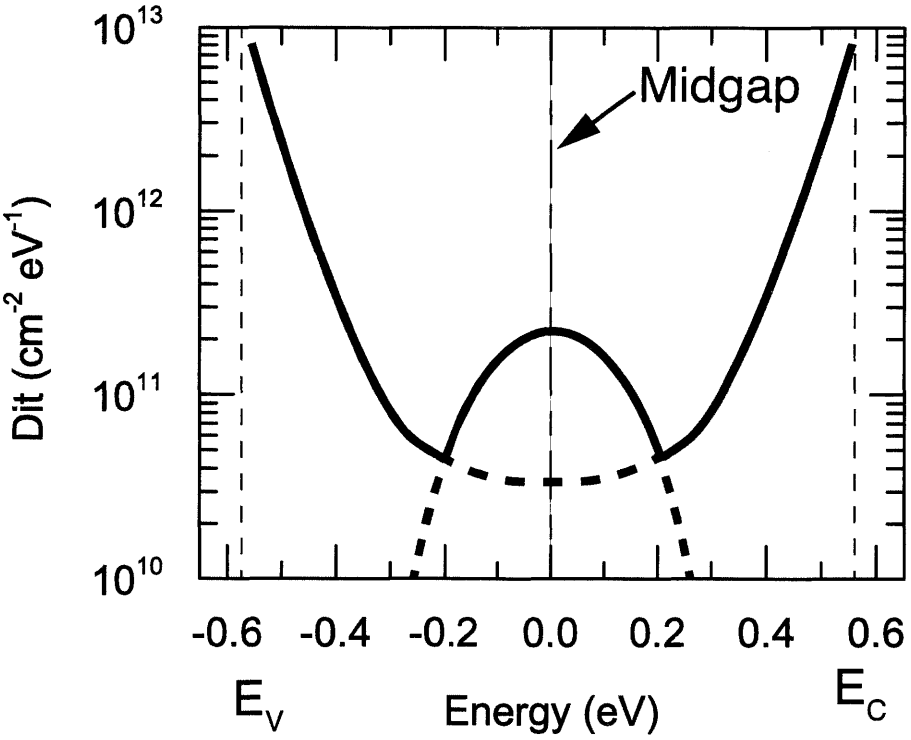


Figure F-2: Schematic diagram of a hypothetical silicon nanowire current limiter with interface charge density, Q_{IT}. The interface charge density has the effect of depleting the outer part of the silicon nanowire, even with no voltage applied. If Q_{IT} is too high relative to the doping density and the tip radius, the entire nanowire can be depleted with no potential applied.

than the actual nanowire diameter, *i.e.* $r_{eff} < r_{NW}$. Adapting the analyses presented in [111] and [113], we can model the effect of the interface states, compare it to device data, and put bounds on the density of interface states D_{it}. This work can be used to guide future work so that the doping and nanowire diameter can be chosen so that the nanowire is not fully depleted at $V_{DS} = 0$ V.

Assume that the nanowire is n-type, circular and radially symmetric with radius R. We make the Boltzmann approximation and assume that all of the donors are ionized. The space charge in the semiconductor is given by

$$\rho(r) = q(p(\Phi(r)) - n(\Phi(r)) + N_D) \tag{F.2}$$

where $\Phi(r)$ is the potential difference from the intrinsic Fermi level, E_i.

Thus:

$$n(\Phi) = n_0 \exp\left(\frac{q\Phi(r)}{kT}\right) \tag{F.3}$$

$$n(\Phi) = p_0 \exp\left(-\frac{q\Phi(r)}{kT}\right) \tag{F.4}$$

where n_0 and p_0 are the intrinsic carrier concentrations. We will use the abrupt depletion approximation, and assume that the silicon is depleted to some radius, r_d:

$$\rho(r) = \begin{cases} 0 & 0 \le r < r_d \\ qN_D & r_d \le r \le R \end{cases} \tag{F.5}$$

We can solve Poisson's equation in polar coordinates to find the potential, $\Phi(r)$.

$$\nabla^2\Phi(r) = \frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\Phi(r)}{\partial r}\right) = -\frac{\rho(r)}{\epsilon_s} \tag{F.6}$$

This differential equation can be solved through integration and the intermediate steps are shown in Appendix G. The final result is:

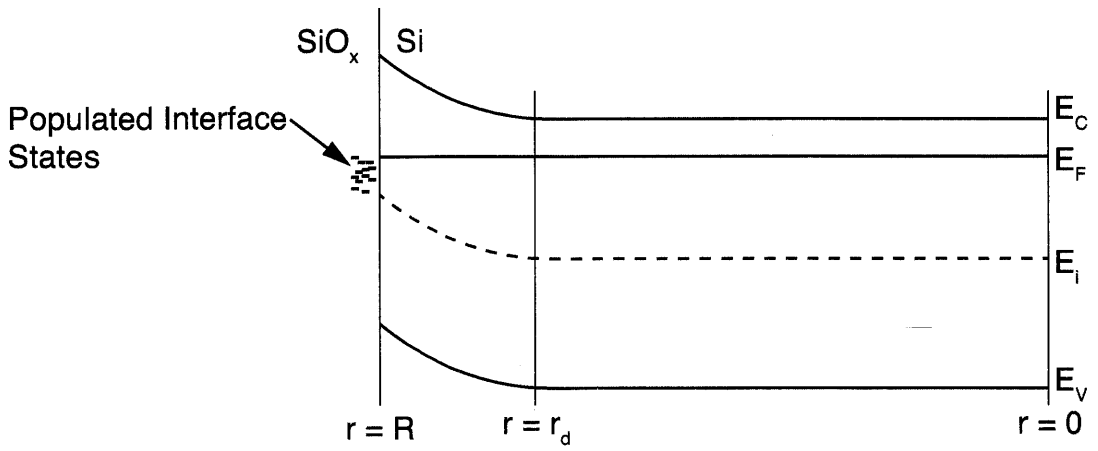


Figure F-3: Band diagram of an Si nanowire with no potential applied, showing the outer edge depleted due to interface states. If D_{it} is high enough and the doping low enough, the entire nanowire may be depleted.

$$\Phi(r) = \Phi_0 - \frac{qN_D}{4\epsilon_s}\left(r^2 - r_d^2 - 2r_d^2 \ln\left[\frac{r}{r_d}\right]\right) \tag{F.7}$$

where Φ_0 is the potential of the neutral semiconductor, i.e.

$$\Phi_0 = kT \ln\left(\frac{N_D}{n_i}\right) \tag{F.8}$$

The surface potential, Φ_s, is then

$$\Phi_s = \Phi(R) = \Phi_0 - \frac{qN_D}{4\epsilon_s}\left(R^2 - r_d^2 - 2r_d^2 \ln\left[\frac{R}{r_d}\right]\right) \tag{F.9}$$

This equation is transcendental and cannot be solved analytically. However, through the charge neutrality condition, there is a simple numerical way to find the depletion width, r_d.

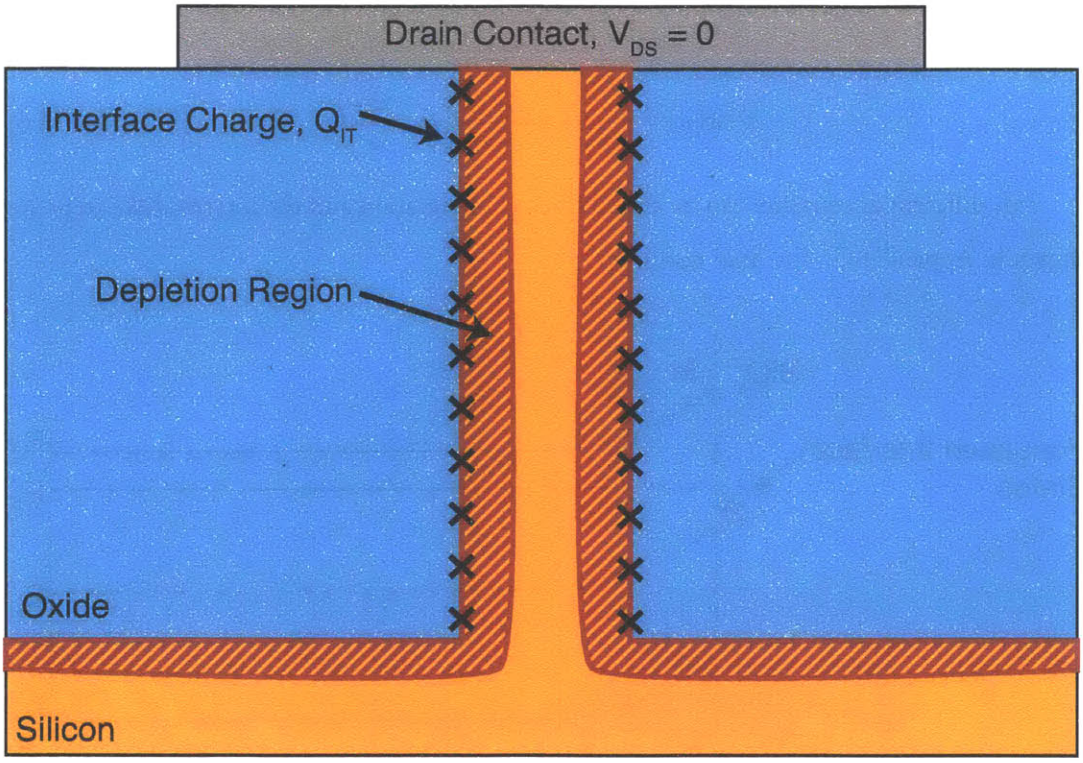


Figure F-4: Schematic diagram of a hypothetical silicon nanowire current limiter with interface charge density, Q_{it}. The interface charge density has the effect of depleting the outer part of the silicon nanowire, even with no voltage applied. If Q_{it} is too high relative to the doping density and the tip radius, the entire nanowire can be depleted with no potential applied.

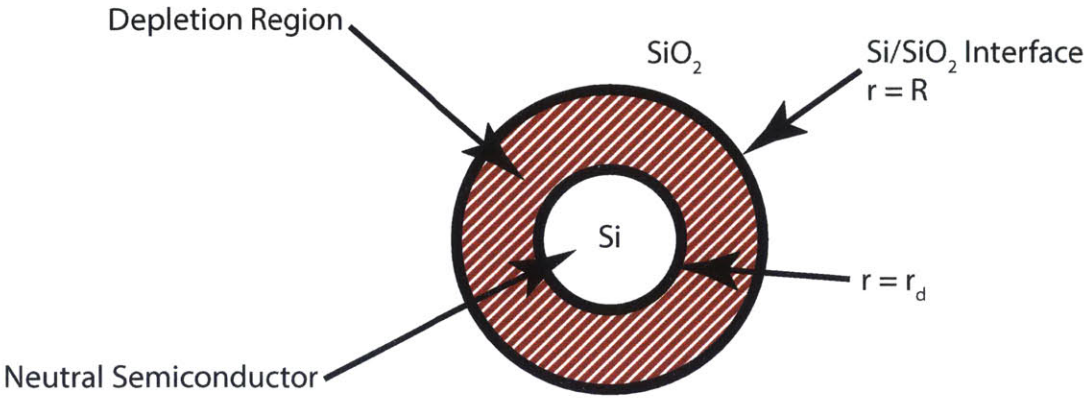


Figure F-5: The nanowire in cross section showing the depletion (shaded) and neutral regions due to interface states.

First, make the simplifying approximation that D_{it} is approximately constant over the region of interest, equation F.1 simplifies to:

$$Q_{it} = -q^2 D_{it} \Phi_s \tag{F.10}$$

In equilibrium, the system must remain charge neutral. This implies that the charge in the area of the depletion region must equal the charge on the surface for each radial slice of the semiconductor. That is

$$\pi q N_D (R^2 - r_d^2) + 2\pi R(Q_{it} + Q_f) = 0 \tag{F.11}$$

This model can be simply extended to handle cases where D_{it} is not constant in energy. To do this equation F.11 can be extended to use the general $Q_{it} = \int D_{it}(\Phi_s)$ and solved over the range $0 < r_d < R$. The rest of the discussion, however, will focus on the case of uniform D_{it}. Assuming uniform D_{it} and no fixed charge Q_f, solving eq. F.11 for Φ_s yields:

$$\Phi_s = \frac{N_D(R^2 - r_d^2)}{2qRD_{it}} \tag{F.12}$$

Equations F.9 and F.12 must be consistent, so they uniquely find the depletion width, r_d. In the case where the nanowire is fully depleted, i.e. $r_d \to 0$, they cannot be solved consistently and equation F.9 is greater than F.12 over the entire domain $0 \leq r_d \leq R$. In this case with

the nanowire fully depleted, the interface charge is fixed at the depletion charge because charge neutrality must hold. A consequence of this is that the surface potential is now fixed to:

$$\Phi_s = \frac{N_D R}{2qD_{it}} \tag{F.13}$$

The potential inside the nanowire must be calculated from this surface potential, as the potential in the center of the nanowire will change from Φ_0.

$$\Phi(r) = \Phi_s + \frac{qN_D}{4\epsilon_s} r^2 \tag{F.14}$$

Once the potential at each point in the nanowire is calculated, the electron concentration at each point along the nanowire radius is easily calculated using eq. F.3. To find the effective electron concentration, we need to find the average electron concentration by integrating along the radius:

$$\begin{aligned} n_{eff} &= \frac{1}{\pi R^2}\int_0^R n(\Phi) 2\pi r\, dr \\ &= \frac{2}{R^2}\int_0^R n_0 \exp\left(\frac{q\Phi(r)}{kT}\right) r\, dr \\ &= \begin{cases} n_0 \dfrac{4kT\epsilon_s e^{q\Phi_s/kT}}{N_D q^2 R^2}\left(1-\exp\left(-\dfrac{R^2 N_D q^2}{4kT\epsilon_s}\right)\right) & r_d = 0 \\ n_0 \exp\left(\dfrac{q\Phi_0}{kT}\right)\left[\dfrac{r_d^2}{R^2} + \dfrac{4\epsilon_s kT}{q^2 N_D R^2}\left(1-\exp\left(\dfrac{q^2 N_D (r_d^2 - R^2)}{4\epsilon_s kT}\right)\right)\right] & \text{otherwise} \end{cases} \end{aligned} \tag{F.15}$$

With an analytical expression for n_{eff}, we can begin to explore how the interface trap density effects the silicon nanowire and make some interesting estimates about the state of silicon nanowires for a variety of different doping densities, diameters, and interface trap density. Figure F-6(A) shows how n_{eff} varies with doping density for a 100-nm diameter NW for a variety of different interface trap densities. A characteristic of these plots is that there is a clear inflection point where the nanowire becomes fully depleted. If the doping is lower than this critical doping, the effective carrier concentration decreases exponentially, approaching n_0.

This model indicates that for a 100-nm diameter nanowire with a moderate interface trap density of 1×10^{11} cm^{-2}eV^{-1}, the doping density must be at least $\approx 10^{16}$ to prevent the nanowire

from being fully depleted while quasi-neutral. It is likely that the actual value of D_{it} of our SiNWs is at least 1×10^{11} cm^{-2}eV^{-1}. While high quality planar MOSFETs fabricated on Si with (100) orientation can achieve $D_{it} < 10^{10}$ cm^{-2}eV^{-1} [93]. Due to nano-scale surface roughness induced from the deep-reactive ion etching of the nanowire, and because of the circular cross-section of the nanowire, a superposition of all possible crystal orientations are oxidized. The data shown in Figure F-7(A) indicates that the configuration of the surface (Fig F-7(B)) can change the D_{it} by about an order of magnitude for the same processing conditions.

Figure F-6(B) demonstrates the potential effect of increasing the doping density of the SiNWs to $\approx 5 \times 10^{16}$ cm^{-3}, and shows the dependence on the nanowire diameter. The higher

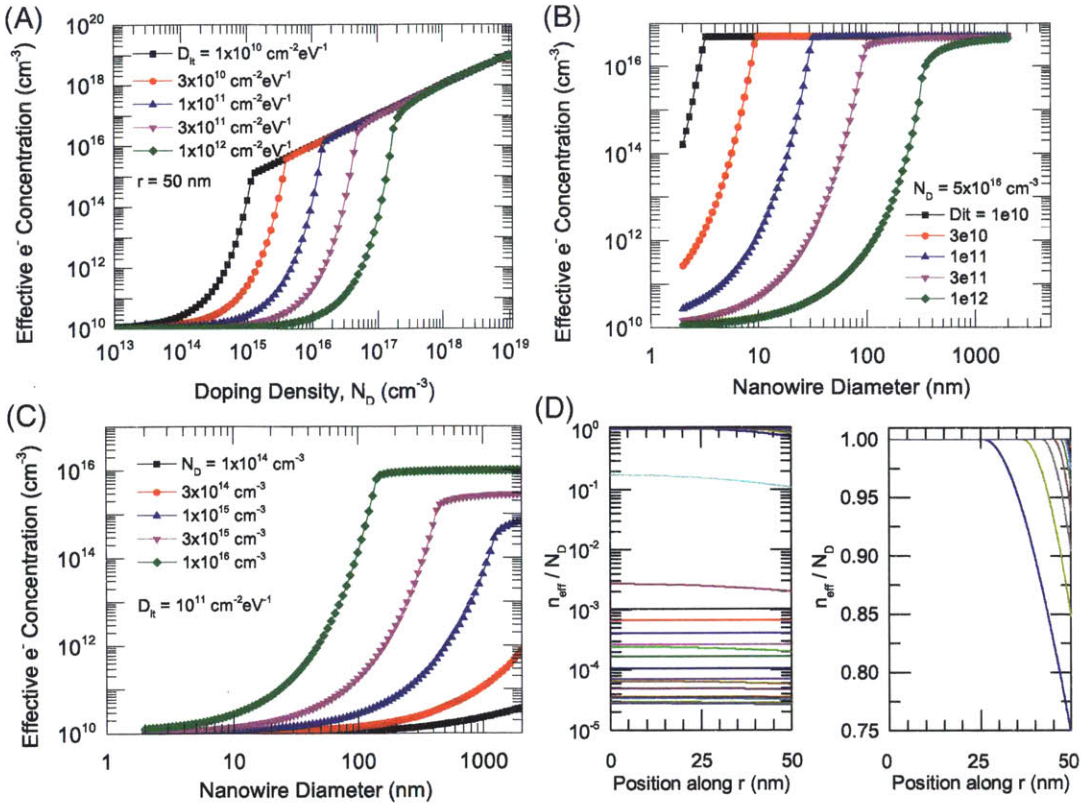


Figure F-6: Simulations of effective electron concentration (n_{eff}) for various nanowire geometries and electrical parameters. (A) n_{eff} vs. N_D for various values of D_{it}. The NW radius was fixed at 50 nm. (B) n_{eff} vs R for various values of D_{it}. The doping was fixed at 5×10^{15} cm^{-3}. (C) n_{eff} vs R for various doping concentrations. D_{it} was fixed at 10^{11} cm^{-3}. (D) semilog (left) and linear (right) plots of n/N_D as a function of position along the channel for the various doping densities in (A) for $D_{it} = 10^{11}$ cm^{-2} eV^{-1}.

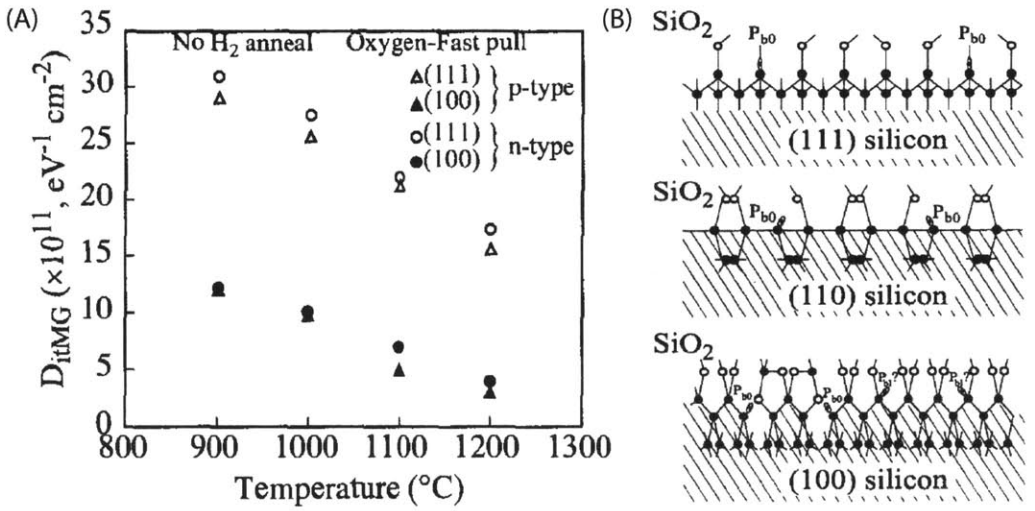


Figure F-7: (A) Midgap interface trap density vs dry oxidation temperature for p and n-type silicon, (100) and (111) orientations. Data are for samples with no hydrogen anneal. Figure reprinted with Permission from [108]. (B) Structure and location of traps (Pb centers) on oxidized silicon wafers of the three primary orientations. Figure reprinted with permission from [104].

doping allows a SiNW with a diameter of 100 nm to support a higher interface trap density of 3×10^{11} $cm^{-2}eV^{-1}$ without being fully depleted. Based on the simple analytical model presented earlier, a device with this geometry should reach ≈ 3.5 μA and begin to saturate at a drain-to-source voltage $V_{DS} < 1$ V with a mobility of 850 cm^2/Vs. As a consequence of the higher doping, the output conductance will be larger ($\approx$ 10 nS), however, the device should still allow for more uniform emission and prevent tip failure due to arcing and Joule heating.

For sufficiently low doping, increasing the nanowire diameter will be unable to compensate for the doping. Figure F-6(C) shows effective electron concentration vs. nanowire diameter for a moderate $D_{it} = 1 \times 10^{11}$ $cm^{-2}eV^{-1}$. These corroborate previous results obtained by Y. Niu and L.F. Velsáquez-García with 1 μ mdiameter, 100 μm tall silicon pillars. When fabricated with 50 Ω·cm ($N_D \approx 1 \times 10^{14}$ cm^{-3}) wafers, test devices had much lower current than was predicted based on results from devices fabricated from wafers with higher doping, analytical models without surface states, and numerical simulations.

To test this models ability to predict device performance, we attempted to fit the temperature dependence of linear conductance extracted from I-V characteristics of a single SiNW

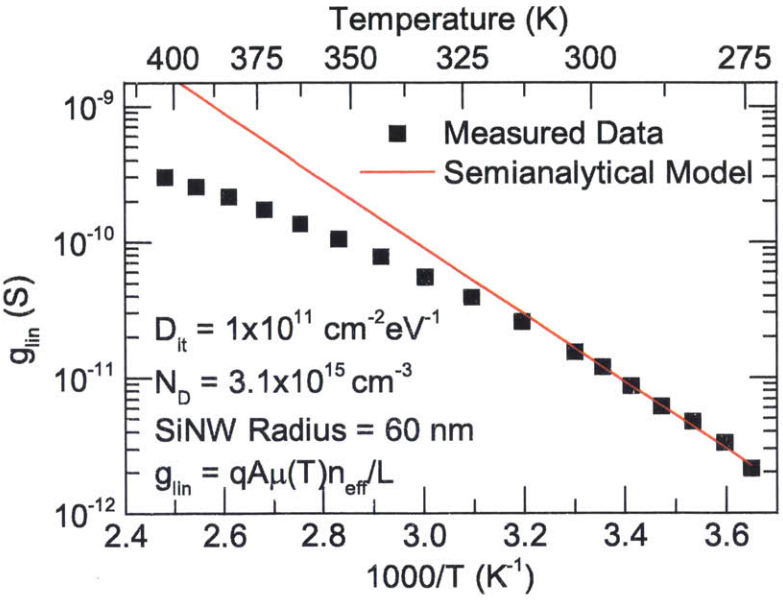


Figure F-8: Comparison of extracted linear conductance, g_{lin} with a numerical model of linear conductance for a SiNW current limiter.

current limiter (see Section 3.4) using this semi-analytical model of surface states. With reasonable values of doping density, nanowire radius, and mobility values from literature, we find a good agreement with the measured characteristics. The model diverges from the measured characteristics at high temperature, possibly due to surface recombination.

Appendix G

Solution of Poisson's equation in cylindrical coordinates for a partially depleted Si nanowire

We begin with Poisson's equation in cylindrical coordinates as given in equation F.6:

$$\nabla^2\Phi(r) = \frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\Phi(r)}{\partial r}\right) = -\frac{\rho(r)}{\epsilon_s} \tag{G.1}$$

We assume that the nanowire has radius R. Making the full depletion approximation, we assume that the nanowire has a depletion edge r_d. Thus, we find that the the space charge:

$$\rho(r) = \begin{cases} 0 & 0 \le r < r_d \\ qN_D & r_d \le r \le R \end{cases} \tag{G.2}$$

multiplying both sides by r, and integrating:

$$\int_0^r \frac{\partial}{\partial r}\left(r\frac{\partial\Phi}{\partial r}\right) = -\int_0^r r\frac{\rho(r)}{\epsilon} \tag{G.3}$$

yields:

$$\left(r\frac{\partial\Phi}{\partial r}\right)=\rho(r)\frac{r^2}{2\epsilon}\Big|_0^R=\begin{cases}-\frac{qN_D}{2\epsilon}\left(r^2-r_d^2\right) & r_d<r<R\\ 0 & r\le r_d\end{cases} \tag{G.4}$$

dividing both sides by r gives an expression for the electric field in the nanowire, $E(r)$:

$$\frac{\partial\Phi}{\partial r}=-E(r)=\begin{cases}-\frac{qN_D}{2\epsilon}\left(r-\frac{r_d^2}{r}\right) & r_d<r<R\\ 0 & 0\le r\le r_d\end{cases} \tag{G.5}$$

Integrating both sides gives the potential:

$$\int_0^r\frac{\partial\Phi}{\partial r}=-\frac{qN_D}{2\epsilon}\int_0^r\left(r-\frac{r_d^2}{r}\right) \tag{G.6}$$

Solving the integral with the boundary condition that at $r=0$, $\Phi(0)=\Phi_0$, the quasi-neutral potential, gives:

$$\Phi(r)=\begin{cases}\Phi_0-\frac{qN_D}{4\epsilon}\left(r^2-r_d^2\right)-2r_d^2\ln\left(\frac{r}{r_d}\right) & r_d<r<R\\ \Phi_0 & 0\le r\le r_d\end{cases} \tag{G.7}$$

and substituting $r=R$ gives an equation for the surface potential:

$$\Phi_s=\Phi(R)=\Phi_0-\frac{qN_D}{4\epsilon}\left(R^2-r_d^2\right)-2r_d^2\ln\left(\frac{R}{r_d}\right) \tag{G.8}$$

Appendix H

Process Flow for ungated field emitter arrays with nanowire current limiters

Step	Tool	Description	Processing Conditions / Recipe
0		Starting substrate: 150 mm <100> n-Si prime wafer	
1	RCA-ICL	RCA clean prior to tube run	
2	Tube-5C FieldOx	Grow 2500 Åoxide hardmask	1000 C wet oxidation
3	Coater6	HMDS/Coat wafers with 1.1μm Resist/Prebake	Resist: SPR700 / T1HMDS recipe
4	i-stepper	Expose dots	5 μm pitch 0.6 μm features Mask designed by Vivi Jayanty
5	Coater6	PEB / Develop / and PB resist	PUDDLE3
6	Metrology	Verify exposure in optical microscope and image dots in SEM	
7	AME5000	Etch oxide dots in $CF_4/CHF_3/Ar$ Chemistry 20% overetch	Baseline ox new, ~ 120 s
8	LAM490B	Rough etch of Si cones using SF_6/O_2 chemistry	Nitride etch, ~ 30 s
9	STS2	Etch nanowires using DRIE	FARDAD recipe, 14 minutes
10	Asher-TRL	Strip oxide and DRIE polymer. Must be done immediately after etching	>30 minutes in the barrel asher
11	Metrology	Measure pillar diameter and tip diameter in SEM	
12	RCA-TRL	RCA clean prior to tube run	

13	Tube-A2	Tip Sharpening / Diameter Shrinking	950 C wet oxidation. Target diameter of pillar: 100nm Target tip size, <10nm. Use process simulator to guide oxidation time
14	Oxetch-BOE	Strip oxide in BOE	etch rate 90 Å/s

Appendix I

Process Flow for gated field emitter arrays with nanowire current limiters

Step	Tool	Description	Processing Conditions/recipe
1	Alignment Marks		
1.1	RCA-ICL	Standard RCA Clean	10 min SC-1 (5:1:1 DI Water:H_2O_2:NH_3 at 80°C 1 min HF dip (50:1 DI water:HF) 15 min SC-2 (6:1:1 DI water:H_2O_2:HCl at 80°C SRD
1.2	Coater6	Coat with 1.1um resist	60s 90C prebake
1.3	Istepper	Photolithography LVL:0	Recipe: T1HMDS Alignment Marks Maskname FEAREV2 Exposure: 160 ms
1.4	Coater6	Develop	Dynamic puddle developer dispense 120C 30s Postbake Recipe: PUDDLE3
1.5	AME5000	STI Etch of alignment marks	40s in Ch.B recipe:STI:CH.B
1.6	LAM490B	Roughen surface to improve contrast	1:00 Black Si Etch
1.7	P10	MEASUREMENT STEP	Measure step height of alignment marks Using profilometer: Nominal result: 5000 A
1.8	ASHER-ICL	Remove resist	3 minutes
1.9	FLX	MEASUREMENT STEP	Measure Wafer bow Used for later stress compensation
2	Mesa Formation and planarization		
2.1	RCA-ICL	Standard RCA clean prior to oxidation	
2.2	Tube-5C	Hardmask oxidation - 2500 A	19 minutes and 4 seconds 1050 C wet oxidation
2.3	UV1280	MEASUREMENT STEP	Measure thickness in ellipsometer
2.4	Coater6	Coat with 1.1um resist	60s 90C prebake Recipe: T1HMDS

2.5	Istepper	Photolithography LVL:01	LVL Name: MESA Maskname FEAREV2 Exposure: 160 ms
2.6	Coater6	Develop	Dynamic puddle developer dispense 120C 30s Postbake Recipe: PUDDLE3
2.7	AME5000	Pattern Oxide etch mask	Recipe: Baseline-ox-new 90s / Endpoint
2.8	AME5000	Mesa Etch	Etch continues without breaking vacuum Recipe: Guerrera deep Si 575 sec Nominally 2um deep trench
2.9	ASHER-ICL	Remove resist	3 minutes
2.10 a b	 P10 SEM	MEASURMENT STEPS	 measure step heigh of trenches image sidewall of trenches
2.11	RCA-ICL	Standard RCA clean prior to oxidation	
2.12	Tube-5C	Liner oxidation - 500 A	1000C dry oxidation 1 hour
2.13	DCVD	PECVD deposition of oxide	2 microns to front and backside backside oxide is deposited to compensate stress
2.14	Tube-5D	Anneal oxide	950 C 1 Hr O2 Anneal
2.15	DCVD	PECVD deposition of oxide	3 microns to front and backside (5um total) backside oxide is deposited to compensate stress
2.16	Tube-5D	Anneal oxide 950 C 1 Hr O2 Anneal	
2.17	UV1280	MEASUREMENT STEP	measure oxide thickness and uniformity
2.18	Outside	CMP of oxide	Sent wafers to vendor: Entrepix Instructions to polish oxide and stop on Si Use 2 wafer as pilot wafers
2.19	premetal-piranha	post-cmp clean	2x10minutes in 3:1 H2SO4:H2O2

		required to return to processing	15s dip in 50:1 DI H2O:HF
2.20		MEASUREMENT STEPS	
a	P10		Measure step height of oxide/Si to see overetch
b	UV1280		Measure thickness of oxide
c	SEM		Image in SEM for particles
3	Emitter and Si Nanowire Formation		
3.1	RCA-ICL	Standard RCA Clean	
3.2	Tube-5B	Grow 500 ALiner oxide	1000C dry oxidation 1 hr
3.3	DCVD	Deposit Hardmask	250nm DCVD oxide
3.4	Tube-5D	Hardmask densification	1 hour 950 C under O2
3.5	Coater6	Coat front of wafer with photoresist	Hardbake 120C 60s Recipe: Protect
3.6	FLX	MEASUREMENT STEP	Measure wafer bow
3.7	OxEtch-BOE	Timed etch of backside oxide to compensate stress from oxide removed during CMP	Iterate between 3.6 and 3.7 until wafer bow is 0
3.8	Premetal-piranha	Strip resist	10minutes in 3:1 H2SO4:H2O2 15s dip in 50:1 DI H2O:HF
3.9	Coater6	Coat with 1.1um resist	60s 90C prebake Recipe: T1HMDS
3.10	Istepper	Photolithography LVL:02	LVL Name: 0.6um dots Maskname FEAREV2 Exposure: 160 ms 0.5um Focus
3.11	Coater6	Develop	Dynamic puddle developer dispense 120C 30s Postbake Recipe: PUDDLE3
3.12		MEASUREMENT STEPS	
a	Microscope		Optically verify vernier marks are aligned
b	SEM		Fine alignment and PR dot size
3.13	AME5000	Etch hardmask	Recipe: Baseline-ox-new 110s with 10s Descum
3.14	SEM	MEASUREMENT STEP	verify oxide disk shape and size
3.15	LAM490B	Rough emitter cone etch	25s Standard Nitride on Si Recipe + 10s overetch
3.16	SEM	MEASUREMENT STEP	Measure neck of cone

3.17	STS2	Si Nanowire etch	Etch pillars using recipe GUERRER1 Etch conditions: 6.7s C_4F_8 passivation cycle @ 45 sccm, 5s SF_6 etch cycle @ 90 sccm, 600 Watts RF (passivation), 800 Watts RF (etch), 120 Watts bias power, passivate first. Constant pressure 24 mTorr. Total etch time was 8 minutes. End on etch step to minimize polymer contamination.
3.18	Asher-TRL	Remove photoresist and Polymer	Ash in barrel asher minimum 1 hr to remove excess polymer and strip PR
3.19	OxEtch-BOE	Strip oxide hardmask in BOE	
3.20	SEM	MEASUREMENT STEP	Measure Emitter tip cone and pillar diameter and uniformity.
3.21	RCA-TRL	Standard RCA clean prior to oxidation	
3.22	Tube A2	Reduce emitter and pillar diameters using oxidation	Oxidize emitters and nanowires at 950 C using wet oxidation for time based on Silvaco simulations to attain sharp emitters and pillars of the correct diameter. Temperature is limited to 950 C because of viscoelastic flow of oxide at T>950 C.
4	Dielectric Fill-in and Planarization		
4.1	RCA-TRL	Standard RCA Clean	May be omitted if transferring right from diffusion furnace (recommended)
4.2	Tube-B4 Poly	Polysilicon deposition	LPCVD of Polysilicon 800 A at 590 C
4.3	RCA-TRL	Standard RCA clean prior to oxidation	May be omitted if transferring right from PolyTube (recommended)
4.4	Tube-A2	Oxidize polysilicon	40 minutes at 950 C wet oxidation. Enough to oxidize polysilicon + 50% overoxidation to ensure poly is completely consumed

			run 3-5 monitor wafers with 1000A thermal oxide for characterization
4.5 4.6	UV1280 RCA-TRL	MEASUREMENT STEP Standard RCA Clean	measure thickness and uniformity of poly-Si May be omitted if transferring right from diffusion furnace (recommended)
4.7	VTR	Nitride fill in	Deposit 1um LPCVD Si-Rich Nitride Using standard recipe run 3-5 monitor wafers (blank Si) for characterization
4.8 a b c	 UV1280 SEM AFM	MEASUREMENT STEPS	 Measure Nitride thickness and uniformity image sample ensuring regular pattern and no agglomeration. Optional: cleave and xsem of a wafer image surface roughness of the nitride
4.9	GnP	CMP Planarization of nitride film	Standard auto recipe polishing rate 4 A/s. Use monitor wafers to characterize polishing rate prior to running real wafers. Don't run for more than 1800s continuously. Enusure wafer is seated well in polishing head prior to starting.
4.10	premetal-piranha	post-cmp clean required to return to processing	2x10minutes in 3:1 H2SO4:H2O2 15s dip in 50:1 DI H2O:HF
4.11	UV1280	MEASUREMENT STEP	Measure thickness of nitride and oxide in various spots over wafer
5	Gate Definition, Deposition and Patterning		
5.1	NitrEtch-HotPhos	Hot Phosphoric Etch	Etch nitride to expose 200-300 nm of oxide domes. Etch rate 4nm/min
5.2 a	 SEM	MEASUREMENT STEPS	 Image sample to ensure oxide domes are exposed

b	AFM		Image sample to determine height of oxide dome
5.3	RCA-TRL	Standard RCA Clean	
5.4	Tube-6B n-Poly	Deposit gate polysilicon	800 nm n-poly run 3-5 monitor wafers with 1000A thermal oxide for characterization
5.5	RTA2	Dopant activation	800 C 30s RTA
5.6 a b	UV1280	MEASUREMENT STEP	 measure thickness and uniformity of poly-Si measure resistivity of poly
5.7	GnP	Polish Polysilicon to open gates	Timed polish of polysilicon
5.8	SEM	MEASUREMENT STEP	measure gate aperture diameter repeat 5.7 is underpolished
5.9	premetal-piranha	post-cmp clean required to return to processing	2x10minutes in 3:1 H2SO4:H2O2 15s dip in 50:1 DI H2O:HF
5.10	Coater6	Coat with 1.1um resist	60s 90C prebake
5.11	Istepper	Photolithography LVL:2	Recipe: T1HMDS Gate Maskname FEAREV2 Exposure: 160 ms
5.12	Coater6	Develop	Dynamic puddle developer dispense 120C 30s Postbake Recipe: PUDDLE3
5.13	AME5000	Etch gate polysilicon	120s in Ch.B recipe: PolySi:CH.B
5.14	Asher-ICL	Strip resist	3 minutes
6	Metalization		
6.1	HMDS-TRL	HMDS oven prior to coating with photoresist	Recipe 5
6.2	Coater	Spin coat Image reversal resist	AZ5214E Resist 3000 RPM, 7s dispense, 30s spin cycle (1.5 um of resist) Prebake oven 95 C 30 minutes
6.3	Istepper	Photolithography LVL:3	Metal Maskname FEAREV2b Exposure: 120 ms

6.4	Coater6	Image reversal bake	Recipe: PEB95 (95C 90s)
6.5	Istepper	Flood expsosure	500 ms, mask removed
6.6	Wetbench	Develop Resist	AZ922 Developer until clear (45 s)
6.7	Microscope	MEASUREMENT STEP	Verify features
6.8	EbeamFP	Deposit Metal Stack	Ni/Ti/Au 10nm/50nm/100nm
6.9	PhotoWetAu	Liftoff	Overnight in Acetone and then sonicate
6.10	Microscope	MEASUREMENT STEP	Verify good liftoff
6.11	HMDS-TRL	HMDS oven prior to coating with photoresist	Recipe 5
6.12	Coater	Spin resist to protect front side during backside film etching	SPR700 1000 RPM 7s dispense, 30s spin cycle
6.13	Postbake	Hardbake resist	1 hour 120C
6.14	STS1	Etch backside Poly and Nitride. Watch for clear	NITRIDE RECIPE. Variable time
6.15	LAM590-AU	Etch backside oxide	Standard oxide recipe
6.16	PhotoWetAu	Strip resist	Microstrip 2001 - 30 mins 70C in waterbath on hot plate x2 / SRD
6.17	Tube-B1 Au	Sinter metal	30 mins at 350C under forming gas
6.18	GreenFlo	Release Emitter tips	Silox Vapox III pad etch - 5 mins

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