Performance Limits of Silicon Solar Cells Due to Structural Defects

by

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Bachelor of Science, University of Oregon, 2007
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ABSTRACT

To minimize the risk of catastrophic climate change, about ten terawatts of photovoltaics must be deployed in the next fifteen years. Reaching this target will require dramatic reductions in the cost and capital intensity of manufacturing photovoltaic modules coupled with a significant increase in module efficiency. The majority of the factory and equipment costs to produce the crystalline silicon modules that account for over 90% of modules sold today are for production of silicon wafers. While lower-cost wafers can be produced with cheaper equipment, the efficiency of modules incorporating these wafers is limited by the presence of structural defects, like grain boundaries and dislocations, that are absent from more expensive alternatives.

This thesis presents a methodology to quantify the technology innovations necessary to reach climate-driven deployment targets for photovoltaics and shows an analysis based on current commercial technology incorporating monocrystalline silicon absorbers. Then, a model for the electrical activity of dislocations and grain boundaries and a methodology for incorporating this model into technology computer aided design (TCAD) simulations of high-efficiency solar cells are presented. The model and method are validated by comparison to analysis of the material properties and device performance of silicon solar cells containing structural defects. TCAD simulations across a wide range of defect concentrations and distributions are used to determine the material requirements for low-cost silicon containing structural defects to approach the performance of expensive, structural defect-free silicon in several high-efficiency solar cell architectures. Aspects of device design that mitigate the impact of these defects, notably higher injection-levels of electronic carriers, are identified.

Thesis Supervisor: Tonio Buonassisi

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CHAPTER

1

INTRODUCTION AND MOTIVATION

1.1 Climate-Driven Deployment Targets for Photovoltaics*

Recent studies show that carbon dioxide (CO_2) emissions must peak in the next fifteen years to ensure a high probability of limiting average global warming to less than 1.5 – 2 °C above pre-industrial levels [2]–[6] and thereby avoid the worst effects of climate change. As global energy demand is expected to rise significantly over the same period [2], [3], [7], achieving this goal will require the deployment of terawatts of new low-carbon energy generation, compared with less than 1 TW of non-hydro renewables today.

Photovoltaics (PV) have several advantages compared with other low-carbon technologies: the vast size of the solar resource [7], [8], the proven track-record of reliability [9]–[11] and bankability [12] of PV installations, the rapidity with which new manufacturing capacity can be brought online and projects developed and built [13], and their modular nature, which allows deployment in areas that may lack electric grid infrastructure. Concordantly, aggressive PV deployment targets, ranging from 1–10 TW by 2030, are widely viewed as vital to mitigate climate change (Figure 1.1, green symbols/line) [2], [3], [14]–[16].

* This chapter is largely taken from Ref. [1] and is reprinted under a Creative Commons Attribution 3.0 Unported Licence (http://creativecommons.org/licenses/by/3.0/legalcode). The cost and growth models used are available as a Microsoft Excel spreadsheet and a Matlab file, respectively, in the associated Electronic Supplementary Information on the publisher's website. The Matlab code was written and executed by J.R. Poindexter, and the climate targets and projections were compiled by R.C. Kurchin.

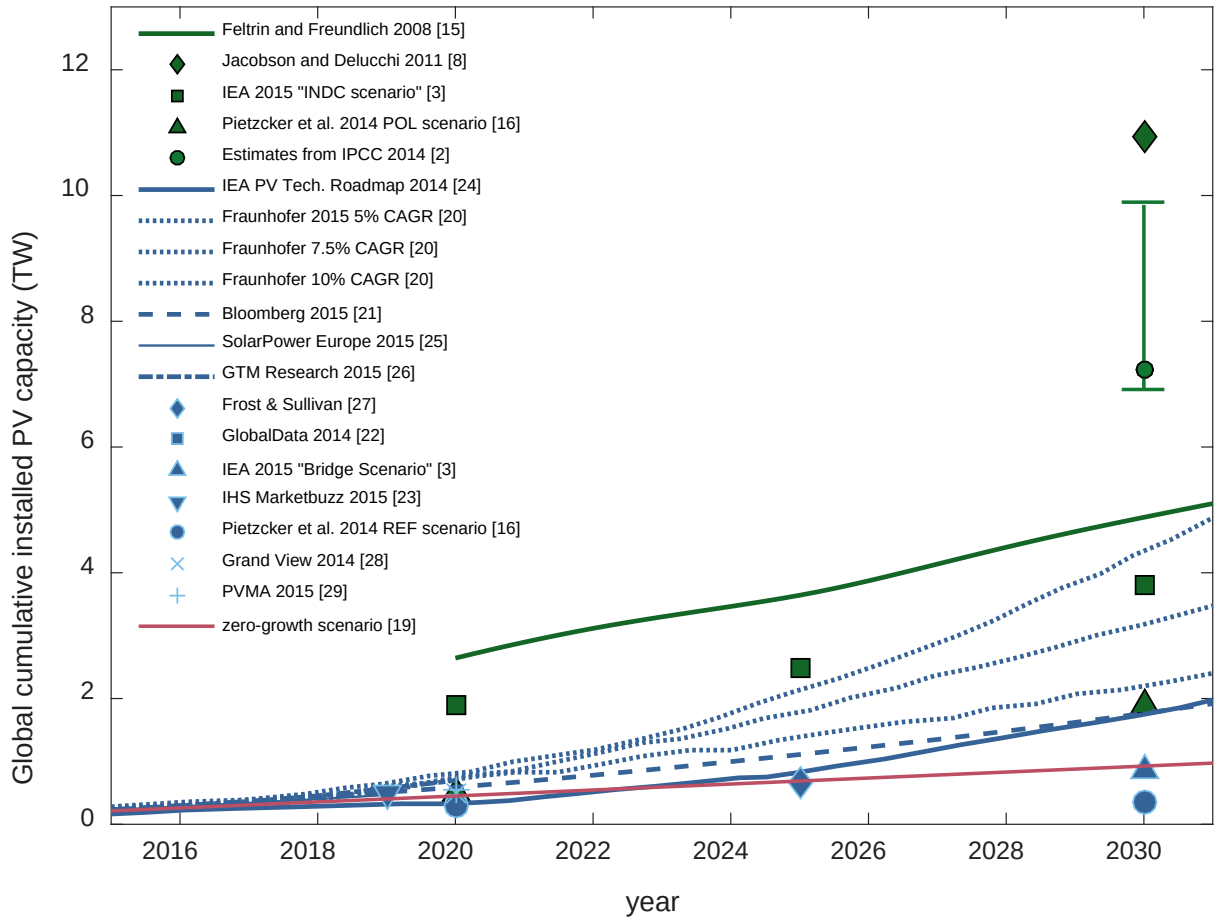

Figure 1.1. PV deployment targets consistent with average warming less than 2°C above pre-industrial levels (green symbols and line), industry projections of PV deployment (purple symbols and lines), and upper bound of future installations with no additional manufacturing capacity (pink line). Lines represent annual data, symbols represent data with lower temporal resolution.

In this thesis, a range of climate and CO_2 reduction scenarios are considered, which results in a range of PV deployment targets. These targets are shown in Figure 1.1 with the rated capacity of all installed PV in the world on the *y*-axis and the year on the *x*-axis. The highest targets provide the lowest risk to the climate. The different sources are described below.

The targets from the Intergovernmental Panel on Climate Change (IPCC) 2014 Synthesis Report [2] reflect the average and interquartile range from the set of predicted scenarios consistent with 430-480 ppm CO_2-equivalent stable concentration. However, the report only provided targets for the fraction of primary energy demand in 2030 met by low-carbon sources.

To show a PV target in Figure 1.1, the primary energy demand is taken from the International Energy Agency's (IEA) World Energy Outlook Special Report [3], and a third of the IPCC's low-carbon share is assigned to PV. This calculation yields range of about 7–10 TW. The two scenarios shown from the same IEA report mentioned above include one assuming all (pre-COP21) pledges already made by countries are met on time ("INDC scenario") and one intermediate scenario ("Bridge Scenario"). Jacobson and Delucchi [14], [8] assumed that all non-electric systems will be electrified and that all electricity will be provided by wind, hydroelectric, and solar technologies. Feltrin and Freundlich's [15] calculations were based on the IPCC Third Assessment report [17] and Hoffert *et al.*'s seminal paper [18] as well as the assumption that PV would satisfy the difference between projected capacities of other technologies and carbon-free electricity required to meet projected demand consistent with 450 ppm. Pietzcker *et al.* [16] predicted penetration based on an economic model of the electricity market and provided a reference scenario and a scenario in which policies are enacted to cause solar to be sufficiently economically competitive to be consistent with 2° C average warming. For sources that reported only energy output and not generation capacity, a very conservative capacity factor of 20% is assumed. Capacity factor is the ratio of average power production (typically either over a year or over the lifetime of a power plant) to the peak production capacity—the rated wattage of a PV panel or array in the case of solar PV.

Future deployment of PV depends on a number of factors. The following discussion focuses on the upper bound imposed by one technical constraint, the annual manufacturing capacity for PV modules, and one market constraint, total demand for PV. Manufacturing capacity limits annual installed capacity, which in turn limits cumulative installed capacity each year. Demand for PV modules has a strong dependence on public policy and the cost of competing (*e.g.*, fossil fuel) and supporting (*e.g.*, balance-of-systems, energy storage) technologies. However, under a given set of assumptions about the economic and technology environment, total demand can be given as a function of PV module price. This relationship is called a demand curve (See Figure 1.3).

As shown by the pink curve in Figure 1.1, current PV manufacturing capacity [19] is sufficient to produce just under 1 TW in the next 15 years. Thus, growth in manufacturing capacity is needed to meet climate-driven deployment targets. Note that the growth rate of cumulative installed capacity is often quoted for the PV industry. In this thesis, "growth" and

"growth rate" refer only to growth of *manufacturing* capacity (i.*e.* annual, not cumulative, installations). According to market research [19], under the current cost structure for PV modules, total demand would be less than 1 TW even if their price was equal to their variable cost of production.

Several PV industry projections [16], [20]–[29] (Figure 1.1, purple symbols/lines) predict deployment comparable to some climate-driven targets, though the most aggressive projections fall well short of targets, like those from the IPCC, that minimize climate risks. Even these projections imply significant growth in manufacturing capacity and easing of demand constraints. However, most publicly available projections do not establish whether current technology can reach these targets and fail to identify effective pathways to achieve the necessary manufacturing capacity and demand.

In the rest of this chapter, bottom-up cost modeling is used to evaluate (1) if current crystalline silicon PV module technology can achieve growth rates commensurate with climate targets without external financial support and (2) what innovation-driven cost reductions are needed for sufficient demand to reach these targets. The results show that dramatic reductions in the capital intensity and cost of PV module manufacturing are needed. The technology pathways that are identified to accomplish these goals incorporate low-cost, low-capex silicon into high-efficiency PV panels. The efficiency of most panels that use such materials are limited by the presence of structural defects like grain boundaries and dislocations. Therefore, this thesis goes on to describe a model for evaluating the impact of these defects on advanced PV solar cells, determine the materials requirements to achieve high efficiency, and identify solar cell architectures that can help mitigate their detrimental effects.

1.2 Bottom-up Cost and Sustainable Growth Model

1.2.1 Bottom-up Cost Model

The cost model [30], [31], presented schematically in Figure 1.2, produces a discounted cash flow for a hypothetical monocrystalline silicon PV manufacturer by summing the individual cost components (the equipment, materials, labor, and business expenses) of the manufacturing process and subtracting these from revenues and financing. Financial decisions are affected by a

discount rate (in this case equal to the weighted average cost of capital, *WACC*, taken from Ref. [32]), depreciation of capital equipment, and amount of working capital (cash on hand to cover operational expenses for a fixed period of time—3 months in this model—which is then reinvested). In simple terms, the "cash in" variables are (1) net revenues from PV module sales, expressed per unit as operating margin (*margin*), and (2) debt financing. The relationship between price, cost, and margin can be expressed mathematically as:

$$margin = \frac{price/_{unit} - cost/_{unit}}{price/_{unit}}. \quad (1.1)$$

Because debt typically leverages equity within the company, it is described by the variable *debt/equity ratio* (*DER*), which is held constant over time in this analysis.

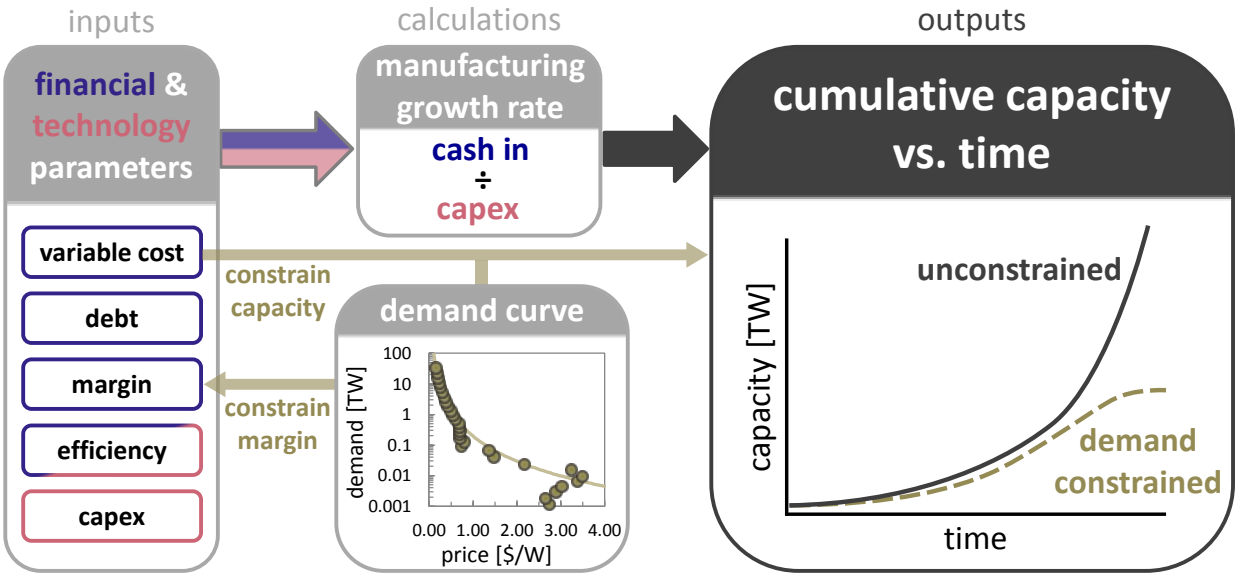

Figure 1.2. Schematic of cost model used to calculate economically sustainable growth rate, constrained by power law fit to a market-driven demand curve **[19]**, to predict cumulative capacity.

The "cash out" variables (before taxes and interest on debt are paid) are the fixed costs of new factories and equipment (expressed as *capex*) and the *variable costs* of production. Because we are interested in the cost per unit power, not per panel, both fixed and variable costs are divide by the power produced by the module. *Efficiency* is used as a proxy variable for module power, and $/W as the units of capex and cost. To estimate an upper bound for manufacturing capacity growth rate, it is assumed that no dividends are paid and all profits (after taxes and interest on debt) are reinvested in expansion.

Taxes (*T*) and interest on debt (*I*) are calculated after margin. The baseline scenario considered here is one in which the price is set such that internal rate of return (*IRR*, equivalent to interest earned on money invested in producing PV modules) calculated from the discounted cash flow equals the *WACC*. We call this price the "minimum sustainable price" (*MSP*), because it is the minimum price required for sufficient returns to investors to sustain investment [30].

1.2.2 Sustainable Growth Model

The ratio of "cash in" (margin and debt) to capex determines how quickly new factories can be built and therefore how quickly PV manufacturing capacity can grow. Thus, increases in "cash in" or decreases in capex increase growth rate. Quantitatively, the growth rate in manufacturing capacity (G_{M}) is calculated as:

$$G_{\mathrm{M}} = \frac{(margin - I - T) \times (1 + DER)}{PPER + C}, \tag{1.2}$$

where *PPER* is the ratio of capex (*i.e.*, plant, property, and equipment) in the previous year ("*y* – 1") to gross revenue in a given year "*y*" and *C* is working capital divided by revenue[31].

To set an upper bound on cumulative installed capacity, 100% utilization of manufacturing capacity is assumed. Because we consider a 15-year time horizon while PV panels typically last at least 20 years, no replacement is also assumed. Therefore, cumulative installed capacity is just the sum of the previous year's cumulative capacity and the manufacturing capacity in the current year. Manufacturing capacity in the current year is manufacturing capacity in the previous year times one plus the growth rate.

If costs and price remain constant over time, then G_{M} is constant. This amounts to exponential growth, which provides a lower bound on the growth rate required to install a certain cumulative capacity by a certain time. G_{M} is the derivative of annual installed capacity. If $G_{\mathrm{M},C}$ is the growth rate required to reach a capacity *C* in a time *t*, then if in any year $y < t$, $G_{\mathrm{M},y} < G_{\mathrm{M},C}$, there will have to be another year $y' < t$ when $G_{\mathrm{M},y'} > G_{\mathrm{M},C}$ in order to reach capacity *C* by time *t*. Thus, $G_{\mathrm{M,C}}$ provides a lower bound on the growth rate necessary to reach capacity *C* by time *t*.

1.2.3 Demand Constraint

The growth rate calculator begins by assuming a constant margin. The product of this margin and the sum of fixed and variable costs sets a selling price. If cumulative capacity exceeds demand at this price, the calculator takes the price corresponding to this capacity on the demand

curve, and uses the (lower) margin implied by this price. This reduced margin limits growth. If price falls below variable cost, production ceases altogether.

The demand curve used to determine demand at a given price is taken from Ref. [19], includes both historical and projected demand, and is shown in Figure 1.3a. From the historical data, it is clear that demand is a strong function of both the market and policy environments. Furthermore, sometimes as in the last several years, installations cannot keep up with demand at a given price. To determine the installation constraints imposed by PV module manufacturing, we are interested in the maximum demand at a given price. The growth model also requires a single-valued function for demand at a given price. Therefore, the demand curve is fit with an analytical function, neglecting points that clearly indicate artificially low demand. A power law is obtained:

$$demand = 197155 \times price^{-2.735}, \quad (1.3)$$

which fits the demand curve with an R^2 value of 0.9917. The result of this fitting is shown in Figure 1.3b, and the fitted curve is shown with the full demand curve from Ref. [19] in Figure 1.3c.

As mentioned above, demand is strongly dependent on the business and policy environment with many factors can influence "willingness to pay" for PV. These include:

- Grid constraints and electricity markets, including utility tariff structures, ancillary services markets, and electric grid technology.
- Energy and climate policy, including carbon pricing, fossil fuel subsidies, and supply- and demand-side PV subsidies like feed-in-tariffs, investment tax credits, renewable portfolio standards, low/zero-interest loans, subsidized land or equipment, *etc*.
- The cost of supporting or competing technologies like fossil fuels, energy storage, PV balance-of-systems, labor for manufacturing and installation, *etc*.

To account for these uncertainties, while keeping the analysis as general as possible, the power law is shifted with a constant scaling factor:

$$demand = c \times 197155 \times price^{-2.735}, \quad (1.4)$$

where c is a constant. In this analysis, c = 0.54 and c = 2.19 are considered. While this appears to represent a factor of two uncertainty of demand at a given price, Equation (1.4) can be rewritten as:

$$demand = 197155 \times (price \times c^{-1/2.735})^{-2.735}, \quad (1.5)$$

and one observes that these values of *c* only represent a factor of 0.25 uncertainty in the price at which a given cumulative PV capacity will be demanded. Figure 1.3d shows the demand curve from Ref. [19], along with the power law fit and the shifted power law curves.

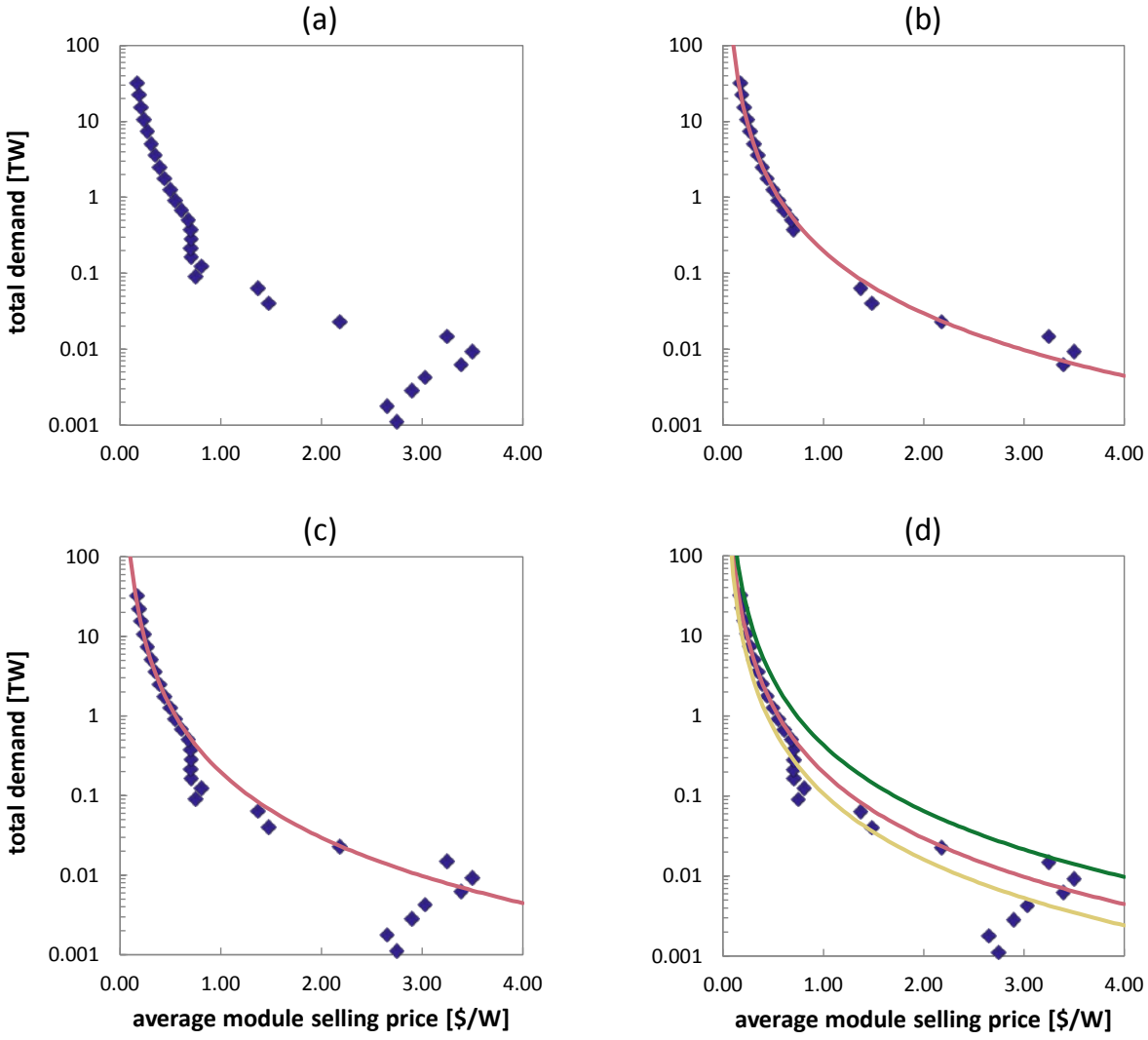

Figure 1.3. (a) Installed capacity (demand) as a function of selling price (historical and projected) **[19]**. (b) Power law fit to historical data, excluding points where installations appear to be constrained by something other than module price. (c) Power law fit from (b) with full demand curve. (d) Full demand curve with power law fit and power law shifted to account for uncertainty in the future market and policy environments.

1.2.4 Choice of Crystalline Silicon

This thesis, including the cost and growth modeling, focuses on crystalline silicon (c-Si). c-Si has many advantages over competing technologies, both established and novel. It represents over 90% of the PV market today [33], has dominated for decades [34], has a large existing manufacturing base, is sufficiently abundant to scale to tens of terawatts [35], and is non-toxic. It also has a rich history of research with a wealth of data, including cost data, available.

The sustainable growth modeling methodology described above, and therefore the capex and cost implications described below, could apply to any technology. This includes commercially available thin-film technologies like cadmium telluride and copper (indium, gallium) diselenide. However, the ability of these technologies to scale to multiple terawatts is likely limited by the availability of Te and In [15], [36], [37].

Non-silicon technologies have the challenge of scaling from a lower baseline. c-Si starts from a manufacturing base of more than 50 GW/year. New technologies, which traditionally take 10–15 years to commercialize [38], therefore face the additional burden of scaling to this capacity. If we assume they start from a capacity of 100 MW in 2016, have the same operating margin as assumed here for silicon, and hold the same three months of working capital, they would require about 100 times less capex than the target identified below to reach 10 TW by 2030 (about 6 times less if they have $30\%_{rel}$ higher margin). If they do not enter commercial production until 2021, they would require more than twice the margin assumed here for silicon and 80 times less capex than is necessary for silicon to reach 10 TW by 2030. There is certainly an opportunity for a low-cost technology to gain market share through significantly higher margins and lower capex, but the bar is quite high to impact 2030 climate targets. Through exponential growth, the potential for new technologies to make a significant contributions to installed PV capacity after 2030, even as soon as 2040, is much greater.

1.3 (Technology) Drivers of Growth Potential for PV

1.3.1 Demand-Constrained Growth Model Sensitivity Analysis

Figure 1.4 shows a sensitivity analysis of each of variable in the cash flow. This analysis indicates which of these variables have the greatest potential to increase growth rate and ease the

demand constraint. Figure 1.4a shows the demand-constrained cumulative installed capacity in 2030 for a range of values, varying each parameter independently. The left axis in Figure 1.4b shows the unconstrained installed PV capacity in 2030, which depends only on the growth rate. The right axis in Figure 1.4b shows the corresponding growth rates.

For the baseline calculation around which these parameters are varied (the point of intersection of the curves in Figure 1.4), current industry data is used for variable costs, capex, and efficiency; margin is set such that the net profit is equal to the cost of capital [32]; and a debt/equity ratio of 1:1 is used. These baseline parameters are listed in Table 1.1, and details of how they were selected are in Refs. [30], [31].

Table 1.1. Model parameters for baseline scenario and other scenarios in **Figure 1.6**.

Parameter	Baseline	Line-of-sight	Increased debt	Low-variable cost advanced concept	High-efficiency advanced concept
Module efficiency	16.0%	18.0%	18.0%	18.0%	24.0%
Wafer Thickness (µm)	180	120	120	20	20
Kerf loss (µm)	130	130	130	20	20
Variable costs ($/W)	0.541	0.264	0.264	0.184	0.189
Fixed costs ($/W)	0.183	0.091	0.091	0.047	0.043
Fixed + variable costs ($/W)	0.724	0.355	0.355	0.231	0.231
Margin	15%	15%	15%	15%	15%
DER	1:1	1:1	5:1	1:1	1:1

Results from the baseline scenario show that growth rate must be increased while costs are decreased to reach aggressive deployment targets. As stated in Chapter 1.1, the baseline scenario is limited by demand to less than 1 TW in 2030 (Figure 1.4a), but even without demand constraints, manufacturing growth would limit cumulative installed capacity to 3.4 TW (Figure 1.4b).

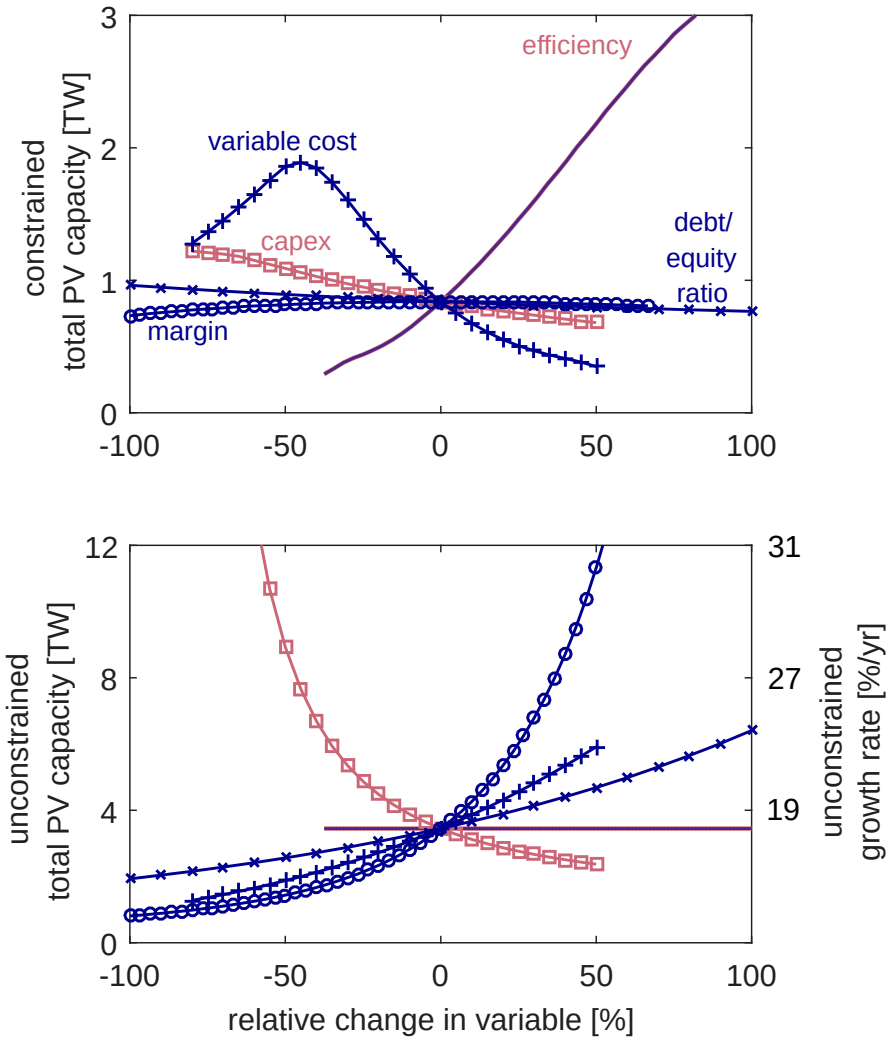

Figure 1.4. a) Demand-constrained cumulative installed capacity in 2030 as a function of capex, module efficiency, margin, variable costs, and debt/equity ratio. b) Unconstrained cumulative installed capacity in 2030 as a function of the same variables. This capacity depends only on growth rate (right axis). Each parameter is varied independently and reported as a fractional increase or decrease from the baseline scenario.

This sensitivity analysis shows that three of these variables (margin, debt/equity ratio, and capex) can increase growth rate but have little potential to reduce cost and increase demand, while the other two (variable costs and efficiency) can reduce cost but have little potential to increase growth rate.

Increasing margin increases growth rate by increasing revenue from sales (a major component of "cash in"). However, PV modules have become a commodity with little product differentiation. Module manufacturers are therefore price-takers with little ability to impact

margin [39], [40], and there appears to be little practical opportunity to increase growth rate by increasing margins.

Increased debt without significant reductions in cost will increase growth temporarily. Ultimately, however, once the demand ceiling is reached, margin will be eroded, leading to reduced revenue, reduced growth and lower total installed capacity. The increased debt approach is therefore risky for manufacturers. Increased debt is also a weaker lever on growth than reducing capex, which reduces the cost for a new factory. Assuming constant "cash in," reduced capex increases the rate at which new factories can be built and manufacturing capacity added.

In the growth model used here, the only positive effect reducing variable cost has on installed capacity is triggering a reduction of price due to the assumption of constant margin. Margin is assumed to be constant because technology diffusion and the treatment of PV modules as a commodity by consumers and installers drive down prices in response to reduced variable costs. Lower prices mean lower revenue ("cash in"). At constant capex, that means slower growth. Therefore, while reducing variable costs eases the demand constraint on total installed PV capacity, it reduces growth rate as well. This trade-off leads to the maximum in the variable costs curve in Figure 1.4a.

Increasing efficiency, on the other hand, reduces both fixed and variable costs (per unit power). Assuming efficiency increases while capex and variable costs per module remain constant, higher efficiency can ease the demand constraint while maintaining a constant growth rate. This constant growth rate is indicated by the flat efficiency curve in Figure 1.4b.

In certain instances, the financial incentives experienced by an individual company can oppose the goal of maximizing PV deployment. For example, to maximize short-term revenue, a company is motivated to reduce costs, striving for first-mover advantage or struggling to keep up with competitors. However, once a cost-reducing innovation spreads throughout the entire industry and prices are reduced across the board, lower prices decrease margins in absolute dollars [41]. Thus, the so-called "race to the bottom" generally results in decreased sustainable manufacturing growth rates, except for the first movers. In contrast, across-the-board increases in sustainable manufacturing growth rates can be achieved by reducing capex. Note that even if the entire industry lowers capex, the sustainable growth rate will increase for all companies, as new factories cost less money to build. However, the longer-term investment in capex reduction does not have as strong an impact on short-term revenue as other cost-reduction measures; thus, capex

reduction is often not prioritized in industry roadmaps. Other trade-offs between the techno-economic inputs shown in Figure 1.4 are analyzed in Figure 1.5.

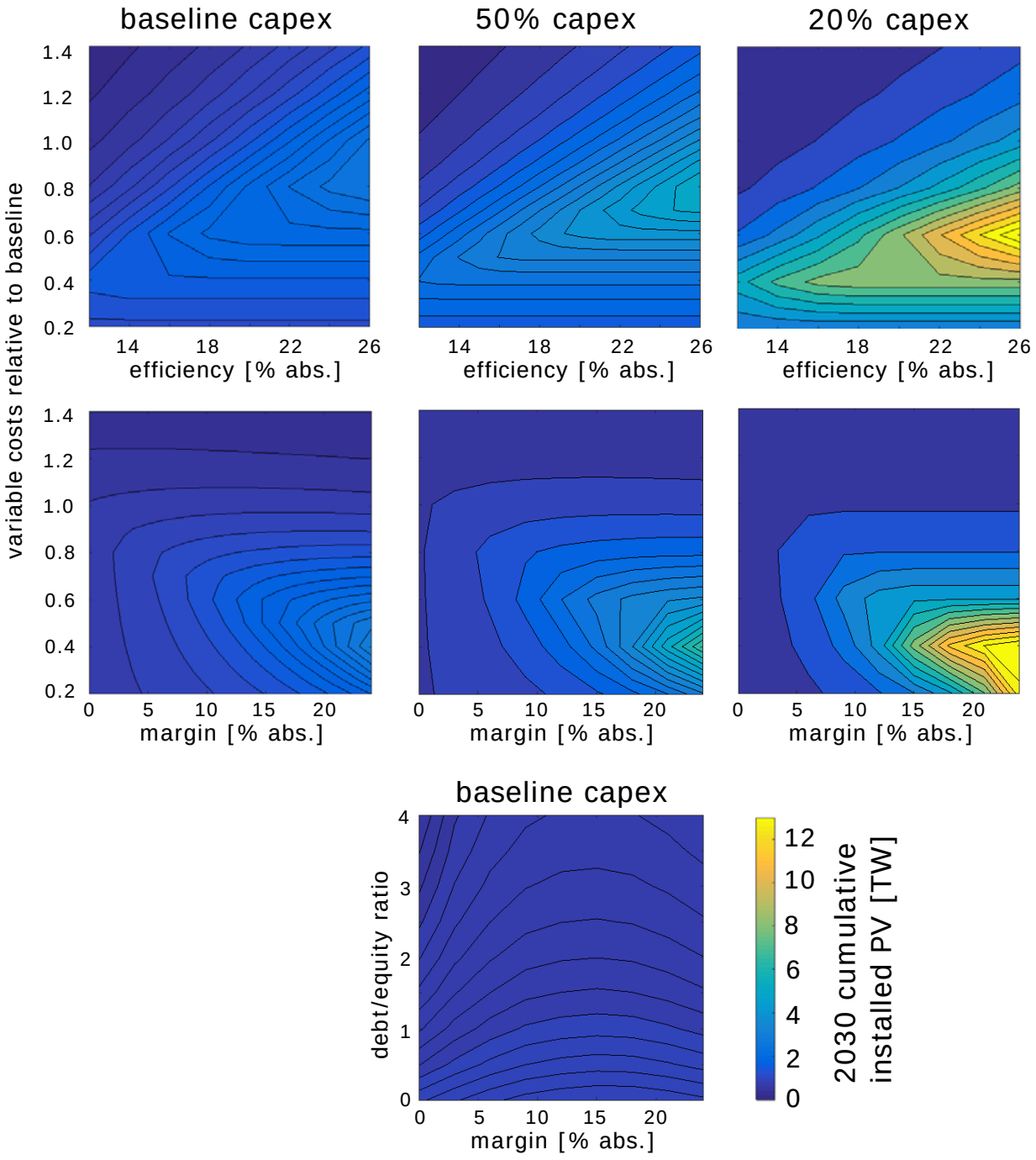

Figure 1.5. Contour plots of installed capacity in 2030 *vs.*relative changes in pairs of variables for (a) efficiency and variable costs at baseline capex, (b) efficiency and variable costs with a capex reduction of 50% from baseline, (c) efficiency and variable costs with a capex reduction of 80% from baseline, (d) margin and variable costs at baseline capex, (e) margin and variable costs with a capex reduction of 50% from baseline, (f) efficiency and variable costs with a capex reduction of 80% from baseline, (g) operating margin and debt/equity ratio with baseline capex.

Figure 1.5a,b,c shows the capacity achievable through simultaneous changes in only the technological variables. The relationship between capex and efficiency is monotonic, because efficiency affects cost alone and capex affects growth rate much more strongly than cost. However, there is an optimum value of variable costs at any combination of efficiency and capex because variable costs affect both cost and growth rate to a similar degree. This fact implies that while some reduction of variable costs are probably required to reach high installed capacity, continuous reductions will ultimately limit growth rate.

Figure 1.5d,e,f shows that by increasing margin, the optimum value of variable costs is reduced. Conversely, if margin falls, the optimum value of variable costs actually increases. This relationship is due to the fact that growth rate is driven by *PPER*. Therefore, revenue must be sufficiently high relative to factory costs to enable rapid increases in manufacturing capacity.

Figure 1.5g shows the relationship between debt/equity ratio and margin. Debt/equity ratio is often increased when margin decreases to enable further growth. However, in a price-constrained environment, this approach does not yield increased cumulative capacity because neither of these variables reduces cost. Ultimately, in a price-constrained environment, increased growth from increased debt/equity ratio will further reduce margin because in this situation, margin will be set by demand rather than cost, so it is not an effective long-term strategy.

1.3.2 PV Technology and Deployment Scenarios

To quantify the efficacy of various capex- and cost-reduction approaches, Figure 1.6 shows the cumulative installed capacity as a function of time for several representative scenarios: the baseline scenario with today's technology (light blue), line-of-sight technology improvements from industry roadmaps (red), two advanced technology scenarios (dark blue and green), and line-of-sight technology with an increased debt/equity ratio (tan). Key input parameters for each scenario are in Table 1.1.

The colored lines are constrained by our baseline assumptions for demand as a function of module price. The shaded area indicates the range of installed capacity when demand is increased or decreased from this baseline, as described in Chapter 1.2.3. When the colored line is on the top boundary of the shaded area, it indicates that installed capacity is growth-constrained rather than demand-constrained for that scenario with our baseline demand assumptions. The shaded bars to the right of the plot indicate the range of capacities in 2030 with increased and

decreased demand. The dark lines on those bars indicate capacity obtained with the power law fit to the demand curve in Ref. [19]. Climate targets are also included for reference (gray).

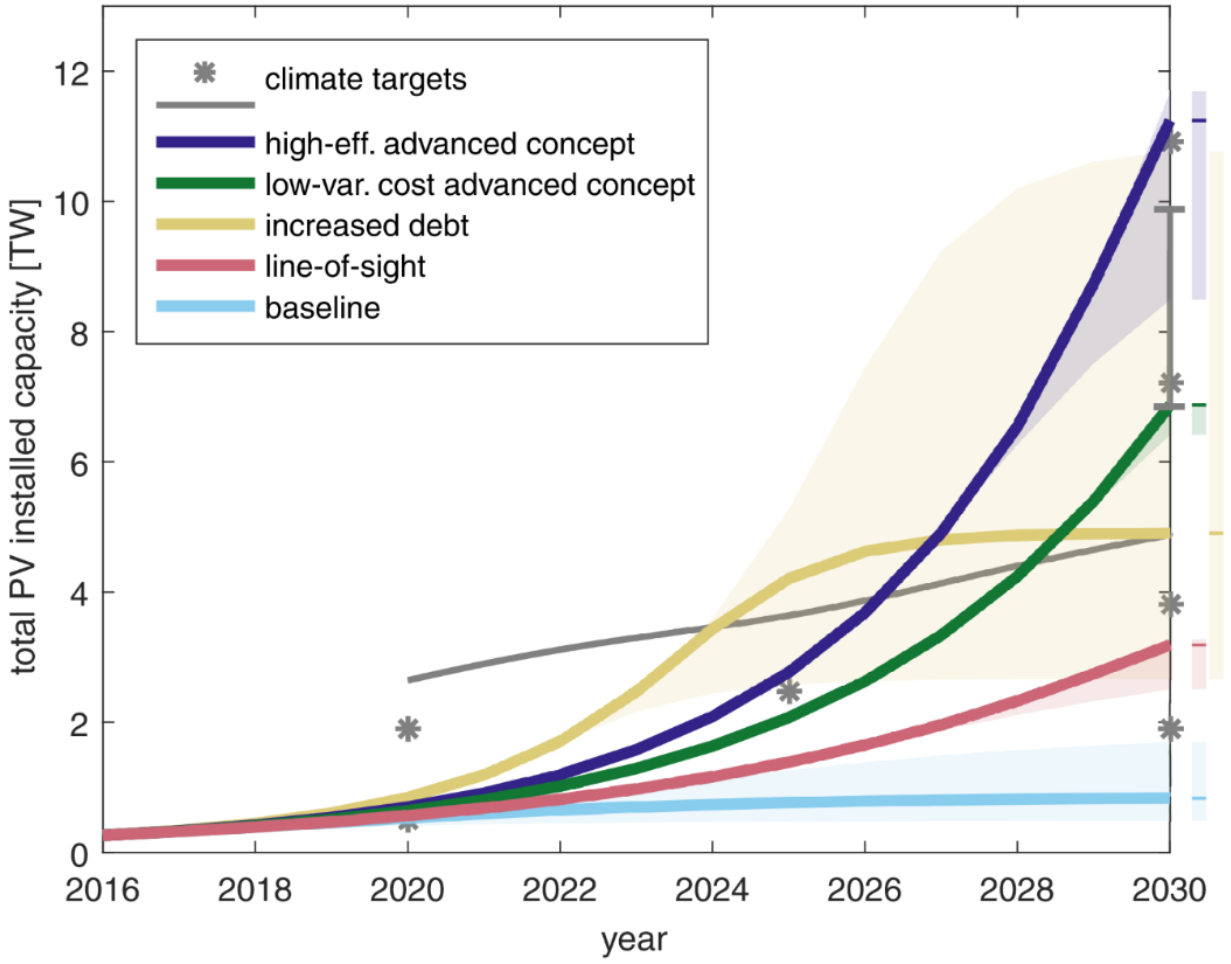

Figure 1.6. Climate targets (gray line and symbols) along with projections for: baseline technology (light blue), line-of-sight technology improvements (red), an advanced technology concept focused on increased efficiency (dark blue), an advanced technology concept focused on reduced variable costs (green), and line-of-sight technology improvements with a debt/equity ratio of 5:1 (tan). The shaded area indicates the range obtained with increased and decreased demand. Colored lines indicate projection for power law fit to projected demand curve from Ref. **[19]**. Shaded bars to the right of the plot indicate the range of capacities in 2030 with increased and decreased demand. Dark lines on these bars indicate capacity obtained with the power law fit to the demand curve in Ref. **[19]**.

Line-of-sight technology reduces wafer thickness from 180 µm with 130 µm of kerf (sawdust) to 120 µm with 130 µm of kerf. Additional modest reductions in capex and variable costs and an increase in efficiency are included as well. In this scenario, a total installed capacity of 3.2 TW is achievable by 2030. Gains in growth rate due to reduced capex are offset by reductions in

revenue due to reduced variable costs, so the line-of-sight technology actually has a slightly lower unconstrained growth rate than baseline. Total installed capacity is limited by both price (3.2 TW) and growth rate (3.3 TW) for line-of-sight technology, indicating a need to reduce both capex and cost further.

Scenarios for two advanced PV technology concepts are therefore also considered. In both scenarios, wafer thickness and kerf are reduced to 20 µm each (the equivalent of 40 µm-thick kerfless wafers), which significantly reduces both capex and variable costs. A further 71% reductions in capex is then coupled to either (1) a further 45% reduction of variable cost and the same increase in efficiency as in the line-of-sight scenario (to $18\%_{abs}$) , or (2) a 25% further reduction of variable costs and an increase in efficiency to $24\%_{abs}$ (which further reduces both capex and variable costs). Scenario 1 represents direct reduction of variable costs by reducing the cost of inputs to production like electricity and silver, either through price reductions, quantity reductions, or replacement. This approach results in reduced revenue, which limits growth rate, and a cumulative installed capacity in 2030 of 6.9 TW. Scenario 2, which drives cost reduction primarily by increasing efficiency, results in faster growth and a cumulative installed capacity in 2030 of 11.2 TW.

For scenarios that require technological innovation (efficiency increases, capex reduction), all innovations are assumed to be available starting in 2016. While clearly optimistic, this assumption gives an upper bound for the impact of innovation. However, when new technology is developed and adopted is crucial in the impact it can have on future PV deployment. Figure 1.7 shows this effect for (a) line-of-sight technology, (b) line-of-sight technology with increased debt, (c) the high-efficiency advanced technology concept, and (d) the low-variable cost advanced technology concept. The importance of developing and rolling out new technology as quickly as possible is clear. Furthermore, the potential for debt to maintain high growth rates in the short-term while lower capex technology is developed is shown in the comparison between Figure 1.7a and Figure 1.7b.

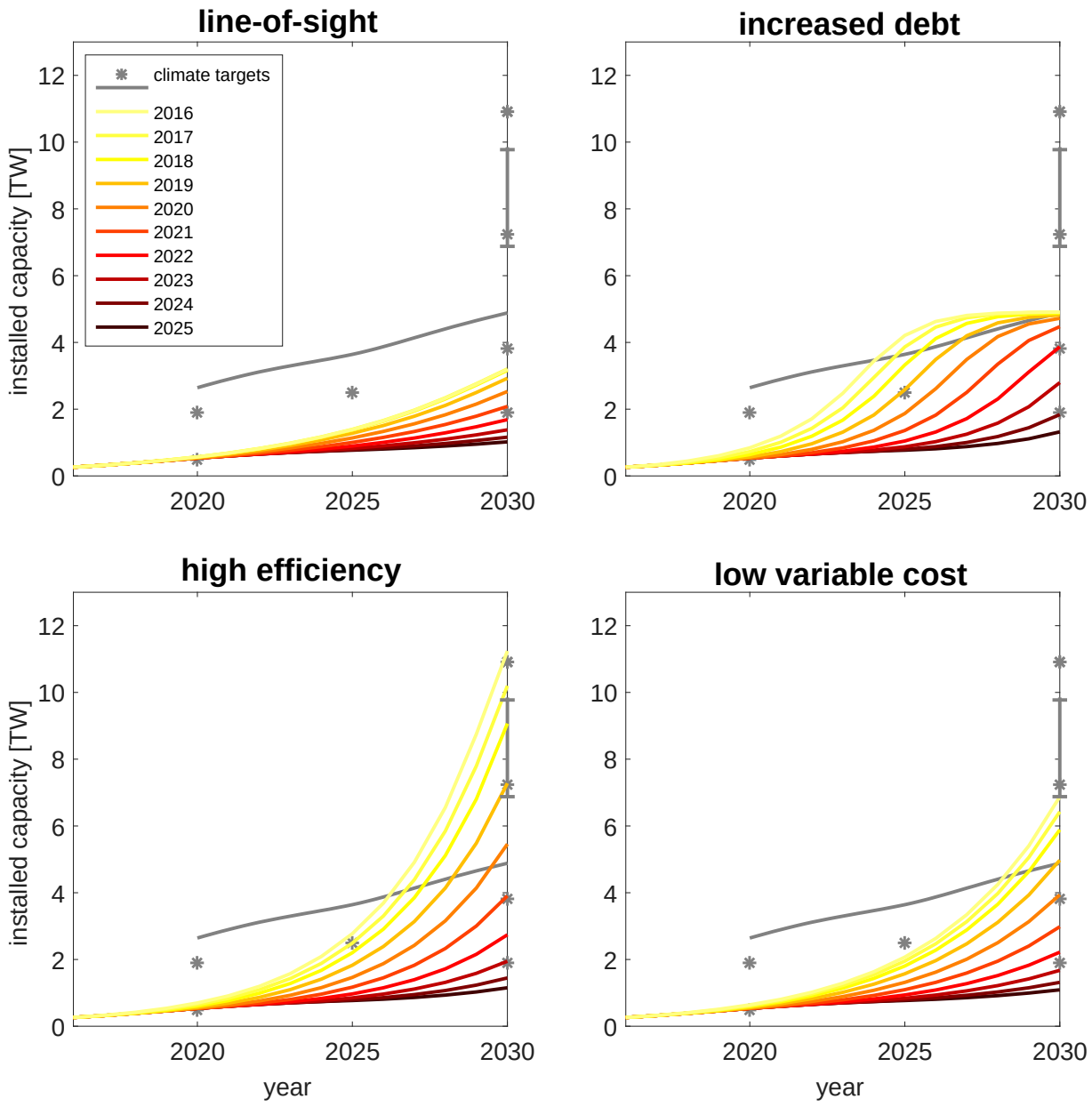

Figure 1.7. Climate targets (gray line and symbols) along with projections for installed capacity in each year for: (a) line-of-sight technology improvements, (b) line-of-sight technology improvements with a debt/equity ratio of 5:1, (c) the high-efficiency advanced technology concept, and (d) the low-variable cost advanced technology concept. Each curve indicates an adoption of the technology in a different year (darker curves are later and lighter curves are earlier). Installations proceed according to the baseline scenario until the new technology is adopted.

As just mentioned, debt can be used to increase growth rate, and this may be necessary in the short-term as new technologies are developed. However, as discussed in Chapter 1.3.1, debt would have to come with significant reductions in cost to fuel long-term growth. To illustrate

this point, a scenario with line-of-sight technology improvements and a debt/equity ratio of 5:1 is shown in Figure 1.6. As with the line-of-sight scenario with a debt/equity ratio of 1:1, installed capacity is limited to less than 5 TW. In addition, changes in the demand curve have a much stronger effect in this scenario than in the technology innovation scenarios, with the high demand case yielding 11 TW of PV but the low demand case less than 3 TW. This sensitivity leads to a large range in the total amount of debt that would have to be sourced in such a scenario, ranging from $0.9 trillion to $3.7 trillion with baseline projected demand requiring $1.6 trillion. Finally, the interest rate on debt also has a significant impact on the installed capacity in the increased debt scenario. An increase from 5% (baseline assumption) to 10% reduces installed capacity in the high-demand case from 11 to 7 TW, as shown in Figure 1.8.

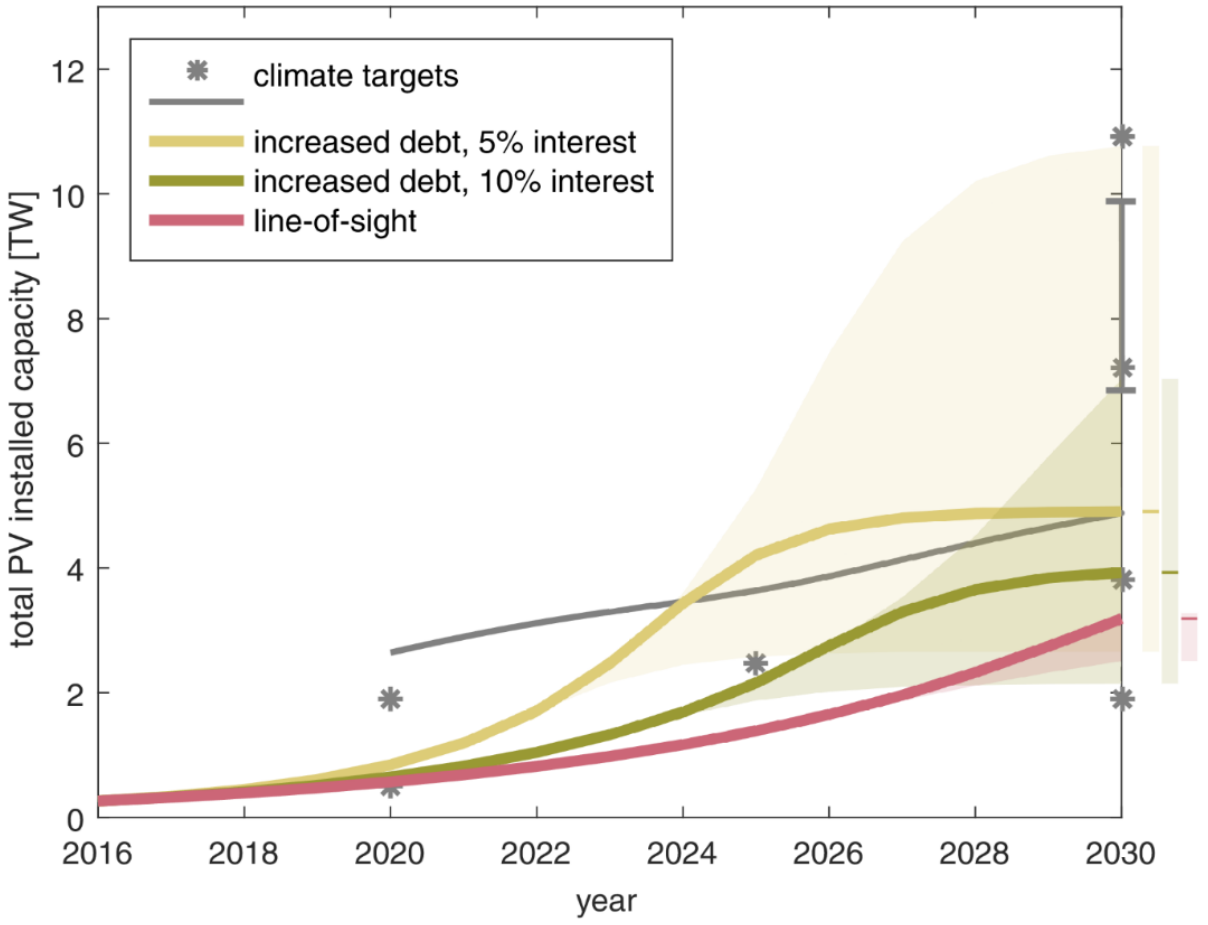

Figure 1.8. Climate targets (gray line and symbols) along with projections for: line-of-sight technology improvements (red), line-of-sight technology improvements with a debt/equity ratio of 5:1 and an interest rate on debt of 5% (tan), and line-of-sight technology improvements with a debt/equity ratio of 5:1 and an interest rate on debt of 10% (brown). The shaded area indicates the range obtained in with increased and decreased demand. Colored lines indicate projection for power law fit to projected demand curve from Ref. **[19]**.

There are clear and redundant pathways to achieve the reductions in variable costs and capex, as well as the improvements in efficiency described in the advanced scenarios. Variable cost reductions up to 40% are on industry roadmaps as described in detail in Refs. [30], [33].

Capex reductions are available through a variety of process modifications. Some examples follow. Replacing slurry wire sawing with structured or diamond wire eliminates equipment for slurry collection and increases throughput [42]. Kerfless wafering would also eliminate this equipment and the equipment used to recondition scrap silicon. The throughput of emitter formation can be increased in the case of batch processing with a gas dopant source (*e.g.*, $POCl_3$) by depositing at lower pressure [43]. This process can also be completely replaced by ion implantation [44], [45] or chemical vapor deposition (CVD) either of a dopant source [46], a doped epitaxial Si layer [47], or a polysilicon layer [48]. CVD and implant emitter formation also obviate the need for edge isolation because they are single-sided processes. The capex associated with contact firing can be reduced for a traditional belt furnace process by increasing the throughput of the entire manufacturing process (the throughput of a belt furnace is just determined by the belt length). Belt furnace firing can also be replaced by laser-firing [49]–[51] or another more efficient furnace [52], [53]. On the module level, capex can be reduced by eliminating the aluminum frame [54]–[56] and simplified tabbing and stringing of cells together [57].

However, the largest component (over 30%) of the capex in PV module manufacturing is the production of polysilicon feedstock. Reduction of the silicon wafer thickness from its current value of about 180 µm to 10–20 µm (with equivalent reductions in kerf loss, or 30–50 µm with no kerf loss) would eliminate 90% of this capex. Multiple technologies exist, some of which have already demonstrated high efficiency on wafers as thin as 35 µm, including silicon grown epitaxially directly from vapor sources [58], silicon wafers produced directly from molten silicon without casting and wire-sawing [59], and thinner wire saws [42], [60], [61]. Thinner wafers also contribute to higher throughput processing, further reducing capex. Specifically, the throughput of crystal growth, ingot cropping, wire sawing, and wet chemical steps are increased by having thinner wafers.

Czochralski growth of traditional monocrystalline silicon (Cz-Si) is also very capital-intensive, representing another 15% of the capex in a monocrystalline silicon PV module [31]. Directional solidification of multicrystalline silicon (mc-Si) is relatively low capex, and recent

results on “high-performance” mc-Si offer promising routes to high efficiency [58], [62]. The capex associated with mc-Si could be reduced by planned moves to larger ingots [33], [63] (further increasing throughput). Cz-Si could be replaced by mc-Si, one of the growth techniques mentioned above, or another technique like kyropolis growth, which has demonstrated good material quality with potentially low capex [64]. Combined, all the processes mentioned above represent over 75% of the capex of producing a monocrystalline PV module [31].

Multiple PV cell technologies, including passivated emitter and rear local contacts, heterojunctions, interdigitated back contact designs, and fully passivated contacts, have demonstrated efficiencies over 25% [58], and roadmaps exist up to 26 – 29% [33], [65], [66]. There is also promising work to reduce cell-to-module losses [67]–[69].

1.3.3 Enabling High-Efficiency PV with Low-Cost/Low-Capex Silicon

As mentioned above, there are several established and early-stage commercial techniques for producing Si wafers for solar cells with substantially lower cost and lower capex than Cz-Si. The most well-established is directional solidification of mc-Si, which (together with its “high-performance” variant) currently account for 65% of the Si wafers produced for solar cells [70]. Others include Si wafers grown directly from gas- or liquid-phase Si, “quasi-monocrystalline” grown using a similar technique to high-performance mc-Si but with large monocrystalline seeds [71], and Si grown by the “non-contact crucible” (kyropolis) method. In all of these techniques, decorated crystal defects, including dislocations and grain boundaries have been shown to limit device performance [72]–[75], [62], [76]–[78], [71], [79]–[86], [64]. However, strides have been made to improve the performance of these materials in the presence of these defects [58], [59], [64], [81], [87]–[89]. Because low cost, low capex, and high efficiency are all required for manufacturing growth sufficient to reach PV deployment targets for climate change mitigation, continuing the trend toward higher efficiency in these materials is critical.

This thesis presents a model for the electrical activity of grain boundaries and dislocations, including the recombination and charging associated with these defects. This model is implemented into three-dimensional technology computer aided design (TCAD) simulations of several advanced solar cells to determine what the effects of these defects are, the materials requirements to reach high efficiency in each architecture, and what device design attributes mitigate the presence of these defects. It is shown that Si with dislocations and grain boundaries

can approach the performance of monocrystalline Si as long as the concentration of metal impurities decorating the crystal defects is relatively low. It is also shown that features of device design that increase the relative concentration of injected charge carriers, like thinner wafers, excellent surface passivation and passivated contacts, and light doping improve performance in the presence of these defects.

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CHAPTER

2

DISLOCATIONS AND GRAIN BOUNDARIES IN SILICON

2.1 Density of States at Dislocations in Silicon

A dislocation is a one-dimensional (1-D) disturbance of the crystal lattice of a solid. It is typically described as either an insertion or removal of a half-plane of atoms (edge-type dislocation) or a distortion of two lattice planes (screw-type dislocation) such that by taking equal steps around a circuit in different lattice directions, the final point is different from the starting point (Figure 2.1) [90], [91]. The vector from the end point of such an incomplete circuit to its starting point is called the Burgers' vector (***b***), and is often used to characterize dislocations.

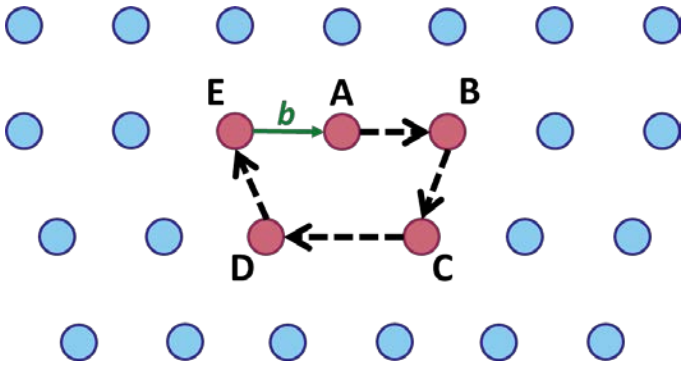

Figure 2.1. Schematic of an (edge-type) dislocation. The blue circles represent atoms in the crystal lattice, and the red points represent a circuit (ABCDE) which does not return to its starting point. The black dashed arrows represent equal steps (AB, BC, CD, DE—one lattice site per step) taken in the lattice plane shown. The circuit ending at E and not A represents the presence of a dislocation (in this case, an extra half-plane of atoms inserted above, and including, A). The green solid arrow represents the Burgers' vector (***b***), which is used to characterize dislocations. It is the vector from the end to the start of the incomplete circuit. Figure adapted from Ref. **[91]**.

The set of points at which the lattice distortion occurs is called the dislocation core, and the vector connecting these points is called the dislocation line. When such a structure is introduced in the lattice of a Si crystal, there are unsatisfied Si-Si bonds at the dislocation core. The electrons associated with these unsatisfied bonds can either bond to each other in a process called dislocation core reconstruction [90], [92], bond to impurity atoms (often metals) in the Si crystal [90], [93], [94], or remain unsatisfied or "dangling" (typically when there is a change in the vector of a dislocation line or "kink") [90]. Dangling bonds and many metal impurities introduce energy states deep within the band gap of silicon [90], [95]–[98]. Metal impurities can also accumulate in the strain field around the dislocation core or precipitate at energetically favorable nucleation sites at the dislocation core [99], [100].

Bond reconstruction typically leads to shallow (75–100 meV) 1-D bands of energy levels that can be occupied by electronic charge carriers extending into the band gap from the edges of the valence and conduction bands [90], [92], [95]. As stated above, metal point defects, metal precipitates, and dangling bonds introduce energy levels deep within the band gap. Thus, the density of states that can be occupied by electronic carriers at dislocations resembles the one shown in Figure 2.2.

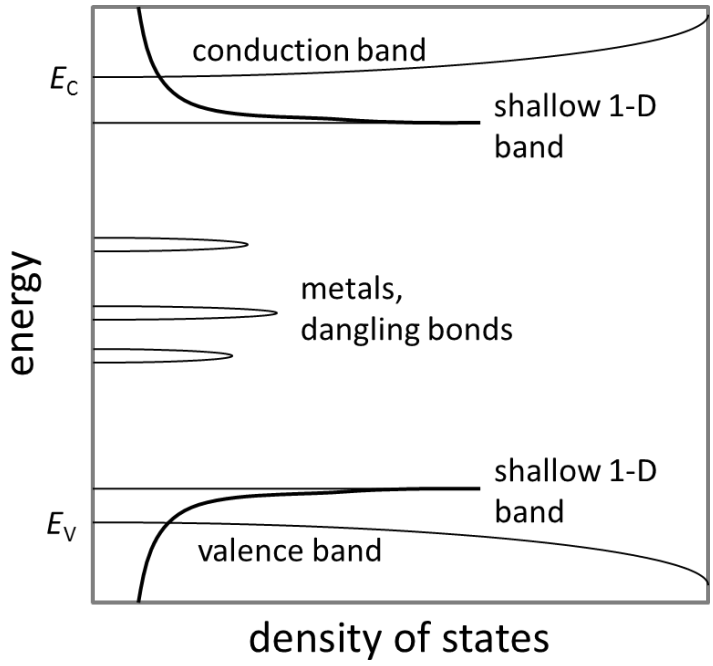

Figure 2.2. Density of states that can be occupied by electronic charge carriers (electrons and holes) present at typical dislocations in silicon. Figure adapted from Ref. **[92]**.

It has been shown that at room temperature (and the range of temperatures around it that includes the typical operating temperatures of Si solar cells) that recombination at dislocations is dominated by electronic transitions through states deep within the band gap [95], [101], [102]. It has further been shown that these states are predominantly associated with metal impurities rather than dangling bonds [73], [74], [101]. However, the presence of shallow states, and particularly the occupation of these states by (predominantly majority) charge carriers has a significant impact on the recombination rate through nearby deep levels and can directly influence the behavior of electronic devices made with Si wafers containing dislocations.

2.1.1 Extension of Dislocation Model to Grain Boundaries

It has been shown that grain boundaries, particularly small-angle grain boundaries that are especially detrimental in mc-Si solar cells, can be thought of structurally as arrays of dislocations [72], [103]–[105]. Further, it has been shown that the recombination activity of small-angle grain boundaries is localized to individual dislocations [72]. Thus, it is not surprising that material properties that increase either the density of dislocations or the concentration of metals at a grain boundary increase its recombination activity. This relationship has been shown experimentally [106]–[113].

2.2 Previous Dislocation and Grain Boundary Models

Because of their importance in determining the performance of mc-Si solar cells, a variety of models exist for the impact of dislocations and grain boundaries on Si wafers and Si solar cells. Almost all of these models involve the use of a single parameter that defines the recombination rate at the crystal defect. For dislocations, this parameter is the line recombination velocity or recombination strength, γ, which has unit of cm^2/s. For grain boundaries, the parameter is the surface recombination velocity, *SRV*, which has units of cm/s.

The most popular model for dislocations was introduced by Donolato [114]. Based on earlier work by Lax [115], he derived an analytical solution for the recombination rate at a dislocation with arbitrary γ in a semi-infinite Si wafer in low-injection. This model has two parameters: γ and a background lifetime for the Si wafer, τ_0. He also related the recombination rate in his model to the fraction of carriers that would be collected by a nearby junction, and therefore to an electron-beam-induced current (EBIC) contrast. Riepe *et al*. extended this model to finite

domains [116]. Budhraja *et al*. [117] extended a similar model from Van Opdorp *et al*. [118] to include effects of wafer surfaces with finite *SRV*. Kittler *et al*. [102] analyzed dislocation recombination to explain EBIC contrast measurements using Shockley-Read-Hall (SRH) statistics [119], [120], assuming low-level injection. Kveder *et al*. introduced a more detailed model for dislocation recombination and charging [95]. This model solved self-consistently for the emission and capture of electrons and holes using the full density of states, with rate equations built up from first principle analyses. This model is similar to one proposed earlier by Wilshaw and Booker [121], but better accounts for capture and emission by shallow states within the band gap. Due to the number of rate equations that need to be solved in this model, it was only applied to analysis of EBIC contrast and a constant minority carrier density far from the dislocation was assumed rather than incorporating the dislocation model into a finite element simulation.

There are relatively few applications of these models in numerical simulations of large-area structures, and almost none of full solar cells. Sopori [122], [123] used an analytical model to determine diode parameters for a dislocation-free region of a solar cell and a region containing a dislocation cluster. He then used a parallel diode model with finite resistance to consider the effects of different distributions of these clusters. However, he only used one set of diode parameters for each region and used a lower photocurrent in the region containing the dislocation.

Both analytical and numerical models have been applied to grain boundaries as well. In many of these models, grain boundary electrical activity is determined solely by an *SRV* and the local minority carrier concentration. This approach mirrors the one taken by Donolato and similar authors with dislocations. In both cases, the effect of grain boundary charging is neglected. This model has the advantages of simplicity and relatively easy extraction of its key parameters [124]–[128]. Stokkan *et al*. combined recombination velocity models for dislocations and grain boundaries with the recombination velocities determined by the structural properties of the defects [103]. They incorporated this model into 2-D finite element simulations of carrier diffusion and fit the results to experimental maps of excess carrier density. By assuming the recombination velocities were determined by a single-level mid-gap defect, they estimated the capture cross-section of such a defect. Other authors incorporated these types of models into analytical (diffusion length or lifetime-based diode models) [129] or finite element simulations

of full devices, though they typically focused on small-grained thin-film polycrystalline silicon [130].

Several models include the effects of grain boundary charging, either through the use of the SRH model for mid-gap defect states, an assumption of charging based on the Fermi level and the assumed defect level, or the inclusion of shallow acceptors at grain boundary attributed to pipe diffusion of dopants. These models have been applied to measurements of local recombination in Si wafers like EBIC [112]. They have also been applied to simulations of full devices. However, most of these simulations were focused on thin-film small-grained Si solar cells [131]–[134]. They therefore consider very thin devices (10 μm or less), small grains (less than 5 μm), and low background lifetimes (1 μs or less). The emitter profiles and other device features were not consistent with current industrial parameters, advanced industrial parameters or pre-commercial parameters for wafer-based mc-Si solar cells. Furthermore, these authors made no modifications to the SRH parameters to account for the interaction of shallow defects with the deep defects.

Altermatt *et al*. [135], [136] simulated solar cells in 3-D (which they showed was necessary to avoid underestimating the impact of grain boundaries as discussed in Chapter 3.3.4) with grain boundaries whose electrical activity was governed by mid-gap defects obeying SRH statistics with a density of states determined using a defect-pool model. The defect-pool model shifts the density of states based Fermi level during processing (and doping concentration of the finished cell). They showed that such a model was applicable down to doping concentrations greater than 5×10^{15} cm^{-3}. The devices simulated were slightly thicker (30 μm) but still had lifetimes of 1 μs or less and cell architectures quite different from those for wafer-based mc-Si solar cells.

Full numerical simulations and parallel diode models of real devices have also been performed using different combinations of minority carrier lifetime or diffusion length for different grains [137]–[140]. However, the method for determining the appropriate parameters to use requires fitting device performance data for a given cell architecture.

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CHAPTER

3

PROPOSED MODEL FOR DISLOCATIONS AND GRAIN BOUNDARIES IN SILICON SOLAR CELLS†

3.1 Density of States and Recombination Statistics

As discussed in Chapter 2.2, Kveder *et al*. [95] presented and validated a model for the electrical activity of dislocations based on first principles analysis of carrier capture and recombination statistics for both clean dislocations and those decorated with metal impurities. Stokkan *et al*. [103] have shown that, from an electrical perspective, grain boundaries can be treated as arrays of dislocations. Bauer *et al*. [72] have shown that the recombination of dislocation arrays forming small-angle grain boundaries is the localized to the individual dislocations making up the arrays. They also contended that these defects are the most detrimental in solar cells made from "standard" mc-Si. Here "standard" implies that no seeding was used to influence the nucleation of grains in the silicon ingot. Currently, seeding is typically done either with large-area monocrystalline seeds, as in so-called "quasi-monocrystalline" silicon [71], [79], [142], or with small, randomly oriented seeds, as in so-called "high-performance" mc-Si [76].

Kveder's model involves transitions between many different energy levels. It was shown previously [135], [136] that a simplification to one single energy level near mid-gap can be

† Much of this Chapter is reproduced from Ref. [141] under a Creative Commons License (http://creativecommons.org/licenses/by-nc-nd/4.0/legalcode). The baseline device models were developed by H. Wagner and P.P. Altermatt.

effective if the grain size is not too small (smaller than usual in mc-Si material) and if the doping concentration is not too low (about 5×10^{15} cm^{-3} at the usual grain size of mc-Si material). This simplification may also have the advantage that it removes a degree of freedom of the input parameters (the energy distribution of defects) and therefore captures the dynamics of phenomena in a more straightforward way [136].

In this thesis, a similar approach is used. The electrical activity of dislocations and grain boundaries is modelled using a mid-gap defect with a single energy level whose recombination is governed by Shockley-Read-Hall (SRH) statistics [119], [120]. Both an acceptor and a donor are used in order to account for the presence of shallow 1-D bands extending from both the conduction and valence band edges. The enhanced recombination and band bending associated with metals decorating dislocations and grain boundaries is captured by applying transformations to the minority- and majority-carrier capture cross-section of the defect. Here, "minority" refers to electrons for the donor and holes for the acceptor. "Majority" refers to electrons for the acceptor and holes for the donor. This nomenclature refers to carriers that are expected to be in the minority and majority when each type of defect dominates recombination. This transformation depends on the line density of these defects along the dislocation, and is described by the following expressions:

$$\sigma'_{\text{majority}} = \sigma_{\text{majority}} \times a, \tag{3.1}$$

$$\sigma'_{\text{minority}} = \sigma_{\text{minority}} \times \frac{b}{N_{\text{DL}}}, \tag{3.2}$$

where a and b are parameters that can be adjusted to fit experimental data and N_{DL} is the line density of recombination centers along the dislocation.

The parameters a and b are fit, and the model is validated by comparing simulations with the model to Kveder's simulated results using the full density of states and the electron-beam-induced current (EBIC) experiments he used to fit the free parameters in his model. The technology computer aided design (TCAD) software Sentaurus Device [143] is used for the simulations. A two-dimensinal (2-D) domain (see Figure 3.1) is chosen to match Kveder's simulations and the experiments [101], [102]. This domain includes a 10 µm-thick Si wafer with a Schottky contact covering the whole of the top surface. A Schottky barrier height of 0.7 eV is used to match that of aluminium on Si. The simulated domain is 100 µm wide, although varying the width from 10 µm to 1000 µm does not affect the results. Doping densities of 5×10^{14} cm^{-3} and 1×10^{15} cm^{-3} are used to match the relevant experiments and Kveder's simulations. The

background lifetime of the Si wafer is set to 1 μs based on the reported concentrations of copper and nickel in the wafers used in the experiments and these impurities' known effects on carrier lifetimes in Si [96]. However, varying the background lifetime from 100 ns to 10 ms does not affect the results. All simulations are performed with the properties of Si at 300 K and compared to experiments and Kveder's simulations at this temperature. It is not expected that this model will be valid at significantly lower (*e.g.*, liquid nitrogen) temperatures.

Following the method of Schroder [144], We simulate the excitation due to the 30 keV electron beam used in the experiments as a circular area of diameter 6 μm with a constant generation rate (G) depending on the electron beam current (I_{beam}):

$$G = I_{\mathrm{beam}}(\mathrm{pA}) \times (4.55 \times 10^{20}\mathrm{pA}^{-1}\mathrm{cm}^{-3}), \tag{3.3}$$

A dislocation is introduced into the simulation as a 12.25 nm^2 region (the area of the strain field around the dislocation core) inside the electron-beam excitation volume. Mid-gap recombination centers are placed at the interface between this region and the surrounding silicon wafer with a density corresponding to N_{DL}. Note that while N_{DL} is a line density with units of cm^{-1} as is typical for describing dislocations as 1-D objects, the interface density of recombination centers is defined in Sentaurus as an areal density with units of cm^{-1}. This value is obtained by dividing N_{DL} by the perimeter of the box defining the dislocation (14 nm).

As inputs to the model described in equations (3.1) and (3.2), we use the set of defect parameters extracted by Kveder *et al.*, including N_{DL}, $\sigma_{\mathrm{minority}}$, and $\sigma_{\mathrm{majority}}$. A 2-D model is used because it requires significantly less computation time and fitting the free parameters requires many iterations. However, using a 3-D model with a spherical excitation volume and a rectangular prism rather than a square defining the dislocation changes the current by less than 5% relative. EBIC contrast is calculated using the current from a simulation that includes a dislocation and the current from an identical simulation in which the dislocation/bulk interface contains no defects.

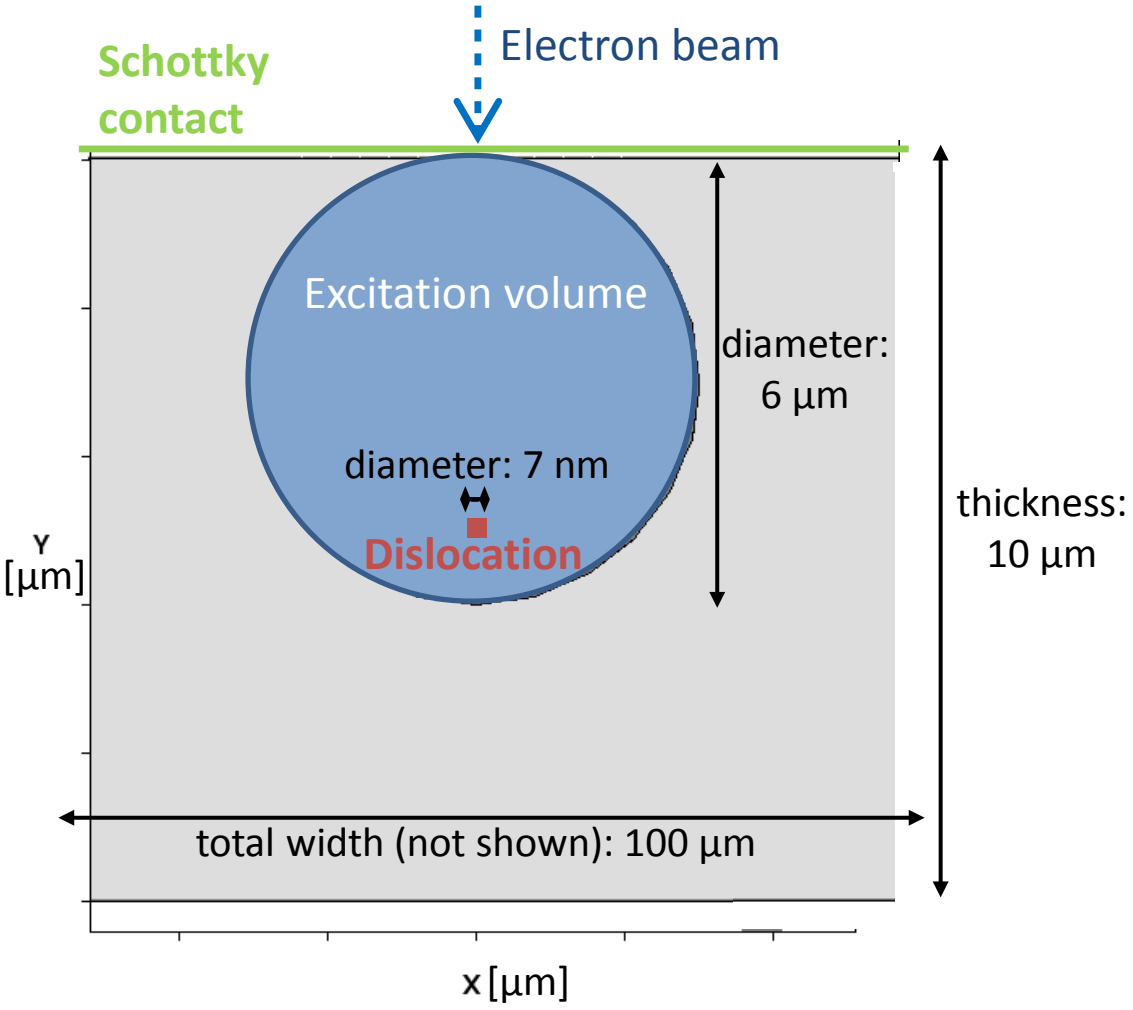

Figure 3.1. Schematic of domain for simulated EBIC experiment. The blue circle represents the excitation volume of carriers generated by the electron beam. The green line represents the semi-transparent Schottky contact on the front surface of the device. The full width of the domain is not shown but is 100 µm.

3.2 Parameter Fitting and Model Validation

The parameters a and b are varied to simultaneously fit EBIC contrast as a function of electron beam current (excess carrier density, Figure 3.2a) and N_{DL} (Figure 3.2b), as well as band bending around the dislocation (ΔE_C, Table 3.1). Good agreement is found for a = 1.4 (dimensionless) and b = 5.5×10^6 cm^{-1}. As shown in Figure 3.2a, we closely match the experimental EBIC contrast as a function of electron beam current (generation rate).

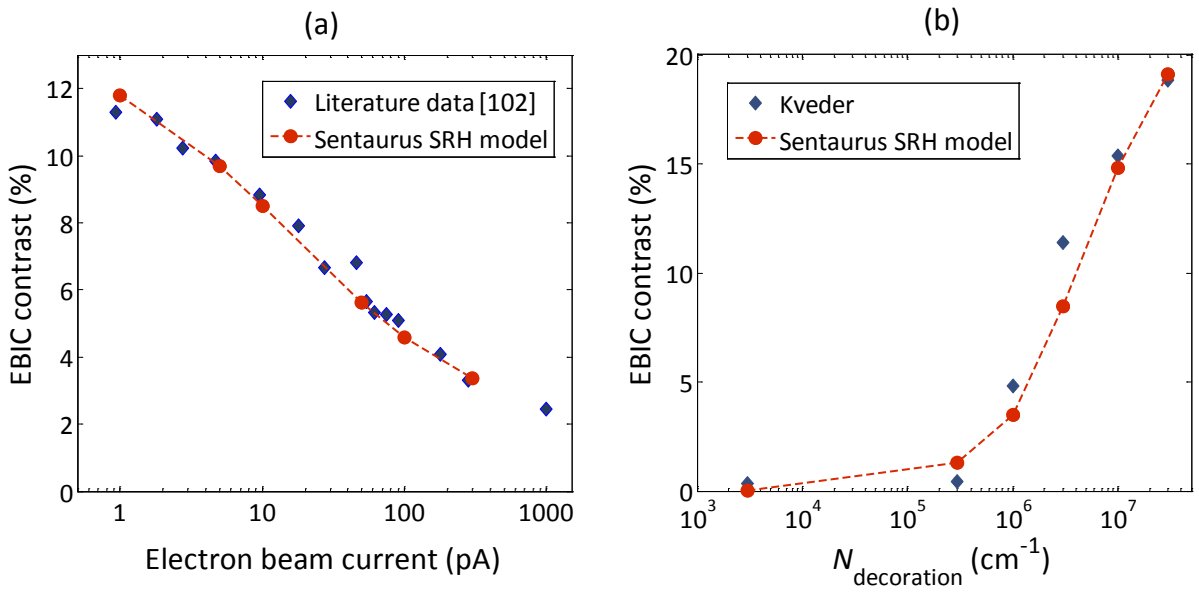

Figure 3.2. a) Simulated and literature **[102]** experimental data for EBIC contrast *vs*. electron-beam current; b) EBIC contrast *vs*. line density of impurities from Kveder's model and Sentaurus SRH model using Kveder's expression for minority carrier density as a function band bending (from Sentaurus Device simulations). Figure reproduced from Ref. **[141]** under a Creative Commons License.

Table 3.1 compares band bending around the dislocation in Sentaurus simulations to values simulated by Kveder *et al*. Kveder assumed a constant minority carrier density at the edge of the depletion region around the charged dislocation. In Sentaurus Device, carrier concentrations are solved self-consistently at every point in the finite element mesh. There is significant spatial variation in excess carrier density in the simulated domain in Sentaurus because minority carriers are extracted through the Schottky contact, creating a depletion region near the top surface and a steady-state gradient in minority carrier density through the device thickness. The generation rate is adjusted so the peak hole density outside the dislocation space-charge region in the Sentaurus simulations matches Kveder's values.

Table 3.1. Band bending at dislocation from Sentaurus model and Kveder's model with varying defect properties.

N_{DL} (cm^{-1})	σ_{min} (cm^2)	σ_{min}' (cm^2)	σ_{maj} (cm^2)	σ_{maj}' (cm^2)	$\Delta E_{C,Kveder}$ (meV)	$\Delta E_{C,Sentaurus}$ (meV)
3.0×10^{7}	6.5×10^{-14}	1.2×10^{-15}	2.0×10^{-15}	2.8×10^{-15}	60	64
2.4×10^{6}	5.5×10^{-14}	1.3×10^{-14}	5.0×10^{-14}	7.0×10^{-14}	64	64
2.2×10^{5}	6.5×10^{-15}	1.6×10^{-13}	2.0×10^{-15}	2.8×10^{-15}	4	2

A similar issue arises with the comparison of EBIC contrast as a function of N_{DL}. Kveder *et al*. calculated EBIC contrast solely from the recombination rate at the dislocation. In Sentaurus, the current is determined by the full solution of the Poisson equation and the continuity equations for electrons and holes at every point in the finite element mesh. As with the band bending, these results do not agree. However, the band bending from the Sentaurus simulations can be inserted into Kveder's expression for the minority hole density around the dislocation core as a function of band bending:

$$p_{\mathrm{DL}} = p \times \exp\left(q\,\Delta E_{\mathrm{C}} / k_{\mathrm{B}}T\right), \tag{3.4}$$

where p_{DL} hole density near the dislocation core, p is the hole density in the bulk wafer, q is the electron charge, k_B is Boltzmann's constant, and T is temperature. Using this minority carrier density, the recombination rate (R) can be calculated using SRH statistics with the modified capture cross-sections from Equations (3.1) and (3.2) as:

$$R = \frac{4\pi r^2 N_{\mathrm{DL}}\, v_{thh}\, v_{the}\, \sigma_{maj}\, \sigma_{maj}(n\, p_{\mathrm{DL}} - n_i^2)}{v_{the}\, \sigma_{maj}\left(n + N_{\mathrm{C}} \exp\left(E_t - E_t / k_{\mathrm{B}}T\right)\right) + v_{thh}\, \sigma_{min}\left(p_{\mathrm{DL}} + N_V \exp\left(E_t - E_t / k_{\mathrm{B}}T\right)\right)}, \tag{3.5}$$

where r is the radius of the strain field around the dislocation core in cm, v_{thh} and v_{the} are the thermal velocity of holes and electrons respectively, n is the majority electron concentration equal to the excess carrier density plus the dopant concentration, n_i is the intrinsic carrier concentration, N_C and N_V are the effective densities of states in the conduction and valence bands respectively, E_C and E_V are the conduction band minimum and the valence band maximum energies respectively, and E_t is the energy level of the mid-gap recombination center. If this recombination rate is converted to EBIC contrast (C) using Kveder's method:

$$C = 0.2\,\frac{R}{D\,p}, \tag{3.6}$$

where D is the diffusivity of holes, the results agre $D\ p$ e with Kveder's (Figure 3.2b).

3.3 Solar Cell Models

3.3.1 Unit Cells in Device Simulations

Solar cells are large-area devices with lateral dimensions typically on the order of cm. However, they have gradients in carrier and current density that can be large on the order of nm

(in the emitter, for example, which in a typical homojunction cell is on the order of 100 nm thick and in a typical heterojunction cell, 10 nm). Therefore, reducing the size of the domain of the simulation is critical to enable a solution in a reasonable amount of time. In all of the simulations in this thesis, reflective boundary conditions are used for all lateral dimensions (*i.e.*, not thickness). Reflective boundary conditions produce reflective symmetry across the boundary. It is as if there is a mirror image of the simulated domain next to it in all lateral directions, and this pattern repeats infinitely. In order to make this appropriate, the simulated domain must terminate in lateral directions at a line of symmetry in the device. Since the fingers used in solar cell metallization patterns are periodic, they make appropriate symmetry points. In this thesis, the lines of symmetry are always the mid-point of a metal finger or the point halfway between two metal fingers. Schematics of the devices simulated below help illustrate this point, as does Figure 3.8.

3.3.2 Devices Simulated

For an overview of contemporary numerical simulations of solar cells, see Refs [145], [146]. In this thesis, four types of solar cells are simulated (Figure 3.3 and Figure 3.4). Three are used to consider broadly the effects of dislocations and grain boundaries on different types of solar cells, and one is used to validate the defect model for grain boundaries. All four have a *p*-type Si base doped with boron. The first is a standard industrial cell with a full-area rear contact and aluminum back surface field. This cell will be referred to as an "Al-BSF" cell. The Al-BSF cell has a phosphorus-doped diffused emitter with selective doping under the front contacts. The second cell is a passivated emitter, rear totally diffused (PERT) cell. It has an identical front to the Al-BSF cell, but the rear side has local contacts with a passivating dielectric between them. In 2-D, the rear contact is a line contact similar to the grid on the front side. In 3-D, it is simulated as a square contact. The PERT structure is typically used for *n*-type cells due to their lower base doping. It is used here because the rear side of the PERT and heterojunction cells are the same, and the heterojunction is much more lightly doped for better band alignment of the base and heteroemitter. As just mentioned, the third cell is a heterojunction with an identical rear side to the PERT cell. It has an *n*-type gallium phosphide (GaP) emitter on the front side. The simulated mobility and doping concentration of the GaP are sufficient that it does not have (or require) a transparent conducting oxide (TCO) on the top of the emitter. GaP is used here rather

than a more typical hydrogenated amorphous Si (a-Si:H) cell because the primary goal is to explore difference between heterojunction and homojunction cells. a-Si is far from an ideal heterojunction partner for crystalline Si. GaP is used instead so that optimize parasitic absorption, band alignment, and conductivity can be optimized. Key parameters for these models are listed in Table 3.2 These solar cell models were not developed as part of this thesis; they are based on previously published work [145], [147].

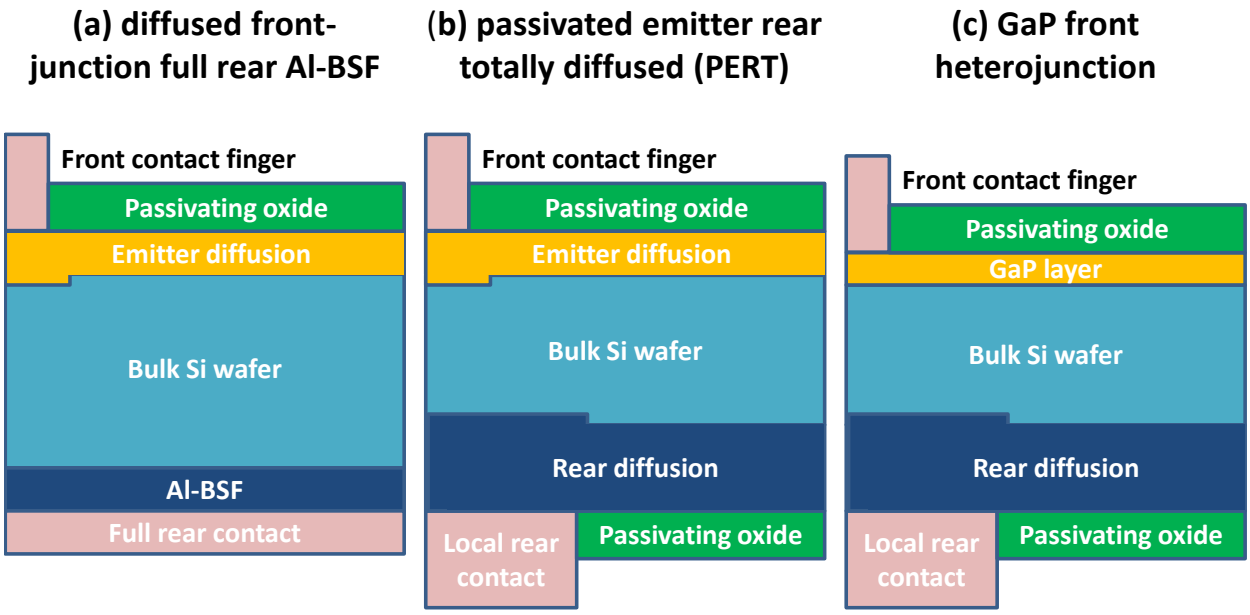

Figure 3.3. Schematic diagrams of the simulated domain of three solar cells simulated in this thesis. a) Al-BSF cell with a selective diffused emitter on the front side and a full rear contact with aluminum back surface field. The simulated domain extends from the midpoint of one front contact finger halfway to the next finger. b) PERT cell with identical front side to the Al-BSF cell and local rear contacts with a selective diffusion above them and passivating dielectric between them. The simulated domain extends from the midpoint of both the front and rear contacts halfway to the next contacts. In 3-D, the rear contacts are simulated as squares rather than lines. c) Heterojunction cell with GaP heterojunction on the front side and an identical rear side to the PERT cell.

Table 3.2. Key parameters for solar cells simulated.

Parameter	BSF	PERC	Heterojunction
Base doping	7×10^{15} cm^{-3}	7×10^{15} cm^{-3}	6×10^{14} cm^{-3}
Emitter peak doping concentration	5×10^{19} cm^{-3}	5×10^{19} cm^{-3}	2×10^{20} cm^{-3}
Emitter depth	700 nm	700 nm	10 nm
Rear peak doping concentration	5×10^{18} cm^{-3}	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
Rear doping depth	1 µm	5 µm	5 µm
Surface Recombination Velocity	1000 cm/s	1000 cm/s	1000 cm/s
Bulk lifetime	1 ms	1 ms	1 ms
GaP lifetime	N/A	N/A	100 ns
GaP mobility	N/A	N/A	27 cm^2/Vs (e^-) 13 cm^2/Vs (h^+)

For the experimental validation of the grain boundary model (Chapter 5.3), standard Si/a-Si:H heterojunction (SHJ) solar cells were fabricated by the Holman Research Group at Arizona State University. In order to simulate the effects of grain boundaries on these cells, a Sentaurus model for SHJ cells was required. A model developed at the Solar Energy Research Institute of Singapore is used [148]. Parameters from this model are adjusted to match those used by Filipič *et al*. [149], which better match the experimental devices, as well as to fit the performance of a cell fabricated on a control Cz-Si wafer B-doped to 1.5×10^{18} cm^{-3} with a bulk lifetime of about 1.5 ms. These devices contain a *p*-type Si wafer with an intrinsic a-Si:H layer on both the front and the back, an *n*-type a-Si:H layer on the front to act as heteroemitter, a *p*-type a-Si:H layer on the rear, degenerately doped indium tin oxide (ITO) on both the front and the rear as a conductive window layer and anti-reflective coating with a Ag grid (5 fingers and one bus bar on the front side) and a full-area Ag contact on the rear side (see Figure 3.4). Following Filipič *et al*., the ITO is simulated as a conductor rather than a semiconductor with resistivity (ρ) determined by the doping density (N_D) and a mobility (μ) of 30 cm^2/Vs, using the relation $1/\rho = q\mu N_D$ where q is the electron charge.

The cells are planar (*i.e.*, not surface-textured), and the optical generation profile used in Sentaurus is simulated in OPAL 2 [150] using the full front layer stack under normal illumination with the AM1.5G spectrum and the default light-trapping model [151]. Effects of

contact shading are added after the fact by shifting the *J-V* curve down to match the measured J_{SC}.

The cells are 1 cm square and had a single grain boundary in them. To simulate this structure, a 5 mm simulated domain that included half of the contacts is used. A schematic of this structure is shown in Figure 3.4. Table 3.3 shows the key parameters used in these simulations. a-Si:H is a highly defective material with defects deep in the band gap associated with dangling bonds and bandtails with an exponential energetic distribution from the valence and conduction band edges. The parameters used to simulate these defects are listed in Table 3.4. The energetic distribution of traps is assumed to be Gaussian for the deep defects and exponential for the bandtails, described by the equations $N_t(E) = N_0 \exp(-(E-E_0)^2/(2E_S^2))$ and $N_t(E) = N_0 \exp(-|E-E_0/E_S|)$, respectively. Recombination at the interface between the Si wafer and the *i*-a-Si:H layer is also modeled with a Gaussian distribution of mid-gap defects, whose parameters are listed in Table 3.4.

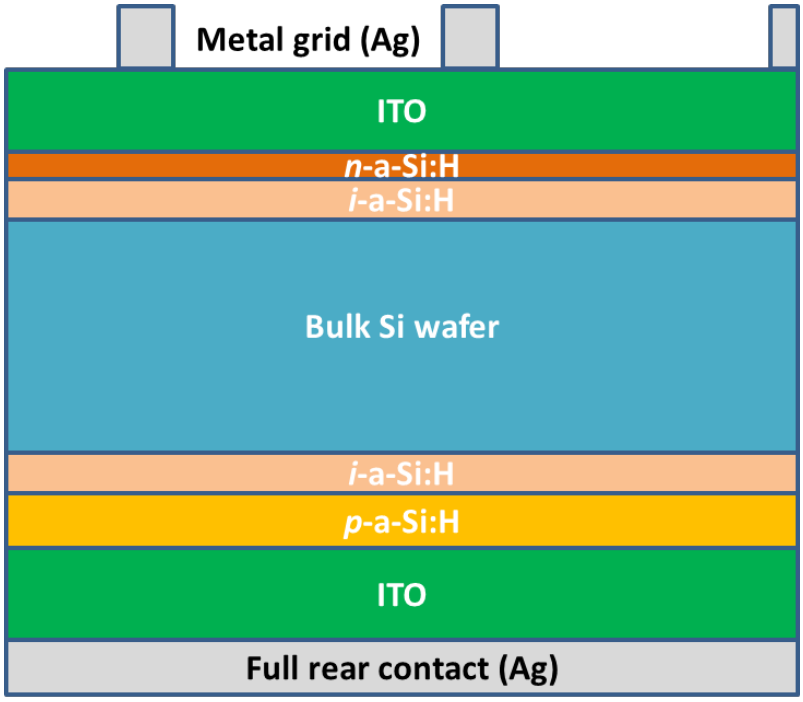

Figure 3.4. Schematic diagram of SJH solar cells simulated domain for comparison to experimental devices fabricated at Arizona State University. Both sides have an intrinsic a-Si:H layer under a doped a-Si:H layer and an ITO layer. The front side has a 5-contact metal grid, half of which is included in the simulated domain. The rear has a full area Ag contact. Schematic is not to scale.

Table 3.3. Key parameters for silicon heterojunction simulations.

Parameter	Value
i-a-Si:H thickness	6 nm
n-a-Si:H thickness	4.5 nm
p-a-Si:H thickness	10 nm
Si wafer thickness	180 μm
Front ITO thickness	130 nm
Rear ITO thickness	240 nm
n-a-Si:H doping	1×10^{19} cm^{-3}
p-a-Si:H doping	1×10^{19} cm^{-3}
Front ITO doping	2.6×10^{20} cm^{-3}
Rear ITO doping	1.7×10^{20} cm^{-3}
ITO mobility	30 cm^2/Vs

Table 3.4. Parameters for a-Si:H defect levels.

Parameter	*n*-a-Si:H	*i*-a-Si:H	*p*-a-Si:H	a-Si/Si interface
$N_{0,\text{deep}}$	5×10^{17} cm^{-3}	5×10^{15} cm^{-3}	5×10^{17} cm^{-3}	3×10^{11} cm^{-3}
$N_{0,\text{CB tail}}$	3×10^{18} cm^{-3}	3×10^{18} cm^{-3}	3×10^{18} cm^{-3}	N/A
$N_{0,\text{VB tail}}$	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}	N/A
Deep acceptor E_0	E_V + 0.7 eV	E_V + 0.9 eV	E_V + 0.8 eV	E_C - 0.46 eV
Deep donor E_0	E_V + 0.5 eV	E_V + 0.7 eV	E_V + 1.0 eV	E_V + 0.46 eV
Deep acceptor E_S	0.22 eV	0.22 eV	0.22 eV	0.2 eV
Deep donor E_S	0.22 eV	0.22 eV	0.22 eV	0.2 eV
Deep acceptor σ_n / σ_n	10^{-14} / 10^{-15} cm^{-3}	10^{-14} / 10^{-15} cm^{-3}	10^{-14} / 10^{-15} cm^{-3}	1.9×10^{-17} / 1.9×10^{-18} cm^{-3}
Deep donor σ_n / σ_n	10^{-15} / 10^{-14} cm^{-3}	10^{-15} / 10^{-14} cm^{-3}	10^{-15} / 10^{-14} cm^{-3}	1.9×10^{-18} / 1.9×10^{-17} cm^{-3}
Valence bandtail E_S	0.05 eV	0.05 eV	0.05 eV	N/A
Conduction bandtail E_S	0.03 eV	0.03 eV	0.03 eV	N/A
Valence bandtail σ_n / σ_n	10^{-15} / 10^{-16} cm^{-3}	10^{-15} / 10^{-16} cm^{-3}	10^{-15} / 10^{-16} cm^{-3}	N/A
Conduction bandtail σ_n / σ_n	10^{-16} / 10^{-15} cm^{-3}	10^{-16} / 10^{-15} cm^{-3}	10^{-16} / 10^{-15} cm^{-3}	N/A

3.3.3 Implementation of Dislocations[‡]

To simulate dislocations, a rectangular prism 4 nm square is introduced in the center of the simulated domain. 4 nm is chosen as typical of the size of the strain field around a dislocation core in Si. This prism passes through the entire silicon layer perpendicular to the plane of the wafer (Figure 3.5a), but not through the passivating dielectrics or the GaP emitter in the heterojunction cell. An areal concentration of mid-gap recombination centers is introduced at the interface between the prism and the rest of the Si wafer (Figure 3.5b). To match the traditional description of dislocations as line defects, this concentration is reported as a line density (N_{DL}) in units of cm^{-1}. N_{DL} is obtained by multiplying the areal density of recombination centers by the perimeter of the prism representing the dislocation. N_{DL} determines the charging and recombination rate of the dislocation. Since there is one dislocation in the simulated domain, the dislocation density is simply $1/x^2$, where x is the lateral dimension of the (square) simulated domain (Figure 3.5a). The dislocation density can then be varied by changing the size of the simulated domain.

This approach is similar to the one described for EBIC simulations in Chapter 3.1, however dislocations in solar cells have to be simulated in 3-D rather than 2-D because they typically propagate perpendicular to the plane of the wafer. The approach described for EBIC simulates a dislocation propagating parallel to the plane of the wafer. This direction is reasonable for the misfit dislocations in the EBIC experiments to which those simulations were compared, but not for Si wafers produced by any of the methods described in Chapter 3.1.

Because the size of the simulated domain is used to define the dislocation density, it no longer corresponds to the spacing between contacts. To account for this fact, the area of the contacts is adjusted, so that it is always the same fraction of the wafer area. This adjustment gives the correct contact recombination but does not address issues of series resistance losses between contacts or current crowding at the contacts, which are implicitly assumed to be negligible. Because the cells simulated all have highly conductive emitters that are fairly carrier selective,

[‡] Portions of this chapter have been submitted to *Solar Energy Materials and Solar Cells* and are reproduced here with permission from the publisher.

these effects can be safely ignored. This assumption is confirmed by comparing the efficiency (η), open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), and fill factor (FF) of simulations with N_{DL}=0 for all of the simulated domains. These factors vary by less than 1.5% relative as shown in Table 3.5.

The simulated domain described above is equivalent to a domain where the dislocation is in one corner and is cut at the midpoints of two sides of the rectangular prism in Figure 3.5b. This domain is used for the simulations in Chapter 4.3.

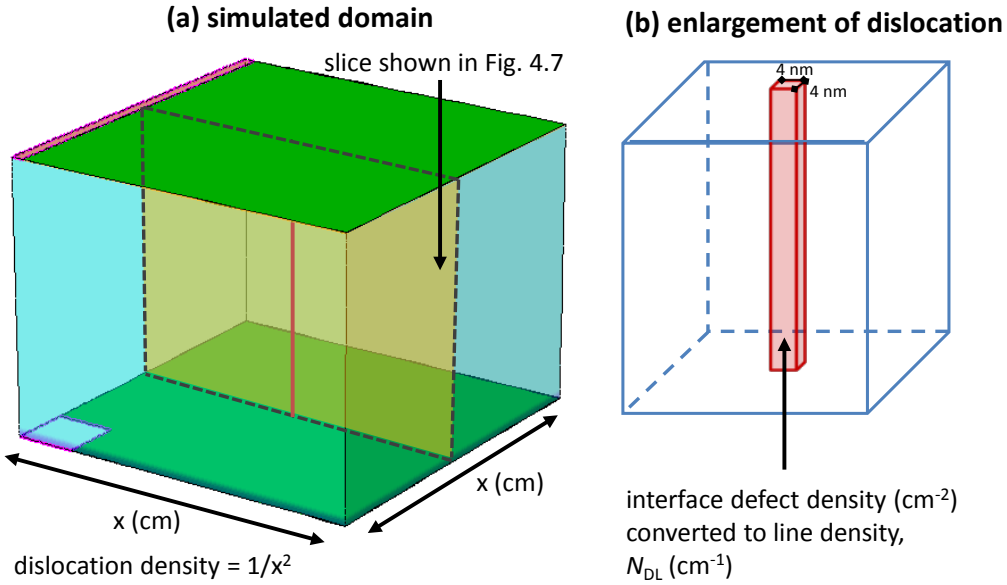

Figure 3.5. Schematic of dislocation simulation. (a) The simulated domain (always square), whose lateral dimensions determine the dislocation density. (b) Enlarged schematic of the dislocation itself, modeled as a rectangular prism within the Si wafer. The interface between this region and the Si wafer is populated with mid-gap recombination centers. The density of these defects is multiplied by the perimeter of the prism to give a line density of recombination centers, N_{DL}, with units of cm^{-1}.

Through the application of reflective boundary conditions, the simulations described above model dislocations homogeneously distributed throughout the cell. However, in real materials, dislocations tend to be clustered. The results from these simulations can be used to calculate current-voltage (*J-V*) curves for a solar cell containing dislocation clusters with a given dislocation density within the clusters ($DD_{cluster}$) in units of cm^{-2}, and a given N_{DL} (cm^{-1}) at each individual dislocation. We construct these *J-V* curves by taking a weighted average of the external current as a function of external voltage for the clusters and the dislocation-free regions

of the cell, using the fractional area covered by each region as weights. Mathematically, this can be expressed using the formula:

$$J_{cell}(V) = A_{DL} \times J_{DL}(V) + (1\text{-}A_{DL}) \times J_{clean}(V), \quad (3.7)$$

where V is voltage, $J_{cell}(V)$ is the current density for the whole device as a function of voltage, $J_{DL}(V)$ is the current density as a function of voltage within the dislocation cluster, $J_{clean}(V)$ is the current as a function of voltage for the dislocation-free region of the cell, and A_{DL} is the fraction of the total cell area containing dislocation clusters. This analysis relies on the assumption that the dislocation clusters are macroscopic, such that the area of interaction between each cluster and the dislocation-free region around it is much smaller than the area of either region individually.

Table 3.5. Comparison of cell parameters for different simulated domain widths with N_{DL}=0.

Cell Type	Domain Width (μm)	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)
Al-BSF	10	18.69	609.2	37.91	80.92
	20	18.75	609.5	38.02	80.91
	50	18.76	609.5	38.04	80.91
	100	18.78	609.6	38.09	80.89
	200	18.77	609.6	38.08	80.86
	500	18.70	609.6	38.06	80.60
PERT	10	21.73	673.3	39.82	81.07
	20	21.89	675.9	39.93	81.07
	50	21.93	676.4	39.96	81.11
	100	21.95	677.2	39.98	81.08
	200	21.95	677.3	40.00	81.02
	500	21.81	677.3	39.99	80.51
heterojunction	10	22.85	696.8	40.96	80.07
	20	22.91	699.0	40.96	80.02
	50	22.68	701.0	40.93	79.05
	100	22.93	700.9	40.94	79.93
	200	22.90	701.1	40.94	79.81
	500	22.68	701.0	40.94	79.05

This assumption is tested by comparing results from application of Equation (3.7) to a full parallel-diode model using Griddler 2.0 [152]. *J-V* curves for simulations of PERT cells without dislocations and with dislocation density of 10^6 cm^{-2} are fit to the two-diode equation [153]. The results of these fittings are then input into Griddler with area fractions of 10% and 50%. Figure 3.6 and Table 3.6 show the excellent agreement between these results and the results from Equation (3.7). Recent results from Haug *et al*. confirm that this result is quite general [154].

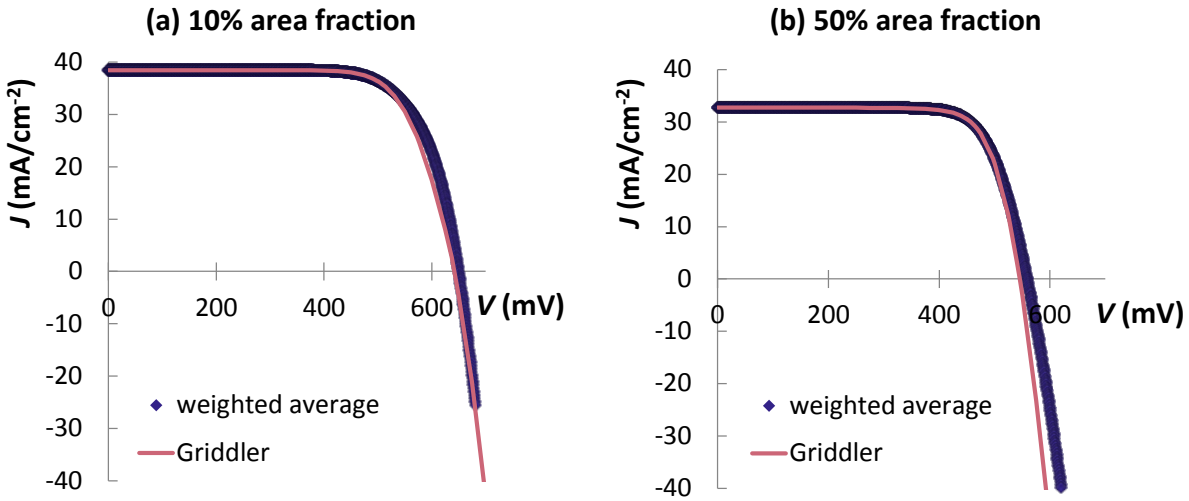

Figure 3.6. *J-V* curves for PERT cell with 10% and 50% coverage of dislocation clusters with dislocation density of 10^6 cm^{-2} simulated by taking the weighted average of the *J-V* curves of the dislocated and dislocation-free regions as described by equation (1) (purple diamonds) and a full parallel diode model using Griddler 2.0 (pink lines). Good agreement between weighted average and parallel diode simulations is reached.

Table 3.6. Comparison of weighted average and parallel diode simulations of dislocation clusters.

	Weighted average		**Griddler**		**Relative difference**	
	10% area fraction	50% area fraction	10% area fraction	50% area fraction	10% area fraction	50% area fraction
Efficiency (%)	18.25	13.77	18.18	13.75	0.4%	0.2%
V_{OC} (mV)	650.0	559.3	642.0	545.6	-0.2%	0.1%
J_{SC} (mA/cm^2)	38.41	32.79	38.48	32.77	1.3%	2.5%
***FF* (%)**	73.11	75.10	73.60	76.90	-0.7%	-2.3%

3.3.4 Implementation of Grain Boundaries

The grain boundary is implemented as a 2-D interface placed 2 nm from two of the edges of the simulated domain (Figure 3.7). This defect is populated with mid-gap recombination centers. The areal density of these recombination centers (N_{GB}) is determined using the approach of Stokkan *et al*. [103] to treat the grain boundary as an array of dislocations as described in Chapter 3.1. Stokkan calculates N_{GB} for a non-coincident site lattice grain boundary with a misorientation angle of θ (taken to be 2° for the simulations in this thesis) as:

$$N_{GB} = \frac{\pi}{2} {N_{DL}}^2 \times \frac{4\varepsilon \sin\left(\theta/2\right)}{B}, \tag{3.8}$$

where ε = 5.5 nm is the radius of the dislocation core for a grain boundary misoriented by 2° and B = 0.9035 Å is the magnitude of the Burgers' vector for a Shockley partial dislocation [90]. N_{GB} is then varied by varying N_{DL}, however this is equivalent to varying any of the other parameters. Square domains are chosen, so that the grains are also square and can be characterized by a single length.

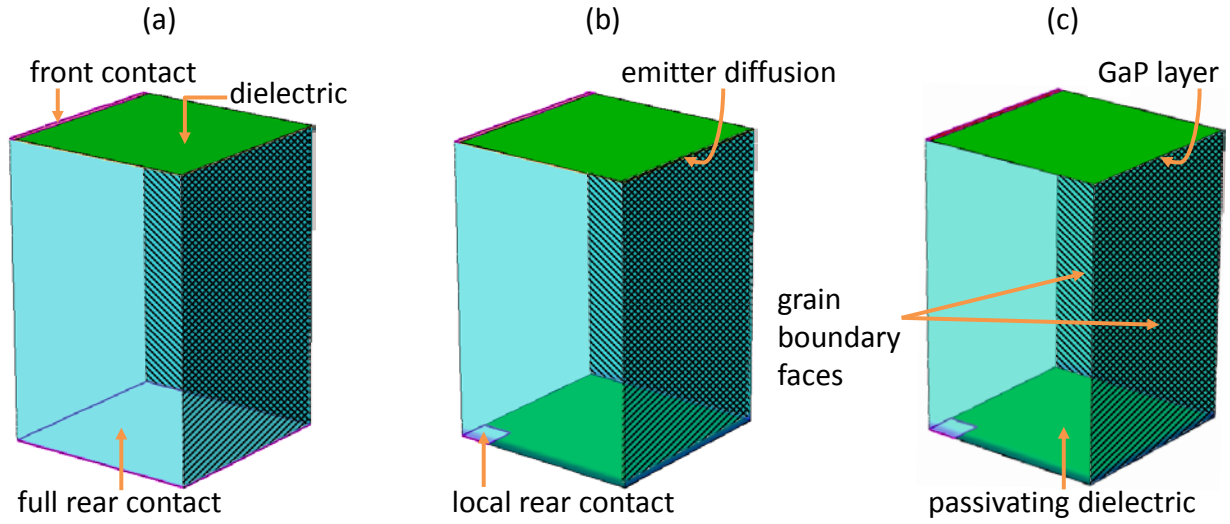

Figure 3.7. Schematics of the simulated domains. Grain boundaries are implemented as interface traps on the two right faces of the device (cross-hatched). Note that the interface is actually not the edge of the simulation domain but 2 nm from the edge. a) Al-BSF cell, b) PERT cell, (c) GaP/Si front heterojunction cell. Figure reproduced from Ref. **[141]** under a Creative Commons License.

This domain contains one fourth of one grain boundary. The boundary conditions guarantee that this is numerically equivalent to simulating an array of grains through reflective symmetry. A schematic illustrating reflection across one side of the boundary is shown in Figure 3.8. Throughout this thesis, the linear distance between parallel grain boundaries is referred to as "grain size" because it is a standard parameter for describing the density of grain boundaries within a wafer, and these simulations are of square arrays of grain boundaries. However, small-angle grain boundaries, which limit the performance of standard mc-Si, often terminate in the middle of a grain, and therefore a more appropriate term in this case might be "grain boundary spacing" or "inter-grain boundary distance."

As with the simulations of dislocations, the domain width is used to determine grain size rather than contact spacing. For grain sizes smaller than the contact spacing, the contact dimensions are again scaled down proportionally, resulting in changes to the device parameters of less than 4% relative for the Al-BSF cell, less than 1.5% relative for PERT and less than 1% relative for the heterojunction (Table 3.7).

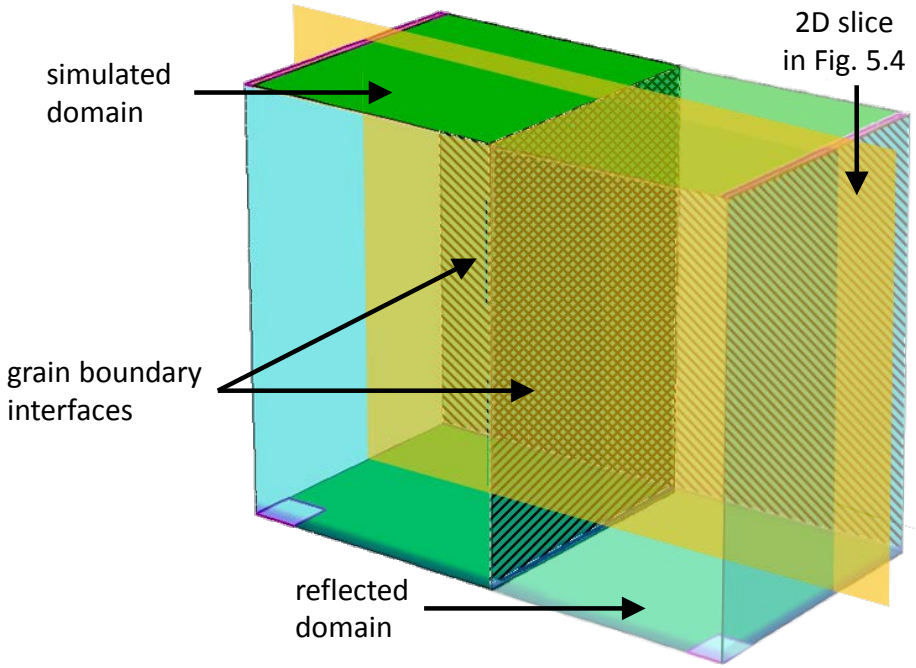

Figure 3.8. Simulated domain with reflection over one boundary: opaque prism on left is the simulated domain, transparent prism on right is one implied reflected domain. Cross-hatching shows grain boundary interfaces. Yellow surface shows slice shown in Figure 5.4. Figure reproduced from Ref. **[155]** © 2016 IEEE.

Table 3.7. Comparison of cell parameters for different simulated domain widths with N_{GB}=0.

Cell Type	Domain Width (μm)	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)
Al-BSF	10	19.26	609.2	38.51	82.08
	20	19.31	609.5	38.60	82.08
	50	19.73	615.0	39.05	82.18
	100	19.96	615.2	39.48	82.16
	200	19.33	609.6	38.67	82.03
	400	19.30	609.6	38.67	81.88
PERT	10	22.39	673.3	40.45	82.18
	20	22.54	675.7	40.57	82.23
	50	22.31	672.9	40.36	82.16
	100	22.42	674.7	40.45	82.16
	200	22.58	677.3	40.59	82.13
	400	22.51	677.4	40.61	81.84
heterojunction	10	23.52	696.8	41.60	81.14
	20	23.58	699.0	41.59	81.09
	50	23.61	700.5	41.59	81.04
	100	23.60	700.9	41.57	81.00
	200	23.57	701.1	41.58	80.87
	400	23.44	701.1	41.57	80.43

It has been shown previously [135] that columnar grains have to be simulated in 3-D rather than 2-D. In a 2-D simulation, carriers moving perpendicular to the simulated plane do not get closer to a grain boundary. However, in a real material with columnar grains, carriers moving parallel to a grain boundary approach another portion of that grain boundary, as illustrated in Figure 3.9. Therefore, the grain simulations described above are 3-D simulations that match a columnar grain structure. The exception is the SHJ simulations used to validate the grain boundary model by comparing to experimental devices. The experimental devices have exactly one grain boundary in them running linearly through the device. Therefore, they are correctly

simulated in 2-D with the grain boundary implemented as an interface 2 nm from the edge of the simulated domain.

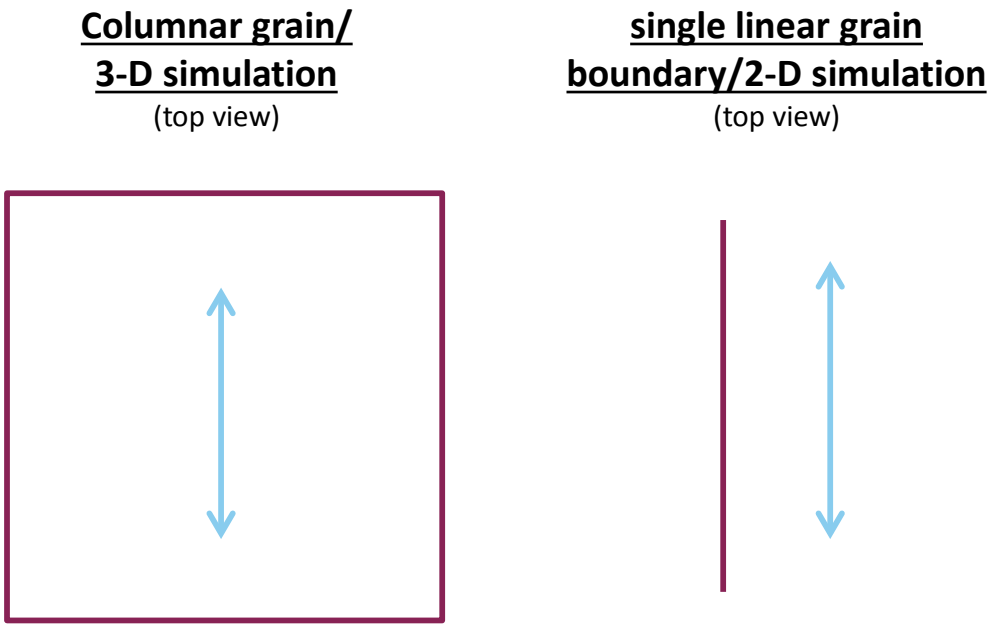

Figure 3.9. Grain boundary (red line) and carrier moving parallel to a grain boundary surface (blue arrow) in a 3-D simulation (left) and in a 2-D simulation (simulation). The 3-D case represents columnar grains and the 2-D case represents a single linear grain boundary.

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CHAPTER

4

EFFECTS OF DISLOCATIONS ON SILICON SOLAR CELLS[§]

4.1 Homogeneously Distributed Dislocations: Comparison to Historical Data

Simulated results for Al-BSF cells with dislocations included are compared with experimental data from literature [156]. Figure 4.1 shows simulated efficiencies as a function of dislocation density (x-axis) and N_{DL} (data series) as well as literature data. Reasonable agreement is oberved. The literature data falling across a range of N_{DL} is not surprising since the data include several Si growth techniques and only average dislocation density. Data slightly below the simulated curves is also reasonable, as the simulations assume a 1 ms minority carrier lifetime away from the dislocation, which may be higher than in the experimental devices.

[§] Much of this chapter has been submitted to *Solar Energy Materials and Solar Cells* and is reprinted here with permission from the publisher. The Trina Solar world record mc-Si solar cell was fabricated and measured by Z. Xiong and P.J. Verlinden. I performed the analysis of this data.

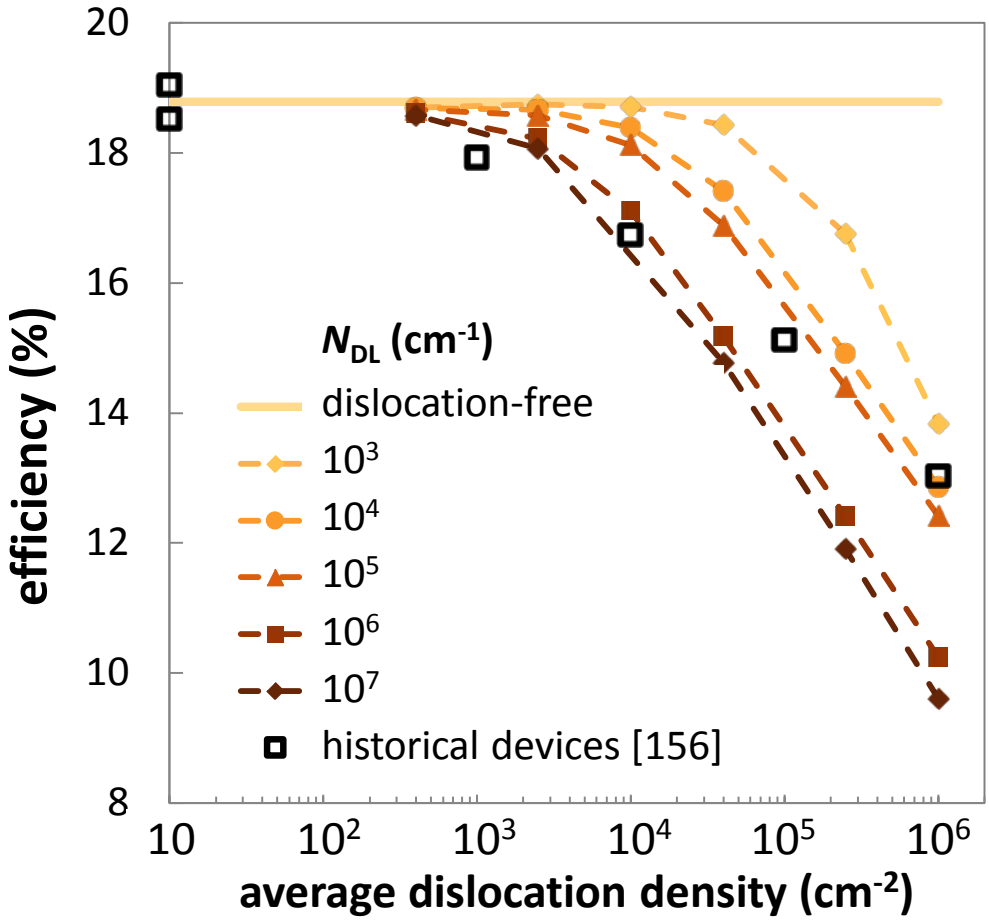

Figure 4.1. Efficiency of Al-BSF solar cells plotted *vs.* average dislocation density. Simulated efficiencies for a range of N_{DL} (data series) are compared with experimental results from literature **[156]**. There is good agreement between simulations and literature data.

4.2 Dislocation Clusters

Figure 4.2–Figure 4.5 show contour plots of efficiency, V_{OC}, J_{SC}, and *FF* as a function of $DD_{cluster}$ and the dislocated area fraction (A_{DL}) of the cell, for a range of N_{DL} from 10^3–10^7 cm^{-1} in both PERT and heterojunction cells (left and right panels). It is clear from these results that all three factors—A_{DL}, $DD_{cluster}$, and N_{DL}—are critical in determining the effect of dislocations on device performance.

To explicitly show the effect of clustering, lines of constant average dislocation density are also plotted in Figure 4.2–Figure 4.5 as blue dashed lines. These contours reveal the relative effect of clustered *vs.* homogeneously distributed dislocations: at low N_{DL}, these contours follow

the contours of cell efficiency, while at high N_{DL} they do not. Hence, at high N_{DL}, higher cell efficiencies are reached if the dislocations are clustered than if they are homogeneously distributed. Generally, clustering improves performance, however we reiterate that the effect is more pronounced at higher N_{DL}. This result contrasts with earlier simulations, which suggested clustered dislocations were worse [122], [123]. However, these simulations examined only a single pair of diode parameters for a dislocation-free and a dislocated region, and they assumed lower photocurrent generated in the dislocated region. This discrepancy highlights an advantage of the approach to modeling dislocations taken in this thesis. Because the model has microscopic properties embedded in it, it can be used to generate values for local diodes to use in circuit modeling. Having to guess at these values based on empirical data can make it unclear what the real relationship is between the local diode parameters and the dislocation cluster material properties.

For low $N_{DL}=10^3$ cm^{-1} (top row of Figure 4.2), cell efficiency does not improve when $DD_{cluster}$ is reduced below about 10^5 cm^{-2}. Below this value, recombination outside the base dominates the total recombination losses. The exact value for this plateau will depend on the specific device design. The heterojunction cell is more robust to the presence of dislocations than the PERT cell at low N_{DL} but performs worse at high N_{DL}. The robustness at low N_{DL} is attributed to the fact that the silicon wafer in the optimized [147] heterojunction cell is more lightly doped than in the optimized [147] PERT cell (6×10^{14} cm^{-3} *vs.* 7×10^{15} cm^{-3}), while the injection level at the maximum power point is much higher (5×10^{14} cm^{-3} *vs.* 10^{13} cm^{-3}) due to reduced recombination in the emitter, at the front surface, and in the front contact. This combination leads to a smaller fraction of the mid-gap recombination centers being occupied by majority carriers and reduced charging of the dislocations (Figure 4.6). This reduced charging decreases the size of the depletion region around the dislocations, reducing recombination at the defects. In contrast, at high N_{DL}, recombination through the dislocation pushes the heterojunction into low injection. Then, the lighter doping leads to a larger depletion region around the dislocations and to higher recombination. The injection level and relative size of the depletion region in these two cases is illustrated in Figure 4.7. It is notable that while heterojunction architectures are typically reserved for Cz-Si, these architectures can also maximize the efficiency of high-performance mc-Si and other high-lifetime materials whose performance is limited by dislocations.

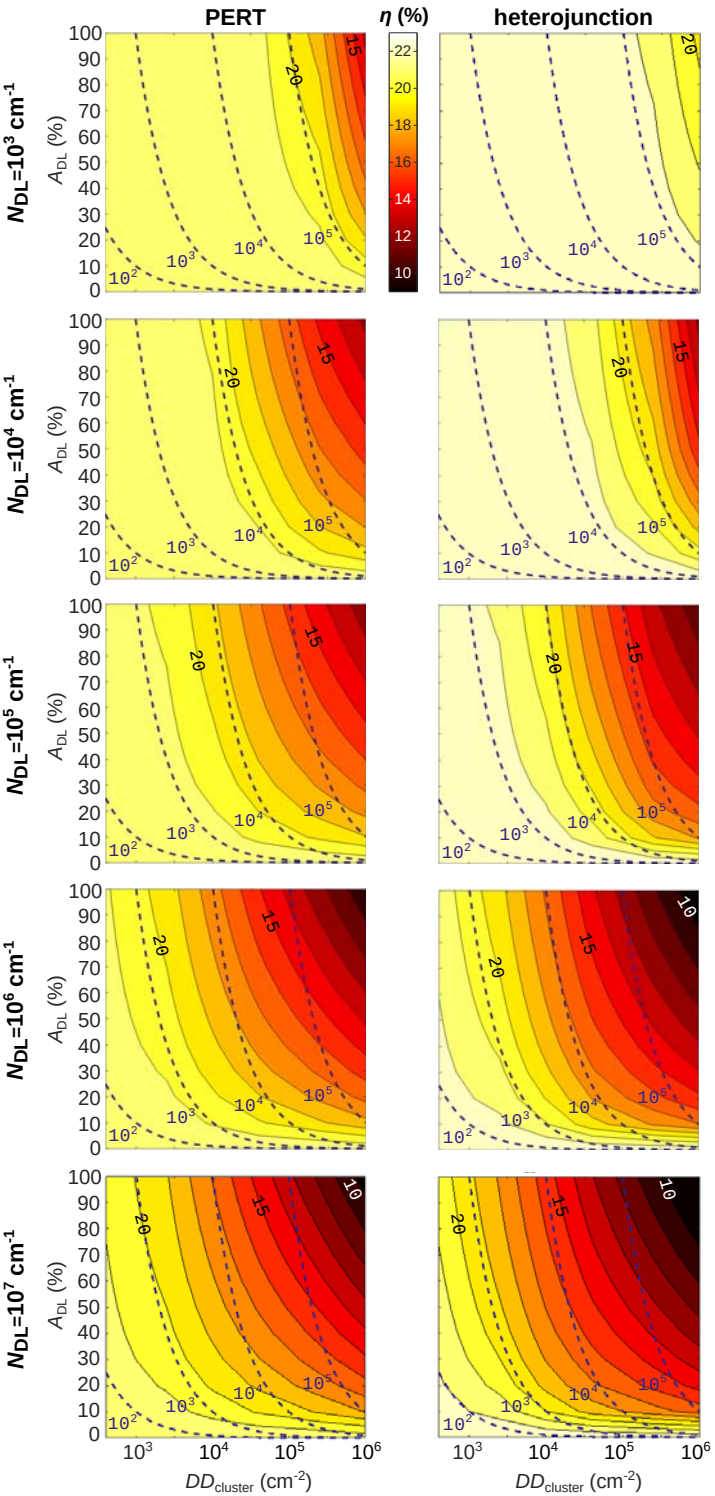

Figure 4.2. Contour plots of simulated efficiency as a function of dislocation density within dislocation clusters ($DD_{cluster}$) and dislocated area fraction (A_{DL}) of the cell for a range of N_{DL} (rows) in PERT (left column) and heterojunction (right column) solar cells. The heterojunction is more robust to the presence of dislocations at low N_{DL} and more sensitive to the presence of dislocations at high N_{DL}. Blue dashed lines indicate constant average dislocation density in the cell, showing that clustered defects have less impact than homogeneously distributed ones.

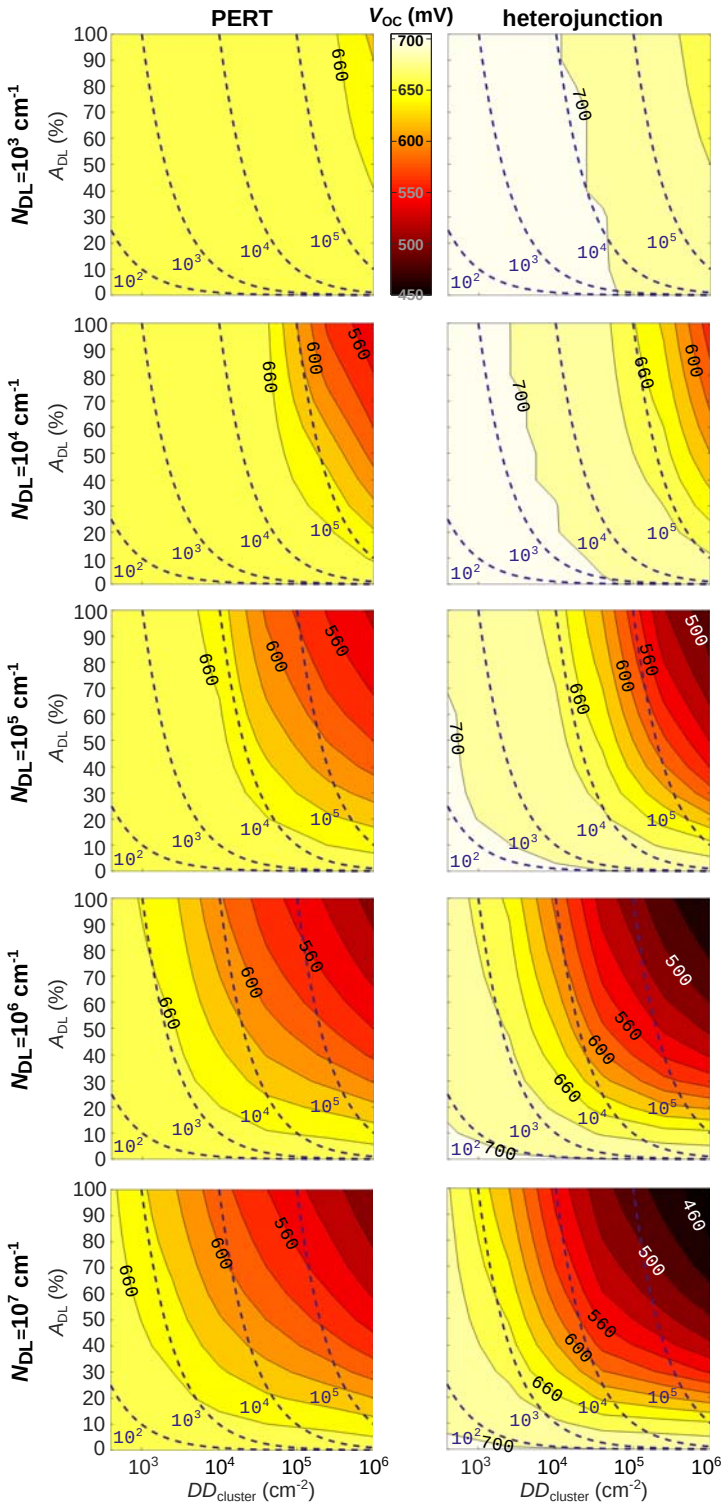

Figure 4.3. Contour plots of simulated V_{OC} as a function of $DD_{cluster}$ and A_{DL} of the cell for a range of N_{DL} (rows) in PERT (left column) and heterojunction (right column) solar cells.

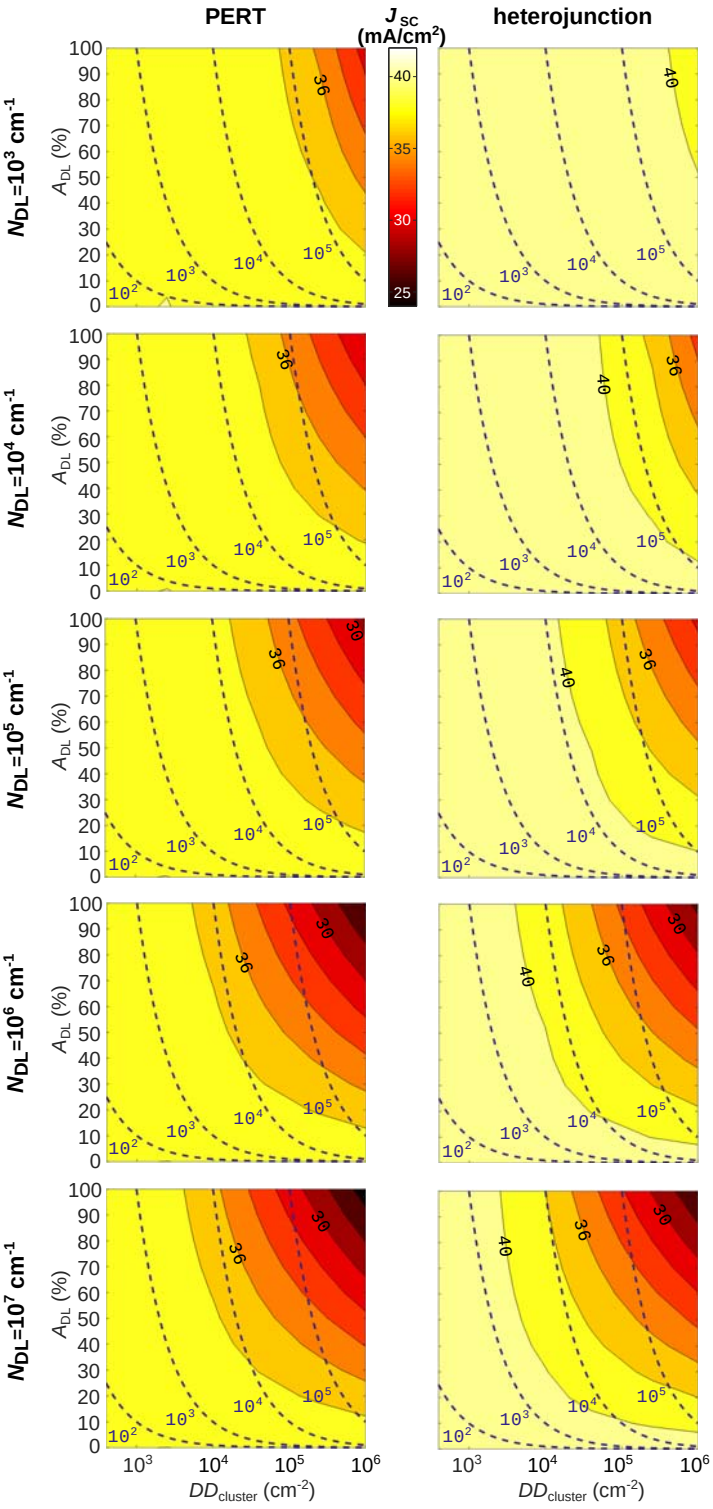

Figure 4.4. Contour plots of simulated J_{SC} as a function of $DD_{cluster}$ and A_{DL} of the cell for a range of N_{DL} (rows) in PERT (left column) and heterojunction (right column) solar cells.

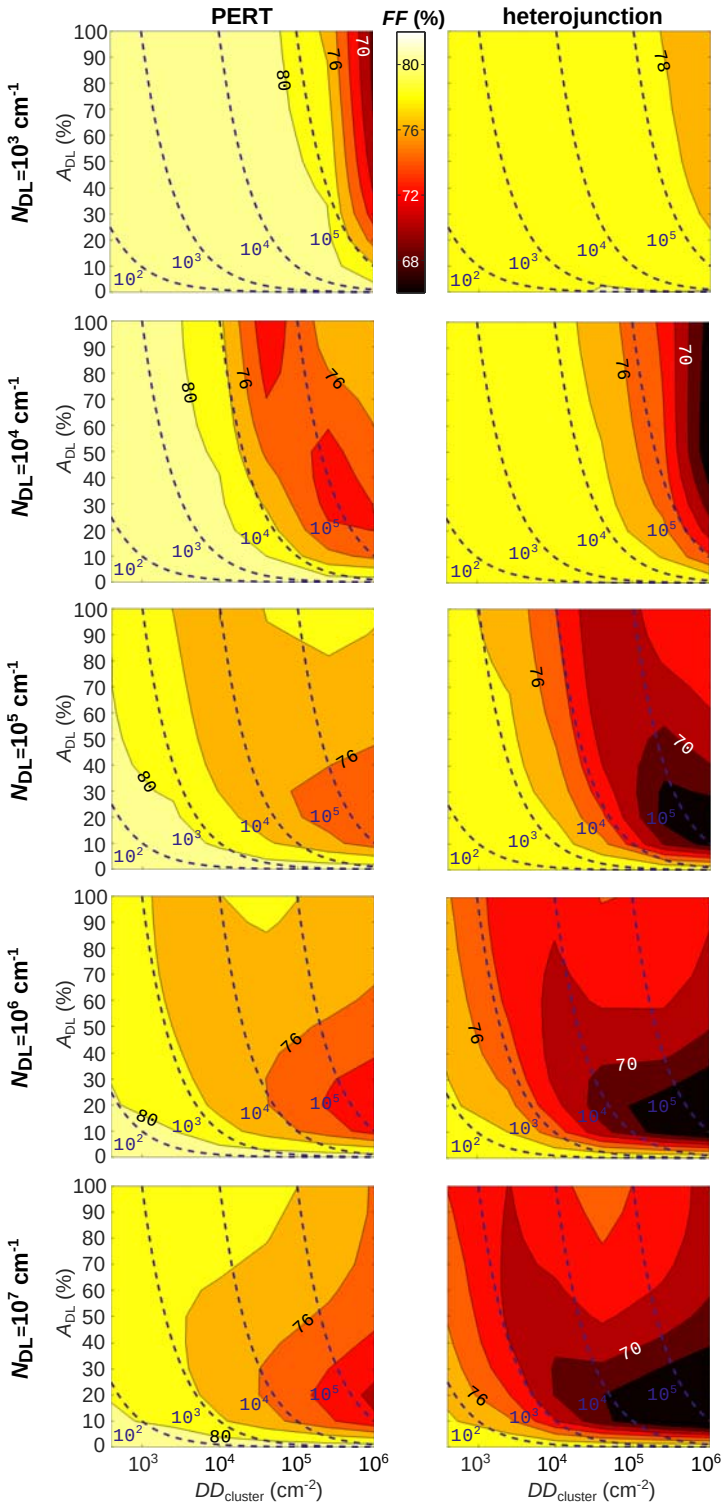

Figure 4.5. Contour plots of simulated *FF* as a function of $DD_{cluster}$ and A_{DL} of the cell for a range of N_{DL} (rows) in PERT (left column) and heterojunction (right column) solar cells.

Both the PERT and the heterojunction cells can achieve efficiencies approaching those of monocrystalline silicon. For low N_{DL}, this occurs for average dislocation densities between 10^4 and 10^5 cm^{-2} for the PERT cell and above 10^5 cm^{-2} for the heterojunction. For high N_{DL}, it occurs for the PERT cell only below a dislocation density of 10^4 cm^{-2} with an area fraction of 10% or below 30% area fraction for a dislocation density of 10^3 cm^{-2}. For the heterojunction, these values are even lower with an area fraction of 10% required for a dislocation density of 10^3 cm^{-2}.

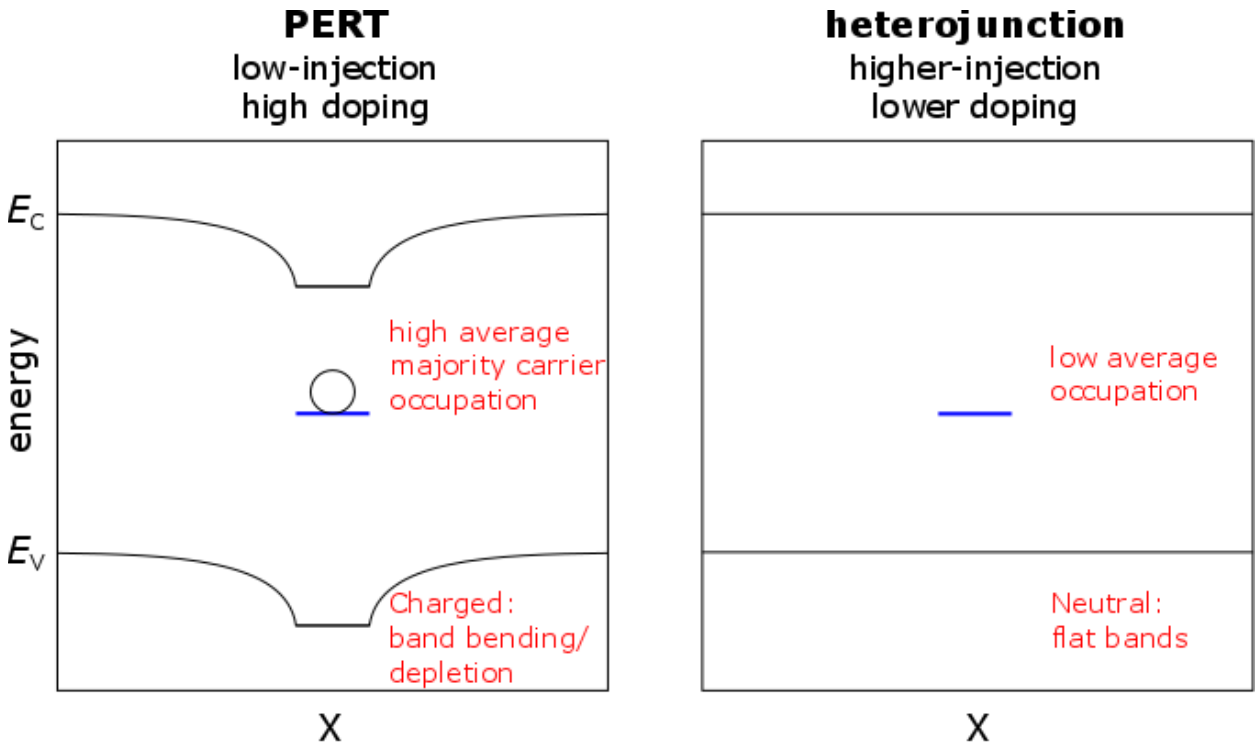

Figure 4.6. Schematic illustrating the origin of increased robustness of the heterojunction simulated in this thesis. Left image shows increased average occupation in the more heavily doped PERT cell, which operates at lower injection, leading to a depletion region around the defect and more recombination. Right image shows the mostly unoccupied defect in the more lightly doped heterojunction, which operates at higher injection, leading to flat bands and less recombination.

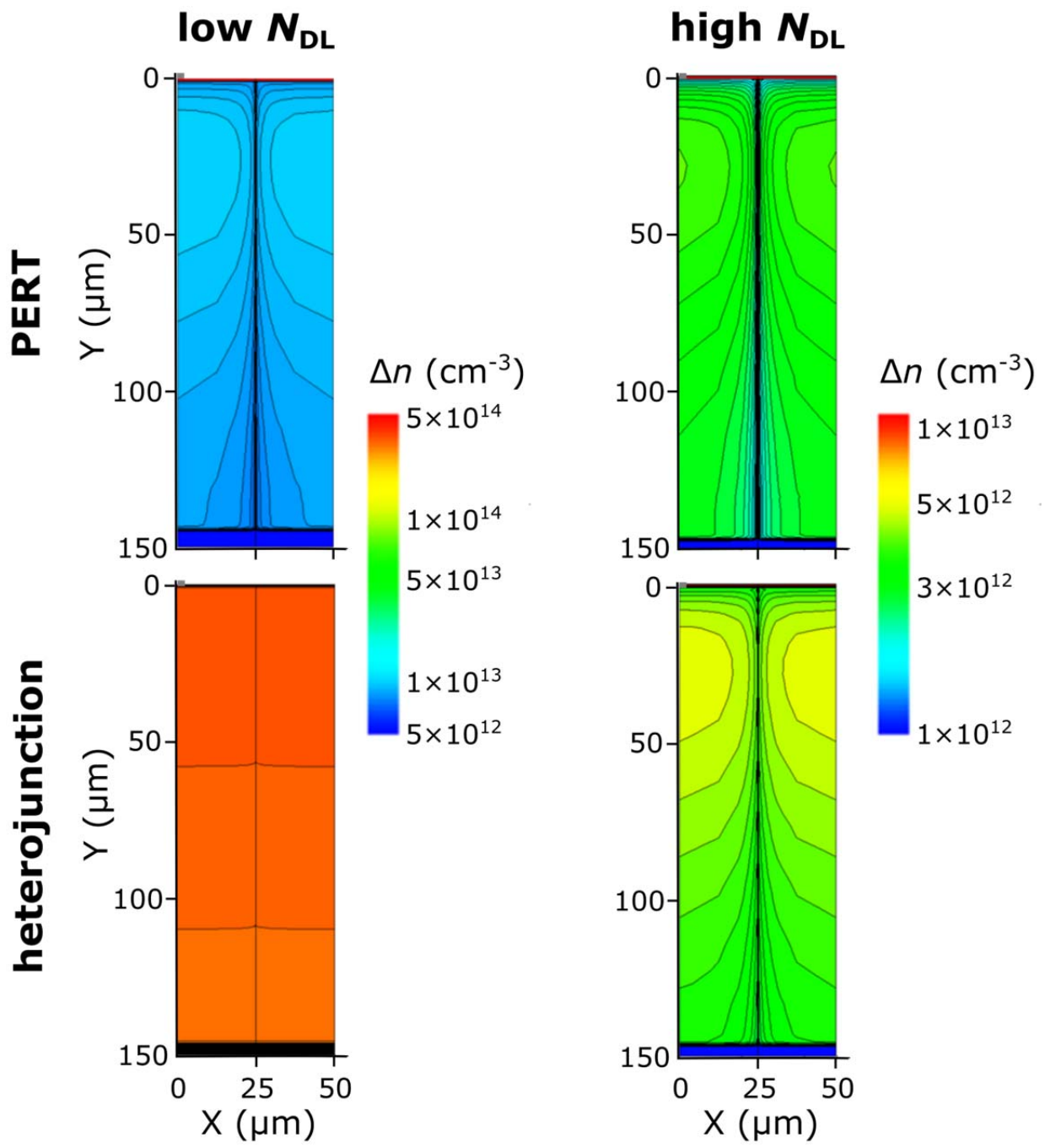

Figure 4.7. The excess carrier density plotted in the neighborhood of a dislocation line, simulated at the maximum power point of the PERT (top row) and the heterojunction (bottom row) cells. The heterojunction cell is in higher injection for low N_{DL} (10^3 cm^{-1}, left column), leading to less charging of the dislocation, a smaller depletion region around the dislocation, and less recombination at the dislocation. Both devices are in low-injection for high N_{DL} (10^6 cm^{-1}, right column), leading to similar charging and a larger depletion region in the more lightly doped heterojunction device. The left scale bar is the low N_{DL} simulations and the right scale bar is for the high N_{DL} simulations.

4.3 Application to Experimental Devices

Analysis to this point has assumed that the dislocation-free regions of the simulated cells are high-lifetime (1 ms) and contain no other defects. However, the model can also be used to predict the performance of materials, such as high-performance mc-Si, that contain other defects outside of the dislocation clusters. This approach is demonstrated with the world record high-performance mc-Si solar cell from Trina Solar [58]. It has a passivated emitter and rear (PERC) structure that is similar to the PERT structure described in Chapter 3.3.2. Differences include the emitter profile, the fact that it does not have a full rear diffusion but only a local Al-BSF above the rear contacts, the profile of this Al-BSF, the background lifetime, and the spacing and width of the front and rear contacts.

This cell was simulated in detail by Trina Solar [87]. Using similar parameters to this simulation, similar results were obtained. There are slight discrepancies because while the emitter and Al-BSF peak doping concentrations and doping depths were the same, the exact profiles were different. To compensate for this, the background lifetime was changed slightly from the values used by Trina. Specifically, they used a deep defect at mid-gap and a shallow defect at $E_C - E_t = 0.1$ eV with $\tau_{n,deep} = 250$ μs, $\tau_{p,deep} = 2500$ μs, and $\tau_{n,shallow} = \tau_{p,shallow} = 7.6$ μs. These values were modified to $\tau_{n,deep} = 100$ μs, $\tau_{p,deep} = 6000$ μs, and and $\tau_{n,shallow} = \tau_{p,shallow} = 3.75$ μs. The resulting *J-V* parameters are comparable to both the experimental device and Trina's simulation, as shown in Table 4.1.

Table 4.1. Comparison of cell performance from simulations of world record mc-Si solar cell from this thesis and Trina Solar **[87]** with experimental data.

Source	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)	V_{MPP} (mV)	J_{MPP} (mA/cm^2)
Trina (experimental)	21.25	667.8	39.78	79.97	566.6	37.49
Trina (simulation)	21.30	669.5	39.78	79.96	562.4	37.87
This thesis (simulation)	21.27	667.3	39.97	79.73	559.0	38.04

To predict the performance of this device if all of the dislocation clusters were removed, first, a photoluminescence (PL) image of the cell is taken, with a resolution of 155 μm/pixel (Figure 4.8). PL images the local radiative recombination in a sample during steady-state excitation with above-band gap light. This recombination rate is proportional to the square of the excess carrier density, so the image can be used to determine both the local dislocation density, and the local recombination strength of these dislocation clusters.

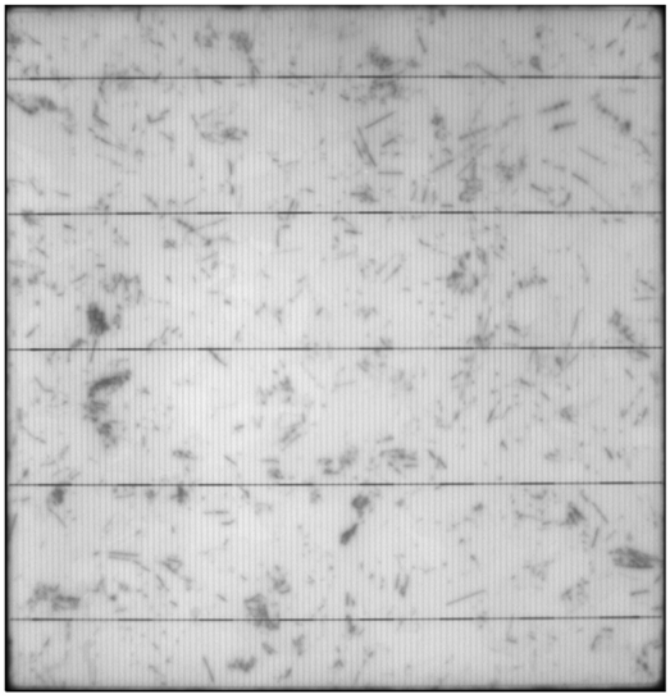

Figure 4.8. Photoluminescence image of Trina Solar's high-performance mc-Si PERC record **[58], [87]** solar cell at an internal photon flux density of 5.747×10^{16} $cm^{-2}s^{-1}$ (resolution: 155 μm/pixel, total area: 156×156 mm^2).

To obtain dislocation density, a method similar to one developed for quantifying dislocation density from low-resolution images of a dislocation-etched silicon wafer is used [157]. In this approach, the greyscale image is turned into a binary image by making all pixels with a greyscale value greater than a designated threshold value white and all pixels with a value below the threshold black. Thus, areas with high non-radiative recombination (and therefore lower excess carrier density and lower radiative recombination) appear black and high-lifetime areas appear white. This approach assumes that areas with much lower lifetime than those around them contain dislocations (the bus bars are removed from the image manually and the fingers are

removed by eliminating all features that appear as vertical lines). With the PL image, instead of calibrating with a higher resolution image as in [157], it is assumed that each black pixel contains a certain number of dislocations (100 in this case). The number of black pixels is then summed over an area containing 100 pixels (2.4 mm^2) to determine the average dislocation density in each of these regions. These regions can be thought of as "macro-pixels."

To obtain an estimate for N_{DL} in each of the regions containing dislocation clusters, the average PL contrast (ratio of local PL intensity to maximum PL intensity) is measured in each macro-pixel. By correlating this contrast to simulations of total radiative recombination in dislocation clusters compared to total radiative recombination in dislocation-free areas, N_{DL} for each dislocation cluster is determined.

Using the simulated *J-V* curves for each combination of dislocation density and N_{DL}, the effect of dislocations can be subtracted from the measured *J-V* curve using the same weighted average approach described in Chapter 3.3.3. Specifically, the following formula is used:

$$J_{clean}(V) = \frac{Jcell(V) - \sum A_{DL} \times J_{DL}(V)}{1 - \sum A_{DL}}, \quad (4.1)$$

where $J_{clean}(V)$ is the calculated current as a function of voltage for a dislocation-free solar cell, $J_{cell}(V)$ is the measured current as a function of voltage, A_{DL} is the fractional area of each measured dislocation cluster, and $J_{DL}(V)$ is the simulated current as a function of voltage for the combination of dislocation density and N_{DL} extracted for each measured dislocation cluster.

The results for the world record mc-Si solar cell are shown in Table 4.2. Due to the high quality of the wafer used for this cell, the impact of dislocations is limited. The calculated efficiency increase is 0.26% absolute, mostly due to a 0.42 mA/cm^2 increase in J_{SC}. We attribute the large difference in J_{SC}, accompanied by a small difference in V_{OC} to the highly asymmetric capture cross-sections for majority and minority carriers at the dislocations. This asymmetry means that recombination is dominated by the dislocation at J_{SC} conditions and by other parts of the device at V_{OC}.

Table 4.2. Simulated effect of removing dislocations from world record mc-Si solar cell.

	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)
mc-Si world record (experimental)	21.25	667.8	39.78	79.97
Dislocation-free (simulated)	21.51	668.3	40.20	80.06

Once the dislocation-free *J-V* curve is obtained, the device performance for any arbitrary distribution of dislocation clusters can be calculated. These calculations would show not only the limits of performance but the effect of smaller reductions in dislocation density and decoration as well as changes in dislocation distribution.

4.4 Validation of Baseline Dislocation Model

Comparison to the world record mc-Si cell can also be used to validate the baseline dislocation model. First, a model for a dislocation-free cell is developed. This model depends solely on changing the lifetime associated with the shallow and deep energy defects. The shallow defects are associated with dislocations and grain boundaries as discussed in Chapter 2.1. Therefore, the concentration of these shallow defects that is simulated was decreased by the area fraction of the whole wafer that contained dislocations (obtained as described in Chapter 4.3). This decrease led to a new $\tau_{n,shallow}' = \tau_{p,shallow}' = 4.29$ μs. The minority carrier (electron) lifetime associated with the deep defect is increased as well. The new value ($\tau_{n,deep}'$) was chosen so that the total recombination in the device (according to the SRH formalism in Equation (4.2)), with $\tau_{n,deep}'$ in the non-dislocated areas and $\tau_{n,deep,i}$ in each dislocated region to give the measured PL contrast in that region (binned into ranges of 10% contrast) was equal to the total recombination (according to Equation (4.2)) for the original values of $\tau_{n,shallow} = \tau_{p,shallow} = 3.75$ μs, $\tau_{n,deep} = 100$ μs and $\tau_{p,deep} = 6000$ μs. This calculation gave a value of $\tau_{n,deep}' = 200$ μs, with $\tau_{p,deep}' = \tau_{p,deep} = 6000$ μs. The SRH recombination is given by:

$$R = \frac{(n\,p - {n_i}^2)}{\tau_p\,(n+n_1)+\tau_n\,(p+p_1)}, \tag{4.2}$$

with $n_1 = n_i \exp((E_t - E_0)/kT)$ and $p_1 = p_i \exp((E_0 - E_t)/kT)$ where E_0 is the intrinsic energy level. The total recombination described above is given by:

$$R_{tot} = A_{\mathrm{DL-free}} R\left(\tau'_{n,\mathrm{shallow}}, \tau'_{p,\mathrm{shallow}}, \tau'_{n,\mathrm{deep}}, \tau_{p,\mathrm{deep}}\right) + \sum_i A_{DL,i} R\left(\tau_{n,\mathrm{shallow}}, \tau_{p,\mathrm{shallow}}, \tau^i_{n,\mathrm{deep}}, \tau_{p,\mathrm{deep}}\right), \tag{4.3}$$

where $\tau_{n,deep}^{i}$ is chosen such that the PL contrast matches the region *i* in the PL image as described above. This is compared to the total recombination for the original simulation of the experimental world record mc-Si cell calculated using Equation (4.2).

Using the *J-V* curve simulated with the new lifetime values, the effect of the dislocation clusters in the world record mc-Si cell are added back in using the same *J-V* curves as in Chapter

3.3.3 and Equation (3.7), with A_{DL} and $J_{DL}(V)$ values taken from the curves associated with each dislocation cluster as described in Chapter 4.3. The resulting *J-V* curve shows excellent agreement with the experimental curve as shown in Figure 4.9 and Table 4.3.

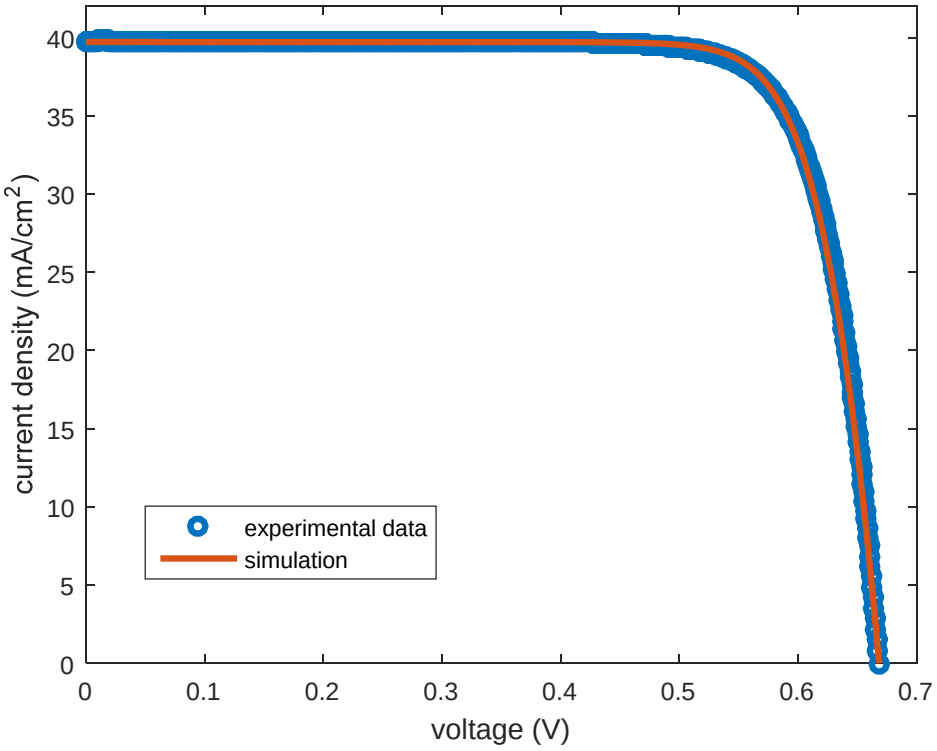

Figure 4.9. Comparison of simulated and experimental *J-V* curves for world record mc-Si solar cell. Simulated curve is obtained by adding dislocations to a simulated *J-V* curve representing the non-dislocated area of the cell.

Table 4.3. Comparison of experimental and simulated device performance for world record mc-Si solar cell.

	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	V_{MPP} (mV)	J_{MPP} (mA/cm^2)
mc-Si world record (experimental)	21.25	667.8	39.78	79.97	566.6	37.49
mc-Si world record (simulated)	21.33	668.5	39.71	80.35	563.6	37.85

CHAPTER

5

EFFECTS OF GRAIN BOUNDARIES ON SILICON SOLAR CELLS**

5.1 Comparison to Historical Data

Computational resources limit the grain sizes that could be simulated to less than 1 mm × 1 mm. These sizes are comparable to those near the bottom of high-performance mc-Si ingots [158] and those in kerfless wafers grown directly from molten silicon [84], [159]. Since simulated performance varies relatively smoothly with grain size, performance of larger grains can extrapolated from these results.

Figure 5.1 shows good agreement between simulated device performance and experimental devices in literature [135] as a function of grain size (x-axis) and the areal density of recombination centers at the grain boundary (N_{GB}, data series). The spread in the experimental data is attributed to variation in device design, background lifetime away from the grain boundary, and the concentration of impurities decorating the grain boundaries. Variation in impurity concentration in the bulk and at the grain boundaries arises from differences in growth and processing.

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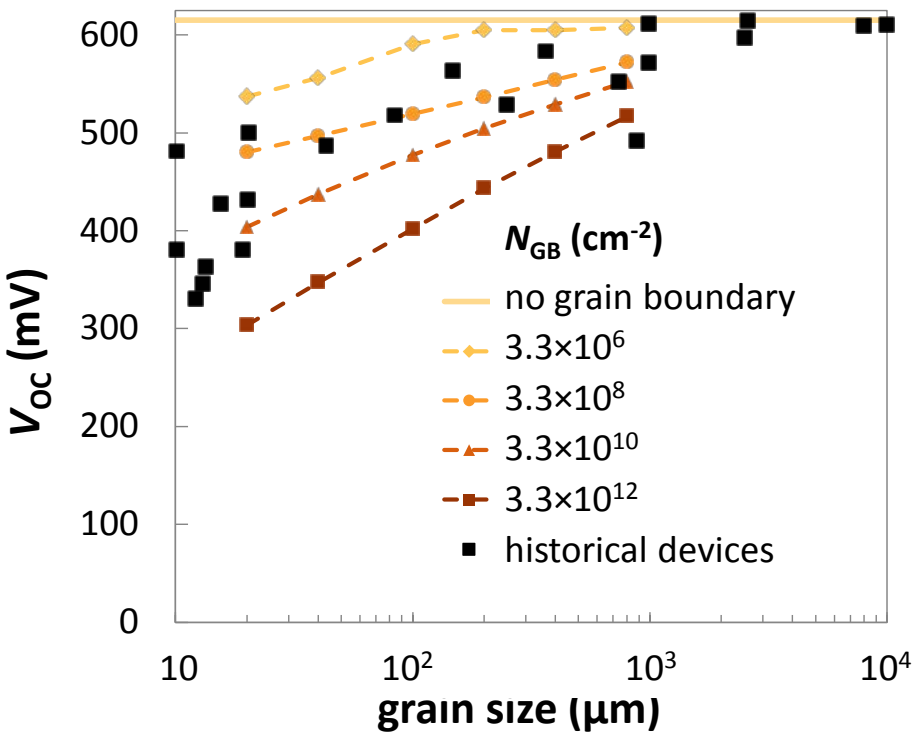

Figure 5.1. Effect of grain size on open-circuit voltage (V_{OC}) for Al-BSF devices. Experimental literature data **[135]**, shown as black dots, is compared to TCAD simulations of grain boundaries with varying areal density of deep defects states (N_{GB}).

N_{GB} is related to the density of dangling bonds and the density of metal impurities segregated to the grain boundary. These parameters are in turn correlated to the physical structure of the grain boundary [106]. Therefore, grain boundary type and misorientation angle strongly influence the distribution of N_{GB} in a wafer, with recombination activity ranging from undetectable to severe. The range of N_{GB} in these simulations endeavors to represent this full range. The line of best fit to the historical data in Figure 5.1, $N_{GB} = 3.3\times10^8$ cm^{-2}, corresponds to a grain boundary surface recombination velocity for electrons (SRV_e) in the *p*-type bulk silicon wafer of approximately 2.2×10^5 cm/s and surface recombination velocity for holes (SRV_h) of about 480 cm/s, using the formulas [103]:

$$SRV_e = \sigma_e \times v_{the} \times N_{GB}, \quad (5.1)$$

$$SRV_h = \sigma_h \times v_{thh} \times N_{GB} \quad (5.2)$$

σ_e and σ_h are the electron and hole capture cross-sections of the mid-gap defect (see Chapter 3.1 for details), and $v_{the} = 2\times10^7$ cm/s and $v_{thh} = 1.7\times10^7$ cm/s are the thermal velocities of electrons and holes, respectively.

5.2 Comparison of PERT and Heterojunction Cells

Having established that the a TCAD model for grain boundaries is in reasonable agreement with experimental data, a grain boundary is inserted into the models for the two advanced device architectures described in Chapter 3.3.2: (a) passivated emitter and rear totally diffused (PERT) cell, with an identical junction and front metallization pattern to the Al-BSF cell but local rear contacts [145], [147]; (b) a heterojunction device with a front-side gallium phosphide (GaP) emitter and identical rear side to the PERT cell [147].

Figure 5.2 shows simulated device performance as a function of grain size (*x*-axis) and N_{GB} (data series). SRV_e and SRV_h can be calculated from N_{GB} using Equations (5.1) and (5.2) above. However, *SRV* does not provide insight into the effects of grain boundary charging. Charging and injection-level effects are discussed below.

Simulated efficiencies exceed 20% for both device architectures for grains of about 1 mm with N_{GB} less than 3.3×10^6 cm^{-2} ($SRV_e = 2.2\times10^4$ cm/s, $SRV_h = 5$ cm/s). The efficiency *vs.* grain size curve for PERT cells with $N_{GB} = 3.3\times10^{10}$ cm^{-2} ($SRV_e = 2.2\times10^6$ cm/s, $SRV_h = 4.8\times10^4$ cm/s). has a slope of 6% (absolute) per decade. Linear extrapolation suggests that centimeter-sized grains with this grain boundary defect concentration could achieve 20% efficiency. As described in Chapter 4.3, Trina Solar reported a world record efficiency of 21.25% for 6" screen-printed solar cells on mc-Si wafers [58] with a similar cell architecture to the PERT cell simulated here. While grain size was not reported for these devices, reports on similar material give averages on the order of 1 cm [76]. Smaller-grained materials with lower grain boundary defect concentrations may also be viable. Sio *et al*. showed median SRV_e less than 2×10^4 cm/s for a representative set of grain boundaries in a commercial *p*-type mc-Si ingot in the as-grown and processed states. For many of these grain boundaries, SRV_e was reduced below 100 cm/s by gettering and hydrogenation [160]. Other mc-Si (high-performance *p*-type, *n*-type) showed similar or lower *SRV* [161]. Hanwha Q-Cells has reported efficiencies on kerfless wafers grown directly from molten silicon of 19.1% [59]. Again, grain sizes were not reported but similar material has grain sizes on the order of hundreds of microns [84], [159].

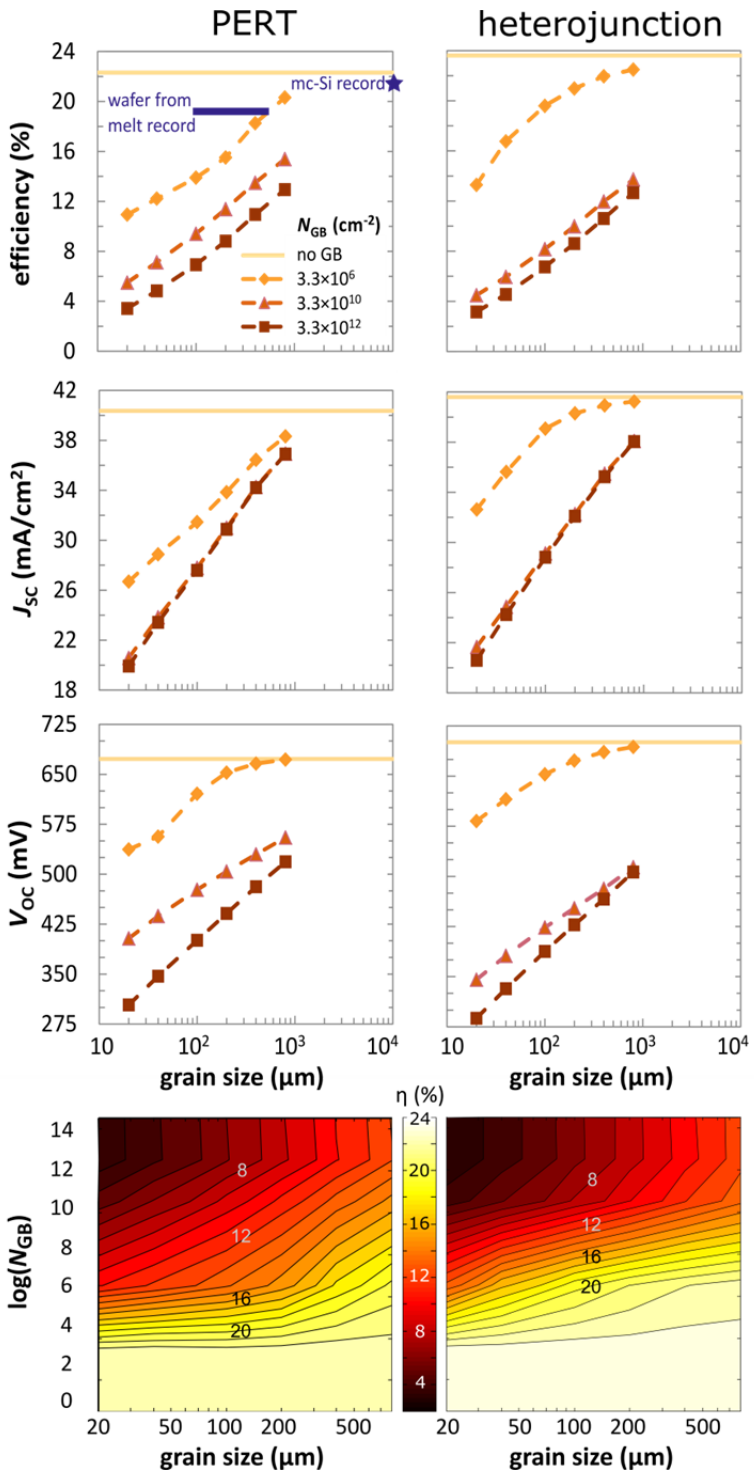

Figure 5.2. Simulated device performance as a function of grain size (*x*-axis) and N_{GB} (data series) for advanced homojunction (PERT) and heterojunction solar cells. Blue star indicates efficiency of world record mc-Si cell described in Chapters 4.3 and 4.4. Blue line indicates the highest reported efficiency for wafers grown directly from molten Si with presumed grain size. Bottom figures show contour plots of efficiency as a function of grain size (*x*-axis) and N_{GB} (*y*-axis) for each architecture.

As with the simulations of cells with dislocations, the simulated heterojunction is more robust to grain boundaries with low-to-intermediate values of N_{GB} than the homojunction device. To elucidate this difference, recombination is analyzed at the maximum power point in each region of the device (Figure 5.3): front contact, emitter, junction, bulk silicon wafer, and rear contact. Here, the emitter refers to the *n*-type region of the PERT cell, including the front surface, and the GaP layer in the heterojunction device, including the GaP/Si interface and the GaP front surface. The junction refers to the space-charge region, and the bulk silicon wafer includes the quasi-neutral portion of the base, the back-surface field region, and the passivated part of the rear surface. The portion of the rear surface in direct contact with the metal of the rear contact is treated separately ("rear contact"). Both the heterojunction and homojunction cells are dominated by recombination at the grain boundary in the bulk silicon wafer. The heterojunction has significantly less bulk recombination than the PERT cell at moderate impurity concentrations but more at high impurity concentrations.

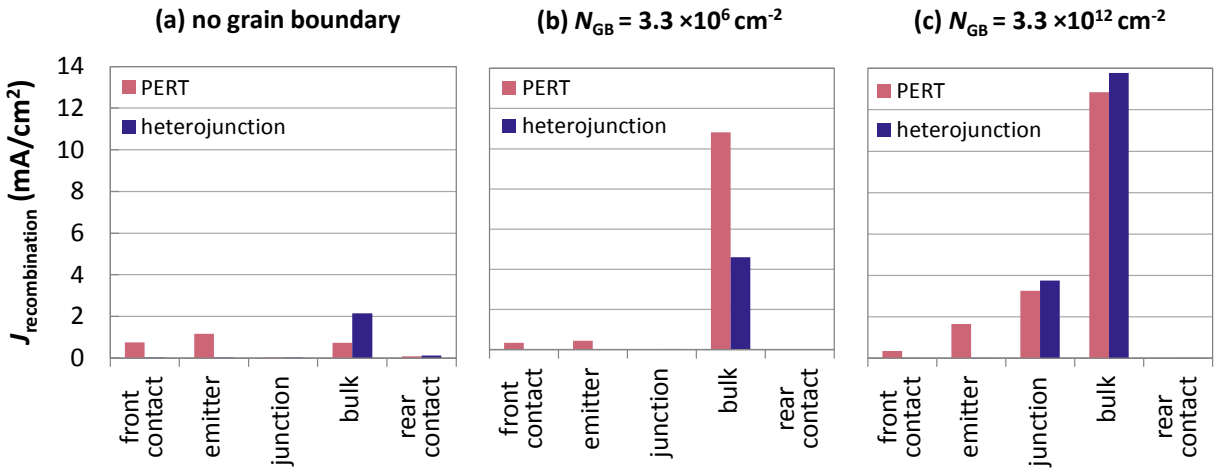

Figure 5.3. Simulated recombination in each region of the PERT and heterojunction devices: front contact, emitter (*n*-type portion of the PERT cell, GaP layer of the heterojunction), junction (space-charge) region, bulk Si wafer, and rear contact. a) No grain boundary included in the simulation, b) N_{GB} = 3.3×10^{6} cm^{-2}, c) N_{GB} = 3.3×10^{12} cm^{-2}.

As with cells with dislocations, the difference in the performance of the two devices is attributed to their optimized [147] base doping and their injection level rather than to effects of the junction itself, as might be expected from earlier work [162]. The doping concentrations and excess carrier densities at the maximum power point (MPP) for both devices are shown in Table

5.1. Higher injection in the heterojunction device is due to reduced recombination at the front surface, in the emitter, and at the front contact as shown in Figure 5.3.

Table 5.1. Optimized **[147]** doping concentration of base Si wafer and injection level at maximum power point (MPP) with $N_{GB} = 3.3\times10^{6}$ cm^{-2} for PERC and heterojunction device.

	PERT	Heterojunction
Base doping concentration	7×10^{15} cm^{-3}	6×10^{14} cm^{-3}
Injection level at MPP	$10^{11} – 10^{12}$ cm^{-3}	10^{14} cm^{-3}

The lower injection level in the homojunction device leads to greater occupation of the mid-gap defects at the grain boundary by majority holes (see Figure 4.6). With 100 μm grains and $N_{GB} = 3.3\times10^{6}$ cm^{-2}, the interface charge density at MPP is about 1000 times greater in the homojunction device (1–3 $\times10^{6}$ cm^{-2} *vs*. 3–4$\times10^{3}$ cm^{-2} depending on the position within the cells). This charging creates a depletion region around the grain boundary that drives electrons to the grain boundary, enhancing recombination. The difference in the size of this depletion region for the PERT and heterojunction devices is shown for 100 μm grains with $N_{GB} = 3.3\times10^{6}$ cm^{-2} in Figure 5.4a,c.

Higher N_{GB} increases recombination, lowering the injection level and increasing the grain boundary charging in the heterojunction device to the level of the homojunction device. The depletion region surrounding these heavily decorated grain boundaries is larger in the heterojunction device than in the homojunction device due to its lighter doping (Figure 5.4b,d). Thus, at high values of N_{GB}, the heterojunction performs worse than the homojunction. These effects of injection level and doping concentration show similar trends to earlier work on charged grain boundaries in silicon [131], [163], [133], [134], including those that draw contrary conclusions because they only consider devices in low-level injection (low-lifetime grains at relatively high doping concentrations) with very recombination-active grain boundaries.

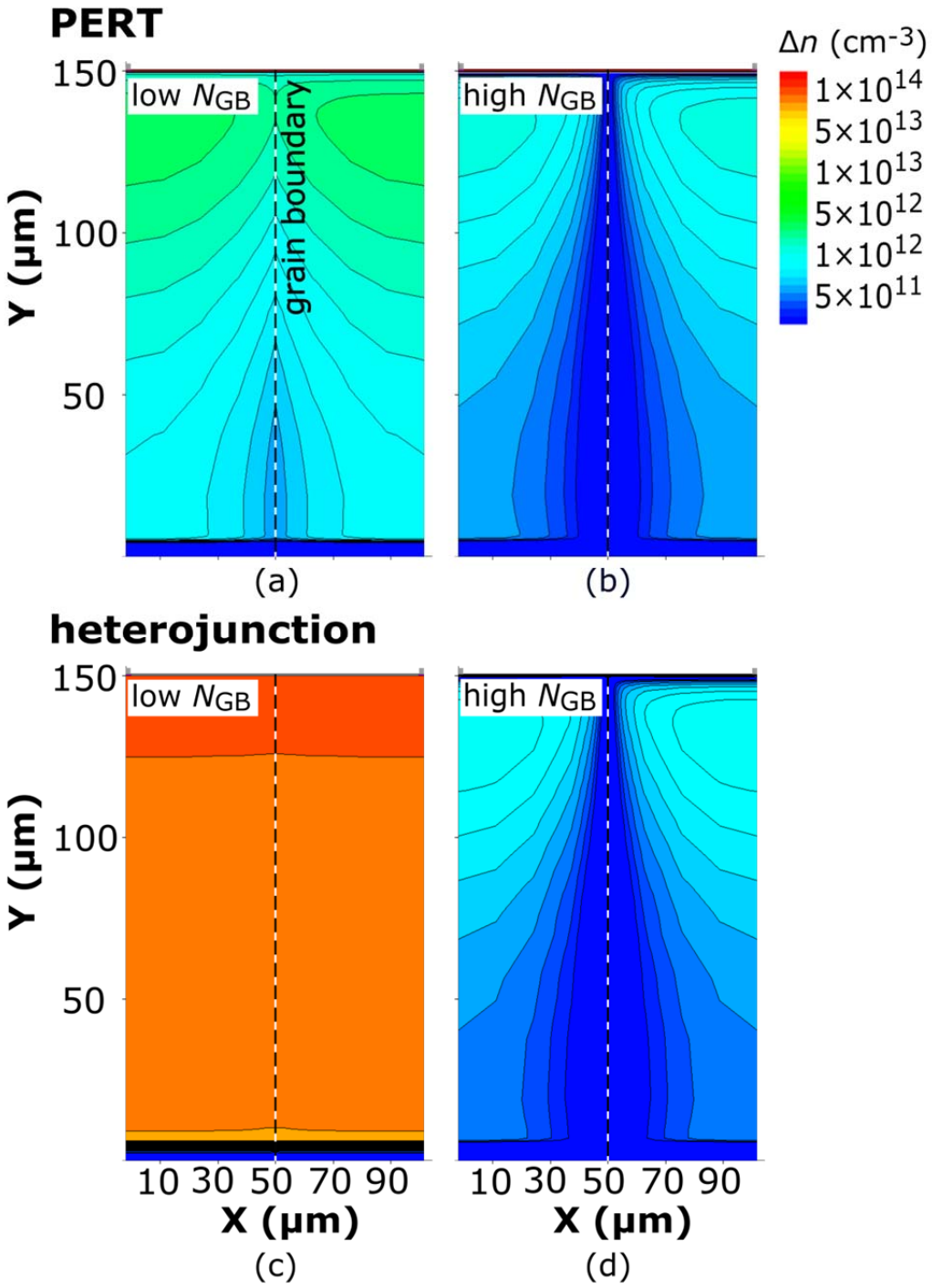

Figure 5.4. a) Excess carrier density (Δn) of a representative 2-D slice of a PERT (a,b) and heterojunction cell (c,d) at the maximum power point with $N_{GB} = 3.3\times10^{6}$ cm^{-2} (a,c) and $N_{GB} = 3.3\times10^{12}$ cm^{-2} (b,d). Simulated domain is from $x = 0$ to $x = 50$ μm. $x = 50$ to $x = 100$ μm included for clarity in visualizing the depletion region around the grain boundary (see Figure 3.8).

5.3 Experimental Validation of Grain Boundary Model

In order to validate the model for the electrical activity of grain boundaries, a wafer was obtained from a quasi-monocrystalline Si ingot seeded with six monocrystalline seeds oriented with the <110> direction up (growth direction) [164], [165]. The tiling of the seed crystals on the bottom of the crucible led to the formation of nine small-angle grain boundaries due to dislocation nucleation and pile-up at the seed interfaces. The misorientation and structure of these grain boundaries was described in Ref. [164]. This wafer is cut into nine pieces as shown in Figure 5.5. Of these nine pieces, five contain only a single grain boundary. These five pieces are processed by the Holman Group at Arizona State University into SHJ solar cells, with two cells per wafer piece (see Figure 5.5).

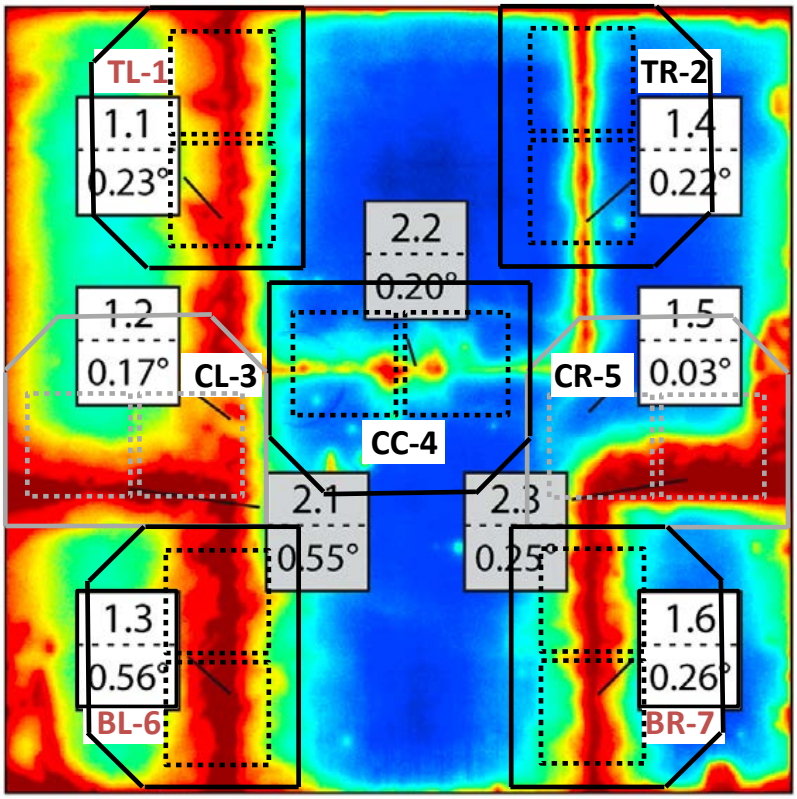

Figure 5.5. Microwave photoconductance decay image labeled with grain boundary misorientation angle. Red indicates areas of low lifetime and blue areas of high lifetime. Lines of red indicate the location of grain boundaries. The position and shape of samples cut from this wafer are identified with solid lines and the position of cells fabricated on these samples with dashed lines. Samples and cells outlined in black have exactly one grain boundary in them and those outlined in grey have more than one. Image adapted from Ref. **[164]**.

Before the metallization step in the solar cell process, the injection-dependent lifetime of each sample is measured at Arizona State University using quasi-steady-state photoconductance measured with a Sinton Instruments WCT-120 [166]. PL imaging is used to map the lifetime and excess carrier density in each of the cells, following the process described in Refs. [167]–[169]. The PL images are taken with a deep-depletion Si CCD (Princeton Instruments PIXIS) with a 1024×1024 pixel array, using a zoom lens with a 6 cm field of view (60 µm/px resolution). The sample is illuminated with a diode laser with a central wavelength of 808 nm. A 1 mm-thick InP wafer is placed in front of the lens to act as a long-pass filter and filter out sub-band gap luminescence and reflected light. Since the samples show a characteristic injection dependence for lifetime distinct from typical Cz-Si wafers, the sample containing the least recombination-active grain boundary (central wafer—CC-4—in Figure 5.5) was used for calibration rather than a monocrystalline sample as suggested by Sio *et al.* [169]. This injection-dependent lifetime curve is shown in Figure 5.5.

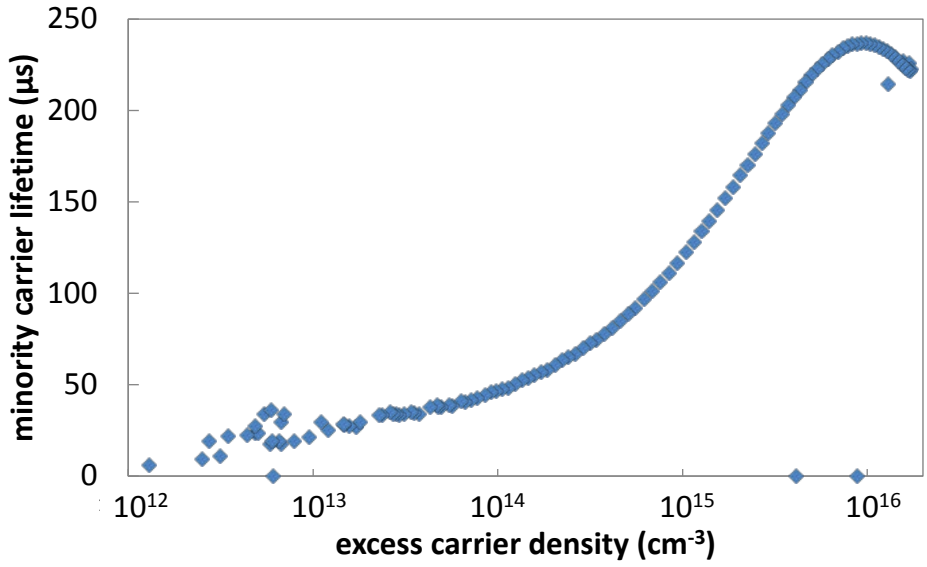

Figure 5.6. Injection-dependent lifetime of sample with least grain boundary recombination (center sample in Figure 5.5).

The background lifetime in the simulations is taken to be the lifetime of this sample at the simulated injection level at the maximum power point (about 3×10^{14} cm^{-3}). In order to distinguish the electron and hole lifetimes, the injection-dependent lifetime is fit (by Mallory

Jensen, MIT) using the method of Murphy *et al*. [170] to obtain a capture cross-section ratio. For this calculation, it is assumed that the injection-dependent lifetime is dominated by a single defect at mid-gap. From these calculations a background lifetime of τ_n = 70 µs and τ_p = 262.5 µs is obtained.

The effect of the grain boundary on device performance is simulated varying N_{GB} and simulating *J-V* curves. These curves are compared to pseudo-*JV* curves obtained from Suns-V_{OC} measurements (also using a tool from Sinton Instruments) [171], [172] of the experimental devices. Suns-V_{OC} pseudo-*JV* curves are used rather than true *J-V* curves because the metallization on the cells is inconsistent and adding series resistance as a fitting parameter makes it possible to fit the curves with too wide a range of N_{GB}. Once a suitable value of N_{GB} is found to fit a pseudo-*JV* curve, the same value of N_{GB} is used to simulate excess carrier density as a function of position in the cell at illumination intensities of 0.117 suns and 0.233 suns, corresponding to two of the laser powers used for PL images.

Line scans (perpendicular to the grain boundary) of excess carrier density are then taken from the calibrated PL images (see Figure 5.7). These profiles of excess carrier density are averaged over the length of the grain boundary, and the result is compared to the simulated excess carrier density. The grain boundaries are not perfectly straight, having some variation in their position in the direction perpendicular to their primary axis. This variation leads to a broadening of the excess carrier density profile as minimum of one line is rarely the minimum of another. To fit this broadened profile, the width of the spatial variation is measured in the PL image, and a set of eleven simulated profiles with their center points offset up to this width are averaged together (see Figure 5.8).

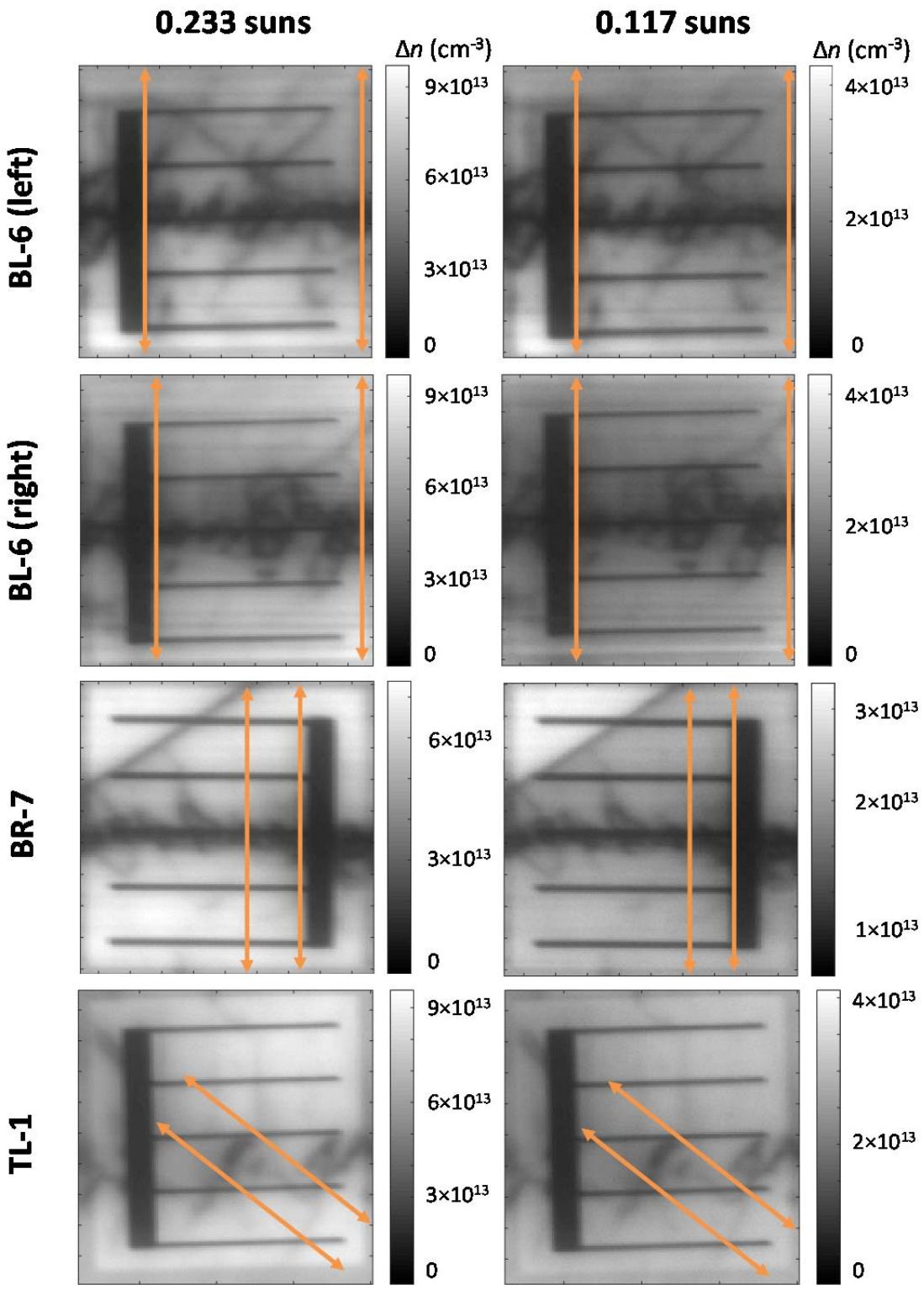

Figure 5.7. Calibrated PL images showing excess carrier densities of samples whose excess carrier density profile and *J-V* curves are fitted. Orange lines indicate direction and length of line scans taken for profiles as well as the position of the first and last line scans taken.

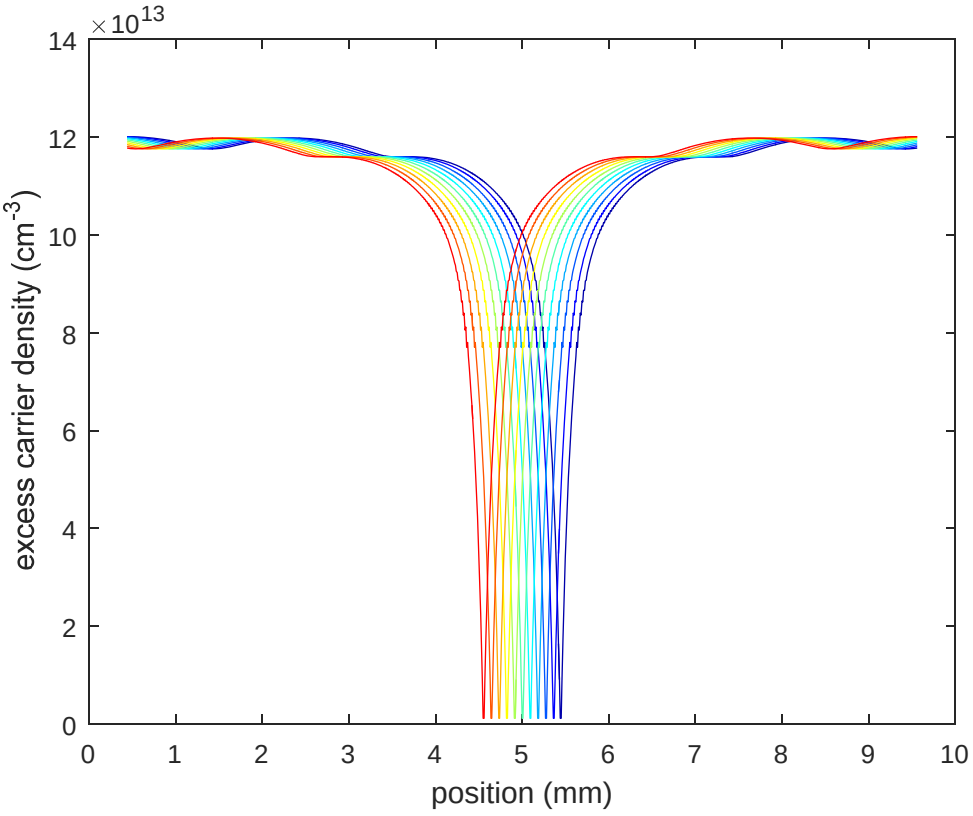

Figure 5.8. Example of simulations averaged to match averaging of the line scans of experimental excess carrier density maps. Each simulation is symmetrical, and each color represents a shift in position. The total width at the *x*-intercept is the width over which the center of the grain boundary varies.

The results of these fittings are shown in Figure 5.9. The slope of the excess carrier density curve in the bottom row of Figure 5.9 shows a bimodal characteristic. The lower slope is attributed to an area of lower background lifetime in the cell. The agreement near the minimum of this curve and of the ultimate maximum of excess carrier density is taken to indicate a good fit to the model. The agreement generally between simulation and experiment for both the excess carrier density profiles and the pseudo-*JV* data indicates that the grain boundary model presented in this thesis captures the injection-dependent recombination of grain boundaries in silicon and can quantitatively predict the effect of grain boundaries on the performance of silicon solar cells.

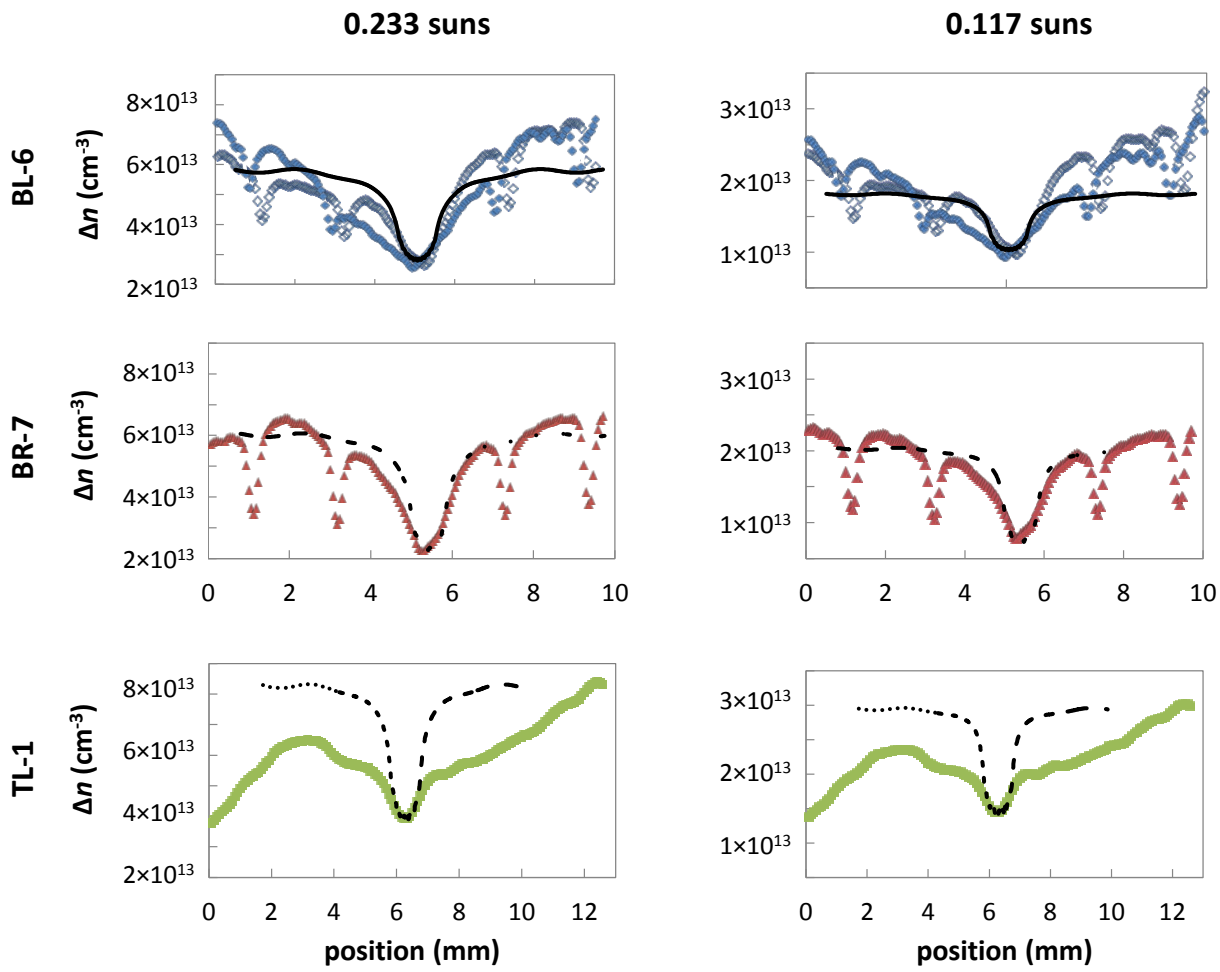

Figure 5.9. Simulated (black lines) and experimental (colored symbols) excess carrier density profiles across the grain boundary in three different samples. The experimental data is sample TL-1 shows a region with much lower slope than the simulated data in part of the profile due to a low lifetime region coincidentally located near the grain boundary.

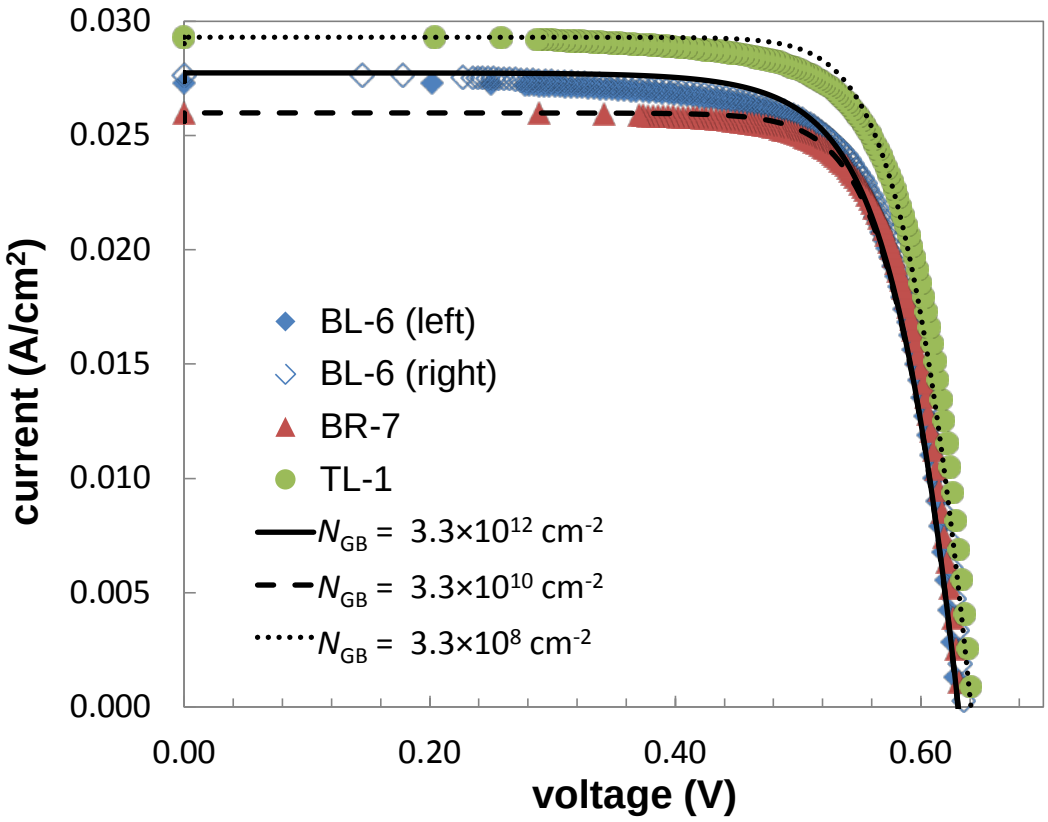

Figure 5.10. Simulated *J-V* curves and experimental pseudo *J-V* curves from Suns-V_{OC} measurements of three samples.

CHAPTER

6

CONCLUSIONS

The best hope for minimizing the risk of catastrophic climate change is to reduce greenhouse gas emissions enough to keep atmospheric carbon dioxide concentrations under about 450 ppm. Achieving this goal will likely require manufacturing and installing on the order of ten terawatts of PV. PV based on crystalline silicon absorbers offer the most promising route to achieving this goal. The risk associated with the availability and cost of key elements of commercial thin-film absorbers—tellurium in cadmium telluride and indium in copper (indium, gallium) diselenide—is high. The history of technology teaches us that a new absorber would likely take ten to fifteen years to commercialize. Even if a new technology entered commercial production today, it would have to be orders of magnitude cheaper and lower capex than silicon in order to scale to ten terawatts in the next fifteen years. To reach climate-driven PV deployment targets with crystalline silicon will require either trillions of dollars of government subsidies, trillions of dollars in low-interest debt for companies with leverage ratios of about 5:1, or substantial reductions in the capex and cost of current crystalline silicon technology combined with significant increases in efficiency. Chapter 1 of this thesis set quantitative targets for the technology innovations necessary to reach these targets.

Most of the capex for current technology goes into making the silicon wafer itself. Low-cost, low-capex established, early commercial, and lab-scale alternatives to current processes for crystallization and wafering exist, but the efficiency of solar cells produced with these methods lag behind that of wire-sawn wafers grown by the Czochralski method. The reason for this difference in efficiency is largely the presence of structural defects like dislocations and grain boundaries in these alternative materials.

This thesis set out to answer two questions: first, what are the efficiency limits for silicon solar cells that contain dislocations and grain boundaries? Second, can the deleterious effects of these defects be mitigated through materials engineering and device design? To answer these

questions, simulations tools were developed to analyze the performance impacts of these defects in advanced solar cell architectures, and these tools were validated through comparison to experiment. It is determined that the performance of silicon with dislocations and grain boundaries can approach that of Czochralski silicon. This finding derives from the understanding that structural defects themselves have a minor impact on efficiency, and it is largely metal impurities segregated to these defects that worsen performance. Thus, if the concentration if impurities at these defects can be controlled or the defects can be passivated, the presence of dislocations and grain boundaries will not limit efficiency. Performance across the parameter space including the density and distribution of structural defects as well as the concentration of impurities segregated to these defects is mapped for several device architectures. These maps indicate that high efficiency can be achieved with realistic values of defect density and impurity concentration. Refinements of existing processing knowledge related to crystal growth, gettering, and hydrogenation should be sufficient to realize high efficiency on low-cost, low-capex substrates.

However, the results from Chapter 1 indicate that by itself, this process engineering will not be enough to achieve the aggressive deployment targets mandated by climate concerns. Wafer thickness will likely have to be reduced by an order of magnitude to eliminate a substantial portion of the third of capex that goes into the production of polysilicon feedstock. This reduction will require either new wire-saw technology or the elimination of wire-sawing. Either way, new wafer handling techniques will be necessary. Throughout module production, processes either need to be eliminated or have their capex reduced by factors of three to five. These reductions will require new processes, like local rather than global applications of heat (*e.g.*, laser processing replacing furnaces) or massive increases in the throughput of existing processes (*e.g.*, low-pressure diffusion enabling five times more wafers per through tighter spacing). Simultaneously, efficiency, particularly at the module level, must be increased beyond today's best commercial modules, while costs come down by a factor of three to four. New schemes for all-back-contacted cells and passivated contacts appear to offer routes to achieve these efficiencies while larger factories and cheaper equipment can reduce cost and capex. Thin, high-efficiency devices are promising for defective materials as well because the smaller volume of material and the higher injection levels that come with thinner substrates and better

passivation of surfaces and contacts reduce the impact of structural defects (and often point defects).

The engineering challenges to producing PV technology for the terawatt scale are great. However, we have the tools to tackle these challenges, and synergies like high-efficiency devices that mitigate the presence of defects or low-capex crystallization techniques that can eliminate downstream process steps show the confluence of PV research. With sustained innovation, PV is on the verge of fulfilling the promise that the enormity of the solar resource can play a substantial role in addressing the enormity of the dual challenges of energy poverty and climate change.

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REFERENCES

[1] D. Berney Needleman, J. R. Poindexter, R. C. Kurchin, I. M. Peters, G. Wilson, and T. Buonassisi, "Economically sustainable scaling of photovoltaics to meet climate targets," *Energy Environ. Sci.*, Apr. 2016.

[2] IPCC Core Writing Team, "Climate Change 2014: Synthesis Report. Contribution of Working Groups I, II and III to the Fifth Assessment Report of the Intergovernmental Panel on Climate Change," IPCC, Geneva, Switzerland, 2014.

[3] International Energy Agency, "Energy and Climate Change: World Energy Outlook Special Report," 2015.

[4] P. Friedlingstein, R. M. Andrew, J. Rogelj, G. P. Peters, J. G. Canadell, R. Knutti, G. Luderer, M. R. Raupach, M. Schaeffer, D. P. van Vuuren, and C. Le Quéré, "Persistent growth of CO2 emissions and implications for reaching climate targets," *Nat. Geosci.*, vol. 7, no. 10, pp. 709–715, Sep. 2014.

[5] J. Rogelj, W. Hare, J. Lowe, D. P. van Vuuren, K. Riahi, B. Matthews, T. Hanaoka, K. Jiang, and M. Meinshausen, "Emission pathways consistent with a 2 °C global temperature limit," *Nat. Clim. Change*, vol. 1, no. 8, pp. 413–418, Oct. 2011.

[6] UNFCCC. Conference of the Parties (COP), "Adoption of the Paris Agreement. Proposal by the President.," Paris, France, Dec. 2015.

[7] P. Moriarty and D. Honnery, "What is the global potential for renewable energy?," *Renew. Sustain. Energy Rev.*, vol. 16, no. 1, pp. 244–252, Jan. 2012.

[8] M. Z. Jacobson and M. A. Delucchi, "A Path to Sustainable Energy by 2030," *Sci. Am.*, vol. 301, no. 5, pp. 58–65, Nov. 2009.

[9] M. D. Kempe, "Ultraviolet light test and evaluation methods for encapsulants of photovoltaic modules," *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 2, pp. 246–253, Feb. 2010.

[10] E. Hasselbrink, M. Anderson, Z. Defreitas, M. Mikofski, Y.-C. Shen, S. Caldwell, A. Terao, D. Kavulak, Z. Campeau, and D. DeGraaff, "Validation of the PVLife model using 3 million module-years of live site data," in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*, 2013, pp. 7–12.

[11] D. C. Jordan and S. R. Kurtz, "Reliability and Geographic Trends of 50,000 Photovoltaic Systems in the USA," in *29th European PV Solar Energy Conference and Exhibition*, 2014.

[12] W. Hoffmann, "PV solar electricity industry: Market growth and perspective," *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 18–19, pp. 3285–3311, Nov. 2006.

[13] U.S. Energy Information Admistration, "Annual Energy Outlook 2015," DOE/EIA-038(2015), Apr. 2015.

[14] M. Z. Jacobson and M. A. Delucchi, "Providing all global energy with wind, water, and solar power, Part I: Technologies, energy resources, quantities and areas of infrastructure, and materials," *Energy Policy*, vol. 39, no. 3, pp. 1154–1169, Mar. 2011.

[15] A. Feltrin and A. Freundlich, "Material considerations for terawatt level deployment of photovoltaics," *Renew. Energy*, vol. 33, no. 2, pp. 180–185, Feb. 2008.

[16] R. C. Pietzcker, D. Stetter, S. Manger, and G. Luderer, "Using the sun to decarbonize the power sector: The economic potential of photovoltaics and concentrating solar power," *Appl. Energy*, vol. 135, pp. 704–720, Dec. 2014.

[17] “Climate Change 2001: Mitigation,” Intergovernmental Panel on Climate Change (IPCC), 2001.
[18] M. I. Hoffert, K. Caldeira, A. K. Jain, E. F. Haites, L. D. D. Harvey, S. D. Potter, M. E. Schlesinger, S. H. Schneider, R. G. Watts, T. M. L. Wigley, and D. J. Wuebbles, “Energy implications of future stabilization of atmospheric CO2 content,” *Nature*, vol. 395, no. 6705, pp. 881–884, Oct. 1998.
[19] P. Mints, “Price Point and other Ecomomic Levers Required for Over 1-TWp of PV,” SPV Market Research, Dec. 2015.
[20] J. Mayer, S. Philipps, N. S. Hussein, T. Schlegl, and C. Senkpiel, “Current and Future Cost of Photovoltaics: Long-term Scenarios for Market Development, System Prices and LCOE of Utility-Scale PV Systems,” Fraunhofer ISE, Freiburg, Germany, 2015.
[21] S. Henbest, “New Energy Outlook 2015,” Bloomberg Finance L.P., 2015.
[22] “Solar PV Module Value Chain – Market Size, Average Price, Market Share and Key Country Analysis to 2020,” GlobalData, Oct. 2014.
[23] S. Wilkinson, J. Berg, and S. von Aichberger, “Marketbuzz,” IHS Technology, Mar. 2015.
[24] “Technology Roadmap: Solar Photovoltaic Energy,” International Energy Agency, Paris, France, 2014.
[25] M. Rekinger and F. Thies, “Global Market Outlook for Solar Power 2015-2019,” SolarPower Europe.
[26] A. James, “Global PV Demand Outlook 2015-2020: Exploring Risk in Downstream Solar Markets,” GTM Research.
[27] P. Gunjan, “Global Solar Power Market,” Frost & Sullivan, Jun. 2014.
[28] “Solar PV Market Analysis And Segment Forecasts to 2020,” Grand View Research, San Francisco, CA, Feb. 2014.
[29] PV Market Alliance, “Global PV Market Report,” Jun. 2015.
[30] D. M. Powell, M. T. Winkler, A. Goodrich, and T. Buonassisi, “Modeling the Cost and Minimum Sustainable Price of Crystalline Silicon Photovoltaic Manufacturing in the United States,” *IEEE J. Photovolt.*, vol. 3, no. 2, pp. 662–668, Apr. 2013.
[31] D. M. Powell, R. Fu, K. Horowitz, P. A. Basore, M. Woodhouse, and T. Buonassisi, “The capital intensity of photovoltaics manufacturing: barrier to scale and opportunity for innovation,” *Energy Environ. Sci.*, 2015.
[32] R. Fu, T. L. James, and M. Woodhouse, “Economic Measurements of Polysilicon for the Photovoltaic Industry: Market Competition and Manufacturing Competitiveness,” *IEEE J. Photovolt.*, vol. 5, no. 2, pp. 515–524, Mar. 2015.
[33] ITRPV Working Group, “International Technology Roadmap for Photovoltaic (ITRPV): 2014 Results,” SEMI PV Group, Apr. 2015.
[34] B. Burger, K. Kiefer, C. Kost, S. Nold, S. Philipps, R. Preu, T. Schlegl, G. Willeke, H. Wirth, I. Brucker, A. Häberle, V. Schacht, and W. Warmuth, “Photovoltaics Report,” Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany, Nov. 2015.
[35] C. Wadia, A. P. Alivisatos, and D. M. Kammen, “Materials Availability Expands the Opportunity for Large-Scale Photovoltaics Deployment,” *Environ. Sci. Technol.*, vol. 43, no. 6, pp. 2072–2077, Mar. 2009.
[36] M. A. Green, “Estimates of Te and In prices from direct mining of known ores,” *Prog. Photovolt. Res. Appl.*, vol. 17, no. 5, pp. 347–359, Aug. 2009.
[37] M. Woodhouse, A. Goodrich, R. Margolis, T. James, R. Dhere, T. Gessert, T. Barnes, R. Eggert, and D. Albin, “Perspectives on the pathways for cadmium telluride photovoltaic

module manufacturers to address expected increases in the price for tellurium," *Sol. Energy Mater. Sol. Cells*, vol. 115, pp. 199–212, Aug. 2013.
[38] E. Fitzgerald, A. Wankerl, and C. Schramm, *Inside Real Innovation: How the Right Approach Can Move Ideas from R&D to Market - And Get the Economy Moving*. Singapore: World Scientific, 2011.
[39] C. Zheng and D. M. Kammen, "An innovation-focused roadmap for a sustainable global photovoltaic industry," *Energy Policy*, vol. 67, pp. 159–169, Apr. 2014.
[40] T. Voituriez and X. Wang, "Real challenges behind the EU–China PV trade dispute settlement," *Clim. Policy*, vol. 15, no. 5, pp. 670–677, Sep. 2015.
[41] M. Bazilian, I. Onyeji, M. Liebreich, I. MacGill, J. Chase, J. Shah, D. Gielen, D. Arent, D. Landfear, and S. Zhengrong, "Re-considering the economics of photovoltaic power," *Renew. Energy*, vol. 53, pp. 329–338, May 2013.
[42] A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, T. L. James, and M. Woodhouse, "A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs," *Sol. Energy Mater. Sol. Cells*, vol. 114, pp. 110–135, Jul. 2013.
[43] M. Muhlbauer, A. Piechulla, C. Voyer, M. Citro, R. Dahl, and P. Fath, "Industrial low-pressure phosphorus diffusion for high performance and excellent uniformity," in *26th European International Conference on Photovoltaic Solar Energy, 5-9 Sept. 2011*, 2011, pp. 2028–30.
[44] M. Sheoran, M. Emsley, M. Yuan, D. Ramappa, and P. Sullivan, "Ion-implant doped large-area n-type Czochralski high-efficiency industrial solar cells," in *2012 38th IEEE Photovoltaic Specialists Conference (PVSC)*, 2012, pp. 002254–002257.
[45] E. Cho, Y. Ok, K. Ryu, B. Rounsaville, A. D. Upadhyaya, V. Upadhyaya, and A. Rohatgi, "Comparison of POCl3 diffusion with phosphorus ion implantation for Czochralski and Quasi-mono silicon solar cells," in *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th*, 2014, pp. 2966–2968.
[46] J. Engelhardt, A. Frey, S. Gloger, G. Hahn, and B. Terheiden, "Passivating boron silicate glasses for co-diffused high-efficiency n-type silicon solar cell application," *Appl. Phys. Lett.*, vol. 107, no. 4, p. 042102 (4 pp.), Jul. 2015.
[47] T. Rachow, N. Milenkovic, B. Steinhauser, J. Benick, S. Janz, M. Hermle, and S. Reber, "Solar Cells with Epitaxial or Gas Phase Diffused Emitters above 21% Efficiency," in *5th International Conference on Silicon Photovoltaics, SiliconPV 2015, March 25, 2015 - March 27, 2015*, 2015, vol. 77, pp. 540–545.
[48] P. G. Borden, L. Xu, B. McDougall, C. P. Chang, D. Pysch, P. Voisin, and S. W. Glunz, "Polysilicon tunnel junctions as alternates to diffused junctions," in *Proceedings of the 23rd European Photovoltaic Solar Energy Conference*, Valencia, Spain, 2008.
[49] E. Schneiderlöchner, R. Preu, R. Lüdemann, and S. W. Glunz, "Laser-fired rear contacts for crystalline silicon solar cells," *Prog. Photovolt. Res. Appl.*, vol. 10, no. 1, pp. 29–34, Jan. 2002.
[50] J. He, S. Hegedus, U. Das, Z. Shu, M. Bennett, L. Zhang, and R. Birkmire, "Laser-fired contact for n-type crystalline Si solar cells: Laser-fired contact for Si solar cells," *Prog. Photovolt. Res. Appl.*, vol. 23, no. 9, pp. 1091–1099, Sep. 2015.
[51] M. Graf, J. Nekarda, F. L. Togny, A. Streek, R. Bohme, and R. Preu, "Comprehensive Simulation and Acceleration of the Foil-metallization Laser Process," *Energy Procedia*, vol. 77, pp. 694–700, Aug. 2015.

[52] S. Peters, “Rapid Thermal Processing of Crystalline Silicon Materials and Solar Cells,” Ph.D., University of Konstanz, Konstanz, Germany, 2004.
[53] “Breakthrough Furnace can Cut Solar Industry Costs,” National Renewable Energy Laborartory, Golden, CO, USA, NREL/FS-6A42-59012, Aug. 2013.
[54] S. A. Mann, M. J. de Wild-Scholten, V. M. Fthenakis, W. G. J. H. M. van Sark, and W. C. Sinke, “The energy payback time of advanced crystalline silicon PV modules in 2020: a prospective study,” *Prog. Photovolt. Res. Appl.*, vol. 22, no. 11, pp. 1180–1194, Nov. 2014.
[55] “Plug and Play: Purchase, Install, and Connect Residential Solar Power in Hours,” *Energy.gov*. [Online]. Available: http://energy.gov/eere/success-stories/articles/plug-and-play-purchase-install-and-connect-residential-solar-power. [Accessed: 26-Jan-2016].
[56] “DUOMAX Series Dual Glass Module | Trina Solar USA.” [Online]. Available: http://www.trinasolar.com/us/product/PDG5.html. [Accessed: 26-Jan-2016].
[57] T. Buck, R. Kopecek, J. Libal, R. Petres, K. Peter, I. Rover, K. Wambach, L. J. Geerligs, E. Wefringhaus, and P. Fath, “Large Area Screen Printed N-Type MC-SI Solar cells With B-Emitter: Efficiencies Close to 15% and Innovative Module Interconnection,” in *Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion*, 2006, vol. 1, pp. 1060–1063.
[58] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, “Solar cell efficiency tables (version 47),” *Prog. Photovolt. Res. Appl.*, vol. 24, no. 1, pp. 3–11, Jan. 2016.
[59] “Hanwha Q CELLS confirms 19.1% cell efficiencies with 1366’s ‘Direct Wafer’ technology,” *PV-Tech*, 04-Nov-2015. [Online]. Available: http://www.pv-tech.org/news/hanwha_q_cells_confirms_19.1_cell_efficiencies_with_1366s_direct_wafer_tech. [Accessed: 08-Nov-2015].
[60] B. Terheiden, T. Ballmann, R. Horbelt, Y. Schiele, S. Seren, J. Ebser, G. Hahn, V. Mertens, M. B. Koentopp, M. Scherff, J. W. Müller, Z. C. Holman, A. Descoeudres, S. D. Wolf, S. M. de Nicolas, J. Geissbuehler, C. Ballif, B. Weber, P. Saint-Cast, M. Rauer, C. Schmiga, S. W. Glunz, D. J. Morrison, S. Devenport, D. Antonelli, C. Busto, F. Grasso, F. Ferrazza, E. Tonelli, and W. Oswald, “Manufacturing 100-µm-thick silicon solar cells with efficiencies greater than 20% in a pilot production line,” *Phys. Status Solidi A*, vol. 212, no. 1, pp. 13–24, Jan. 2015.
[61] C. Gay, “Significant research and technical paths for silicon: beyond DOE Sunshot goals,” presented at the 25th Workshop on Crystalline Silicon Solar Cells and Modules, Keystone, CO, USA, 29-Jul-2015.
[62] F. Schindler, B. Michl, A. Kleiber, H. Steinkemper, J. Schon, W. Kwapil, P. Krenckel, S. Riepe, W. Warta, and M. C. Schubert, “Potential Gain in Multicrystalline Silicon Solar Cell Efficiency by n-Type Doping,” *IEEE J. Photovolt.*, vol. 5, no. 2, pp. 499–506, Mar. 2015.
[63] G. Fisher, M. R. Seacrist, and R. W. Standley, “Silicon Crystal Growth and Wafer Technologies,” *Proc. IEEE*, vol. 100, no. Special Centennial Issue, pp. 1454–1474, May 2012.
[64] M. Kivambe, D. M. Powell, S. Castellanos, M. Ann Jensen, A. E. Morishige, K. Nakajima, K. Morishita, R. Murai, and T. Buonassisi, “Minority-carrier lifetime and defect content of n-type silicon grown by the noncontact crucible method,” *J. Cryst. Growth*, vol. 407, pp. 31–36, Dec. 2014.
[65] R. M. Swanson, “Approaching the 29% limit efficiency of silicon solar cells,” in *Conference Record of the Thirty-first IEEE Photovoltaic Specialists Conference, 2005*, 2005, pp. 889–894.

[66] “Energy Department Announces $12 Million to Accelerate Record-Breaking Solar Cell Efficiency.” [Online]. Available: http://apps1.eere.energy.gov/news/progress_alerts.cfm/news_id=20465. [Accessed: 29-Dec-2015].
[67] I. Haedrich, M. Wiese, B. Thaidigsman, D. Eberlein, F. Clement, U. Eitner, R. Preu, and H. Wirth, “Minimizing the Optical Cell-to-module Losses for MWT-modules,” *Energy Procedia*, vol. 38, pp. 355–361, 2013.
[68] I. Haedrich, U. Eitner, M. Wiese, and H. Wirth, “Unified methodology for determining CTM ratios: Systematic prediction of module power,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 14–23, Dec. 2014.
[69] J. Muller, D. Hinken, S. Blankemeyer, H. Kohlenberg, U. Sonntag, K. Bothe, T. Dullweber, M. Kontges, and R. Brendel, “Resistive Power Loss Analysis of PV Modules Made From Halved 15.6 x 15.6 cm^2 Silicon PERC Solar Cells With Efficiencies up to 20.0%,” *IEEE J. Photovolt.*, vol. 5, no. 1, pp. 189–194, Jan. 2015.
[70] ITRPV Working Group, “International Technology Roadmap for Photovoltaic (ITRPV): 2015 Results,” SEMI PV Group, Mar. 2016.
[71] C. C. Hsieh, Y. C. Wu, A. Lan, H. P. Hsu, C. Hsu, and C. W. Lan, “Comparison of defect formations in solar silicon growth from small random and large oriented seeds,” *J. Cryst. Growth*, vol. 419, pp. 1–6, Jun. 2015.
[72] J. Bauer, A. Hahnel, P. Werner, N. Zakharov, H. Blumtritt, A. Zuschlag, and O. Breitenstein, “Recombination at Lomer Dislocations in Multicrystalline Silicon for Solar Cells,” *IEEE J. Photovolt.*, vol. PP, no. 99, pp. 1–11, 2015.
[73] M. Rinio, A. Yodyungyong, S. Keipert-Colberg, D. Borchert, and A. Montesdeoca-Santana, “Recombination in ingot cast silicon solar cells,” *Phys. Status Solidi A*, vol. 208, no. 4, pp. 760–768, 2011.
[74] M. I. Bertoni, D. P. Fenning, M. Rinio, V. Rose, M. Holt, J. Maser, and T. Buonassisi, “Nanoprobe X-ray fluorescence characterization of defects in large-area solar cells,” *Energy Environ. Sci.*, vol. 4, no. 10, pp. 4252–4257, Sep. 2011.
[75] J. Schön, F. Schindler, W. Kwapil, M. Knörlein, P. Krenckel, S. Riepe, W. Warta, and M. C. Schubert, “Identification of the most relevant metal impurities in mc n-type silicon for solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 107–115, Nov. 2015.
[76] Y. M. Yang, A. Yu, B. Hsu, W. C. Hsu, A. Yang, and C. W. Lan, “Development of high-performance multicrystalline silicon for photovoltaic industry,” *Prog. Photovolt. Res. Appl.*, vol. 23, no. 3, pp. 340–351, Mar. 2015.
[77] D. Zhu, L. Ming, M. Huang, Z. Zhang, and X. Huang, “Seed-assisted growth of high-quality multi-crystalline silicon in directional solidification,” *J. Cryst. Growth*, vol. 386, pp. 52–56, Jan. 2014.
[78] S. Fu, Z. Xiong, Z. Feng, P. J. Verlinden, and Q. Huang, “Cell Performance Prediction based on the Wafer Quality,” *Energy Procedia*, vol. 38, pp. 43–48, 2013.
[79] Y. Miyamura, H. Harada, K. Jiptner, S. Nakano, B. Gao, K. Kakimoto, K. Nakamura, Y. Ohshita, A. Ogura, S. Sugawara, and T. Sekiguchi, “Advantage in solar cell efficiency of high-quality seed cast mono Si ingot,” *Appl. Phys. Express*, vol. 8, no. 6, p. 62301, Jun. 2015.
[80] M. Trempa, C. Reimann, J. Friedrich, G. Müller, A. Krause, L. Sylla, and T. Richter, “Influence of grain boundaries intentionally induced between seed plates on the defect generation in quasi-mono-crystalline silicon ingots: Influence of grain boundaries

intentionally induced between seed plates," *Cryst. Res. Technol.*, vol. 50, no. 1, pp. 124–132, Jan. 2015.
[81] E. Kobayashi, Y. Watabe, R. Hao, and T. S. Ravi, "High efficiency heterojunction solar cells on n-type kerfless mono crystalline silicon wafers by epitaxial growth," *Appl. Phys. Lett.*, vol. 106, no. 22, p. 223504, Jun. 2015.
[82] E. Kobayashi, Y. Watabe, R. Hao, and T. S. Ravi, "Efficient Heterojunction Solar Cells on n-type Epitaxial Kerfless Silicon Wafers," in *Proceedings of the 31st European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2015.
[83] A. Lorenz, "1366 Direct Wafer: Demolishing the Cost Barrier for Silicon Photovoltaics," 1366 Technologies, DOE-1366-04738, Aug. 2013.
[84] U. Hess, P. Y. Pichon, S. Seren, A. Schonecker, and G. Hahn, "Crystal defects and their impact on ribbon growth on substrate (RGS) silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 117, pp. 471–5, Oct. 2013.
[85] G. Hahn and A. Schönecker, "New crystalline silicon ribbon materials for photovoltaics," *J. Phys. Condens. Matter*, vol. 16, no. 50, p. R1615, Dec. 2004.
[86] K. Nakajima, R. Murai, S. Ono, K. Morishita, M. M. Kivambe, D. M. Powell, and T. Buonassisi, "Shape and quality of Si single bulk crystals grown inside Si melts using the noncontact crucible method," *Jpn. J. Appl. Phys.*, vol. 54, no. 1, p. 15504, Jan. 2015.
[87] W. Deng, F. Ye, Z. Xiong, D. Chen, W. Guo, Y. Chen, Y. Yang, P. P. Altermatt, Z. Feng, and P. J. Verlinden, "Development of high-efficiency industrial p-type multi-crystalline PERC solar cells with efficiency greater than 21%," *Energy Procedia*, under review.
[88] W. Deng, D. Chen, Z. Xiong, J. Dong, Y. Feng, H. Li, H. Zhu, M. Zhong, Y. Yang, Y. Chen, Z. Feng, P. P. Altermatt, and P. J. Verlinden, "20.8% efficient PERC solar cell on 156 mm×156 mm p-type multi-crystalline silicon substrate," in *Photovoltaic Specialist Conference (PVSC), 2015 IEEE 42nd*, 2015, pp. 1–6.
[89] Crystal Solar, "Imec and Crystal Solar Demonstrate 22.5 Percent nPERT Si Solar Cells on Kerfless Epitaxial Wafers." [Online]. Available: http://www.prnewswire.com/news-releases/imec-and-crystal-solar-demonstrate-225-percent-npert-si-solar-cells-on-kerfless-epitaxial-wafers-300251309.html. [Accessed: 15-Apr-2016].
[90] H. Alexander and H. Teichler, "Dislocations," in *Handbook of Semiconductor Technology Set*, K. A. Jackson and W. Schröter, Eds. Wiley-VCH Verlag GmbH, 2000, pp. 291–376.
[91] D. Hull and D. J. Bacon, *Introduction to dislocations*. Oxford: Butterworth-Heinemann, 2011.
[92] V. Kveder and M. Kittler, "Dislocations in Silicon and D-Band Luminescence for Infrared Light Emitters," *Mater. Sci. Forum*, vol. 590, pp. 29–56, 2008.
[93] A. Bourret, J. Desseaux, and A. Renault, "Core structure of the Lomer dislocation in germanium and silicon," *Philos. Mag. A*, vol. 45, no. 1, pp. 1–20, Jan. 1982.
[94] B. Ziebarth, M. Mrovec, C. Elsässer, and P. Gumbsch, "Interstitial iron impurities at cores of dissociated dislocations in silicon," *Phys. Rev. B*, vol. 92, no. 19, p. 195308, Nov. 2015.
[95] V. Kveder, M. Kittler, and W. Schröter, "Recombination activity of contaminated dislocations in silicon: A model describing electron-beam-induced current contrast behavior," *Phys. Rev. B*, vol. 63, no. 11, Mar. 2001.
[96] A. A. Istratov, T. Buonassisi, M. D. Pickett, M. Heuer, and E. R. Weber, "Control of metal impurities in 'dirty' multicrystalline silicon for solar cells," *Mater. Sci. Eng. B*, vol. 134, no. 2–3, pp. 282–286, Oct. 2006.

[97] J. Schmidt, B. Lim, D. Walter, K. Bothe, S. Gatz, T. Dullweber, and P. P. Altermatt, “Impurity-Related Limitations of Next-Generation Industrial Silicon Solar Cells,” *IEEE J. Photovolt.*, vol. 3, no. 1, pp. 114–118, Jan. 2013.
[98] G. Coletti, “Sensitivity of state-of-the-art and high efficiency crystalline silicon solar cells to metal impurities: Sensitivity of crystalline silicon solar cells to metal impurities,” *Prog. Photovolt. Res. Appl.*, p. n/a-n/a, Mar. 2012.
[99] B. Sopori, “Silicon solar-cell processing for minimizing the influence of impurities and defects,” *J. Electron. Mater.*, vol. 31, no. 10, pp. 972–980, Oct. 2002.
[100] M. Trushin, O. Vyvenko, W. Seifert, M. Kittler, I. Zizak, A. Erko, M. Seibt, and C. Rudolf, “Combined XBIC/μ-XRF/μ-XAS/DLTS investigation of chemical character and electrical properties of Cu and Ni precipitates in silicon,” *Phys. Status Solidi C*, vol. 6, no. 8, pp. 1868–1873, Aug. 2009.
[101] M. Kittler, C. Ulhaq-Bouillet, and V. Higgs, “Recombination activity of ‘clean’ and contaminated misfit dislocations in Si (Ge) structures,” *Mater. Sci. Eng. B*, vol. 24, no. 1, pp. 52–55, 1994.
[102] M. Kittler and W. Seifert, “Two types of electron-beam-induced current behaviour of misfit dislocations in Si (Ge): experimental observations and modelling,” *Mater. Sci. Eng. B*, vol. 24, no. 1, pp. 78–81, 1994.
[103] G. Stokkan, S. Riepe, O. Lohne, and W. Warta, “Spatially resolved modeling of the combined effect of dislocations and grain boundaries on minority carrier lifetime in multicrystalline silicon,” *J. Appl. Phys.*, vol. 101, no. 5, p. 53515, 2007.
[104] Y. Miyamura, H. Harada, S. Ito, J. Chen, and T. Sekiguchi, “Structural Study of Small Angle Grain Boundaries in Multicrystalline Si,” *Mater. Sci. Forum*, vol. 725, pp. 157–160, Jul. 2012.
[105] D. Oriwol, E.-R. Carl, A. N. Danilewsky, L. Sylla, W. Seifert, M. Kittler, and H. S. Leipner, “Small-angle subgrain boundaries emanating from dislocation pile-ups in multicrystalline silicon studied with synchrotron white-beam X-ray topography,” *Acta Mater.*, vol. 61, no. 18, pp. 6903–6910, Oct. 2013.
[106] J. Chen and T. Sekiguchi, “Carrier recombination activity and structural properties of small-angle grain boundaries in multicrystalline silicon,” *Jpn. J. Appl. Phys.*, vol. 46, no. 10R, p. 6489, 2007.
[107] J. Chen, T. Sekiguchi, D. Yang, F. Yin, K. Kido, and S. Tsurekawa, “Electron-beam-induced current study of grain boundaries in multicrystalline silicon,” *J. Appl. Phys.*, vol. 96, no. 10, pp. 5490–5495, Nov. 2004.
[108] Z.-J. Wang, S. Tsurekawa, K. Ikeda, T. Sekiguchi, and T. Watanabe, “Relationship between Electrical Activity and Grain Boundary Structural Configuration in Polycrystalline Silicon,” *Interface Sci.*, vol. 7, no. 2, pp. 197–205, Aug. 1999.
[109] T. Buonassisi, A. A. Istratov, M. D. Pickett, M. A. Marcus, T. F. Ciszek, and E. R. Weber, “Metal precipitation at grain boundaries in silicon: Dependence on grain boundary character and dislocation decoration,” *Appl. Phys. Lett.*, vol. 89, no. 4, p. 42102, 2006.
[110] M. I. Bertoni, S. Hudelson, B. K. Newman, D. P. Fenning, H. F. Dekkers, E. Cornagliotti, A. Zuschlag, G. Micard, G. Hahn, G. Coletti, and others, “Influence of defect type on hydrogen passivation efficacy in multicrystalline silicon solar cells,” *Prog. Photovolt. Res. Appl.*, vol. 19, no. 2, pp. 187–191, 2011.
[111] T. Sameshima, N. Miyazaki, Y. Tsuchiya, H. Hashiguchi, T. Tachibana, T. Kojima, Y. Ohshita, K. Arafune, and A. Ogura, “Interaction between Metal Impurities and Small-Angle

Grain Boundaries on Recombination Properties in Multicrystalline Silicon for Solar Cells," *Appl. Phys. Express*, vol. 5, no. 4, p. 42301, Apr. 2012.
[112] T. Kojima, T. Tachibana, Y. Ohshita, R. R. Prakash, T. Sekiguchi, and M. Yamaguchi, "Temperature-dependent recombination velocity analysis on artificial small angle grain boundaries using electron beam induced current method," *J. Appl. Phys.*, vol. 119, no. 6, p. 65302, Feb. 2016.
[113] W. Seifert, G. Morgenstern, and M. Kittler, "Influence of dislocation density on recombination at grain boundaries in multicrystalline silicon," *Semicond. Sci. Technol.*, vol. 8, no. 9, p. 1687, 1993.
[114] C. Donolato, "Modeling the effect of dislocations on the minority carrier diffusion length of a semiconductor," *J. Appl. Phys.*, vol. 84, no. 5, pp. 2656–2664, 1998.
[115] M. Lax, "Junction current and luminescence near a dislocation or a surface," *J. Appl. Phys.*, vol. 49, no. 5, pp. 2796–2810, May 1978.
[116] S. Riepe, G. Stokkan, T. Kieliba, and W. Warta, "Carrier density imaging as a tool for characterising the electrical activity of defects in pre-processed multicrystalline silicon," *Solid State Phenom.*, vol. 95–96, pp. 229–234, 2004.
[117] V. Budhraja, B. Sopori, N. Ravindra, and D. Misra, "Improved dislocation model of silicon solar cells with the effect of front and back surface recombination velocity," *Prog. Photovolt. Res. Appl.*, vol. 22, no. 12, pp. 1256–1266, Dec. 2014.
[118] C. Van Opdorp, A. T. Vink, and C. Werkhoven, "Minority carrier recombination at surfaces, dislocations and microdefects: evaluation of parameters from near band edge luminescence," in *Proceedings of the 6th International Symposium on Gallium Arsenide and related compounds, St. Louis, MO, USA*, 1976, pp. 317–330.
[119] W. Shockley and W. T. Read Jr, "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, p. 835, 1952.
[120] R. N. Hall, "Electron-hole recombination in germanium," *Phys. Rev.*, vol. 87, no. 2, p. 387, 1952.
[121] P. R. Wilshaw and G. R. Booker, "New results and an interpretation for SEM EBIC contrast arising from individual dislocations in silicon," in *Microscopy of Semiconducting Materials, 1985. Royal Microscopical Society Conference, 25-27 March 1985*, 1985, pp. 329–36.
[122] B. L. Sopori, "Defect Clusters in Silicon: Impact on the Performance of Large-Area Devices," *Mater. Sci. Forum*, vol. 258–263, pp. 527–534, 1997.
[123] B. Sopori, V. Budhraja, P. Rupnowski, S. Johnston, N. Call, H. Moutinho, and M. Al-Jassim, "Defect clusters in multicrystalline silicon: Their nature and influence on the solar cell performance," in *Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE*, 2009, pp. 1969–1974.
[124] H. C. Sio, T. Trupke, and D. Macdonald, "Quantifying carrier recombination at grain boundaries in multicrystalline silicon wafers through photoluminescence imaging," *J. Appl. Phys.*, vol. 116, no. 24, p. 244905, Dec. 2014.
[125] G. Micard, G. Hahn, A. Zuschlag, S. Seren, and B. Terheiden, "Quantitative evaluation of grain boundary activity in multicrystalline semiconductors by light beam induced current: An advanced model," *J. Appl. Phys.*, vol. 108, no. 3, p. 34516, 2010.
[126] W. K. Metzger, "How lifetime fluctuations, grain-boundary recombination, and junctions affect lifetime measurements and their correlation to silicon solar cell performance," *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 9, pp. 1123–1135, Sep. 2008.

[127] R. Corkish, P. P. Altermatt, and G. Heiser, “Numerical simulation of electron-beam-induced current near a silicon grain boundary and impact of a p–n junction space charge region,” *Sol. Energy Mater. Sol. Cells*, vol. 65, no. 1–4, pp. 63–69, Jan. 2001.
[128] R. Corkish, T. Puzzer, A. B. Sproul, and K. L. Luke, “Quantitative interpretation of electron-beam-induced current grain boundary contrast profiles with application to silicon,” *J. Appl. Phys.*, vol. 84, no. 10, pp. 5473–5481, Nov. 1998.
[129] M. Imaizumi, T. Ito, M. Yamaguchi, and K. Kaneko, “Effect of grain size and dislocation density on the performance of thin film polycrystalline silicon solar cells,” *J. Appl. Phys.*, vol. 81, no. 11, p. 7635, 1997.
[130] B. Ba, M. Kane, and J. Sarr, “Modelling recombination current in polysilicon solar cell grain boundaries,” *Sol. Energy Mater. Sol. Cells*, vol. 80, no. 2, pp. 143–154, Oct. 2003.
[131] C. H. Seager, “Grain boundary recombination: Theory and experiment in silicon,” *J. Appl. Phys.*, vol. 52, no. 6, pp. 3960–3968, Jun. 1981.
[132] S. A. Edmiston, G. Heiser, A. B. Sproul, and M. A. Green, “Improved modeling of grain boundary recombination in bulk and p-n junction regions of polycrystalline silicon solar cells,” *J. Appl. Phys.*, vol. 80, no. 12, p. 6783, 1996.
[133] E. Christoffel, M. Rusu, A. Zerga, S. Bourdais, S. Noël, and A. Slaoui, “A two-dimensional modeling of the fine-grained polycrystalline silicon thin-film solar cells,” *Thin Solid Films*, vol. 403–404, pp. 258–262, Feb. 2002.
[134] M. G. Deceglie, M. D. Kelzenberg, and H. A. Atwater, “Effects of bulk and grain boundary recombination on the efficiency of columnar-grained crystalline silicon film solar cells,” in *2010 35th IEEE Photovoltaic Specialists Conference (PVSC)*, 2010, pp. 001487–001490.
[135] P. P. Altermatt and G. Heiser, “Development of a three-dimensional numerical model of grain boundaries in highly doped polycrystalline silicon and applications to solar cells,” *J. Appl. Phys.*, vol. 91, no. 7, p. 4271, 2002.
[136] P. P. Altermatt and G. Heiser, “Predicted electronic properties of polycrystalline silicon from three-dimensional device modeling combined with defect-pool model,” *J. Appl. Phys.*, vol. 92, no. 5, p. 2561, 2002.
[137] H. Wagner, M. Müller, G. Fischer, and P. P. Altermatt, “A simple criterion for predicting multicrystalline Si solar cell performance from lifetime images of wafers prior to cell production,” *J. Appl. Phys.*, vol. 114, no. 5, p. 54501, Aug. 2013.
[138] B. Michl, M. Rüdiger, J. A. Giesecke, M. Hermle, W. Warta, and M. C. Schubert, “Efficiency limiting bulk recombination in multicrystalline silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 98, pp. 441–447, Mar. 2012.
[139] A. Ingenito, O. Isabella, S. Solntsev, and M. Zeman, “Accurate opto-electrical modeling of multi-crystalline silicon wafer-based solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 123, pp. 17–29, Apr. 2014.
[140] A. K. Ghosh, C. Fishman, and T. Feng, “Theory of the electrical and photovoltaic properties of polycrystalline silicon,” *J. Appl. Phys.*, vol. 51, no. 1, p. 446, 1980.
[141] D. Berney Needleman, H. Wagner, P. P. Altermatt, and T. Buonassisi, “Assessing the Device-performance Impacts of Structural Defects with TCAD Modeling,” *Energy Procedia*, vol. 77, pp. 8–14, Aug. 2015.
[142] X. Gu, X. Yu, K. Guo, L. Chen, D. Wang, and D. Yang, “Seed-assisted cast quasi-single crystalline silicon for photovoltaic application: Towards high efficiency and low cost silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 101, pp. 95–101, Jun. 2012.

[143] “Sentaurus Device User Guide,” Synopsys, Version H-2013.03, Mar. 2013.
[144] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2005.
[145] P. P. Altermatt, “Models for numerical device simulations of crystalline silicon solar cells—a review,” *J. Comput. Electron.*, vol. 10, no. 3, pp. 314–330, Sep. 2011.
[146] A. Fell, K. R. McIntosh, P. P. Altermatt, G. J. M. Janssen, R. Stangl, A. Ho-Baillie, H. Steinkemper, J. Greulich, M. Muller, B. Min, K. C. Fong, M. Hermle, I. G. Romijn, and M. D. Abbott, “Input Parameters for the Simulation of Silicon Solar Cells in 2014,” *IEEE J. Photovolt.*, pp. 1–14, 2015.
[147] H. Wagner, T. Ohrdes, A. Dastgheib-Shirazi, B. Puthen-Veettil, D. König, and P. P. Altermatt, “A numerical simulation study of gallium-phosphide/silicon heterojunction passivated emitter and rear solar cells,” *J. Appl. Phys.*, vol. 115, no. 4, p. 44508, Jan. 2014.
[148] Z. P. Ling, S. Duttagupta, F. Ma, T. Mueller, A. G. Aberle, and R. Stangl, “Three-dimensional numerical analysis of hybrid heterojunction silicon wafer solar cells with heterojunction rear point contacts,” *AIP Adv.*, vol. 5, no. 7, p. 77124, Jul. 2015.
[149] M. Filipič, Z. C. Holman, F. Smole, S. De Wolf, C. Ballif, and M. Topič, “Analysis of lateral transport through the inversion layer in amorphous silicon/crystalline silicon heterojunction solar cells,” *J. Appl. Phys.*, vol. 114, no. 7, p. 74504, 2013.
[150] S. C. Baker-Finch and K. R. McIntosh, “A freeware program for precise optical analysis of the front surface of a solar cell,” in *2010 35th IEEE Photovoltaic Specialists Conference (PVSC)*, 2010, pp. 002184–002187.
[151] M. A. Green, “Lambertian light trapping in textured solar cells and light-emitting diodes: analytical solutions,” *Prog. Photovolt. Res. Appl.*, vol. 10, no. 4, pp. 235–241, Jun. 2002.
[152] J. Wong, “Griddler: Intelligent computer aided design of complex solar cell metallization patterns,” in *Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th*, 2013, pp. 0933–0938.
[153] M. A. Green, *Solar cells : operating principles, technology, and system applications*. Englewood Cliffs, NJ : Prentice-Hall, c1982., 1982.
[154] H. Haug, M. S. Wiig, R. Søndenå, and J. Wong, “Simulating the effect of lifetime non-uniformity on solar cell performance using cmd-PC1D 6 and Griddler 2,” *Energy Procedia*, under review.
[155] D. Berney Needleman, H. Wagner, P. P. Altermatt, and T. Buonassisi, “3-D TCAD Modeling of Grain Boundaries in High-efficiency Silicon Solar Cells,” under review.
[156] A. Augusto, D. Pera, H. J. Choi, P. Bellanger, M. C. Brito, J. Maia Alves, A. M. Vallera, T. Buonassisi, and J. M. Serra, “Residual stress and dislocations density in silicon ribbons grown via optical zone melting,” *J. Appl. Phys.*, vol. 113, no. 8, p. 83510, 2013.
[157] D. Berney Needleman, H. Choi, D. M. Powell, and T. Buonassisi, “Rapid dislocation-density mapping of as-cut crystalline silicon wafers,” *Phys. Status Solidi RRL – Rapid Res. Lett.*, vol. 7, no. 12, pp. 1041–1044, 2013.
[158] T. Lehmann, C. Reimann, E. Meissner, and J. Friedrich, “Clarification of the relation between the grain structure of industrial grown mc-Si and the area fraction of electrical active defects by means of statistical grain structure evaluation,” *Acta Mater.*, vol. 106, pp. 98–105, Mar. 2016.
[159] J. Rand, G. Rozgonyi, J. Lu, and R. Reedy, “Characterization of Silicon-Film trade; sheet material,” in *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference, 2002*, 2002, pp. 98–101.

[160] H. C. Sio, S. P. Phang, T. Trupke, and D. Macdonald, “Impact of Phosphorous Gettering and Hydrogenation on the Surface Recombination Velocity of Grain Boundaries in p-Type Multicrystalline Silicon,” *IEEE J. Photovolt.*, vol. PP, no. 99, pp. 1–9, 2015.
[161] H. C. Sio and D. Macdonald, “Direct comparison of the electrical properties of multicrystalline silicon materials for solar cells: conventional p-type, n-type and high performance p-type,” *Sol. Energy Mater. Sol. Cells*, vol. 144, pp. 339–346, Jan. 2016.
[162] S. Steingrube, O. Breitenstein, K. Ramspeck, S. Glunz, A. Schenk, and P. P. Altermatt, “Explanation of commonly observed shunt currents in c-Si solar cells by means of recombination statistics beyond the Shockley-Read-Hall approximation,” *J. Appl. Phys.*, vol. 110, no. 1, pp. 14515–14515, 2011.
[163] J. Wong, J. L. Huang, S. Varlamov, M. A. Green, R. Evans, M. Keevers, and R. J. Egan, “Structural inhomogeneities in polycrystalline silicon on glass solar cells and their effects on device characteristics,” *Prog. Photovolt. Res. Appl.*, vol. 19, no. 6, pp. 695–705, Sep. 2011.
[164] K. E. Ekstrøm, G. Stokkan, R. Søndenå, H. Dalaker, T. Lehmann, L. Arnberg, and M. Di Sabatino, “Structure and dislocation development in mono-like silicon: Structure and dislocation development in mono-like silicon,” *Phys. Status Solidi A*, vol. 212, no. 10, pp. 2278–2288, Oct. 2015.
[165] R. Søndenå, K. E. Ekstrøm, G. Stokkan, H. Dalaker, T. Lehmann, L. Arnberg, and M. Di Sabatino, “Effect of phosphorus gettering on quasi-single crystalline silicon wafers,” in *Proceedings of the 30th European Photovoltaic Solar Energy Conference*, 2015.
[166] R. A. Sinton and A. Cuevas, “Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data,” *Appl. Phys. Lett.*, vol. 69, no. 17, pp. 2510–2512, Oct. 1996.
[167] S. Herlufsen, J. Schmidt, D. Hinken, K. Bothe, and R. Brendel, “Photoconductance-calibrated photoluminescence lifetime imaging of crystalline silicon,” *Phys. Status Solidi RRL - Rapid Res. Lett.*, vol. 2, no. 6, pp. 245–247, Dec. 2008.
[168] J. A. Giesecke, M. C. Schubert, B. Michl, F. Schindler, and W. Warta, “Minority carrier lifetime imaging of silicon wafers calibrated by quasi-steady-state photoluminescence,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 3, pp. 1011–1018, Mar. 2011.
[169] H. C. Sio, S. P. Phang, T. Trupke, and D. Macdonald, “An accurate method for calibrating photoluminescence-based lifetime images on multi-crystalline silicon wafers,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 77–84, Dec. 2014.
[170] J. D. Murphy, K. Bothe, R. Krain, V. V. Voronkov, and R. J. Falster, “Parameterisation of injection-dependent lifetime measurements in semiconductors in terms of Shockley-Read-Hall statistics: An application to oxide precipitates in silicon,” *J. Appl. Phys.*, vol. 111, no. 11, p. 113709, Jun. 2012.
[171] R. A. Sinton and A. Cuevas, “A quasi-steady-state open-circuit voltage method for solar cell characterization,” in *Proceedings of the 16th European Photovoltaic Solar Energy Conference*, Glasgow, UK, 2000.
[172] M. J. Kerr, A. Cuevas, and R. A. Sinton, “Generalized analysis of quasi-steady-state and transient decay open circuit voltage measurements,” *J. Appl. Phys.*, vol. 91, no. 1, pp. 399–404, Jan. 2002.