

Adaptable Power Conversion for Grid and Microgrid Applications

by

Wardah Inam

B.S. Electronics Engineering, GIK Institute (2010)

S.M. EECS, Massachusetts Institute of Technology (2013)

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Author
Department of Electrical Engineering and Computer Science
May 20, 2016

Certified by.....
David J. Perreault
Professor, Department of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by.....
Khurram K. Afridi
Assistant Professor, University of Colorado Boulder
Thesis Supervisor

Accepted by
Leslie A. Kolodzeijski
Chair, Committee on Graduate Students

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Abstract

Power electronics convert and control power and are an essential part of many electronic devices and systems. Increasingly, power converters need to operate over widely varying operating conditions (voltage, current and power level), which can degrade their performance. In many applications, power converters are also being interconnected to form power systems. This is challenging as the converters may have to operate in various configurations. In order to ensure best performance, power converters and systems need to adapt to the operating conditions by adjusting topology, component values or control characteristics. In this thesis, two applications are considered: universal input power supplies and off-grid electrification.

More than 3 billion power supplies were sold worldwide in 2014 [1], with efficiencies ranging from 50-90% [2], which results in significant energy loss. A major portion of these are universal input power supplies (designed to operate at AC line voltages found globally). In this thesis, a control technique, Variable Frequency Multiplier (VFX), is developed which compresses the effective operating range required of a resonant converter by switching the inverter and/or rectifier operation between processing energy at a fundamental frequency and one or more harmonic frequencies. This technique was applied to the inverter stage of a stacked-bridge LLC converter for a universal input power supply. An efficiency of 94.9% to 96.6% was achieved for a 50 W converter operating across the entire (4:1) input voltage range.

Even though centralized grid infrastructure is widespread, access to electricity is still limited in many parts of the developing world. More than 1.2 billion people globally do not have access to electricity [3]. In this thesis, an ad hoc modular microgrid architecture is developed and field-tested. Contrary to how conventional power systems are designed, these microgrids do not require pre-planning and can operate in any network configuration. Smart power management units have been designed to arbitrarily connect power sources and loads, forming an autonomous microgrid. Accurate power sharing of multiple power sources is demonstrated. A methodology to attain the lowest system cost by designing power converters that reduce lifetime energy loss has also been developed. This enables affordable and

reliable electricity to be provided in off-grid areas.

Improvements in these applications will have a significant impact on power utilization from the existing grid infrastructure, and will help define the future of power utilization where this infrastructure does not exist. Moreover, the techniques and designs developed, in this thesis, for adaptable and efficient operation of power converters and systems can be easily extended to other applications.

Thesis Supervisor: David J. Perreault

Title: Professor, Department of Electrical Engineering and Computer Science

Thesis Supervisor: Khurram K. Afridi

Title: Assistant Professor, University of Colorado Boulder

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Chapter 1

Introduction

Power electronics convert and control power and are an essential part of many electronic devices and systems. Increasingly, power converters need to operate over widely varying operating conditions (voltage, current and power level), which can degrade their performance. In many applications, power converters are also being interconnected to form power systems. This is challenging as the converters may be connected to operate in various configurations. In order to ensure best performance, power converters and systems need to adapt to the operating conditions by adjusting topology, component values or control characteristics.

The two main applications considered in this thesis are grid-interface power supplies and off-grid electrification. Improvements in these applications will have a significant impact on power utilization from the existing grid infrastructure, and will help define the future of power utilization where this infrastructure does not exist. The techniques and designs developed, in this thesis, for adaptable and efficient operation of power converters and systems can be easily extended to other applications.

1.1 Motivation

1.1.1 Efficient universal input power supplies

More than 3 billion power supplies were sold worldwide in 2014 [1], with efficiencies ranging from 50-90% [2]. It is estimated that power supply losses account for 20-70% of all the energy that electronic products consume; with more than 3.5 billion power supplies currently being used only in the US, this amounts to about 3-4% of all US electricity usage [6]. A major portion of these power supplies are universal input power supplies (designed to operate at AC line voltages found globally). The importance of universal input power supply design has increased significantly in the recent past because of global market expansion and wide adoption of portable electronics. In this thesis, a technique to improve efficiency of universal input power supplies, without increasing cost, is presented.

1.1.2 Ad hoc microgrids for off-grid electrification

Even though centralized ac grid infrastructure is widespread, access to electricity is still a concern in large parts of the developing world. Today, about one out of every 5 people, i.e. more than 1.3 billion people in the world, do not have access to electricity and are denied a basic standard of living [3]. This deficiency impedes most aspects of human development: health, education and economic development.

It is estimated that people who don't have access to electricity spend around 10-30% of their household income on fuel-based lighting [7]. Moreover, around a billion people are served in health facilities without electricity and cannot get adequate healthcare [8]. Furthermore, approximately 50% of children in the developing world attend schools that do not have access to electricity, which limits their learning experience [8]. Thus access to energy is crucial to improving the standard of living in developing countries.

With declining solar panel, battery and power electronics costs, the economic viability of distributed generation has improved. This opens up many new ways

of interacting with the grid or enabling energy access. The microgrids currently being deployed in off-grids areas in the developing world are centralized (with all the generation and/or storage co-located), which increases the distribution cost and limits the type of power sources connected to the grid.

In this thesis, a low-cost ad hoc microgrid architecture is developed that enables quick deployment of modular microgrids.

1.2 Background and Thesis Contribution

1.2.1 Efficient universal input power supplies

A trend in power electronics has been to strive for high power density and high efficiency across a wide operating range [9]. High power density can be achieved by switching power converters at a high frequency. At these high frequencies, resonant converters use soft switching (i.e. Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS)) to reduce switching losses to achieve high efficiency [10], [11]. Although soft-switched resonant converters can achieve high efficiency at a nominal operating point, the efficiency tends to degrade considerably with variations in input voltage, output voltage and power level [12].

Resonant converters commonly use frequency control [10], [11] and/or phase shift control [13] to compensate for variations in input voltage and power levels. If switching frequency is increased to reduce output power or gain of the converter, such as in a series resonant converter operated above resonance to maintain ZVS, switching losses increase. Also, with operation over a wide frequency range as often required in resonant converters, the magnetics cannot be optimally designed. Furthermore, circulating currents may increase proportionally as load is decreased, resulting in higher losses at light loads. With phase shift control, operation over a wide range is likewise challenging. In many resonant converters, when two legs of the inverter are phase shifted with respect to each other, they have asymmetrical current levels at the switching transitions. The leading inverter leg can lose ZCS and the lagging leg can

lose ZVS. Other control techniques such as asymmetrical current mode control [14] and asymmetrical duty cycle PWM control [15] also have limitations, such as loss of ZVS.

In this thesis, a new technique, termed as Variable Frequency Multiplier (VFX) is introduced and its effectiveness is demonstrated for a universal input power supply. In the VFX technique, additional "frequency multiplier" modes of operation of the inverter and/or rectifier are used to provide additional sets of operating characteristics for the converter to achieve and maintain high performance across a wide operating range. Frequency multiplier circuits are often used in extreme high-frequency RF applications (e.g., where transistor f_T is a concern), and are sometimes used in switched-mode inverters and power amplifiers ([16], [17]). While it has been proposed to employ frequency multipliers in dc-dc converters ([18], [19]), this is not usually done, as the output power of a frequency multiplier inverter is inherently low relative to the needed device ratings. However, frequency multiplication is used here as an additional operating mode of the inverter and/or rectifier, for wide-range voltage and/or power conditions. In this context, frequency multiplication can be used to extend the efficient operating range of a converter and to improve its performance across power and voltage.

The proposed VFX technique can be applied to the inverter and/or rectifier, for a wide input and/or output voltage range. In this thesis, its use is demonstrated for a wide input voltage range using VFX operation of the inverter, and it is shown how this technique can be applied to the rectifier. Universal input power supplies need to operate over a wide input voltage range, making it extremely challenging to design resonant power converters for such a wide range of operation. So, a VFX technique is demonstrated, which is employed in the inverter of an LLC resonant converter that is designed to operate across a 4:1 input voltage range of 85 V to 340 V. It enables rescaling of operation between 120 Vac (nominal) and 240 Vac (nominal) systems, making it particularly effective in meeting world-wide voltage standards, without adding more components.

1.2.2 Ad hoc microgrids for off-grid electrification

The lack of electricity is one of the most pressing concerns in the developing world. While there is a significant need to provide electricity access, the current technologies have not been able to scale to serve these areas. In developing countries, grid electricity is often unreliable or entirely unavailable. The governments of these countries do not have the financial resources to increase generation to meet increasing demand in grid-connected areas, let alone to electrify off-grid areas. Also, grid extension to small or remote areas can be very expensive [20]. The deployment of individual systems (such as solar home systems and diesel generators) have seen growth in recent years due to ease of deployment [21]. However, they are very expensive and require complex financing solutions. Moreover, it is difficult to extend their operation beyond what they have been originally designed for (usually only lighting and cellphone charging in a single household). Recently, centralized microgrids (all the generation and storage are co-located) have received more attention, especially in the developing world, due to the relatively low cost of electricity achieved by aggregate generation [22]. However, centralized microgrid development has its own challenges. Centralized microgrids require a high upfront capital investment to set up, leading to expensive and complex financing. Also, they traditionally require rigorous planning and participation of a large percentage of the community to be financially feasible.

Work done by Sanders et al. [23] develops a new microgrid architecture with distributed storage, however, as all the generation is co-located, a high voltage step-up for distribution is needed to reduce distribution costs. This high voltage step-up is costly and requires additional safety measures.

In this work, an ad hoc modular microgrid architecture is developed and field-tested. Contrary to how conventional power systems are designed, these microgrids do not require pre-planning and can operate in any network configuration. Smart power management units (PMUs) have been designed to arbitrarily connect power sources and loads, forming an autonomous microgrid. Accurate power sharing of multiple power sources is demonstrated. A methodology to attain the lowest system

cost by designing power converters that reduce lifetime energy loss has also been developed. This enables affordable and reliable electricity to be provided in off-grid areas.

1.3 Thesis Organization

The remainder of this thesis is organized as follows. The second chapter introduces the VFX technique and its application to bridge-type inverters and rectifiers. The third chapter presents the VFX technique applied to the dc-dc power stage of a universal input power supply and presents experimental results showing its high degree of effectiveness in this application. The fourth chapter introduces energy access and presents a case for the introduction of low-voltage dc microgrids for off-grid areas. Chapter 5 explains the ad hoc microgrid architecture that is developed. Chapter 6 deals with the design of the low-cost converters to support this dc microgrid architecture and provides details of the first prototypes built. Chapter 7 presents improvements in the design of the load converters to reduce system cost. Chapter 8 deals with the stability and power flow control of ad hoc dc microgrids. Chapter 9 concludes the thesis and presents recommendations for future research.

Chapter 2

Variable Frequency Multiplier Technique

The Variable Frequency Multiplier (VFX) technique can be applied to the inverter stage and/or rectifier stage of a resonant converter to achieve a wide input voltage and/or output voltage range operation, or to extend the efficient operating power range. In this technique, the duty ratio and the switching frequency of an inverter and/or rectifier is changed, as input and/or output voltages change such that it processes power between dc and a specific harmonic of its switching frequency (rather than just its fundamental harmonic) to create different modes of operation. By operating between dc and a higher harmonic, the dc-ac (or ac-dc) voltage gain of the inverter or rectifier changes, resulting in an added operating mode with different transfer characteristics. In the case of a frequency controlled converter, this allows the converter to be operated over a narrower (intermediate ac) frequency range for a wide voltage conversion range and/or power range. Depending on the circuit architecture, more than two modes can be created.

This chapter describes the mathematics of the VFX technique along with its application to the inverter stage and/or rectifier stage of resonant or other ac-link converters. To demonstrate the utility of this technique, we have built an LLC converter with a two-mode VFX technique applied to the inverter stage to efficiently extend the input voltage range of the converter. This would make the power stage

suitable for use in a "universal input" converter operable at 120 or 240 Vac, while only requiring a narrow-range design of the tank circuit (e.g., suitable for 120 Vac operation), thereby improving achievable efficiency. Aspects of this work have also been reported in publication [24].

2.1 Technique Applied to an Inverter

To understand the VFX technique applied to an inverter, consider the stacked bridge inverter as shown in Fig. 2-1 with an output voltage v_{inv} ($v_{inv} = v_{inv1} + V_{bus} - v_{inv2}$).

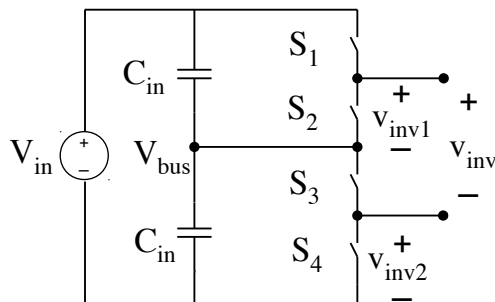


Figure 2-1: Stacked bridge inverter with input voltage V_{in} and output voltage v_{inv} .

This inverter under VFX control operates in two modes: Fundamental VFX mode (mode 1) and second harmonic VFX mode (mode 2). This change in mode is synthesized by changing the switching pattern of the inverter switches and it results in an output voltage (v_{inv}) which is of a different magnitude, hence, it changes the voltage gain of the inverter. In mode 1, there are two switching states in one switching period, as summarized in Table 2.1. In state "a" switches 1 and 4 are on, and in state "b" switches 2 and 3 are on, as shown in Fig. 2-2. Mode 1 results in twice the amplitude of the individual inverter outputs, as shown in Fig. 2-3.

Table 2.1: Switch states and the voltage of the inverter in fundamental VFX mode (Mode 1)

State	On switches	v_{inv}
a	1, 4	V_{in}
b	2, 3	0

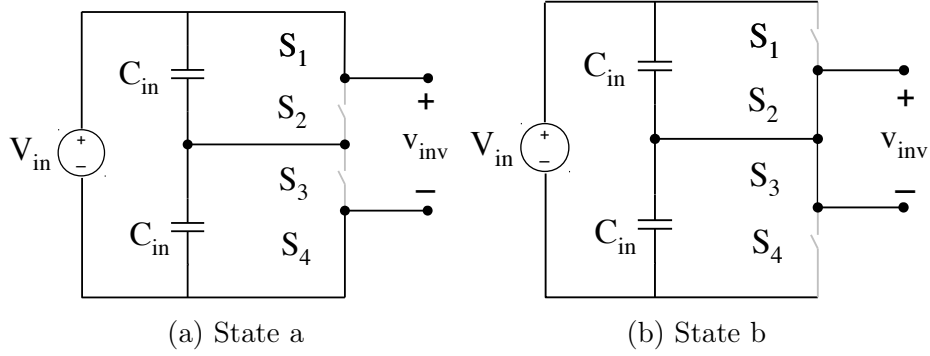


Figure 2-2: Stacked bridge inverter with input voltage V_{in} and output voltage v_{inv} in mode 1.

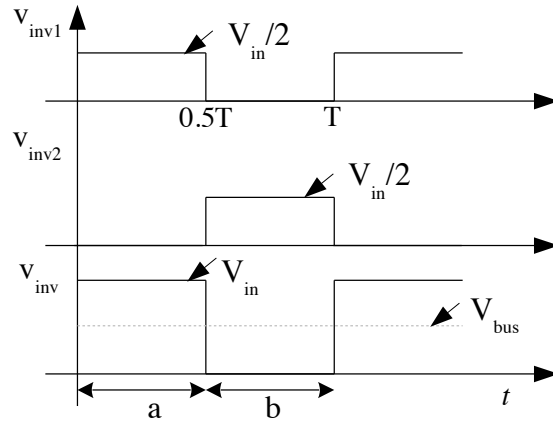


Figure 2-3: Output voltages of the two inverters v_{inv1} and v_{inv2} and the resulting inverter voltage v_{inv} in Mode 1.

In mode 2, there are four switching states in one switching period, as summarized in Table 2.2. The VFX mode results in half the dc-to-ac voltage gain and double the frequency of the output waveform for a single switching cycle, as shown in Fig. 2-5. Thus, for the transformation stage to see the same frequency as in mode 1 (i.e., the same frequency of inverter output v_{inv}), the converter is operated at half the switching frequency of mode 1 (with each switching device operating at half the rate of the output ac waveform).

To create the switching patterns discussed above, and to extend this to other topologies, frequency analysis is useful. Considering Fourier analysis, the square pulse output of inverter 1 (Fig. 2-6) can be expressed as the following Fourier series:

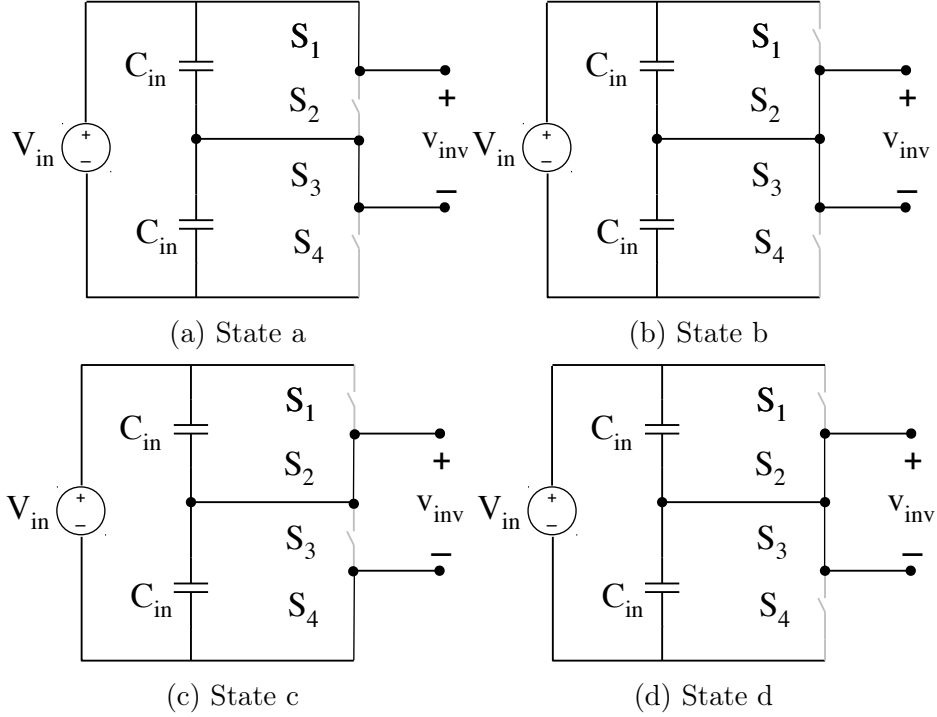


Figure 2-4: Stacked bridge inverter with input voltage V_{in} and output voltage v_{inv} in mode 2.

Table 2.2: Switch states and Output voltage of the inverter in the second harmonic vfx mode (mode 2)

State	On switches	v_{inv}
a	1, 3	$V_{in}/2$
b	2, 3	0
c	2, 4	$V_{in}/2$
d	2, 3	0

$$v_{inv1} = \frac{D_1 V_{in}}{2} + \sum_{n=1}^{\infty} \frac{V_{in}}{\pi n} \sin(n\pi D_1) \cos\left(\frac{2\pi n t}{T}\right). \quad (2.1)$$

Here, V_{in} is the input voltage, T is the switching period and D_1 is the duty ratio of inverter 1. The output of inverter 2 (v_{inv2}) is described by a similar equation but with duty ratio D_2 .

Figure 2-7 shows the amplitude of the fundamental harmonic of this waveform and several harmonic voltages as a function of the selected duty ratio. The amplitude has been normalized to the maximum amplitude ($\frac{2V_{dc}}{\pi}$). By choosing the duty ratio

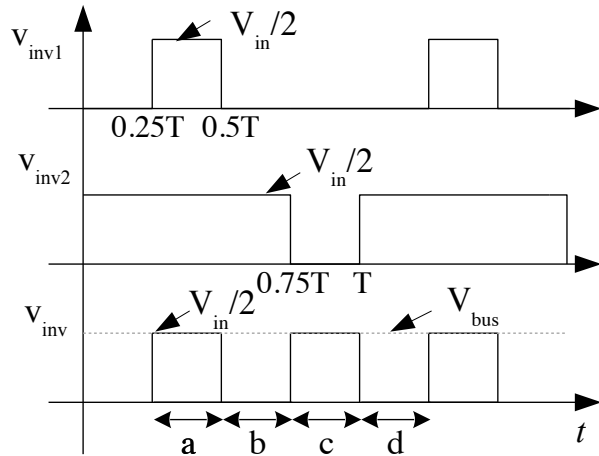


Figure 2-5: Output voltages of the two inverters v_{inv1} and v_{inv2} and the resultant inverter voltage v_{inv} in Mode 2.

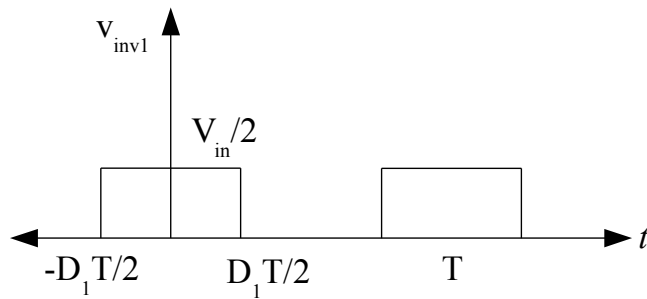


Figure 2-6: Square pulse train output (v_{inv1}) with duty cycle D_1 and time period T .

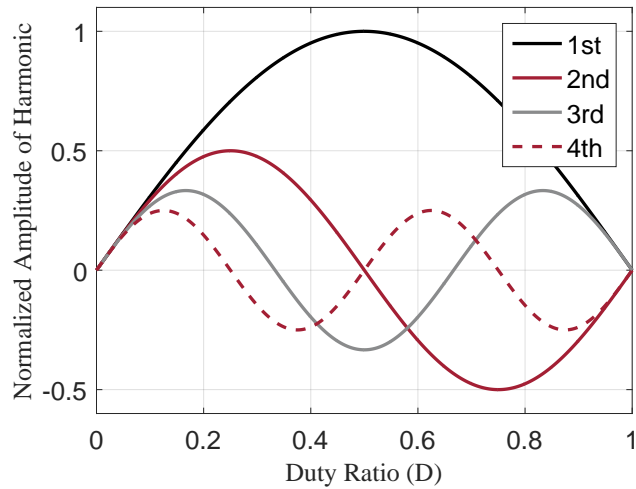


Figure 2-7: Normalized amplitude of the first four harmonics of a rectangular wave with duty ratio D .

of the half bridges correctly, the desired output can be synthesized, while canceling (or reducing) undesired frequencies. In mode 1, the fundamental of the half-bridge inverter waveforms have to be reinforced. Hence, the duty ratios $D_1 = 0.5$ and $D_2 = 0.5$ are chosen. As the output is the difference between the inverter output voltages (v_{inv1} and v_{inv2}), to reinforce these waveforms, the two half bridges have to be switched 180° out of phase, as shown in Fig. 2-3 and expressed in Equation (2.2).

$$v_{inv1} = \frac{V_{in}}{2} + \sum_{n=1}^{\infty} \frac{2V_{in}}{\pi n} \sin(n\pi 0.5) \cos\left(\frac{2\pi n t}{T}\right). \quad (2.2)$$

In mode 2, the second harmonic has to be reinforced, hence, $D_1 = 0.25$ and $D_2 = 0.75$ are chosen, which results in the maximum amplitude of the second harmonic, while canceling out the fundamental component. As the output voltage of the inverter is the difference between the two half bridge inverter voltages (v_{inv1} and v_{inv2}), to reinforce the second harmonic, the fundamentals of the two waveforms are in phase, as seen from Fig. 2-7. In this mode, the fundamental harmonic of the half bridge waveforms is canceled while the second harmonic is reinforced so the output frequency doubles while the output amplitude is halved, as shown in Fig. 2-5 and expressed in Equation (2.3).

$$v_{inv1} = \frac{V_{in}}{4} + \sum_{k=1}^{\infty} \frac{2V_{in}}{\pi k} \sin(k\pi 0.5) \cos\left(\frac{2\pi k t}{T}\right), \quad (2.3)$$

where $k = 2n$. It should be noted that the dc component of the inverter output is different in the two modes, which imposes a rebalancing of blocking capacitor voltages when the operating mode is switched. For the same output frequency, the two inverters switch at half the output frequency. Note that in each case (for the two-mode VFX inverter), the ac output waveform is a square wave. This technique can thus be used in many kinds of ac link topologies, including all kinds of resonant converters and dual-active bridge converters.

2.2 Technique Applied to a Synchronous Rectifier

A rectifier receives an ac current (or voltage) at its input and presents an ac voltage (or current) at its input, which results in dc power being absorbed and delivered to the output as dc voltage and current. The amount of power absorbed depends on the amplitude of the voltage (or current) presented at the input of the rectifier. Hence, the VFX technique can likewise be applied to the rectifier to make the ac voltage at its input be either at the fundamental of the rectifier devices' switching frequency or at a harmonic of the devices' switching frequency in order to convert the ac input power to dc.

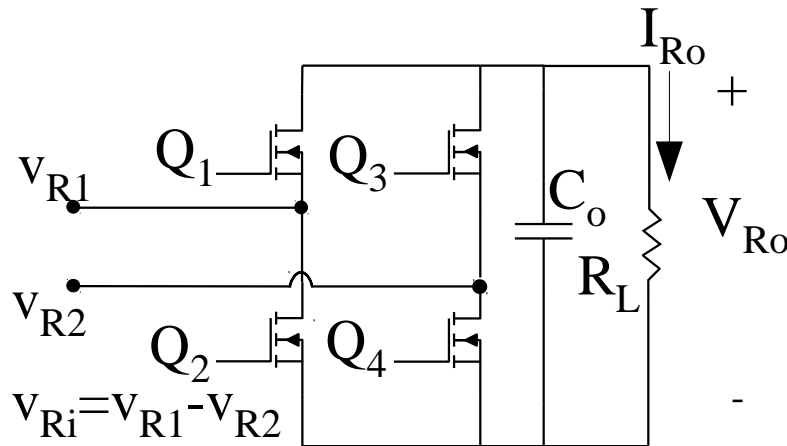


Figure 2-8: Full bridge synchronous rectifier with a resistive output load.

For example, consider a full bridge synchronous rectifier as shown in Fig. 2-8. Similar to the inverter presented in the previous section, we can create two modes of operation by changing the switching pattern of Q_1 , Q_2 , Q_3 and Q_4 , which determines the rectifier input voltage. In mode 1, the input voltage of leg 1 of the rectifier (v_{R1}) is equal to the rectifier output voltage (V_{Ro}) for half the switching cycle (Q_1 and Q_4 switched on), while the input voltage of leg 2 of the rectifier (v_{R2}) is zero. In the

second half of the switching cycle (Q_2 and Q_3 switched on), v_{R2} is equal to V_{Ro} and v_{R1} is zero, as shown in Fig. 9. The resulting voltage at the input of the rectifier v_{Ri} is the difference of the input voltages of the two rectifier legs ($v_{Ri} = v_{R1} - v_{R2}$) and is either $+V_{Ro}$ or $-V_{Ro}$ with 50% duty ratio. The voltage waveform at the input of the rectifier (Fig. 2-9), can be used to determine the ac-to-dc voltage gain of the rectifier in mode 1.

$$M_{R,mode1} = \frac{V_{Ro}}{v_{Ri,pk-pk}} = \frac{V_{Ro}}{2V_{Ro}} = 0.5. \quad (2.4)$$

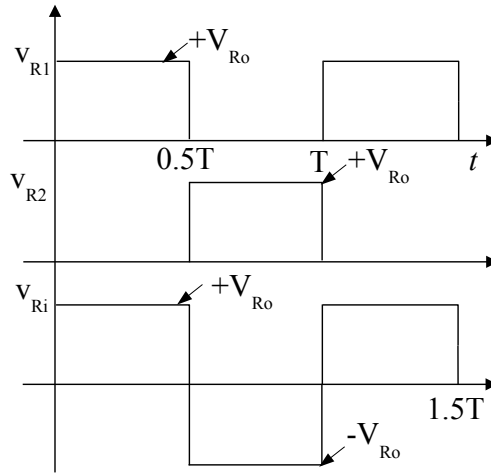


Figure 2-9: Voltage waveforms at the rectifier input during mode 1.

In mode 2, v_{R1} is equal to V_{Ro} for 75% duty cycle and v_{R2} is phase shifted by 90 degrees of the fundamental (a quarter of the period T) and equal to V_{Ro} for 25 % duty cycle. The resulting rectifier input voltage v_{Ri} has twice the frequency at which the rectifier switches operate, and is either V_{Ro} or 0. In order to have the same input (ac) voltage frequency as mode 1, the rectifier switches are switched at half the frequency of mode 1 (with all devices operating at the same frequency). The resulting voltage waveforms are shown in, Fig. 2-10 and as seen from the figure, the ac-to-dc voltage gain of the rectifier doubles in mode 2.

$$M_{R,mode2} = \frac{V_{Ro}}{v_{Ri,pk-pk}} = \frac{V_{Ro}}{V_{Ro}} = 1. \quad (2.5)$$

This gives us a number of design opportunities. For example, one can operate the converter with double the output voltage (if the input voltage remains the same), effectively increasing the output voltage range of the converter.

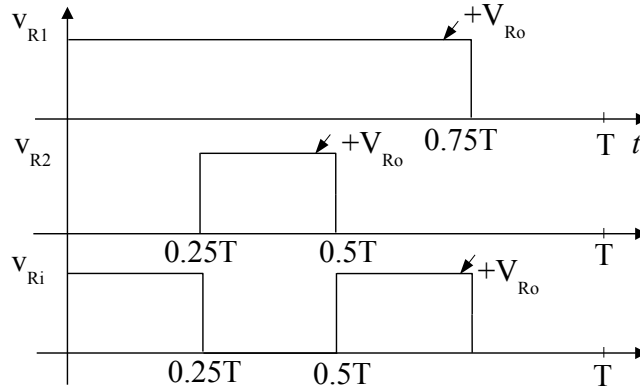


Figure 2-10: Voltage waveforms at the rectifier input during mode 2.

With the rectifier driven by a nearly sinusoidal current waveform (due to a resonant tank in a resonant converter), the amount of power transferred by controlling the phase difference between the current and the input voltage of the rectifier can be controlled. Consider a simplified case where the input voltage and current are in phase, using Fundamental Harmonic Approximation (FHA) the effective input of the rectifier can be represented as an equivalent resistor ($R_{eqv} = k_o R_L$), where R_L is the output load resistor, and k_o is a constant that depends on the ratio between the fundamental harmonic of the voltage and the current.

In mode 1, the fundamental frequency components of the voltage waveform and the current waveform for the rectifier shown in Fig. 2-9 are given by:

$$v_{Ri-ac,mode1} = \frac{4}{\pi} V_{Ro} \sin(\omega t). \quad (2.6)$$

$$i_{Ri-ac,mode1} = \frac{\pi}{2} I_{Ro} \sin(\omega t). \quad (2.7)$$

Where V_{Ro} is the dc rectifier output voltage and I_{Ro} is the dc rectifier output cur-

rent. The ratio of the ac voltage and current, representing the equivalent resistance, is given as:

$$R_{eqv,mode1} = \frac{v_{Ri-ac,mode1}}{i_{Ri-ac,mode1}} = \frac{8}{\pi^2} R_L. \quad (2.8)$$

Where R_L is the dc load resistor at the output of the rectifier, equal to V_{Ro}/I_{Ro} (for continuous steady-state operation). Using the two-mode VFX technique, we alter the rectifier characteristics (while still operating with a "resistive" characteristic) by changing the switching pattern of the switches. The magnitude of the fundamental frequency component of the ac rectifier input voltage V_{Ri-ac} decreases by half:

$$v_{Ri-ac,mode2} = \frac{2}{\pi} V_{Ro} \sin(\omega t). \quad (2.9)$$

For the same output power, I_{Ro} decreases by half, so the input current is given by:

$$i_{Ri-ac,mode2} = \pi I_{Ro} \sin(\omega t). \quad (2.10)$$

Hence, the equivalent resistance is equal to:

$$R_{eqv,mode1} = \frac{2}{\pi^2} R_L. \quad (2.11)$$

The second operating mode in VFX gives us the opportunity to adjust the voltage and current profile of the rectifier (e.g., keeping an equivalent ac input resistance at a different dc output voltage, or changing the effective ac output resistance for a given dc resistive loading on the rectifier).

The two-mode VFX technique presented can be easily extended to higher modes, given an appropriate rectifier structure. It can likewise be applied to many other rectifier topologies, such as stacked rectifiers, voltage-fed rectifiers, current-doubler rectifiers, etc.

Chapter 3

VFX Technique Applied to the Dc-Dc Converter of a Power Supply

The proposed VFX technique is demonstrated in a dc-dc converter stage designed for a universal-input laptop power supply. The ac voltage varies in different countries but the nominal voltage is either 110-120 Vrms at 60Hz, or 220-240 Vrms at 50 Hz. Therefore, 120 Vrms and 240 Vrms have been selected as the nominal upper limits for the two modes of converter operation, corresponding to peak dc voltages of 170 V and 340 V applied to the dc-dc converter. The VFX technique is very useful for this application because there are two distinct peak input voltages separated by a factor of two in amplitude, allowing us to use the VFX technique to rescale them to a common range at the resonant tank.

An LLC converter has been selected for the dc-dc stage [25]. It uses frequency control to regulate the output voltage and has many advantages. The main advantage is that it has the capability to regulate the output voltage over a wide range of input voltage and power with only a small variation in the switching frequency. Also, it achieves zero voltage switching (ZVS) over the entire range of operation, thus reducing the switching losses. Moreover, the leakage and magnetizing inductance of the transformer can be incorporated into the design.

Figure 3-1 shows the schematic of the LLC converter, which has been implemented with a stacked-bridge inverter appropriate for voltage step-down and VFX operation.

As the input voltage is high, stacked half bridges are used, with the resonant capacitor C_r also serving as a blocking capacitor. This reduces the voltage stress of the transistors by half as compared to a non-stacked full bridge or half bridge, which increases the performance with available high-frequency devices. The transformation stage consists of a series inductor (L_r), a capacitor (C_r) and a parallel inductor (L_m). The capacitor not only provides resonant filtering but also provides dc blocking for flux balancing.

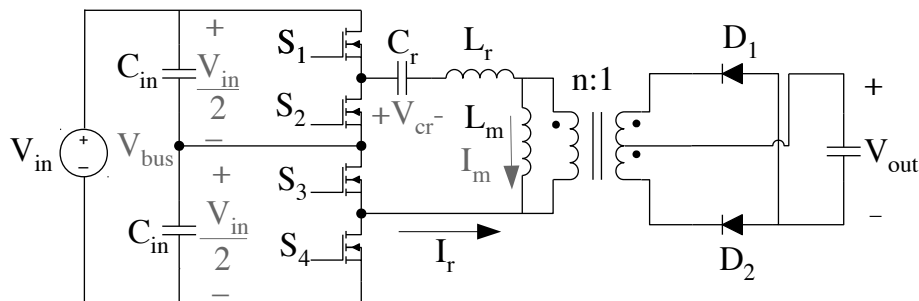


Figure 3-1: Schematic of the LLC converter with a stacked bridge inverter incorporating the VFX technique.

The transformer leakage and magnetizing inductance can be used instead of separate inductors [26]. A center-tapped transformer is used to reduce the number of series diodes in the rectification path. This increases the loss of the transformer and the voltage stress of the diodes. However, this trade-off is still beneficial because of the low output voltage. Synchronous rectification can be used to further reduce losses in the rectification stage [27], [28], [29] but was not used here. The converter is designed using the method outlined in [30], as described in detail below. Fundamental harmonic analysis (FHA) is used to analyze and design the converter. Time-based [31] and approximate methods [32], [33] could be used for a more accurate gain analysis.

The converter is designed for a maximum input voltage of 170 V in the fundamental mode and an output voltage V_{out} of 20 V. To ensure that the power supply (of which the dc/dc converter is the second stage) has a sufficiently high power factor (i.e., greater than 0.95), the minimum input voltage for the dc-dc stage is 85 V. For input voltages above 170 V, the second harmonic VFX mode is used to decrease the voltage that the transformation stage sees by half.

Using FHA, all the voltages and currents are represented by their fundamental components, and the secondary-side variables are reflected to the primary side to obtain the approximated circuit shown in Fig. 3-2.

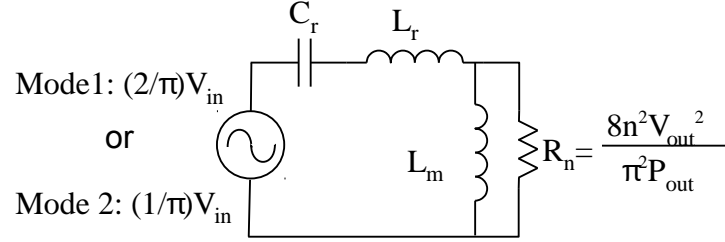


Figure 3-2: Fundamental harmonic model of the LLC converter.

In mode 1, the peak ac output voltage of the inverter is $V_{in}/2$, providing a fundamental ac amplitude of $(2/\pi)V_{in}$. Hence, the transformer turns ratio has been selected as:

$$n = \frac{V_{in-max}}{2V_{out}} = 4.25. \quad (3.1)$$

The recommended range of the ratio of L_m/L_r (referred to as k) is between 3 to 10 [30]. Smaller values of k result in a narrow and steep gain curve but cause a much higher magnetizing current, leading to higher loss. To have a reasonable minimum frequency, magnetizing current and dead time, the value of k is chosen as 7. The value of k can be optimized for a narrower frequency range or a higher efficiency depending on the intended application. The maximum gain (M_{max}) of the resonant network is selected to be higher than 2, i.e, 2.4, to ensure sufficient gain, even with the inaccuracies of using fundamental harmonic analysis.

To ensure ZVS, the input impedance of the resonant network needs to be inductive at the drive frequency. The borderline between the inductive and capacitive region is when the impedance is purely resistive. By equating the imaginary part of input impedance $(x - \frac{1}{x} + \frac{xk}{1+k^2x^2Q^2})$ equal to zero, the value of Q is found. Here, $x = f_{inv}/f_r$, where f_{inv} is the inverter output voltage frequency (which is the switching frequency in mode 1 and half the switching frequency in mode 2) and f_r is the resonant tank

frequency ($f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$).

$$Q = \sqrt{\frac{1}{(1-x^2)k} - \frac{1}{k^2 x^2}}. \quad (3.2)$$

Substituting the value of Q in the expression for gain M leads to the maximum gain (M_{max}).

$$M = \sqrt{\frac{1}{(1 + \frac{1}{k}(1 - \frac{1}{x^2}))^2 + Q^2(x - \frac{1}{x})^2}}, \quad (3.3)$$

$$M_{max} = \frac{x}{\sqrt{x^2(1 + \frac{1}{k}) - \frac{1}{k}}}.$$

The maximum gain leads to the minimum normalized frequency. This value of x_{min} is substituted in the expression of Q to get the maximum Q below which ZVS is maintained.

$$Q_{max} = \frac{1}{k} \sqrt{\frac{1 + k(1 - \frac{1}{M_{max}^2})}{M_{max}^2 - 1}} = 0.1706. \quad (3.4)$$

The values of n , k , R_n and Q_{max} are used to calculate target values of L_r , L_m and C_r :

$$L_r = \frac{Q_{max} R_n}{\omega_r} = 6.36 \mu H,$$

$$L_m = k L_r = 44.5 \mu H, \quad (3.5)$$

$$C_r = \frac{1}{Q_{max} R_n \omega_r} = 15.9 \mu F.$$

The dead-time should be sufficient such that the current in the inductor L_m at the switching instant can discharge the voltage on the MOSFET before it is switched on. By equating the charge required to the current in inductor L_m during the dead time, the deadtime is calculated as $t_d = 8C_{ds} f_r L_m = 62 ns$. Using FHA, the gain curve of the transformation stage is determined, as shown in Fig. 3-3a.

If the converter had been designed without considering the VFX technique as a half bridge implementation, the operating voltage range would have been 85 V to 340 V. This results in the transformer being designed for double the transformer turns ratio, 8.5 rather than 4.25, as calculated from Equation (3.1). Also, the maximum gain (M_{max}) of the transformation stage would have to be doubled, 4 rather than 2, resulting in higher inductor losses. The rest of the components would remain the same. Hence, this would result in an increase in losses.

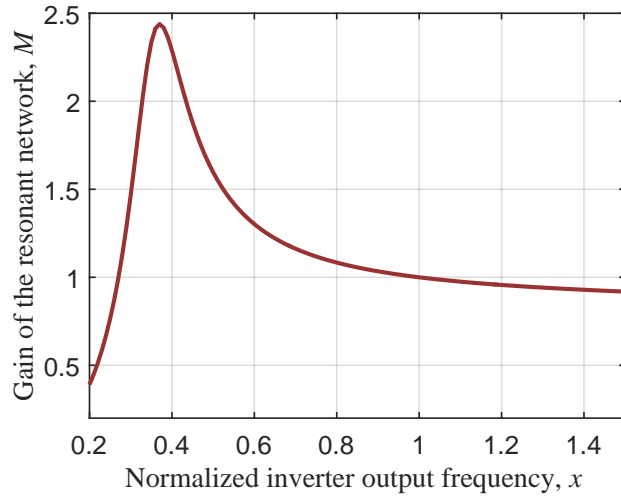
3.1 Experimental Prototype and Results

Using the design values from the previous section, a prototype for the converter was built, as seen in Fig. 3-4. The components used for the experimental prototype are summarized in Table 3.1. Full detailed schematics, along with components used and illustrations of the circuit board layout are provided in Appendix A.

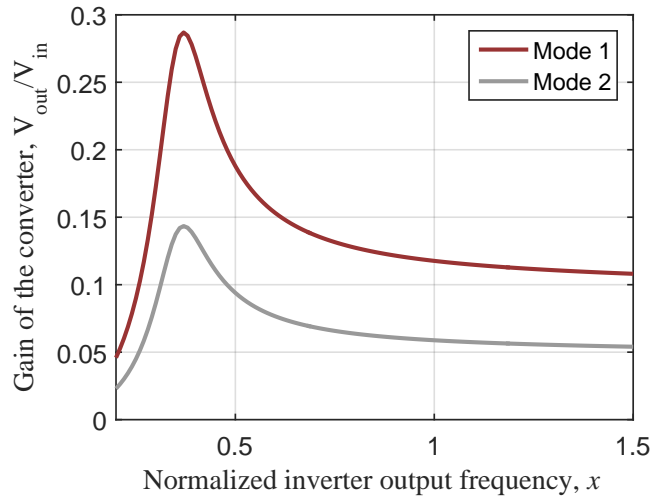
Table 3.1: Components used in the experimental prototype

Components	Type
Controller	150 MHz digital signal controller (TI's TMS320F28335)
Signal Isolators	150 Mbps two channel digital isolator (NVE Corporation's IL711), Qty: 2
Gate Drivers	600-V/4-A High and low side gate driver (IR's IRS21867), Qty: 2
Transistors	200-V/34-A OptiMos power transistor (Infineon's IPD320N20N3), Qty: 4
Capacitors	Cr: 15.99 pF/250 V COG, Cout: 20 μ F/25-V, Cin: 1 μ F/250-V Qty: 2
Inductors	Lr: 3.6 μ H, RM8A100 3F3 core, litz wire (6 turns, 48 AWG, 1000 strands).
Transformer	RM10A160 3F3 core, Primary litz wire (17 turns, 46 AWG, 450 strands). Secondary litz wire (4 turns, 46 AWG, 450 strands).
Diodes	60-V/3-A Schottky diode (NXP's PMEG6030), Qty: 2

The dc-dc converter is a step-down converter operating at the series tank (L_r, C_r) resonant switching frequency (f_r) of 500 kHz. It has an input voltage range of 85 V - 340 V, fixed output voltage of 20 V and a rated output power of 50 W. Table 3.2 summarizes the converter specifications. To control the output power and gain, frequency control is utilized, while the appropriate VFX mode is used based on input voltage being above or below 170 V (in the laptop power supply case, one can either select the mode based on instantaneous voltage, or more effectively based on detection



(a) The gain (M) of the transformation stage using FHA. It has a peak gain at inverter output voltage frequency (f_{inv}) of 0.4 times the resonant tank (L_r and C_r) frequency.

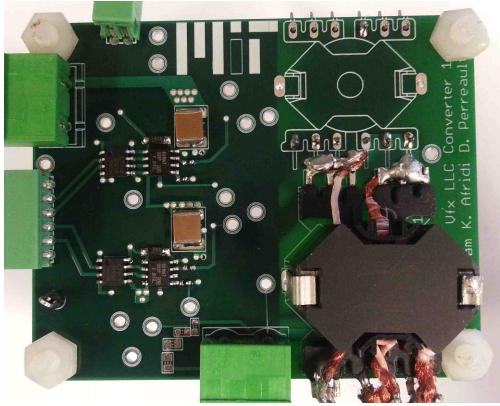


(b) The gain of the converter (V_{out}/V_{in}) using FHA. Mode 1 has twice the voltage gain of Mode 2.

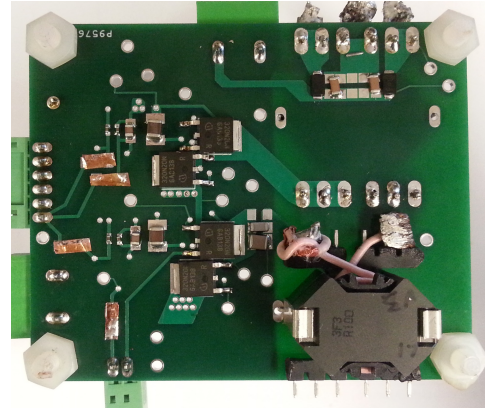
Figure 3-3: Voltage gain of (a) the transformation stage and (b) converter, using FHA.

of the ac line voltage range in use). The transformer was designed to exploit the integrated magnetizing inductance. The leakage inductance was used as part of the resonant inductance. However, this was insufficient and a series inductor was added to provide the required series resonant inductance.

The prototype was tested using a resistive load. The converter operates with ZVS

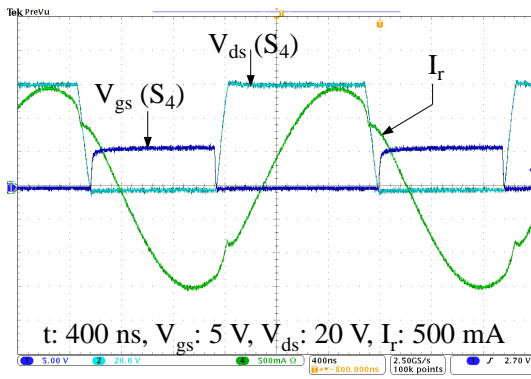


(a) Top side

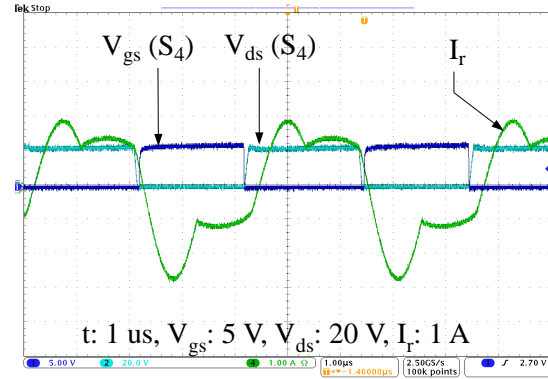


(b) Bottom side

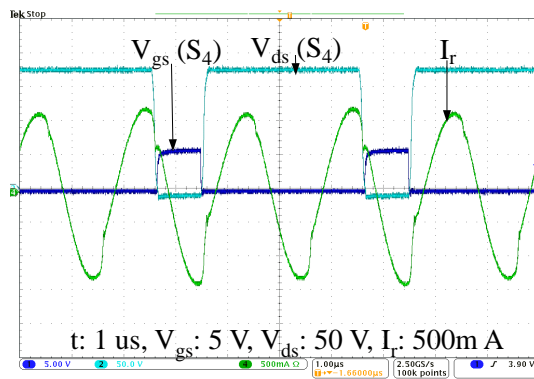
Figure 3-4: Picture of the (a) top side and (b) bottom side of the prototype board.



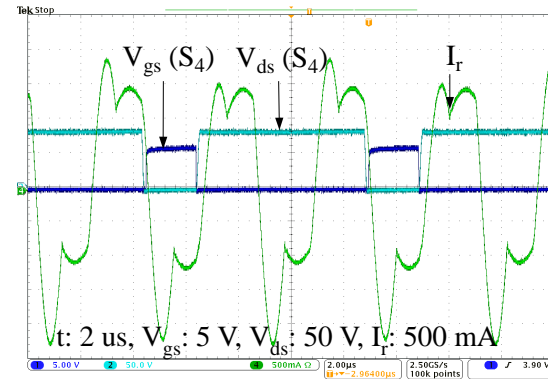
(a) At 340 V in mode 1



(b) At 170 V in mode 1

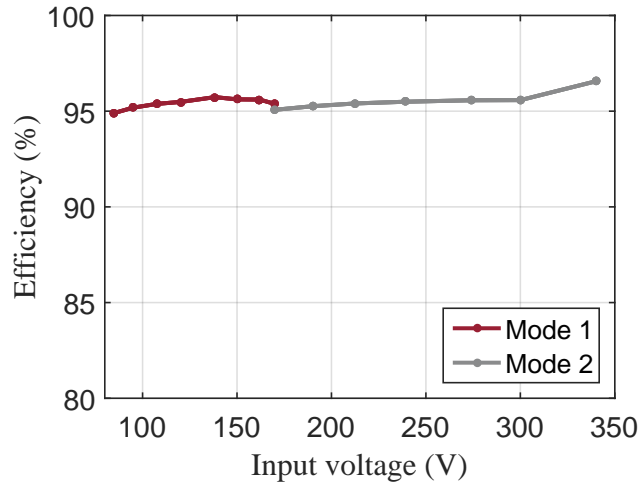


(c) At 340 V in mode 2

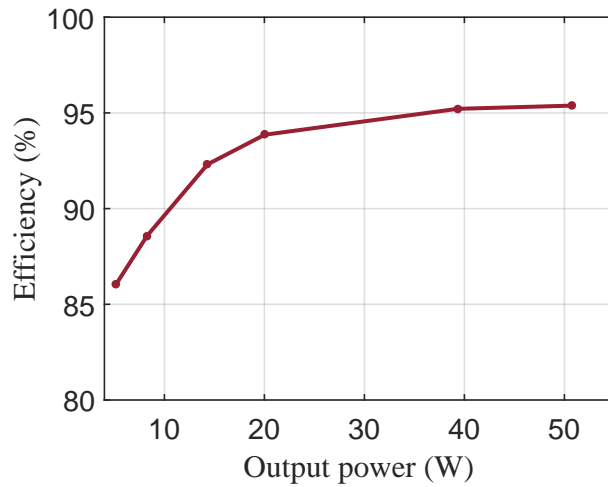


(d) At 170 V in mode 2

Figure 3-5: Current and voltage waveforms of the converter at 50 W when operated in mode 1, fundamental mode, and in mode 2, VFX mode. (1-Blue) Gate voltage of switch S_4 , (2-Turquoise) drain-source voltage of switch S_4 , and (4-Green) current output of lower half-bridge that is flowing into the transformer primary.



(a) Efficiency vs Input voltage



(b) Efficiency vs Output power

Figure 3-6: Efficiency of the converter (a) with variation in input voltage with fixed output voltage and 50 W output power operating in mode 1 and 2, and (b) with variation in output power with 170 V input voltage and fixed output voltage operating in mode 1.

Table 3.2: Prototype converter specifications

Parameter	Value
Input voltage (V_{in})	85-340 V
Output voltage (V_{out})	20 V
Output power (P_{out})	5 W-50 W
Nominal Switching frequency (f_r)	500 kHz

across the entire range of operation. The switching waveforms for input voltages of 170 V and 85 V at 50 W in mode 1 are given in Fig. 3-5 (a) and (b), respectively. It shows the current input to the transformer primary, which is also the output current of the bottom inverter, the gate drive voltage of switch S_4 and the drain-source voltage of switch S_4 . At 170 V (Fig. 3-5 (a)), the current is sinusoidal with a cusp at the switching instants. The converter was operated below resonance, to increase the gain of the transformation stage, as the input voltage decreased. As the converter is operated away from resonance, the current waveform distorts and does not remain sinusoidal. However, the experimental gain is very similar to that calculated by using FHA and ZVS is still maintained.

For input voltages above 170 V, operation is changed to the VFX mode and the waveforms for 170 V and 340 V are given in Fig. 3-5 (c) and (d), respectively. The converter is operated at half the normal-mode switching frequency, which decreases the frequency-dependent switching losses, and ZVS is still maintained, resulting in high efficiency.

The efficiency of the converter was measured across input voltage in both modes and across output power. The measured efficiency of the converter at rated power, as a function of input voltage, is plotted in Fig. 3-6 (a). The converter continues to operate with high efficiency across the two modes, and the converter efficiency varies from 94.9% to 96.6% . The measured efficiency as a function of output power and fixed input voltage of 170 V in fundamental mode varies from 86% to 95.4% and is plotted in Fig. 3-6 (b). The high efficiency over a wide operation range demonstrates the effectiveness of the VFX technique.

3.2 Conclusion

In this chapter, the VFX technique is applied to the inverter of an LLC converter, to demonstrate the effectiveness of this technique for universal input power supplies. This technique increases the input voltage range by a factor of two, and the converter achieves high efficiency over a wide range of operation. The experimental prototype is able to achieve an efficiency of 94.9% to 96.6% across the entire input voltage range at 50 W output power, and 86% to 95.4% across a 10:1 power range with 170 V input voltage. Hence, the VFX technique can be very useful to obtain high efficiency across a wide range of operation.

Chapter 4

A Case for Innovation in Electricity Access

4.1 Understanding Energy Access

Access to affordable energy is crucial for economic and human development. There is no single agreed upon definition of energy access. The International Energy Agency, in the World Energy Outlook, [34] defines modern energy access as: "a household having reliable and affordable access to clean cooking facilities and to a minimum level of electricity consumption which is increasing over time" where the minimum level of electricity is assumed to be 250 kWh per year for a rural household and 500 kWh per year for an urban household. As this definition of energy access is difficult to measure, there is significant variation in the statistics quoted by different sources. Although energy access involves both cooking facilities and electricity, the focus of this thesis will primarily be on electricity access. Here, electricity access is analyzed within the context of off-grid areas in developing countries, and the provision of a basic level of electricity to run the essential electronics of modern day: lights, fans, cell phones and/or other small electronics.

The ideal solution for electricity provision would be to provide consumers with uninterrupted and virtually unlimited access to electricity, as is the norm in developed countries where around the clock electricity is considered a basic necessity. However,

this is not possible in off-grid parts of developing countries due to the high cost of the grid infrastructure needed, and the limited availability of financial resources. Additionally, in off-grid areas, there is not even a demand for such high powered access as there is limited purchasing power to acquire and run high power appliances. Hence, there's a need for metrics to define what electricity means in different contexts.

The World Bank has attempted to measure and classify access to electricity through a multi-tier approach [35]. This approach divides provision of electricity into two 5-tier indices. The first index is based on electricity supply and the second index is based on electricity services. Electricity supply is measured according to the metrics of peak available capacity, duration of usage during daytime, evening supply, affordability, legality and quality. Electricity services can be measured by metrics based on the appliances they can serve; starting simply with basic lighting and cell phone charging usage, and going upwards in power to higher powered appliances. This approach provides a measure of energy access by weighted index, of electricity supply and services, for a certain area, and quantifies quality of service provided by different solutions, allowing comparison between different areas.

Technology developed in this thesis is easily expandable to the highest levels of service (tier 5 as per World Bank's multi-tier approach), which does not lock off-grid areas in low energy lifestyles, and provides an opportunity for off-grid areas to expand energy access with increasing demand in the long run.

4.2 Different Approaches for Electricity Access

The preferred choice for electrification infrastructure of almost all governments is grid-based electrification. This top-down centralized approach is favored because it is a well-tested and an age-old method of electrification. Also, if done right, it can provide reliable electricity and does not hamper its citizens from increasing their energy consumption and setting up economic activities with increased electricity consumption. However, grid extension might not always be the most economical solution. Transmission and distribution can be costly to set up and maintain, especially given

low electricity demand in remote areas [20]. Additionally, grid electricity is generally unreliable in developing countries. The governments of these countries do not have the financial resources to provide reliable electricity to grid connected areas or to increase generation to cope with increasing demand, let alone to provide electricity to off-grid areas. International Energy Agency estimates [21] that it will cost around \$48 billion to provide universal energy access, and the gap between expected cost and available public funding is around \$34 billion dollars, requiring involvement of the private sector to reduce the gap.

The private sector has employed different bottom-up decentralized approaches, such as the use of individual systems (for example, solar home systems and diesel generators) and microgrids. Individual systems have seen rapid growth in the recent past due to the ease of deployment [21]. However, they are expensive and require complex financing solutions. Also it is difficult to extend their capacity beyond what they have been originally designed for i.e. usually lighting and cellphone charging only. On the other hand, microgrids can provide lower cost electricity as they aggregate generation and load, thus decreasing the cost per watt [22]. However, development of centralized microgrids (with all generation and storage co-located) has its own challenges. Centralized microgrids require a high upfront capital investment to set up, leading to expensive and complex financing. Also, they traditionally require rigorous planning and participation from a large percentage of the community to be financially feasible [36].

While there is a pressing need to provide electrification to off-grid areas, the current technologies have not been able to scale to serve the vast majority of off-grid populations. The first step in the energy access ladder has been to move from kerosene or candles to solar lamps. The deployment of solar lamps has grown significantly in recent years due to their low cost, however, they only provide light (and sometimes cell phone charging) rather than a source of electricity [37]. The next step is the provision of electricity for basic appliances. However, the end goal should be provision of electricity with high availability, affordability, adequacy, convenience and reliability. Technological innovation with strong business fundamentals will allow this to happen.

The modular microgrids enabled by PMUs developed in this thesis are a step towards attaining this goal.

4.3 Providing Affordable Electricity

The cost of providing electricity, and the willingness of users to pay varies considerably across off-grid areas [38], [37]. Hence, there cannot be one solution which is ideal for all. However, modular and expandable systems can help in pairing electricity supply with consumer demand and purchasing power.

4.3.1 Drivers of cost of electricity

There are three major costs drivers of off-grid electrification systems: planning and financing, hardware components, and installation and operation. Each of these is discussed in detail in the following subsections.

Planning and financing

Before the system is installed, time and resources are spent in selecting the community, designing the system and acquiring financing for the system. This can be a substantial cost but varies immensely across Energy Service Providers and geographic regions.

Hardware components

The design of the system determines the components used. The power sources and storage, distribution, electronics and appliances determine the cost of the components. The power sources and storage, and distribution dominate these costs [36]; each of these is described in detail in the following two subsections.

Power Sources and Storage: In any power system, the choice of the type of power generation technology is key in determining cost. The cost of electricity from different types of generation varies in different areas and depends on the cost of the technology, resource availability and the national policy and regulations of that region. For example, some countries have lower solar irradiance, so the cost of solar

power (\$/W) is higher compared to areas which have higher irradiance. Also, in some countries, government subsidies make kerosene and diesel much cheaper than other sources of generation. In the power sector, a diversified generation mix is preferred as it results in the most economical and reliable systems [39]. However, in smaller systems, the diversity of generation may be limited, which might lead to dependence on energy storage for reliability. Using efficient electronics, efficient appliances and demand management, the capacity of sources and storage required can be decreased.

Renewable energy, especially solar power, is one of the most common means of generating electricity in off-grid areas [22]. As the cost of solar panels, batteries and power electronics has been rapidly decreasing over time, solar powered microgrids have seen significant growth. Solar power can be easily set up for small-scale usage, compared to other renewable energy alternatives, and continues to be the main generation source for off-grid electrification.

Distribution Wiring: The distribution voltage, distance and power delivered determine the distribution wiring costs. Higher voltage, lower power and short distances lead to lower conductor material cost. However, if the distribution voltage is increased substantially, the insulation costs and protection equipment costs increase drastically, so voltage needs to be kept low. Power delivered is determined by the demand, and might not be easily reduced. Distance, by contrast, is an effective means of controlling cost, as it can be substantially reduced by having distributed generation close to consumption. Distribution costs can thus most effectively be reduced by locating power sources close to consumption units.

Installation and operation

Depending on the size of the microgrid being installed, the installation time and costs can vary drastically. Small microgrids with fewer components are simpler and cheaper to install, while larger setups are costlier and more complex, requiring more expertise as components from various vendors need to be connected together.

Microgrid operators are responsible for general maintenance of the generation and distribution assets. In addition to providing maintenance, microgrid operators selling

electricity as a service periodically collect payments from their customers. Most microgrid operators rely on door to door cash collections, which are extremely costly [37]. However, some microgrid operators (especially in Africa) have adopted the use of mobile payments for collections, which is significantly cheaper than cash collections, leading to scalability of microgrids.

4.3.2 Ability to pay

The high cost of using alternatives to electricity enhances the economics of solar power. Considering only lighting, the current household spending, using kerosene, candles and other fuel sources is comparable, and in most cases higher than the amount that would be spent on off-grid solar lighting [38]. For basic appliances, such as lights, fans and cell phones, solar power is affordable even for low-income households if the systems are designed efficiently.

The ability to pay for electricity varies in different countries. This mostly depends on what consumers are currently paying for alternatives (such as kerosene). Also, within a community, the purchasing power of the members can vary significantly. Hence, technology development needs to take into account the electricity demands of various consumer segments. The technology developed in this thesis provides low cost electricity to reach the poorest members of the community, as well as higher priced electricity to customers that require more reliability.

4.4 Impact of Electricity Access

The following subsections describe the social, economic and environmental impact of providing electricity access through renewable energy.

4.4.1 Social and economic impact

There is a considerable amount of literature available that shows how provision of electricity improves the standard of living of those living in off-grid areas. For exam-

ple, a World bank study looks at the economic benefits of providing services, such as electric lighting and television, with the provision of electricity [38]. The study shows that replacing kerosene lamps with electric lighting is not only cheaper, as it costs less for the same amount of Lumens, but there are also measurable health benefits. Kerosene lamps cause air pollution by emitting small particles which do not disperse in the air. The respiratory sicknesses caused by these particles result in a loss of 3 adult working days a year, and an increased infant mortality rate. The health benefits of using electric lighting versus kerosene have been quantified at \$2.5 per household per year. Also, this study shows a correlation between electricity access and better rates of higher educational attainment, home business revenues, and health awareness from watching television.

Another study, conducted on more than 10,000 low-income households in India, [40] shows that non agricultural incomes of rural households increased by about 28.6 percent over 11 years due to good quality electricity. However, the increase was only 9 percent for households with unreliable electricity. This shows the importance of reliability, even in the context of the developing world. The provision of reliable electricity to the low-income segment improves livelihood, education and health opportunities through lighting, labor saving devices and access to information through electronic communication devices [41].

In addition to providing economic and social benefits to household consumers in off-grid areas, reliable electricity can also create opportunities for sustainable economic development through productive use of electricity for income generation. For example, with the use of refrigerators and freezers, retailers in off-grid areas can prolong shelf life of perishable goods, leading to higher profits [42]. The productive use of electricity will in turn lead to higher demand and ability to pay, allowing electricity providers to attain higher financial returns, resulting in scaling up of new energy access deployments. Hence, one of the major features of the technology developed in this thesis is to provide owners of solar home systems or solar pumps with a supplementary source of income by selling electricity generated, in excess of their productive use, to the microgrid.

4.4.2 Environmental impact

More than 1.2 billion people do not have access to electricity globally. Under the "business as usual" scenario, if they are connected to the traditional grid infrastructure, and use mainly fossil fuels to provide electricity, it will result in unsustainable CO_2 emissions. Hence, while building new power systems, there is a need to be more environmentally conscious and to not make the mistakes made in the past, which promoted high carbon emitting technologies.

The environmental impact of providing renewable energy to off-grid areas can be huge. The scale is evident from the fact that, as per conservative estimates, only replacing kerosene used for lighting with clean energy would lead to a CO_2 emissions reduction of 5 Gigatons over 20 years [43].

Chapter 5

Ad Hoc Microgrids for Off-grid Electrification

5.1 Definition

An ad hoc microgrid is formed by the arbitrary interconnection of power management nodes - a node consists of a power source or load, interfaced via power electronics. These nodes can be deployed with limited infrastructure pre-planning and operate autonomously with distributed control, as shown in Fig. 5-1.

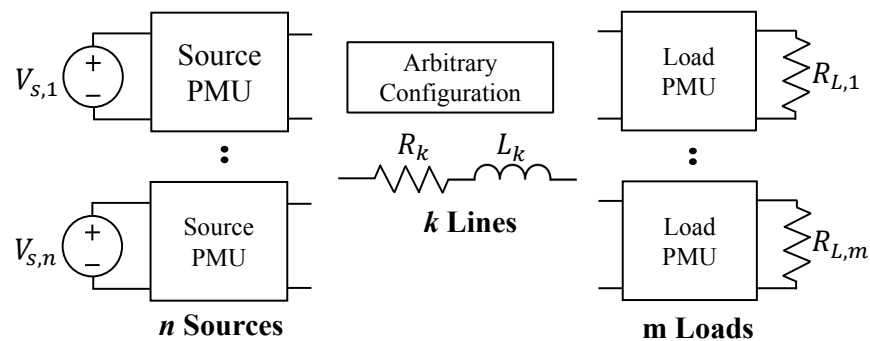


Figure 5-1: Arbitrary interconnection of Power Management Units (PMUs) forming an adhoc microgrid.

5.2 Type of Distribution

The debate about whether to have a dc or ac grid began more than a century ago. This is usually referred to as the “war of the electric currents” [44]. At that time, it was found that an ac grid was a more feasible option, mainly because it was difficult to step up and down dc voltages and thus dc had more loss over large distances owing to the need to distribute electricity at the final (relatively low) utilization voltage. However, after the development of power semiconductor devices and the advancement in power electronics, this question has to be reevaluated, especially for off-grid microgrids [45]. In developed countries, changing to dc is not considered feasible owing to the vast and costly ac power grid infrastructure already established. However, dc distribution inside buildings is being proposed as it can result in cost reduction [9]. For the developing world, grid infrastructure is not present in many places, so introducing a dc microgrid can be a more feasible option.

The three main considerations in choosing dc or ac microgrids are:

1. Type of power generation
2. Type of loads available
3. Size of the grid

For the application considered in this thesis, safety and stability are also major concerns as the ad-hoc microgrid proposed has to be easily configurable and safe for untrained users to install and interact with, while keeping costs low.

5.2.1 Type of power generation

Conversion losses depend on the type of interface; an ac generating source interfaced with dc distribution results in greater loss as compared to a dc to dc interface [46]. In this network, PV panels, which are low-voltage dc sources, are being considered as the power generating source. The power generated by the PV panels needs to be stored in batteries, which are also low voltage dc, and are connected to the network via power electronics. Hence, it is more efficient to interface these dc sources with a

Low Voltage Direct Current (LVDC) grid.

5.2.2 Types of loads available

Most loads, especially those used in off-grid areas, such as LED lights and cellphones, are dc and will have less conversion loss if they are powered from a dc grid [23], [47]. Also, most loads (e.g., televisions) that appear to be ac are inherently dc but are commonly available as ac (with ac to dc conversion) because of the existing ac grid infrastructure. Hence, it is much easier to find ac appliances in the market rather than dc. However, as the dc off-grid electrification market matures, the cost and availability of dc appliances is predicted to improve [48].

5.2.3 Size of the grid

The size (geographical span and power transferred) of the grid determines its distribution losses. In the proposed system, a distributed network is created where the power source is in close proximity of the consuming units, as the power management units are usually placed in neighbouring houses. A study of 71 villages (10,000 households) in the Indian state of Bihar, conducted by Varshney et al.[49], found that the average distance from each house to its next five closest neighbors is 19.26 m, with a standard deviation of 4.76 m. With these small distances and the low power (around 25 W per household) being distributed, LVDC can achieve acceptable efficiencies.

5.2.4 Safety

To transfer electricity over large distances, high voltage is preferred as it reduces the line losses or decreases the cost of the wiring. However, high voltage distribution can be unsafe, especially in a system which is set up and maintained by un-trained users.

There are many potential safety hazards when dealing with electricity, and some are even fatal. One of the main causes of death by electric shock is ventricular fibrillation, when the heart ceases to pump blood, causing a cardiac arrest. Other effects such as muscular contractions, burns and injuries from falling also occur but

ventricular fibrillation has the highest mortality rate and will be considered in this discussion.

The severity of the electric shock depends on the magnitude, duration and frequency of the current. The magnitude of the current is determined by the voltage applied and the impedance of the human body. The impedance varies depending on the person's weight, and external conditions. Impedance is lowest for saltwater-wet conditions, i.e. the condition one might have when the person is sweaty. To determine currents for safe operation, Dalziel theory [50], Koepkens theory [51] and IEC standards are commonly used. As the IEC standards are the most conservative among these, they were considered in this discussion. According to the IEC 60479 standard [52], electric current above 120 mA is highly likely to cause ventricular fibrillation. Considering the dc impedance of the human body (940Ω) from Table 3 of IEC60479, voltages below 100 V will not cause ventricular fibrillation. As the impedance of the human body may vary, the more conservative IEC61201 standard [53] was considered. According to Fig. 6 of this standard, 70 V (dc) is the minimum threshold for ventricular fibrillation in saltwater-wet conditions. Hence, voltages which are commonly used for ac appliances, e.g., approximately 120 V_{rms} (220 V_{rms} in South Asia), are not touch safe. The duration of the contact is important because there are parts of the heart cycle (recovery from excitation-T) during which the ventricles are most vulnerable to cardiac arrest, hence, if the current flows for a very short period of time, the probability of cardiac arrest decreases [52]. Moreover, ac current is more dangerous than dc current because it causes more frequent and severe muscular contractions. From [53], 50 V and below is considered to be a safe range of operation.

If ac voltage is considered, users will not be able to safely interact with the network, and extra safety measure will be needed (such as taller distribution poles, carefully insulated connectors, etc.), which increases the cost of the system. Also, LVDC is preferred as HVDC is not touch safe and requires additional safety measures, such as protection devices for basic and fault protection, which increases the cost and complexity of the system [54].

5.2.5 Stability

A dc distribution system offers greater ease of achieving stability as compared to ac distribution [45]. Stability is a major concern in microgrids, where each load is a significant portion of the total power of the system. An ac system requires the use of voltage and frequency control for stable operation. This is regulated with active and reactive power control. On the other hand, in dc systems the control is simpler as only the voltage needs to be regulated. As the proposed microgrid is not pre-planned, an ac system will be challenging to set up and control.

5.2.6 DC distribution chosen

Many of the loads of interest in in off-grid areas are low-voltage dc, available energy sources (solar) are inherently low-voltage dc, and dc energy storage is a necessary component, making low-voltage dc a better choice for these microgrids. Also, for this application, safety and stability are major concerns because the ad-hoc microgrid proposed has to be low cost, easily configurable and safe for untrained people to interact with. Hence, a dc microgrid is a more viable option.

5.3 Overview of the Micorgrid

Power Management Units (PMUs) are needed to form an ad hoc microgrid. The source PMU provides the power conversion necessary to interface power sources (such as PV panels, batteries etc) with the network, controls power from multiple power sources, and decides which loads are to be served. The load PMU provides the power conversion necessary to power different loads (such as fans, cell phones etc) and performs demand management based on the decisions made by the source PMUs. Fig. 5-2 shows this ad hoc microgrid in a residential setting.

The microgrid has the following features:

- PV panels are used for power generation, and lead acid or Lithium Iron Phosphate batteries are used for storage. These are external to the PMUs. Other

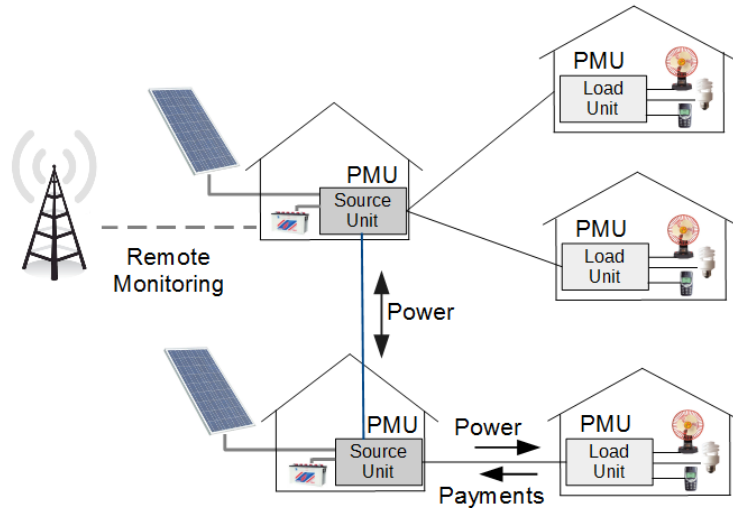


Figure 5-2: The Power Management Units (PMUs) can connect power generating sources and loads to form an ad hoc microgrid. A residential microgrid is depicted.

generating sources could also be utilized with the appropriate power conversion interface.

- Two types of PMUs, as shown in Fig. 5-2, are present: a source unit and a load unit. The source PMU takes power from the solar panels and/or the network, and charges a battery. It also takes power from the battery to supply to the network, while maintaining distribution voltage. The load PMU powers the electric devices and appliances. For demand management, the load PMU has the capability to vary the power supplied, or to switch the power on or off.
- The distribution of electricity is at a low voltage and is done by low-cost wires strung between PMUs.
- The power transferred between units is measured, and this measurement is used to remunerate the power generator and bill the power consumer.
- Information is transferred between units for scheduling and control of the system.
- A scheduling and dispatch algorithm running on the source PMU(s) ensures

reliable power for the consumers, as per their demand, even with limited resources.

- Multiple source and load PMUs can be connected to form an ad hoc micro-grid. This connection can be arbitrary to form any network configuration. This enables non-experts to set up microgrids.

The complete system with a source unit and multiple load units is shown in Fig.5-3. Each unit consists of power conversion, control and communication modules.

A source unit's power conversion modules comprise of a charge controller to charge the battery from the solar panel and a source converter to step-up the battery voltage to the network voltage and to control the power output of each each source. The control module computes and provides scheduling, dispatch and pricing information. The communication module comprises of GSM communication for remote monitoring and for payment transactions, and RS485 communication for local communication.

The load unit's power conversion module comprises of a load converter, which provides power conversion for different types of loads. The communication module consists of only local communication (RS485), and a sub-control unit which makes decisions (such as controlling current or shedding loads) based on signals from the source PMU.

5.4 Ensuring Arbitrary Interconnection

The source and load converters can be connected in arbitrary configurations. Each unit must be designed in such a way that the network formed by arbitrary interconnection is stable. The load converters in this system have tightly-regulated output voltages. While providing constant power, they thus have a negative incremental input impedance, because in order to deliver constant power to their output, they must draw constant power at their input. Hence, as their input voltage increases, their input current decreases, and vice versa. This negative incremental resistance has a well-documented destabilizing effect on power networks [55].

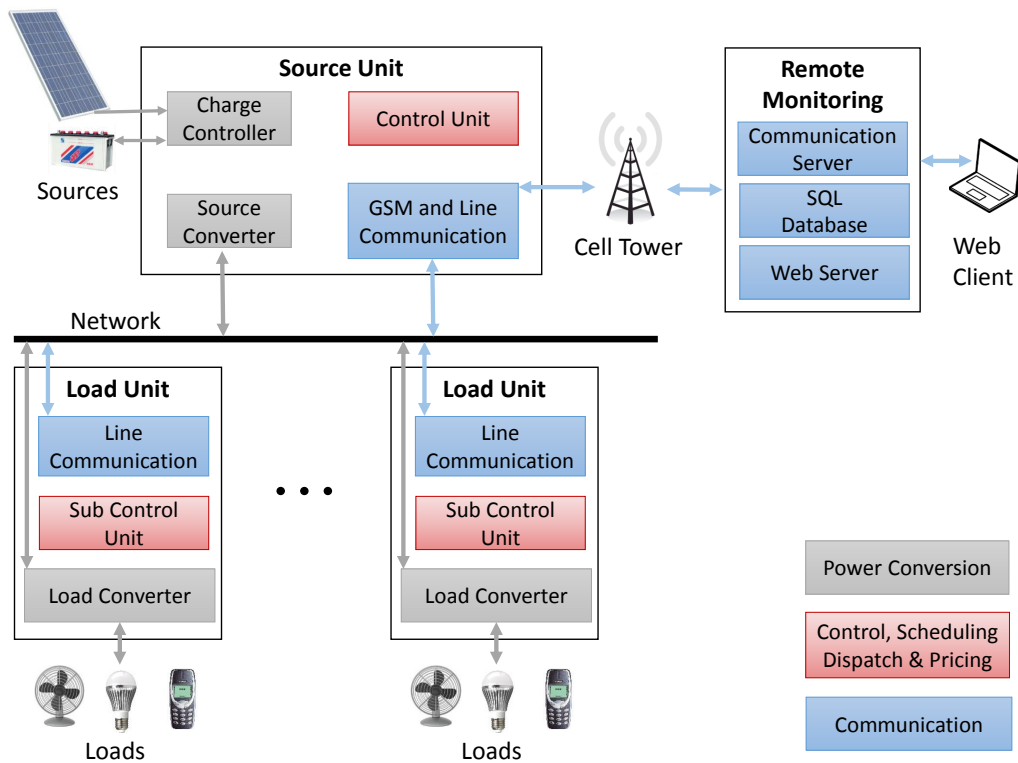


Figure 5-3: Detailed overview of the microgrid with connected PMUs. Each PMU comprises of power conversion, control and communication modules.

In order to ensure stability in dc microgrids, many different methods are utilized [56]. The two main methods are: addition of passive components and modifying the controller to have passivity based control. The former is chosen, because (as will be shown in Chapter 8) by simply adding sufficient input capacitance any converter (off-the-shelf) can be used in the micogrid. Whereas, changing the control of a converter, by modifying its code, might not be possible in many cases. For stability, a certain amount of capacitance must be present at the input of the converter [57]; this is discussed in detail in Chapter 8 and given by Equation (5.1).

$$C_k > \frac{p_k \tau_{\max}}{v_{\min}^2}, \quad (5.1)$$

where C_k is the input capacitance of the k th converter, p_k is the output power, τ_{\max} is the maximum time constant of the lines used (L_{\max}/R_{\min} , note that τ doesn't change with an increase in length of a particular wire as both L and R scale proportionally), and v_{\min} is the minimum voltage on the network. A capacitance is usually already present at the input of the converter to bypass the input of the converter (to minimize the voltage ripple seen by the converter) and for EMI filtering. For stability, this capacitance needs to be larger than C_k found previously.

5.5 Control of Distributed Power Sources

When multiple sources are connected without coordinated control in a microgrid, the steady-state fraction of total power, each source supplies, is fixed and is determined by the line resistances and the voltage difference of each supply. To allow each source unit to set (and update) its portion of total supplied power (“dynamic load sharing”), while simultaneously regulating the microgrid voltage, a two-level controller is proposed. Similar to conventional hierarchical control [58], the primary control consists of a “virtual” (droop) resistor (r_d) and secondary control consists of an offset voltage δ , as shown in Fig. 5-4. However, unlike the conventional method, the droop resistance is only used for limiting circulating current and achieving acceptable voltage regulation in the transient, and not to achieve current-sharing in steady-state.

Also, the secondary control is not only used for voltage restoration (similar to the conventional method), but also for accurate power sharing.

Primary control

In considering the use of droop control for dynamic load sharing, the individual source converters are modelled as Thevenin equivalents having a Thevenin voltage equal to reference voltage (u) for the converter, and a Thevenin resistance (the "droop" resistance, r_d) that is implemented by controlling the source unit to reduce output voltage (v_k for k th converter) below this reference voltage, as more current is drawn from it. This is shown in Fig. 5-4 and given in Equation (5.2). The droop resistance is a control parameter internal to the power converter, and hence, *does not* dissipate power. In the proposed method, the droop resistance is used to limit circulating current and to achieve acceptable voltage regulation in the transient, and hence, the droop resistance (unlike the conventional method) does not need to be much larger than the line resistance and is the same for all sources.

$$v_k = u - i_k r_k, \quad (5.2)$$

where v_k is the output voltage, r_d is the droop resistance and i_k is the output current of k th source.

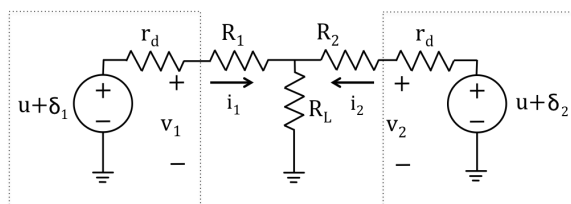


Figure 5-4: Two sources with output voltages v_1 and v_2 connected to a load R_L with resistive lines R_1 and R_2 .

Secondary control

In the secondary control, an offset voltage δ is added to mitigate the network voltage deviation caused by droop control and to control the power sharing ratio. The integral

controller used is given in Equation (5.3):

$$\begin{aligned}
 \dot{\delta}_k &= k_{i,v}e_v + k_{i,p}e_{p,k}, \\
 e_v &= u - \bar{v}, \\
 e_{p,k} &= \lambda_k\bar{p} - \bar{\lambda}p_k.
 \end{aligned}
 \tag{5.3}$$

Where e_v is the voltage error defined as the deviation of the average voltage of all the sources (\bar{v}) from the desired nominal voltage (u). λ_k is used to specify a desired fraction of total power that each source supplies. $e_{p,k}$ is the error of the power of each source, compared to the desired value.

This proposed two-level control not only allows accurate power sharing, but also maintains the voltage within limits. Further details are provided in Chapter 8.

5.6 Design Methodology

The source PMU can take multiple inputs (such as PV panels and network connection) and is able to charge/discharge a battery. The load PMU takes power from the network and has multiple outputs for different loads, as shown in Fig. 5-5.

The energy access space is a cost constrained environment, so cost is a major consideration in design. The cost of the PMU, as well as that of the overall system needs to be kept low. For this, the number of voltage conversion steps that require added power conversion stages, as well as the energy storage requirements of the passives needs to be decreased. Efficiency is also a major concern as loss translates directly to increased system cost (principally through increases in required sizing of batteries and solar panels); this is consistent with other applications as well [59].

5.6.1 Power rating

The power rating of the source PMU is set at 250W, to leverage benefits of economies of scale. All major solar manufacturers (e.g., Yingli, Suntech, Trina Solar and Sungen) produce solar panels with a minimum power rating of 250 W. Some manufacturers

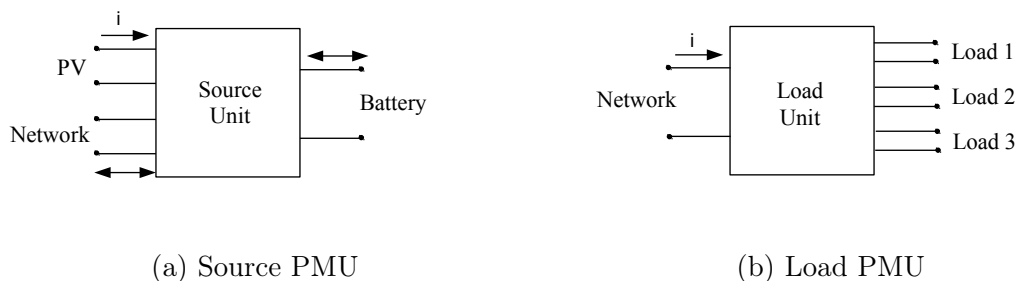


Figure 5-5: PMUs to interface sources and loads to the grid network.

have smaller-sized solar panels for off-grid areas but their cost per watt is significantly higher [36] compared to larger-sized panels. At present, in off-grid areas, smaller-sized solar panels of around 40 W are being deployed for solar home systems, which are much more expensive per watt. Thus, aggregating loads to provide power from larger solar panels will allow microgrids to attain cost savings due to economies of scale.

Considering the basic loads used by households in off-grid areas, the power rating of the load PMU is set at 25 W. For a single home, the most common basic loads that need to be powered are lights (5 W, two LED lights at 2.5 W each), a cell phone (2.5 W) and a fan (15 W). Televisions (e.g.15" Phocos, 18 W) or small refrigerators (e.g., Chotukool, 62 W) are possible loads but are not affordable for most people living in off-grid areas due to low and oftentimes unstable incomes. Also, these devices require higher power, which will increase operating costs of the entire system. These higher-rated loads can be powered by PMUs with a higher power rating, which can be obtained at an additional cost by users with higher ability to pay. However, a 25 W power rating is sufficient for most basic loads in off-grid areas.

5.6.2 Voltages of operation

The battery and distribution voltages need to be determined, as they will affect the power converter and distribution design.

For safety reasons, the distribution voltage needs to be below 50 V [53]. In the ad-hoc microgrid, the two voltage levels considered for distribution are 24 V and 48 V. These voltages are commonly used by the automotive/trucking (24 V), and

Table 5.1: Common Loads

Appliances	Approx. Power Rating (W)
Basic Loads	
Lights	5
Cell Phone	2.5
Fan	15
Additional Loads	
Television (15")	18
Refridgerator (Chotukool)	62

telecom (48 V) industries. The electronic components used by these industries are low cost and easily available. Hence, relying on these electronic components makes it easier to build low cost PMUs. While operating at 48 V lowers the distribution losses, it increases the cost of the load converters, which has 12 V and 5 V outputs, due to higher power conversion cost. The higher conversion cost for 48 V distribution mainly arises from the higher device stresses and passive costs owing to the higher conversion ratio (and especially due to the cost of magnetics) [60]. The consumer module is the most price sensitive element in the whole network (low-cost consumer modules are needed to drive adoption; generation and distribution costs are more readily absorbed by the electricity supplier). Also, 24 V is much safer than 48 V [61], and is being promoted as an indoor dc distribution standard by the EMerge Alliance [62]. In this thesis, 24 V will be used for distribution, as this voltage is reasonable for the power levels and distribution distances considered in this application (see Fig. 5-6), and safer for the prototype stage. However, the designs presented can be easily extended to 48 V, which may be preferred for future deployments, especially in areas with lower population density and higher power requirements.

To lower cost of the source unit, a battery voltage of 24 V would be preferred because typical solar panel voltages vary from 25 V to 40 V and the network voltage has been chosen as 24 V. The lead-acid batteries being considered are nominally 12 V; and putting two of these in series results in a battery voltage of 24 V. Also, the cost of batteries (\$/Ah) decreases very sharply up to 33 Ah and then it flattens out [36]. Hence, the cost of having two 90 Ah batteries will be almost the same as having

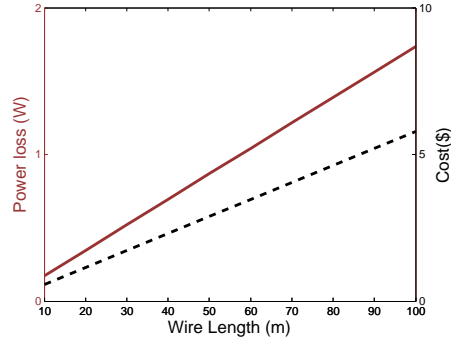


Figure 5-6: Power loss in distribution and wire cost with 25 W transferred at 24 V with 14 AWG wire costing \$0.0578 per meter.

a single 180 Ah battery. However, to increase adoption of the system, compatibility with existing Solar Home Systems (SHS) is needed. Currently, most SHSs in off-grid areas have 12 V batteries, hence, a 12 V battery voltage is considered for storage in this system.

An additional feature of high-voltage dc or ac distribution could be added when power is being transferred over large distances (requiring an additional power management unit to interface with this transmission voltage). However, this requires better protection, insulation and taller electricity poles; this could be explored further in future applications.

5.6.3 Motivation for modularity

Each power source (including energy storage) has its own PMU interfacing it with the grid. The use of two PMUs has been discussed in the previous sections, however, the modular nature allows new/more modules to be developed and easily integrated with the microgrid. For example, other power sources such as diesel generators, turbines for small scale hydro etc. can easily be connected to the network using specialized PMUs. Each source unit is designed to optimize power utilization from the respective sources, and to control the power flow in the network. As load units are controlled based on the decisions made by the source units, many loads for a single residence can be powered and controlled by a single source PMU. In the previous sections, residential loads have been highlighted as having a single PMU. However, for the

connection of other loads, such as agricultural loads (e.g. pumps) or commercial loads (e.g. freezers), separate PMUs could be used.

These microgrids can easily be expanded because they are designed to be modular. Power sources or loads can seamlessly be added to or removed from the network using PMUs that automatically integrate into the distributed communication and control network. The microgrid remains operational and stable with these configuration changes. This allows distributed generation to be easily integrated with the microgrid.

5.7 Software Overview

The microgrid will often be under-supplied because ensuring that all loads are served with certainty under various contingencies is too costly given that it will require higher capacity PV panels and batteries. Therefore, the PMU needs control software that efficiently allocates and dispatches power, considering generation and load uncertainty. This section provides an overview of software that can potentially be deployed on the grid for efficient management of resources.

This software should enable the grid to learn about user preferences in terms of power demand; produce a schedule that accounts for the stochastic nature of generation and load; and make dispatch decisions in real-time based on grid state estimates as shown in Fig. 5-7. The scheduling with load forecast has been developed [63], while the generator scheduling and dispatch aspects of the software are proposed for future development.

5.7.1 Scheduling

Studies indicate that common criteria for grid contingency scheduling (such as the $N - 1$ condition) are too conservative and do not represent the true probability of failure [64]. Instead, the PMU schedules generation and load by explicitly reasoning about the probability of not serving the requested load. This reduces cost and improves user comfort. The scheduling algorithm takes as input generation and load forecasts and outputs a schedule with probabilistic guarantees on serving load. It does this

by employing a risk-based tatonnement approach that is able to run on a distributed network of low-cost microcontrollers [63].

Load forecast

Instead of modeling power demand as an agglomerated load curve, the software uses statistical learning to classify loads into user activities (i.e. charging a cell phone or lighting at night) [65][66]. This approach allows the microgrid to make smart decisions about how to schedule and shed load, which means that the grid is able to constantly improve the load forecast by updating its model of user preferences.

Generator forecast

Historical solar irradiation data can be used to predict the solar profile for the scheduler. For example, National Renewable Energy Laboratory provides historical Irradiance and temperature data for many countries [67]. The data can be used to create the probability of various scenarios, such as sunny vs. cloudy days, to account for uncertainty in generation.

5.7.2 Real-time dispatch

Using state estimates for the batteries' charge states and loads' current power consumption, the dispatch algorithm can decide which loads to serve and which batteries provide power. The dispatcher makes decisions to ensure that users receive an agreed upon quality of service and that excess battery capacity is rewarded. Hierarchical control is applied, as described in section 5.5, to ensure that each generator contributes the allocated amount and maintains the grid voltage within limits.

5.8 Conclusion

The ad hoc microgrid creates a decentralized energy market that enables scalable deployment of distributed generation to provide affordable electricity in off-grid areas.

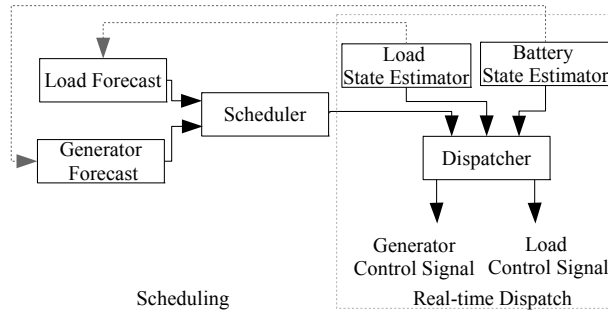


Figure 5-7: Overview of scheduling and dispatch in the grid.

Compared to individual Solar Home Systems, the cost per watt of electricity provided by this network is lower. This is due to demand aggregation, as larger but less expensive (\$/W) solar panels can be used rather than the smaller (less wattage) individual solar home systems. Also, by managing the aggregated demand, resources can be utilized optimally, further reducing the cost of generation and storage. The cost of distribution is also reduced, compared to centralized microgrids (all the generation co-located) that are currently being deployed, because power sources are distributed (in close vicinity of the loads). Compared to conventional microgrids, this system is less capital intensive and more scalable because it is built from the bottom up, and is inherently modular rather than depending on a large centralized generation facility. Hence, the proposed system provides affordable and scalable electricity access.

Chapter 6

Designing Low-cost Source and Load Converters

The ad hoc microgrid is composed of solar panels, batteries, source PMUs, load PMUs, wiring and appliances. The PMUs consist of power conversion, communication and control modules. The source unit's power conversion module consists of a charge controller (to charge the battery from the solar panel) and a source converter (to interface the battery to microgrid). In this thesis, for development of PMUs, an off-the-shelf charge controller was used (Linear Technology's LT8490), hence, only the source converter design will be discussed in this chapter. The load unit's power conversion module consists of a load converter. The details of the source and load converter are described in Section 6.1 and 6.2.

6.1 Source Converter

The source converter is the interface between the power source and the network. It is a bi-directional converter which takes power from the battery, steps it up to the network voltage, and takes power from the network and stores it in the battery. Table 6.1 summarizes the converter specifications.

Table 6.1: Source converter specifications

Parameter	Value
Input (battery-side) Voltage Range	10-15 V
Nominal Output (grid-side) Voltage	24 V
Output power	250 W

6.1.1 Selection of topology to reduce cost

The cost of a converter depends on its power range, voltage range, frequency of operation and efficiency. These factors also dictate the converter topology selected. Power and voltage range are dependent on the applications and are determined by the system level design. Hence, the control handles available are frequency of operation, efficiency of operation and topology selection. The low-cost power converters commonly found in the market are generally based on the lowest part count and cost topology. These converters are operated at low frequencies, and are comprised of low-cost and inefficient components. The low-cost components adversely affect the efficiency of these converters, especially over a wide voltage or power range.

The topology selected determines the number of components used as well as the voltage and current stresses on these components. These components, consisting of energy storage devices, switching devices, ICs, PCB and cooling systems, determine the cost of the converter. Within these components, the magnetics and switching devices are usually not only the dominant cost, but are also directly dependent on the topology selected.

Cost of magnetics

The key drivers of the cost of magnetics are the material and labor costs [68]. The amount of energy which needs to be stored affects the size of the magnetics, and thus the material cost. A higher energy storage requirement needs more material, leading to an increase in cost. The labor cost is determined by the manufacturing process utilized, which is mostly dependent on the frequency of operation and the efficiency required. For example, in a high frequency design, litz wire is used to decrease loss;

constructing Litz wire is a more labor intensive process than constructing solid wire, which increases costs.

Cost of switching devices

The cost of switching devices is determined by the chip area and packaging. The chip area is determined by the current and voltage stress. In a vertical device, the voltage determines the die thickness, while current determines the die area. In a lateral device, both current and voltage influence die area. Hence, higher current and voltage stresses increase the chip size, resulting in higher cost [69].

A direct converter, which has a direct dc path between input and output, has less energy storage requirements and less switch device stresses compared to an indirect converter [70]. As the cost of magnetics and switches can be reduced by selecting a direct converter, a synchronous boost converter, which is a direct converter, was implemented, as shown in Fig. 6-1. This converter acts as a synchronous boost converter for power flow from the battery to the grid and as a synchronous buck converter when charging the battery from the grid.

6.1.2 Designing the power stage of the source converter

The synchronous boost converter steps up the voltage from 12 V to 24 V with some additional range for both input and output voltage variation. The chosen frequency of operation is 500 kHz. The three categories of components to choose are: inductors, transistors and capacitors. Table 6.2 summarizes the parameters of the source converter.

The value of the inductor determines the current ripple, and hence the losses in the inductor and transistors. In this converter, high input current (up to 20 A) can flow, and hence it is preferred that it operates in continuous conduction mode (CCM) at high power, which reduces the current ripple. A current ripple of 10% peak-to-peak at full power (2.5 A) is chosen. This results in an inductor size of 4.8 μH with 0.5 duty cycle (D_b), using Equation (6.1). Where $V_{i,b}$ is the input voltage of the boost

Table 6.2: Source converter parameter values

Parameter	Description	Nominal Value
$V_{i,b}$	Input Voltage	12 V
$C_{i,b}$	Input Capacitance	110 μF
L_b	Inductor	4.7 μH
$C_{o,b}$	Output Capacitance	120 μF
$V_{o,b}$	Output Voltage	24 V
D_b	Duty Cycle	0.5
D'_b	1-Duty Cycle	0.5
f_b	Switching Frequency	500 kHz
$I_{o,b}$	Output Current at Full Load	10.42 A
$R_{o,b}$	Output Resistance ($V_{o,b}/I_{o,b}$)	2.3 Ω

converter, f_b is the switching frequency and $\Delta i_{L,b}$ is the peak-to-peak ripple current. A 4.7 μH inductor was chosen, as it is the closest standard value readily available.

$$L_b = \frac{V_{i,b} D_b}{f_b \Delta i_{L,b}} \quad (6.1)$$

The transistors need to handle this peak current stress, and have low output capacitance and on-state resistance to minimize loss of the converter. The peak current of the transistors is given by Equation (6.2).

$$I_{sw-pk,b} = \frac{\Delta i_{L,b}}{2} + \frac{I_{o,b}}{1 - D_b} \quad (6.2)$$

Maximum $I_{sw-pk,b}$ is around 22 A for both transistors, and the maximum voltage stress is equal to $V_{o,b}$, 24 V. The transistors chosen, as seen in Table 6.3, can handle these stresses.

The output voltage needs to have a small ripple (less than 100mV). Hence, the output capacitor is selected accordingly, using Equation (6.3).

$$C_{o,b} > \frac{I_{o,b} D}{f_{sw,b} \Delta v_{o,b}} \quad (6.3)$$

Slightly larger capacitance is chosen to account for the added ripple due to ESR of the capacitance.

The prototype board is shown in Fig. 6-2, and the detailed schematic and PCB

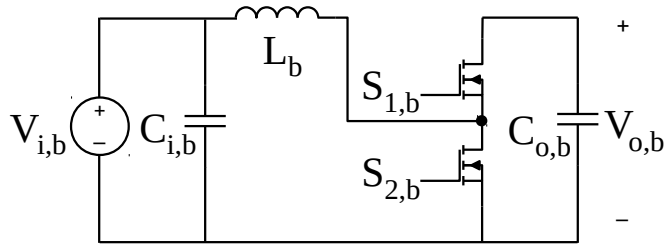


Figure 6-1: Schematic of the source converter implemented using synchronous boost topology.

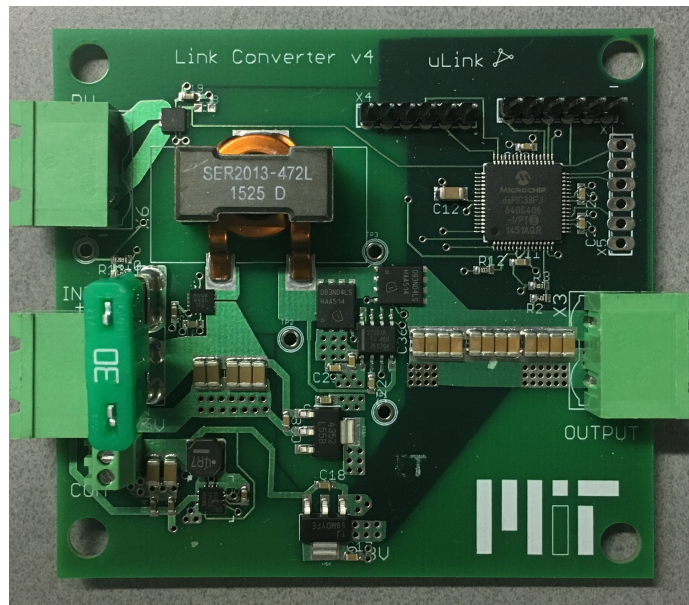


Figure 6-2: Prototype board of the source converter

layout can be found in Appendix B.

6.1.3 Cost of the converter

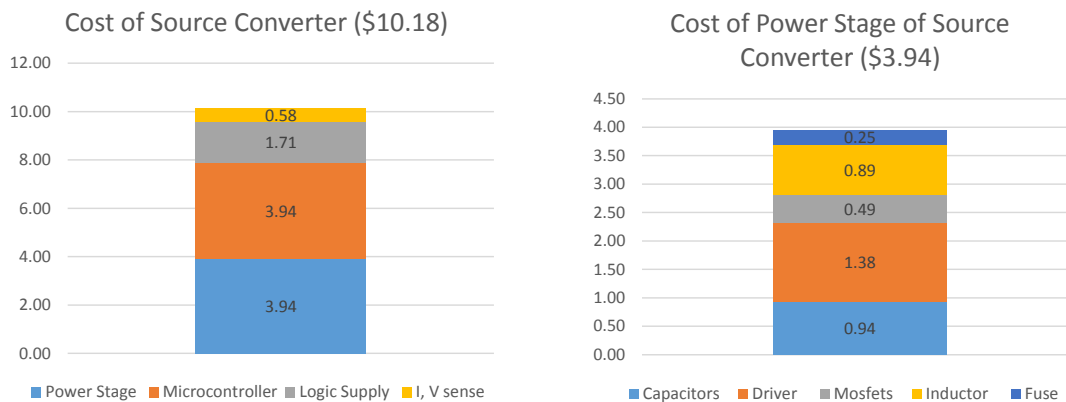
The converter's power stage has been optimized for low cost, as shown in Fig. 6-3 and Table 6.3. Costs are indicated for published supplier component costs (e.g., from "digikey") at 10,000 unit component quantities. The logic supply cost and microcontroller cost can further be reduced, as shown in Table 6.4, as they have not been optimized for this design. The detailed schematics, PCB layout and bill of materials for the source converter is provided in Appendix B.

Table 6.3: Components of the power stage of source converter

Components	Type	Cost (\$)
Fuse	30A/32VDC Automotive Fuse (0287030.PXCN), Qty: 1	0.116
Capacitors	Input: 22 μ F/25V 1206 X5R MLCC, Qty:5	0.112
	Output:10 μ F/50V 1206 X5R, Qty:12	0.816
Inductor	4.7 μ H Coilcraft's power Inductor SER2013-472MLB	0.89
Gate Driver	120V/3A High and low side gate driver (UCC27201A), Qty: 1	1.38
MOSFET	40V/ 49A, N- Channel OptiMOS (BSC093N04LS), Qty: 2	0.49

Table 6.4: Other components of the source converter

Components	Type	Cost (\$)
Controller	50 MIPS, 1.04ns PWM Resolution (DsPIC33FJ64GS406), Qty: 1	3.83
	Capacitors:0.1 μ F/25V 0603 Qty:4, 10 μ F/50 V 1206, Qty: 1	0.0778
Current Sensor	\pm 15.5 A Hall effect sensor (ACS711), Qty: 1	0.448
Voltage Sensor	0.1% 0.1 W- Resistors 0603, Qty: 4	0.125
Buck Converter	5V/1A Synchronous Buck Regulator (TS30011), Qty: 1 4.7 μ H/ 2A	0.325
	Inductor Qty: 1, 0.1 μ F/25 V Capacitors, Qty: 4	0.354
Voltage Regulators	3.3V/1A Low-dropout voltage regulator (TLV1117-33), Qty: 1	0.165
	10V/1A Low-dropout voltage regulator (LM2940), Qty: 1	0.818



(a) Source converter

(b) Power stage

Figure 6-3: Cost of 250 W bidirectional boost converter. Costs are based on published distributor costs at 10,000 component pricing.

6.1.4 Control of source converter

In order to regulate the output voltage of the converter, the average current mode control was implemented [71]. This is a two-loop control, with an inner current control loop and an outer voltage control loop. Because the inner loop is much faster than the outer loop, the converter model can be simplified, as shown in Fig. 6-4 [72].

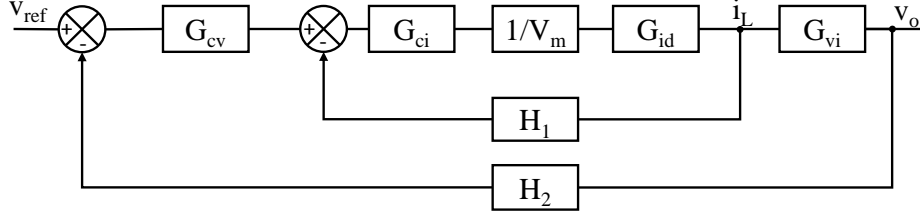


Figure 6-4: Average current control converter model

First, the inner current control function, G_{ci} is found using the pidtune function of MATLAB. For this, G_{id} (transfer function i_L/d of the converter) is needed, which is given by Equation (6.4), using $V_m = 3.3$ and $H_1 = 1$ (reference is set as i_L). G_{id} and the open loop transfer function ($T_i(s)$) with the current loop controller is shown in Fig. 6-5.

$$G_{id} = \frac{sC_{o,b}V_{o,b} + I_{L,b}2D'_b}{s^2L_bC_{o,b} + s(L_b/R_{o,b}) + D_b'^2} \quad (6.4)$$

Second, the outer voltage control function, G_{cv} is found by using the pidtune function. For this, the current dynamics are neglected because of the fast response of the inner control loop, and G_{vi} is simplified by neglecting the inner current loop dynamics as shown in Equation (6.5). G_{vi} and the open loop transfer function ($T_v(s)$) with the voltage loop controller is given in Fig. 6-6. The open loop transfer function of the system is shown in Fig. 6-7. The current reference for the inner loop is generated using the outer voltage loop.

$$G_{vi} = \frac{1 - D}{sC_{o,b} + 1/R_{o,b}} \quad (6.5)$$

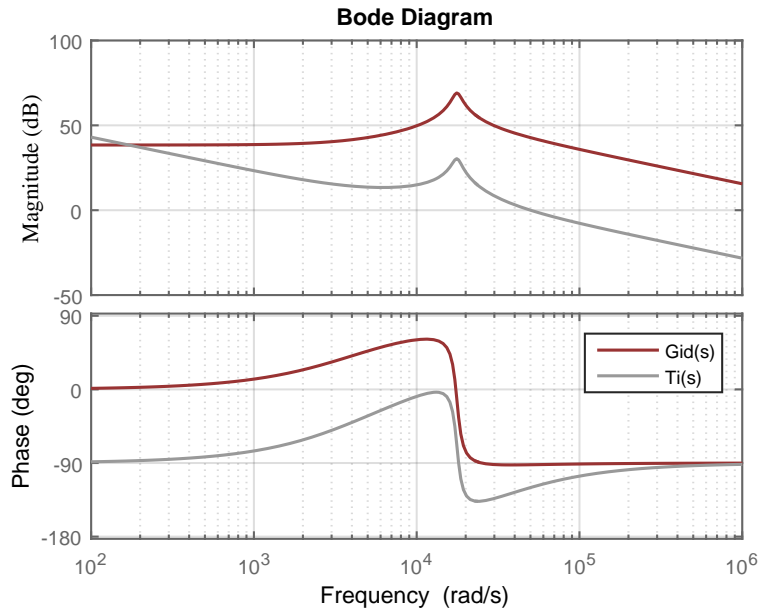


Figure 6-5: Bode plot of $G_{id}(s)$ and $T_i(s)$.

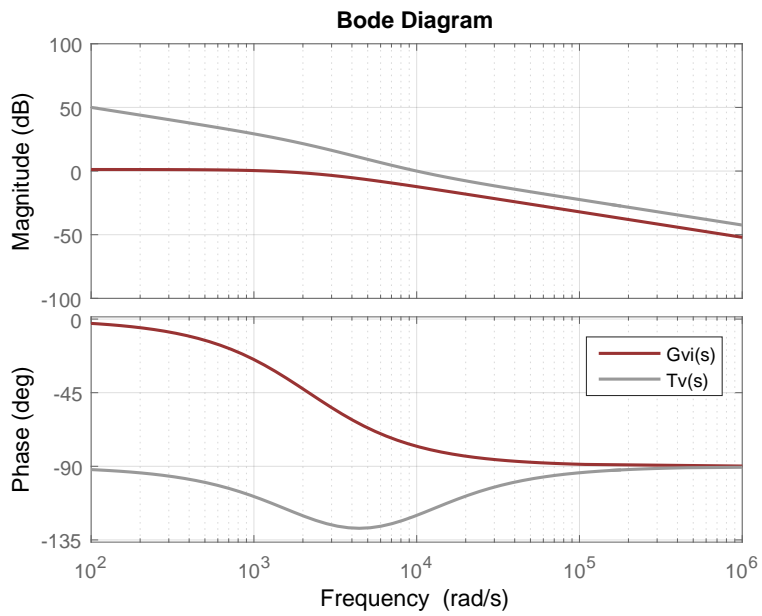


Figure 6-6: Bode plot of $G_{vi}(s)$ and T_v .

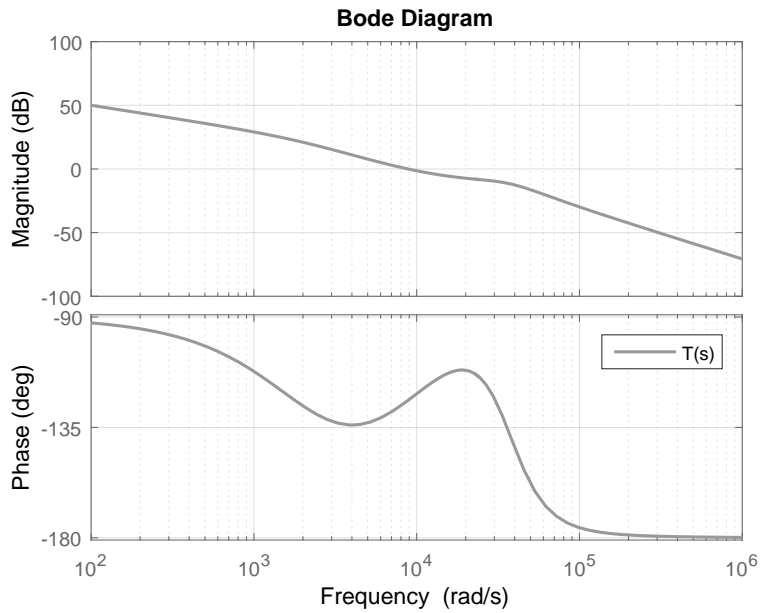


Figure 6-7: Bode plot of $T(s)$.

6.1.5 Experimental results

The efficiency of the converter was measured across the entire range from 2.5 W to 250 W for 12 V input and 24 V output, as shown in Fig. 6-8. A peak efficiency of 96.6% was achieved.

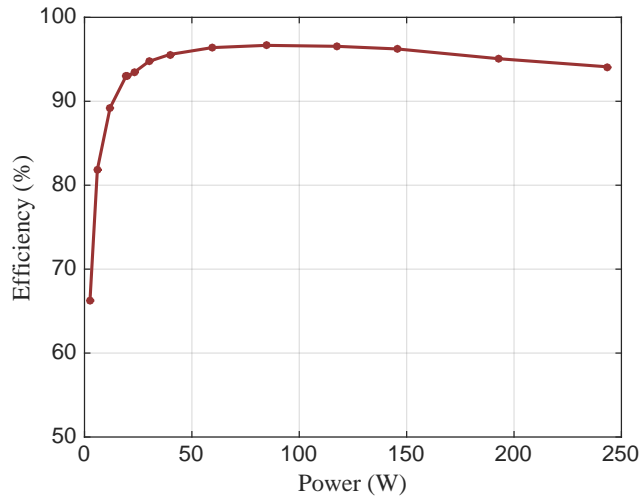


Figure 6-8: Efficiency of boost converter from 2.5 W to 250 W for 12 V input and 24 V output.

Because of the loss, a heat sink needs to be used to keep the temperature of

the converter within safe limits. Advanced Thermal Solutions' maxiFLOW heat-sink (ATS-52310P-C1-R0) was used. However, for avoiding the additional cost associated with the heat-sink, the enclosure of the source unit could be appropriately designed.

6.2 Load Converter

The load converter provides the conversion necessary to power different loads from the microgrid. It can switch the loads on and off and control how much power they consume.

The most common uses of electricity vary in different communities in developing countries, depending primarily on the weather, cell phone coverage and entertainment trends. In the hotter climate of South Asia, the most common usage of electricity is for lighting, communication and cooling, i.e. for lights, cellphone charging and fans [73]. Televisions and refrigerators are also desired, but not many people can afford them or pay for the electricity used to power them. Hence, 25 W is sufficient to power basic loads, as shown in Table 6.5. Consequently the load converter for the PMU is specified to provide the following outputs:

Table 6.5: Power ratings of common appliances

Application	Quantity	Approximate power rating (W)
Led lights	2	2.5 W
Cell phone	1	5 W
Fan	1	15 W

- 12 V, 5 W current regulated output for LED lights.
- 5 V, 2.5 W voltage regulated output for cell phone charging.
- 12 V, 15 W voltage regulated output for fans, tv etc.

6.2.1 Designing with safety consideration

Safety consideration is critical for electrical products which people come into contact with. For a product's safety, the four hazards that need to be considered are; electric shock, high energy hazard, mechanical injury and fire hazard. All these are important, but during the design phase of electric circuits, safety consideration for electric shock hazard is primarily considered.

As specific safety standards do not exist for rural microgrid equipment, IEC 60950 "Safety of information technology equipment" [74] is used as the most relevant standard available. Also, Power over Ethernet (PoE) is the most similar application available which deals with delivery of data and power in ad hoc systems with similar voltage and power characteristics as the ad hoc microgrid.

Considering standards for a similar application: power over ethernet

Power over Ethernet (PoE) is a method to transmit data and power over ethernet cables. These are unshielded twisted pair (UTP) cables such as CAT5 or CAT6. Common applications of PoE are wireless access points, security cameras and voIP phones. IEEE 802.3 standardizes this transfer of data and power, and the most recent standard governing PoE is IEEE 802.3at (also known as PoE plus), which can power up to 25.5 W at a maximum voltage of 57 V. However, there are also higher power PoE devices, such as those from Linear Technology, which are backward compatible with these standards.

Figure. 6-9 shows power sourcing equipment (PSE) and a powered device (PD) in a PoE architecture (referred to as Alternative B). Here, power is transferred on a spare pair of wires, however, power can also be transferred on data lines with center trapped transformers (referred to as Alternative A).

Although the PD is operating at less than 60 V, which is considered Safety Extra Low Voltage (SELV), it is still not completely safe as it is connected to the PSE by long cables which can pick up voltage transients. This can be due to inductive or capacitive coupling of high voltages present close by. Hence, it is categorized as

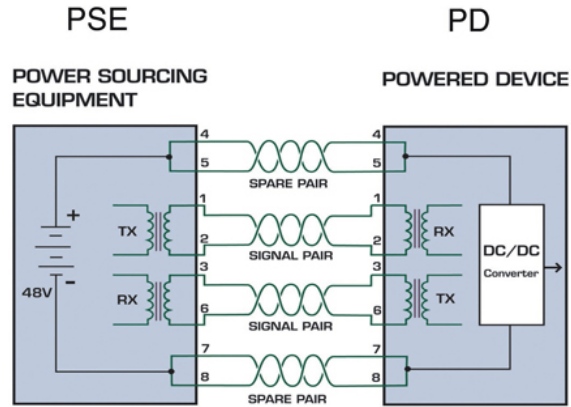


Figure 6-9: Power can be transferred using spare pair of wires on ethernet cables. Image from: Ethernet Protection Guide [4].

SELV-derived TNV-1, where TNV stands for Telecommunication Network Voltage. According to isolation requirements of IEEE 802.3, based on IEC60950 sub-clause 6.2 [75], isolation is needed between SELV circuits and telecommunication networks, as high voltage transients might be picked up and carried through the lines. Hence, the PD has to be isolated. This means that the dc/dc converter, as shown in Fig. 6-9, in the PD needs to have galvanic isolation. This may be avoided if the enclosure itself is isolated and has no exterior connectors, such as non-isolated buttons or conducting wires.

In the ad hoc microgrid load power management unit, the load converter needs to be isolated as it has accessible external connectors for loads. Also, isolation is especially needed for powered devices if the cable is externally routed (outside buildings, which might not share the same ground), which is the case in the ad hoc microgrid application. Another reason for the need for isolation is unreliable grounding [76], which might occur in this application.

Protection during lightning strike

The damage done by a lightning strike is determined by what the strike hits. According to IEC 62305 "Protection against lightning- Part 4: Electrical and electronic systems within structures" [77], lightning could be damaging if it strikes any of the following:

- Building or structure.
- Earth next to the structure.
- Supply line.
- Earth next to the supply line.

A direct lightning strike is catastrophic. There is no protection scheme that can reliably protect a power line or structure if lightning hits it. To avoid lightning hitting a structure or wiring, protection measures such as lightning arrestors can be deployed [77].

While designing power converters for this application, protection for only indirect lightning strikes needs to be considered. An indirect strike is when lightning strikes the earth or a structure next to power lines. Indirect strikes affect the voltage of a line by electromagnetic pulses, electrostatic pulses and ground potential rise [78]. Electromagnetic pulses appear due to the large magnetic fields being generated by the large current burst created by lightning. This is usually in the form of a common mode voltage transient. However, if the power line and the ground line have different lengths, or if the protection devices on one of the lines fails to work, this common mode transient converts to a differential mode voltage transient. A transformer can protect against common mode transients, but cannot protect against differential mode voltage transients. Electrostatic pulse, created by the electrostatic field, results in the lines being electrically charged. These lines have to be discharged by a connection to the earth. The ground potential rise is due to the large currents flowing in the non-zero resistance of the ground, which creates a temporary ground potential rise.

The transients over voltages caused by an indirect lightning strike are of very short duration and high intensity; they are commonly know as surges, and require the use of surge protection devices. However, over voltage transients might also occur due to switching of large electrical equipment on the network. Surge protection devices suppress these over voltage transients by short circuiting the two lines, or the line to the ground. To suppress differential mode transients, surge protection devices (SPDs)

are placed between the two lines, and to suppress common mode transients the SPDs are connected from line to the ground. Generally, the voltage and current ratings of the common mode SPDs need to be higher. Varistors (MOVs or Polymer), zener diodes and Avalanche TVS diodes are some of the commonly used SPDs that might be used in circuits [79]. Transient voltage surge suppressors (TVSS) such as TVSS diodes are a low-cost solution to suppress these high voltage transients. However, they have a very low current rating and will not be able to withstand very high currents (which flow during a surge). Hence, the TVS clamps the voltage to a safe value till the bulk input capacitor starts to charge up. The use of a transformer, as well as TVSS has been shortlisted for this application.

6.2.2 Topologies considered

Isolated topologies were considered for this converter, as galvanic isolation is desired for safety reasons, such as protection from lightning strikes or other fault conditions. Transformers are commonly used for this purpose, as not only do they provide isolation, but also provide any required voltage transformation (through the transformer turns ratio). However, in this case, only a modest voltage conversion ratio is needed.

Flyback, forward and push-pull topologies were considered for the load converter. A flyback converter was implemented, with a single switch and single diode. The advantages of the flyback topology, in this context, are that it requires very few components, and can provide multiple isolated outputs using a multi-winding transformer. In this case, a 5 V cell phone charging outlet could have been an additional output of the transformer, however, to avoid cross regulation, an off-the-shelf IC was used to drop the voltage from 12 V to 5 V, as the 5 V power requirement is low (about 10% of the total power, i.e. 2.5 W). Although the flyback topology utilizes relatively fewer components, it has high device stresses, and requires an energy storage transformer that can have relatively high volume and cost.

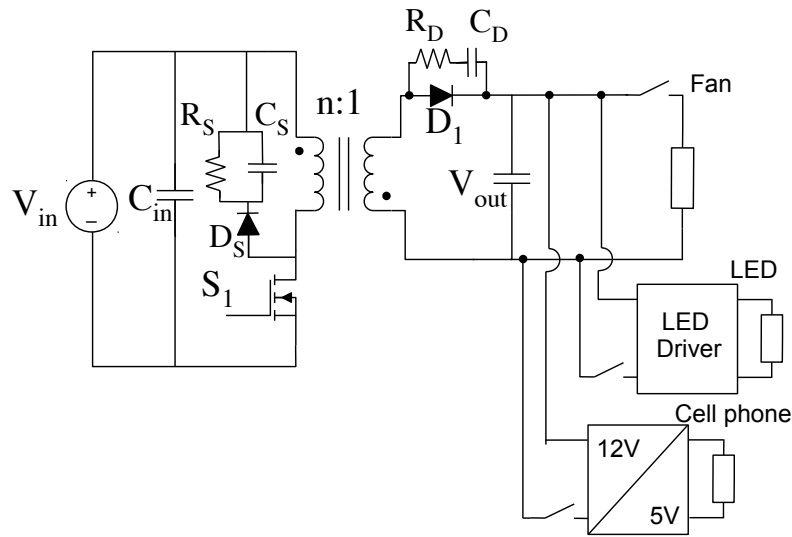


Figure 6-10: Schematic of the load converter with a flyback main power stage.

6.2.3 Design of the 12 V power stage

The specifications for the converter are given in Table 6.6 and the flyback topology implemented is shown in Fig. 6-10.

The flyback converter is composed of three stages: the inversion stage, transformation stage and rectification stage. The inversion stage is composed of a single switch, the transformation stage is composed of a transformer, and the rectification stage is composed of a single diode. Due to parasitics of the transformer, snubber circuits are added to protect the switch and diode. As described below, there is also transient voltage suppression and EMI filtering provided at the input of the flyback converter. The capacitance of the EMI filter also serves to provide improved network stability, as described below and in Chapter 8.

Type of operation

The flyback is a well-studied topology, and good design references for it are easily available [80]. The first decision to be made is whether to operate in Discontinuous

Table 6.6: Power ratings of common appliances

Parameter	Specifications
Power Stage	
Input Voltage	24-25 V
Output voltage	12 V
Rated Power	25 W
Cell Phone Converter	
Input Voltage	12 V
Output voltage	5 V
Rated Power	5 W
LED Driver	
Input Voltage	12 V
Output voltage	12 V
Rated Power	5 W

Conduction Mode (DCM) or Continuous Conduction Mode (CCM). In CCM, the RMS current is lower than in DCM, which leads to lower conduction and MOSFET turn-off losses, and requires a smaller EMI filter. However, unlike DCM, it has a right-half plane zero, thus requiring careful design of the compensator. As high switching frequencies (greater than 500 kHz) will be used, it is preferred to operate in CCM mode to decrease the current ripple, as litz wire cannot be used due to cost constraints.

Transformer

The transformer design requires calculating the transformer turns ratio and the magnetizing inductance. Limiting the duty cycle to 50% would be preferred, as not only will it decrease the voltage stress on the diode, but also eliminates the need for slope compensation (for subharmonic oscillations) in the feedback design [81].

Using a maximum 50% duty cycle ($D_{max} = 0.5$), the turns ratio is found using Equation (6.6).

$$n_{s2p} = \frac{(V_{out} + V_{f,diode})(1 - D_{max})}{(V_{in,min}D_{max})}, \quad (6.6)$$

where n_{s2p} is the secondary to primary turns ratio of the transformer, V_{out} is the output voltage of the converter, $V_{f,diode}$ is the forward voltage drop of diode, D_{max} is

the maximum duty cycle and $V_{in,min}$ is the minimum input voltage of the converter. The chosen output voltage is 12 V, the forward voltage drop of the diode is 0.45 V and the minimum input voltage selected is 24 V. This results in n_{s2p} of 0.52.

Next, the magnetizing inductance, L_m , is found, using Equation 6.7, which will ensure CCM operation over a wide range of output power.

$$L_m = \frac{(V_{out} + V_{f,diode})(1 - D_{nom})^2}{2I_{out}\beta f_{sw}n_{s2p}^2}, \quad (6.7)$$

where D_{nom} is the nominal duty cycle, I_{out} is the output power of the converter, β is the percentage of the maximum load current at which the converter still operates in CCM and f_{sw} is the switching frequency of the converter. $D_{nom} = 0.5$, $I_{out} = 2.0833A$, $\beta = 0.15$ and $f_{sw} = 524$ kHz are used to get L_m of 35 μ H.

An off-the-shelf transformer with similar rating to that calculated above was selected; the closest transformer that could be found was the Coilcraft FA2900-alb transformer, which is designed for Power Over Ethernet flyback converters. This converter has a transformer turns ratio of 0.47 and magnetizing inductance of 40 μ H. These values result in a maximum duty cycle of 0.52 and a β of 13%.

The primary current of the transformer is calculated to design the transformer. For this, the primary peak current is first calculated using Equation (6.8), which is also used for over current protection.

$$\begin{aligned} I_{p,pk} &= \frac{I_{in}}{D_{max}} + \frac{I_{p,ripple}}{2}, \\ I_{in} &= \frac{I_{out}n_{s2p}D_{max}}{(1 - D_{max})\eta_{conv}}, \\ I_{p,pk2pkripple} &= \frac{V_{in}D_{max}}{f_{sw}L_m}. \end{aligned} \quad (6.8)$$

where $I_{p,pk}$ is the peak current of the transformer primary, I_{in} is the input current of the converter, $I_{p,pk2pkripple}$ is the peak-to-peak ripple current of the transformer primary and η_{conv} is the expected efficiency of the converter. Using an expected efficiency of 86% resulted in $I_{p,pk2pkripple}=0.6$, $I_{in}=1.26$ A and $I_{p,pk}=2.7$ A.

$$I_{p,rms} = \sqrt{D} \sqrt{I_{p,pk}^2 + \frac{I_{p,pk-pkripple}^2}{3} - I_{p,pk} I_{p,pk2pkripple}}. \quad (6.9)$$

Using the above calculated values and Equation (6.9), $I_{p,rms}$ is found to be 1.74 A. The code to calculate these values is provided in Appendix B.

Transistor and snubber circuit

There is high voltage stress on the switch due to the leakage inductance of the transformer. When the switch turns off, the current in the leakage inductance begins to charge the output capacitance of the switch. The higher this current, the greater the voltage stress. The energy is then dissipated in the switch. In order to reduce the switch voltage, a snubber circuit is used. The simplest clamping snubber circuit is the RCD snubber, which is composed of a resistor, capacitor and a diode (R_s , C_s and D_s in Fig. 6-10). The leakage inductance energy is dissipated in the resistor of this snubber circuit.

When the switch is turned off, ideally (without parasitics of the transformer), the voltage on the Mosfet is given as $V_{ds} = V_{in,max} + (V_{out} + V_{f,diode})/n$, which approximately equals 51 V. Using the the snubber voltage of around 51 V, R_s is found using Equation (6.10) [82], the required snubber resistance is calculated as:

$$R_s = \frac{(2V_{snub} - nV_{out})^2 - (nV_{out})^2}{2L_{leakage}f_{sw}I_{p,pk}^2}, \quad (6.10)$$

where V_{snub} is the snubber voltage and $L_{leakage}$ is the primary-side leakage inductance of the transformer. This equation gives us a resistance of approximately 3 k Ω . In order to have a 2.5% ripple of the snubber voltage, the snubber capacitance is chosen using Equation 6.11.

$$C_s = \frac{V_{snub}}{R_s f_{sw} \Delta V_{snub}}, \quad (6.11)$$

where ΔV_{snub} is 2.5% of V_{snub} . This equation results in a capacitor value of approximately 25 nF.

Input and output capacitance

The output capacitor needs to be designed to reduce the output voltage ripple and also to allow a small step in voltage with a large step in output current. The capacitor which justifies both these requirements is found using Equations (6.12) and (6.13).

$$C_{out,ripple} = \frac{I_{out}}{V_{out,ripple} f_{sw}}, \quad (6.12)$$

$$C_{out,step} = \frac{\Delta I_{step}}{2\pi \Delta V_{out,step} f_{bw}}, \quad (6.13)$$

where $V_{out,ripple}$ is the output voltage ripple, ΔI_{step} is the output current step, and f_{bw} is the control bandwidth of the converter. Using an output voltage ripple ($V_{out,ripple}$ of 1%), maximum current step (which is the largest load switching on) of 0.8 A and tolerable output voltage step of 0.5 V, an output capacitor value of 48.5 μF and 16 μF is calculated using Equation (6.12) and (6.13), respectively. Hence, an output capacitance of at least 50 μF is chosen.

The input capacitance required to provide 1% input voltage ripple is calculated using Equation (6.14).

$$C_{in,ripple} = \frac{I_{in}}{DV_{in,ripple} f_{sw}}, \quad (6.14)$$

This value is 19 μF , however, a much larger input capacitance (60 μF) is used to reduce the input voltage ripple as this equation does not take into account the long wiring from the source unit to the load unit.

Rectification diode and rectifier snubber circuit

The rectification diode ideally has to block a voltage of $V_{out} + V_{in}/n$. However, ringing is observed when the MOSFET turns on due to the parasitic capacitance of the schottky diode and the transformer leakage inductance. An RC snubber can be used to reduce this ringing [83]. In order to reduce the ringing frequency by half ($f_{osc} =$

Table 6.7: Specification of components chosen for LTC3805-5

Pin	Description
Pin 1 (SSFLT)	For soft start a 10 nF capacitor is used. The converter starts in about 1.2 ms and then has a soft start of 2.6 ms
Pin 2 (ITH)	This pin is used to get isolated voltage feedback. The description of the feedback is provided in the text
Pin 3 (FB)	As isolated feedback is used hence this pin is grounded
Pin 4 (RUN)	A voltage divider with 3.7 k and 47 kΩ is used to provide a run voltage of 14 V
Pin 5 (FS)	For a frequency of 524 kHz, a resistor of 47 kΩ is used
Pin 6 (SYNC)	Pin is left open
Pin 7 (ISENSE)	20 mΩ resistor is used
Pin 8 (OC)	For over current protection a resistor divider of two 1 kΩ resistors is added at Vsense
Pin 9 (Vcc)	A resistor of 10 kΩ and a capacitor of 1 μF are used for initial start-up, and then the IC is powered by auxillary winding.
Pin 10 (Gate)	For this, a diode, capacitor (10 μF) and a resistor (330 Ω) are used. This pin is connected to the gate of the transistor

$\frac{1}{2\pi\sqrt{L_{s,leakage}C_{diode}}}$), a diode snubber capacitor ($C_{sn,diode}$) is chosen. This amounts to a diode snubber capacitor equal to about 3 times the diode capacitance, C_{diode} . The diode snubber resistance to provide critical damping is $R_{sn,diode} = \sqrt{\frac{L_{s,leakage}}{C_{diode}+C_{sn,diode}}}$. The resulting values are $C_{sn,diode} = 0.24nF$ and $R_{sn,diode} = 33\Omega$.

Feedback control

For the control of the converter, a Linear Technology IC, LTC3805-5, was chosen. Table 6.7 summarizes the specification of the components used with the IC.

To design the isolated voltage feedback, a linearized model of the converter is valuable. There are many flyback models, which use different assumptions, that can be found in the literature. The flyback converter model from Basso's book is used [5] to design the feedback control. The open-loop transfer function for the flyback converter is given in Equation (6.15).

$$\begin{aligned}
H_{flyback}(s) &= \frac{V_{out}(s)}{v_c(s)} = G_o \frac{(1 + \frac{s}{\omega_{z1}})(1 - \frac{s}{\omega_{z2}})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2})}, \\
G_o &= \frac{R_{out}}{nR_{sense}G_{FB}} \frac{1}{\frac{(1-D)^2}{\tau_L} + 2M_c + 1}, \\
\omega_{z1} &= \frac{1}{R_{ESR,Cout}C_{out}}, \\
\omega_{z2} &= \frac{(1-D)^2 R_{out}}{DL_m n^2}, \\
\omega_{p1} &= \frac{\frac{(1-D)^3}{\tau_L}(1 + 2\frac{S_e}{S_n}) + 1 + D}{R_{out}C_{out}}
\end{aligned} \tag{6.15}$$

where G_o is the dc gain, ω_{z1} is the frequency of the first zero, ω_{z2} is the frequency of the second zero (which is the right half plane zero) and ω_{p1} is the frequency of the first pole. Peak current mode control also adds two poles at half the switching frequency. Q_p is the quality coefficient of the subharmonic poles at half the switching frequency ($\omega_n = \pi f_{sw}$), which is determined by $Q_p = \frac{1}{\pi((1-D)\frac{S_e}{S_n} + 0.5 - D)}$. R_{out} is the output resistor, R_{sense} is the current sense resistor, $\tau_L = \frac{2L_m n^2 f_{sw}}{R_{out}}$, $M_c = \frac{V_{out}}{nV_{in}}$, and G_{FB} is the current gain of the IC. For LTC3805-5, the current gain is unknown, hence, a simulation was used to estimate the current gain, which was calculated to be approximately 20. The first zero is determined by the ESR ($R_{ESR,Cout}$) and capacitance (C_{out}) of the output capacitor. The pole position, determined by ω_{p1} , varies with the compensation ramp. S_e is the compensation ramp slope, which is determined by $\frac{S_n(\frac{1}{\pi} - 0.5 + D)}{(1-D)}$ and S_n is the on-time slope determined by $\frac{V_{in}R_{sense}}{L_m}$. The bode plot of the converter transfer function can be seen in Fig. 6-11.

For the controller, a high dc gain and a high crossover frequency is required for low static error and fast response, respectively. Also, a phase margin greater than 45° is required to avoid an overly oscillatory response. A crossover frequency of $f_{sw}/100$ is chosen (such that the half-cycle sampling lag should not be particularly important). At this frequency, the phase and magnitude of the transfer function is used to calculate the boost required for the phase and gain. For a 65° phase margin, at least 60° of phase boost is required. A type 2 compensator is used, which can provide a phase boost of up to 90° . This compensator has two poles and a zero, with

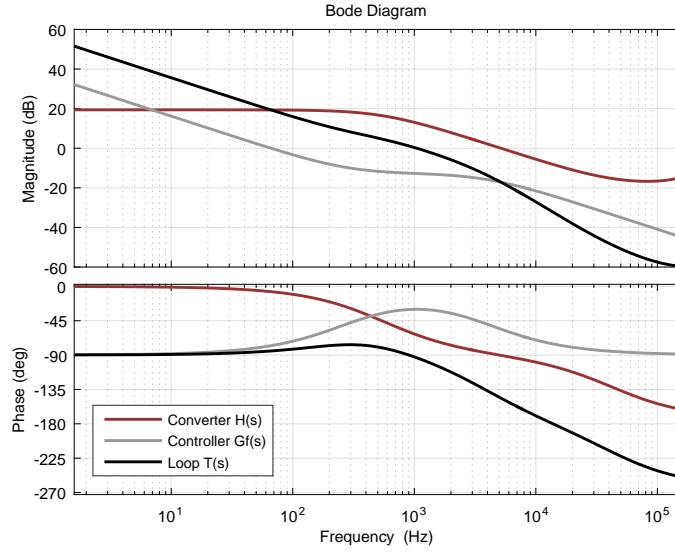


Figure 6-11: Transfer function ($H_{flyback}(s)$) of the flyback converter with and without compensation.

one pole at the origin.

A shunt regulator, TL431, is used to create a type 2 compensator, as shown in Fig. 6-12. The transfer function of the compensator is given in Equation (6.16). Using this equation and the required gain and phase margin, the components of the compensator ($R_{upper}=10\text{ k}\Omega$, $R_{lower}=2.7\text{ k}\Omega$, $R_{LED}=6.5\text{ k}\Omega$, $C_{c1}=5.3\text{ nF}$, $C_{c2}=8.1\text{ nF}$ and $R_{pullup}=10\text{ k}\Omega$) are calculated. A current gain of 20 is used for the IC (G_{fb}).

$$G_{comp}(s) = \frac{V_{FB}(s)}{V_{out}(s)} = \frac{R_{pullup}CTR}{R_{LED}} \cdot \frac{1 + sR_{upper}C_{c1}}{sR_{upper}C_{c,1}(1 + sR_{pullup}C_{c2})}. \quad (6.16)$$

The controller and open loop system bode plot are shown in fig. 6-11.

EMI filter

For EMI suppression, an input filter has to be designed. This filter will also help in achieving stability of the system, as discussed in Chapter 8. The system is shown in Fig. 6-13.

For EMI filter design, the Middlebrook criteria is used [84] to avoid undesirable

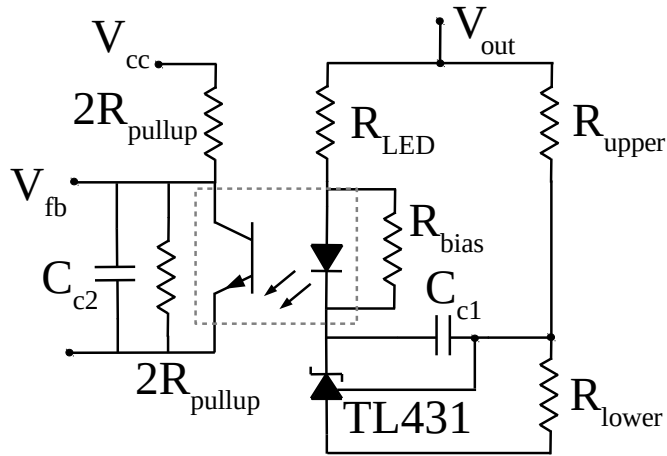


Figure 6-12: Second order feedback using a (model) optocoupler and a TL431 shunt regulator. This technique is described in [5].

converter behavior owing to the effect of the filter. Negative effects to be avoided include changes in the control-to-output dynamics of the converter owing to the input filter and input filter oscillations owing to the negative-input resistance effect of the closed-loop converter. A model for the system, as shown in Fig. 6-14. The open loop input impedance of a flyback converter (Z_D) is given by Equation (6.17), where R is the output resistance, D' is the inverse duty cycle, D is the duty cycle, n is the transformer turns ratio, L_m is the magnetizing inductance, and C_o is the output capacitance.

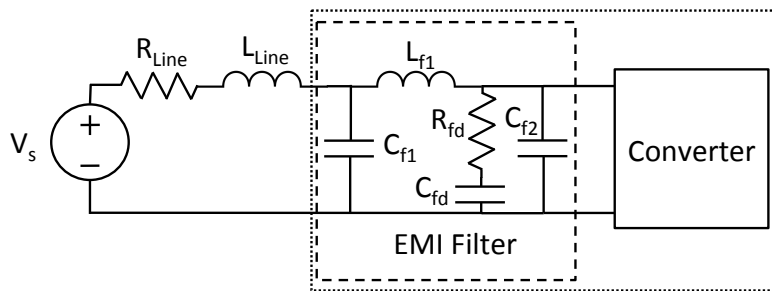


Figure 6-13: Converter System.

Table 6.8: EMI filter Specifications

Parameter	Value
C_{f2}	$60\mu F$
L_{f1}	$8\mu F$
C_{fd}	$125\mu F$
R_{fd}	0.32Ω

$$Z_D = \frac{RD'^2 (1 + s\frac{L_m n^2}{D'^2 R} + s^2\frac{L_m C_o n^2}{D'^2})}{D^2 n^2 (1 + sRC_o)}, \quad (6.17)$$

The closed loop input impedance of the flyback converter (Z_N) is given by Equation (6.18).

$$Z_N = -\frac{D'^2 R}{D^2 n^2} \left(1 - \frac{sLDn^2}{RD'^2}\right), \quad (6.18)$$

The output impedance of the filter Z_o is given by Equation (6.19),

$$Z_o = X_{Cf2} || (X_{Cfd} + R_d) || X_{Lf1}, \quad (6.19)$$

where X_{Cf2} is the impedance of C_{f2} , X_{Cfd} is the impedance of C_{fd} and R_d is the damping resistance which is usually the ESR of the electrolytic capacitor C_{fd} , and X_{Lf1} is the impedance of the filter inductor L_{f1} . Here, C_{fd} and R_{fd} are found by the method highlighted in the paper by Erikson et. al [85] and summarized in Table 6.8.

As $||Z_D||$ and $||Z_N||$ are larger than $||Z_o||$ at all frequencies, the filter does not alter the operation of the regulated converter, as shown in Fig. 6-15. This can also be seen from the magnitude and phase plots of the converter transfer function (G_{vd}) with and without the filter, as shown in Fig. 6-16.

6.2.4 5 V output post regulating converter

A buck converter steps down the 12 V output to provide a 5 V output. Full details of this design are included in Appendix B. As the current requirement is low (less than 1 A), a buck converter IC (TPS562209) was used. This switches at 650 kHz and has

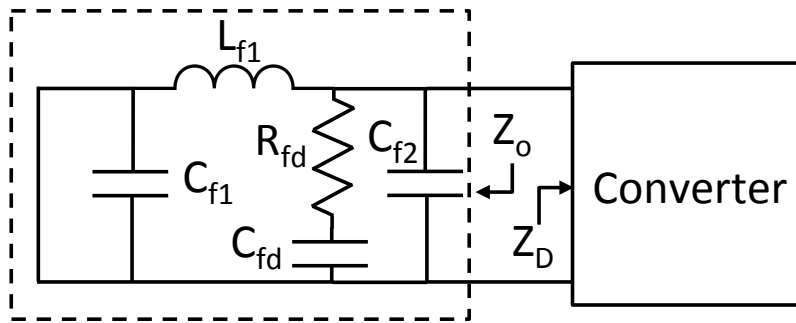


Figure 6-14: Model of the system for designing the EMI filter to not change the control-to-output dynamics of the converter and/or have input filter oscillations owing to the negative-input resistance effect of the closed-loop converter.

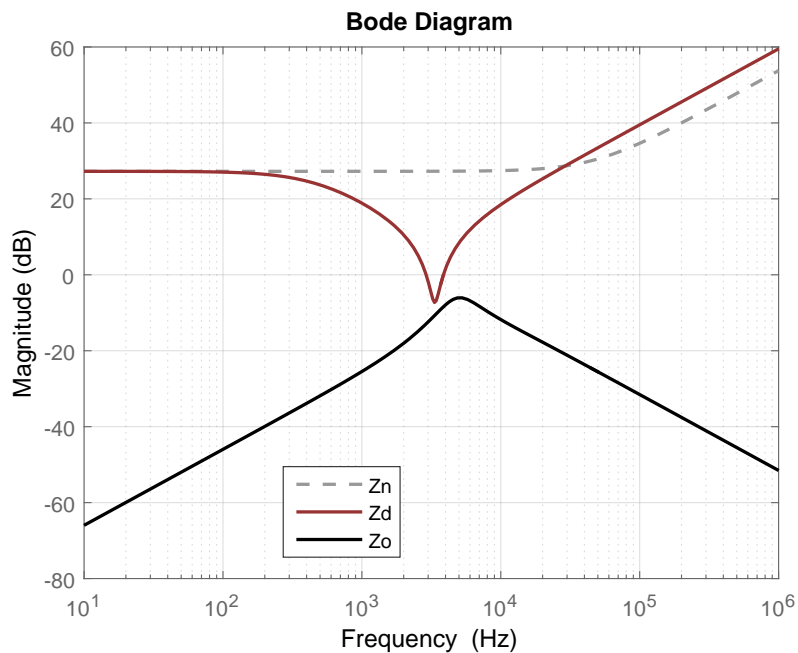


Figure 6-15: Middlebrook's impedance design criteria with input impedance of the converter and output impedance of the filter.

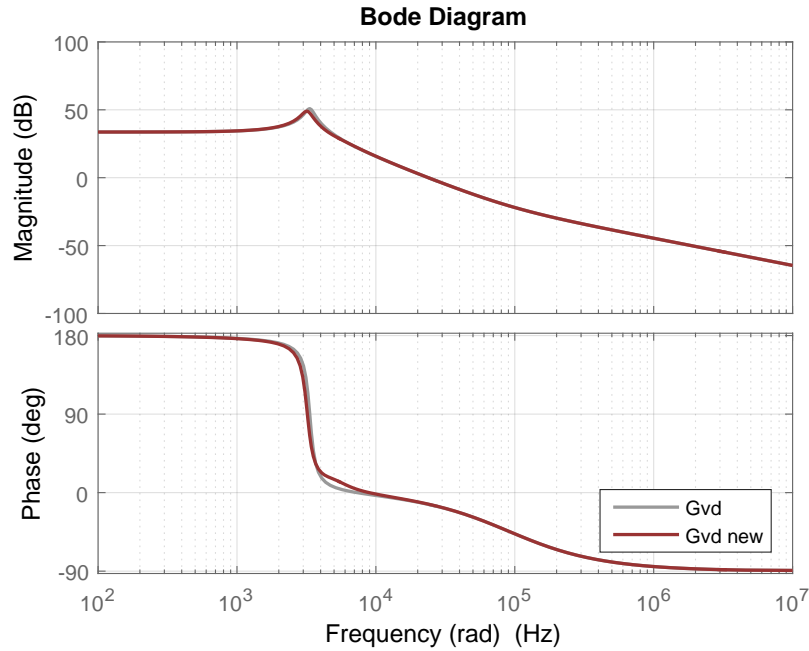


Figure 6-16: Converter transfer function with and without the EMI filter.

the capability of carrying 2 A of output current. An external inductor ($4.7 \mu\text{H}$) and three capacitors ($30 \mu\text{F}$ each) are added to the IC to create the buck converter. This IC has the ability to be switched off using the enable pin, however, as it is powering the microcontroller with a 3.3 V step down regulator, it is always kept switched on, and an external switch is added to control the 5 V output.

6.2.5 Converter for current-regulated output

To power the LEDs, a current regulated output port is designed. For this, a buck LED driver (AL8805) was used, which provides up to 1 A of current. An external resistor is added to limit the current. Also, an external inductor ($33 \mu\text{H}$) and capacitor ($1 \mu\text{F}$) are added to create the buck converter. The LED can be dimmed by decreasing the duty cycle of the PWM signal from the microcontroller. Complete schematics, layout and bill of materials for this converter are included in Appendix B.

Table 6.9: Load converter components for 12 V power stage

Component	Type	Unit Cost (\$)
Inverters		
Input Capacitors	10 μ F/50 V Ceramic Capacitors, Qty: 5	0.068
Transistors	150V/26A MOSFET (FDD390N15A), Qty:1	0.472
Snubber	3.3 k Ω (2W) Resistor Qty:1; 22 nF/100V Capacitor, Qty:1	0.155
Control IC	100 V/ 1 A Schottky diode, Qty: 1	1.76
Transformer	Current mode Flyback dc/dc controller (LTC3805), Qty: 1	1.89
Rectifier	Power Transformer (FA2900) Qty:1	
Diode	60 V/3 A Schottky diode (PMEG6030), Qty:1	0.12
Diode snubber	33 Ω (1W) Resistor, Qty:1; 240pF/100V NPO Capacitor	0.047
Output Capacitor	22 μ F/16V ceramic capacitors	0.054
Circuit Protection		
Switch	20V/4.2 A MOSFET(SMD15PL), Qty: 1	0.054
Fuse	Fuse Glass 2AG, Qty: 1; 250V/10A clip cartridge	0.18
Output Diode	30V/2A Schottky diode, Qty: 1	0.045

6.2.6 Experimental prototype and results

A prototype converter was built, using the calculated design specifications. Table 6.9 summarizes the components used in the converter.

The efficiency of the main 12 V power stage of the load converter is shown in Fig. 6-17. This efficiency does not include the microcontroller power, as this is considered part of the communication circuit.

The cost breakdown of the 12 V main power stage is provided in Table 6.9, and overall cost is given in Table 6.10. The cost breakdown of the main stage and overall load converter is shown in Fig. 6-19.

6.3 Evaluating Capacitive Isolation for Load Converter

Galvanic isolation is desired in the load converter for safety reasons. Transformers are commonly used for this purpose as they not only provide isolation but also provide any required voltage transformation (through the transformer turns ratio). However, in this case, only a modest voltage conversion ratio is needed. Consequently, there is

Table 6.10: Load converter components other than the main power stage

Component	Type	Cost (\$)
Buck IC	3 A Sync Buck Regulator	0.60
Additional R,C	8.2 and 47 $k\Omega$, resistors, 22 μ F/16 V and 0.1 μ F/ 50 V capacitors	0.059
Inductor	4.7 μ F 3 A inductor (NR6028T4R7M)	0.091
Output capacitor	10 μ F/10 V capacitors, Qty: 3	0.069
Current control		
Driver	LED driver AL8805, Qty:1	0.315
Additional R,C	0.3 Ω resistor, Qty:1; 1 μ F/16V capacitor	0.076
Inductor	33 μ H 1.45 A inductor (TYS6045330M-10)	0.144
Diode	30 V/2 A Schottky diode	0.045
Sensing		
Current	Current Monitor (ZXCT1110QW5-7), Qty:1 0.02 Ω (0.5 W) and 17.8 $k\Omega$ resistors	0.628
Voltage	10 $k\Omega$, 2.7 $k\Omega$, 3.9 $k\Omega$ and 4.7 $k\Omega$ resistors	0.0036
Logic		
Microcontroller	50 MIPS, 1.04ns PWM Resolution (DsPIC33FJ64GS406), Qty: 1	3.83
Additional R,C	8.2 $k\Omega$ resistor ; 1 μ F/16 V and 10 μ F/10 V capacitors	0.089
Regulator	3.3 V LDO (AZ1117CH-3.3), Qty:1 10 μ F/10 V capacitors, Qty:4	0.344

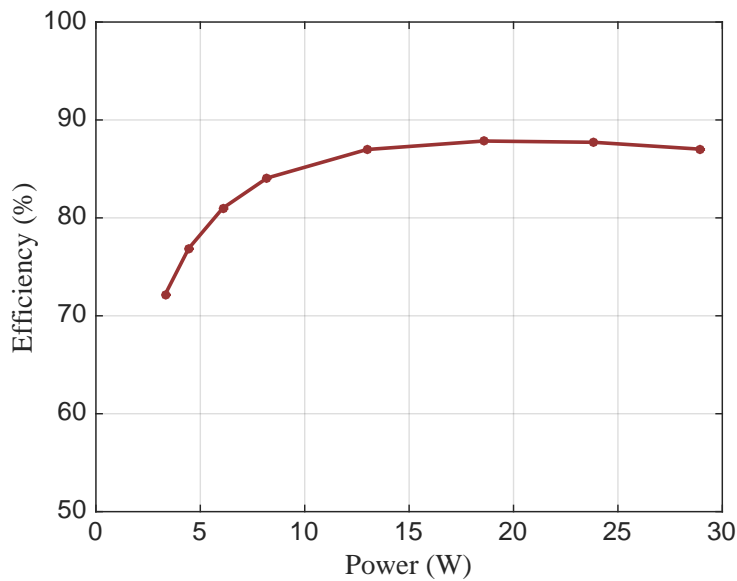


Figure 6-17: Measured efficiency vs output power of the flyback load converter.

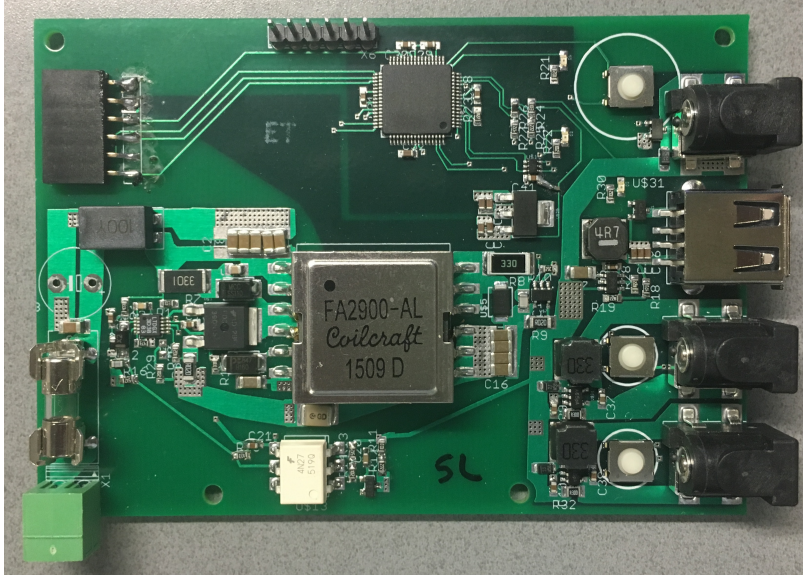
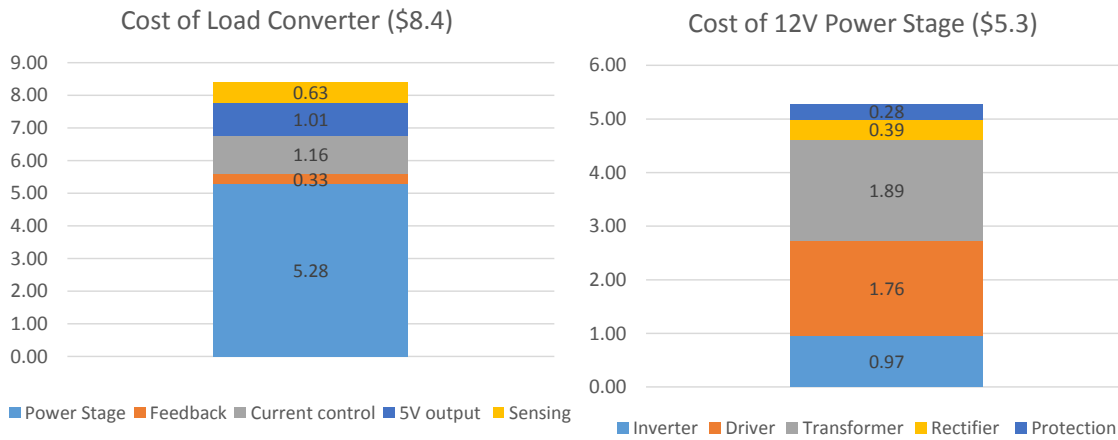


Figure 6-18: Prototype board of the load converter implemented using flyback topology.



(a) Load converter

(b) 12 V main power stage

Figure 6-19: Cost of 25 W isolated flyback converter, with 10,000 unit pricing at available distributor prices.

the possibility of realizing the desired safety isolation with capacitive techniques at lower cost and smaller size.

6.3.1 Safety capacitors

There are two types of safety capacitors:

Table 6.11: Safety capacitor ratings

Category	Rated AC Voltage	Dielectric Standing Voltage at 60 Hz	Impulse Voltage
Y1	250	1500	8000
Y2	250	1500	5000
Y3	250	1500	2500
X1	250	1500	4000
X2	250	1500	2500

- X capacitors: These are used in line-to-line applications where failure of component would not lead to danger of electric shock, as they short on failure.
- Y capacitor: These are used in line-to-ground applications where failure of component could lead to an electric shock, as they open upon failure.

For Johanson dielectrics capacitors, the values are given in Table 6.11. Both X and Y capacitors are rated for high AC voltage, dielectric withstanding voltage and impulse voltage (an impulse voltage is applied based on IEC60384-14 and IEC 60950 standard), however, Y capacitors are chosen for this application due to their property of opening under fault.

In order for the product to meet safety requirements, it has to pass the following tests outlined in IEC 60950:

- Electrical strength: The dielectric strength test ensures that the electrical strength of the insulating materials is adequate.
- Ground continuity: The ground continuity test ensures that in case of an earth fault, a person touching the conductive parts that are exposed is not hurt.
- Touch current: The insulation resistance test determines how effective the insulation is in reducing leakage current. This ensures that if a person touches an exposed conductive part, the current flowing through the body is within the safety limit.

For the load converter, electrical strength and touch current need to be considered

during the circuit design process. The continuity test will be considered at a later time, during the enclosure design process of the load PMU.

Electrical strength

The electrical strength test applies an over voltage to the circuit to test its isolation. According to the PoE standard, the circuit should be able to withstand a steady state high voltage for at least a minute, as well as repetitive high voltage surges [86]. According to IEC 60950, $1500 V_{rms}$ (50 or 60 Hz) for 60 s or 2250 V dc voltage can be applied across the isolation boundary that is being tested.

An isolation transformer has a primary and secondary winding wound on the same core, with a separation between the two windings to provide creepage and clearance. This separation allows the transformer to meet the electrical strength test. On the other hand, capacitive isolation using Y-rated capacitors is sufficient to meet the electrical strength requirements, as shown in table 6.11.

Touch current

When touching an accessible conductive part of a device, current can flow through the body. This current can be lethal if it exceeds a certain value. In this application, distribution voltage is kept low and is dc, hence avoiding high touch current. According to IEC 60950, the maximum touch current is 0.25 mA when the circuit is not connected to protective earth, and 3.5 mA when the circuit is connected to protective earth [87].

An ideal transformer rejects a common-mode signal, as it does not create any flux in the core. Hence, even if there is a high floating voltage at the output of the transformer, and a person touches it, he/she will be safe. This is because even though a path from the line to ground is formed, the common-mode current does not pass through. However, a real transformer might have parasitic capacitance between primary and secondary windings, thus allowing current to pass through. Hence, this capacitance needs to be minimized to further reduce the feed-through current.

Capacitive isolation works on the principle that the common mode noise is a

low frequency noise, and the impedance of the capacitor is inversely proportional to frequency. Hence, for low frequency noise, it provides a high current path, and for a high frequency signal it provides a low impedance path. For ac systems (50 or 60 Hz), the touch current requirement limits the highest capacitance value to a few nano Farads. Hence, most Y capacitors are rated for a maximum of 4.7 nF. However, in a purely dc system, with low voltage, higher capacitance can be used.

6.3.2 Design of a capacitively isolated load converter

A capacitively isolated series resonant converter, as shown in Fig. 6-20, was developed and tested to explore the possible use of capacitive isolation in this application. The inversion stage is composed of a half-bridge inverter (S_1, S_2), the transformation stage is composed of inductors (L_{r1}, L_{r2}), and capacitors (C_{r1}, C_{r2}), and the rectification stage is composed of a full-bridge diode rectifier (Q_1, Q_2, Q_3 and Q_4).

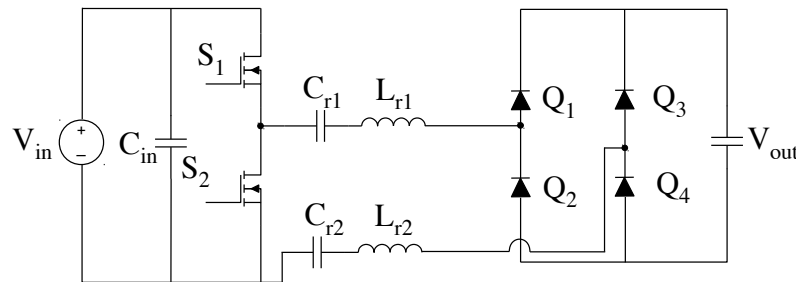


Figure 6-20: Capacitively isolated series resonant converter.

Analysis

In order to design the circuit, fundamental harmonic approximation (FHA) is used. The inverter voltage is a square pulse with an amplitude of V_{in} . The fundamental component of this is a sinusoidal wave with an amplitude of $2V_{in}/\pi$. As the two inductors ($L_{r1} = L_{r2}$) are in series, the inductance doubles. The two capacitors ($C_{r1} = C_{r2}$) are in series and result in an effective capacitance of half the value. The diode rectifier is approximately modeled as a resistor with a value of ($R_e = 8R_{out}/\pi^2$), where R_{out} is the output load resistance. The circuit created by using FHA is shown

Table 6.12: Capacitively isolated converter specifications

Parameter	Value
V_{in} (V)	28
V_{out} (V)	12
P_{out} (W)	25

in Fig. 6-21. The current in the network is given by Equation (6.20).

$$i_s = \frac{V_{s1}}{\sqrt{(X_{Lr} + X_{Cr})^2 + R_e^2}} \angle -\tan^{-1}\left(\frac{X_{Lr} - X_{Cr}}{R_e}\right) \quad (6.20)$$

where V_{s1} is the amplitude of the fundamental sinusoidal component of the square pulse ($2V_{in}/\pi$). X_{Lr} is the impedance of the effective inductor at the switching frequency (ω_s) given as ($X_{Lr} = 2\omega_s L_{r1}$) because $X_{L,r1} = X_{L,r2}$. X_{Cr} is the impedance of the effective capacitor given as $X_{Cr} = 2/(\omega_s C_{r1})$ because $X_{C,r1} = X_{C,r2}$. At resonance ($\omega_s = \omega_r$), reactance of the network is equal to zero, hence, the current is determined by the load resistance and is given in Equation (6.21).

$$i_{s,rmsatres} = \frac{V_{s1}}{R_e} = \frac{2V_{in}}{\sqrt{2}\left(\frac{8R_{out}}{\pi^2}\right)} \quad (6.21)$$

If this was a purely lossless network, it could operate at resonance (slightly above for ZVS) with 24 V input voltage and 12 V output voltage as the gain of the inverter and rectifier (M_{conv,ω_o}) is 0.5. However, due to the $R_{ds,on}$ of the MOSFET, ESR of the inductor and capacitor, and forward voltage drop of the diodes, the output voltage is lower. This voltage drop of the converter is approximately equal to:

$$v_{drop} \approx i_{s,rms}(R_{dson} + ESR_{Cr} + \omega L_r/Q_L) + 2v_{f,diode}. \quad (6.22)$$

For the converter, there are two options: either to operate with a full bridge rectifier ($M_{conv,\omega_o} = 1$) and then drop the voltage on the resonant tank or to operate with a slightly higher input voltage. For a more efficient operation the latter approach is chosen. The converter specifications are given in Table 6.12.

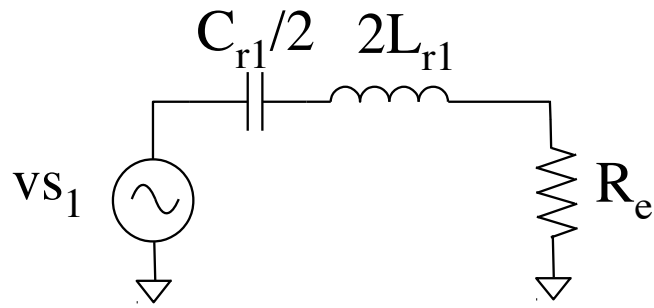


Figure 6-21: Fundamental harmonic approximation of the series resonant converter.

Selection of the resonant tank components

Often, the series resonant converter is designed with a high Q tank to keep the switching frequency variation low. This frequency is varied to regulate the output voltage with variation in input voltage. In the design of the capacitively isolated series resonant converter, not only is low inductance preferred to reduce the losses in the inductor, but also low capacitance is required to decrease the cost of the capacitors. However, both these objectives can not be met simultaneously. For a particular resonant frequency, decreasing the inductance increases the capacitance ($X_{Lr,\omega_o} = X_{Cr,\omega_o}$), and hence a trade-off between loss and tank Q needs to be made.

Inductor Selection: The inductor value is chosen to be small enough such that the inductor is printable on the PCB board without resulting in high losses. Using air core printed PCB inductors, the cost of the inductor can be nearly eliminated. In order to attain high efficiency, 4 oz copper was used for the the inductor. To determine the price increase of using 4 oz compared to 1 oz, quotes were solicited from various pcb manufacturers. It was observed that the magnitude of price increase greatly depends on the expertise of the pcb manufacturer. There was less than a \$0.26 increase in price for a 2 layer 4 oz ($3 \times 3 \text{ in}^2$) board compared to a 1 oz board. The use of buried or blind vias was avoided as it increases the cost significantly.

Type of capacitors chosen: Ceramic capacitors are commonly used due to their high energy density. The dielectrics of these capacitors determine their loss. NPO or COG dielectrics are preferred over X7R due to lower loss and due to stability

of value. However, Y-rated COG capacitors are expensive and their size is limited to a maximum of 1 nF. In order to get 30 nF, 30 capacitors need to be placed in parallel, which is very costly. Film capacitors (still Y type) were used as they are less expensive and have higher capacitance values available.

Selection of frequency: In order to reduce the inductance required, high frequency is preferred. The size of the inductance is determined by the lowest frequency at full load. To regulate output voltage with decreasing load values, the frequency is increased to decrease the gain. For this setup, the highest frequency was limited to 2.5 MHz, which was the highest frequency the gate driver could switch at.

Frequency was chosen such that losses incurred could be minimized. The loss of the converter is estimated in Equation (6.23)

$$P_{loss} = i_{s,rms}^2 (R_{dson} + ESR_{Cr} + \frac{\omega_{sw} L_r}{Q_L}) + 4i_{s,av} v_{f,diode} + 2Q_g V_g f_{sw}, \quad (6.23)$$

where R_{dson} is the on-state resistance of the transistor, ESR_{Cr} is the equivalent series resistance of the capacitor, L_r is the resonant inductor, Q_L is the inductor quality factor, $v_{f,diode}$ is the forward voltage of the diode, Q_g is the gate charge of the transistor, V_g is the gate voltage and f_{sw} is the switching frequency. Using $Q_L = 100$ and peak load, the efficiency of the converter was plotted against varying capacitor values (C_r), as shown in Fig. 6-22. Using 1.5 Mhz, the efficiency versus variation in Q_L was plotted in Fig. 6-23. As seen from the graph (Fig. 6-23), Q_L of the inductor higher than 100 was preferred.

6.3.3 Experimental results of the capacitively isolated load converter

The converter is designed considering the converter specifications provided in Table 6.12. To meet these specifications, 40 V Vishay switches (SIR836D) and 30 V NXP diodes (PMEG3050) were selected. In order to attain the highest efficiency, the highest capacitance was chosen (30 nF). The capacitance required was achieved by

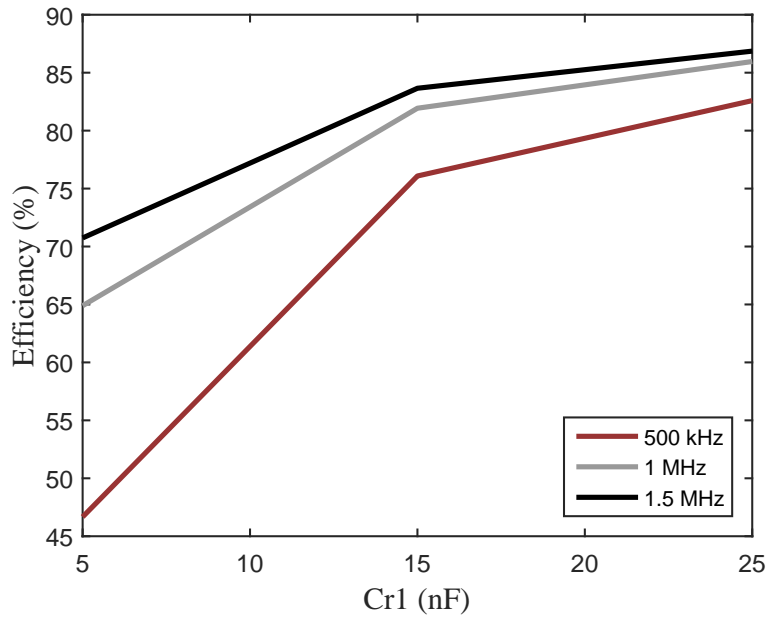


Figure 6-22: Efficiency of the capacitively isolated converter with respect to the chosen resonant capacitor at varying frequencies with $Q_L=100$.

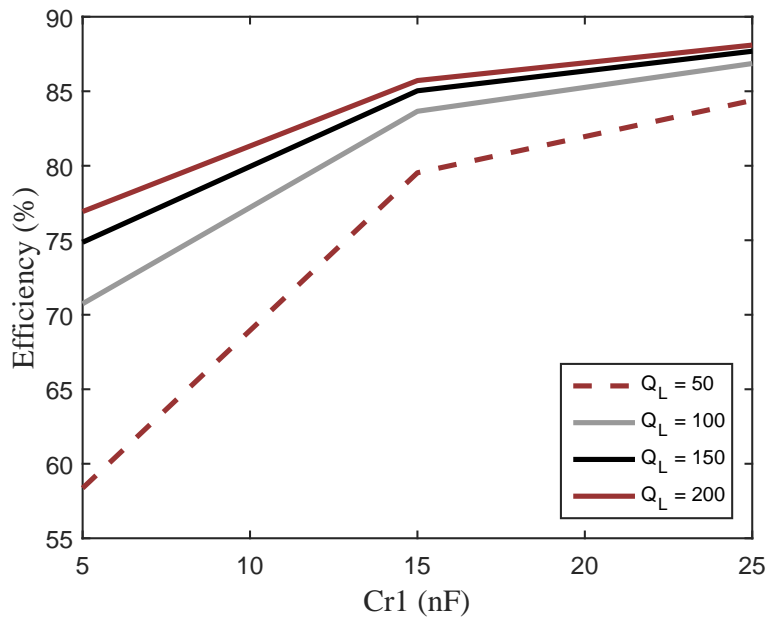
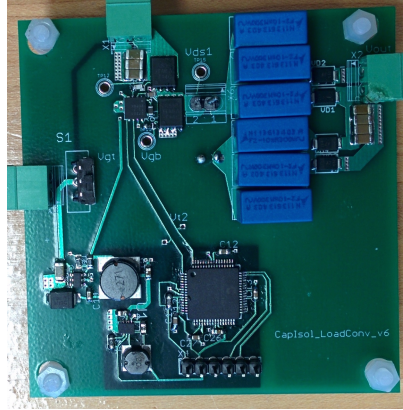
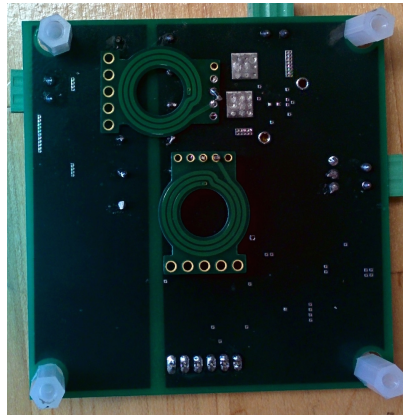


Figure 6-23: Efficiency of the capacitively isolated converter with respect to the chosen resonant capacitor with varying component Q of the inductor plotted for $f_{sw} = 1.5$ MHz.



(a) Top side



(b) Bottom side

Figure 6-24: Picture of the (a) top side and (b) bottom side of the prototype capacitively isolated board.

placing three 10 nF film capacitors in parallel. However, their measured capacitance was 8.8 nF each. A spiral aircore pcb inductor (6-turn, 2 layer and 4 oz copper) of 0.6 nH was used. This was sourced from coilcraft’s planar magnetics kit.

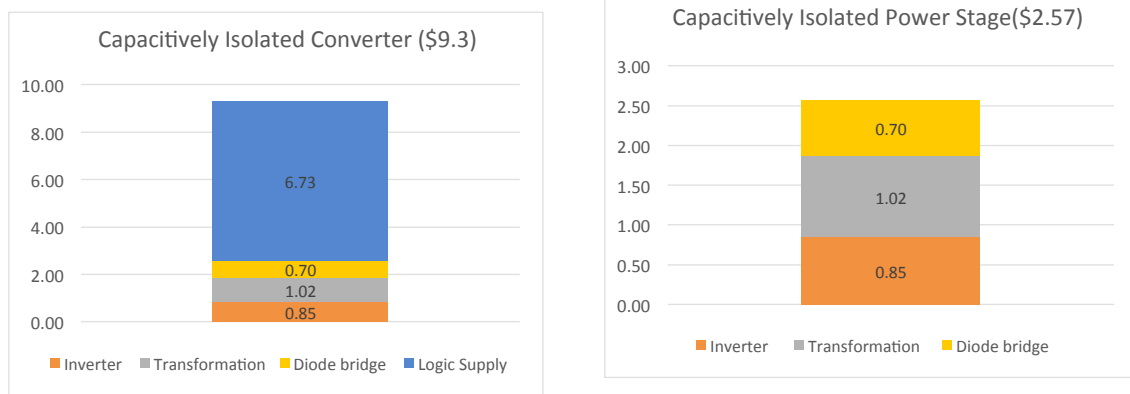
An estimate of the inductor’s ESR was made using physical measurements of the geometry of the inductor. This was estimated as $50\text{ m}\Omega$. The ESR of an individual 10 nF capacitor was estimated by modifying the setup described by Hanson et. al [88], which was calculated to be $0.16\ \Omega$. Three capacitors were placed in parallel to reduce the effective resistance.

The prototype board of the converter is shown in Fig 6-24, and the components used are shown in table 6.13.

The switching waveforms for full load (25 W) are shown in Fig. 6-26, and for

Table 6.13: Components used in the experimental prototype of the capacitively isolated converter

Component	Type	Cost (/ \$)
Inverter		
Input Capacitors	10 μ F/50 V ceramic capacitors, Qty: 4	0.068
Gate Driver	120V/3A High and low side driver (UCC27201D), Qty: 1	1.31
Transistors	40V Trenchfet power MOSFET (SIR836DP), Qty: 2	0.248
Transformation		
Inductors	6 turn, 2 layer, 4oz copper pcb inductors (Coilcraft's Kit C356)	—
Capacitors	Y2 0.01 μ F Film Capacitor (B32021A3103M289), Qty: 6	0.17
Rectification		
Diodes	30-V/4-A Schottky diode (PMEG3050), Qty:4	
Capacitors	10 μ F/25 V Ceramic Capacitors, Qty: 4	0.02
Logic		
Controller	Microcontroller (DsPIC33FJ64GS406) and other R and C	3.9
12 V	Buck Converter (LMR16006) and other L, R and C	1.71
3.3 V	Buck Converter (TPS62177) and other L, R and C	0.948



(a) Capacitively isolated load converter

(b) Power stage of capacitively isolated load converter

Figure 6-25: Cost of capacitively isolated load converter, based on 10,000 units at published distributor costs.

light load (2.5 W) are shown in Fig. 6-27. Frequency control is used when the load decreases. However, at 50 Ω and higher load resistances, asymmetrical duty cycle control was used, as the frequency required was greater than 2.5 MHz (the maximum frequency). The variation in frequency with respect to load is provided in Fig. 6-29. During duty cycle control, a 0.7 to 0.75 duty cycle is used as the load decreases.

The estimated loss is given in figure 6-28. As seen from the figure, the diode loss dominates, followed by losses from the capacitor and inductor, respectively. The

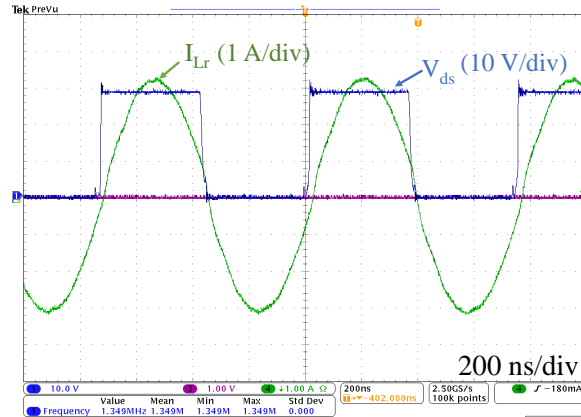


Figure 6-26: Switching waveforms of the Inductor current and output voltage of the inverter at full load.

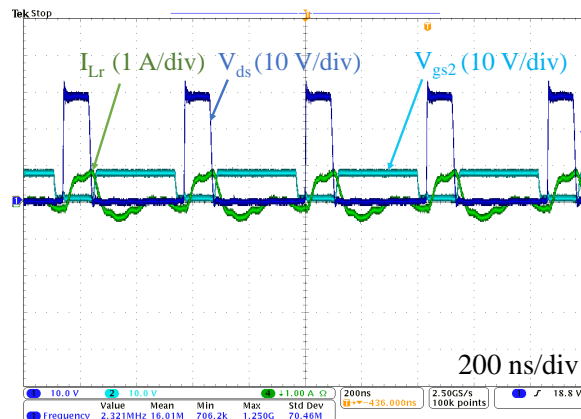


Figure 6-27: Switching waveforms of the Inductor current, output voltage of the inverter and gate signal of bottom switch at 2.5 W of output power.

diode loss can be decreased by using synchronous rectification, however, this requires additional gate drivers. The increased efficiency does not justify the resulting increase in cost and complexity. The experimental efficiency of the converter is shown in Fig. 6-30. This does not include the power to drive the microcontroller. Peak efficiency of 90.2 % at around 11 W of output power was achieved.

Cost of the capacitively isolated load converter

The cost of the power stage of the capacitively isolated load converter was calculated as \$2.57 and the cost of the entire converter was calculated as \$9.3. Here, the logic supply and microcontroller have not been optimized, hence, the converter cost can

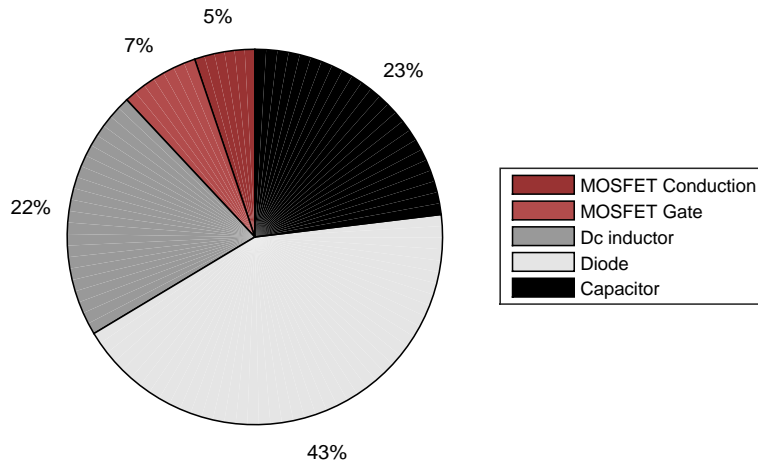


Figure 6-28: Estimated loss break-down of the capacitively isolated converter.

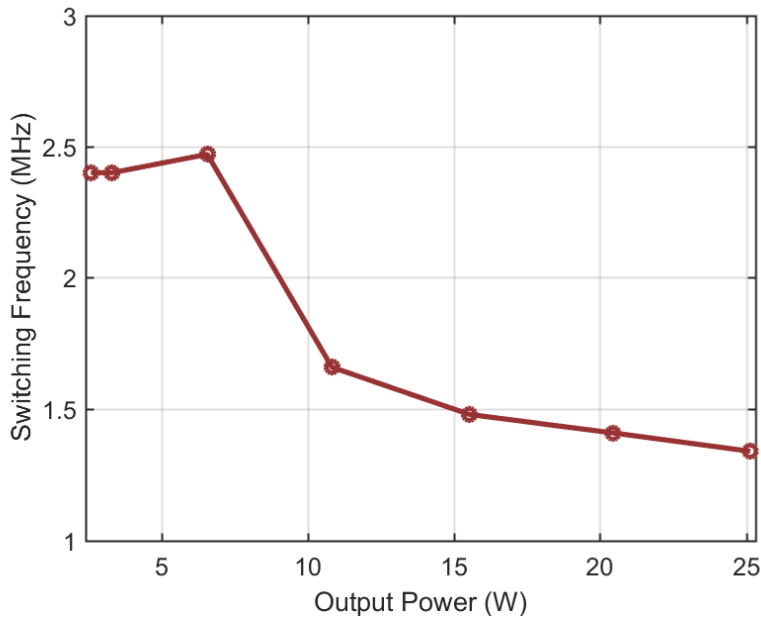


Figure 6-29: Frequency control and asymmetrical duty cycle control used to control the converter as load varies.

be further reduced. The major loss of the converter was in the diodes. By using synchronous rectification, this loss can be reduced, however, this will significantly increase the cost of the converter as two half bridge drivers and a signal isolator

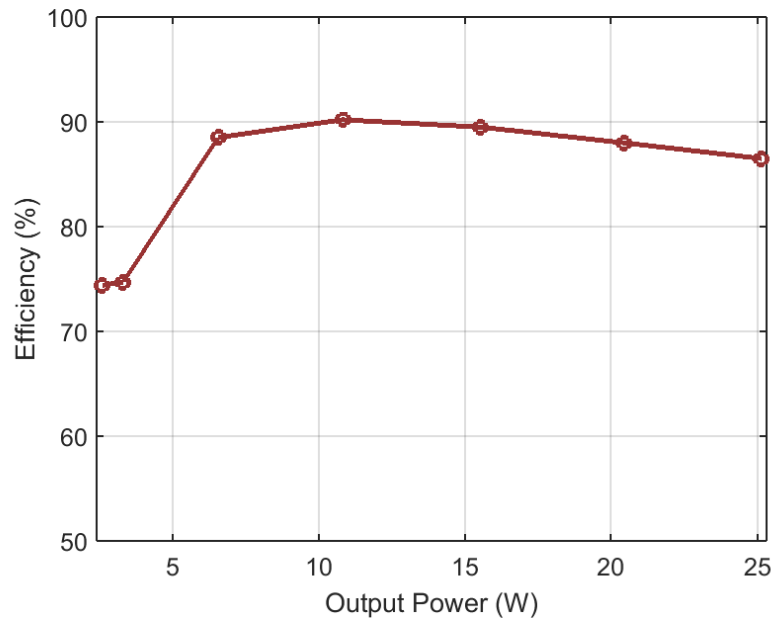


Figure 6-30: Experimental efficiency of the converter as load varies from 2.5 W to 25 W with 28 V input voltage 12 V output voltage.

will be required. Also, the control of the full-bridge synchronous rectifier will be challenging.

6.4 Conclusion

This chapter details the design of the low-cost source and load converters. With a low cost of \$3.94 for the source converter power stage, the peak efficiency achievable was 96.6%. For the flyback load converter, the power stage cost was \$5.3 with a peak efficiency of 87.8% . Although low converter cost was achieved, the lower efficiency affects the system cost (this will further be evaluated in the next chapter). Also, the possible use of capacitive isolation was explored. A low power-stage cost was attainable, however, the efficiency achievable without synchronous rectification was low. Hence, the flyback converter was selected as the low-cost load converter for this application.

Chapter 7

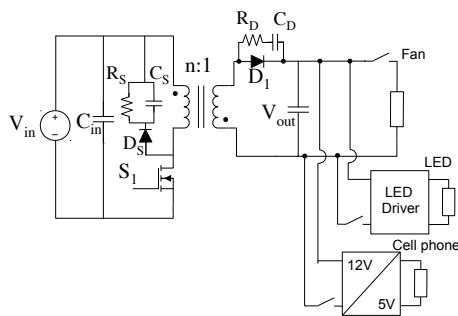
Designing Converters to Reduce System Cost

Power converters play a major role in determining the total system cost of many applications, such as distributed energy and electricity backup systems. However, detailed analysis of the impact of converter efficiency variation with load on total system cost, with the load profile taken into consideration, has rarely been discussed in literature. Several works have investigated the cost of individual components that affect the power converter cost [89], [90]. Moreover, the optimization of reliability versus cost has made significant progress [91], [92]. While some works compare efficiency and cost of different system topologies [93], works that model and assess the total system cost impact of converters are still rare [94]. A sophisticated design methodology, which determines the cost and efficiency trade-off of power converters, will enable us to better evaluate new topologies and to decrease the total system cost.

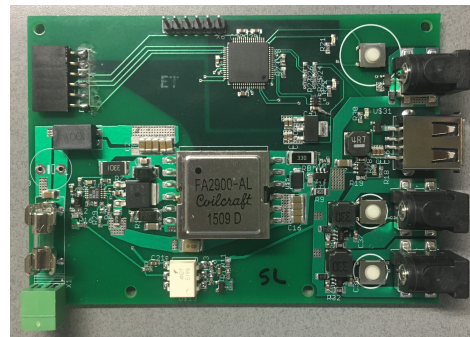
Power converters are usually designed to meet objectives, such as optimizing efficiency or reducing converter cost, without considering the context of the impact of the converter on overall system performance and system-level cost. For a high-efficiency application, the design emphasizes on increasing the peak efficiency and/or a source-related weighted efficiency such as California Energy Commission, or "CEC efficiency" [95], rather than optimizing the efficiency curve in the context of an overall power system development. For low-cost applications, design often emphasizes the initial

or "first" cost of the converter, rather than the initial or lifetime cost of the system. Hence, power converters with low component count are often utilized, minimizing the converter's initial cost, but not necessarily the system's initial or lifetime cost. The discrepancy between these two approaches arises because no framework exists to assess the design trade-off between efficiency and cost over the lifetime of an application. These design decisions have prevailed in part because there have been few opportunities to co-design the power converters and the entire application. However, creating new power systems (e.g., dedicated microgrids, power distribution systems, etc.), presents an opportunity to truly co-design and co-optimize the power system and the power converters.

In this chapter, the optimization of converters to meet system-level goals is discussed. A weighted efficiency metric is proposed, which is derived from the percentage of energy processed by the converter at each power level, based on system-level studies. This helps design power converters which will minimize the total energy loss in the system. This is followed by a method to trade-off efficiency and cost of power converters to decrease overall system cost. This helps in justifying the increased cost of the converter, and in selecting the power converter that achieves the lowest system cost. This methodology is demonstrated using two types of load converters. However, this can be extended to evaluate the source converter design for the system under investigation, or to other energy applications entirely.

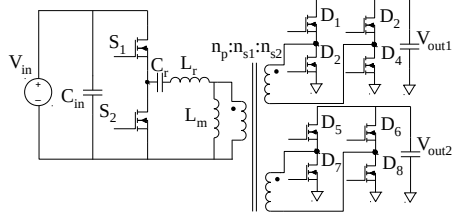


(a) Schematic of the flyback converter

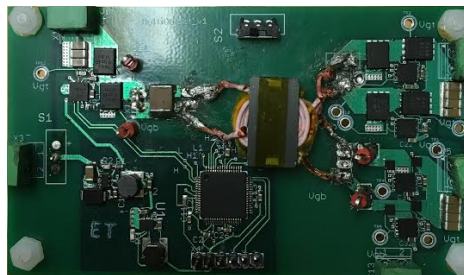


(b) Prototype of the flyback converter

Figure 7-1: Flyback converter.



(a) Schematic of the first version of resonant converter



(b) Prototype of the first version of the resonant converter

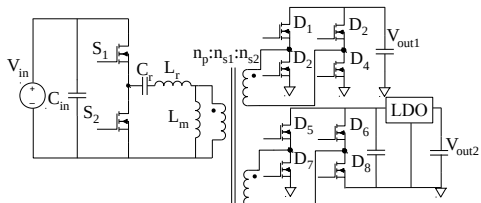
Figure 7-2: Multi-output resonant converter with litz wire transformer.

7.1 Converters Evaluated

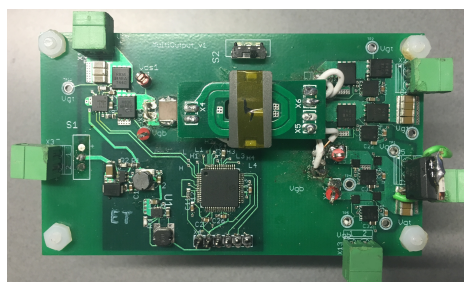
Two types of load converters, one hard-switched PWM and two ZVS soft-switched resonant converters, were built to demonstrate the proposed methodology. For the hard switched converter, the flyback topology was selected. Two versions of the multi-output resonant converter were built: version 1 incorporated a transformer with litz wire winding and version 2 incorporated a transformer with printed circuit board winding.

7.1.1 Flyback converter

The flyback converter is one of the simplest and most-common power conversion topologies for low-power isolated conversion. It requires very few components; a simple flyback power stage consists of a switch, a transformer and a diode. Owing to



(a) Schematic of the second version of the resonant resonant



(b) Prototype of the second version of the resonant converter

Figure 7-3: Multi-output resonant converter with PCB transformer.

the small component count it can have quite low first cost. Despite the advantage of simplicity, there are some drawbacks: the converter suffers from high device stresses, requires a gapped energy storage transformer transformer and is relatively large in volume. The schematic and prototype board of the flyback converter built are shown in Fig. 7-1. The flyback stage is followed by dedicated post-regulators to manage powering of cell-phones and LEDs, in addition to providing direct output for loads, such as fans. In this analysis only the 12 V main power stage will be considered. The components used for the power stage of the converter are detailed in Chapter 6 and in Appendix B, and the cost of the power stage is provided in Fig. 7-7.

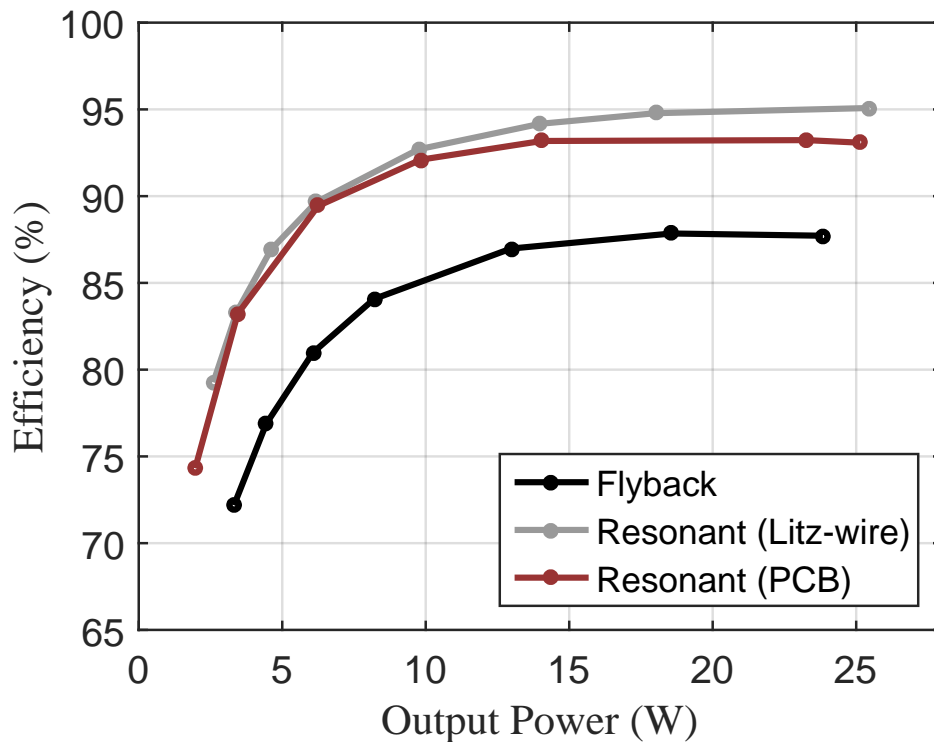


Figure 7-4: Efficiency vs output power of the three converters built.

7.1.2 Multi-output resonant converter

Two variations of a multi-output LLC resonant converter, as shown in Fig. 7-2 and Fig. 7-3, have been developed with the goal of directly supplying both 12V and 5V outputs at high efficiency. The switching frequency gives us control over the voltage

levels of both outputs, while the phase shift on the synchronous rectifier allows us to adjust individual outputs. Due to cross-regulation, both frequency control and phase shifting are necessary for an effective output voltage control (Full details of these designs, including complete schematics, magnetics designs, bill of materials, PCB layout and control code can be found in Appendix C).

The first version of the resonant converter utilizes a transformer with litz-wire winding and the second version utilizes a transformer with printed circuit board winding. For these converters, the two outputs are at 12V and 5V, requiring a minimum transformer turns ratio of 12:12:5 if only the transformer is used to provide the voltage conversion. An efficient design of the transformer can be challenging if a large number of turns are used to realize an exact turns ratio, leading to higher copper requirement. Hence, for these transformers, a turns ratio of 2:2:1 is used with phase shift control to step the output voltage down from 6V to 5V in the first variation (Fig. C-1) and using an LDO post regulator to step down the voltage in the second variation (Fig. 7-3a). The transformer leakage inductance was used as the resonant inductor (L_r) and the leakage was estimated using the transformer's cantilever model [96].

Version 1: transformer with litz wire winding

Table 7.2 provides details of the components used in the 12 V power stage of the prototype converter. The cost of the main power stage is summarized in Fig. 7-7. The transformer is composed of an EELP18 core of N49 material with a gap resulting in a magnetizing inductance of 4.87 μH . For the primary winding, 4 turns of 48 AWG/450 strands litz wire was used. For the secondary 12 V and 5V windings, 4 and 2 turns of the same litz wire were used, respectively. The transformer was not fully packed, so the copper loss can further be reduced. The effective inductance (L_r) was around 200 nH and the summary of measured transformer parameters is provided in Table 7.1. Agilent's 4395A impedance analyzer, Tektronix MSO4104 Oscilloscope and P6139a voltage probes were used for these measurements. A capacitance (C_r) of 200nF was used and the converter was operated, almost at resonance, at 800kHz.

Table 7.1: Summary of transformer parameter measurements for cantilever model

Parameter	Approximate Measured Value (Litz wire Transformer)	Approximate Measured Value (PCB Transformer)
L_{11}	4.87 μH	3.35 μH
l_{12}	200 $n\text{H}$	100 $n\text{H}$
l_{13}	11.37 μH	726 $n\text{H}$
l_{23}	465 $n\text{H}$	358 $n\text{H}$
n_2	1	1
n_3	0.5	0.5

Phase shift between the bridge legs of the rectifier was used to drop the voltage from 6 V to 5 V, at the second output. The control signal for the 12 V full-bridge rectifier is in phase with the control signal for the inverter bridge. One of the legs of the 5V rectifier is in phase with the inverter bridge, while the second leg is phase-shifted to decrease the output voltage. The phase shift was decreased from 12.3% to 1.8% at full load.

Version 2: transformer with PCB winding

In this version, to reduce cost as compared to the litz wire, the transformer winding was printed on a 4 oz copper, 6 layer circuit board. The cost of using 4 oz copper as compared to 1 oz copper is slightly higher, but 4oz copper yields higher efficiency. The details of the PCB windings to realize the multi-port transformer is presented in Appendix C. The increased cost per board has been taken in to account in the cost of the transformer in Table 7.2. In this prototype, phase-shift control was not very effective due to the leakage inductance L_{13} (from cantilever model) being very small, hence, an LDO was added to drop the voltage from 6V to 5V. The transformer core had a gap resulting in a magnetizing inductance of 3.35 μH . It had an effective inductance of 150 $n\text{H}$, which was utilized as the resonant inductor (L_r) and had a 200 $n\text{F}$ capacitance (C_r). This converter was operated at around 915 kHz.

Table 7.2: Components of the 12 V power stage of the resonant converters

Component	Type	Cost (\$)
Inverter		
Input Capacitors	10 μ F/50 V ceramic capacitors, Qty: 4	0.068
Gate Drivers	120V/3A High and low side driver (UCC27201D), Qty: 1	1.31
Transistors	40V/21A TrenchFET (SIR836DP), Qty: 2	0.248
Transformation		
Capacitor	0.1 μ F/50 V ceramic COG capacitor Qty: 2	0.119
Transformer (Litz wire)	EELP 18, N49 core, Primary: 4 turn, 48 AWG/450 strands litz wire. Secondary 1: 4 turn, 48 AWG/450 strands, Secondary 2: 2 turn, 48 AWG/450 Strands	4.50
Transformer (PCB)	EILP 18, N49 core with clamp and 4 oz copper PCB Primary and Secondary 1: 4 turns, Secondary 2: 2 turns	0.708
Rectification		
Mosfets	20V/20A TrenchFET (SIR484DP), Qty:4	0.302
	100V/1.2 A Half bridge gate driver, Qty: 2,	1.582
Gate Drivers	Bootstrap capacitor: 0.1 μ F/50V	0.007
	Bypass capacitor: 10 μ F/25 V	0.067
Digital Isolator	150 Mbps 2.5kV/ μ s dual channel isolator, Qty:1	0.833
Output Capacitors	10 μ F /50 V ceramic capacitors, Qty: 4	0.095

7.2 Determining the Weighted Efficiency of a Converter Resulting in Minimum Energy Loss

In this section, a weighted efficiency metric is proposed, which is based on the actual percentage of energy processed by the converter at each power level during a year. To determine the converter efficiency profile that would result in minimum energy loss, first the annual load profile of the converter is determined. From this, the fraction of time the system spends at each output power level in a year is found, then the fraction of output energy drawn at each power level is calculated. Combining this histogram with the efficiency versus output power curve, the weighted efficiency of the converter can be determined.

7.2.1 Annual load profile

The estimation of the annual load profile takes into account the loads, the variation of each load's power consumption, and the duration each load will be used in a year.

This system consists of four loads - an indoor light bulb (3 W), an outdoor light bulb (3 W), a fan (15 W), and a cell phone (2.5 W). Each load's power consumption is modelled considering product and manufacturing variations. The usage duration of each load is derived from user information collected during interviews, along with irradiance and temperature data.

In this model, a light is switched on during times when it is dark outside and people are awake. To determine the ambient light, solar irradiation data from National Renewable Energy Laboratory (NREL) for the location of choice (Jamshedpur, India) was used [67]. The interviews conducted during a field trial (details provided in Appendix D) were used to assess when people are awake and when they are likely to use indoor or outdoor light bulbs. These two were overlapped to determine the amount of time light bulbs are likely to be switched on during each hour of the day in the year. To determine the load profile of the fan, user behaviour information, and outside temperature data was used. The fan is switched on when the temperature is high outside (more than 31° C). As the fan is indoors, the correlation between indoor temperature and usage of the fan will be higher. Cellphone usage is harder to predict as it is based on the number of phones per household. During field interviews, it was found that the number of phones varies and is dependent on the number of people in the house. In this model, one phone is charged every day. The time the phone starts charging can vary, however, the phone is usually charged for at least three hours per day.

Using the plot of output power (load profile that was calculated) as a function of time, the histogram of the fraction of time the system spends at each power level is calculated. Using this information, the percentage of energy consumed at each power level is then calculated, as shown in Fig. 7-6.

7.2.2 Weighted efficiency

A power converter's efficiency curve is a fundamental indicator of its performance. Many well-known efficiency metrics are derived from the efficiency curve, for example, the CEC efficiency is the weighted average of the efficiencies at six power levels

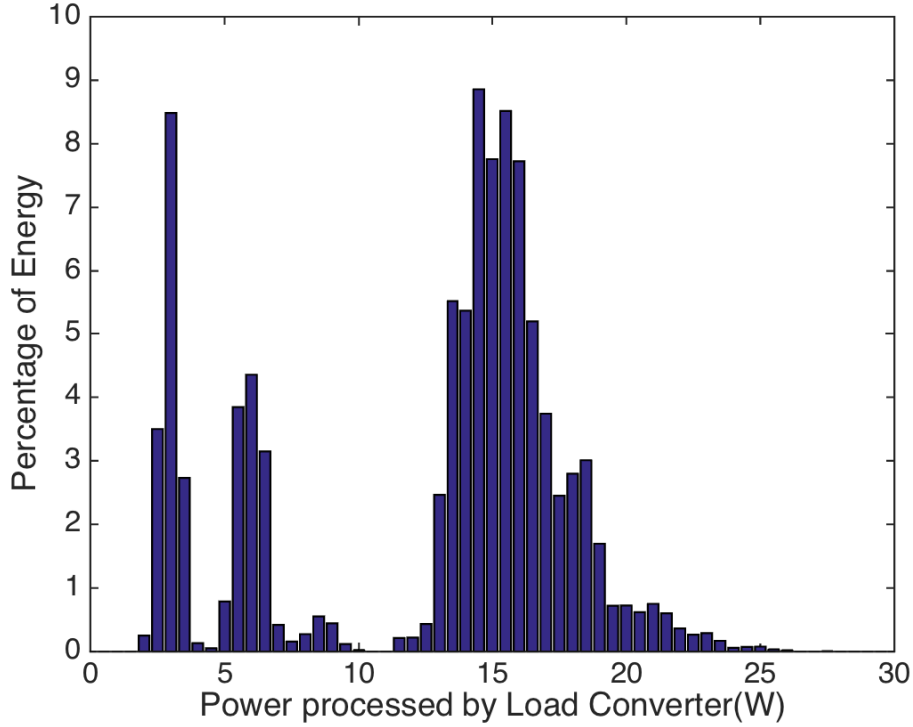


Figure 7-5: Percentage of energy processed by the load converter including variation in each load’s power consumption.

($\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}$). The CEC efficiency gives more weight to high loads, however, the load profile considered in this thesis is dominated by light-load and mid-load usage. A metric for this system is derived by removing each load variation (e.g., an LED light consuming 3.1 W is considered to be consuming 3 W) and aggregating consecutive power level bins with low percentages of energy output, as shown in Fig. 7-6. The resulting weighted efficiency metric is shown in Equation 7.1. Using these metrics, the weighted efficiency of the three converters is calculated, as shown in Table 7.3

$$\eta_{energy} = 0.11\eta_{12\%} + 0.24\eta_{24\%} + 0.03\eta_{34\%} + 0.48\eta_{60\%} + 0.09\eta_{70\%} + 0.04\eta_{84\%} + 0.01\eta_{94\%} \quad (7.1)$$

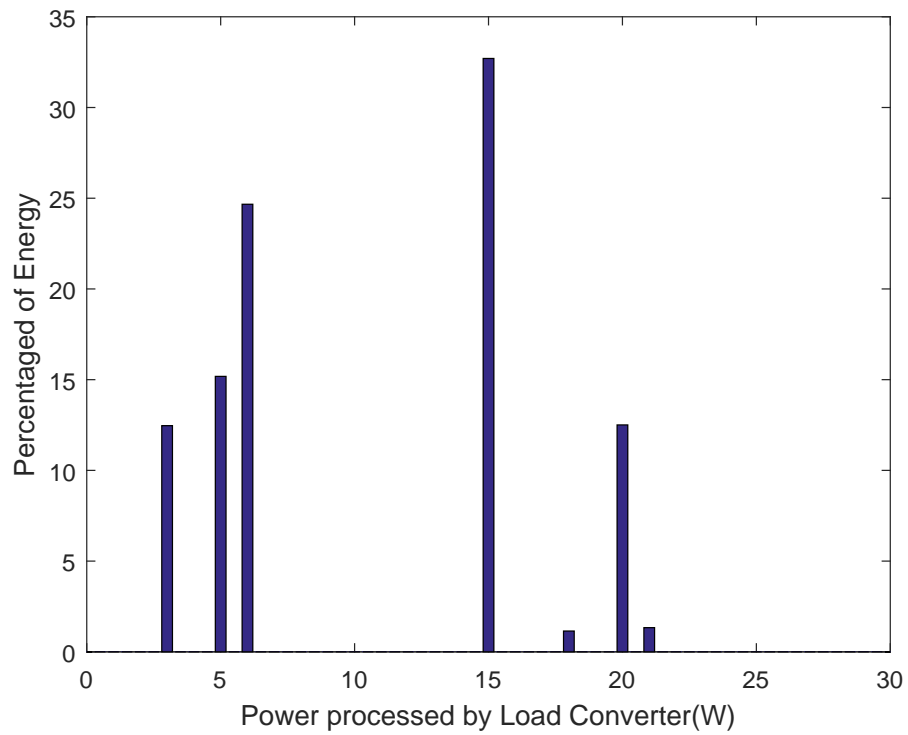


Figure 7-6: Percentage of energy processed by the load converter, assuming no variation in each load's power consumption.

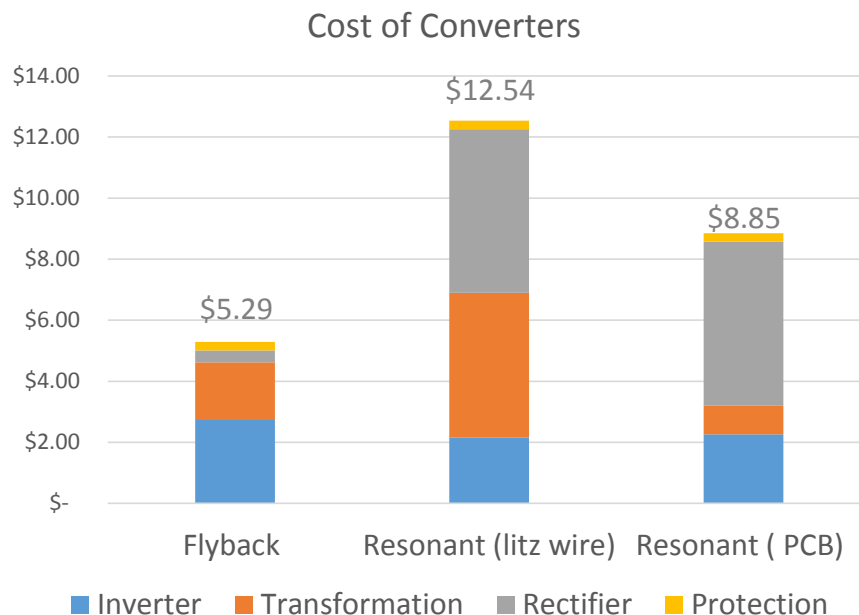


Figure 7-7: Cost of the 12 V power stage of each of the three converters.

Table 7.3: Weighted efficiency metric for three converters

Converter	η_{energy}
Flyback	85.82%
Resonant (Litz wire)	93.17%
Resonant (PCB)	91.96%

7.3 Determining the Cost of Efficiency of the Power Converters

To calculate whether the increased efficiency of the converter justifies the increased cost, a system-level simulation was performed. This involved determining the initial and a 15-year lifetime cost of the system for each of the three converters built. A system having five load converters, as illustrated in Fig. 7-9, is modelled taking all the major losses into consideration (i.e., charge controller, source converter, battery charging/ discharging, distribution and load converter loss). The following subsections describe the steps required to calculate the total system cost and these steps are summarized in the flowchart presented in Fig. 7-8. The code used to simulate

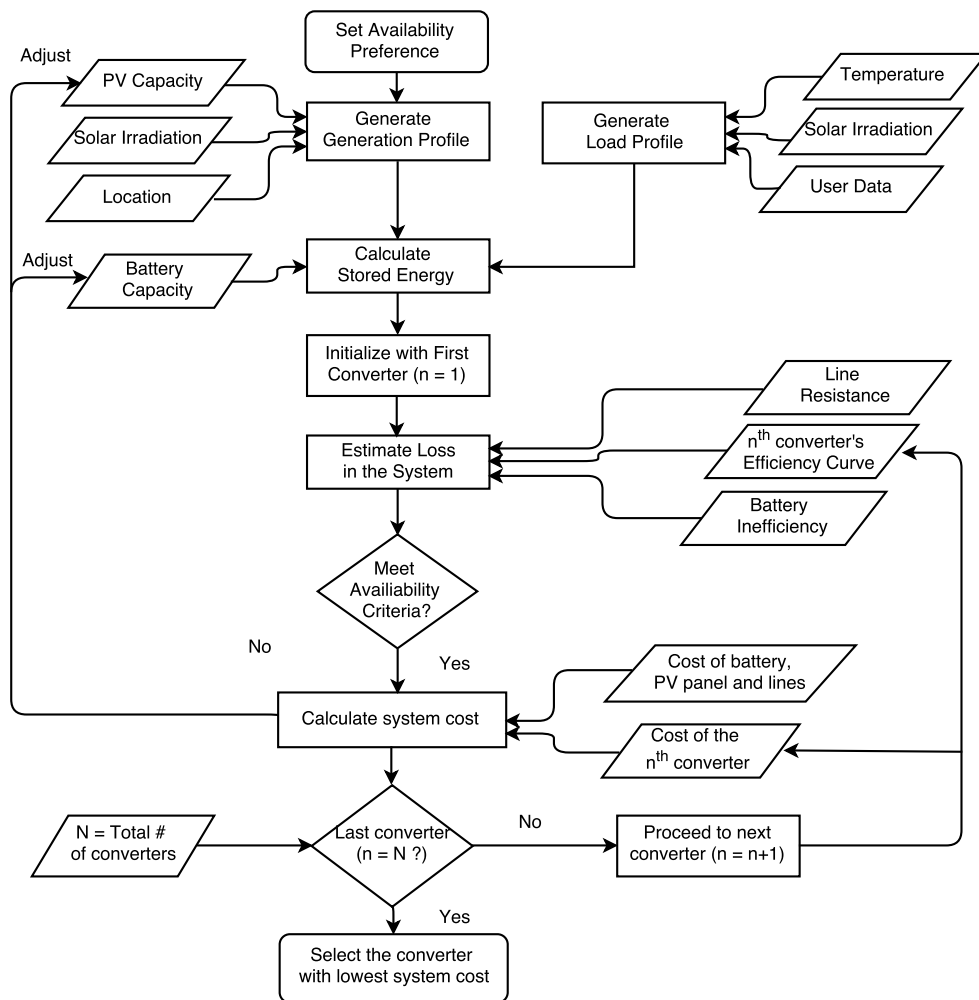


Figure 7-8: Determining the cost of the system with each power converter.

the system and calculate the system cost using the three converters is provided in Appendix C.

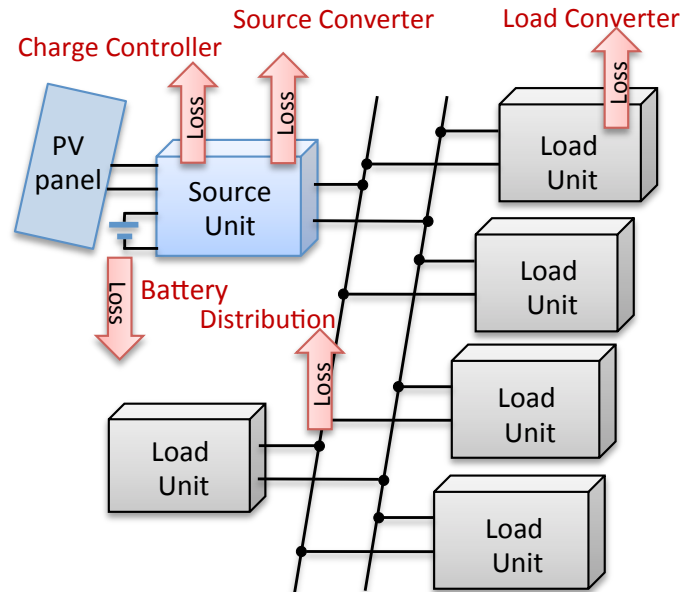


Figure 7-9: A six power management unit system depicting the losses incurred.

Set availability preference

The first step of system cost calculation is to set a desired level of system availability, which is defined as the ratio of energy provided to energy demand. The system cost increases greatly as the availability preference crosses 90 %, hence, the cost of providing 100% availability is much higher than the cost of non-served energy. An availability of 92% was chosen for the simulation.

Calculate generation and load profiles

The generation profile is derived from solar irradiance data of the target location - Jamshedpur, India in this case. The power generated is calculated throughout a year based on different sized solar panels, using the irradiance data from NREL and the capacity of those panels. Similarly, the load profile is determined, as discussed earlier

Table 7.4: System parameters and cost of components used

Parameters	Value
System Parameters	
Number of source units	1
Number of load units	5
Number of Poles	5
Wiring length (per household) from source	40 m
Wiring size	2.55 mm ²
Network voltage	24 V
Availability	92 %
Battery (LFP) lifetime	5 years
Pole (bamboo) lifetime	5 year
System lifetime	15 years
Cost	
PV panel	\$0.7/W
LFP battery	\$0.5/Wh
Power wire	\$0.06/m
Cat3 cable	\$0.03/m
Poles (bamboo)	\$3.33/pole
Source Unit	\$40
Load Unit	\$15 + power stage cost

in Section 7.2.1.

Stored energy

Using the generation profile and load profile, the energy storage requirement is calculated for each hour of the day. The amount of energy stored in the system depends on the battery capacity and the difference of generation and load. If a battery is fully charged, any extra power generated will not be stored, resulting in "spillage", or loss of use of the capability of the solar energy source.

Losses in the system

System losses affect power generation and the required energy storage. Converter inefficiency, battery charging/discharging inefficiency and line resistances contribute to the losses in the system, as shown in Fig. 7-9. These losses are accounted for, as power flow is tracked throughout the system.

Table 7.5: Initial and lifetime cost of the system for 92% availability

Converter	Battery Capacity	PV Panel Capacity	Power Stage (\$/unit)	Power Stage (\$/5 units)	Initial System (\$)	Lifetime System Cost
Flyback	22 Ah	200 W	\$5.28	\$26.4	\$460	\$757.4
Resonant (litz wire)	20 Ah	180 W	\$12.54	\$62.7	\$470.4	\$743.7
Resonant (PCB)	20 Ah	190 W	\$8.85	\$44.3	\$458.9	\$732.2

Breakdown of Initial Cost

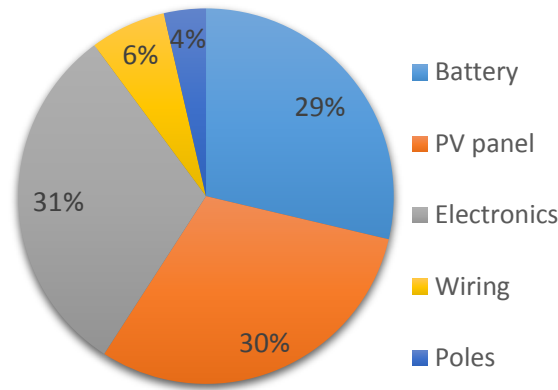


Figure 7-10: Cost breakdown of the system with five Flyback load converters and one source converter.

Iterating and comparing system costs

The system's initial cost includes the cost of the PV panel, battery, converters, distribution lines and mounting poles, as summarized in Table 7.4. The lifetime cost, over 15 years, includes the additional cost of replacement of system components. The battery (Lithium Ferro Phosphate) and poles (bamboo) are replaced every 5 years. Before calculating the system cost, whether the system still meets its target availability is checked after the losses are incurred. For a given converter, battery and PV panel capacity, may need to be increased to meet the availability specification, and the loss calculation iterated until the availability criteria is met.

The simulation is designed to produce the optimal configuration of PV panels and batteries resulting in the lowest lifetime cost. Figure. 7-10 provides the initial capital cost breakdown of the system using the flyback converter. The simulation process

is repeated for every power converter in consideration, and the converter with the lowest lifetime cost is selected. Table 7.5 summarizes the results of the simulation. It can be seen that version 2 of the resonant power converter, with the higher initial cost as compared to the flyback converter, leads to a system with lower initial *and* lifetime costs. The decrease in initial system cost, despite its higher converter cost, is due to the higher weighted efficiency of the multi-output converter which reduces the initial sizing (and hence cost) of other system components, leading to a net system cost reduction. The improved lifetime cost follows from this advantage.

7.4 Conclusion

This chapter summarizes the proposed design methodology to evaluate power converters for the load converter, which play a major role in determining the system cost. Two types of power converters, hard-switched and soft-switched resonant converters, were built to demonstrate the methodology. Although the resonant converter with a PCB transformer had a higher power stage cost, compared to the flyback converter, it resulted in the lowest initial capital and lifetime cost. In this work, only the 12 V main power stage was considered in the analysis. However, this work can easily be extended to include other outputs of the converter.

Chapter 8

Stability and Control of Ad Hoc Dc Microgrids

This chapter focuses on the stability and control of ad hoc networks. Typical methods of stability analysis are not well-suited to ad hoc networks. Methods based on the Middlebrook criterion (also used for input filter design) rely on the ratio of two impedances and typically result in conditions which are applicable only to a particular network configuration, require drastic simplification of the network, and/or are overly restrictive [97], [98]. Passivity-based methods rely on an empirical impedance measurement and are hence not suited for a priori network design [99]. State-space approaches are promising, but previous attempts have placed unrealistic constraints on the network configuration—requiring sources and loads to be paired [100]. Stability is of particular concern because each device is interfaced to the network by a tightly-regulated power converter, which gives the loads a negative incremental impedance [101]. Because they are not pre-planned, ad hoc networks require closed-form conditions that are valid for many network configurations.

Once stability has been guaranteed, it is also useful to control the power flows and voltage levels in the network. In theory, achieving accurate power dispatch and voltage regulation is not difficult, and several suitable methods have been proposed [102], [103]. Many of these methods have not been experimentally validated and do not account for critical nonidealities, like communication delays [104], [105], [106].

In practice, primary (droop) control remains the technique most commonly used for power sharing and secondary control is used to restore the network voltage [58]. Accurate power sharing is principally achieved through the use of very large droop gains (r_d , shown as r_{kk} in Fig. 8-1) relative to the line resistance, which, as discussed further in Section 8.2, is often not acceptable.

To derive a suitable set of conditions for stability, state-space approach is used on a network (graph) with an unspecified incidence matrix. These conditions show that stability of any interconnection of sources and loads can be guaranteed by limiting the total power drawn by the loads and by ensuring a minimum capacitance at the input of each load, which is often already present in the input filter of the load converter. These conditions are more tractable, less complex, and more flexible than previous stability criteria. To achieve acceptable voltage regulation in the transient, and precise power sharing in steady-state, a new, multipurpose, secondary controller is proposed and validated, in simulation and experiment. Unlike previous controllers, multipurpose control achieves precise steady-state power sharing by allowing each δ_k (Fig. 8-1c) to vary independently. Further, this controller is suitable for bidirectional sources—allowing, for example, a battery to either charge from or discharge to the network.

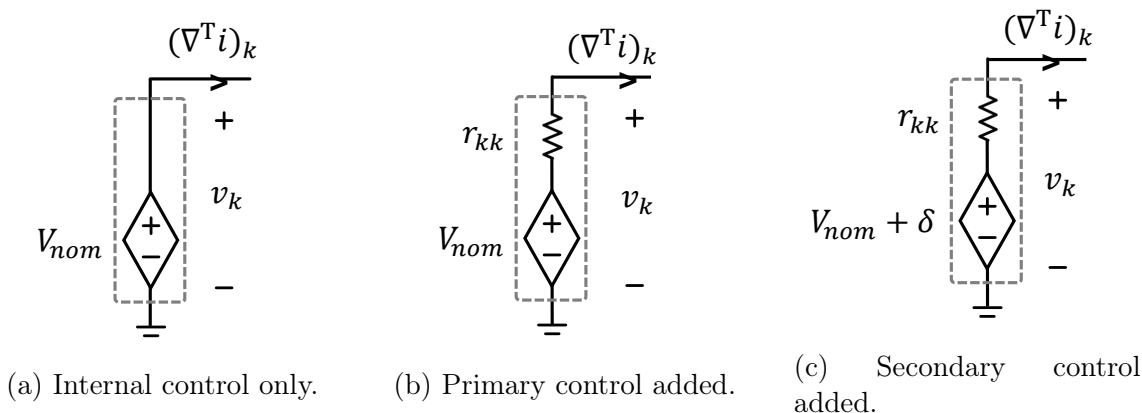


Figure 8-1: Source model with successive levels of hierarchical control. v_k is the converter output voltage. The model with primary control is used for stability analysis in Sections 8.2 and 8.3; secondary control is discussed in Sections 8.4 and 8.5.

The difficulty of guaranteeing the stability and autonomously control of ad hoc

networks has been obstructing their development. In this chapter, simple constraints and control strategies are presented, which help to remove these barriers. Here, “source” is used to describe the combination of a power source, power converter to interface with the network, and communication/control unit to autonomously coordinate with the other sources to schedule and dispatch power. Likewise, “load” refers to a power load and an associated power converter that interface it to the network.

8.1 Microgrid Architecture and Models

The models chosen to represent the sources, loads, and lines are presented in this section. It is assumed that there is timescale separation between the internal converter dynamics and the network dynamics, which allows the use of analytically tractable and general models that can be adapted to describe many converters: droop-controlled voltage sources and constant power loads.

8.1.1 Hierarchically-controlled sources

The model used to represent the source depends on the control scheme used, as shown in Fig. 8-1. The function of each control mechanism is briefly summarized here, and discussed further in Section 8.4. Internal control, which refers to the standard voltage and/or current control loops inside each converter, does not require communication and—for voltage-source converters—realizes $v_k = V_{nom}$. Primary (droop) control varies the output voltage of each converter proportionally to the output current, mimicking a resistor r_d (shown as r_{kk} in Fig. 8-1b). Primary control causes v_k to deviate from the nominal voltage V_{nom} , but allows each converter to control its power output. To mitigate the network voltage deviation caused by primary control, secondary control is used to increment the reference voltage of each converter by δ_k . There are many methods of calculating δ_k , [103], [107]—in Section 8.4 two of these methods are discussed: the standard method [58] and the proposed multipurpose method. Secondary control requires communication. In our system, communication occurs much more slowly than network dynamics (a second degree of time-scale sep-

aration on top of the converter vs. network dynamics), so in the following sections, a droop controlled source (Fig. 8-1b) will be used to evaluate the existence, feasibility, and stability of an equilibrium point.

8.1.2 Loads

The load is modeled as a constant power load (CPL) in parallel with a capacitor, as shown in Fig. 8-2. Using a CPL is a conservative choice because it represents a perfectly regulated power converter with infinite control bandwidth [108]. The parallel capacitor represents the input capacitance of the load converter and is critical for stability in the scheme proposed here. Note that, although the capacitors used for this purpose typically have non-zero parasitic resistance which actually tends to improve system stability margins, that resistance is excluded here.

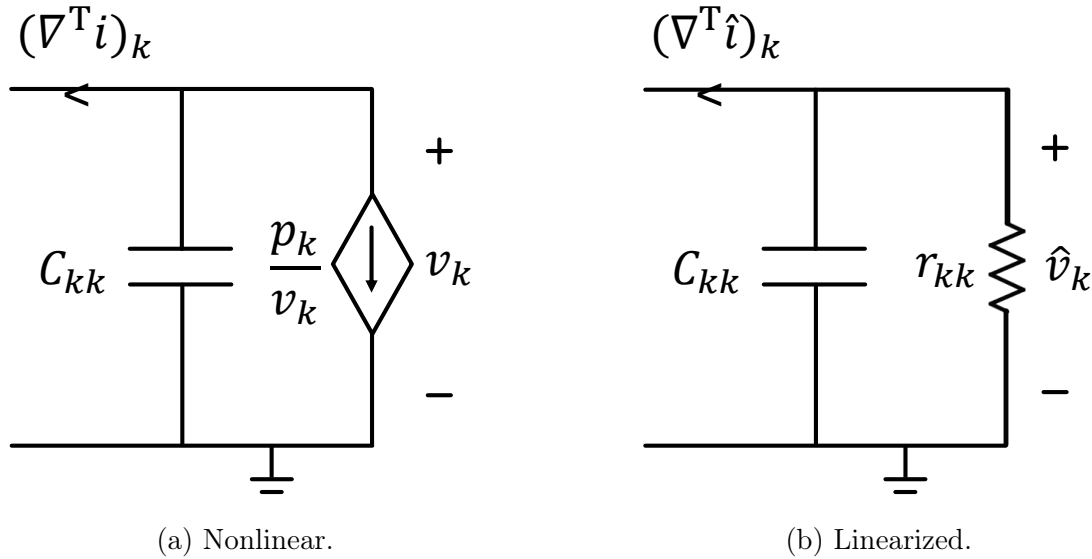


Figure 8-2: Load model. (a) Constant power load with input capacitance, (b) Linearized model used for small signal analysis: $r_{kk} = -V_k^2/P_k$.

8.1.3 Interconnecting lines

The sources and loads are connected by lines modeled with equivalent resistors and inductors, as shown in Fig. 8-3; the time constant of the lines ($\tau_\alpha = L_{\alpha\alpha}/R_{\alpha\alpha}$) are

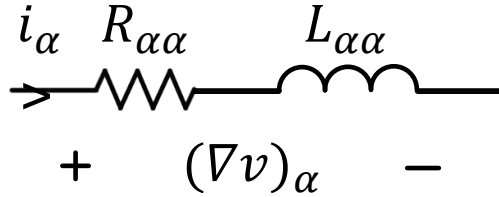


Figure 8-3: Line model.

important to the stability approach undertaken here.

8.1.4 Defining an ad hoc microgrid

To guarantee appropriate operation, in Sections 8.2 and 8.3, bounds on each of the three free parameters will be solved for certifying a set of constraints will be met— independent of the configuration of the network. The parameters and constraints that have been chosen are summarized here.

Constraints

- Minimum equilibrium node voltage V_{min} (that is, the network voltages are constrained to be above some minimum allowed value).
- Minimum equilibrium distribution efficiency $\eta_{min} = P_{out}/P_{in}$. P_{out} is the total power drawn from the network (sum over nodes where $v_k(\nabla^\top i)_k$ is negative) and P_{in} is the total power put into the network (sum over nodes where $v_k(\nabla^\top i)_k$ is positive).
- Small-signal stability of equilibrium point.

Given parameters

- s sources, l loads, and m lines.
- Nominal network voltage V_{nom} .

- Maximum aggregate load power $P_{\Sigma} = \max P_{out}$.
- Maximum line time constant τ_{max} .

Free parameters

- Load input capacitance C_{kk} .
- Droop resistance: source r_{kk} .
- Maximum resistance between a source and a load R_{max} .

8.1.5 Mathematical representation

Any network adhering to the constraints given above can be represented as a graph with $n = s + l$ nodes and m edges. It is assumed that the graph is strongly connected, and that there is a path between every pair of nodes.

The matrices are defined as follows:

- $v \in \mathbb{R}^{n \times 1}$, a vector of node voltages.
- $i \in \mathbb{R}^{m \times 1}$, a vector of line currents.
- $R \in \mathbb{R}^{m \times m}$, a diagonal matrix with $R_{\alpha\alpha}$ equal to the resistance of line α .
- $L \in \mathbb{R}^{m \times m}$, a diagonal matrix with $L_{\alpha\alpha}$ equal to the inductance of line α .
- $r \in \mathbb{R}^{n \times n}$, a diagonal matrix with r_{kk} equal to the resistance from node k to ground. For source nodes, r_{kk} is the droop resistance, while for load nodes, $r_{kk} = -(V_k)^2/P_k$, the linearized constant power load resistance.
- $C \in \mathbb{R}^{n \times n}$, a diagonal matrix with C_{kk} equal to the capacitance from node k to ground. For source nodes, C_{kk} is the parasitic capacitance ($C_{kk} \rightarrow 0$), while for load nodes, C_{kk} is the converter input capacitance.
- $\nabla \in \mathbb{R}^{m \times n}$, an incidence matrix which defines the network topology. Row α has two non-zero elements: $\nabla_{\alpha s} = 1$ and $\nabla_{\alpha t} = -1$, with i_{α} defined as the current

from source node s to target node t . Accordingly, $(\nabla v)_\alpha$ is equal to the voltage drop across line α , and $(\nabla^\top i)_k$ is equal to the total current flowing out of node k .

Using these definitions, the small-signal equations can be written for any network configuration defined by ∇ :

$$C \frac{d\hat{v}}{dt} + r^{-1}\hat{v} + \nabla^\top \hat{i} = 0, \quad (8.1)$$

$$L \frac{d\hat{i}}{dt} + R\hat{i} = \nabla \hat{v}. \quad (8.2)$$

Here $x \approx X + \hat{x}$ which denotes the small-signal variation \hat{x} around the equilibrium point X .

For any pre-determined topology, these equations can be used to numerically check stability and equilibrium point feasibility. However, to design ad hoc systems, the component values have to be picked such that *any* ∇ will result in a system that has an appropriate equilibrium point. This problem is further explored in the following sections.

8.2 Existence and Feasibility of Equilibrium

There are three components of network stability:

- Existence of feasible equilibrium point.
- Small-signal stability of the network.
- Large-signal stability of the network.

The first two components of network stability for ad hoc dc microgrids are discussed in detail, while Large-signal stability is outside the scope of this work.

8.2.1 “Worst-case” network configuration

Existence of an equilibrium point corresponds to the sources’ ability to supply the demanded power. In addition, there are typically tighter bounds specifying a minimum node voltage (V_{min}) and a minimum distribution efficiency (η_{min}). Although the configuration of an ad hoc network can be arbitrary, existence and feasibility of an equilibrium point can be certified by considering a “worst-case” configuration for a set of sources, lines, and loads, assuming the total load power is p_{Σ} and the maximum resistance between a source and a load is R_{max} . The highest distribution losses and maximum voltage deviation both occur when the loads and sources are maximally separated, as shown in Fig. 8-4. Note that the load may be a single load or many loads connected in parallel, but a single source results in a strictly larger voltage deviation compared to multiple parallel sources because of r_d .

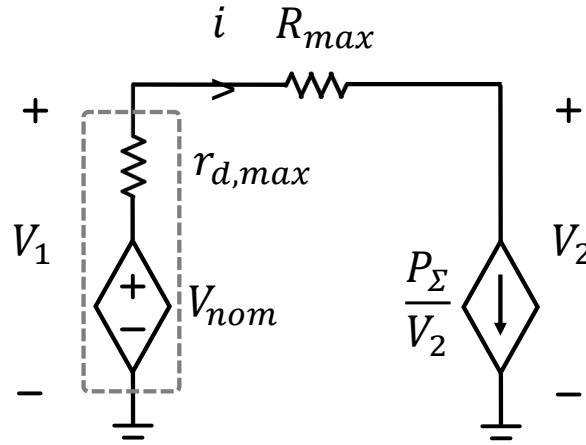


Figure 8-4: Configuration with the highest distribution losses and voltage deviation shown in equilibrium. In terms of the existence and feasibility of an equilibrium point, this is the “worst-case” configuration that can be formed from a set of sources, lines, and loads defined as defined in Section 8.1.4.

8.2.2 Existence of equilibrium

The network shown in Fig. 8-4 will have an equilibrium point (i.e. a real solution) if and only if:

$$R_{max} + r_{d,max} \leq \frac{V_{nom}^2}{4P_{\Sigma}}. \quad (8.3)$$

When (8.3) is binding, $V_2 = V_{nom}/2$ and the total power dissipated at the load is equal to the total power dissipated in the lines. In typical electrical networks, $V_{min} \gg V_{nom}/2$ and $\eta \gg 0.50$, so additional analysis is needed to ensure the feasibility of the equilibrium.

8.2.3 Feasibility of equilibrium

There are two constraints— $\eta \geq \eta_{min}$ (η defined in 8.1.4) and $V_2 \geq V_{min}$ —which together determine the two free parameters in the system— R_{max} and $r_{d,max}$. First, the minimum voltage level is used to fix the sum of the resistances. From Fig. 8-4, the voltage deviation constraint will be satisfied when:

$$R_{max} + r_{d,max} \leq \frac{V_{min}(V_{nom} - V_{min})}{P_{\Sigma}}. \quad (8.4)$$

Next, the distribution efficiency constraint is determined:

$$\eta_{min} \leq \frac{P_{\Sigma}}{\left(V_{nom} - \frac{P_{\Sigma}}{V_2} r_{d,max}\right) \frac{P_{\Sigma}}{V_2}}. \quad (8.5)$$

These constraints—(8.4) and (8.5)—can be reduced to explicit expressions for R_{max} and $r_{d,max}$ (as both constraints will bind simultaneously) by substituting $V_2 = V_{min}$ into (8.5). This way, (8.4) can be used to find the maximum total resistance, and then (8.5) can be used to split the total allowable resistance into the line resistance and the droop resistance:

$$R_{max} \leq \frac{V_{min}^2(1 - \eta_{min})}{P_{\Sigma}\eta_{min}}, \quad (8.6)$$

$$r_{d,max} \leq \frac{V_{min}(\eta_{min}V_{nom} - V_{min})}{P_{\Sigma}\eta_{min}}. \quad (8.7)$$

Note that, because $r_{d,max}$ is an internal control parameter, it does not dissipate

power. Accordingly, the efficiency will always be higher than the per unit voltage deviation: $\eta > V_2/V_{nom}$.

To summarize: given an ad hoc microgrid defined by a nominal voltage V_{nom} , a maximum total load P_Σ , and some constraints— V_{min} and η_{min} —as long as $V_{min} \geq V_{nom}/2$ an equilibrium point will exist for any network configuration and, Eqs. (8.6) and (8.7) can be used to solve for the allowable line and droop resistances. If the network is overloaded and these constraints are not satisfied, load shedding can be used to ensure appropriate operation. The ability to shed load through operation of the load converters is one of the features of the proposed approach to the ad hoc grid.

8.3 Small-signal Stability

In addition to feasibility, the stability of the equilibrium point needs to be guaranteed. This is especially difficult for ad hoc networks for two reasons:

- All loads are interfaced to the network via tightly-regulated power electronic converters and hence have a negative incremental impedance, which has a destabilizing affect on the network.
- The network configuration is not predetermined, so conditions are found on the individual units (sources/loads) such that the microgrid formed by *any interconnection* will be stable.

Existing methods of stability analysis are not well-suited to overcoming these challenges. In this section a more general state-space approach that we have used to develop suitable conditions is presented. Here, we rely on both linearized models and the assumption that all lines in the network have the same time constant. It has also been shown that the technique can be generalized to nonlinear models and variable time constants using more sophisticated techniques [57].

8.3.1 Simple network

To demonstrate the approach, first consider the simple network shown in Fig. 8-5. A single source, load, and line are connected, with the load linearized around V_1 and drawing power P_1 , where $r_{cpl} = -V_1^2/P_1$. Applying the Routh-Hurwitz stability criterion to the network (equivalently, checking that the real part of each eigenvalue is negative), two necessary and sufficient conditions for small-signal stability are obtained:

$$C_i > \frac{L_l}{R_l + r_d} \frac{P_1}{V_1^2}, \quad (8.8)$$

$$\frac{V_1^2}{P_1} > R_l. \quad (8.9)$$

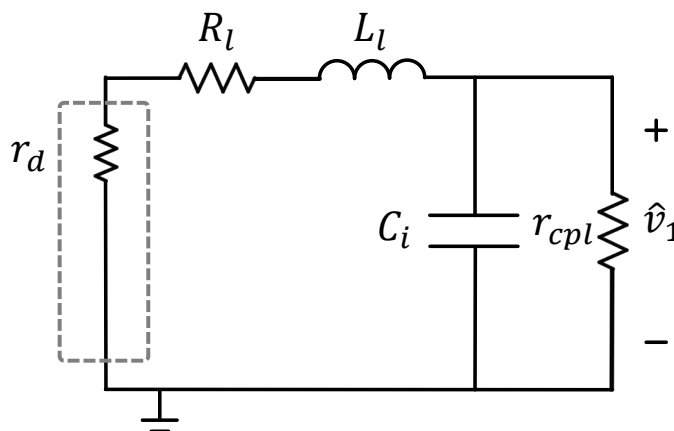


Figure 8-5: Simple system for demonstrating small-signal stability analysis.

8.3.2 General formulation

The same approach can be used on a general system defined by the node and line state equations (8.1) and (8.2). Assuming that all lines have a single time constant $\tau = L_{\alpha\alpha}/R_{\alpha\alpha}$, they can be combined into one second order equation:

$$\tau C \ddot{\hat{v}} + (C + \tau r^{-1}) \dot{\hat{v}} + (\nabla^\top R^{-1} \nabla + r^{-1}) \hat{v} = 0. \quad (8.10)$$

Multiplying by \hat{v}^\top and rearranging:

$$\frac{d}{dt} \frac{1}{2} \left[\hat{v}^\top \tau C \hat{v} + \hat{v}^\top (\nabla^\top R^{-1} \nabla + r^{-1}) \hat{v} \right] = \hat{v}^\top [C + \tau r^{-1}] \hat{v} \quad (8.11)$$

The stability of the network is guaranteed if the following necessary and sufficient conditions are satisfied:

1. The left side of (8.11) defines a convex Lyapunov function:

$$\tau C \succ 0, \quad (8.12)$$

which is trivially satisfied in real networks, and

$$\nabla^\top R^{-1} \nabla + r^{-1} \succ 0. \quad (8.13)$$

2. The right side of (8.11) is always negative:

$$C + \tau r^{-1} \prec 0. \quad (8.14)$$

If the network is completely pre-determined (i.e., the component values and topology are known beforehand), these matrix inequalities can be checked numerically. However, to design ad hoc systems, (8.13) and (8.14) need to be reduced to conditions on individual sources and loads.

8.3.3 Small signal stability: condition 1 of 2

Equation (8.13) can be interpreted physically by noticing that, when multiplied by \hat{v}^\top and \hat{v} , the first term corresponds to the power dissipated in the lines and the second term corresponds to the power dissipated in the loads. Informally, to be stable, the small signal model of the network must always dissipate positive power. This is trivial in systems with positive resistors, but is not necessarily satisfied in networks with constant power loads. Using a path decomposition argument, Equation (8.13)

can be reduced to [57]:

$$\frac{V_{min}^2}{R_{\Sigma} + r_{d,max}} \geq P_{\Sigma}. \quad (8.15)$$

8.3.4 Small signal stability: condition 2 of 2

Equation (8.14) can be reduced by noting that, for a diagonal matrix D , $D \succ 0$ if and only if $D_{ii} > 0$ for all i . Accordingly, $\tau^{-1} + 1/(r_{kk}C_{kk}) > 0$ for all k .

For generator nodes this can be rewritten:

$$r_d C_{kk} > -\tau. \quad (8.16)$$

For positive droop resistances, this is trivially satisfied in the limit $C_{kk} \rightarrow 0$.

For load nodes, however, the condition is not always satisfied:

$$C_{kk} > \frac{\tau P_k}{(V_k)^2}. \quad (8.17)$$

This condition depends on the equilibrium node voltage V_k and equilibrium output power P_k , but can be further simplified by assuming $V_k \geq V_{min}$ and $P_k \leq P_{k,max}$. Hence, each load capacitance must satisfy:

$$C_{kk} > \frac{\tau P_{k,max}}{V_{min}^2}. \quad (8.18)$$

In general, with many line time constants τ in the network, it has been shown [57] that (8.18) generalizes to:

$$C_{kk} > \frac{\tau_{max} P_{k,max}}{V_{min}^2}. \quad (8.19)$$

8.4 Microgrid Control

In the previous sections, conditions were found under which the microgrid, in the presence of internal and primary control, will have a stable equilibrium point. In addition, secondary control is often used to improve the performance of the network. For this discussion, we use the conventional definitions of the control levels: primary

control consisting of a “virtual” (droop) resistor and secondary control consisting of an offset voltage δ , as shown in Fig. 8-1 [58]. Together, primary and secondary control are used to ensure three objectives:

- **Limiting circulating currents.** When ideal voltage sources are connected in parallel through lines with small resistances, small mismatches in the source voltages V_{nom} can cause large circulating currents (currents charging one source from another). Nonidealities make these mismatches inevitable, but these currents can be reduced by including additional resistance.
- **Regulating the network voltage.** The devices connected to the network are designed to operate in a specified voltage range. Accordingly, all node voltages should remain near the nominal voltage V_{nom} . The desired voltage level does not change and should be maintained with or without communication.
- **Dispatching power.** Each source should be able to set (and update) its fraction of total supplied power. Each power source has a cost function that describes how “expensive” it is for that source to supply power (based on factors like the state-of-charge of the battery). To ensure that power is supplied at minimal cost, each time the optimal dispatch is computed, it is required to physically realize the dispatch by coordinating the sources.

Typically, primary control is used to set the fraction of power each source supplies and secondary control is used to correct for the voltage deviation caused by primary control [58]. However, to accomplish power dispatch using only primary (proportional) control, very large droop resistances (gains) must typically be used. These large values of r_d cause large transient voltage deviations, meaning that, using the conventional method, there is an unavoidable trade off between power-sharing accuracy and transient voltage regulation. Maintaining appropriate node voltages is critical for converter operation. While accurate power dispatch is desirable, it is not a critical feature.

To ensure all control objectives are met *even with* small r_d values, here, a new formulation of primary and secondary control is proposed. In this method, the network will function properly (maintaining all node voltages $\geq V_{min}$) in the absence of secondary control by designing r_d in accordance with the V_{min} constraint (Equation (8.7)). Droop control is only used to limit circulating currents, so all r_d values are set equal to $r_{d,max}$, as defined by Equation (8.7). By contrast, in the conventional method, r_d must be updated to change power sharing proportions, which requires communication *anyway*. In the proposed method, r_d values do not change, so primary control of the proposed method is truly local, and power sharing proportions are determined by a new parameter, λ . Using λ the power sharing objective is incorporated into the secondary controller, in addition to the voltage regulation objective. In essence, while the traditional method varies the droop resistances (source Thevenin resistances) to control power sharing, here the Thevenin resistances are fixed, and Thevenin equivalent voltages are adjusted of the sources to control power sharing.

First, the voltage error is defined:

$$e_v = V_{nom} - \bar{v} \quad (8.20)$$

This is the same for each source. \bar{v} is the average node voltage of all sources—it could also be defined as the average node voltage (including loads), but here, it is assumed that only sources have communication capabilities.

Next, λ is used to specify a desired fraction of total power that each source supplies. The power error is defined as:

$$e_{p,k} = \lambda_k \bar{p} - \bar{\lambda} p_k \quad (8.21)$$

This is *not* the same for each source. \bar{p} and $\bar{\lambda}$ are p and λ averaged over the sources.

Together, these can be combined into an integral controller:

$$\dot{\delta}_k = k_{i,v} e_v + k_{i,p} e_{p,k} \quad (8.22)$$

Unlike the standard method of control, in the proposed method, the δ_k 's are not the same for all sources, which allows us to achieve accurate power sharing in steady-state. Additionally, this control can realize arbitrary power sharing ratios—allowing, for example, one source to produce zero power without disconnecting, or batteries to charge from the network (setting $\lambda_{\text{battery}} < 0$ to charge, and > 0 to discharge). The inclusion of primary control limits transient circulating currents, while still maintaining adequate voltage regulation.

The controller can be discretized based on the messaging delay T_m :

$$\delta_k[t] = \delta_k[t - T_m] + T_m k_{i,v} e_v[t] + T_m k_{i,p} e_{p,k}[t]. \quad (8.23)$$

The implementation of the controller can be done in a centralized or distributed manner, depending on the communication configuration of the network. Either a central “master” node can receive the necessary information (voltage and current from each source), compute the δ_k 's, and relay them back to the other sources, or source nodes can locally store the state of all other sources and perform the computations themselves.

8.5 Experimental Validation

Here, validation of a microgrid that adheres to the constraints developed in previous sections is presented, demonstrating power sharing accuracy in response to a load step. The test setup is a microgrid consisting of two source (boost) converters and seven load (flyback) converters connected as shown in Fig. 8-7. This setup uses source and load converters as developed in the previous chapters. First, the network is analyzed in the context of the previously-determined constraints.

8.5.1 Designing a sample network

First, it is demonstrated how the conditions in the equilibrium point section can be relaxed by imposing some restrictions on the network topology. Here, the network is

restricted to a “distributed star” network, where all sources are connected with lines of impedance $Z_2 = R_2 + j\omega L_2$ and all loads are connected to the nearest source with another line of impedance $Z_1 = R_1 + j\omega L_1$, as shown in Fig. 8-7. There are two sources and seven loads on the network, and each load is either off or on: $p_k \in \{0, 20\}W$. The “worst case” under these restrictions is shown in Fig. 8-6. Without any restriction on the configuration, $R_{max} = R_1 + R_2$ and $P_\Sigma = 140 W$. However, in the configuration shown in Fig.8-6, the 7 identical loads can be reduced to a single equivalent load, reducing R_{max} to $R_1/7 + R_2$. Now, using the constraints derived in Section 8.2, allowable r_d , R_1 , and R_2 values can be calculated. The constraints and results are summarized in Table 8.1.

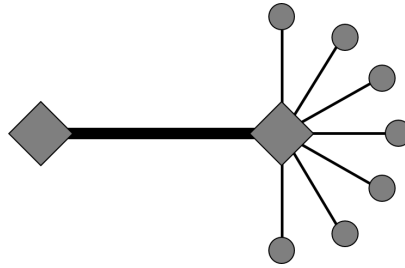


Figure 8-6: Two sources and seven loads connected in the "worst case" distributed star topology.

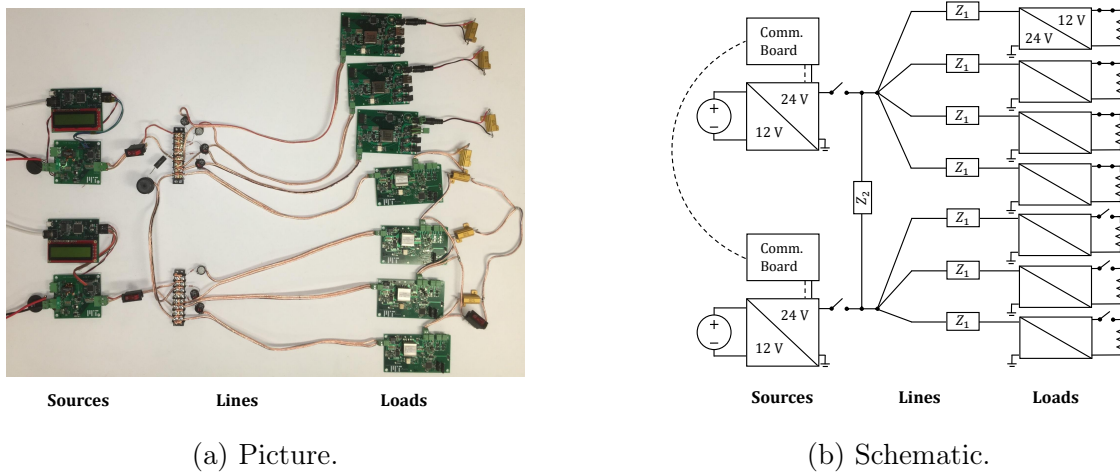


Figure 8-7: Experimental setup with two sources and seven loads.

Table 8.1: Network Specifications

Parameter	Value
Predetermined Parameters	
Network Configuration	Distributed Star
Number of Sources	2
Number of Loads	7
Nominal Voltage (V_{ref})	24 V
Total Load Power (p_{Σ})	140 W
Max Line Time Constant (τ_{max})	0.27 ms
Constraints	
Min Node Voltage (V_{min})	18 V
Min Distribution Efficiency (η_{min})	90%
Free Parameters	
R Between Source and p_{Σ} (R_{Σ})	$0.22 \Omega (\leq 0.26 \Omega)$
Droop Resistance (r_d)	$0.50 \Omega (\leq 0.51 \Omega)$
Load Input Capacitance (C)	$80 \mu\text{F} (\geq 16.7 \mu\text{F})$
Control Parameters	
Time between messages (T_m)	1.5 s
Voltage gain ($k_{i,v}$)	$0.30 \text{ V}^{-1} \text{ s}^{-1}$
Power gain ($k_{i,p}$)	$0.017 \text{ W}^{-1} \text{ s}^{-1}$
Experiment: Line Impedances	
$Z_1 = R_1 + j\omega L_1$	$0.83 \Omega + j\omega(18 \mu\text{H})$
$Z_2 = R_2 + j\omega L_2$	$0.10 \Omega + j\omega(27 \mu\text{H})$

8.5.2 Experimental results

The experimental results are shown in Fig. 8-8 and Fig. 8-9. In Fig. 8-8, $\lambda_1 = \lambda_2 = 1$, and the sources shared power equally. In Fig. 8-9, $\lambda_1 = 1.2$, $\lambda_2 = .8$, and the sources realized the specified ratio. In both cases, a small steady-state error is observed, which is smaller than the tolerance of our measurement equipment. The three largest sources of error are:

- Current sensor in each source converter (ACS711): $\pm 5\%$ accuracy.
- Oscilloscope current probe (TCP0030 and TCP202): $\pm 1\%$ accuracy.

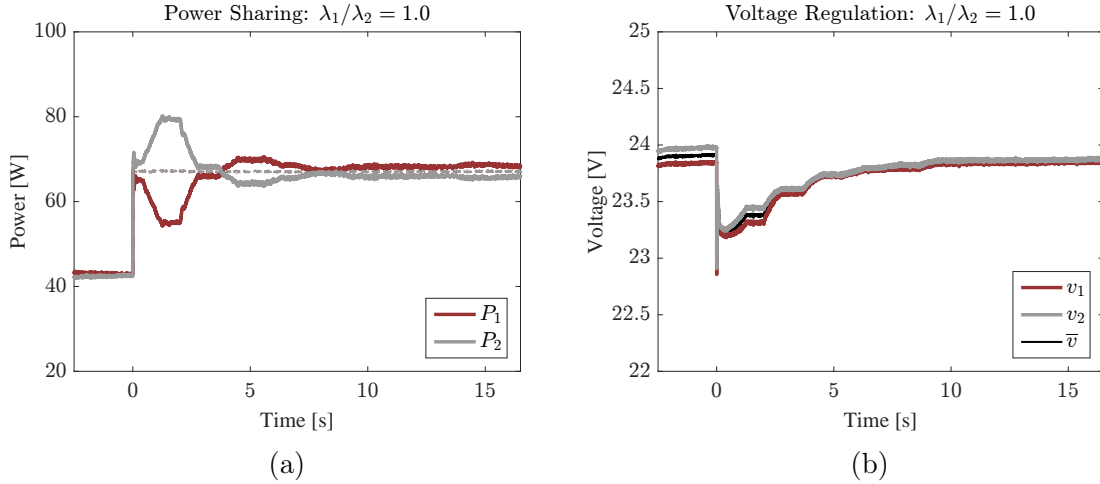


Figure 8-8: Experimental demonstration of equal power sharing accurate to within the precision of the testing equipment.

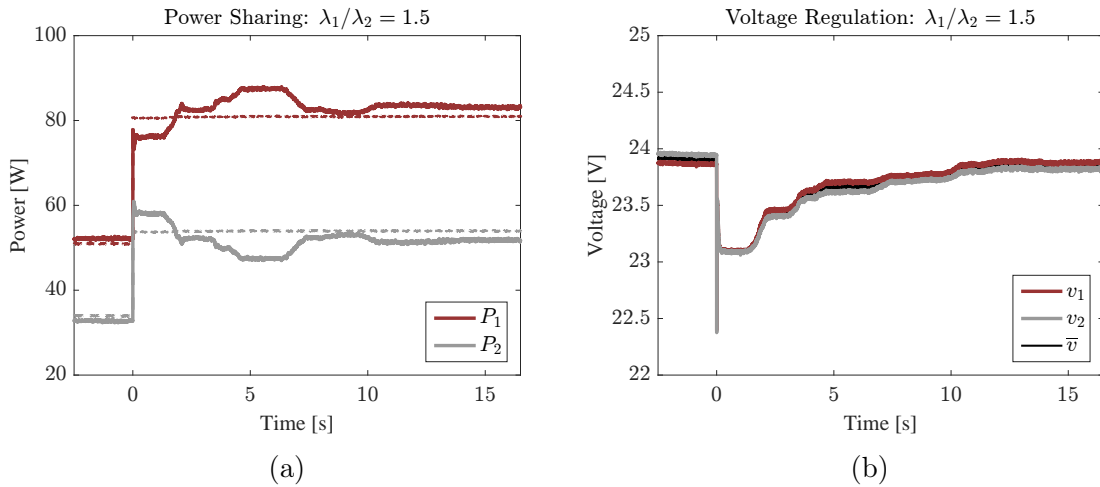


Figure 8-9: Experimental demonstration of realizing a specified, unequal, power sharing ratio accurate to within the precision of the equipment used.

In addition, small variations can be observed (especially in Fig. 8-8a—less than 5% deviation from the desired value) after the controller has largely settled—after approximately 8 s. These are caused by measurement noise, and could be eliminated by turning the controller off once the error is smaller than some threshold.

8.6 Conclusion

In this chapter, it is demonstrated how individual source and load units can be designed to meet relevant set of constraints: existence, feasibility, and small-signal stability of the network equilibrium point. In addition, a new, multipurpose, secondary control scheme was proposed, which can achieve precise steady-state power sharing and is capable of realizing arbitrary power sharing proportions. Broadly, the ability of a modular and reconfigurable microgrid to maintain stable operation was demonstrated to achieve dynamic power sharing, regulate the network voltage, and adhere to efficiency constraints without the need for central pre-planning or oversight.

Chapter 9

Conclusion

This thesis explores adaptable power conversion for two applications: improving efficiency of universal input power supplies and providing affordable electricity in off-grid areas. Improvements made in these applications can have a significant impact on how power from the grid is utilized, and how power utilization is enabled where the grid does not exist. The techniques and design methodology developed for these applications can easily be extended to other applications where adaptable and efficient power conversion is required.

9.1 Contribution

The following two subsections describe the respective contributions of this work to improving universal input power supplies, and creating ad hoc microgrids for off-grid electricity access.

9.1.1 Efficient universal input power supplies

In this work, a new technique (VFX) was developed to efficiently operate converters in a wide operating range (voltage and power). In this technique, the converter either processes energy at the fundamental, or one or more higher harmonic frequencies. This results in gain changes for the inverter and/or rectifier, which extends the input

and/or output range of the converter. The techniques applied to both the inverter and rectifier were presented.

Additionally, the VFX technique was applied to the inverter of the stacked-bridge LLC converter to demonstrate the effectiveness of this technique for universal input power supplies. The LLC converter built was able to achieve a high efficiency, ranging from 94.9% to 96.6%, across the 4:1 input voltage range. The VFX technique can be useful to obtain high efficiency across a wide range of operation and can be applied to other applications where a wide operating range is required.

9.1.2 Ad hoc microgrids for off-grid electricity access

In this work, a new ad hoc microgrid architecture was proposed, which can provide affordable electricity access in off-grid areas. Contrary to how conventional power systems are designed, these microgrids do not require pre-planning and can operate in any network configuration. For these ad hoc microgrids, converters were built with two cost-based strategies: designing converters to reduce cost of the converter, and designing converters to reduce cost of the overall system. A weighted efficiency metric was developed to evaluate the converters built to determine the converter with the lowest lifetime energy loss. A system level simulation with efficiency and cost models of all the components in the system was used to trade-off efficiency and cost to determine the converters resulting in lowest cost of the system. Stability criteria developed for the ad hoc dc network, based on passive components, were used to assess the input filter requirements of the load converter. A two-level control technique was developed to accurately share power from multiple sources and precise power sharing was demonstrated using a two-source and seven-load experimental setup. Moreover, an initial implementation of the proposed approach - including prototype converter hardware and communications - has been tested in field trials and used to draw lessons about key issues with this new technology.

9.2 Recommendations for Future Research

The following two sub-sections describe recommendations for future research.

9.2.1 Efficient universal input power supplies

- The theory of applying this technique to the rectifier stage was presented, however, this was not experimentally demonstrated. The VFX technique applied to the rectifier stage to operate over a wide output voltage range or power range will further advance this research.
- A two mode VFX technique was discussed, however, this technique can be easily extended to higher modes of operation to operate the converter with even a wider operating range. This involves the use of higher harmonics to provide more voltage gains.
- This technique was applied when the converter either operated in mode 1 or mode 2 (as the input voltage seen by the universal input power supply is either 110 Vrms or 220 Vrms at a time), hence, the converter does not need to change modes continuously. Demonstrating how this technique can be applied in continuous operation would allow this technique to be applied in a wide variety of applications.
- Control and sensing techniques to change the modes of operation need to be explored.

9.2.2 Ad hoc microgrids for off-grid electricity access

- A source PMU to integrate solar panels and batteries to the network, and a load PMU to integrate residential loads have been developed. However, work needs to be done to integrate other sources (such as solar pumps, micro hydro, diesel generators etc) and loads (commercial and industrial) on to the network.

- Low voltage dc distribution was used for keeping the cost low and for safety reasons. Developing low cost and safe ad hoc microgrids with interface to high voltage dc or ac distribution has not been explored in this thesis, but could be explored in the future.
- The load converter design was discussed in detail, and multiple load converters were built. Similar work for the source converter needs to be carried out, especially, the design of a very efficient source converter, as currently an expensive heat sink needs to be used. Also, efficient resonant converter topologies, which can be cost competitive with basic topologies, need to be further explored.
- For control of multiple sources, techniques to determine the dispatch function, which determines the power ratio, have not been explored in this thesis, but work on this in the future could benefit the development of ad hoc microgrids.

Appendix A

Schematic, PCB Layout, Components Used and Code for VFX Converter

This appendix provides schematics and images of the PCB layout for the VFX converter. The PCB is designed using EAGLE software of Cadsoft inc. The PCB image is scaled by a factor of 2 for clarity. The components used are provided in a table. Also, the code used to design and analyze the VFX converter is provided.

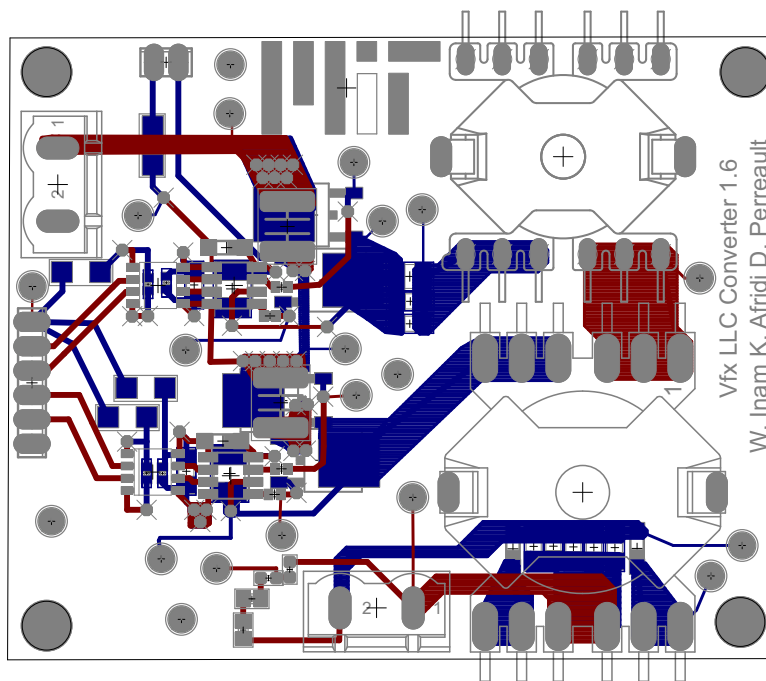


Figure A-2: VFX converter PCB layout, top and bottom layers (zoomed 2x).

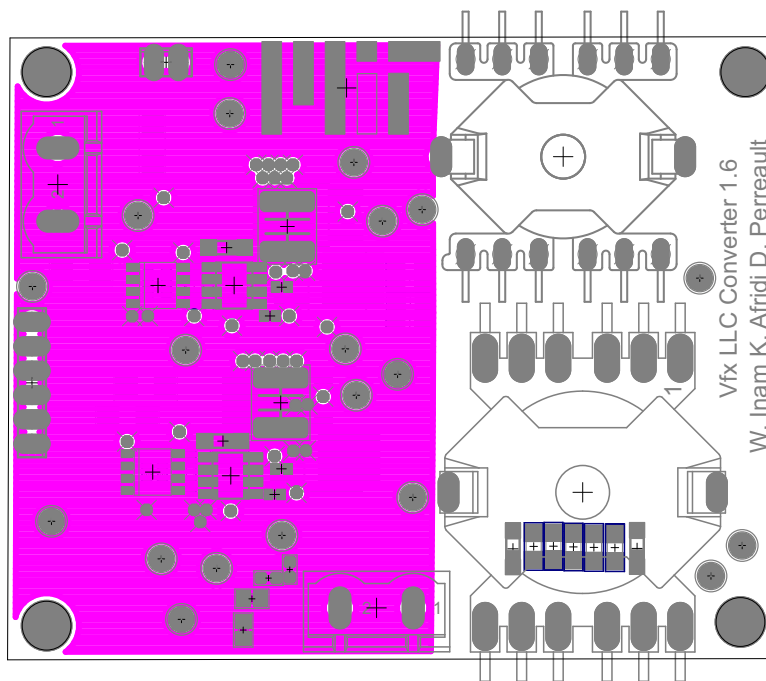


Figure A-3: VFX converter PCB layout middle ground layer (zoomed 2x).

Table A.1: Components of VFX converter

Part	Value	Package
C1	10u	C1206
C2	10u	C1206
C3	10u	C1206
C4	1u	C0402
C5	1u	C0402
C6	10u	C1206
C31	10u	C1206
C32	5600p	C1206
C33	1800p	C1206
C34	0.016u	C1210
C35	10u	C1812
C36	10u	C1812
C37	22u	C1206
C38	22u	C1206
C39	1u	C0402
C40	1u	C0402
C41	1u	C2220
C42	1u	C2220
R1	-	R0603
R2	-	R0805
R3	-	R0805
R4	-	R0603
R5	0	R0402
R6	0	R0402
R7	0	R0402
R8	0	R0402
U\$1	IRS21867	SO8
U\$2	-	-
U\$3	IRS21867	SO8
U\$4	IPD230N20N3G	TO252
U\$5	IPD230N20N3G	TO252
U\$6	IPD230N20N3G	TO252
U\$7	IPD230N20N3G	TO252
U\$8	3.6u	RM8-12
U\$9	IL711	8-SOIC(NB)
U\$10	TRANSFORMER	RM10-12
U\$11	PMEG030	SOD123
U\$12	PMEG030	SOD123
U\$13	IL711	8-SOIC(NB)
U\$14	-	-
U\$19	MMSD3070	SOD123
U\$20	MMSD3070	SOD123
U\$21	-	-
U\$22	-	-
X2	OSTOQ021251	1751248
X3	1881448	2POL254
X5	1881480	6POL254
X6	OSTOQ021251	1751248

```

1 %% VFX_code
2 % This script generates the code to design VFX converter
3 clc
4 clear all
5 %%
6 %For without vfx change Vimax to X2 and Mmax x2
7 %Inputs
8 Vimax=170; %Max input voltage; 340 for without vfx
9 Vinnom=Vimax; % Nominal voltage
10 Vo=20; %Output voltage
11 P=50; % Max power
12 f=500*10^3; % frequency of switching
13 Co=350*10^-12; %output capacitance of transistor
14 Mmin=1; %Min gain
15 Mmax=2.4; % Max gain
16 T=80; %Temperature
17
18 %% Calculated values
19 w=2*pi*f; %angular frequency
20 %step 1 - Transformer transfer ratio
21 n=Vinnom/(2*Vo); %
22 %step 2 -choose k
23 k=7; %Lm/Lr
24 %step 3 - Find Q
25 A_c=(1-1/Mmax^2);
26 B_c=1+k*A_c;
27 C_c=Mmax^2-1;
28 Qmax=sqrt(B_c/C_c)/k;
29 Q=Qmax;
30 %Step 4 - Find reflected load
31 Ro=Vo^2/P; % output resistance
32 R=8*Ro/pi^2; % effective rectifier resistance
33 Rn=R*n^2; % effective rectifier resistance transferred to the primary
34 %step 5 - Find values of components
35 Zo=Q*Rn; %mid calculation

```



```

36 L=Zo/w; %Value of inductor
37 Lm=k*L; %Value of Lm inductor
38 Cr=1/(Zo*w); %Value of capacitor
39 %step 6- Find angle of switching
40 Z=Rn+w*Lm*i;
41 theta=angle(Z);
42 theta=radtodeg(theta);
43 %step 7 - Find fmin and deadtime
44 fmin= 1/sqrt(B_c); % min frequency for max gain
45 td= 8*Co*f*Lm; %Deadtime required for ZVS
46
47 fprintf('k= %i\n',k);
48 fprintf('Q= %f\n',Q);
49 fprintf('fmin= %i Hz\n',fmin);
50 fprintf('Lr= %i H\n',L);
51 fprintf('Cr= %i F\n',Cr);
52 fprintf('Lm= %i H\n',Lm);
53 fprintf('td= %i s\n',td);
54 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
55 %% Plot gain
56
57 Ln=k;
58 i=0;
59 for fn=0.2:0.01:1.5
60     i=i+1;
61     Num=Ln*fn^2; %Numerator of gain function
62     Den= sqrt( ((Ln+1)*fn^2-1)^2+ ((fn^2-1)*fn*Q*Ln)^2); %Denominator of
        gain function
63     M(i)=Num/Den; % Gain function (TI- design doc)
64     Mz(i)=fn/sqrt(fn^2*(1+(1/Ln))-(1/Ln));
65 end
66 fn=(0.2:0.01:1.5);
67 p=plot(fn,M); %Plot gain versus normalized frequency
68 xlabel('Normalized inverter output frequency, \itx ','FontName','Times
        New Roman','fontsize', 15)
69 ylabel('Gain of the resonant network, \itM','FontName','Times New Roman'

```

```

    , 'fontsize', 15)
70 set(p, 'color', [0.6 0.2 0.2], 'LineWidth', 2.5)
71 set(gca, 'linewidth', 1, 'fontsize', 16)
72 axis([0.2 1.5 0.2 2.5])
73 hold on
74 grid on
75 save2pdf('C:\Users\Wardah\Desktop\gain.pdf')
76 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
77 %% Component Design
78
79 %Constants
80 mu=4*pi*10^-7; % magnetic constant
81 rho=1.72*10^-8*(1+0.0039*60); % Resistivity of Cu
82 mil=25.4*10^-6; % 1 mil in meters
83 %3F3 Temperature parameters
84 Cm=[0.25*10^-3; 2*10^-5; 3.6*10^-9];
85 x=[1.63; 1.8; 2.4];
86 y=[2.45; 2.5; 2.25];
87 ct2= [0.79; 0.77; 0.67]*10^-4;
88 ct1=[1.05; 1.05; 0.81]*10^-2;
89 ct0=[1.26;1.28;1.14];
90 %Core Values RM10
91 Ae= 0.96*10^-4; %m^2 %%
92 Bbob=10*10^-3; %m %%
93 hbob=4.25*10^-3; %m %%
94 MLT=52*10^-3; %m %%
95 Ve= 4.310; %cm^3 %%
96 BWindA=12.4*10^-3; % m %%
97 % % 48 AWG
98 n_strands= [3 4 5 6 7 8 9 10 14 15 18 20 24 25 26 30 33 40 45
    46 50 52 60 64 65 75 100 105 108 115 125 140 150 175 180 200
    210 225 300 420 450 675 1000 1100 1680 1700 1725 1800 2700 3400 3800
    4000 4500 6750];
99 od_litz= [ 5 5.5 6 6 6.5 7 7 7.5 8.3 8.5 9.2 9.5 10 10 10 11 12 12 13
    13 14 14 15 15.5 15 16 18 19 19 19.9 20 21.5 22 24 24.5 26 27
    28 31 38 42 47 53 62 71 72 73 75 89 99 144

```

```

124 130 169]*10^-5*2.54;
100 Wawg_a=48;
101 %Calculate currents
102 Im= (2*sqrt(2)/pi)*(n*Vo/(2*pi*f*Lm)); %RMS current magnetizing
      inductance
103 Io=P/Vo; %DC output current
104 Ioe=(Io/n)/(2*sqrt(2)/pi); %RMS current into rectifier
105 Ir=sqrt(Im^2+Ioe^2); %RMS current of resonant inductor
106 Ip=Ioe; %RMS current of transformer primary
107 Is=n*Ioe; %RMS current transformer secondary
108 Vcr_pk=2*n*Vo+2*Ip*sqrt(2)*sqrt(L/Cr)-(Vinnom/2);
109 %%%% Transformer Design %%%%%%%%%%%%%%%
110 B=30*10^-3; %T
111 Vi=Vimax/2; %Peak value
112 flux=Vi/f; %Vi*s
113 %Number of turns
114 np= flux/(2*Ae*B); %Primary turns
115 ns=np/n; %Secondary
116 fv=2; %frequency range for temerpature parameter selection
117 c=(ct0(fv)-ct1(fv)*T+ct2(fv)*T^2);
118 Pc= (Cm(fv)*(f^x(fv))*(B^y(fv))*c)*Ve*10^-3; %originially mW/cm^3 -> W/m
      ^3
119 %for K=2:2:4
120 for j=1:length(od_litz) %Number of litz wire that can fit
121
122     n_turns_b(j)= floor((Bbob/3)/od_litz(j)) ;
123     n_turns_h(j)=floor((hbob)/od_litz(j)); % /2 because two windings
124     n_turns(j)= n_turns_b(j)*n_turns_h(j);
125     if n_turns(j)<np
126         break
127     end
128 end
129 if j==1
130     disp('Litz cant fit');
131     j=2;
132 end

```

```

133 % if K==2
134 litz_strands_p=n_strands(j-1);
135 for K=1:length(od_litz) %Number of litz wire that can fit
136
137     n_turns_b_s(K)= floor((Bbob/3)/od_litz(K)) ;
138     n_turns_h_s(K)=floor((hbob)/od_litz(K)); % /2 because two windings
139     n_turns_s(K)= n_turns_b_s(K)*n_turns_h_s(K);
140
141     if n_turns_s(K)<ns
142         break
143     end
144 end
145 litz_strands_s=n_strands(K-1);
146 % end
147 %end
148 %%Calculate loss
149 Lenpw=MLT*np;%Length of primary wire
150 dc=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a)./39); %Diameter of strand %%
151 Resdc1= (Lenpw*rho)/(pi*dc^2/4);% Resistance of primary 1 wire
152 Rdc_p= Resdc1/litz_strands_p; %Resistance of primary wire
153 Pdc_p= Ip^2*Rdc_p;% DC power loss
154 Fr=1 + ((pi^2*w^2*(mu)^2*np^2*(litz_strands_p).^2*(dc).^6)/(768*rho^2*(
    BWindA).^2));%Pac/Pdc
155 Ppw=Pdc_p*Fr; % AC power loss in primary wire
156
157 Lensw=MLT*ns;%Length of secondary wire
158 dc=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a)./39); %Diameter of strand %%
159 Resdc1s= (Lensw*rho)/(pi*dc^2/4);% Resistance of 1 wire
160 Rdc_s= Resdc1s/litz_strands_s;
161 Pdc_s= Is^2*Rdc_s;% DC power loss
162 Fr=1 + ((pi^2*w^2*(mu)^2*ns^2*(litz_strands_s).^2*(dc).^6)/(768*rho^2*(
    BWindA).^2));%Pac/Pdc
163 Psw=2*Pdc_s*Fr; % AC power loss in secondary wire
164
165 Pcu=Ppw+Psw; %Loss in Cu
166 Ptot_tf= Pcu+Pc; % Total loss

```

```

167
168 fprintf('\nTransformer parameters \n',Lm);
169 fprintf('n= %f\n',n);
170 fprintf('Np= %f\n',np);
171 fprintf('Ns= %f\n',ns);
172 fprintf('Ip= %f A\n',Ip);
173 fprintf('Is= %f A\n',Is);
174 fprintf('Primary strands= %i and secondary strands= %i\n',
        litz_strands_p, litz_strands_s);
175 fprintf('Loss of core= %f W \n', Pc);
176 fprintf('Loss of primary wire= %f W and Loss of secondary wire= %f W\n',
        Ppw, Psw);
177 fprintf('Transformer total loss= %f W \n \n', Ptot_tf);
178
179 %%%%%%%%%%          Inductor          %%%%%%%%%%%%%%%
180 I=Ir*sqrt(2); %Max Current
181 %-----
182 %Cores of different size and different gap size
183 cores = [....
184         'RM08A100' ; 'RM08A160' ; 'RM08A250' ; 'RM08A315' ; 'RM08A400' ; ....
185         'RM10A160' ; 'RM10A250' ; 'RM10A315' ; 'RM10A400' ; 'RM10A630'];
186 %AL is mH for 1000 Turns
187 Al = [100 ; 160 ; 250 ; 315 ; 400;...
188       160 ; 250 ; 315 ; 400; 630];
189 % A is effective core area in cm^2
190 A= [0.63 ; 0.63 ; 0.63;0.63 ; 0.63;...
191     0.83 ; 0.83 ; 0.83 ; 0.83;0.83 ];
192 %core volume in m^3
193 V= [ 2.440 ; 2.440 ; 2.440 ;2.440 ;2.440;...
194     4.310 ;4.310 ;4.310 ;4.310 ;4.310]*10^-6;
195 MLT=[ 42; 42; 42; 42; 42;
196     52 ; 52 ;52 ;52 ;52]*10^-3;
197 % Rth is core thermal resistance in deg. C / W
198 Rth= [38 ; 38 ;38 ;38 ;38 ;
199     30; 30; 30; 30; 30];
200 Bbob=[8.6; 8.6; 8.6; 8.6; 8.6; 10; 10; 10; 10; 10]*10^-3;

```

```

201 hbob=[3.475; 3.475; 3.475; 3.475; 3.475; 4.25; 4.25; 4.25; 4.25;
      4.25]*10^-3;
202 BWindA=[ 10.8; 10.8; 10.8; 10.8; 10.8; 12.1; 12.1; 12.1; 12.1;
      12.1]*10^-3;
203 %-----
204 for i = 1:5
205
206     N(i)=round(1000*sqrt(1000*L/Al(i))); % Number of turns of wire
207     Bpk(i)=(Al(i)*N(i)*I/A(i))*1e-2; % Peak B
208     Pv(i)= (Cm(fv)*((f)^x(fv))*(Bpk(i)*10^-3)^(y(fv))*(ct0(fv)-ct1(fv)*T
      +ct2(fv)*T^2))*1e3;
209     Pc(i)=Pv(i)*V(i); % Power loss in core
210     %-----
211     %To find which strand wire can fit
212     for j=1:length(od_litz)
213
214         n_turns_b(j)= floor(Bbob(i)/(od_litz(j))) ; %Number of wires
      that can fit in the breadth of core
215         n_turns_h(j)=floor(hbob(i)/(od_litz(j)));
216         n_turns(j)= n_turns_b(j)*n_turns_h(j); % Total number turns that
      can fit in the core
217
218         if n_turns(j)<N(i) %The number of turns tha can fit decreases as
      overall diameter of wire increases
219             break % When the number of turns is less than
      the required turns break the loop
220         end
221     end
222
223     if j==1
224         disp('Litz cant fit '); %if litz wire can not fit at all
225         j=2; %For consistency of the code
226     end
227     litz_strands(i)=n_strands(j-1);
228     %-----
229     dw=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a)./39); %Diameter of strand

```

```

230     Aw=pi*(dw)^2/4;
231     lengthw(i)= MLT(i)*N(i); %Lenght of wire
232     Resdcl(i)=rho*lengthw(i)/Aw;%DC Resistance of one wire
233     Res(i)= Resdcl(i)/litz_strands(i);% Accounting skin effects
234
235     Fr(i)=1 + ((pi^2*w^2*(mu)^2*N(i)^2*(litz_strands(i)).^2*(dw).^6)
                /(768*rho^2*(BWindA(i)).^2));%Pac/Pdc
236
237     Pw(i)=Ir^2*Res(i)*Fr(i)*2; %Power loss in wire
238     Ptotl(i)= Pc(i)+Pw(i); %Total power loss
239     Ptotal(i)=Pc(i)+Pw(i) ; %Only accepted ones
240
241 end
242 [minP, In]=min(Ptotal);
243 P1=minP;
244
245 disp(['Inductor parameters'] );
246 disp(['The total loss is ',num2str(Ptotal(In)),'W. The core loss is ',
        num2str(Pc(In)),'W and the copper loss is ', num2str(Pw(In)),'W'] );
247 disp(['Using ',cores(In,:),' core. ', num2str(Wawg_a),'AWG wire with ',
        num2str(N(In)),' turns and of ',num2str(lengthw(In)),'m length.
        There are ', num2str(litz_strands(In)),' strands in parallel' ]);
248 %
249 %%%%%%%%%%% Magnetizing inductor %%%%%%%%%%%
250 Im_max=Im*sqrt(2)*1.1; %Max Current
251 %-----
252 for i = 1:5
253
254     N(i) = round(1000*sqrt(1000*Lm/Al(i))); % Number of turns of wire
255     B(i)= (Al(i)*N(i)*Im_max/A(i))*1e-2; % Peak B
256     Pv(i)= (Cm(fv)*((f)^x(fv))*(B(i)*10^-3)^(y(fv))*(ct0(fv)-ct1(fv)*T+
                ct2(fv)*T^2))*1e3;
257     Pc(i)=Pv(i)*V(i); % Power loss in core
258     %-----
259     %To find which strand wire can fit
260     for j=1:length(od_litz)

```

```

261     n_turns_b(j)= floor(Bbob(i)/(od_litz(j))) ; %Number of wires
           that can fit in the breadth of core
262     n_turns_h(j)=floor(hbob(i)/(od_litz(j)));
263     n_turns(j)= n_turns_b(j)*n_turns_h(j); % Total number turns that
           can fit in the core
264
265     if n_turns(j)<N(i) %The number of turns tha can fit decreases as
           overall diameter of wire increases
266         break           % When the number of turns is less than
           the required turns break the loop
267     end
268 end
269
270 if j==1
271     disp(['Litz cant fit ']); %if litz wire can not fit at all
272     j=2; %For consistency of the code
273 end
274 litz_strands(i)=n_strands(j-1);
275 %-----
276 %Power loss
277 dw=(2.54e-2)* 0.0050.*(92).^((36.-Wawg_a)./39); %Diameter of strand
278 Aw=pi*(dw)^2/4;
279 lengthw(i)= MLT(i)*N(i); %Lenght of wire
280 Resdcl(i)=rho*lengthw(i)/Aw;%DC Resistance of one wire
281 Res(i)= Resdcl(i)/litz_strands(i);% Accounting skin effects
282 Fr(i)=1 + ((pi^2*w^2*(mu)^2*N(i)^2*(litz_strands(i)).^2*(dw).^6)
           /(768*rho^2*(BWindA(i)).^2));%Pac/Pdc
283 Pw(i)=Im^2*Res(i)*Fr(i); %Power loss in wire
284 Ptot(i)=Pc(i)+Pw(i) ; %Total power loss
285 end
286 [minP, In]=min(Ptot);
287 P=minP;
288 Pcore=Pc(In);
289 Pwire=Pw(In);
290 flux=B(In);
291 turns=N(In);

```



```

292 disp([' ' ] );
293 disp('Magnetizing Inductor parameters' );
294 disp(['The total loss is ',num2str(Ptota(In)), 'W. The core loss is ',
      num2str(Pc(In)), 'W and the copper loss is ', num2str(Pw(In)), 'W'] );
295 disp(['Using ',cores(In,:), ' core. ', num2str(Wawg_a), 'AWG wire with ',
      num2str(N(In)), ' turns and of ',num2str(lengthw(In)), 'm length.
      There are ', num2str(litz_strands(In)), ' strands in parallel' ]);
296 %%%%%%%%%%% Transistors %%%%%%%%%%%
297 Irms=Ir/sqrt(2);%Approximating rms current in switch
298 Im_off=Ir*sqrt(2)*sin(deg2rad(theta)); %Current at turn off
299 %%for epc 2010
300 Rds=25*10^-3; %at 5V
301 Coss= 350*10^-12; %output capacitance
302 tf= 10*10^-9; %fall time
303 %Power loss
304 P_cond2=Irms^2*Rds;%Conduction loss
305 P_off2=Im_off^2*tf^2*f/(48*Coss);%Turn off loss
306 P_tot2=4*(P_cond2+P_off2);
307 disp([' ' ] );
308 disp(['Transistor parameters'] );
309 disp(['The total loss is ',num2str(P_tot2), 'W. With condcution loss as '
      ,num2str(4*P_cond2), 'W and switching loss as ',num2str(4*P_off2), 'W.
      ']),
310 disp(['Voltage rating ',num2str(Vinnom), 'V'] );
311 %%%%%%%%%%% Diodes %%%%%%%%%%%
312 Iav=Io/2; %Average current
313 Vf=0.5; %Forward volage drop of switch
314 %Power loss
315 P_diode=Iav*Vf;
316 P_diode_all=2*P_diode;
317 disp(' ' );
318 disp(['Diode parameters'] );
319 disp(['The total loss is ',num2str(P_diode_all), 'W.'])
320 disp(['Voltage rating ',num2str(2*Vo), 'V. Current rating ', num2str(Iav
      ), 'V.']);

```


Appendix B

Design of Low-cost Converters: Schematic, PCB Layout, Components Used and Code for Source and Load Converter

This appendix provides schematics and images of the PCB for the source converter (Fig. B-1, B-2), flyback load converter (Fig. B-4, B-5) and capacitive isolated converter (Fig. B-7, B-8). The components used are also detailed. Also, the code used to design the converters and the control feedback is provided.

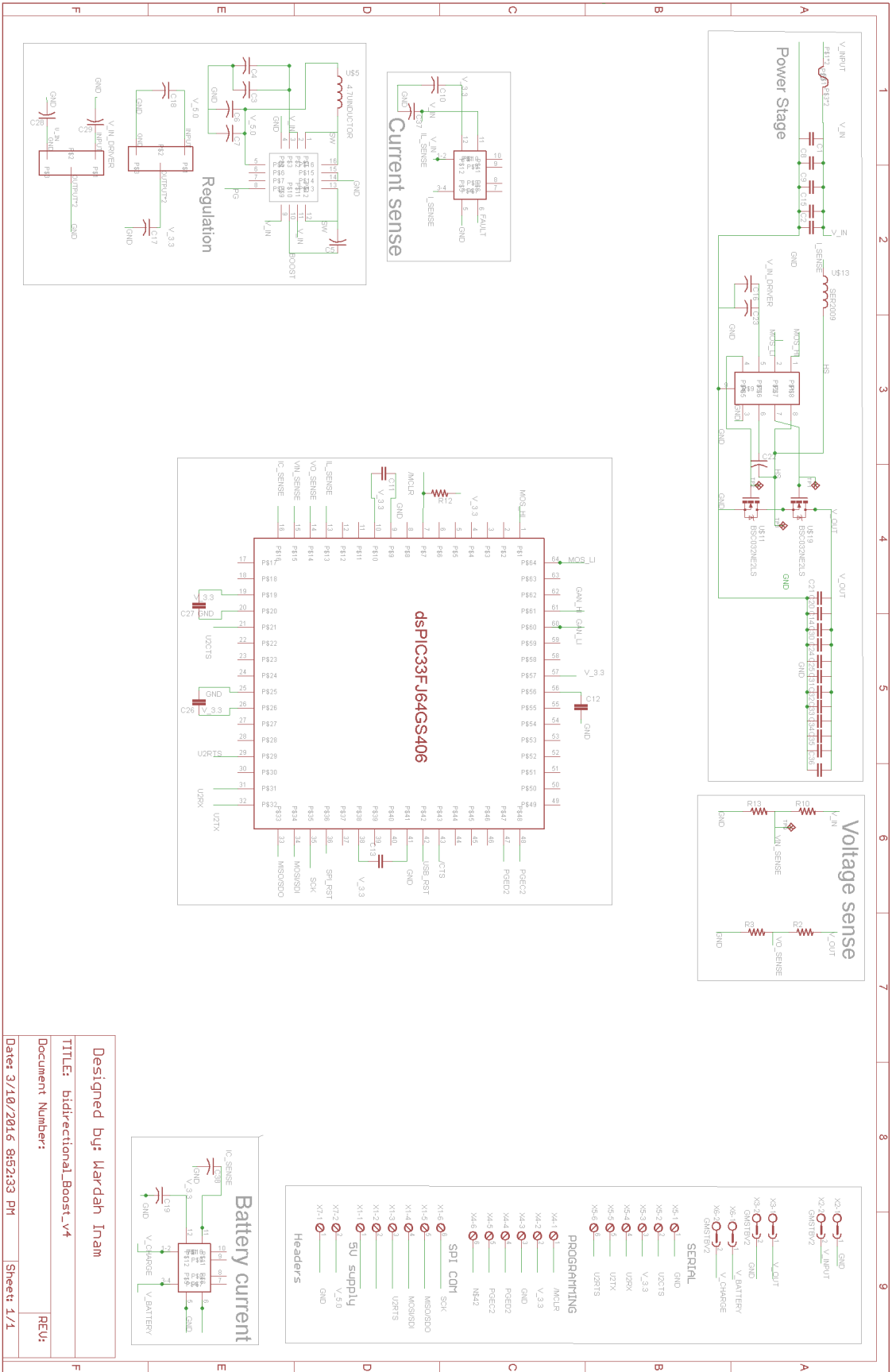


Figure B-1: Source converter (synchronous boost) schematic.

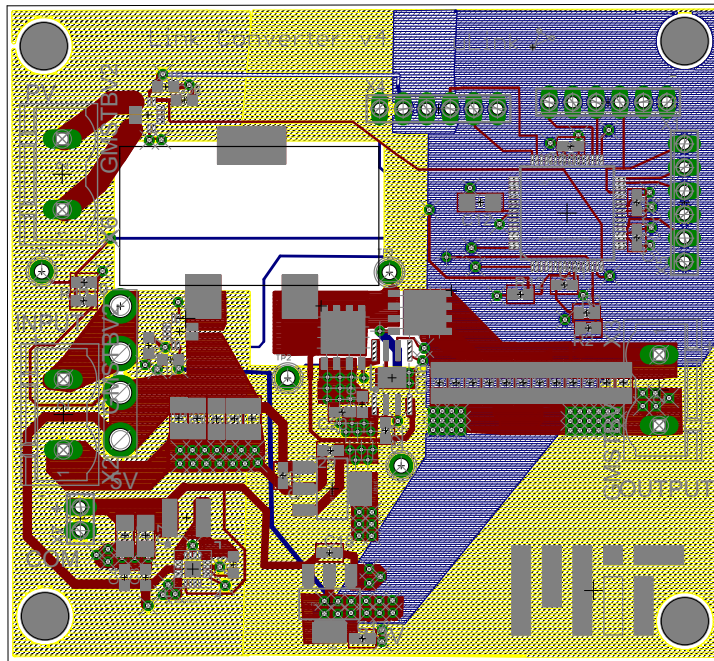


Figure B-2: Source converter PCB layout with four layers (zoomed 2.5x).

Item Qty	Ref Des	Manufacturer	Mfg Part #	Dist Part #	Description	Package	Type	Cost	Total Cost
1	3 X2.X3.X6	On Shore Technology Inc	OOSTO0020151	ED2950-ND	TERM BLOCK HDR 2POS R/A 7.62MM		Through Hole	0.148	0.444
2	3 X2.X3.X6	On Shore Technology Inc	OOSTJ020150	ED2920-ND	TERM BLOCK PLUG 2POS STR 7.62MM		Free hanging	0.45	1.35
3	2 U10, U17	Allegro Microsystems, LLC	ACS711KEKLT-15AB-T	620-1483-2-ND	SENSOR CURRENT HALL 15.5A AC/DC		12-W/FOFN	0.448	0.896
4	C10, C11, C13, C19, C22, C26, C27, C37	Samsung Electro-Mechanics	CL10F104Z88NNNC	1276-1012-2-ND	CAP CER 0.1UF 50V Y5V 0603		603 smt	0.002	0.0192
5	2 U11, U19	Infinion Technologies	BSC093N04LS G	BSC093N04LS GTR-ND	MOSFET N-CH 40V 49A TDSO8		8-PowerTDFN smt	0.246	0.4914
6	7 C1, C2, C6, C7, C8, C9, C15	Murata Electronics North Am	GRM31CR61E226KE15L	490-5527-2-ND	CAP CER 22UF 25V 10% X5R 1206		1206 smt	0.112	0.784
7	1 U1	Littelfuse Inc	01000057Z	F4082-ND	FUSE CLIP BLADE 125V 15A PCB		ATO	0.068	0.068
8	1 U1	Littelfuse Inc	0287030.PXCX	F4202-ND	FUSE AUTOMOTIVE 30A 32VDC BLADE		Through Hole	0.116	0.116
9	1 U9	Texas Instruments	UCC27201ADPAR	296-28428-2-ND	IC DVR HIGH/LOW SIDE 3A 8SOPWR		8-SOIC	1.38	1.38
10	C3, C4, C16, C17, C18, C23, C28, C29	Murata Electronics North Am	GRM188R61E105KA12D	490-3897-2-ND	CAP CER 1UF 25V 10% X5R 0603		603 smt	0.004	0.0344
11	1 U13	Colicraft	SER2013-472MLB	994-SER2013-472MLB	Fixed Inductors SER2013 4.7 uH		smt	0.89	0.89
12	C14, C20, C21, C24, C25, C30, C31, C32, C33, C34, C35, C36, C12	Samsung Electro-Mechanics	CL31A106KBHNNNE	1276-2876-1-ND	CAP CER 10UF 50V 10% X5R 1206		1206 smt	0.068	0.884
13	1 U7	Microchip Technology	DSPIC33FJ64GS406-IP	DSPIC33FJ64GS406-IP-T-ND	IC DSC 16BIT 64KB FLASH 64TQFP		64-TQFP	3.83	3.83
14	1 R3	Panasonic Electronic Compon	ERA-3AEB102V	P1.0KDBTR-ND	RES SMD 1K OHM 0.1% 1/10W 0603		603 smt	0.038	0.038
15	1 R13	Panasonic Electronic Compon	ERA-3AEB202V	P2.0KDBTR-ND	RES SMD 2K OHM 0.1% 1/10W 0603		603 smt	0.029	0.029
16	3 R2, R10, R12	Panasonic Electronic Compon	ERA-3AEB103V	P1.0KDBTR-ND	RES SMD 10K OHM 0.1% 1/10W 0603		603 smt	0.029	0.087
17	1 U4	Semtech Corporation	TS30011-M050QFN	TS30011-M050QFN-RCT-ND	IC REG BUCK 5V 1A SYNC 16-VQFN		16-VQFN	0.325	0.325
18	1 U5	Taiyo Yuden	NRS5020T4R7MMGJ	587-2407-2-ND	FIXED IND 4.7UH 2A 72 MOHM SMD		smt	0.115	0.115
19	1 C5	Murata Electronics North Am	GRM188R71C223KA01D	490-1527-2-ND	CAP CER 0.022UF 16V X7R 0603		603 smt	0.007	0.0068
20	1 U6	Texas Instruments	LM2940MPX-10/NOPB	LM2940MPX-10/NOPB-ND	IC REG LDO 10V 1A SOT223		SOT223	0.818	0.818
21	1 U6	Texas Instruments	TLV111TLV33DCYR	296-28778-2-ND	IC REG LDO 3.3V 1A SOT223		SOT223	0.196	0.196
22	2 X1, X4	Harwin Inc	M20-9990646	952-2270-ND	SIL VERTICAL PC TAIL PIN HEADER		Through hole		
23	1 X7	On Shore Technology Inc.	OOSTVNO2A150	ED10561-ND	CONN TERM BLOCK 2.54MM 2POS PCB		Through hole		

Figure B-3: Bill of Materials of source converter.

```

1 %% This file determines the controller for the source converter
2 clc
3 clear all
4
5 %%Inputs
6 %Converter Specifications
7 Vin_min=10;Vin_max=15;Vin_nom=12;
8 Vout_min=24; Vout_max=30; Vout_nom=24;
9 P=250;
10 C=200*10^-6; %output capacitor
11 L=4e-6;
12 fs=0.5e6;
13 %Inner Loop Specifications
14 Hi=1; %Current gain
15 Vs=3.3;
16 fci=fs/10;
17 %Outer Loop Specifications
18 fcv=fs/50;
19 Hv=0.1;
20 %%
21 %Calculate Converter Specifications
22 D=1-(Vin_nom/Vout_nom);
23 Dn=1-D;
24 R=Vout_nom^2/P;
25 Iin= P/Vin_nom;
26 IL=Iin;
27 %Current loop controller
28 Gid=tf([C*Vout_nom IL*2*Dn], [L*C L/R Dn^2]);
29 % [Gm_id,Pm_id,Wgm_id,Wpm_id] = margin(Gid);
30 TOLiwoutc=Gid*Hi*(1/Vs) %TF of open current loop without controller
31 % opts=pidtuneOptions('PhaseMargin',60)
32 [Gci,infoi]=pidtune(TOLiwoutc,'pi',fci)
33 TOLi=Gci*TOLiwoutc
34 bode(Gid,'b')
35 hold on

```

```

36 bode(TOLi, 'k')
37 legend('Gid', 'TOLi')
38 grid on
39
40 h1 = findobj(gcf, 'Color', 'b', '-and', 'linestyle', '-'); set(h1, 'linewidth'
    , 1.5, 'color', [0.6 0.2 0.2]);
41 h2 = findobj(gcf, 'Color', 'k', '-and', 'linestyle', '-'); set(h2, 'linewidth'
    , 1.5, 'color', [0.6 0.6 0.6]);
42 %h3 = findobj(gcf, 'Color', 'r', '-and', 'linestyle', '-'); set(h3, 'linewidth'
    , 1.5, 'color', [0 0 0]);
43 legend([h1(1) h2(1)], 'Gid(s)', 'Ti(s)', 'Location', 'northeast')
44 %%
45 %Voltage Loop controller
46 Gvi=tf([1-D], [C 1/R]);
47 TOLvwoutc=Gvi*Hv %TF of open current loop without controller
48 [Gcv, infov]=pidtune(TOLvwoutc, 'pi', fcv)
49 TOLv=Gcv*TOLvwoutc
50 figure
51 bode(Gvi, 'b')
52 hold on
53 bode(TOLv, 'k')
54 legend('Gvi', 'TOLv')
55 grid on
56
57 h1 = findobj(gcf, 'Color', 'b', '-and', 'linestyle', '-'); set(h1, 'linewidth'
    , 1.5, 'color', [0.6 0.2 0.2]);
58 h2 = findobj(gcf, 'Color', 'k', '-and', 'linestyle', '-'); set(h2, 'linewidth'
    , 1.5, 'color', [0.6 0.6 0.6]);
59 legend([h1(1) h2(1)], 'Gvi(s)', 'Tv(s)', 'Location', 'northeast')
60 figure
61 %Complete two loop control
62 TOL=(TOLi/(1+TOLi))*TOLv
63 [Gm, Pm, Wgm, Wpm] = margin(TOL)
64 bode(TOL, 'k')
65 legend('TOL')
66 grid on

```



```
67 h2 = findobj(gcf, 'Color', 'k', '-and', 'linestyle', '-'); set(h2, 'linewidth'  
    , 1.5, 'color', [0.6 0.6 0.6]);  
68 legend([h2(1)], 'T(s)', 'Location', 'northeast')
```

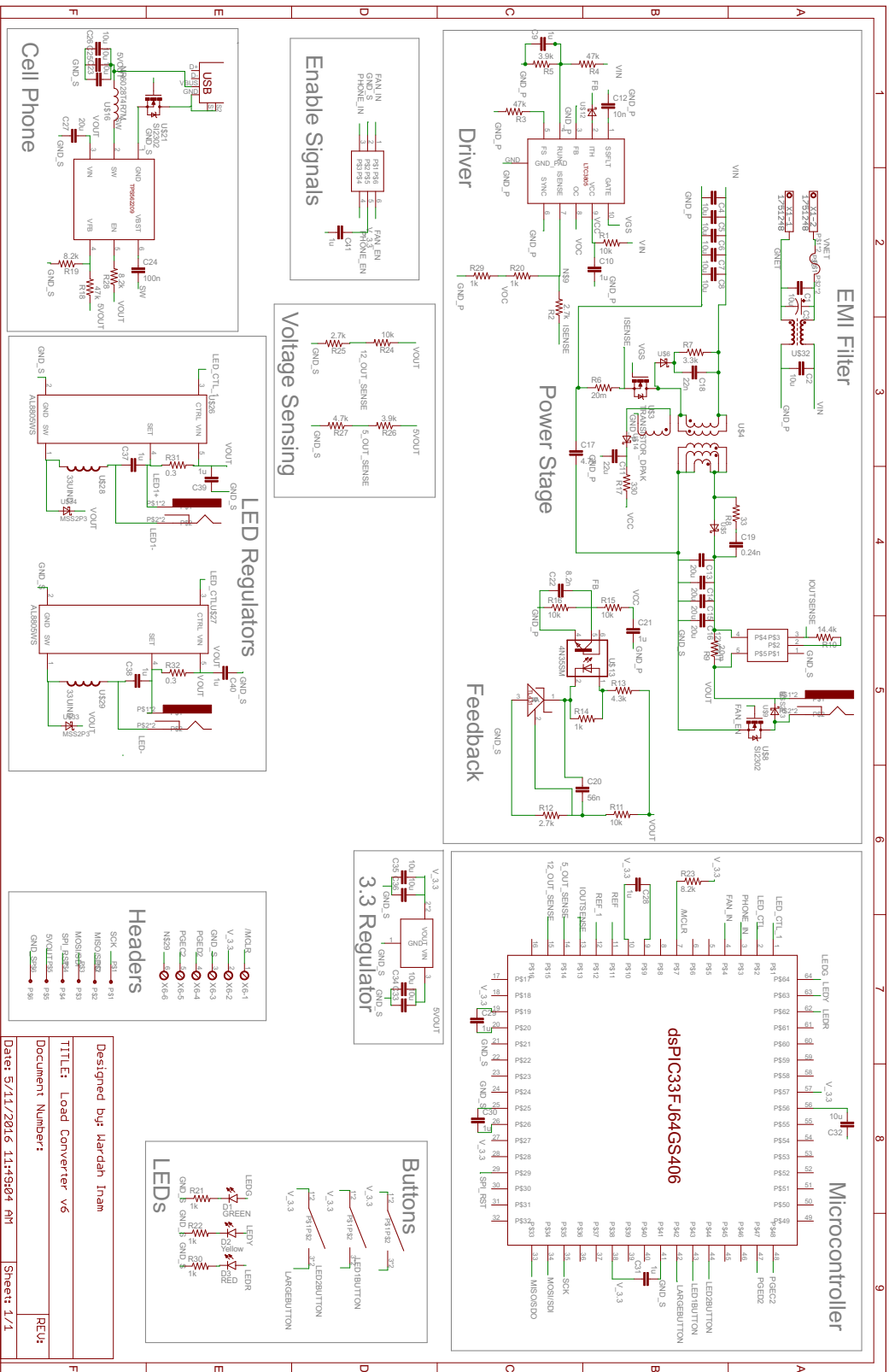


Figure B-4: Load converter (flyback) schematic.

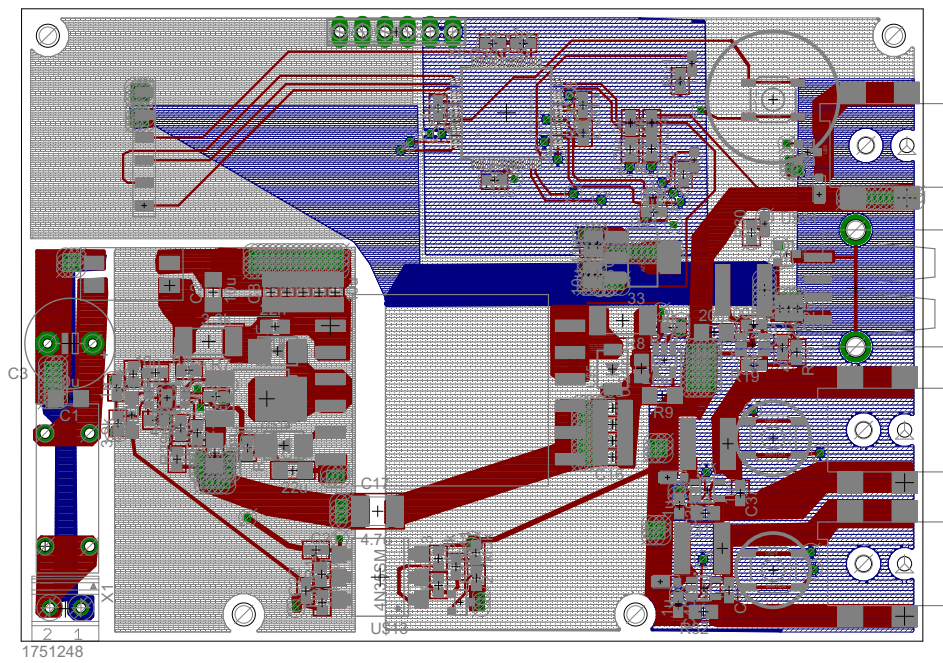


Figure B-5: Load converter PCB layout with four layers (zoomed 2.4x).

Item #	Qty	Ref Des	Mfg Part #	Dist. Part #	Description	Package	Type	Cost/Unit	Cost
1	7	C1,C2,C4,C5,C6,C7,C8	Samsung Electro-Mechanics	C131A106KBHNNNE	CAP CER 10UF 50V 10% X5R 1206	1206	smt	0.068	0.476
2	0	C3							0
3	12	C3,C38,C39,C40,C41	Yageo		CAP CER 1UF 16V Y5V 0603	603	smt	0.0047	0.0564
4	6	C11,C13,C14,C15,C16,C27	Samsung Electro-Mechanics	C131A228MOCULNNC	CAP CER 22UF 16V X5R 1206	1206	smt	0.054	0.324
5	1	C12	Samsung Electro-Mechanics	CL10B103KANNNC	CAP CER 10000PF 25V 10% X7R 0603	603	smt	0.0027	0.0027
6	1	C17	Murata Electronics North Am	GA3430R76D42MWO1L	CAP CER 4700PF 250V/AC X7R 1812	1812	smt	0.144	0.144
7	1	C18	TDK Corporation	C2012R7E2A223K125AA	CAP CER 0.022UF 100V X7R 0805	805	smt	0.02	0.02
8	1	C19	Murata Electronics North Am	GM2165C2A241JA01D	CAP CER 240PF 100V NP0 0805	805	smt	0.023	0.023
9	1	C20	Murata Electronics North Am	GM189R71E563KA01D	CAP CER 0.056UF 25V X7R 0603	603	smt	0.017	0.017
10	1	C22	TDK Corporation	C160C00G1E8221080AA	CAP CER 8200PF 25V C0G 0603	603	smt	0.049	0.049
11	8	C25,C26,C32,C33,C34,C3	Murata Electronics North Am	GM189C81A106MA73D	CAP CER 10UF 10V 20% X6S 0603	603	smt	0.06928	0.55424
12	1	C24	Samsung Electro-Mechanics	CL10F104Z88NNNC	CAP CER 0.1UF 50V Y5V 0603	603	smt	0.0025	0.0025
13	1	D1	Lite-On Inc.	LTST-C191KSKT	LED GREEN CLEAR 0603 SMD	603	smt	0.028	0.028
14	1	D2	Lite-On Inc.	LTST-C191KSKT	LED YELLOW CLEAR 0603 SMD	603	smt	0.03	0.03
15	1	D3	Lite-On Inc.	LTST-C191RKT	LED RED CLEAR 0603 SMD	603	smt	0.028	0.028
16	5	R1,R11,R15,R16,R24	Yageo	RC0603JR-0710KL	RES SMD 10K OHM 5% 1/10W 0603	603	smt	0.0009	0.0045
17	2	R12,R25	Yageo	RC0603JR-072KTL	RES SMD 2.7K OHM 5% 1/10W 0603	603	smt	0.0009	0.0018
18	3	R3,R4,R18	Yageo	RC0603JR-0747KL	RES SMD 47K OHM 5% 1/10W 0603	603	smt	0.0009	0.0027
19	2	R5,R26	Yageo	RC0603JR-073K9L	RES SMD 3.9K OHM 5% 1/10W 0603	603	smt	0.0009	0.0018
20	2	R6,R9	Stackpole Electronics Inc	CSR1206FK20L0	RES SMD 0.02 OHM 1% 1/2W 1206	1206	smt	0.0683	0.166
21	1	R7	TE Connectivity AMP Connect	6-2176070-1	RES SMD 3.9K OHM 1% 2W 2512	2512	smt	0.1	0.1
22	1	R8	Stackpole Electronics Inc.	RMCF2512J13980T	RES SMD 33 OHM 5% 1W 2512	2512	smt	0.024	0.024
23	1	R10	Yageo	RC0603FR-0717K9L	RES SMD 17.8K OHM 1% 1/10W 0603	603	smt	0.0012	0.0012
24	1	R13	Yageo	RC0603FR-074K3L	RES SMD 4.3K OHM 5% 1/10W 0603	603	smt	0.0009	0.0009
25	7	R2,R14,R20,R21,R22,R29,R30	Yageo	RC0603JR-071K1L	RES SMD 1K OHM 5% 1/10W 0603	603	smt	0.0009	0.0063
26	1	R17	Yageo	RC0603JR-073K9L	RES SMD 8.2K OHM 5% 1/10W 0603	603	smt	0.0009	0.0009
27	3	R19,R23,R28	Yageo	RC0603JR-074K3L	RES SMD 4.3K OHM 5% 1/10W 0603	603	smt	0.0009	0.0027
28	1	R27	Yageo	RC0603JR-074K3L	RES SMD 4.7K OHM 5% 1/10W 0603	603	smt	0.0009	0.0009
29	2	R31,R32	Yageo	RC0603FR-073K9L	RES SMD 0.3 OHM 1% 1/8W 0805	805	smt	0.0718	0.1436
30	1	R1	Bel Fuse Inc.	210-3-R	FUSE GLASS 3A 350VAC 1.40VDC 2AG	2AG	Free Hanging	0.08	0.08
31	2	U1	Litefuse Inc.	01110501Z	FUSE CLIP CARTRIDGE 250V 10A PCB	2AG	Through Hole	0.05	0.1
32	1	U2	Linear Technology	LTCS050HMSF-5#PBF	C REG CTRLR BST FLYBK CM 10MSOP	10-TFSOP	fine pitch	1.69	1.69
33	1	U3	Fairchild Semiconductor	FDD390N15A	DIODE SCHOTTKY 150V 26A DPAK	TO-252 (D-Pak)	smt	0.472	0.472
34	1	U4	Colcraft	FA2900-ALB	Power Transformers FA2900 Flyback For TLIM5072		smt	1.89	1.89
35	1	U5	NXP Semiconductors	PMEG6020P-115	DIODE SCHOTTKY 60V 3A SOD128	SOD-128	smt	0.123	0.123
36	1	U6	NXP Semiconductors	SS110-1P-TR-ND	DIODE SCHOTTKY 100V 1A SMA	DO-214AC, SMA	smt	0.035	0.035
37	1	U7	Diodes Incorporated	ZXCT1100M5-7	Current & Power Monitors & Regulators Aut	SOT23-3	smt	0.544	0.544
38	2	U8,U33,U34	Alpha & Omega Semicond	AOC3414	MOSFET N-CH 20V 4.2A SOT23	SOT23-3	smt	0.054	0.108
39	3	U9	Vishay Semiconductor Diode	MSS2P3-MA/89A	DIODE SCHOTTKY 30V 2A MICROSMP	MicroSMP	smt	0.045	0.135
40	1	U10	NXP Semiconductors	74LVCG64GW-Q100H	IC DUAL INVERTER	SOT363	smt	0.054	0.054
41	1	U11	Texas Instruments	TL431AIDBR	IC VREF SHUNT ADJ SOT23-3	SOT-23-3	smt	0.08	0.08
42	1	U12	Micro Commercial Co	MBRX1201PMSTR-ND	DIODE SCHOTTKY 20V 1A SOD123	SOD123	smt	0.048	0.048
43	1	U13	Fairchild Semiconductor	4N27SR2M	OPTOISO 7.5KV TRANS W/BASE 6SMD	6-SMD	smt	0.171	0.171
44	1	U14	Diodes Incorporated	B160A-13-F	DIODE SCHOTTKY 60V 1A SMA	DO-214AC, SMA	smt	0.045	0.045
45	1	U15	Texas Instruments	TPS563209DDCT	DC-DC CONV 60V 1A SMA	DO-214AC, SMA	smt	0.599	0.599
46	1	U16	Taiyo Yuden	NR6028TR7M	DIODE SCHOTTKY 60V 1A SMA	SOT-6	smt	0.091	0.091
47	3	U17,UH9,U22	CU Inc.	PJ-0024H-SMT-TR	FIXED IND 4.7UH 3A 40.3 MOHM SMD	non standard	smt	0.576	1.728
48	1	U18	Microchip Technology	DSPIC33FJ64GS406-I/P	CONN POWER JACK 2.1X5.5MM HI CUR	Type A	fine pitch	3.83	3.83
49	1	U20	Diodes Incorporated	NZ1117CH-3.3TRG1	C REG LDO 3.3V 0.8A SOT223	SOT-223	smt	0.067	0.067
50	3	U23,U24,U25	Panasonic Electronic Compd	EEVQ-QP202	SWITCH TACTILE EPCF-NO 0.02A 15V	non standard	smt	0.136	0.408
51	2	U26,U27	Diodes Incorporated	AL8805W5-7	IC LED Driver DC DC Regulator Analog, PWM	SOT-25	smt	0.315	0.63
52	2	U28,U29	Land Signal Integrity Product	TS56045330M-10	FIXED IND 33UH 1.45A 137 MOHM	non standard	smt	0.144	0.288
53	1	U30	4uoon	19886	Header - 6-pin Female, USB, 0.1", Right Ang	non standard	smt	0.86	0.86
54	1	U31	Assmann WSW Component	ALU11006	Connector Receptacle USB TypeA 1.1 4 Pol	USB-A	smt	0.327	0.327
55	1	U32	Bourris Inc.	SRF0905-100V	INDUCTOR COMMON MODE 10UH 1.6A	Horizontal, 4 PC P	smt	0.478	0.478
56	1	X1	On Shore Technology Inc	OSTO0021251	TERM BLOCK HDR 2POS RA 3.5MM	non standard	Through Hole	0.126	0.126
57	1	X1	On Shore Technology Inc	OSTT_J0211530	TERM BLOCK PLUG 2POS STR 3.5MM	non standard	Free Hanging	0.38	0.38

Figure B-6: Bill of Materials of load converter.

```

1 %% Design of load flyback converter with controller
2 clc
3 clear all
4
5 %Inputs
6 Vin=24; Vin_min=24;Vin_max=25;
7 Vout=12;
8 fsw=524e3;
9 Pout=25;
10 Converter_eff= 0.86; %Assumed converter efficiency
11 V_snub=51; %Snubber voltage
12 Dmax=0.5;
13 %Components
14 %Transformer (http://www.coilcraft.com/pdfs/fa2677.pdf)
15 Lm=40e-6; L_leakage=0.01*Lm; C_parisitic=70e-12; n=0.47; % Sec/primary
16 %Diode
17 Vf_diode=0.45; C_diode=80e-12; I_diode_R=80e-6; %PMEG6030EVP; C_diode (
    @25V) ; Ir at 30V
18 %MOSFET
19 % Rdson= 40e-3; Coss=214e-12; Cgs=2200e-12-80e-12; %AOD4126 (100V)
20 Rdson= ((37+76)/2)*1e-3; Coss=130e-12; Cgs=2000e-12-70e-12; Rg=1.1; Qgd
    =13e-9; %AOD482 (100V)
21 %IC
22 Vdd=9.5; Vgs=2.7;
23 %Feedback
24 Rsense=20e-3; nCout=8; Cout=10e-6*nCout; Cout_ESR=0.007/nCout; Gfb=20; %
    Gfb is the gain in the IC and can be changed
25 %% Suggested Values (http://pdfserv.maximintegrated.com/en/an/AN5504.pdf
    )
26 n_sugg=(Vout+Vf_diode)*(1-Dmax)/(Vin_min*Dmax);
27 Dnom_sugg=(Vout+Vf_diode)/(Vin*n_sugg+(Vout+Vf_diode)); % Dnom is the
    same as Dmax as nominal voltage and minimum voltage are the same
28 beta=0.15; %Converter operates in CCM till 15% of full load.
29 Iout=Pout/Vout;
30 Lm_sugg=(Vout+Vf_diode)*(1-Dnom_sugg)^2/(2*Iout*beta*fsw*n_sugg^2);

```

```

31 sprintf('The suggested values are n_s2p=%f and Lm=%dH',n_sugg, Lm_sugg)
32 %Using and off the shelf flyback converter with the closest ratings,
    FA2900
33 sprintf('The used values are n_s2p=%f and Lm=%dH',0.47, 40)
34 %With these values we get the
35 D = (Vout + Vf_diode)/(Vout+Vf_diode + Vin_min*n);
36 beta= (Vout+Vf_diode)*(1-Dnom_sugg)^2/(2*Iout*Lm*fsw*n_sugg^2);
37 sprintf('The used values give us D=%f and beta =%f',D, beta)
38 %% Used Values
39
40 Ip_ripple= Vin*D/(fsw*Lm);           %Primary Ripple Current
41 Iin = Iout*n*D/((1-D)*Converter_eff); %Primary DC Current
42 Ip_pk = (Iin/D) + (Ip_ripple/2);    %Primary Peak to Peak Current
43 %Ip_pk2=(Iout*n/((1-D)*Converter_eff))+(Vin_min*D)/(2*Lm*fsw); This was
44 %from maxim ap note with added converter efficiency.
45 Ip_rms = sqrt(D)*sqrt((Ip_pk^2 + ((Ip_ripple^2)/3) - (Ip_pk*Ip_ripple)))
    ; %Primary RMS
46 sprintf('The rms current at the primary, Ip_rms=%f and the peak current,
    Ip_pk=%f',Ip_rms, Ip_pk)
47 Vds=Vin_max+(Vout+Vf_diode)/n;
48 Vds_max=Vds+Ip_pk*sqrt(L_leakage/Coss);
49 %Snubber
50 %Method 1 : Using Fairchild
51 %V_snub3 = (n*Vout + sqrt((n*Vout)^2 + 2*3e3*L_leakage*fsw*(Ip_pk^2)))
    /2;
52 R_snub=((V_snub*2-n*Vout)^2-(n*Vout)^2)/(2*L_leakage*fsw*Ip_pk^2) %
    Rearranging the equation found in https://www.fairchildsemi.com/
    application-notes/AN/AN-4147.pdf
53 delV_snub=0.025*V_snub;
54 C_snub=V_snub/(R_snub*fsw*delV_snub); %Fairchild
55 sprintf('For a %d V snubber voltage , R_snub=%d ohm and C_snub=%d F is
    used',V_snub, R_snub, C_snub)
56 %Diode Snubber
57 %method 1- http://www.ti.com/lit/an/slua086/slua086.pdf
58 %https://www.fairchildsemi.com/application-notes/AN/AN-6093.pdf
59 V_diode= Vout+Vin_max/n;

```

```

60 L_leakagec_sec=L_leakage*n^2;
61 C_diode_snub=3*C_diode;
62 R_diode_snub=sqrt(L_leakagec_sec/(C_diode));
63 sprintf('The diode snubber Capacitance=%f nF, and Resistance=%f Ohm',
        C_diode_snub*10^9,R_diode_snub)
64 %Output Capacitor (http://www.ti.com/lit/an/slva559/slva559.pdf)
65 V_Cout_ripple=0.01*Vout;
66 delIstep=Vout/15; %Fan switching off
67 delVoutstep=0.5; %0.5V step in voltage
68 Cout_ripple=Iout*D/(V_Cout_ripple*fsw);
69 ESR1=V_Cout_ripple*(1-D)/Iout;
70 Cout_step=delIstep/(2*pi*delVoutstep*fsw/100);
71 %Input Capacitor
72 Vin_ripple=0.01*Vin;
73 C_in=Iin/(D*fsw*Vin_ripple);
74 %%
75 %Losses
76 %MOSFET
77 P_fet_cond=Ip_rms^2*Rdson; %
78 tch=Qgd*Rg/(Vdd-Vgs);%Conduction Loss (http://www.ti.com/lit/an/slua086/slua086.pdf)
79 P_fet_sw=Coss*Vds^2*fsw/2+ Vds*Ip_pk*tch*fsw;
80 P_fet_total= P_fet_cond+P_fet_sw;
81 %Snubber Loss
82 P_snubber=L_leakage*Ip_pk^2*fsw/2 + V_snub^2/R_snub; %http://www.ti.com/lit/an/slua086/slua086.pdf
83 %Diode Loss
84 %(http://www.st.com/st-web-ui/static/active/jp/resource/technical/document/application\_note/DM00044087.pdf)
85 %http://pdfserv.maximintegrated.com/en/an/AN849.pdf
86 P_diode_rev=V_diode*I_diode_R*(D); % Not taking in to account Temp
87 P_diode_cond= Iout*Vf_diode;
88 P_diode_rec=0; %Schottky
89 P_diode_total=P_diode_rev+P_diode_cond+P_diode_rec;
90 %Diode Snubber loss
91 P_diode_snub=C_diode_snub*V_diode^2*fsw; %http://www.ti.com/lit/an/

```

```

    slua086/slua086.pdf
92 %% Feedback
93 %Ref1: (http://cbasso.pagesperso-orange.fr/Downloads/PPTs/Chris%20Basso
    %20APEC%20seminar%202011.pdf)
94 %Ref2: Book:Switch mode power supplies by basso
95 M=Vout/(n*Vin);
96 Rout=Vout^2/Pout;
97 Tau=2*Lm*n^2*fsw/(Rout);
98 Sn=Vin*Rsense*Gfb/Lm; %http://www.switchingpowermagazine.com/downloads
    /5%20Current%20Mode%20Control%20Modeling.pdf
99 Rslope=2.7e3;
100 DelVsense= (D-0.06)*10e-6*Rslope/(0.8);
101 TimeDelVsense=D/fsw;
102 RateDelVsense=DelVsense/TimeDelVsense;
103 Se=RateDelVsense;
104 G0=Rout/((Rsense*Gfb*n)*((1-D)^2/Tau)*(1+2*Se/Sn)+2*M+1); %Assuming Se
    =0
105
106 fz1=1/(2*pi*Cout_ESR*Cout); wz1=2*pi*fz1;
107 fz2=(1-D)^2*Rout/(2*pi*D*Lm*n^2); wz2=2*pi*fz2;
108 fp1=((1-D)^3/Tau)*(1+2*Se/Sn)+1+D)/(2*pi*Rout*Cout); wp1=2*pi*fp1;
109
110 Qp=1/(pi*((1-D)*Se/Sn+0.5-D));
111 wn=pi*fsw;
112 s=tf('s');
113
114 H=(G0*(1+s/wz1)*(1-s/wz2))/((1+s/wp1)*(1+s/(wn*Qp)+s^2/(wn^2)))
115 opts=bodeoptions;
116 opts.FreqUnits='Hz';
117 opts.PhaseMatching='on';
118 opts.PhaseMatchingValue=0; %ref: PLECS_tl431
119 bode(H, {10,1e6}, 'b', opts)
120 %%%%%%%%%%% Design feedback %%%%%%%%%%%
121 fc=fsw/500;
122 [mag1,phase1]=bode(H, 2*pi*fc);
123 dBgain=20*log10(mag1);

```



```

124 sprintf('The magnitdue is %f dB and the phase is %f',20*log10(mag1),
    phase1)
125
126 deggain=60; %P
127 Vreflower=2.5;
128 Ibridge=0.9e-3;
129 Rpullup=5e3;
130 Copto=6e-12;
131 CTR=0.3;
132 k=tand(deggain/2+2*pi*45/360);
133
134 fpf=(tand(deggain)+sqrt(tand(deggain)*tand(deggain)+1))*fc;
135 fzf=fc^2/fpf; %Same as fc^2/fpf =fc/k;
136
137 Gainf=10^(-dBgain/20);%20 db gain
138 Rlower=Vreflower/Ibridge;
139 Rupper=(12-Vreflower)/Ibridge;
140 GR0=Gainf;
141 C1=1/(2*pi*fzf*Rupper);
142 C2=1/(2*pi*fpf*Rpullup);
143 Rled=CTR*Rpullup/GR0;
144
145 Rledmax=(Vout-1-2.5)*Rpullup*CTR/(4.5-0.5+1e-3*CTR*Rpullup); % 4.5=(9/2
    because of pullup resistor) Basso
146 Rledmax2=(Vout-1-2.5)/1.5e-3; %Richtecks condition
147 if Rled>Rledmax | Rled>Rledmax2
148     sprintf('RLed exceeds maximum value')
149 end
150 sprintf('Rupper= %d, Rlower=%d, Rled=%d, C1=%d, C2=%d, Rpullup=%d',
    Rupper, Rlower, Rled, C1, C2, Rpullup)
151
152 iwzr1=C1*Rupper;
153 iwpr1=C1*Rupper;
154 iwpr2=C2*Rpullup;
155
156 Gf=tf([GR0*iwzr1 GR0], [iwpr1*iwpr2 iwpr1 0]);

```

```

157 hold on
158 bode(Gf, 'k');
159 hold on
160 bode(Gf*H, 'r');
161 h1 = findobj(gcf, 'Color', 'b', '-and', 'linestyle', '-'); set(h1, 'linewidth'
    , 1.5, 'color', [0.6 0.2 0.2]);
162 h2 = findobj(gcf, 'Color', 'k', '-and', 'linestyle', '-'); set(h2, 'linewidth'
    , 1.5, 'color', [0.6 0.6 0.6]);
163 h3 = findobj(gcf, 'Color', 'r', '-and', 'linestyle', '-'); set(h3, 'linewidth'
    , 1.5, 'color', [0 0 0]);
164 legend([h1(1) h2(1) h3(1)], 'Converter H(s)', 'Controller Gf(s)', 'Loop T
    (s)', 'Location', 'southwest')
165 grid on

```

```

1 %% This script calculates the EMI filter and plots the bode plots
2 clc
3 clear all
4
5 %Converter Parameters
6 Vg=24; %input voltage
7 V=12; %output voltage
8 P=25; %Output power
9 I=P/Vg; % Input current
10
11 L=40e-6; %Lm
12 n=0.47; %Transformer turns ratio- ns2p
13 D=V/(V+Vg*n); % Duty cycle
14 Di=1-D;
15 R=V^2/P; %output resistance
16 C=60e-6; %output capacitance
17
18 %Line Parameters
19 %L_l=5e-6; %Line inductance
20 %R_l=0.2; %Line resistnace
21

```

```

22 %Filter parameters
23 C_1=10e-6;
24 L_f=8e-6;
25 C_2=60e-6;
26 s=tf('s');
27 %% Finding damping Capacitance and Resistance
28 Zo_mm=0.5; % Peak output impedance
29 R_of=sqrt(L_f/C_2)
30 scaling_factor=R_of^2*(1+sqrt(1+(4*Zo_mm^2/R_of^2)))/(Zo_mm)^2
31 C_d=scaling_factor*C_2;
32 R_d=R_of*sqrt((2+scaling_factor)*(4+3*scaling_factor)/((2*scaling_factor
    ^2)*(4+scaling_factor)))
33
34 %% Middlebrook criteria
35 Ze=s*L/D^2;
36 Zn=(-Di^2*R/(D^2*n^2))*(1-(s*L*D*n^2/(R*Di^2)));
37 Zd=(R*Di^2/(D^2*n^2))*(1+(s*L*n^2/(Di^2*R))+(s^2*L*C*n^2/Di^2))/(1+s*R*C
    );
38
39 %% Filter
40 %X_Ll=s*L_l;
41 X_C2=1/(s*C_2);
42 X_C1=1/(s*C_1);
43 X_Cd=1/(s*C_d);
44 X_Lf=s*L_f;
45
46 a=X_Cd+R_d;
47 b=a*X_C2/(a+X_C2);
48 Zo=b*X_Lf/(b+X_Lf);
49 %%
50 opts = bodeoptions('cstprefs');
51 %opts.PhaseVisible = 'off';
52 opts.FreqUnits = 'Hz';
53
54 num_Gvd=(-Di/n)*(Vg+V/n)+s*L*I/n;
55 den_Gvd=s^2*(L*C)+s*(L/R)+(Di/n)^2;

```

```

56 Gvd=num_Gvd/den_Gvd;
57 bodeplot(Gvd,opts,'b')
58 Gvd_new=Gvd*(1+Zo/Zn)/(1+Zo/Zd);
59 hold on
60 bode(Gvd_new,opts,'k')
61 xlabel('Frequency (rad)');
62 legend('Gvd_original','Gvd_modified');
63 grid on
64
65 h1 = findobj(gcf,'Color','b','-and','linestyle','-'); set(h1,'linewidth'
    ,1.5,'color',[0.6 0.6 0.6]);
66 h2 = findobj(gcf,'Color','k','-and','linestyle','-'); set(h2,'linewidth'
    ,1.5,'color',[0.6 0.2 0.2] );
67 legend([h1(1) h2(1) ], 'Gvd','Gvd new','Zo','Location','southeast')
68 figure
69 %% Plot for paper
70 opts = bodeoptions('cstprefs');
71 opts.PhaseVisible = 'off';
72 opts.FreqUnits = 'Hz';
73 bodeplot(Zn,opts,'b')
74 hold on
75 bodeplot(Zd,opts,'k')
76 hold on
77 bodeplot(Zo,opts,'r')
78 grid on
79 h1 = findobj(gcf,'Color','b','-and','linestyle','-'); set(h1,'linewidth'
    ,1.5,'color',[0.6 0.6 0.6],'linestyle','--');
80 h2 = findobj(gcf,'Color','k','-and','linestyle','-'); set(h2,'linewidth'
    ,1.5,'color',[0.6 0.2 0.2] );
81 h3 = findobj(gcf,'Color','r','-and','linestyle','-'); set(h3,'linewidth'
    ,1.5,'color',[0 0 0]);
82 legend([h1(1) h2(1) h3(1) ], 'Zn','Zd','Zo','Location','southeast')

```

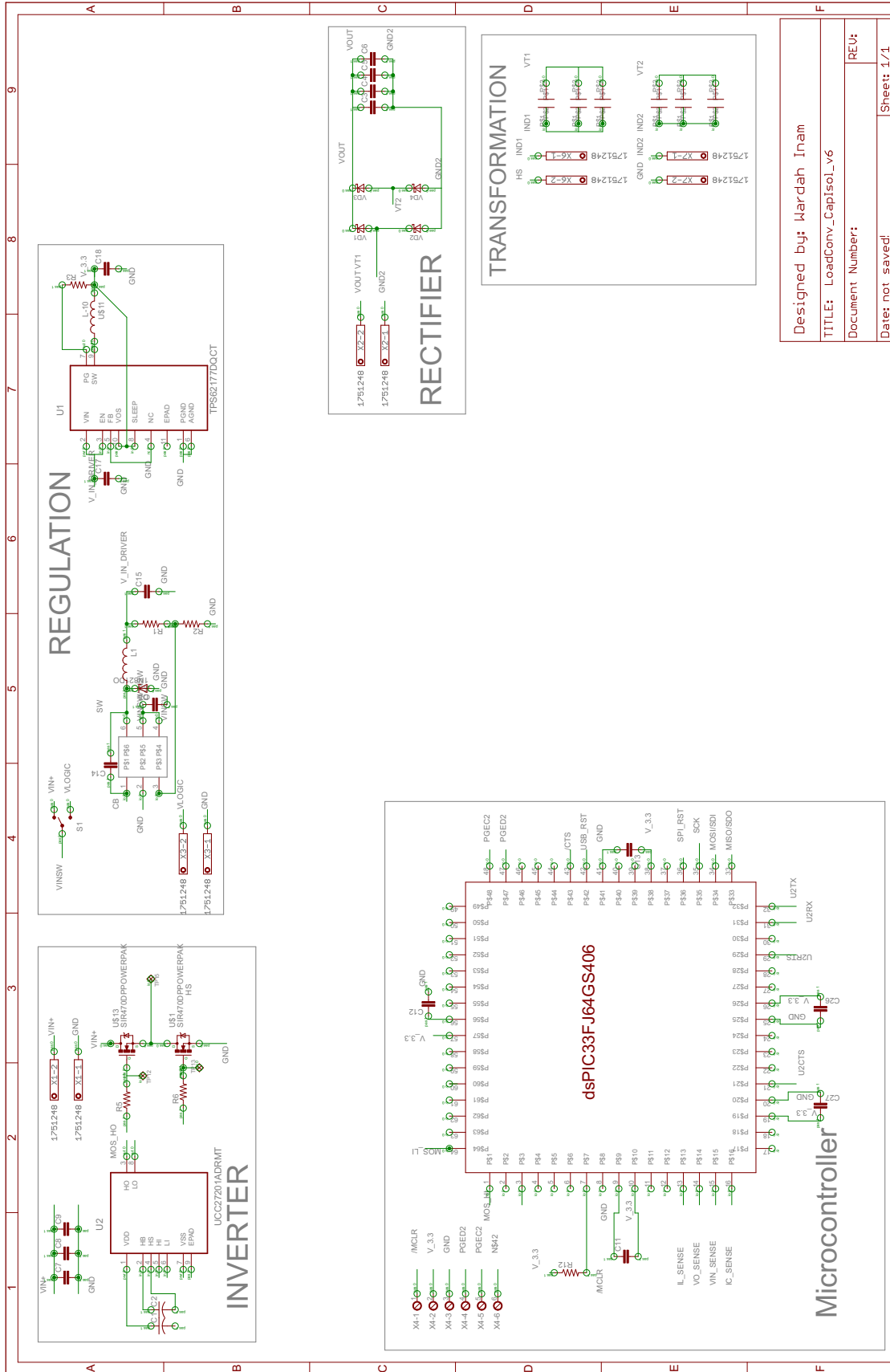


Figure B-7: Capacitively isolated load converter schematic

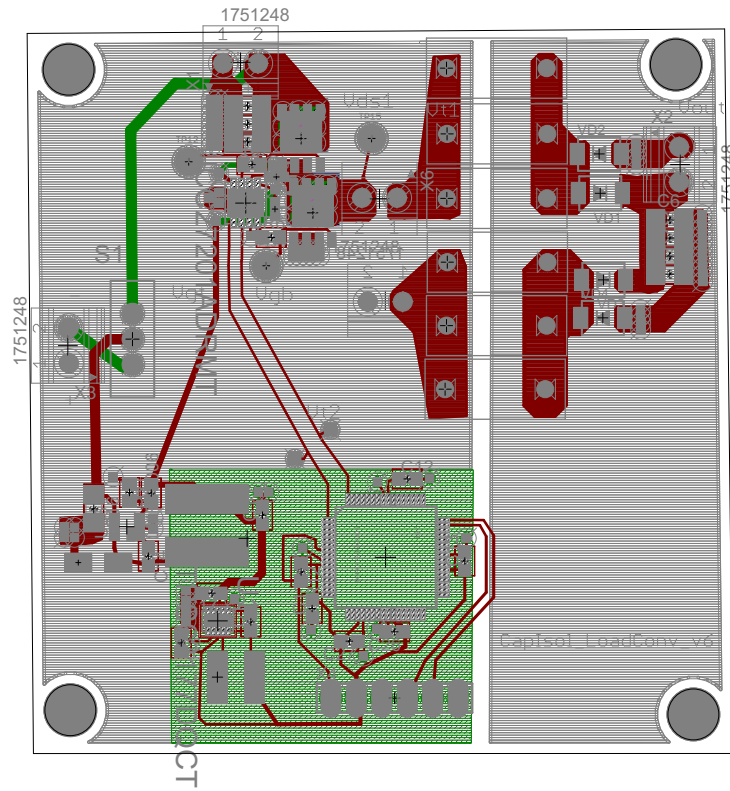


Figure B-8: Capacitive isolation load converter PCB layout with four layers (zoomed 2.7x).

Table B.1: Components of capacitively isolated converter

Stage	Components	Manufacturer Part No.	Info	Qty	Cost	Total
Inverter	Input Capacitor	GRM31CR61H106MA12L	10u/50V	3	0.068	0.204
	MOSFET	SIR836DP-T1-GE3	SIR836	2	0.248	0.496
	Driver	UCC27201DRMR	UCC27201D	1	1.31	1.31
	Bootstrap	GCM2195C1H103JA16D	0.1u,50V	1	0.058	0.058
	Bypass	GRM21BR61E106MA73L	10u,25V	1	0.02	0.02
Logic Supply						
Voltage Regulation 12V	LMR16006 (IC)	LMR16006XDDCR	4-60V/0.8-55V	1	1.274	1.274
	diode	B1100LB-13-F	100V/1A	1	0.089	0.089
	input capacitor	GRM31CR61H106MA12L	10u/50V	1	0.068	0.068
	output capacitor	GRM21BR61E106MA73L	10u/25V	1	0.02	0.02
	Bootsrap cap	GCM2195C1H103JA16D	0.1/50V	1	0.058	0.058
	Inductor	SDR0805-271KL	270uH	1	0.189	0.189
	Resistor 1	RC0603JR-07100KL	100k	1	0.0009	0.0009
	Resistor 2	RC0402JR-0710KL	10k	1	0.001	0.001
3.3V	TPS62177 (IC)	TPS62177DQCR		1	0.743	0.743
	Input capacitor	GRM21BR61E106MA73L	10u/25V	1	0.02	0.02
	Output capacitor	GRM21BR61E106MA73L	10u/25V	1	0.02	0.02
	Inductor	SDR0503-100ML	10uH	1	0.165	0.165
	Resistor	RC0603JR-07100KL	100k	1	0.0009	0.0009
Controller	IC	DSPIC33FJ64GS406-I/PT		1	3.83	3.83
	Capacitor 1	GCM2195C1H103JA16D	.1u/50V	4	0.058	0.232
	Capacitor 2	GRM21BR61E106MA73L	10u/25V	1	0.02	0.02
	Resistor	RC0402JR-0710KL	10k	1	0.001	0.001
Transformation						0
Capacitors	Y2 0.01uF 300VAC	B32021A3103M289	10nF	6	0.1704	1.0224
						0
Diode bridge	PMEG3050	PMEG3050BEP,115	30V,5A	4	0.125	0.5
	Output Capacitor	GRM21BR61E106MA73L	10u, 50V	4	0.068	0.272

```

1 %% This script determines the loss in the capacitive isolation converter
2 clc
3 clear all
4
5 Vin=28; %Input voltage
6 Vout=12; % Output voltage
7 Pout=25; % Output power
8 Rl=Vout^2/Pout; %Output load
9 f=1.34e6; %Switching frequency
10
11 Vs=Vin*(2/pi);% Fundamental voltage, FHA
12 Re=8*Rl/pi^2; % Equivalent resistance of rectifier
13
14 i=Vs/Re; % amplitude of the sinusoidal current
15 irms=i/sqrt(2); % RMS current
16 %%Loss in Mosfet - SIR 836 (at higher temp)
17 Rdson=24e-3; Coss=90e-12; Cg= 580e-12-40e-12; Qg=10e-9; %Ciss-Crss
18 Vg=8.5;
19
20 Loss_Cond_Mosfet=irms^2*Rdson; % 2 because of square of squareroot of 2
    (rms)
21 Loss_Sw_Mosfet= 2*Coss*Vin^2*f; %In 2 Fets (If ZVS not present)
22 Loss_gate_Mosfet=2*Qg*Vg*f; %In 2 fets
23
24 %% Loss in Inductor
25 ESR_ind=50e-3;
26 Loss_ac_inductor=irms^2*ESR_ind;
27 %%Loss in Capacitor
28 ESR10=0.16/3; %ESR of 3 capacitors in parallel
29 Loss_cap=irms^2*ESR10; %Loss in one capacitor
30 %%Loss in diodes -PMEG3050EP
31 Vf=0.3;
32 iav=i/pi; % have sinewave
33 Loss_diodes= Vf*iav*4; %4 diodes
34

```



```

35 Total_loss=Loss_Cond_Mosfet+Loss_gate_Mosfet+Loss_ac_inductor*2+
    Loss_diodes+Loss_cap*2
36 Pin=Pout+Total_loss;
37 Eff=(Pin-Total_loss)/Pin
38
39 Pie=[Loss_Cond_Mosfet Loss_gate_Mosfet Loss_ac_inductor*2 Loss_diodes
    Loss_cap*2 ];
40 figure
41 pie(Pie)
42 colormap ([0.6 0.2 0.2; 0.7 0.3 0.3; 0.6 0.6 0.6; 0.9 0.9 0.9; 0, 0, 0
    ]);
43 legend('MOSFET Conduction', 'MOSFET Gate', 'Inductor', 'Diode', '
    Capacitor', 'Location', 'eastoutside')

```


Appendix C

Design of Converters to Reduce
System Cost: Schematic, PCB
Layout and Components of Resonant
Converters, and System Level
Simulation Code

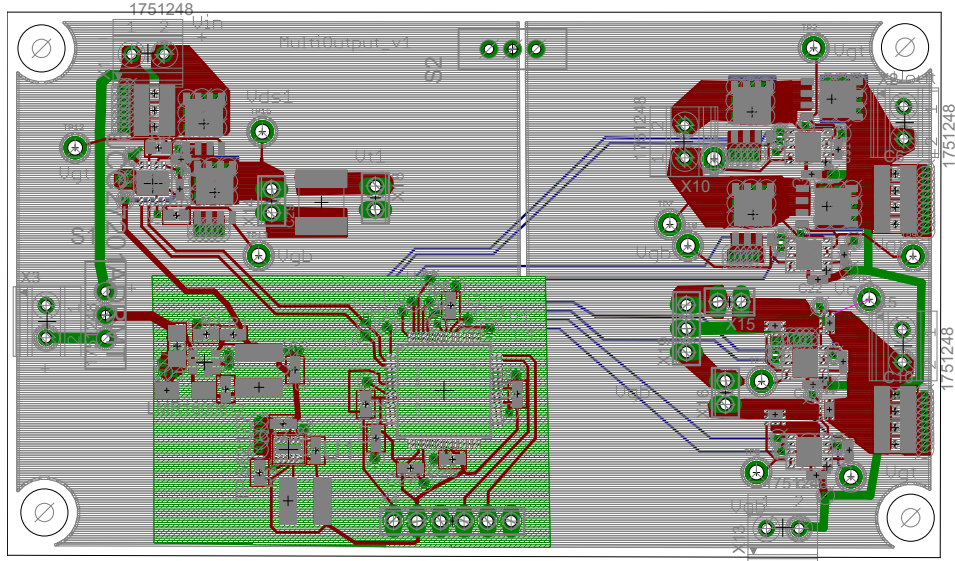
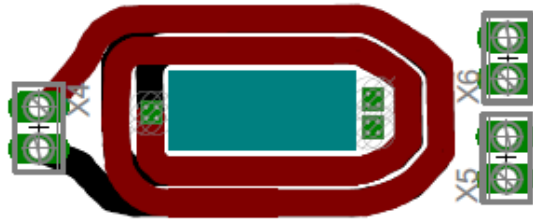


Figure C-2: Resonant converter PCB layout with four layers (zoomed 2.5x).

Table C.1: Power stage components of resonant converters

Stage	Components	Manufacturer Part No.	Info	Qty	Cost	Total
Inverter	Input Capacitor	UMK316BBJ106ML-T	10u/50V, 1206	4	0.095	0.38
	MOSFET	SIR836	40V/21 A	2	0.248	0.496
	Driver	UCC27201D	120V/3A	1	1.31	1.31
	Bootstrap	C1608X5R1H104K080AA	0.1u/50V, 0603	1	0.0068	0.0068
	Bypass	ZRB18AR61E106ME01L	10u/25V, 0603	1	0.067	0.067
Rectifier -12V	MOSFET	SIR484DP-T1-GE3	20V/20A	4	0.301	1.204
	Driver	LM5113SD/NOPB	100V/1.4	2	1.582	3.164
	Bootstrap	C1608X5R1H104K080AA	0.1u/50V, 0603	1	0.0068	0.0068
	Bypass	ZRB18AR61E106ME01L	10u/25V, 0603	1	0.067	0.067
	Isolator	SI8620BB-B-IS	2.5kV	1	0.833	0.833
Transformation	Output capacitor	GRM21BR61C106KE15K	10u/16V, 1206	4	0.022	0.088
	Transformer (Litz wire)	Custom		1	4.5	4.5
	Transformer (PCB)	B66283G0000X149	ELP18/4/10	1	0.34	0.34
	Clamps	B66284F2204X000	EILP18 set	1	0.108	0.108
	Cost increase	Custom	4oz vs 1oz	1	0.26	0.26
	Capacitor	C3216C0G1H104J160AA	0.1u/50V, 1206	2	0.12	0.24



(a) Primary winding: 1 and 6 layer of the PCB.



(b) Secondary winding 1: 3 and 4 layer of the PCB.



(c) Secondary winding 2: 2 and 5 layer of the PCB.

Figure C-3: PCB transformer used for multi-output resonant converter.

Table C.2: Components of the resonant converter

Part	Value	Package
C1	10u/25V	C0402K
C2	0.1u/50V	C0402K
C3	10u/16V	C1206
C4	10u/16V	C1206
C5	10u/16V	C1206
C6	10u/16V	C1206
C7	10u/50V	C1206
C8	10u/50V	C1206
C9	10u/50V	C1206
C10	10u/10V	C1206
C11	0.1u/50v	C0603
C12	10u/25v	C0603
C13	0.1u/50v	C0603
C14	0.1u/50V	C0603
C15	10u/25V	C0603
C16	10u/25V	C1206
C17	10u/25V	C0603
C18	10u/25V	C0603
C19	0.1u/50V	C0402K
C20	10u/25V	C0402K
C21	0.1u/50V	C0402K
C22	10u/25V	C0402K
C23	10u/10V	C1206
C24	10u/10V	C1206
C25	10u/10V	C1206
C26	0.1u/50v	C0603
C27	0.1u/50v	C0603
C28	0.1u/50V	C0402K
C29	100n/50V	C2220K
C30	10u/25V	C0402K
C31	0.1u/50V	C0402K
C32	10u/25V	C0402K
D5	B1100LB	DO201AD
R1	100k	R0603
R2	10k	R0603
R3	100k	R0603
R5	0	R0603
R6	0	R0603
R12	10k	R0603
S1	JS102011SAQN	SWITCH-SPDT
S2	JS102011SAQN	SWITCH-SPDT
U\$1	SIR836	POWERMOS
U\$2	SIR484	POWERMOS
U\$3	SIR484	POWERMOS
U\$4	SIR484	POWERMOS
U\$5	SIA430DJ	POWERPAK-SC70
U\$6	LMR16006	TSOT23-6_DDC
U\$7	DSPIC33FJ64GS406	TQFP64
U\$8	SIR484	POWERMOS
U\$9	SIA430DJ	POWERPAK-SC70
U\$10	SIA430DJ	POWERPAK-SC70
U\$11	10uH	SDR0503
U\$12	SIA430DJ	POWERPAK-SC70
U\$13	SIR836	POWERMOS
U\$14	LM5113	WSON-10
U\$15	LM5113	WSON-10
U\$16	LM5113	WSON-10
U\$17	LM5113	WSON-10
U\$18	220uH	SDR0503
U1	TPS62177	SON50P200X300X80-11N
U2	UCC27201ADRMT	SON80P400X400X100-9N
X1	OSTOQ021251	1751248
X2	OSTOQ021251	1751248
X3	1751248	1751248
X5	OSTOQ021251	1751248
X10	OSTOQ021251	1751248
X13	OSTOQ021251	1751248

```

1 %%This script determines which converter has lowest cost
2 %It calls CreateSystem.m which calls CreatedDemand_Single.m to create
3 %demand profile
4 %To determine cost it calls FindCostwithextPowerstage
5 clc
6 clear all
7
8 Accepted_availabilityPer=0.92;
9 CosttoMinimize=1; % 1=Lifetime cost; 0=InitialCost;
10 PowerStageCost=5.28; %Power Stage cost of flyback load converter
11 LoadEfficiencydata=xlsread('PowerElectronics_Eff','LoadConverter','A2:
    B14');
12 [BatteryCapacity,PVpanelCapacity,InitialCost,TotalCost ]=CreateSystem(
    Accepted_availabilityPer,CosttoMinimize,LoadEfficiencydata,
    PowerStageCost);
13
14 PowerStageCost=12.54; %Power Stage cost of Resonant converter (litz wire
    )
15 LoadEfficiencydata=xlsread('PowerElectronics_Eff','
    LoadConverterMultiOutput','A2:B9');
16 [BatteryCapacity,PVpanelCapacity,InitialCost,TotalCost ]=CreateSystem(
    Accepted_availabilityPer,CosttoMinimize,LoadEfficiencydata,
    PowerStageCost);
17
18 PowerStageCost=8.85; %Power Stage cost of Resonant converter (PCB)
19 LoadEfficiencydata=xlsread('PowerElectronics_Eff','
    LoadConverterMultiOutputPCB','A2:B10');
20 [BatteryCapacity,PVpanelCapacity,InitialCost,TotalCost ]=CreateSystem(
    Accepted_availabilityPer,CosttoMinimize,LoadEfficiencydata,
    PowerStageCost);

```

```

1 function[BatteryCapacity,PVpanelCapacity,CostInitial,CostTotal ]=
    CreateSystem(Accepted_availabilityPer,CosttoMinimize,
    LoadEfficiencydata,PowerStageCost)

```



```

2 %This script designs the system design for the required availability
3
4 num.hours=8760; %24 for 1 day; 8760 for 1 year
5 num.Households=5; %Numer of households with load converters
6 Battery.MinDODPer=0.05; %Minimum % depth of discharge of the battery
7 Battery.InitialPer=0.5; %Initial % charge of the battery
8 Battery.ChargeEff=0.95; %Charging efficiency of battery
9 Battery.DischargeEff=0.95; %Discharge efficiency of battery
10 PVpanel.RatingAtIrradiance=1000; %Max Rated Irradiance of panel
11 Wiring.Length=80; %Length of wiring (40m *2 for return)
12 rho_al= 4*10^-8; %Resistivity of aluminum
13 Wiring.Size=2.5e-6; %in m
14 Network.Voltage=24; %Nominal network voltage
15
16 PVpanelRating_Available=150:10:300; %in W
17 BatteryCapacity_Available=[18:2:32]*12; %in Ah*12= Wh
18 %% Generation data
19 Generation.data=xlsread('pwwatts_hourly_patamda_jharkhand','A20:K8779');
    %Ddata from NREL
20 Generation.Irradiance=Generation.data(:,8); %Irradiance
21 Generation.Temperature=Generation.data(:,6); %Temperature
22 Generation.Hour=Generation.data(:,3); %Time
23
24 %% Load Data
25 load.NoLight1Hours = xlsread('DemandInput.xlsx', 'B9:B32');
26 load.NoLight2Hours = xlsread('DemandInput.xlsx', 'C9:C32');
27 load.NoPhoneHours = xlsread('DemandInput.xlsx', 'D9:D32');
28 load.Power = xlsread('DemandInput.xlsx', 'C2:C5');
29 % Create Load Profile
30 [loadprof] = CreateDemand_Single(Generation,load);
31 Load.data=loadprof(1:num.hours,1);
32 Load.demand_all=Load.data*num.Households;
33
34 %% Load Converter Loss
35 Converter.load_eff=LoadEfficiencydata;
36 Converter.load_power=Converter.load_eff(:,1);

```



```

66 for numBatteries=1:1:length(BatteryCapacity_Available)
67     Battery.Capacity=BatteryCapacity_Available(numBatteries);
68     Battery.MinDOD=Battery.MinDODPer*Battery.Capacity; %Minimum depth of
        discharge
69     Battery.Initial=Battery.InitialPer*Battery.Capacity;
70
71     for numPV=1:1:length(PVpanelRating_Available)
72         PVpanel.Rating=PVpanelRating_Available(numPV);
73         Generation.Output= PVpanel.Rating*Generation.Irradiance/PVpanel.
            RatingAtIrradiance;%Output of solar panel with 1000 W/m2
            rating
74
75         %Charge Controller Loss
76         Function_chargeConverter_Eff_withGeneration= pchip(Converter.
            charge_power,Converter.charge_Eff,Generation.Output);
77         Loss.Generation_Converter_charge=(Generation.Output).*(100-
            Function_chargeConverter_Eff_withGeneration)/100;
78         Effective.Powertobattery=Generation.Output+Loss.
            Generation_Converter_charge;
79
80         %Battery Energy
81         Battery.Energy(1)=Battery.Initial;
82         Battery.Spillage=zeros(num.hours,1);
83         Load.otserved=zeros(num.hours,1);
84         for i=1:num.hours-1
85             if Effective.Powertobattery(i)>=Load.
                data_all_andLinkConverter(i) %Charging
86                 Battery.Energy(i+1)= (Effective.Powertobattery(i)-Load.
                    data_all_andLinkConverter(i))*Battery.ChargeEff+
                    Battery.Energy(i);
87                 if Battery.Energy(i+1)>Battery.Capacity
88                     Battery.Energy(i+1)=Battery.Capacity;
89                     Battery.Spillage(i+1)=(Effective.Powertobattery(i)-
                        Load.data_all_andLinkConverter(i));
90                 end
91             else %Discharging

```

```

92         Battery.Energy(i+1)= (Effective.Powertobattery(i)-Load.
           data_all_andLinkConverter(i))*Battery.DischargeEff+
           Battery.Energy(i);
93         if Battery.Energy(i+1)<Battery.MinDOD
94             Battery.Energy(i+1)=Battery.MinDOD;
95             Load.otserved(i+1)= (Load.data_all_andLinkConverter
           (i)-Effective.Powertobattery(i));
96         end
97     end
98 end
99
100     Availability(numBatteries,numPV)=(1-sum(Load.otserved)/sum(Load
           .data_all_andLinkConverter))*100;
101     [TotalCost(numBatteries,numPV), InitialCost(numBatteries,numPV)
           ]=FindCostwithextPowerstage(BatteryCapacity_Available(
           numBatteries), PVpanelRating_Available(numPV),Wiring,num,
           Load,PowerStageCost);
102     if Availability(numBatteries,numPV)<Accepted_availabilityPer
           *100;
103         TotalCost(numBatteries,numPV)=inf;
104         InitialCost(numBatteries,numPV)=inf;
105     end
106
107 end
108 end
109
110 if CosttoMinimize==1
111     [MinCost,I]=min(TotalCost(:));
112     [rowIndex, colIndex]=ind2sub(size(TotalCost),I);
113 else
114     [MinCost,I]=min(InitialCost(:));
115     [rowIndex, colIndex]=ind2sub(size(InitialCost),I);
116 end
117
118 BatteryCapacity=BatteryCapacity_Available(rowIndex)/12;
119 PVpanelCapacity=PVpanelRating_Available(colIndex);

```

```

120 CostInitial=InitialCost (rowIndex, colIndex);
121 CostTotal=TotalCost (rowIndex, colIndex);
122
123 fprintf('Selected Battery=%d Ah and PV panel=%d W.\n',BatteryCapacity,
        PVpanelCapacity)
124 fprintf('Initial cost of the system= $%g and lifetime cost=$%g\n',
        CostInitial, CostTotal)
125 end

```

```

1 function [loadprof] = CreateDemand_Single(Generation, load);
2 %This script creates the load profile
3 light1_power = load.Power(1);
4 light2_power = load.Power(2);
5 fan_power = load.Power(3);
6 phone_power = load.Power(4);
7
8 %Critical factors
9 Need_light=0.05; %When solar irradiance is below this value
10 Need_fan=31; %When temperature is above this value
11
12 load.NoLight1Hours=load.NoLight1Hours';
13 load.NoLight1HoursMatrix= repmat (load.NoLight1Hours, 365, 1);
14 load.NoLight2Hours=load.NoLight2Hours';
15 load.NoLight2HoursMatrix= repmat (load.NoLight2Hours, 365, 1);
16 load.NoPhoneHours=load.NoPhoneHours';
17 load.NoPhoneHoursMatrix= repmat (load.NoPhoneHours, 365, 1);
18
19 % Phone hour variation
20 firstPhoneHour = find(load.NoPhoneHours,1, 'first');
21 lastPhoneHour = find(load.NoPhoneHours,1, 'last')-1;
22 phone_demand = zeros (365, 24);
23
24 for day = 1:365
25     for hour=1:24
26         hoursadded = (((day-1)*24) + 1) + hour -1;

```

```

27     %light 1
28     lighting1_hours_avail_logical(day, hour) = Generation.Irradiance(
        hoursadded) < Need_light;
29     lighting1_hours_avail(day, hour)=lighting1_hours_avail_logical(
        day, hour)*load.NoLight1HoursMatrix(day, hour);
30     Light1_demand= lighting1_hours_avail.*light1_power;
31
32     %light 2
33     lighting2_hours_avail_logical(day, hour)= Generation.Irradiance(
        hoursadded) < Need_light;
34     lighting2_hours_avail(day, hour)=lighting2_hours_avail_logical(
        day, hour)*load.NoLight2HoursMatrix(day, hour); %*round(rand);
35     Light2_demand= lighting2_hours_avail.*light2_power;
36
37     %fan
38     fan_hours_avail_logical(day, hour) = (Generation.Temperature(
        hoursadded)) > Need_fan;
39     fan_demand= fan_hours_avail_logical.*fan_power;
40
41     end
42     %phone
43     phoneHours = zeros(1,24);
44     %startHour = randi([firstPhoneHour lastPhoneHour]);
45     possibleHour = lastPhoneHour - firstPhoneHour +1;
46     startHour = firstPhoneHour + mod(floor(day/10), possibleHour);
47     phoneHours(1, startHour:startHour+1) = [1 1];
48     phone_demand(day, :) = phoneHours.*phone_power;
49 end
50
51 Total_demand=Light1_demand+Light2_demand+fan_demand+phone_demand;
52 Numelements=numel(Total_demand);
53 Total_demand_row=reshape(Total_demand', 1, Numelements);
54 loadprof=Total_demand_row';
55 end

```

```

1 function [CostTotal, CostInitial] = FindCostwithextPowerstage(
    BatteryCapacity, PVpanelRating, Wiring, num, Load, PowerstageCost)
2
3 %% This script calculates the cost of the system
4
5 num.Years=15; %Lifetime
6 Battery.CostperWh=0.5; %$/Wh
7 Battery.Cost=Battery.CostperWh*BatteryCapacity; %$
8 Battery.Life=5; %battery life
9 Battery.Amount=num.Years/Battery.Life; %Number of batteries used
10
11 PVpanel.CostperW=0.7; %$/W
12 PVpanel.Cost=PVpanel.CostperW*PVpanelRating; %$
13
14 Wiring.Costperm=0.06; %Cost of Aluminum per m
15 Wiring.CostpermCat3=0.03; % Cost of Cat3 cable (half the wire as no
    return)
16 Wiring.Cost=Wiring.Costperm*Wiring.Length*num.Households+Wiring.
    CostpermCat3*Wiring.Length/2*num.Households;
17 Wiring.PolesCostperpole=3.33; %Cost per pole
18 Wiring.PolesCost=Wiring.PolesCostperpole*num.Households;%1 pole per
    household
19 Wiring.PolesLife=5; %pole life
20 Wiring.PolesAmount=num.Years/Wiring.PolesLife;
21
22 Electronics.CostA=40; %Cost of source unit
23 Electronics.CostB=(15+PowerstageCost)*num.Households; %Cost of load unit
24
25 CostInitial=Battery.Cost+ PVpanel.Cost+ Wiring.Cost+ Wiring.PolesCost+
    Electronics.CostA+ Electronics.CostB;
26 CostTotal= Battery.Cost*Battery.Amount+PVpanel.Cost+ Wiring.Cost+ Wiring
    .PolesCost*Wiring.PolesAmount+ Electronics.CostA+ Electronics.CostB;
27
28
29 Load.otservedIndex=find(Load.otserved); %Load not served

```

```
30 for j=1:num.hours
31     Load.demand_all(j==Load.otservedIndex)= false;
32 end
33
34 end
```


Appliance	Number Owned	Power (W)	Enabling Criteria	
Light 1	1	3	Solar output less than	0.05
Light 2	1	3	Solar output less than	0.05
Fan	1	15	Temp higher than (degC)	31
phone charger	1	2.5		

Hours load could be used

	Light1	Light2	phone charger*
1	0	0	0
2	0	0	0
3	0	0	0
4	1	0	1
5	1	0	1
6	1	0	1
7	1	0	1
8	0	0	1
9	0	0	1
10	0	0	1
11	0	0	1
12	0	0	1
13	0	0	1
14	0	0	1
15	0	0	1
16	1	1	1
17	1	1	1
18	1	1	1
19	1	1	1
20	1	1	1
21	1	1	1
22	0	0	0
23	0	0	0
24	0	0	0

*Phone is charged for 3 hours from the acceptable hours; The start-time varies

Figure C-4: The Excel spreadsheet used to create the demand profile.

Appendix D

Field Trial: June 2015

The field trial was conducted over a course of two weeks, in June 2015, in Jamshedpur, India. It was conducted with assistance from TATA steel CSR, who not only identified the village for the trial but also helped with community engagement.

The trial began with surveying of the community members. In this survey, community members were asked about their daily life activities and the decisions made regarding energy and economic matters. This was followed by setting up a microgrid, involving laying out the wires between the selected houses, by using the housing structure for stringing wires. The PMUs were connected using these wires, and switched on to provide electricity to the connected units. Basic software was run to test communication, metering and data logging. After two weeks, the system was taken down, after which detailed exit surveys were conducted to collect feedback from the community.

Details of the Trial

For the field trial, five houses were selected. The source unit was placed in the storage room of house 1, and a load unit was placed in the living room of house 1, as well as each of the four other houses in the vicinity, as shown in Fig. D-1.

A 250 W solar panel (HBL Power systems Ltd.) was placed on the roof of the shed behind house 1. A 180 Ah (HBL Power Systems Ltd.) sealed lead-acid battery was installed in house 1. Each house was provided with two 5 W LED lights, a 10 W

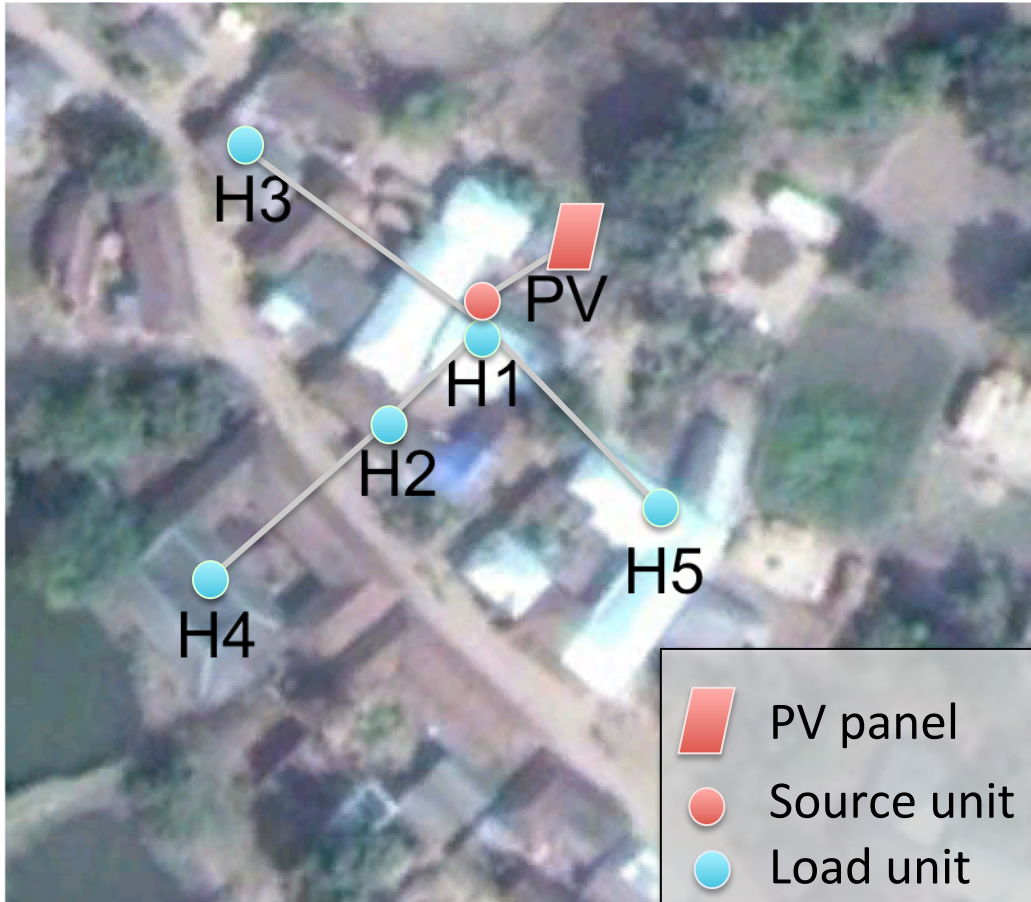


Figure D-1: Solar panel, battery, and five load units connected to the source unit.

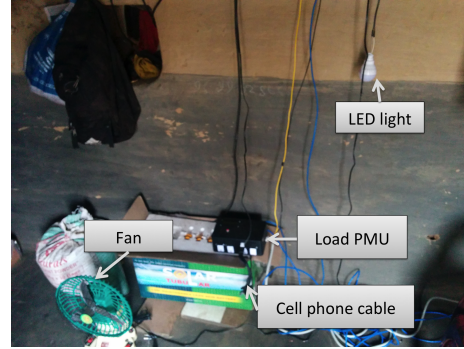
fan and a cell phone charging connector, which were all locally sourced. In total, 200 m of 14 AWG wire was used to connect the PMUs, as shown in Fig. D-2 (a).

Lessons Learnt from the Field Trial

The two main lessons learnt were as follows:

- The wiring requirement for distribution was much higher than the estimated distances. This estimation was made using straight line distance between the houses from the map of the village. This is because the entering point for the wires of each individual house was different according to the structure. Hence, approximately 10 meters of extra wiring per house was required.
- Locally sourced loads were very inefficient for such applications. The specifica-

tion labels on these loads were often found to be incorrect. For example, fans which were labelled as 12 W were consuming up to 36 W.



(a) Installation of wiring between houses (b) Load PMU installed in one of the houses

Figure D-2: Pictures from the field trial.

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