Fully Integrated Ultra Low Voltage Cold Start System for Thermal Energy Harvesting . . .

by

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Abstract

Wireless sensor networks used in various monitoring and sensing applications rely on energy harvesting for battery-less operation, as it minimizes the need for human intervention, and offers long term monitoring solutions. Typical energy harvesters use high efficiency boost converters, which are able to step-up voltages from as low as 10 mV. However, they often need > 200 mV in order to start up initially. Current solutions for achieving a low voltage start up require the use of bulky off-chip transformers, leading to undesired area overhead.

This research work presents proof-of-concept for a fully integrated start-up system, which can cold-start from < 50 mV using on-chip magnetics, and also be used as an energy harvesting charger for ultra low power applications. The use of lossy on-chip transformers in a Meissner Oscillator compared to high-quality off-chip transformers pose new design and optimization challenges. Hence, we have derived intuitive analytical expressions that are well-suited for use with the on-chip magnetics, and used them to co-optimize the oscillator components. An optimized depletion mode MOS transistor was fabricated and tested with an off-chip transformer, to exhibit oscillations from <3 mV DC input voltage. An optimized on-chip transformer, 36x smaller in area than the off-chip transformers, is currently awaiting layout and fabrication. A switched capacitor DC-DC circuit has also been designed, which can rectify and boost up the oscillator's output voltage to 1.2 V, to have a complete start-up system for energy harvesting.

Thesis Supervisor: Anantha P. Chandrakasan
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Acknowledgments

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Chapter 1

Introduction

Energy Harvesting is used to convert energy readily available from the surroundings to electrical energy, in order to power small systems like sensor nodes. Such self-powered operation can be extremely useful in remote sensors and wearable electronics as it eliminates the need for batteries. For these reasons, energy harvesting has been becoming very popular for powering circuits and systems.

Miniaturization of electronics is another key trend in all applications including energy harvesting, and it is particularly essential for wearable personal electronics and health monitoring systems. In case of thermal energy harvesting, if the Thermoelectric Generator (TEG) is made smaller in size, the power available at its output, given a fixed thermal gradient across itself, will be lower. So the energy harvesting system will need to start up and operate from very low power, and low voltages. In addition, the footprint of the energy harvesting system itself needs to be as low as possible.

To date, a low voltage start-up ($<$ 50 mV) for energy harvesting has required the use of bulky off-chip transformers, which are much larger than the integrated circuit itself in both the vertical and horizontal directions, and therefore take up considerable board area. There is need for a completely integrated solution to achieve low voltage start up for energy harvesting applications, without the area overhead.

This research work aims to replace the off-chip transformer with on-chip magnetics to have a fully integrated system, which can be used for cold-start with regular boost converters, or as a stand-alone product for thermal energy harvesting.

1.1 Motivation

1.1.1 Energy Harvesting

Energy harvesting allows the use of ambient sources of energy, like solar, thermal, vibrational, piezoelectric, and others, to power small circuits and systems. This in turn allows circuits to achieve self-sustaining operation by removing the dependence on batteries, or at least to minimize the need for human intervention by prolonging the life of these batteries.

Table 1.1 shows a comparison between some of the common energy harvesting sources in terms of their harvested power per unit area. Thermal energy harvesting shows promise for both regular, indoor use with humans, and for industrial use.

Table 1.1: Comparison of energy sources for harvesting [4]

Energy Source	Harvested Power	
	Human	*Industry*
Vibrational	$4\mu W/cm^2$	$100\mu W/cm^2$
	Human	*Industry*
Thermal	$25\mu W/cm^2$	$1-10mW/cm^2$
	Indoor	*Outdoor*
Solar	$10\mu W/cm^2$	$10mW/cm^2$
	WiFi	*GSM*
RF	$0.1\mu W/cm^2$	$1\mu W/cm^2$

Applications

Energy harvesting finds use in many applications including wireless sensor networks (WSNs), personal wearable electronics, and industrial automation. WSNs are mainly used for monitoring and sensing applications, including area monitoring, environmental monitoring, health monitoring, etc. The sensor nodes for these WSNs may need to be deployed in remote, inaccessible or hazardous locations, where it is unfeasible to change the batteries every few years. This makes it highly desirable for these sensors to be self-powered. Similarly, in smart green buildings, there might be vacuum panels installed in the walls for insulation, where a sensor is needed to monitor the pressure inside the panel and communicate that data out once every hour. Battery-less operation can make it more practical to have such insulations panels, as it obviates the need for battery replacement.

Benefits

The benefits of energy harvesting to power circuits and systems are many, and a lot of them stem from the removal of batteries. Some of the advantages of using energy harvesting over battery power are summarized below:

1. **Lower maintenance costs**, as there is no battery replacement service needed

2. **Long term monitoring and sensing solutions**, as the circuits continue to work for as long as ambient energy is available

3. **Better bio-implantable solutions**, as no surgeries are needed for battery replacement once the device is implanted

4. **Enabling of sensing in remote/hazardous areas**, as no human intervention is required after the initial installation

5. **Less negative environmental impact**, as there is no need for batteries or battery disposal

1.1.2 Low Voltage Start-Up

Being able to start up at low voltages is key for maximizing the harvesting potential of thermal energy harvesting systems. In the recent years, there has been considerable progress in the area of energy harvesting. Several highly efficient boost converters have been published, which are capable of operating from down to 20 mV or even 10 mV input voltages, as shown in Table 1.2. However, these converters often need more than 200 mV for starting up from zero energy initially, resulting in wasted potential. Having a low start-up voltage can therefore allow the use of boost converters' low voltage operation to its full extent.

Table 1.2: Examples of boost converters for energy harvesting applications

Reference Paper	Minimum Input Voltage	Cold-Start Voltage
JSSC 2010 [5]	20 mV	600 mV
BQ25504 2012 [6]	80 mV	330 mV
JSSC 2015 [7]	10 mV	220 mV

1.1.3 Integration

Along with low start-up voltages, having a small footprint can be crucial in many wearable devices and bio applications. While there are some energy harvesters that can start up at lower voltages than the boost converters (refer to Table 1.3), they are not integrated. Instead, they require large board areas.

The energy harvester in [8] can cold-start from as low as 20mV using a Meissner Oscillator. However, it does so using an off-chip transformer with a turns ratio of 100 and it is very inefficient at higher input voltages. The work in [9] tackles the second problem by using the Meissner Oscillator for a cold-start, and then switching to a boost

Table 1.3: Energy harvesting systems with low start-up voltages

Reference Paper	Minimum Input Voltage	Cold-Start Voltage	Integrated?
LTC3108 2010 [8]	20 mV	20 mV	No
ISLPED 2014 [9]	40 mV	40 mV	No

converter for regular operation. However, it also needs an off-chip transformer with a turns ratio of 100, which translates into an undesirable area overhead. Integration for area savings can have a positive impact, particularly in wearable and implantable devices.
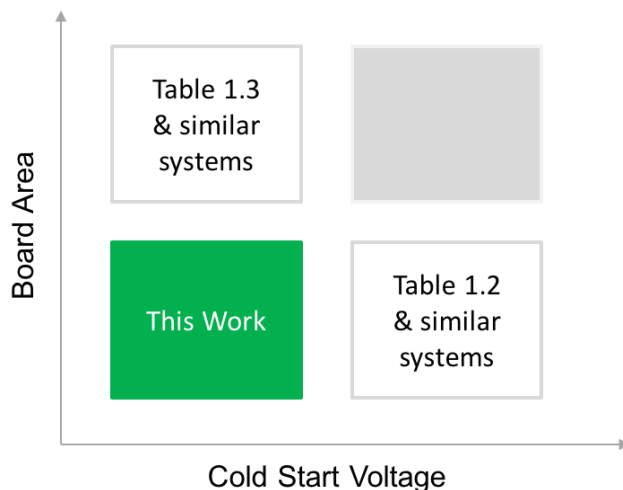
Figure 1-1: Research focus in energy harvesting systems

1.1.4 Research Focus

Based on the previous sections, it can be concluded that there is a noticeable gap in the research area of thermal energy harvesting, and therefore, need for a system that can fill the gap. Figure 1-1 summarizes the current status of the energy harvesting systems, where most of the published solutions either involve the use of bulky off-chip transformers, or lack a low start-up voltage. This research work targets the niche to offer an integrated solution with low cold start voltage for thermal energy harvesting applications.

1.2 Background

1.2.1 Integrated Magnetics

This section provides a brief, basic background on integrated inductors and transformers, and lists some of the works published in the area of integrated magnetics.

Inductors

A simple solenoidal inductor consists of a metal wire wound around a magnetic core, as shown in Figure 1-2 a). The purpose of the core is to provide linkage of magnetic flux from one coil to the next, which ensures that majority of the flux passing through one coil of the inductor, passes through all other coils of the inductor as well. If the flux linkage is high, the self-inductance (L) of the structure will also be high.

a) Solenoidal Inductor   b) Planar Inductor   c) Toroidal Inductor
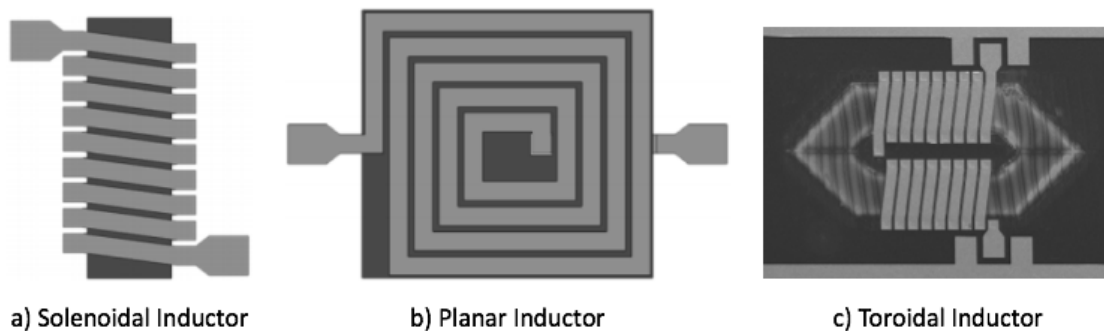
Figure 1-2: Common integrated inductor designs [1]

Accordingly, in the absence of a magnetic core, the inductance of the structure is much lower. Therefore, the resonant frequencies are much higher ($>$ 100 MHz). While air core inductors are good for use in high frequency integrated applications, having magnetic cores becomes important for use in medium frequency designs: in the range of 100 kHz to 100 MHz. One example of air core inductors are planar/spiral inductors, as shown in Figure 1-2 b).

In a solenoidal inductor, the return path of the flux is through the air rather than

the core. The air gap stores energy, which is undesirable in a regular transformer, as a transformer is expected to transfer all energy from the input to the output. To avoid the energy storage, it is beneficial to have a toroidal structure, which closes the magnetic path through magnetic core material, and minimizes flux leakage. While off-chip toroidal inductors are often circular in shape, the integrated toroidal inductors are typically designed with two inductors in parallel, with a closed magnetic core, as shown in Figure 1-2 c). This is done to make sure that the inductor is aligned along the hard axis, as explained in the following section.

B-H Curves

The magnetic flux density, B, in the core of an inductor is related to the magnetizing force, H, which generated the flux, via the permeability of the magnetic material as

$$B = \mu H \tag{1.1}$$

In this equation, $\mu = \mu_r \mu_o$, where μ_r is the relative permeability of a material ($\mu_r = 1$ for vacuum). Different magnetic materials, such as ferrite cores, metal alloys like Permalloy, metal oxides, etc. can display widely different relative permeabilities [10]. Having a high permeability core is desirable for a transformer as it provides low energy storage in the core.

Due to magnetocrystalline anisotropy, the properties of a magnetic core differ based on its alignment, say along x-axis vs. y-axis. As an example, the B-H curve for a particular integrated inductor is shown in Figure 1-3. As can be seen in the plot, the relative permeability along the easy axis is small, while that along the hard axis is large. Therefore, it is beneficial to place the transformer along the hard axis rather than the easy axis.
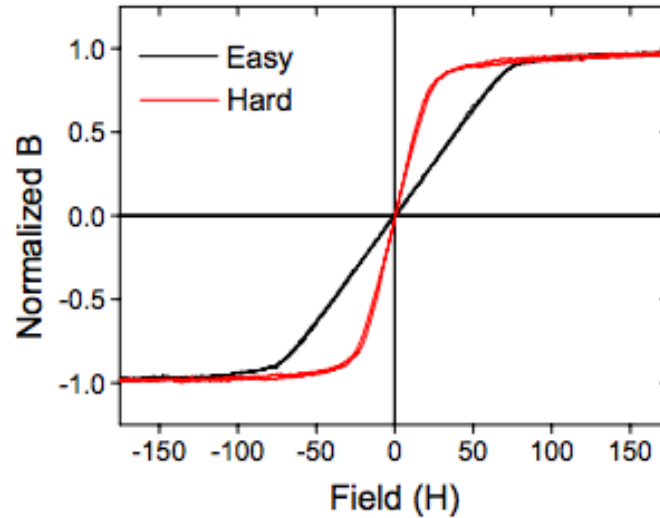
Figure 1-3: Example of a B-H curve [2]

Transformers and Sources of Loss

A transformer has two sets of coils, primary and secondary, wound around the same magnetic core. So, the flux from the primary windings is linked to the secondary windings. Therefore, in addition to self-inductance of the primary and secondary coils, transformers also have a mutual inductance (M) between the two coils. Some sources of losses for transformers are listed below:

- **Core Losses**: They consist of losses due to eddy currents and hysteresis loss. Eddy currents can be reduced by slicing, laminating, and then stacking the magnetic cores instead of using a single thick block of magnetic material. Materials with lower core conductivity have lower eddy current losses.

- **Copper Losses**: They refer to the losses caused by the DC resistance of copper windings and they can be reduced by using thicker metal windings.

- **Skin Effect**: It is caused by the increase in AC resistance as the currents concentrate around the outer edges of the conductor at higher frequencies. Skin effect can be minimized by using copper thickness that is smaller than one skin

depth.

- **Proximity Effect**: It is caused by magnetic fields in the neighbouring coils carrying currents in the same direction, and it also increases the AC resistance of the coils at higher frequencies. Proximity effect can be reduced by interleaving primary windings with the secondary windings.

Recent Examples of Integrated Magnetics

In the last decade, there has been a big push towards using integrated magnetics for power conversion. [11] demonstrated a DC-DC converter with 2nH integrated inductors using stacked interleaved topology. [12, 13] proposed the use of planar inductors for high frequency DC-DC conversion, while [14] employed thin film coupled-magnetic-core inductors for voltage regulation. [15] and [16] proposed toroidal power inductors and V-Groove thin film inductors, respectively, for potential use in power applications.

The works listed above have been focused on using integrated inductors for high frequency DC-DC conversion, and did not involve the use of transformers for energy harvesting. [17] investigated the use of bondwire micromagnetics as transformers for the use in energy harvesting applications, with potential for die-level integration. However, the transformers used in [17] are comparable in area to the bulky off-chip transformers. Texas Instruments (TI) used integrated transformers as magnetic fluxgate sensors for current sensing applications [18]. This research work investigates the use of the same fluxgate magnetics technology, further described in Chapter 3, for use in energy harvesting.

1.2.2 Thermoelectric Generators

When a thermocouple is subjected to a temperature gradient, it produces a voltage difference across the two electrical conductor, via a phenomenon called the Seebeck
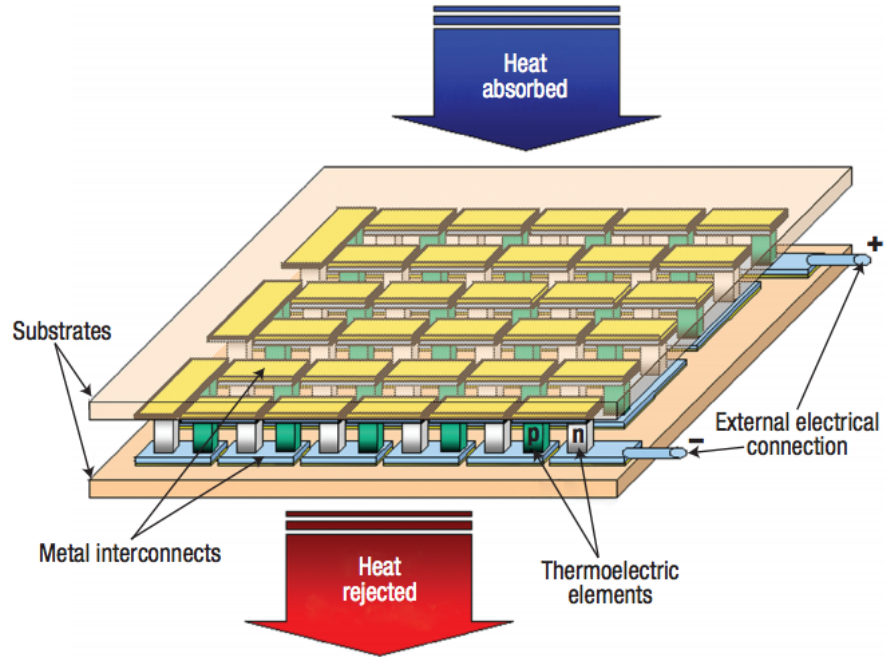
Figure 1-4: A typical thermoelectric device [3]

effect. Thermoelectric generators (TEGs) are modules made of several thermocouples connected in series electrically, and in parallel thermally, as shown in Figure 1-4. In circuit analysis, TEGs are modeled as a DC voltage source in series with a resistance, as shown in Figure 1-5.

Most TEGs employ Bismuth Telluride (Bi_2Te_3) or similar V-VI materials to form thermocouples using n-type and p-type legs [19, 20, 21]. The two main factors affecting the performance of a TEG are the size of each thermoleg, in terms of its base area
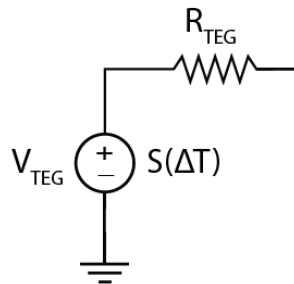
Figure 1-5: Circuit model for a TEG

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and height, and the number of such elements in a given area. As an end-user, one does not have control over these parameters.

A designer can connect commercially available TEG modules in series or parallel, and side-by-side or stacked, to suit the application requirements. Multiple TEGs can be placed side-by-side in series to get higher voltage, or in parallel to get a lower electrical resistance, but at the cost of higher area. So one of the most important parameters in selecting the TEG is its power per unit area for a given temperature differential. The trade offs between area, voltage, and resistance can later be made for the selected TEG. For reference, typical TEGs in the wearable size range ($< 10cm^2$ in size) with ~5Ω electrical resistance can produce about 20 mV of DC output voltage from a temperature gradient of 1 K across themselves [22].

Thermal resistance is another important parameter when selecting a TEG, as it dictates the size of the heat sink to be used for maximum thermal power transfer. Thermal resistance is analogous to electrical resistance in the sense that having a higher electrical resistance relative to the rest of the circuit implies a higher voltage drop across the element. So, a higher thermal resistance is desirable for a TEG, as it means that a greater percentage of the total temperature gradient over the system will drop across the TEG itself, enabling it to deliver a higher output voltage. Multiple TEGs can be stacked atop one another to have a higher thermal resistance without an increase in base area.

The size of the heat sink is a critical consideration for miniaturization of thermal energy harvesting systems, as it can be much larger than the size of the TEG itself. For reference, two heat sinks placed next to a TEG and a dime are shown in Figure 1-6. The small turquoise heat sink is much more manageable as part of a wearable device than the larger, and much heavier, aluminum heat sink, but the former also has a higher thermal resistance. To use a specific heat sink, the TEG needs to be chosen to match the thermal resistance of that heat sink in order to achieve high
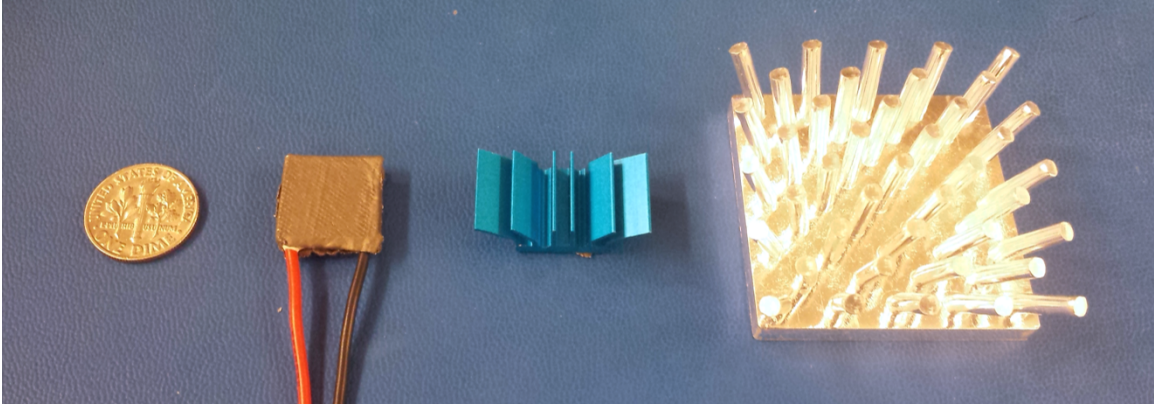
Figure 1-6: Example of heat sink sizes

energy efficiency.

The thermal resistance of a TEG is typically lower than that of a heat sink and it is a challenge to match the thermal resistances of the two while keeping the total area in the wearable range. But having low start-up voltages can allow the use of smaller heat sinks to start up the system, and it can even allow the TEG to be used without a heat sink. This can also be useful in other applications where the area consumption is a greater concern than maximum power transfer.

1.3   Thesis Contributions

Some key contributions of the author towards this thesis are listed below, and elaborated on in the following chapters:

1. System design of a charger for thermal energy harvesting, using two cascaded stages: a Meissner Oscillator, and a switched capacitor DC-DC converter, to provide proof-of-concept for a fully integrated energy harvesting system with a low cold start voltage.

2. Analysis of the Meissner Oscillator circuit to develop and validate a criteria for the optimization of integrated transformers and transistors. The loop gain expression derived provides an intuitive sense of how the geometrical parameters

of the transformer should change in order to get better performance from the overall system.

3. Design of optimized transistors for use in the Meissner Oscillator circuit, followed by demonstration with an off-chip transformer to observe transformer oscillations with < 3 mV DC input voltage.

4. Analysis of various transformer structures to predict the one with the highest potential for use in a Meissner Oscillator, and optimization of the selected transformer for low voltage start-up in conjunction with the fabricated transistors

5. While being restricted by the quality factor of the transformer owing to technology limitations, investigation of other techniques to improve the transformer performance and area efficiency.

6. Design of a switched capacitor DC-DC circuit to step up voltages from 0.35 V to 1.2 V, while being powered by the Meissner Oscillator circuit.

Chapter 2

System Overview

The proposed energy harvesting system consists of a TEG to convert thermal energy into electrical energy, followed by step up converter(s) for pumping up low voltages from the TEG to higher levels so as to power the load circuit. The system-level considerations and the overall architecture are discussed in this chapter.

2.1   Design Considerations

The energy harvesting system is required to have the following features and abilities:

- To extract power from a small TEG and small heat sink, in the wearable size range

- To cold start from ultra low voltages (30 mV), without using bulky off-chip components

- To provide an output voltage of 1.2 V to be used as supply by the subsequent circuitry, implying a conversion ratio of 40-50 times

- To have a small footprint itself

2.2 Implementation

In order to start up from 30 mV DC voltage, a Meissner Oscillator circuit is used, which is discussed in detail in Chapter 3. The Meissner Oscillator alone cannot provide a 50x DC-DC step up ratio from such low voltages using lossy on-chip transformers. So, another step-up conversion stage is needed to assist the oscillator.

To meet the requirement of being an integrated solution, a switched capacitor (SC) DC-DC circuit is used as a second stage in the system, which will be further discussed in Chapter 4. The switched capacitor circuit is cascaded on to the Meissner Oscillator circuit, as shown in Figure 2-1.
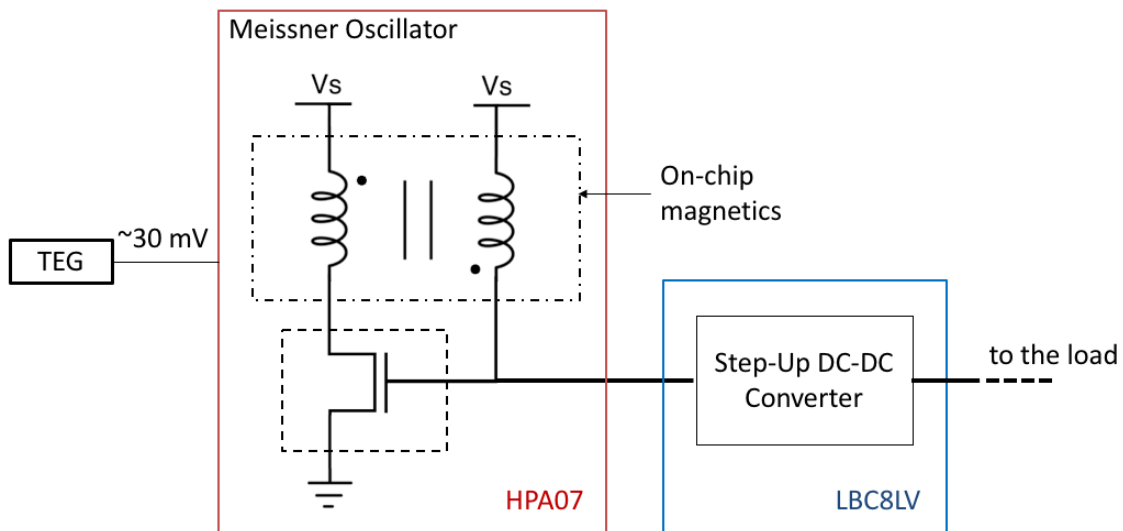
Figure 2-1: Block diagram of the energy harvesting charger

It is assumed that in the worst case, the Meissner Oscillator should be able to provide around 400 mV at the output. Since 400mV is not enough to directly power switches, the second stage is needed to step up the voltage from 0.4 V to 1.2 V, as per the requirements listed previously. The charge pump circuit operates from the output power provided by the Meissner Oscillator, steps up the voltage to 1.2 V, and stores it on a capacitor on chip.

2.3 System Level Architecture

The proposed system has the ability to be used as a stand alone charger for energy harvesting applications. The system architecture in such a case would be the same as shown in Figure 2-1. Output voltage regulation and power management capabilities can be added to it in the future, once the proof-of-concept has been tested successfully.

This system can also be used as an integrated cold-start stage for a subsequent boost converter, which would take over in regular operation for higher efficiency. System level architecture of the cold start system with the boost converter is shown in Figure 2-2.
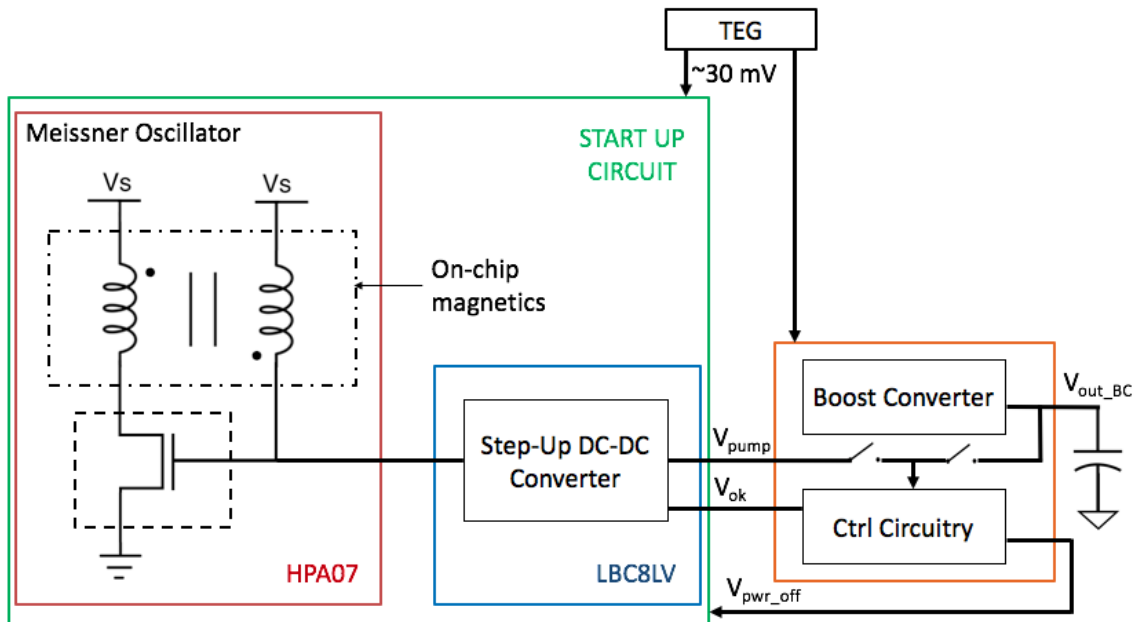
Figure 2-2: Block diagram of the start-up system with boost converter

Once the output voltage of the start-up system is above 1.2 V, it will send an output signal to the boost converter to indicate that the voltage is ready to be used. The control circuits in boost converter can then start consuming power from the SC DC-DC output capacitor and start up the boost converter, which will start charging its own output capacitor. If the boost converter takes too much power from the output

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and the voltage levels on the SC output capacitor drop, the V_{OK} signal needs to go low until the capacitor charges back up again. In such a case, the charge on the output capacitor of the boost converter would keep accumulating over multiple cycles.

Once the boost converter's output capacitor is charged up to the desired levels, it can be used to power the control circuits for self-sustaining operation, at which point the SC DC-DC circuit would no longer be needed. Therefore, once the hand over is complete, the boost converter can send a digital signal back to the SC DC-DC circuit to power it off.

The following chapters will discuss the individual design and implementation of the constituent blocks of the start up system: the Meissner Oscillator and the SC DC-DC circuit.

Chapter 3

Meissner Oscillator

3.1 Background

Meissner Oscillators, also known as Armstrong oscillators because of their similar topologies, are one of the oldest, classic LC oscillators [23]. They were invented in 1913 by Austrian Alexander Meissner in Germany, and Edwin Armstrong in the United States [24]. These days, Meissner Oscillators are used in many energy harvesting systems, both academically [9] and commercially [8].

A Meissner Oscillator consists of a transformer and a transistor, as shown in Figure 3-1. The secondary winding of the transformer forms an LC tank circuit with the gate capacitance of the transistor. A small AC voltage signal at the gate of the transistor translates into a change in current in the transistor, as well as in the primary branch. The primary coil of the transformer, also known as the ticker coil, then provides feedback to the secondary coil through magnetic coupling and a feedback loop is formed, which can lead to sustained oscillations. The oscillation condition for this configuration is discussed in Section 3.2.

A standard implementation of the Meissner Oscillator as a step-up converter is shown in Figure 3-2, where the oscillator is followed by a voltage doubler circuit for
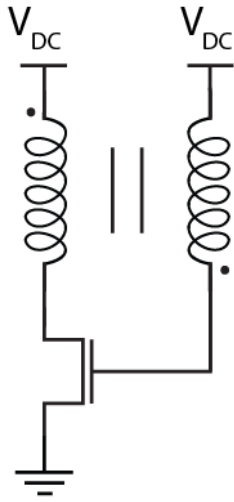
Figure 3-1: Miessner Oscillator circuit diagram

recitification. The oscillator produces sustained large signal oscillations at node V_x, which are positively offset by C1, rectified by the two diodes, and stored on C2 to provide a stable output voltage. Similar implementations were also used in [8, 9, 17].
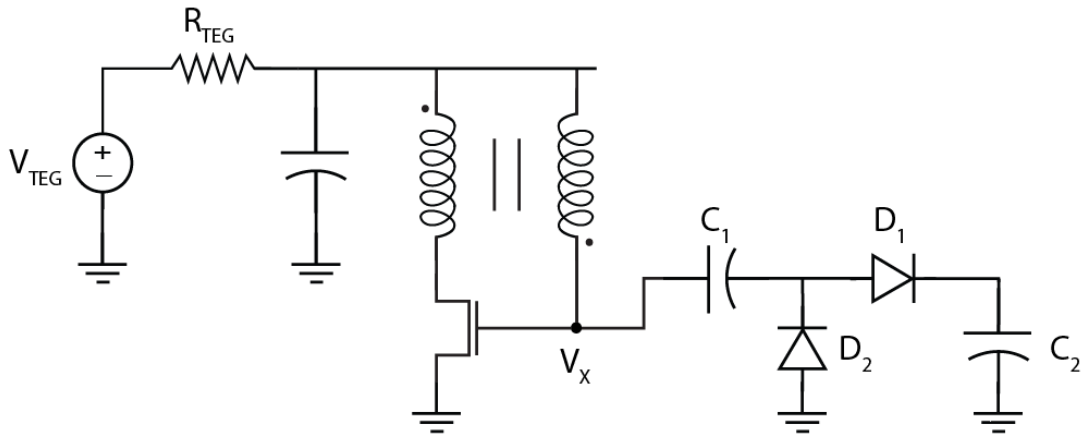
Figure 3-2: Miessner Oscillator step-up converter circuit diagram

3.2   Analysis for Optimization

To be able to predict the conditions under which the circuit will oscillate, open loop, small signal analysis was performed. The Meissner Oscillator feedback loop was broken at the gate of the FET, and a small AC signal was applied to it, as shown in Figure 3-3. The gate capacitance of the FET was added to the output for appropriate loading conditions.
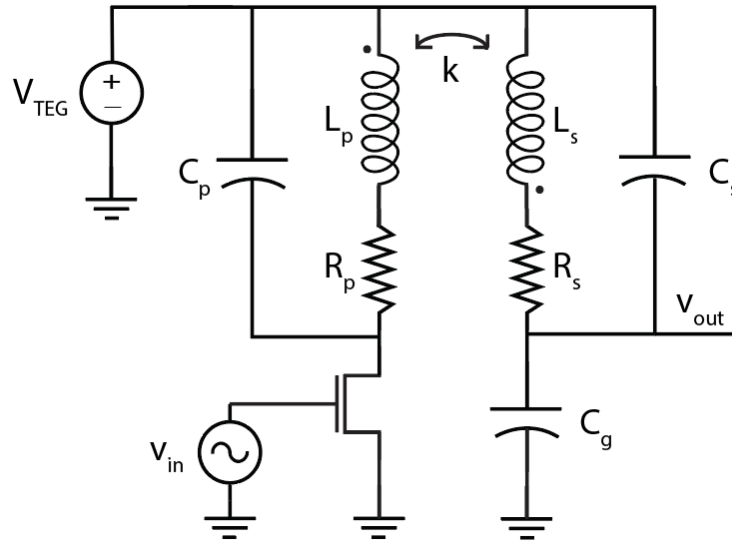
Figure 3-3: Miessner Oscillator for open loop analysis

3.2.1   Small Signal Analysis

The small signal model for the Meissner Oscillator is shown in Figure 3-4. The major parameters of the transistor and transformer that affect the oscillation condition, and need to be taken into account for optimization, are
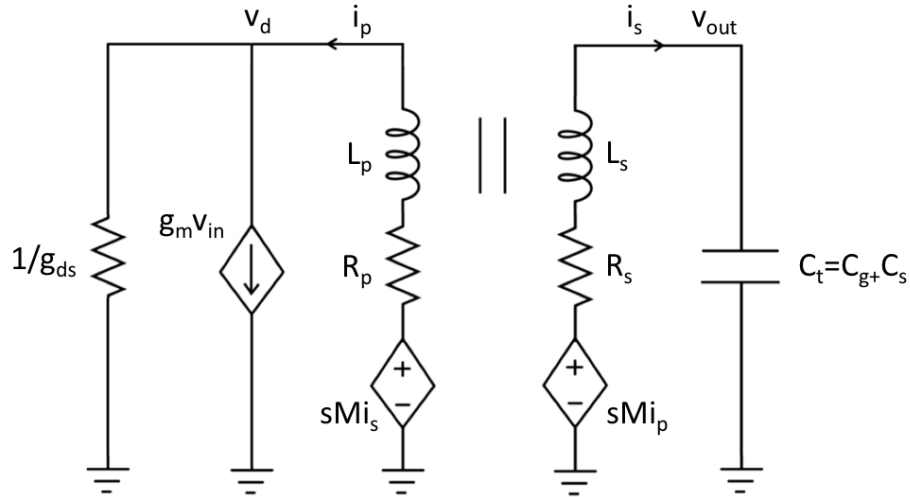
Figure 3-4: Small signal model of the Meissner Oscillator

g_m: Transconductance of the MOS transistor

g_{ds}:   Output conductance of the MOS transistor

C_g: Gate capacitance of the MOS transistor

L_p: Primary inductance of the transformer

L_s: Secondary inductance of the transformer

R_p: Resistance of the primary coil

R_s: Resistance of the secondary coil

C_s: Capacitance of the secondary coil

M: Mutual inductance of the transformer

k: Coupling factor between the primary and secondary windings, where

$$M = k\sqrt{L_p L_s} \tag{3.1}$$

The feedback diagram for this small signal model can be drawn, by inspection, as shown in Figure 3-5 a). This model can be simplified by 1) replacing the inner loop with its transfer function H_1 (refer to equation 3.2), and 2) combining the two

summation blocks at the input into one. The feedback diagram thus obtained is shown in Figure 3-5 b).

$$H_1 = \frac{1}{s^2 L_s C_t + s R_s C_t + 1} \tag{3.2}$$

The new formed inner loop can now be replaced with its transfer function, H_2, to obtain a simple feedback diagram with a single feedback loop, as shown in Figure 3-6. The transfer function H_2 can be written as

$$H_2 = \frac{1}{g_{ds}(s L_p + R_p) + 1} \tag{3.3}$$

Based on Figure 3-6, the transfer function from v_{in} to v_{out} can be written as

$$\frac{v_{out}}{v_{in}} = \frac{g_m H_2 s M H_1}{1 - H_1 H_2 s^3 M^2 g_{ds} C_t} \tag{3.4}$$

Substituting expressions from equations 3.2 and 3.3 into equation 3.4, the transfer function becomes

$$\frac{v_{out}}{v_{in}} = \frac{s M g_m}{(g_{ds}(s L_p + R_p) + 1)(s^2 L_s C_t + s R_s C_t + 1) - s^3 M^2 C_t g_{ds}} \tag{3.5}$$

This three pole system is complicated for hand-analysis, and not useful for gaining intuitive understanding of the oscillation condition. Therefore, the transfer function needs to be simplified to a two pole system through reasonable assumptions, which can later be verified numerically for an appropriate range of parameters. In order to do this, we can temporarily revert to the analysis with an ideal transistor, that has $g_{ds} = 0$. The transfer function for the simplified model becomes

$$\left.\frac{v_{out}}{v_{in}}\right|_{g_{ds}=0} = \frac{s M g_m}{s^2 L_s C_t + s R_s C_t + 1} \tag{3.6}$$

At resonance, the complex conjugate poles of the system lie on the $j\omega$ axis in a root
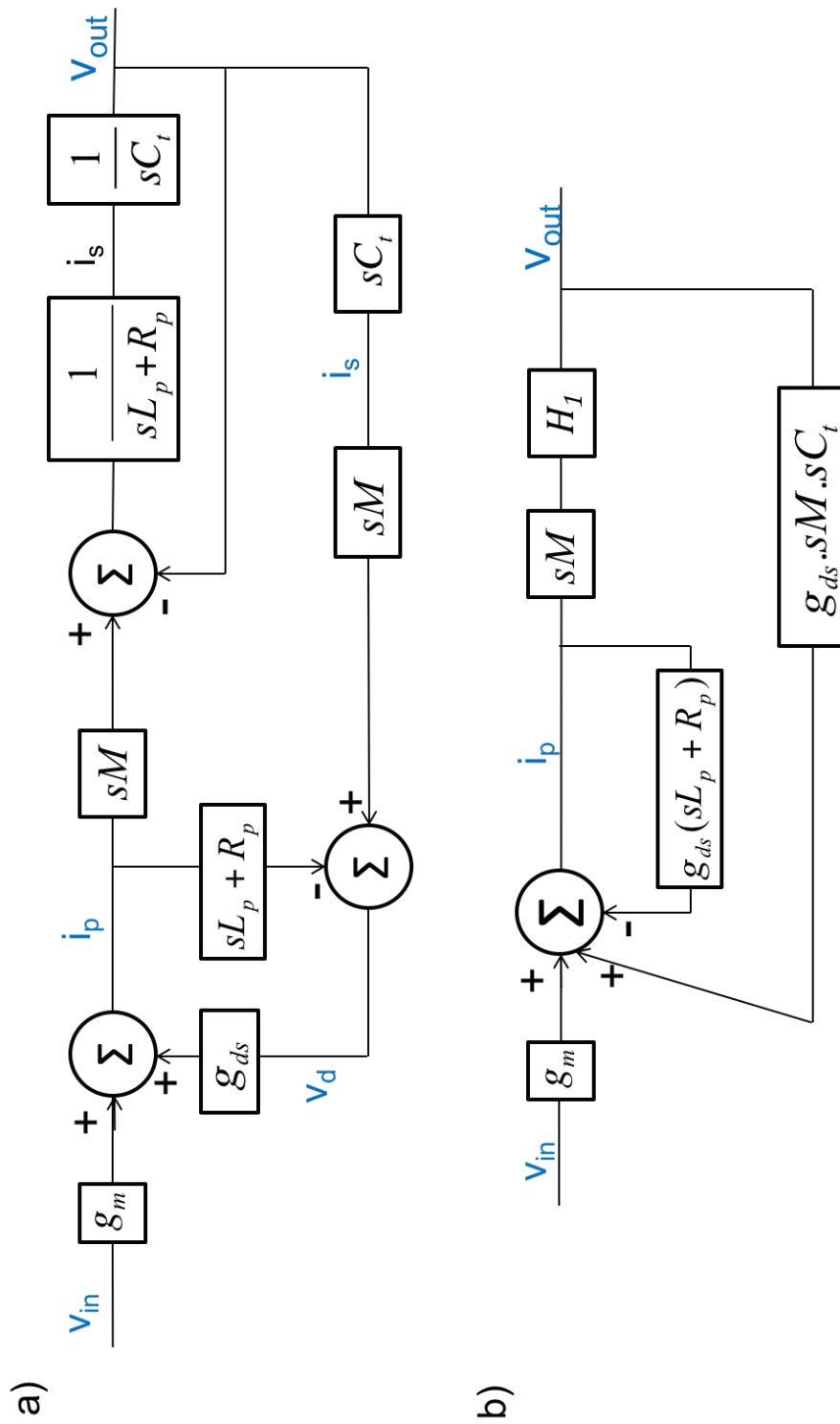
Figure 3-5: Feedback diagram of the Meissner Oscillator a) Basic version b) After initial simplification steps
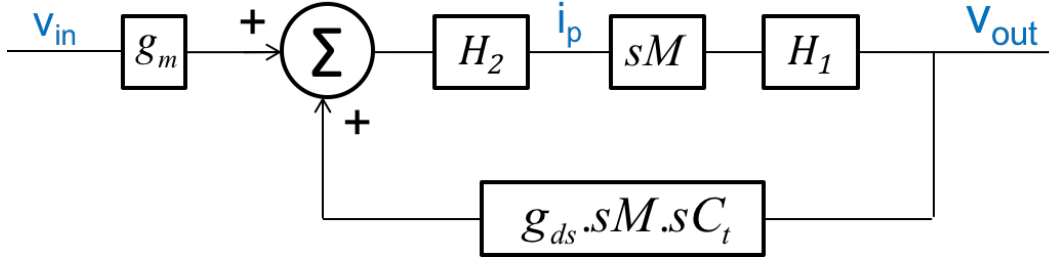
Figure 3-6: Simplified feedback model of the Meissner Oscillator

locus plot. So, the resonant frequency of the system can be written as

$$\omega_r = \frac{1}{\sqrt{L_s C_t}} \tag{3.7}$$

Then, the loop gain at resonance becomes a real term, that is

$$\left.\frac{v_{out}}{v_{in}}\right|_{g_{ds}=0,\omega=\omega_r} = \frac{M g_m}{R_s C_t} \tag{3.8}$$

Note that $g_{ds} = 0$ is not a realistic situation, and equation 3.8 is not an accurate representation of the system's behavior, as shown in the following section. However, g_{ds} should not have a significant impact on the resonant frequency of the system. Assuming that the resonant frequency has not changed much between the two-pole system in equation 3.6 and three-pole system in equation 3.5, we can substitute the frequency from equation 3.7 into the transfer function in equation 3.5, where $s = j\omega$. Doing so and simplifying, the transfer function becomes

$$\left.\frac{v_{out}}{v_{in}}\right|_{\omega=\omega_r} = \frac{j\omega M g_m}{j\omega(g_{ds}R_p R_s C_t + R_s C_t + g_{ds}L_p k^2) - g_{ds}R_s \frac{L_p}{L_s}} \tag{3.9}$$

The assumption that the resonant frequencies are similar in the two cases will hold true if the second term in the denominator of equation 3.9 is negligible compared to the first term. This is indeed the case for both on-chip and off-chip transformers at low DC input voltages, as per the scope of the work. Therefore, neglecting the second

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term in the denominator, the transfer function from v_{in} to v_{out} reduces to a purely real term, which represents the loop gain of the system. Using equation 3.1, we can write this loop gain as

$$\text{Loop gain} = g_m \left(\frac{R_s C_t (g_{ds} R_p + 1)}{k\sqrt{L_p L_s}} + g_{ds} k \sqrt{\frac{L_p}{L_s}} \right)^{-1} \qquad (3.10)$$

In theory, the system should oscillate if the loop gain is greater than one. But in practice, we need the loop gain to be sufficiently greater than one for sustained oscillations. Nevertheless, from equation 3.10, the oscillation requirement can be written as

$$g_m \left(\frac{R_s C_t (g_{ds} R_p + 1)}{k\sqrt{L_p L_s}} + g_{ds} k \sqrt{\frac{L_p}{L_s}} \right)^{-1} > 1 \qquad (3.11)$$

If we refer to the first term in the brackets as A, and the second term as B, then the sum A+B needs to be minimized, and g_m should be maximized, in order to meet the oscillation condition. However, the two terms are not independent of one another. Changing transformer parameters to reduce one term typically ends up increasing the other one. For example, increasing the number of turns on the secondary coil of the transformer to reduce term B will increase L_s and reduce k, but also raise R_s and C_s, thereby increasing term A, as explained in Section 3.4. Therefore, the optimal solution can be reached when the two terms become equal, i.e. A = B. This direction has been followed to optimize the transistor and transformer for low voltage operation.

3.2.2 Verification and Validation

The loop gain expression derived in the previous subsection can in developing an intuitive sense of which direction to make changes in, in order to achieve the desired results. However, the analysis first needs to be verified and validated by comparison against simulations results, to confirm its accuracy.

The transfer function in equation 3.5 was compared to Cadence simulation results
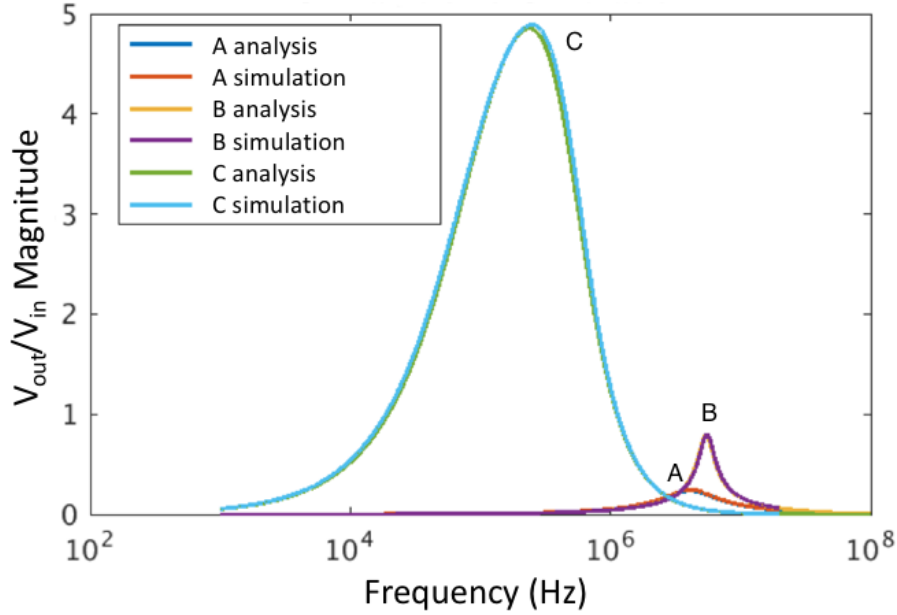
Figure 3-7: Verification of the transfer function v_{out}/v_{in} in equation 3.5, for various transformers

for an open loop AC analysis. The magnitude of $\frac{v_{out}}{v_{in}}$ is plotted in Figure 3-7, over a range of frequencies, for three different transformers:

1. Transformer A: On-chip transformer with an aspect ratio of 2:1, effective turns ratio 1:52

2. Transformer B: On-chip transformer with an aspect ratio of 30:1, effective turns ratio 1:36

3. Transformer C: Off-chip, Coilcraft transformer [25] with turns ratio of 1:50

In all three cases, the plots were generated using the same input voltage of 20mV and the same model of a fabricated MOS device. The evaluation of the transfer function derived analytically matches very well with the results obtained from Cadence simulations for all three, geometrically varied transformers.

The next step is to ensure that the loop gain formulation is accurate and the neglected term does not significantly affect the final results. Figure 3-8 shows a comparison between the loop gain expression in equation 3.10, and the AC gain from
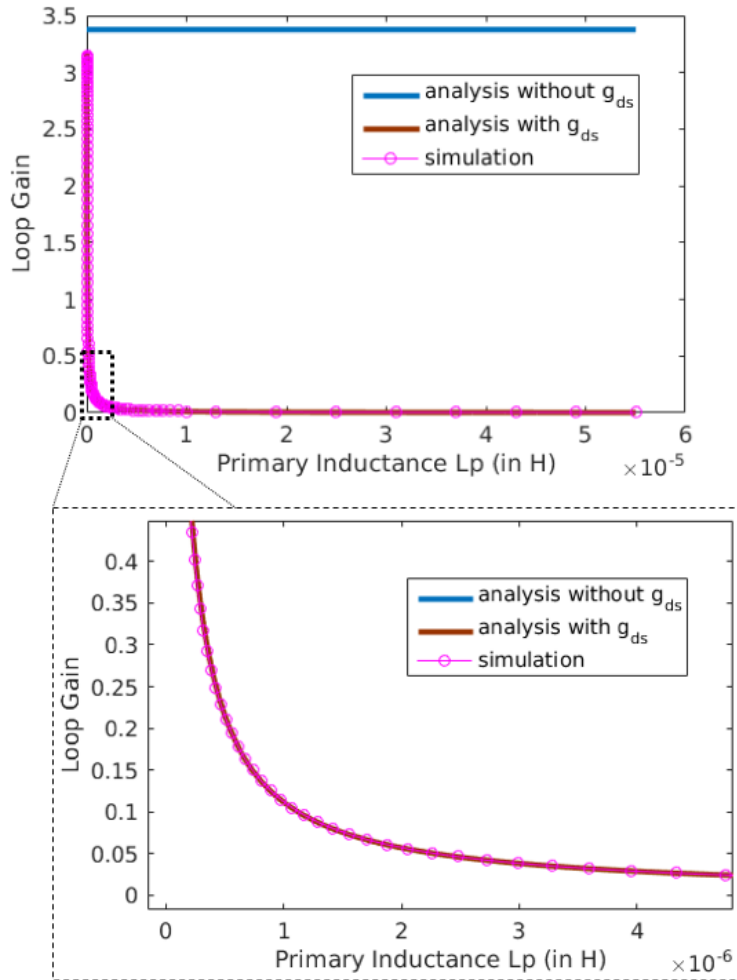
Figure 3-8: Verification of the loop gain expression in equation 3.10 as L_p is swept, keeping the product $L_p L_s$ constant

v_{in} to v_{out} at the resonant frequency, obtained from simulation. The evaluated and simulated loop gain is plotted across a range of values for L_p, with L_s modified at each point such that the product $L_p L_s$ stays constant. The plot shows excellent agreement between the analysis in equation 3.10 and the simulated results. It also shows how the analysis with $g_{ds} = 0$ in equation 3.8 is insufficient in predicting the behavior of the oscillator.

3.2.3 Significance

In most Meissner Oscillator converters published so far, there has been limited control over the design of the transformer, and therefore, little attention has been paid to it. The optimization of the transformer has generally been limited to selecting the turns ratio of off-the-shelf transformers, as in [8], [9], and [26]. But in going from the high quality off-chip transformers to lossy on-chip transformers, many new parameter trade-offs arise, which have been accounted for in this analysis.

The loop gain expression derived in equation 3.10 is valid for both on-chip and off-chip transformers, within the low voltage range for start-up, and forms a good basis for device optimization. However, even with the same loop gain expression, the optimization in the two cases can be very different. Since the off-chip transformers have a much higher quality factors and better coupling than the small on-chip transformers, the last term in the denominator of equation 3.10 is typically dominant. In contrast, for the on-chip transformers, either term may dominate. For example, in case of an off-chip Coilcraft transformer with a turns ratio of 1:50 (Transformer C), having a high quality factor and $k = 0.95$, the loop gain expression with a selected MOS device may be expressed as

$$\text{Loop gain}|_C \simeq \frac{g_m}{g_{ds}k}\sqrt{\frac{L_s}{L_p}} \simeq \frac{g_m N}{g_{ds}k} \tag{3.12}$$

where N is the turns ratio. In comparison, for an on-chip transformer with a similar effective turns ratio (Transformer A), but inherently having much lower inductance and higher resistance than the former, the loop gain expression with the same MOS device may come out to be

$$\text{Loop gain}|_A \simeq \frac{g_m k \sqrt{L_p L_s}}{R_s C_t (g_{ds} R_p + 1)} \tag{3.13}$$

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Significance for transformer optimization

With an off-chip transformer as per equation 3.12, the loop gain is directly proportional to the turns ratio of the transformer and inversely proportional to the coupling factor. While for a particular on-chip transformer, as per equation 3.13, the loop gain is independent of the turns ratio, and is directly proportional to the coupling factor. This shows how the design and optimization of a Meissner Oscillator with on-chip transformers vs. off-chip transformers can be quite dissimilar, and in this case, even contradicting.

Significance for transistor optimization

For the off-chip transformer example in equation 3.12, the most important feature of the transistor for a high loop gain is a high $\frac{g_m}{g_{ds}}$ ratio. Conversely, for the example with the on-chip transformer, an optimum transistor needs a high $\frac{g_m}{C_g}$ for a higher loop gain, rather than a high $\frac{g_m}{g_{ds}}$ ratio. This implies that the transistor needs to be optimized based on the transformer being used, and vice versa. In other words, the transistor and transformer need to be co-optimized.

3.3 Transistor Design

An ideal transistor has infinite transconductance and infinite output impedance. But practical transistors come with trade-offs instead. This section discusses the design and optimization of a transistor within the given resources.

3.3.1 Technology

The fluxgate transformer by TI, described in detail in the following section, is currently available only in one technology: HPA07. HPA07 is a 1.5μm process with a very high native NMOS threshold voltage, V_T. In order to have an integrated Meissner

Oscillator, the MOS transistor needs to be designed and fabricated in the same technology as the transformer. However, the native device in this technology will be in deep sub-threshold if operating from voltages down to 20-30 mV. So, a special depletion mode NMOS device is required.

Based on the V_T of the NMOS device, the region of operation of the transistor may change, as shown in Table 3.1. Therefore, we can target a V_T based on which region of operation can provide the best transistor performance.

Table 3.1: Region of operation for various MOS V_T values

Range of V_T	Region of Operation	Channel Inversion
$V_T > 20$ mV	Sub-threshold	weak to moderate
$0 > V_T > 20$ mV	Above threshold, saturation	moderate
$V_T < 0$	Above threshold, linear	moderate to strong

3.3.2 Optimization

Threshold Voltage

Based on the loop gain expression in equation 3.10, the transistor should have a high transconductance, a high output resistance, and a low gate capacitance. There are several MOS models that can help in predicting the optimal V_T to achieve the desired MOS characteristics, and the following models were considered for this task:

1. **Linear Approximation Models**: These are the most widely used models for hand-analysis, and provide approximate models for each region of operation: linear or saturated, above or sub threshold. However, they do not work well at the boundaries of two different regions, and hence they are not appropriate for predicting optimal V_T in moderate inversion.

2. **EKV Model**: An EKV model, as described in [27], provides a unified MOS model that works in all regions of operation. In its most simplified version, the

EKV model builds on the linear approximation model and provides a means of smoothing out the transitions between different regions of operations.

3. **BSIM Model**: BSIM models were developed in 1987 for use in SPICE simulations [28], and newer versions of it are very commonly used in PDKs around the world today. The BSIM models require a much larger number of parameters to be specified than the other two models, and can therefore be much more complicated.

In the absence of a MOS model to simulate, the EKV model provided a good compromise between accuracy and simplicity in predicting which region of operation would offer the highest transistor gain. Basic parameters extracted from I-V curves of the HPA07 technology were used in the model, with calibration. A plot of g_m and $\frac{g_m}{g_{ds}}$ evaluated across a range of V_T values obtained with a calibrated EKV model is shown in Figure 3-9. The first plot shows that the highest g_m is achieved at $V_T = -180mV$. At a supply voltage of 20 mV and $V_T = -180mV$, the NMOS will operate in the linear regime, and therefore its output resistance must be low, as confirmed by the second plot. Once again, how important the output resistance of the transistor is, depends on which transformer it is used with. As a first estimate, $V_T = -180mV$ was targeted for fabrication of the NMOS device, with varied lengths and widths.
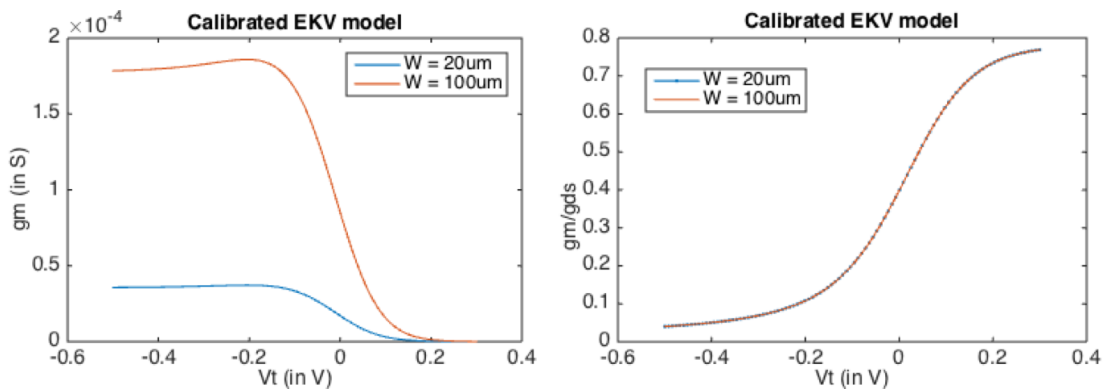
Figure 3-9: g_m and $\frac{g_m}{g_{ds}}$ vs. V_T in an EKV model

Transistor Size

In strong inversion, linear regime, the drain current of NMOS is given as

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3.14}$$

Then, the transconductance can be written as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{3.15}$$

whereas the output conductance becomes

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T - V_{DS}) \tag{3.16}$$

Also, the gate capacitance is can be written as a function of width and length as

$$C_g \propto WLC_{ox} \tag{3.17}$$

From equations 3.15-3.17, it can be seen that g_m, g_{ds}, and C_g are all directly proportional to the width of the transistor. Therefore, increasing the NMOS width to get higher current and higher transconductance will also result in higher gate capacitance. However, while g_m and g_{ds} are inversely proportional to the length, C_g is directly proportional to it. So, reducing the length can improve both g_m and C_g metrics of the transistor at the same time. Therefore, a negative threshold voltage along with a lower gate length is desired.

3.3.3   Fabrication and Measurements

TI fabricated special transistors on six different wafers for this work, using low-V_T implants and a range of substrate doping levels to achieve low threshold voltage. The

fabricated MOS devices have lengths ranging from 0.4 um to 2.2 um, which also affect the threshold voltage level through V_T *roll off*, a phenomenon that lowers the threshold voltage of devices with shorter channel lengths. Additionally, the fabricated MOS devices range in width from 1 mm to 8 mm. A snapshot of one of the wafer sites containing FETs with different widths and lengths is shown in Figure 3-10. The standard size of each FET including the four bond pads is 540 um x 270 um, but special 20 um wide devices were also fabricated for measurement and calibration purposes.

Figure 3-10: Some fabricated NMOS transistors in a variety of sizes

Between the different combinations of substrate doping levels and gate lengths, a large set of threshold voltage levels was achieved for the NMOS devices. Based on the measurements made with V_{DS} and V_{GS} in 20 mV range, it was found that once of the fabricated devices (device X), with average $V_T = -180mV$ and a gate length of $0.5\mu m$, had the highest g_m per width out of all the fabricated transistors, as predicted analytically in the previous section. At the same time, it had a low $\frac{g_m}{g_{ds}}$ ratio, also in line with what the simple MOS models predicted.

Another fabricated device (device Y) with a threshold voltage of -50 mV and a

gate length of $1.1\mu m$, displayed the highest $\frac{g_m}{g_{ds}}$ value. But the drain current and transconductance normalized to unit width of this device were both lower than that of device X. The higher drain current in X can lead to a higher voltage drop across the primary coil, and therefore less drain voltage being available to the NMOS, ultimately leading to a lower g_m value. One way of having a fair comparison between devices X and Y in hand calculations is to pick their widths such that the drain currents are similar. Doing so, device Y exhibits a higher g_m as well as a higher $\frac{g_m}{g_{ds}}$ value, while device X offers a much smaller gate capacitance.

As mentioned in Section 4.2.3, the optimal transistor needs to be picked keeping in mind the transformer that it is to be used with. In analysis, on-chip transformers are seen to provide a higher loop gain with device X than Y, while off-chip transformers are found to favour device Y. Some experimental results with an off-chip transformer and device Y are discussed in Section 4.5.

3.4 Transformer Design

3.4.1 Fluxgate Technology

TI has developed new integrated magnetic fluxgate sensors, which are currently being used in products for current sensing applications. Their fluxgate inductor consists of a high permeability magnetic core made of permalloy sitting above the top metal, and having copper windings around it, as shown in Figure 3-11.

The same fluxgate technology can be used as a transformer in the Meissner Oscillator circuit, to have a fully integrated, low voltage start-up solution. The transformer can be formed by extending the core and adding another set of copper windings adjacent to the previous one, or by having primary windings in the middle surrounded by secondary on either side for better magnetic coupling, as shown in Figure 3-12. The top copper layer can be bonded out to the pads if needed.

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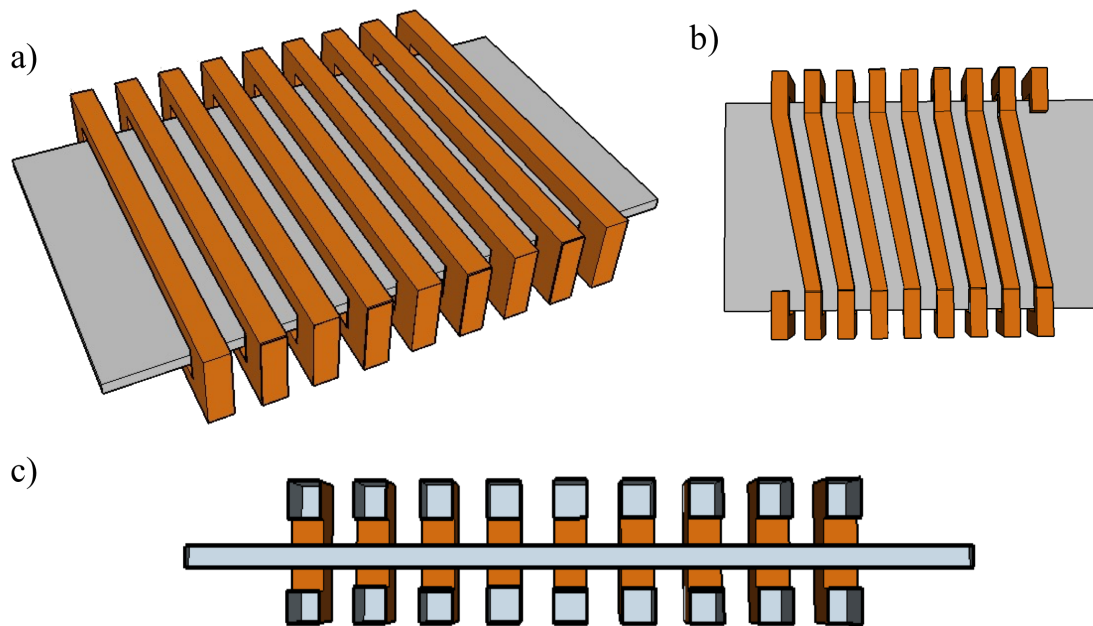
Figure 3-11: Fluxgate inductor having a permalloy core, and copper windings around it a) 3-D view, b) bottom view, c) cross-sectional view
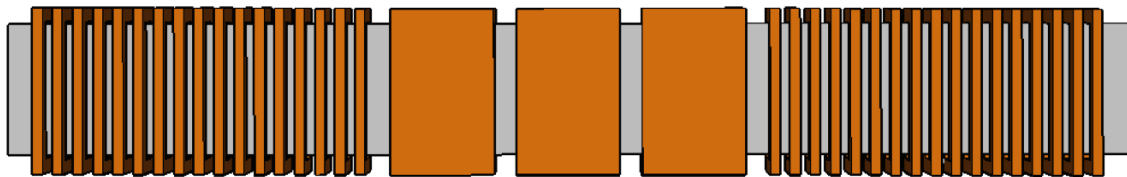
Figure 3-12: Top view of a fluxgate transformer

There are many parameters in the fluxgate technology that can affect the transformer design. Most of these parameters are pre-defined by technology limitations or cost considerations, including height of the copper windings, minimum width of the copper windings, minimum spacing between the windings, spacing between the windings and the core, height of the core, and so on. However, there are still a few important parameters that can be modified to optimize the transformer design, which are listed below, and will be discussed further in the following section.

- W_s: Width of the secondary metal windings

- W_p: Width of the primary metal windings

- N_s: Number of turns on the secondary

- N_p: Number of turns on the primary

- W_{core}: Width of the magnetic core

3.4.2   2-D Design Challenges

When going from off-chip transformers to integrated magnetics, new design challenges arise because of the limitations of the 2-D space. One limitation manifests itself as fringing fields, which affect on-chip transformers to a much higher degree than off-chip ones. In a 2-D transformer, not all of the magnetic flux passing through one turn can be assumed to pass through the adjacent turn. For longer transformers, this effect becomes even more pronounced as very few field lines are able to make it all the way to the edges of the magnetic core, and most of the magnetic field lines exit the core from somewhere in between.

This implies that there are a lot more design trade-offs to be considered in 2-D transformer optimization. Table 3.2 shows how changing a single parameter can affect an on-chip transformer vs. off-chip. For example, while designing an off-chip transformer, the secondary resistance can be reduced by increasing the width of the secondary winding. It might increase the secondary capacitance, but it does not affect any other parameter by much. However, for an on-chip transformer limited to a 2-D space, increasing the width of the secondary winding would mean increasing the length of the transformer, given that the number of turns and spacing between them stays constant. Therefore, it can not only increase the capacitance, but it can also reduce the secondary inductance, along with the coupling factor.

In addition to the geometrical parameters listed in Table 3.2, core width is also an important design parameter. Reducing the width of the core alone can reduce all of

Table 3.2: Design trade-offs for 2-D vs. 3-D transformers

Change in geometry	Effect on electrical parameters									
					On-chip			Off-chip		
	R_p	R_s	C_p	C_s	$L_{p,on}$	$L_{s,on}$	k_{on}	$L_{p,off}$	$L_{s,off}$	k_{off}
$W_s \uparrow$	-	↓	-	↑	-	↓	↓	-	-	-
$W_p \uparrow$	↓	-	↑	-	↓	-	-	-	-	-
$N_s \uparrow$	-	↑	-	↑	-	↑	↓	-	↑	-
$N_p \uparrow$	↑	-	↑	-	↑	-	↑	↑	-	-

the transformer's circuit model parameters: R_s, C_s, R_p, C_p, L_p, L_s, and k. So, the decision of whether or not to reduce/increase the core width, or any other parameter, depends on whether the benefits of reducing the resistance and capacitance outweigh the cost of having lower inductances. The loop gain expression derived in equation 3.10 can help in making that decision at every point in the optimization process.

3.4.3 Optimization

TI provided a list of 16 transformers that were simulated for another application, as a starting point for this work. The list provided information about the transformer geometry, as well as the electrical parameters, which could be analytically evaluated for use with the Meissner Oscillator. Even though the transformers were designed for a different application in mind, the large spread of geometrical parameters provided a good direction for further optimization.

An important step of transformer design is to be able to predict the electrical parameters for a given transformer geometry. This is relatively straightforward to do for resistance. For example, the resistance of the secondary winding can be given as

$$R_s \simeq \frac{2\rho_{Cu} W_{core} N_s}{W_s H_{Cu}} \tag{3.18}$$

The same can also be done for the capacitance. But creating a lumped equivalent

model of the transformer from a distributed LCR network ladder becomes rather complicated. Through magnetics analysis performed by Mohammad Araghchini, it was found that the total capacitance was dominated by winding-to-core capacitance, while the capacitance between two adjacent windings was negligible. Based on this information, the capacitance can be reliably estimated through scaling the capacitance of a measured reference transformer:

$$C_s \simeq C_{ref} \frac{W_{core}}{W_{core,ref}} \frac{W_s}{W_{s,ref}} \frac{N_s}{N_{s,ref}} \qquad (3.19)$$

However, the self-inductance and mutual inductance values can be difficult to predict analytically. Given the non-ideal behavior of the magnetic field lines in the fluxgate transformer, the inductance values and coupling factor scale in a highly non-linear fashion. This necessitates the use of a simulator to assist in transformer design. Hence, a Finite Element Analysis based software, Maxwell, was used in this work to simulate and validate transformer designs. The same software was also used by TI in their simulations, and successfully tested for accuracy using measured data.

Using the loop gain analysis and Maxwell simulator, many different transformer designs were evaluated for use with the optimal transistors. The best one by far has a core length of 2.5 mm and occupies a total area less than $1mm^2$, as shown in Table 3.3. It has a loop gain $\simeq 1.8$ from a supply of 20 mV, when paired with FET X. In theory, this loop gain should be enough for oscillations. But more robust operation can be achieved with a higher supply voltage, like 30 mV. Some other techniques that were explored for improving the transformer, and therefore the Meissner Oscillator performance, include interleaving and using a toroidal structure.

Table 3.3: Optimized fluxgate transformer vs. off-chip transformer parameters

	L_p	L_s	R_p	R_s	Area	$\sqrt{\frac{L_s}{L_p}}$
Optimized fluxgate	30 nH	24 μH	0.46 Ω	263 Ω	$< 1\ mm^2$	28
Coilcraft 1:50 [25]	12.5 μH	31 mH	0.085 Ω	200 Ω	36 mm^2	50
Coilcraft 1:100 [25]	7.5 μH	75 mH	0.085 Ω	340 Ω	36 mm^2	100

Interleaving

As discussed in section 3.4.2, the magnetic field lines in a 2-D fluxgate transformer tend to leak out of the core prematurely, rather than exiting through the ends, especially in long transformers. Hence, for transformer structures where the primary coils are placed together in the middle, surrounded by secondary on each side (refer to Figure 3-12), the field lines generated in the primary coils do not pass through all of the secondary turns, and the coupling factor is low.

This coupling factor can be improved by interleaving the primary and secondary windings, as shown in Figure 3-13. However, since the primary windings are now further apart, there will be less coupling between the primary turns, and therefore the primary inductance will decrease. So the overall gain in coupling factor gets nullified by the loss in primary inductance. This was confirmed by Jorge Troncoso and Nachiket Desai through Maxwell simulations. Since the term $k\sqrt{L_p}$ occurs together in all terms of the loop gain expression in equation 3.10, interleaving was found to provide little benefit overall.
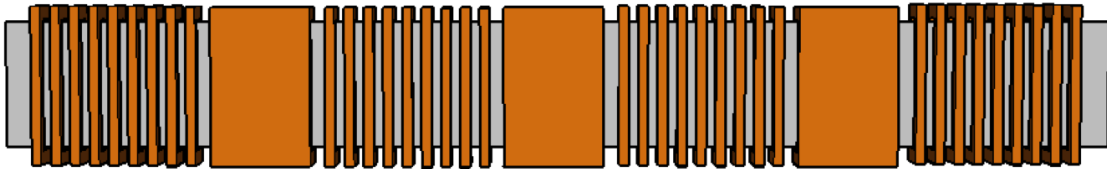
Figure 3-13: Interleaved transformer structure

Using toroidal structures

The magnetic field lines in a solenoidal structure have a long return path through the air once the field lines exit at the edges. Having a toroidal structure can reduce the return path through air by providing an alternative magnetic path. This should reduce the flux leakage between windings, and therefore improve the inductance values and the coupling factor.

Having a true toroidal structure needs a radial magnetic field for improving the transformer performance, so that all directions can be considered hard axis. However, with uni-axial magnetic fields, one direction of alignment becomes the hard axis, while the perpendicular direction becomes the easy axis, as described in Chapter 1. So in order to get the benefits of a toroidal structure in absence of a radial magnetic field, two solenoidal transformers were placed parallel to each other, as shown in Figure 3-14.
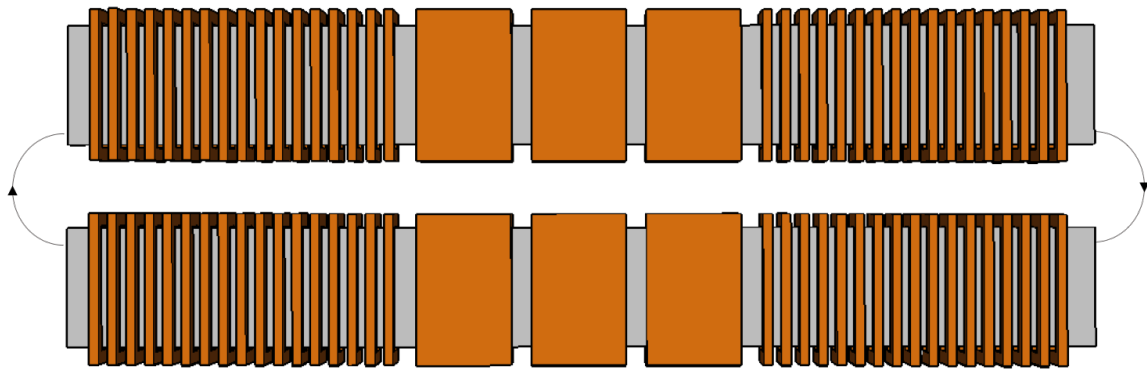
Figure 3-14: Toroidal transformer structure

The proposed toroidal structure is expected to increase the coupling factor and inductance values of the transformer. However, simulating the structure in Maxwell, by Nachiket and the author, showed little improvement in the either of them. The two main reasons behind this are

1. **The long length of the transformer**: The magnetic field lines find a short

path through air to be a lower reluctance path than the much longer path through the magnetic core, so they fringe out before getting to the ends of the core. When very few magnetic field lines are reaching the ends, there is little benefit seen in reducing the the return path for them.

2. **The short height of the core**: In 2-D flux gate transformers, the height of the core is very small compared to the width, so most of the magnetic field lines go back vertically instead of horizontally. Even though the return path through the air is reduced in the horizontal plane by having a toroidal structure, the overall benefit is not considerable.

Despite its inefficacy in improving flux linkage, the toroidal structure remains a useful technique for transformer design as it provides a means of breaking up long transformer structures into smaller parts, which can enable reduction of the square die area.

3.5   Intermediate Measurement and Testing

The optimized fluxgate transformers are in the process of layout for fabrication, so that the complete system can be tested on board, along with the switched capacitor DC-DC circuit, which is also currently in fabrication. At this time, some preliminary testing of the Meissner Oscillator has been completed using a fabricated MOS device and an off-chip transformer to validate the analysis and compare the performance with the state-of-the-art. Some parasitic estimation has also been done to predict the results of board-level integration of the Meissner Oscillator.

3.5.1   PCB Demo with Discrete Components

A printed circuit board (PCB) was designed to test the fabricated MOS device in a Meissner Oscillator configuration with discrete off-the-shelf components. The board

shown in Figure 3-15 consists of the oscillator and rectifier from Figure 3-2. The IC on the board contains a large number of MOS devices, out of which device Y of width 5000 um was used in conjunction with a 1:100 turns ratio Coilcraft transformer, the same as was used in [8, 9]. The size of the output capacitor used in the rectifier circuit was 1 nF. The loop gain of this oscillator based on equation 3.10 should be 9.5 at an input voltage of 20 mV.
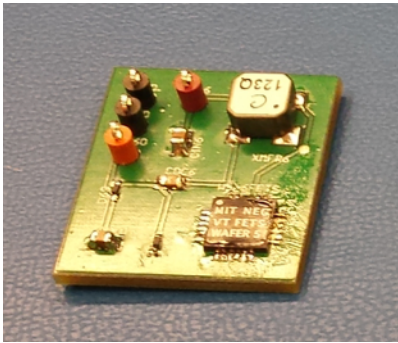
Figure 3-15: Meissner Oscillator with discrete components

The results presented in this section were obtained with ideal DC input voltages (no source resistance) and step inputs. However, the circuit has also been tested with a source resistance of 1Ω and RC delay of $1\mu s$ to make sure that the oscillations start autonomously and not because of the step inputs. Additionally, the PCB demo was successfully tested with a 15mm x 15mm TEG [29] placed on the wrist, which powered the Meissner Oscillator from the temperature differential between the skin and the air.

DC Measurements

The data presented in this section was obtained using an off-chip transformer with 1:50 turns ratio instead of 1:100. A DC voltage was provided to the Meissner Oscillator using a Keithley 2400 SourceMeter, and the voltage at the output capacitor after rectification was measured using another Keithley meter with zero source current.

The efficiency of the Meissner Oscillator over a range of input and output voltages is shown in Figure 3-16. The efficiency of Meissner Oscillators is generally much lower

than that of a boost converter, as can be seen in the plot. At an input voltage of 20 mV and an up-conversion ratio of 60, the peak efficiency is 24%. However, using a transformer with N=100, the same efficiency and output voltage levels are obtained at half the input voltage.
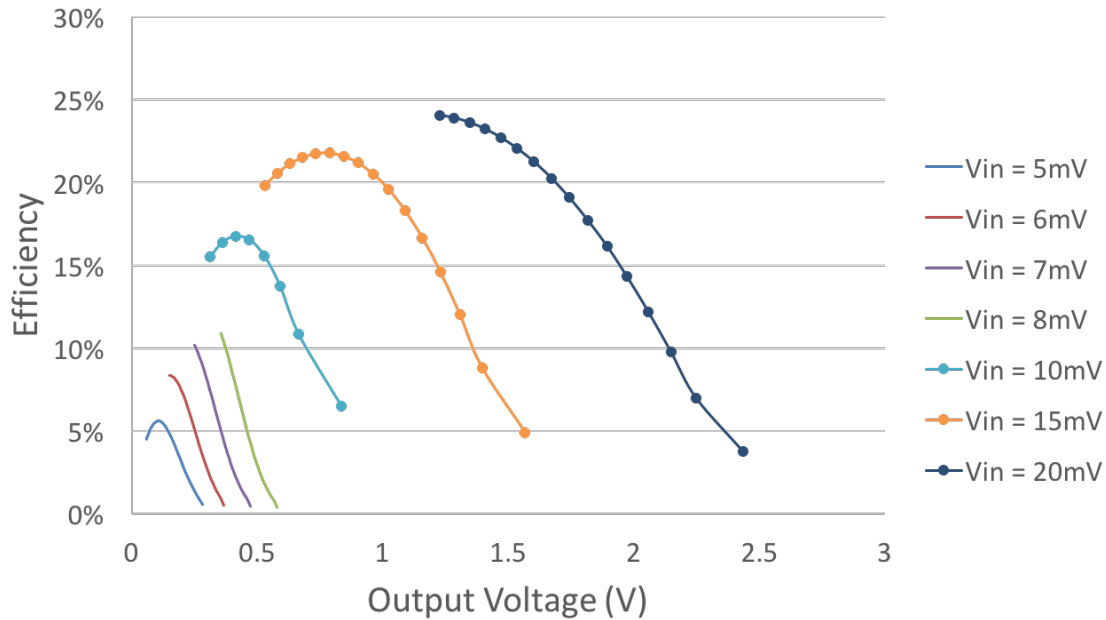
Figure 3-16: Meissner Oscillator efficiency for off-chip transformer with N=50

To be used as a cold start system, a more important metric for the Meissner Oscillator is its start-up time rather than efficiency. To get an idea of the lower limit of start-up times to expect, the waveform at the output capacitor node was captured using an oscilloscope in no-load conditions. The rise times of the output voltage at two different input voltages are presented in Table 3.4.

Table 3.4: Meissner Oscillator rise times in no-load condition

V_{IN} (mV)	V_{OUT} (V)	Time (ms)	
		$0 \rightarrow 50\%\ V_{OUT}$	$0 \rightarrow 90\%\ V_{OUT}$
5	0.23	0.2	1.3
10	0.73	0.14	0.46

AC Measurements

Similar to the previous DC measurement set-up, a DC voltage was provided to the Meissner Oscillator using a Keithley source meter. The voltage signal at the gate of the MOS device was measured with an oscilloscope using 8 pF probes, with no load current being drawn from the rectified output. The waveforms captured at different source voltages are shown in Figure 3-17. Some of the waveform data for the PCB demo is also summarized in Table 3.5.

Figure 3-17: PCB demo measurements: Meissner Oscillator output signal

Table 3.5: Measured oscillation data from PCB demo

Input Voltage V_{in} (mV)	Input Power P_{in} (μW)	Frequency (Hz)	V_{p-p} (V)	V_{max} (V)	Duty Cycle
20	21	70	5.8	2.7	59
15	10	71	4.2	2.0	58
10	3.6	73	2.6	1.2	56
5	0.65	75	1.2	0.6	54
3	0.21	75	0.7	0.5	53

The shape of the waveforms is consistent with those obtained through transient simulations, as shown in Figure 3-18. Since the MOS transistors were specially fabricated, there were no MOS models available for simulation. Instead, predictive

BSIM models were modified to match the I_D-V_{GS}, g_m-V_{GS}, and g_{ds}-V_{DS} curves in order to simulate the closed-loop non-linear behavior of the Meissner Oscillator. Since the models were developed for getting a general idea of the system rather than for high accuracy, the discrepancies in the measured vs. simulated results can be accounted for by imperfect modeling of the MOS devices.
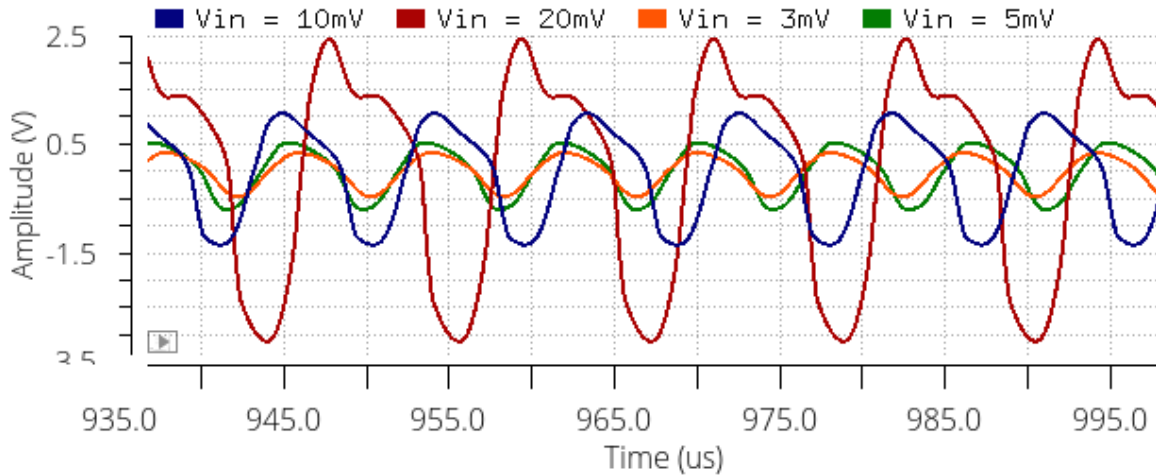
Figure 3-18: Transient simulation results with N = 100 off-chip transformer

For comparison of this Meissner Oscillator performance with that in LTC3108, the gate of the MOS device in LTC3108 was probed using an LTC evaluation kit, DC2042A. The Meissner Oscillator was disconnected from the rectification circuit by de-soldering a capacitor, so that the oscillator was no longer being self-loaded by the LTC3108 power management chip. The resulting waveforms are shown in Figure 3-19. Some oscilloscope measurements recorded at different input voltages are summarized in Table 3.6.

A comparison between the measurement results of the PCB Demo and the LTC3108 evaluation kit from Figures 3-17 and 3-19 shows that the positive area under the curve for $V_{in} = 20mV$ is similar for both LTC3108 and the PCB demo, which implies that the potential output power of the oscillators should be about the same. However, based on the corresponding input power levels in Tables 3.5 and 3.6, the LTC3108 oscillator
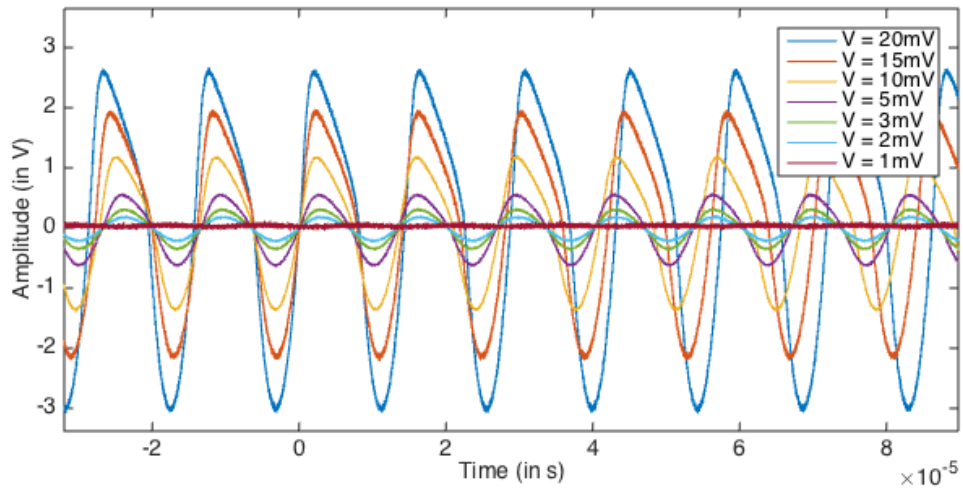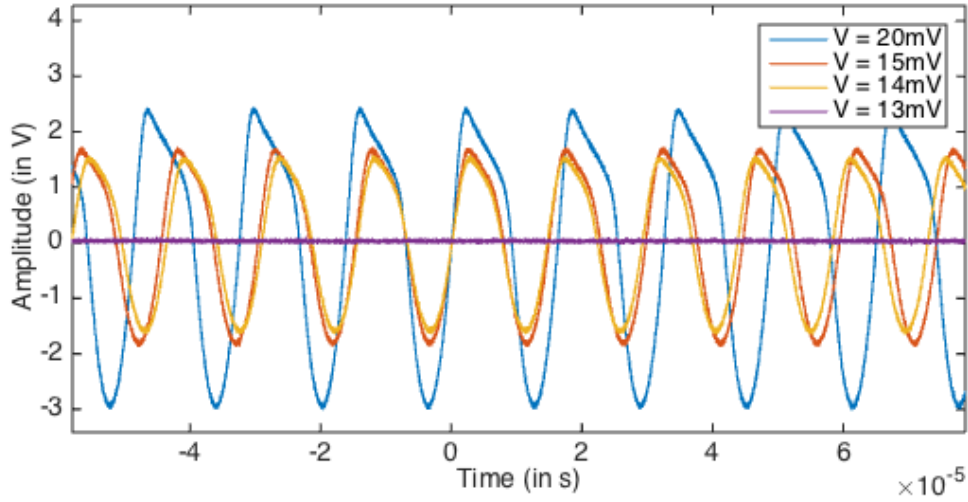
Figure 3-19: LTC3108 evaluation kit measurements: Meissner Oscillator output signal

Table 3.6: Measured oscillation data from LTC3108

Input Voltage V_{in} (mV)	Input Power P_{in} (μW)	Frequency (kHz)	V_{p-p} (V)	V_{max} (V)	Duty Cycle
20	27	62	5.5	2.5	59
15	12	67	3.7	1.7	55
14	11	69	3.3	1.6	53
13	13	N/A	N/A	N/A	N/A
10	8	N/A	N/A	N/A	N/A

needs 30% more power than the PCB demo. For $V_{in} = 15mV$, the PCB demo delivers 18% higher positive area under the curve than LTC3108, while consuming 16% less power. Based on these results, the PCB demo seems to be more efficient than LTC3108, in the specified testing conditions.

A more important metric than efficiency for this Meissner Oscillator is the start-up voltage. From Figures 3-17 and 3-19, when the DC input voltage for the two boards is under 14 mV, the LTC3108 oscillator fails to yield any noticeable oscillations. On the other hand, the PCB demo starts up and reports oscillations of 700 mV_{p-p} from an input voltage of 3 mV. It is able to start oscillating even from 2mV supply with 500 mV_{p-p} amplitude under no load condition. These results are important for the

following reasons:

1. They show that the fabricated MOS device works as expected and allows the oscillator to start up at much smaller voltages than the start-of-the-art, which in turn lends credibility to the analysis.

2. Since the oscillator starts up at such small voltages using the optimized transistor with an off-chip transformer, the results support the possibility of achieving 30 mV start-up using non-ideal fluxgate transformers.

3.5.2   Board Level Integration

For proof of concept, the fabricated MOS device, the fabricated fluxgate transformer, and the charge pump chip will all be connected at the board level. This means that the Meissner Oscillator will suffer from much higher parasitics compared to an integrated solution. The sources of parasitics for the fluxgate transformer connected on a board include the bond wire, the packaging parasitics, and the PCB traces, while the parameters most affected by the parasitics will be the primary resistance, the primary inductance, and the secondary capacitance. Since the secondary inductance and resistance values are much higher, the effect of parasitics on these parameters will be negligible.

For successful board level integration of the Meissner Oscillator, it is important to estimate how these parasitics will impact the oscillator performance. With resistive, inductive, and capacitive parasitics for a typical 1 mil (25 μm) diameter gold bond-wire of length 2 mm, a 16-pin QFN package, and small PCB traces, the loop gain of the Meissner oscillator is expected to reduce by less than 20 %. But since the loop gain margin is already tight with the fluxgate transformer, the additional parasitics can considerably effect the oscillator performance. However, this drop in loop gain can be compensated by increasing the input voltage, and the oscillator can still be expected

to work from a 30 - 40 mV DC supply.

3.6   Summary

The Meissner Oscillator circuit was analyzed in open loop configuration to derive a loop gain expression for device optimization (refer to equation 3.10), which was then validated through comparisons with Cadence simulations. Special depletion-mode FETs were designed to have a higher likelihood of starting up at low voltages with integrated transformers. The specially fabricated FETs were then selected for optimum performance with off-chip as well as on-chip transformers, based on the loop gain expression.

The optimum FET for use with off-chip transformer was demonstrated on a PCB to start oscillating at as low as 2 mV with 500 mV_{p-p} amplitude in no load conditions. In contrast, state-of-the-art LTC3108 was found to start oscillating at 14 mV under the same testing conditions. Since the Meissner Oscillator in the PCB demo starts oscillating at a 7x lower voltage than the LTC3108 part, this design shows a higher likelihood of working with lossy on-chip transformers, which are in the process of being designed for fabrication.

Chapter 4

Switched Capacitor DC-DC Converter

As mentioned in Chapter 2, the SC DC-DC stage is cascaded with the Meissner Oscillator in order to provide the required boosting from 30 mV at the input to $>$ 1.2 V at the output. With two cascaded step-up conversion stages, the efficiency of the overall system can go down quickly. Since the HPA07 technology used for fluxgate transformers is a 1.5μm process, designing a switched capacitor circuit in this technology will result in lower efficiency. Therefore, a newer, more efficient technology called, LBC8LV, was used for the design of the SC DC-DC circuit. This means that the Meissner Oscillator and switched capacitor circuits will have to be on different chips, but the two chips can then be co-packaged to serve as a proof-of-concept for future integration. This chapter discusses the design and simulated performance of the SC DC-DC circuit, which is currently under fabrication.

4.1 Background

Switched capacitor circuits or charge pumps consist primarily of MOS transistors and capacitors, which can both be easily integrated on-chip. This makes charge pumps

a popular choice for step-up, DC-DC conversion circuits. Two of the most common voltage multiplication converters are discussed below.

4.1.1 Dickson Charge Pump

The Dickson charge pump [30] is a classical, well-known solution for on-chip voltage multiplication. It uses diode connected MOS transistors, along with capacitors pumped by two out-of-phase clocks, as shown in Figure 4-1.
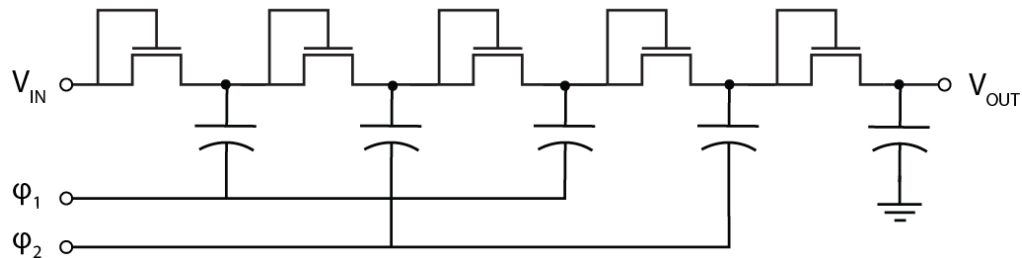
Figure 4-1: 4-stage Dickson charge pump

While this was one of the first few charge pumps, it is not the most efficient. Many other modifications of the Dickson pump have been proposed to improve its efficiency. The most prominent ones involve the use of static and dynamic charge transfer switches [31].

4.1.2 Cascade of Voltage Doublers

Cross-coupled voltage doublers (CCVDs) were introduced more recently than the Dickson charge pumps, but they are also one of the classic solutions in voltage boosting. The first CCVD was proposed in [32], and it used cross-coupled NMOS transistors. The circuit was modified to add PMOS transistors in [33] to get a higher efficiency voltage doubler. A simple implementation of the CCVD is shown in Figure 4-2.
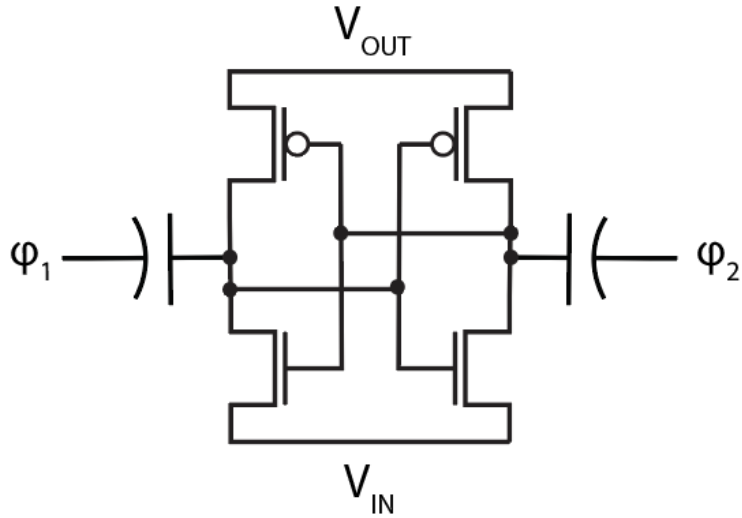
Figure 4-2: Cross-coupled voltage doubler

A cascade of CCVDs can be used as a charge pump to step-up the input voltage to much higher output voltages. This topology is sometimes referred to as the Pelliconi charge pump [34]. A 4-stage cascade of voltage doublers was found to be more efficient than a 4-stage Dickson charge pump by 13% in [35].

4.2   Design

The SC DC-DC circuit has a few, basic requirements, which guided the design of the chip. Since the switched capacitor converter will be powered by the rectified output of the Meissner Oscillator stage, it sets a design constraint on the supply voltage and the input power levels of the SC DC-DC circuit. The entire circuit should be able to operate from a supply voltage of 0.3 V on the lower end and also be able to sustain operation at higher voltages (> 1 V), when there is a large temperature differential applied to the TEG. The available power levels guide the decision on the size of pumping capacitors to be used, along with the clock frequency.

The other requirement is the conversion ratio. Assuming that the Meissner

Oscillator can provide around 0.3 - 0.4 V at the output under no-load condition from the lowest specified input voltage, the switched capacitor circuit will need to provide the remaining voltage boost to 1.2 V. Therefore, it needs to have a gain of 5, which dictates the number of stages needed in the charge pump.

Finally, as a start-up solution, the SC DC-DC system is meant to be used for powering the control circuitry of the boost converter until the output of the boost converter ramps up for self-sustaining operation. Therefore, it is desirable to keep the design of the SC DC-DC converter as simple as possible. These guidelines have been followed in the switched capacitor circuit design, which is further discussed in this section.

4.2.1 Architecture

A switched capacitor DC-DC circuit essentially consists of an N-stage charge pump to boost up the voltage, along with drivers for the charge pump, and an oscillator to generate a clock for the drivers. Some other components added to the design include a non-overlapping clock generator and a voltage detection circuit to indicate when the output voltage is higher than 1.2 V. In addition to these blocks, on-chip rectifiers were added to the chip in order to replace the discrete PCB components.

Two versions of the circuit were placed on the same chip: a basic version, and a secondary version, where the latter contains tuning parameters for the ring oscillator and voltage detector circuit, as well as a bypass mechanism to bypass the SC DC-DC stage altogether for higher efficiency if the input voltage is higher than 1.2 V. The overall architecture of the chip is shown in Figure 4-3.

4.2.2 Charge Pump

A cascade of voltage doublers was used as a charge pump for this design for its simplicity and efficiency. The gain of the cascaded CCVD charge pump is given as
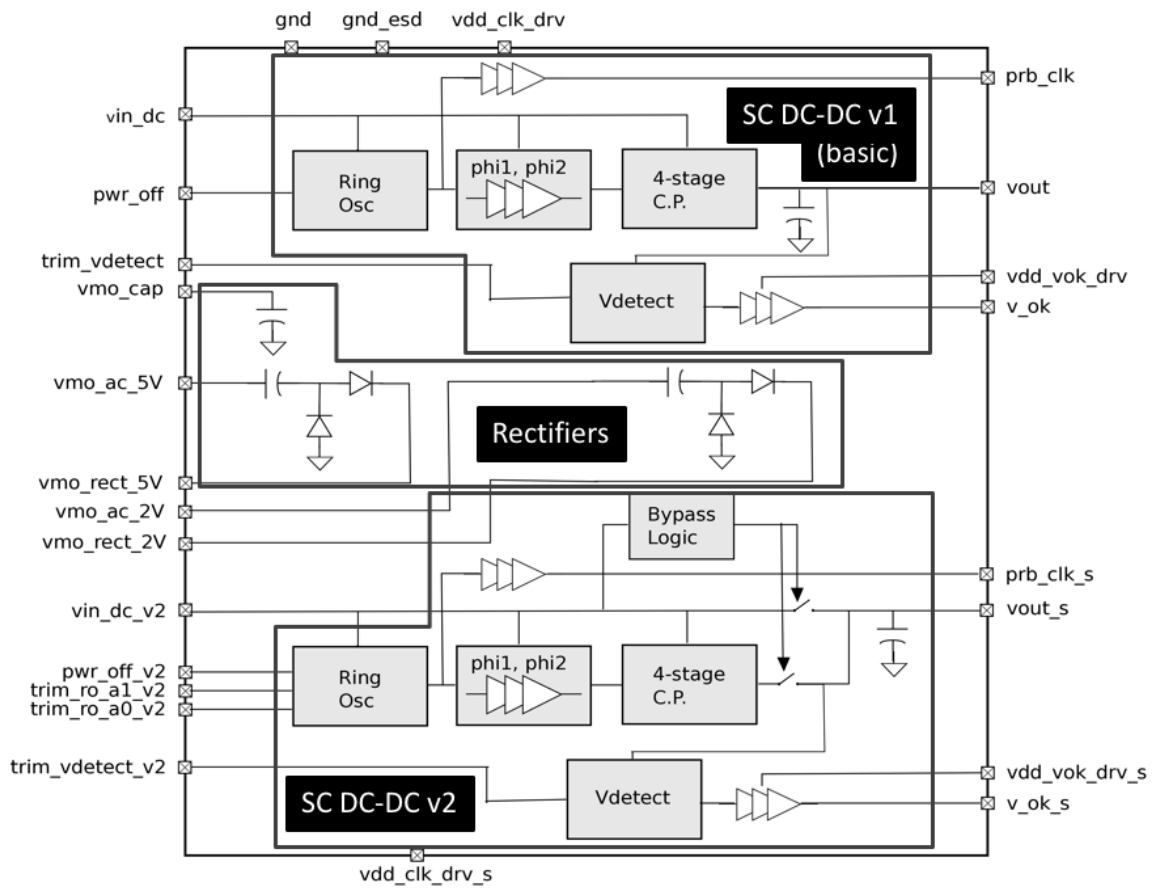
Figure 4-3: Switched capacitor DC-DC chip architecture

N+1 in ideal, no-load conditions, where N is the number of stages. Therefore, 4 stages were employed to get a gain of 5, as shown in Figure 4-4.

All capacitors were sized according to the expected power levels. If the charge pump takes too much power from the Meissner Oscillator, the output voltage of the oscillator will drop and the circuit will not function. Therefore, $50pF$ capacitors were used to limit the current and energy drawn in the low voltage case for the basic version, whereas $100pF$ were used in the second version with digitally tunable clock frequency. A $1nF$ output capacitor was used to store charge in order to power the subsequent stage.

The transistors used in the charge pump were all 1.8 V devices, which can sustain a maximum voltage of 2 V between any two terminals. If the input voltage to the charge pump is around 1 V or above, there is a risk of having a high voltage difference ($> 2V$) across some terminals of the transistors, which can damage the transistors. Such a situation can arise when the charge pump is just starting up, and the voltage at the output node of the first stage goes below zero because of reverse current flow in dead time, while the voltage pumped up by the capacitor is around $2V_{DD}$. In this situation, there can be a transient voltage > 2 V across the drain-source terminal of M2, which can damage the PMOS device.

In order to resolve the problem without adding complexity to the circuit, diodes were added from the main input to the output of each stage, as shown in Figure 4-4. This helps in protecting the devices from having a high potential difference across themselves, and also helps reduce the start-up time, by charging the outputs directly in the beginning. The diodes were designed using 5V NMOS transistors, and sized for the trade-off between reverse leakage current and forward ON current, so that the leakage current would not degrade the charge pump efficiency significantly.
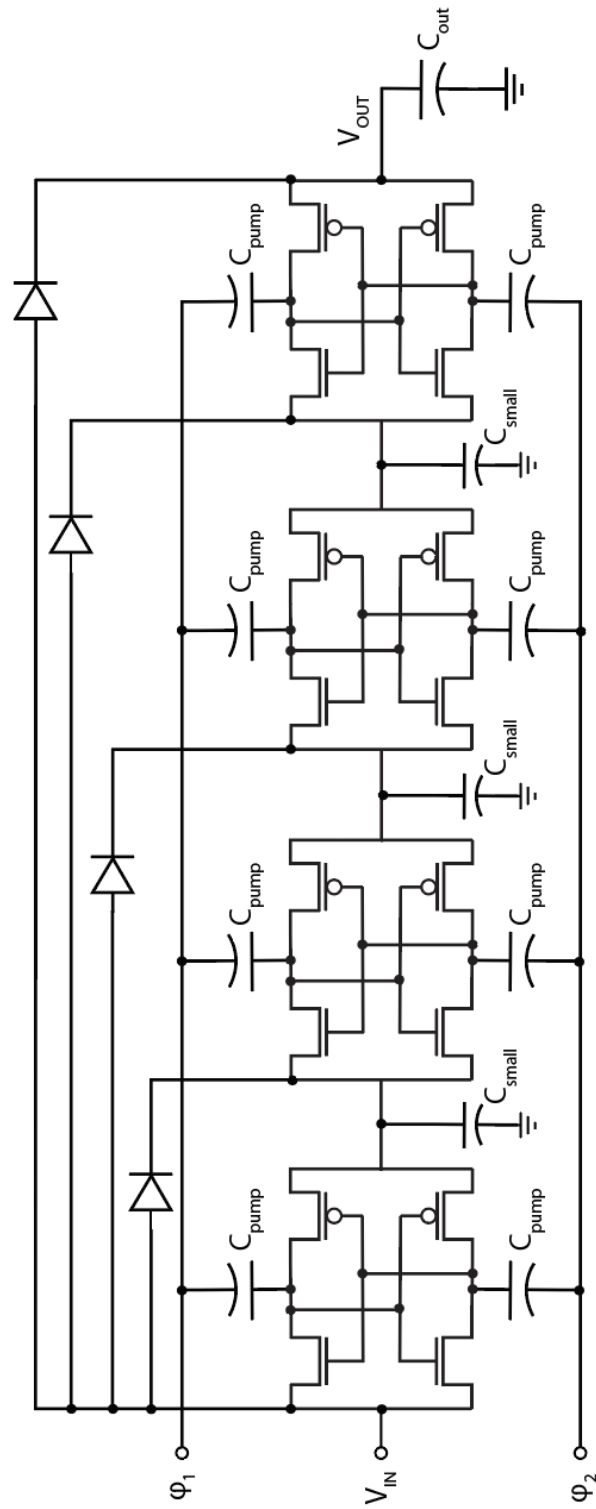
Figure 4-4: Charge Pump design with 4-stage cascade of voltage doublers
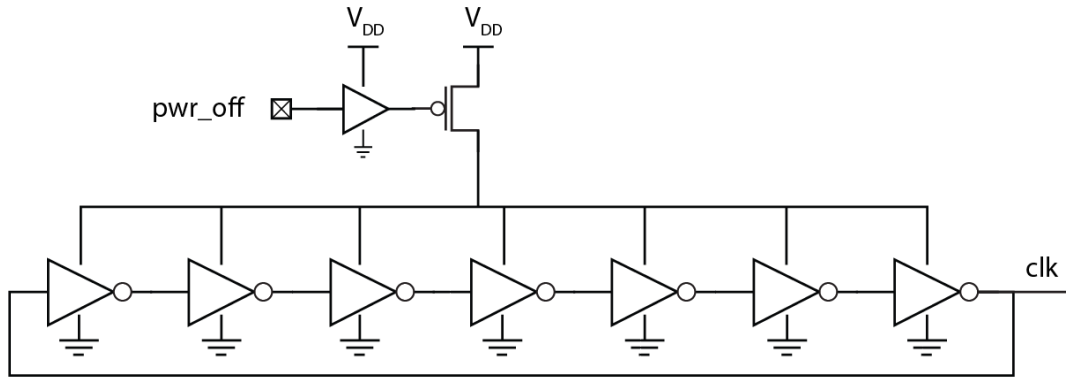
Figure 4-5: 7 - stage ring oscillator with power off control

4.2.3 Clock

The Meissner Oscillator frequency will typically lie in 100 kHz - 20 MHz range, depending on the exact circuit conditions. The clock frequency for the SC DC-DC circuit can be much lower, in the kHz range, and it needs to be selected to have a good trade-off between input power levels and pumping capacitor sizes. Having very low clock frequencies can lead to much slower start-up times and lower efficiency, while having very high frequencies can make the charger extract more power from the Meissner Oscillator than needed for sustainable operation.

For on-chip clock generation, ring oscillators offer very low power consumption and fast start-up times while requiring minimal area. These three features make the ring oscillators an excellent choice for the application in question. A simple 7-stage ring oscillator was used to generate a clock for the charge pump, as shown in Figure 4-5, with identical inverters in each stage, and a switch to power off the circuit. A ring oscillator with 2 digital control bits was used in the secondary version to provide four frequency settings.

Ring oscillators have a disadvantage of being very sensitive to process, voltage, and temperature (PVT) variations. The significance of such variations is discussed below in context of the switched capacitor start-up circuit.

Frequency variation with supply voltage

For a simple ring oscillator without any additional control, the clock frequency varies extensively with supply voltage. While this can be a problem for many other applications, it does not pose a major concern here. At lower supply voltages, the ring oscillator should consume less power and provide lower clock frequency so that the switched capacitor circuit overall consumes only as much power as can be provided by the Meissner Oscillator. Having a voltage dependent frequency can allow the SC DC-DC power to be scaled accordingly with the power levels available from the Meissner Oscillator output.

Process and temperature variation

Unlike voltage variation, process and temperature variation of the clock frequency are quite undesirable for operation of the SC DC-DC circuit. In order to improve the process and temperature variation of the ring oscillators, techniques like current starving and voltage regulation are often employed. However, they require the use of control voltages or bias circuits, which themselves come with a high start-up time penalty and added circuit complexity in order to operate at low power levels. The clock frequency in this application does not need to be very precise for robust circuit operation. Therefore, it is not justifiable to compromise start-up times for less frequency variation.

Inverter Stage

In the given technology, the threshold voltage variation with length and width was found to be quite significant, and increasing the length of the transistor was found to decrease its threshold voltage. Therefore, multiple transistors of the same size were stacked in series or parallel to get a higher length or width.

An inverter stage with tuning, used in the secondary version, is shown in Figure

4-6. Two digital control bits are used in this version to provide four frequency settings, as listed in Table 4.1 for the nominal corner at $V_{DD} = 0.3V$.

Table 4.1: Ring oscillator frequency settings

Bits BA	Frequency (kHz)
00	4
01	6
10	8
11	10

Extracted Simulation Results

The ring oscillator layout was RC extracted and simulated for performance evaluation. The clock frequencies generated by the ring oscillator at an ideal supply voltage of 0.3 V are tabulated over process and temperature corners in Table 4.2. The frequency variation spans two decades, from the weak corner at $-20\,^{\circ}$C to the strong corner at $100\,^{\circ}$C. Accordingly, the power consumed by the ring oscillator varies from 20 pW to 35 nW. The duty cycle of the clock over all process and temperature corners was simulated to be 50% +/- 4.5% at $V_{DD} = 0.3V$.

Table 4.2: Ring oscillator frequency over corners at $V_{DD} = 0.3V$

Process	Frequency		
	$-20\,^{\circ}$C	$27\,^{\circ}$C	$100\,^{\circ}$C
Nominal	3.1 kHz	6.1 kHz	9.8 kHz
Strong	12.4 kHz	16.4 kHz	19.7 kHz
Weak	142 Hz	775 Hz	2.7 kHz
PNSkew	457 Hz	1.67 kHz	4.9 kHz
NPSkew	2.0 kHz	3.9 kHz	6.9 kHz

The SC DC-DC circuit is designed to deal with a large frequency range, so it comfortably handles the ring oscillator frequency variation and operates well over all corners, as shown in Section 4.3.
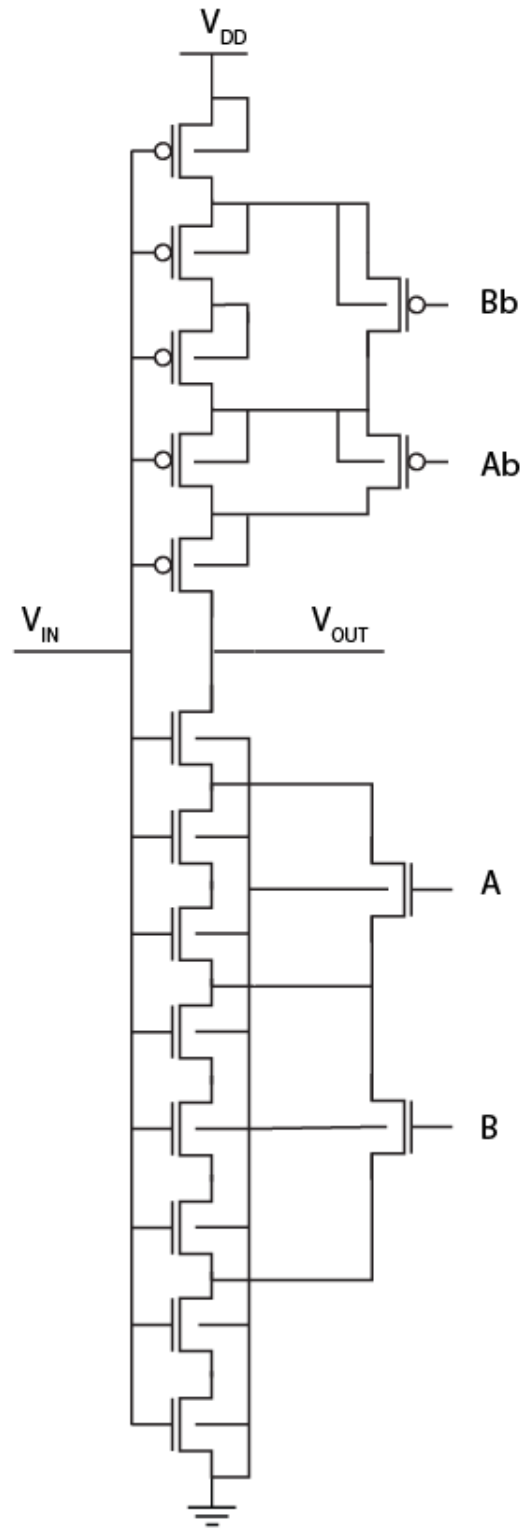
Figure 4-6: Ring oscillator inverter stage with 4 frequency settings

4.2.4 Other Auxiliary Circuits

Non-overlapping Clock Generators

In order to avoid short circuit path from the output voltage to the input supply voltage in a charge pump, it is essential to have non-overlapping clocks with a small dead time between them. In order to generate these non-overlapping clocks from the ring oscillator output clock, two NOR gates were used, as shown in Figure 4-7.
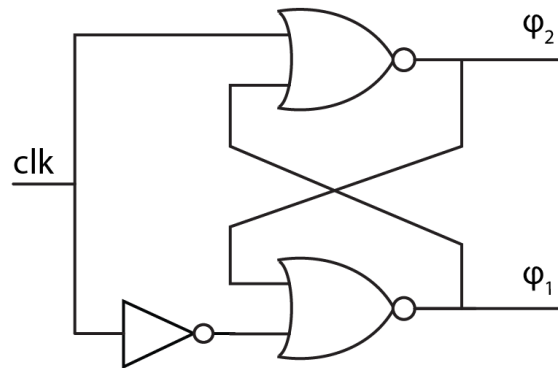
Figure 4-7: Non-overlapping clock generator

Voltage Detection Circuit

The voltage detection circuit is needed to detect when the output voltage has crossed 1.2 V, so as to send an output signal (v_ok) to the subsequent stage, signaling that the output voltage is ready for use. This circuit should have a low start up time in order to detect the voltage early in the fast corners. It should also have a hysteresis window of 0.1-0.2 V so that the circuit does not get stuck in a loop when the detection circuit is operating at the tripping point.

For the voltage detection circuit, the topology proposed in [36] was used, as it does not need any comparators, bias circuits, or additional circuitry to work. The transistors were selected and sized appropriately to detect a voltage of around 1.2 V. The sizing of transistors was also based on the trade off between power, speed, and

the hysteresis window. A single control bit for tuning was added to the circuit in the second version to curb the power levels in the slow corners, while providing higher speeds in the nominal and fast corners.

The inverters were designed with 5V devices, where the first staged was designed to have a strong PMOS and weak NMOS, while the second stage was designed to have a strong NMOS and a weak PMOS, to reduce the risk of false positives on v_ok signal, when the output voltage is just starting to ramp up initially. Under nominal conditions, the circuit consumes pW's of power when the supply voltage is less than the trigger voltage, and it draws < 0.6 pA of current once the supply voltage exceeds the trigger point, and v_ok signal goes high.
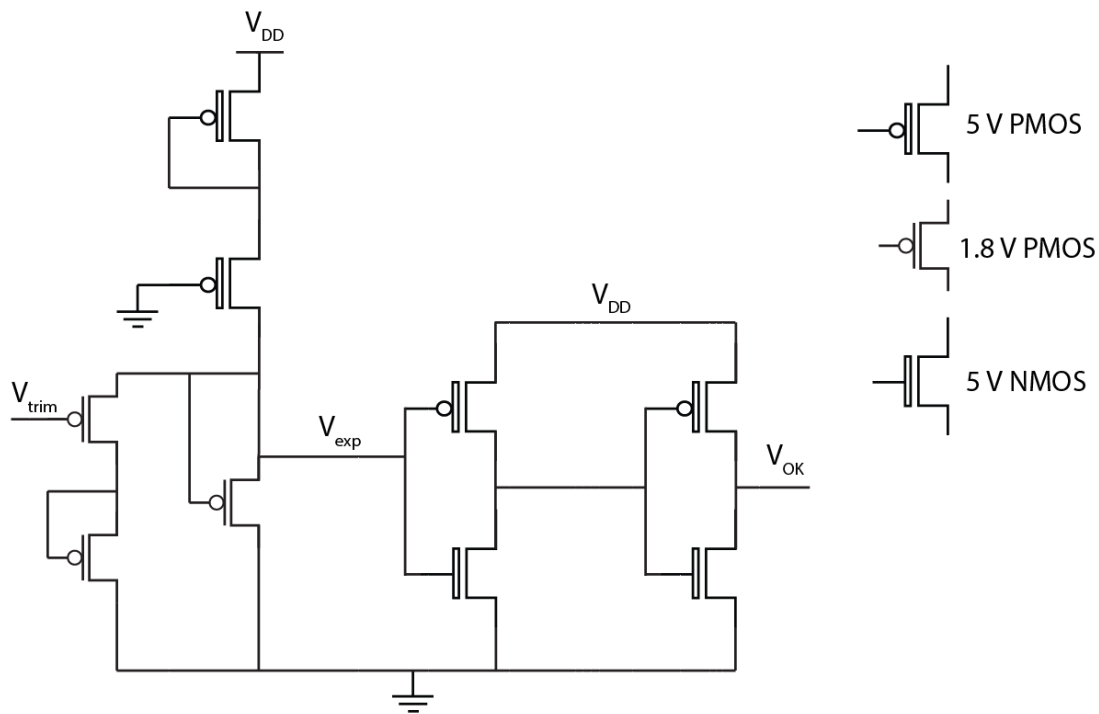
Figure 4-8: Voltage detection circuit with trimming ability

Additional drivers were used to drive the v_ok signal to the output pads. Since these drivers are only required for testing purposes, they were powered through an external ideal DC voltage source of 1.2 V during simulation.

Rectifiers

A voltage-doubler rectifier circuit using diodes and capacitors, as shown in Figure 3-2, was added to the chip to rectify the AC signal generated by the Meissner Oscillator. This provides an alternative to the discrete PCB components, which is essential for an integrated solution when being used with on-chip magnetics.

The flavors of p-n junction diodes included in the technology kit displayed high ON voltages, and therefore low currents over the voltage range of interest. So, the rectifier diodes were custom designed with MOS transistors. Two versions of the rectifier were added on chip for testing purposes, using the transistors in Table 4.3.

Table 4.3: Comparison of rectifier diodes

Device flavor	V_T	V_{max}	Use case	Comments
1.8 V PMOS	Low	Low	with on-chip transformers	-
5 V native NMOS	High	High	with off-chip transformers	need DNWs

The rectifier circuit with NMOS transistors placed in deep n-wells (DNWs) is shown in Figure 4-9. The storage capacitor is not connected directly to the rectifier, so that the two versions of the rectifier can share a single storage capacitor one at a time, and therefore allow area savings.
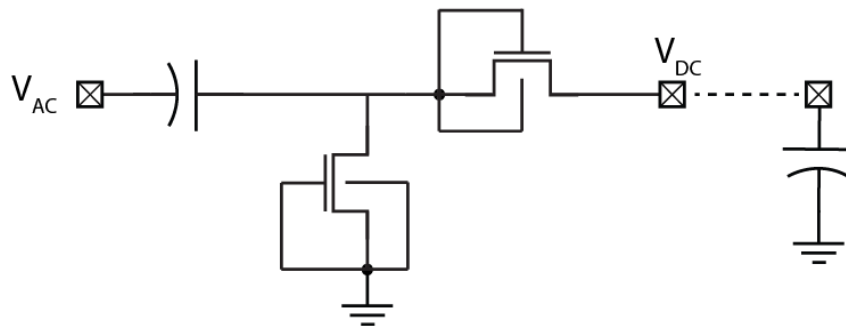
Figure 4-9: On-chip 5V rectifier

4.2.5 Layout

The layout of the SC DC-DC chip is shown in Figure 4-10. The total area of the chip is 3mm x 3mm, which contains two versions of the SC DC-DC circuit. The area of the basic SC DC-DC version for use with on-chip transformers, along with the rectifiers, is $\simeq 5mm^2$. If the fabricated FET and the transformer are both to placed on the same chip, the total area will be dominated by the SC DC-DC circuit, and it will be $\simeq 5mm^2$, much smaller than the off-chip transformers.
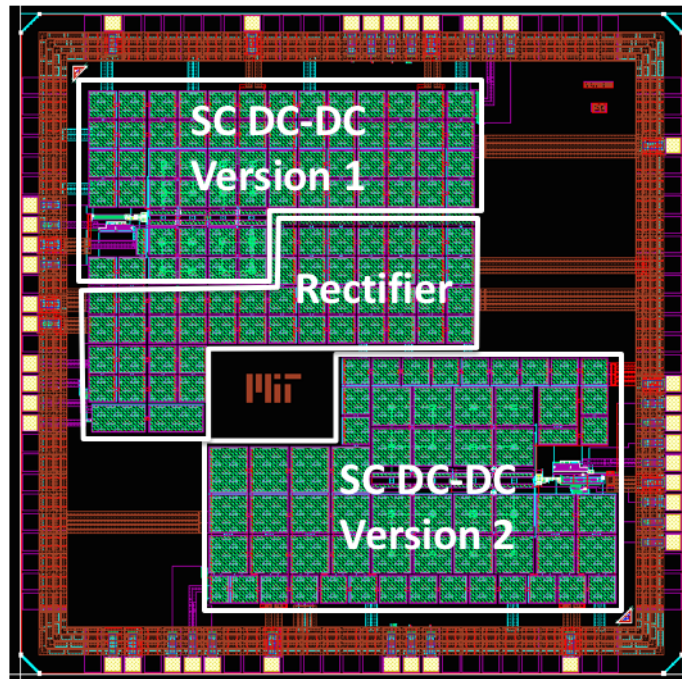
Figure 4-10: Layout of the switched capacitor DC-DC chip

High density caps were used for the rectifier as well as the charge pump capacitors in the two versions. The total area of the chip is dominated by the capacitors, as there is > 3 nF of capacitance on the chip altogether.

4.3 Simulations Results

To evaluate the switched capacitor circuit performance, the top level layout cell was RC extracted and simulated. Some of the post-extraction simulation results are presented in this section.

4.3.1 Testbench Set Up

For transient simulation testbench set-up, the ideal choice for the input signal is to use the Meissner Oscillator as a source to the SC DC-DC chip. However, the LBC8LV PDK is not compatible with the MOS models that were used for the Meissner Oscillator simulation, and therefore the two could not be simulated together (accurately) in either environment. In the absence of a good simulation model for the source circuit of SC DC-DC chip, one alternative is to feed ideal AC waveforms to the SC DC-DC rectifier circuit. Another similar alternative is to feed measured waveforms from the PCB demo as the source. Both alternatives were employed for the transient simulations.

The results presented in the following sections are for the basic SC DC-DC version with 2V rectifier. In the test set up, the output capacitor was loaded with a 1nA current source throughout the simulation to make sure that the output ramps up even with some leakage currents. A voltage controlled current source was also added to the output which starts drawing 24 nA of current once the output voltage ramps up and the v_ok signal goes high. Together, there is a load current of 25 nA at the output after the output voltage becomes ready for use.

4.3.2 Start-Up Times

For start-up time simulation presented in Figure 4-11, measured Meissner Oscillator output AC waveforms from an input voltage of 4 mV under no-load conditions were provided as a source to the SC DC-DC chip. The transient results over 5 process
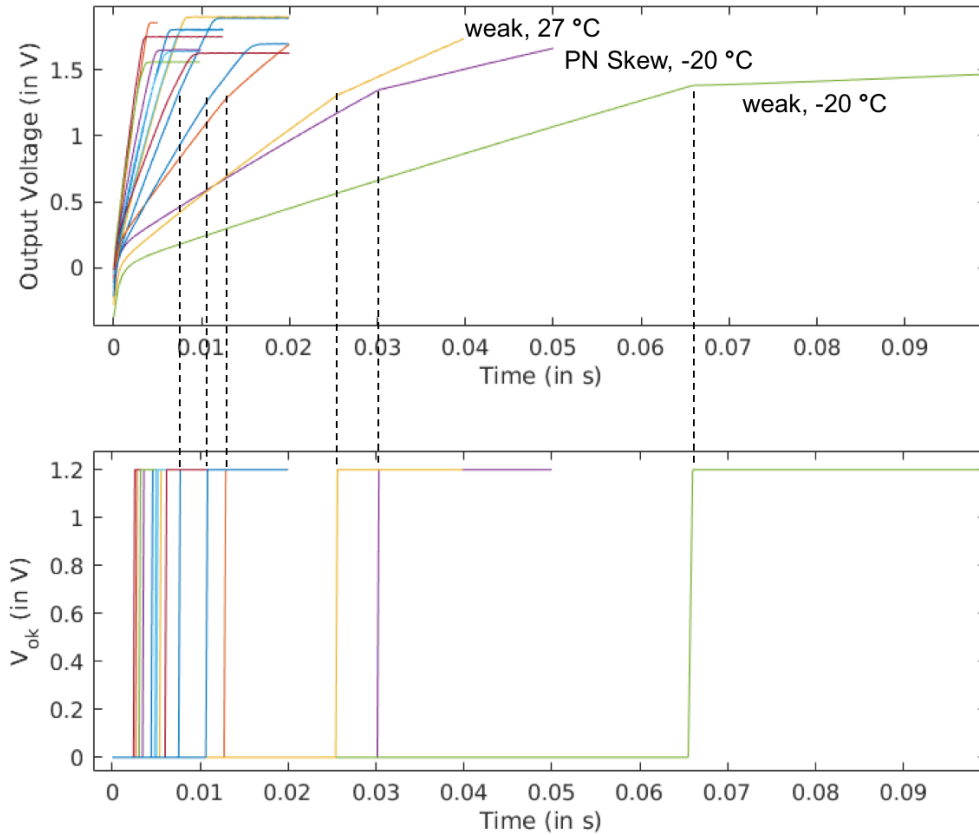
Figure 4-11: Start-up behavior of the SC DC-DC circuit over corners

corners: Nom, Strong, Weak, NPSkew, and PNSkew, and 3 temperature corners: $-20\,°C$, $27\,°C$ and $100\,°C$, are plotted. The output voltage over all corners ramps up to around 1.2 V, following which the voltage detection circuit gives an OK signal and the load circuit starts drawing power from the output. As expected, the slowest rise time is observed in the weak corner at $-20\,°C$, while the fastest rise time is occurs in the strong corner at $100\,°C$. The start up times increase with decreasing clock frequencies (provided in Table 4.2).

It should be noted that these transient simulations do not predict the behavior of the full system at an input voltage of 4 mV when connected together for testing, as the amplitude of the measured waveforms, provided as source, does not reduce
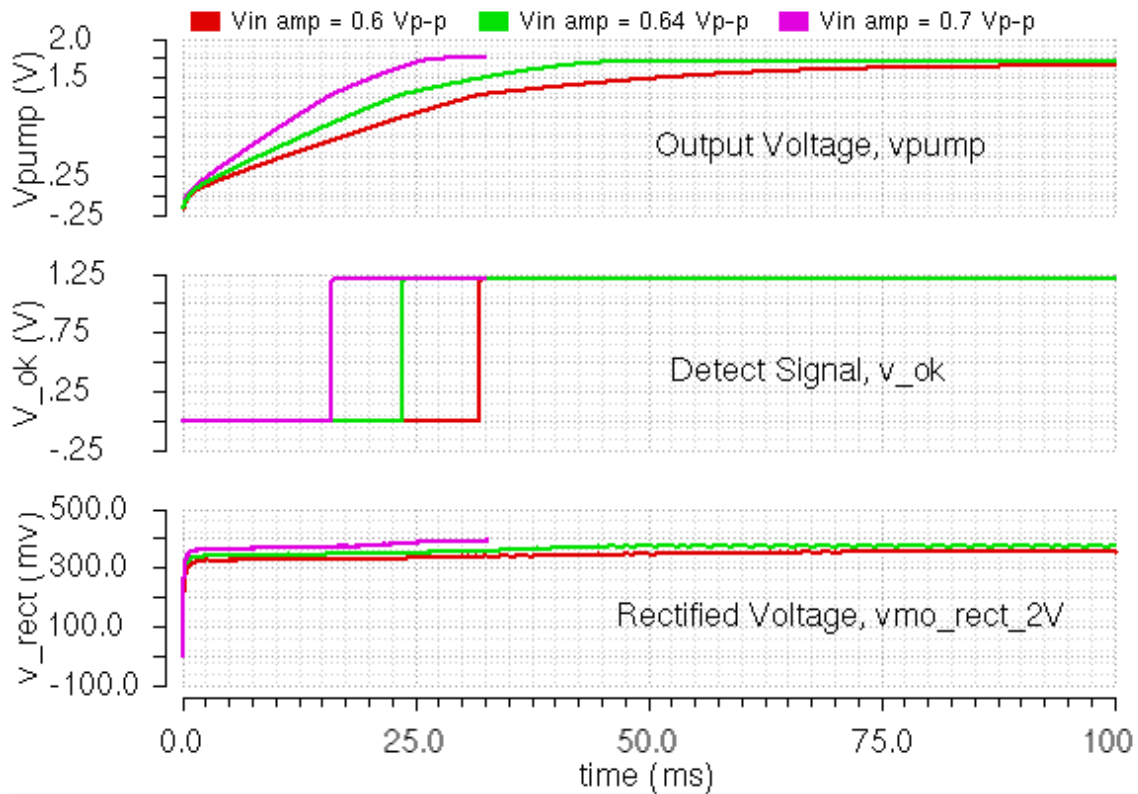
Figure 4-12: Start-up behavior of the SC DC-DC circuit for different input amplitudes

when loaded by the SC DC-DC circuit, unlike in the real situation. Therefore, actual testing of the full system on a PCB board is necessary for a better idea of the actual system performance. In the mean time, the circuit was simulated at lower amplitudes of the AC waveforms for good measure.

Figure 4-12 shows the start-up behavior of the system for an ideal sinusoidal voltage source of 600 mV_{p-p}, 640 mV_{p-p}, and 700 mV_{p-p} at 75 kHz frequency in the nominal corner. The circuit is able to operate well even at a peak-to-peak amplitude of 0.6 V, with a rise time of less than 40 ms. Based on these results, the system can be expected to work from 4 mV DC supply when put together with the PCB demo with the off-chip transformer.
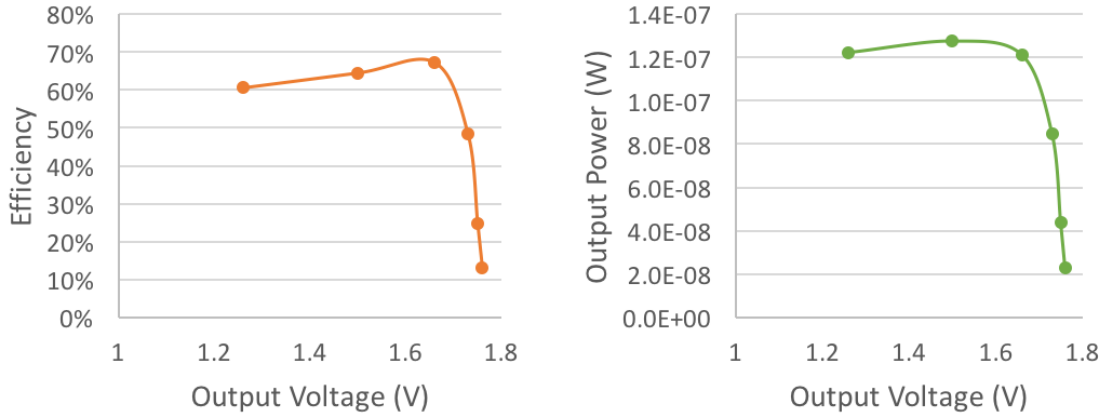
Figure 4-13: Efficiency and output power levels for the SC DC-DC circuit

4.3.3 Efficiency

To simulate the efficiency of the charge pump circuit, an ideal sinusoidal input voltage with amplitude 0.35 V and frequency 75 kHz was provided to the 2V rectifier pins of the chip. Then, the input power of the charge pump and the final output voltage V_{pump}, were measured at different loading conditions. The resulting efficiency plot and output power levels in the nominal corner are shown in Figure 4-13.

With the given signal of 350 mV amplitude, the rectified output settles to 375 mV - 390 mV. The peak efficiency seen in this case is 67%, while the maximum output power is 128 nW. These power levels are good enough for working with the PCB demo using off-chip transformers from a 4mV DC supply.

4.4 Summary

A 4-stage cascade of CCVDs was used as a charge pump to step-up the voltage from 0.3 V at the input to > 1.2 V at the output. The charge pump includes a voltage detection circuit to indicate when the output voltage is available for use. It also contains on-chip rectifiers to replace the discrete components on PCB. The clock for the charge pump is designed with a 7-stage ring oscillator, which takes a default-LOW

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power signal to turn off the charge pump once the output voltage of the (optional) following boost converter stage has ramped up.

The charge pump circuit along with the rectifiers consumes $5\ mm^2$ of area. The total area consumed by the start-up system, including the Meissner Oscillator, is expected to be dominated by the SC DC-DC chip, and have the same area of $5\ mm^2$. This area is dominated by the capacitors, and it can be reduced in future designs for specific applications.

From simulation results, the SC DC-DC circuit can be expected to work together with the Meissner Oscillator and provide > 1.2 V at the output, from an input voltage of 4 mV at the input. The maximum output power to be expected at such a low input voltage is around 100 nW.

Chapter 5

Conclusions and Future Work

This research work has demonstrated significant progress in its aim of achieving a completely integrated system with low voltage start up for thermal energy harvesting applications. It has the potential of making a powerful impact on the use of energy harvesting for WSNs, wearable electronics, and bio-implantable devices, by enabling form factor reduction by manifolds compared to the existing solutions today.

This section summarizes the important conclusions of the thesis, and discusses the future work to be done in this research work. It also suggests directions to explore for making further improvements to the system.

5.1 Thesis Summary

5.1.1 Summary of Accomplishments

The key accomplishments of this research work, to date, are listed below:

1. Derivation of a loop gain expression, which was crucial to the design and optimization of on-chip devices. The expression was validated for accuracy with

Cadence simulations, and it is reproduced below for convenience:

$$g_m \left(\frac{R_s C_t (g_{ds} R_p + 1)}{k \sqrt{L_p L_s}} + g_{ds} k \sqrt{\frac{L_p}{L_s}} \right)^{-1} > 1$$

2. Design, fabrication, and testing of optimum FETs in a Meissner Oscillator to demonstrate oscillations from a voltage less than $\frac{1}{4}$th that of the state-of-the-art, using the same off-chip transformer

3. Exposing parameters that need to be optimized in on-chip transformers for use with the fabricated FETs, and designing an optimum transformer

4. Exploring paths for improving the transformer design through

   (a) interleaving to improve the coupling factor

   (b) using toroidal structure to save area

5. Designing a switched capacitor DC-DC circuit to form a full start-up system for energy harvesting

5.1.2 Comparison with the State-of-the-Art

The comparison of the research work performance with the state-of-the-at is premature at this time, since the full system has not been tested yet. However, a comparison based on a mix of measured, simulated, and expected performance is shown in Table 5.1.2.

5.2 Future Work

This section lists out the work to be completed in the near future, and provides some other directions that can be followed in the long term.

Table 5.1: Comparison with the state-of-the-art

	Energy Source	Topology	Min. Cold Start Voltage	Transformer Area
LTC3108 2010 [8]	thermal	MO	20 mV *	36 mm^2 (off-chip)
JSSC 2011 [22]	thermal	boost converter	35 mV (mech. kick-start)	N/A
ISSCC 2012 [37]	thermal, solar	boost	330 mV	N/A
ISLPED 2014 [9]	thermal	MO+boost converter	40 mV *	36 mm^2 (off-chip)
JSSC 2015 [7]	thermal, solar	boost converter	220 mV	N/A
IEEE Trans. 2015 [17]	thermal	MO	228 mV 104 mV	24 mm^2 28 mm^2
This Work	thermal	MO+switched capacitor CP	4 mV *	36 mm^2 (off-chip)
This Work w/ fluxgate	thermal	MO+switched capacitor CP	<50 mV **	1 mm^2

* with 1:100 turns ratio transformer
** expected, not measured results

5.2.1 Immediate Tasks

Listed below are some of the immediate tasks that need to be completed in the next three months as a part of this project:

- Assemble and test the fabricated SC DC-DC chip with an off-chip transformer

- Layout the optimized transformer design and send for fabrication

- Assemble and test the on-chip transformer

- Test the entire system on board level, with the integrated transformers, optimized fabricated transistors and the SC DC-DC circuit, along with a TEG input

This demo on a PCB can serve as a proof of concept for a completely integrated start-up solution. Other packaging/testing options, arranged in order of increasing time and cost, are
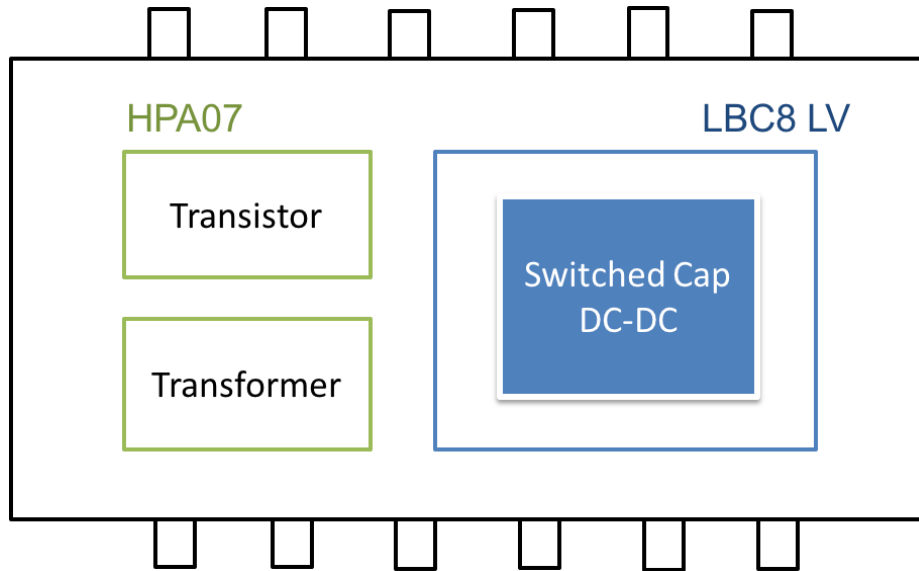
Figure 5-1: Co-packaging option for proof-of-concept of a fully integrated solution

- Co-packaging the transistor, transformer and SC DC-DC chip in a single package, as shown in Figure 5-1

- Fabricating the transformer and transistor together on the same chip in HPA07 technology

- Adding the fluxgate metal on top of LBC8 LV to have both the Meissner Oscillator and the SC DC-DC circuit on the same die

5.2.2   Ideas to Improve Performance

Explore transistors from other technologies

For use in a Meissner Oscillator, the best suited transistor as per equation 3.10 is the one with the highest $\frac{g_m}{g_{ds}}$ and/or $\frac{g_m}{C_g}$ compared at similar drain currents, and for $V_{gs} = V_{ds} =$ tens of mVs. In the future, when fluxgate metal is ready to be placed on top of newer technologies, it would open up an entire selection of transistors to be considered for use in the oscillator. It would then be possible to compare the

transistors in mature technologies based on the aforesaid features, and find the most suitable NMOS device for better oscillator performance.

Increase the height of magnetic core

The height of the magnetic core in TI's fluxgate transformers is fixed for time and cost effectiveness. However, increasing the core height can offer dramatic increases in the transformer performance. Doubling the core height can double L_p and L_s without affecting R_s and C_s. This would increase the loop gain of the Meissner Oscillator and allow the system to cold start at even lower voltages.

Explore the use of other integrated magnetics technologies

With future technological advancements, it can be possible to use better core and winding materials for the magnetics in order to have transformers with higher quality factors. This, again, results in a higher loop gain and therefore better circuit performance.

5.2.3 Other Directions

Some of the other work that was not covered in this project, but can be pursued in the future, includes the following:

- Create more accurate MOS models for the specially fabricated transistors, along with variation models

- Test the full system with an off-the-shelf boost converter chip at the output

- Custom design a boost converter for use in regular operation with this cold start system to get a higher conversion efficiency

- Further explore the idea of using integrated magnetics for the boost converter

- Investigate the use of bio-potentials for energy harvesting to use the system for bio applications, where integration is a necessity

Appendix A

Acronyms and Abbreviations

CCVD   Cross-Coupled Voltage Doublers

CP   Charge Pump

DNW   Deep N-Well

FET   Field Effect Transistor

MO   Meissner Oscillator

MOS   Metal Oxide Semiconductor

PCB   Printed Circuit Board

PDK   Product Development Kit

QFN   Quad Flat No-Leads Package

SC   Switched Capacitor

TEG   Thermoelectric generator

TI   Texas Instruments

WSN   Wireless Sensor Networks

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