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Dielectric Coating Thermal Stabilization During GaAs-Based Laser Fabrication for Improved Device Yield

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The quality and yield of GaAs-based ridge waveguide devices fabricated at MIT Lincoln Laboratory were negatively impacted by the random lot-to-lot appearance of blisters in the front-side contact metal. The blisters signaled compromised adhesion between the front-side contact metal, underlying SiO_2 dielectric coating, and semiconductor surface. A thermal-anneal procedure developed for the fabrication of GaAs slab coupled optical waveguide (SCOW) ridge waveguide devices stabilizes the SiO_2 dielectric coating by means of outgassing and stress reduction. This process eliminates a primary source of adhesion loss, as well as blister generation, and thereby significantly improves device yield. Stoney's equation was used to analyze stress-induced bow in device wafers fabricated using this stabilization procedure. This analysis suggests that changes in wafer bow contribute to the incidence of metal blisters in SCOW devices.

Key words: PECVD, GaAs, film stress, metal blister, blister, adhesion

INTRODUCTION

GaAs ridge waveguide laser devices have been fabricated for many applications including wavelength- and coherent-beam-combined laser systems, high-power mode-locked lasers, high-power directly modulated lasers for optical communication, and development of surface-emitting devices.[1–5] The most recently fabricated devices have been slab-coupled optical waveguide (SCOW) lasers and amplifiers. The SCOW device is fabricated with an epitaxially grown, multiple-quantum-well active region, which emits a large, nearly circular, near-diffraction-limited beam.[6] A cross-section scanning electron micrograph of a typical SCOW device is shown in Fig. 1.

The fabrication of GaAs ridge waveguide devices requires the deposition of a SiO_2 dielectric coating as an insulating layer between the GaAs semiconductor surface and the front-side contact metallization. The initial fabrication of GaAs SCOW devices was plagued by the appearance of random lot-to-lot front-side contact metal disruptions in the form of blisters. Microscopic examination revealed that these blisters were due to adhesion failures between the front-side contact metal, underlying SiO_2 dielectric coating, and semiconductor surface. The presence of blisters generated concerns about the quality of metal–semiconductor electrical contact resistance, and ultimately device performance and reliability. For these initial fabrications, the full wafer rejection rate was >50% primarily due to the presence of front-side blisters. These front-side contact metal blisters typically appeared after the final fabrication step, a 450°C anneal performed to alloy the back-side contact metal. We hypothesize that changes in the low-temperature (<300°C) plasma-enhanced chemical vapor deposition (LT-PECVD) SiO_2 dielectric coating during this anneal stimulated the formation of front-side contact metal blisters.

GaAs device structures are typically grown by molecular beam epitaxy (MBE) or organometallic vapor-phase epitaxy (OMVPE) at temperatures between 500°C and 700°C. Low-temperature SiO_2 dielectric coatings are utilized in the fabrication of

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GaAs devices to minimize performance degradation due to thermal-processing-induced changes in the epitaxial layer structure.[7,8] These LT-PECVD SiO_2 dielectric coatings are known to incorporate hydrogen and nitrogen as $SiO_xH_yN_z$, and will outgas and densify if exposed to temperatures above the deposition temperature.[9–12] Measurement of refractive index and buffered hydrofluoric acid (BHF) etch rate are useful indicators of the LT-PECVD dielectric coating composition and stoichiometry, which can be influenced by deposition process parameters such as deposition temperature, radio frequency (RF) power, process gas composition, total flow, gas ratio, and system configuration.[11,13,14]

A series of experiments were performed to examine the impact of thermal annealing on the LT-PECVD SiO_2 coating. This study demonstrated the need to thermally stabilize the SiO_2 coating by outgassing in conjunction with film stress reduction. Postdeposition annealing of LT-PECVD coatings has previously been reported for stress relaxation, device electrical performance improvement, and high-yield wafer bonding.[9,14–16] Thermal stabilization and forced outgassing of LT-PECVD SiO_2 have been employed to reduce contact-metal blister formation in the fabrication of SiO_2/Pt/lead zirconate titanate (PZT)/Pt capacitors.[10] The impact of SiO_2 film stress and thermal-cycling-induced wafer bow changes was examined to understand the effect of wafer bowing on blister formation. Based on the results of process observations and experiments, a dielectric-coating thermal-anneal procedure was developed, contributing to greatly improved metal–dielectric–semiconductor adhesion and device yield.

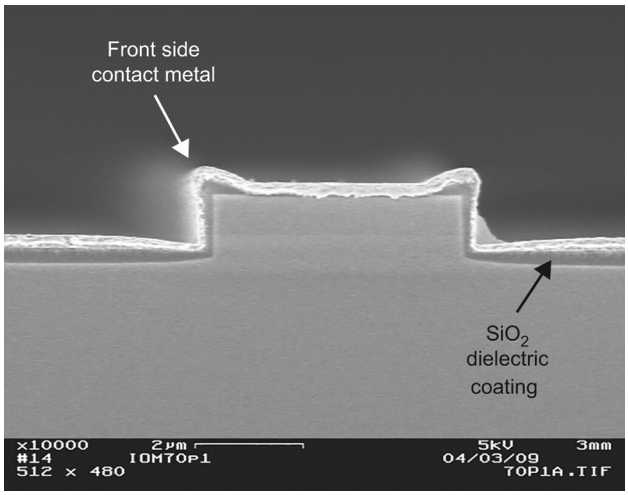

Fig. 1. SCOW device cross-section. Front-side contact metal and SiO_2 dielectric coating layers are labeled.

EXPERIMENTAL PROCEDURES

The GaAs SCOW device processing sequence has been described in detail previously and is represented in Fig. 2.[17,18] A two-layer etch mask, composed of an upper layer of Al_2O_3 and a lower layer of LT-PECVD SiO_2, was utilized in an inductively coupled plasma reactive ion etching (ICP-RIE) system to dry-etch ridge stripes. The etch mask was removed, and a dielectric coating consisting of a 300-nm layer of LT-PECVD SiO_2 was deposited at 200°C in a Samco PD200-STP deposition system on the sample front side to insulate the exposed ridge sidewalls. This tool utilizes tetraethylorthosilicate (TEOS) in nitrogen carrier gas, mixed with oxygen to deposit a low-stress dielectric coating. A photolithographic process was employed to open ridge-top vias. The dielectric coating was dry-etched with CF_4 in a parallel-plate reactive-ion etching (RIE)

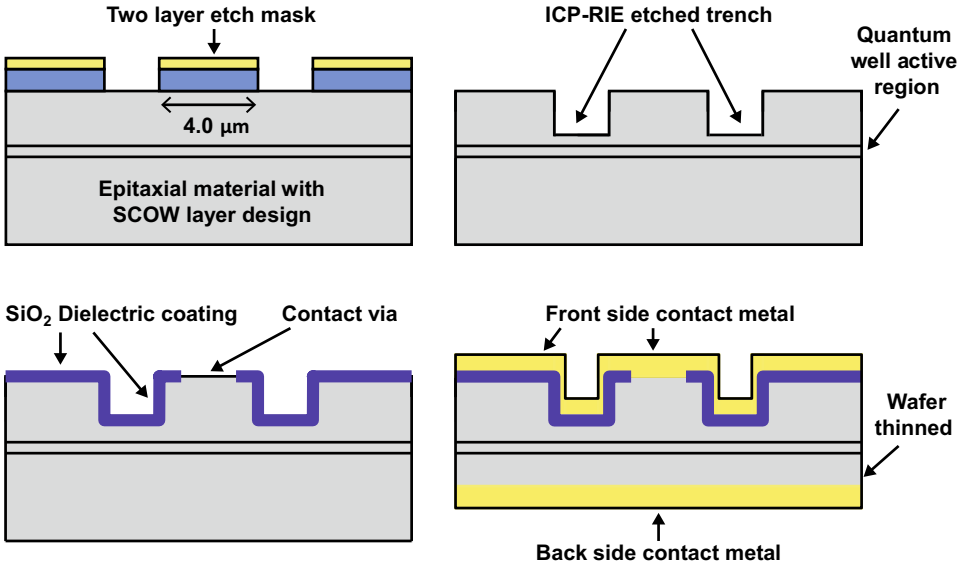

Fig. 2. Schematic representation of SCOW fabrication sequence.

system followed by sputter deposition of a Ti/Au/Pt/Au front-side contact metal layer. The sample was then thinned by mechanical lapping and polishing of the back side, and an *n*-GaAs contact metal stack consisting of electron-beam-evaporated Ge/Au/Ni/Au and sputtered Ti/Pt/Au packaging metal layers were deposited. The final fabrication step was a rapid thermal anneal (RTA) at 450°C for 45 s to alloy the *n*-GaAs contact metal.

To identify the source of the front-side blistering, three SCOW device wafer test samples were processed with annealing steps added to two of the three samples. Since the primary trigger of the blistering had been observed to be the back-side contact metal alloy anneal step, additional 450°C, 45 s anneals were added to the fabrication sequence to see if these would trigger visible front-side changes. Key processing steps for the three samples are detailed in Table I. Sample A was annealed immediately after the SiO_2 dielectric coating deposition, sample B was annealed immediately after the front-side contact metallization was completed, and sample C was a control that followed the standard fabrication sequence. These samples were examined by standard and Nomarski microscopy at each step of the fabrication sequence.

To investigate changes in the composition of LT-PECVD SiO_2 dielectric coatings due to thermal annealing, refractive index and BHF etch rate were measured as a function of anneal temperature. Test wafers were prepared by coating 300-μm-thick silicon wafers with two dissimilar dielectric coatings, a LT-PECVD SiO_2 coating deposited at 200°C and thermal SiO_2 grown by steam exposure at 1000°C to be used as a temperature-stable control. These wafers were annealed in a RTA system, over a temperature range of 200°C to 1000°C, at 100°C intervals, for 300 s. The samples were measured by ellipsometry to document film refractive index; they were then masked with photoresist and etched for 30 s in BHF before measuring the etched step using a stylus profilometer to calculate the BHF etch rate.

Thermal stress-bow experiments were performed using a Toho FLX-2320s in stress–temperature measurement mode to evaluate the LT-PECVD SiO_2-coated silicon test wafers. In this measurement mode, the temperature is ramped up to 490°C and back to room temperature to obtain coating stress as a function of wafer temperature. Measured stress values were then utilized to estimate changes in SCOW device wafer bow caused by thermal cycling.

RESULTS AND DISCUSSION

SCOW Device Tests

There were no notable front-side changes or unexpected observations through the LT-PECVD SiO_2 dielectric coating deposition step. Sample A was annealed following the dielectric coating deposition step, and no change was observed. All samples were then processed through the front-side contact metal deposition step, with no observable change in appearance. Sample B was annealed, and microscopic examination revealed a small number of disruptions and blisters (0.5 blisters/cm^2) in the front-side contact metal. The samples were then processed through the back-side thinning and contact metallization steps. There were no notable changes for all three samples before the final RTA processing step. All samples were then annealed at 450°C for 45 s and inspected. Sample A was blister free with no observable changes, as shown in Fig. 3. Sample B was observed to have an increase in blister density (2.0 blisters/cm^2), as shown in Fig. 4. Sample C was observed to have a large number of blisters (4.7 blisters/cm^2), as shown in Fig. 5. The results of the anneal test are listed in Table II.

Annealing sample A immediately after LT-PECVD SiO_2 dielectric coating deposition produced changes to the film composition, outgassing the film before additional processing, preventing the formation of blisters. Annealing sample B immediately after front-side metal deposition created a small number of blisters due to outgassing. Annealing this sample a second time after back-side processing caused a slight increase in blister density. This demonstrates that annealing the coating before back-side processing contributes to a reduction in blister density. Annealing control sample C as the final step in the SCOW process created the largest number of blisters. As illustrated by the blister peaks present in the Nomarski image in Fig. 5, thermal cycling appears to result in ejection of gas or particulates from the dielectric coating, contributing to adhesion loss and blister formation.

Table I. SCOW anneal experiment processing steps

Step	Sample A	Sample B	Sample C (Control)
ICP-RIE ridge etch			
SiO_2 dielectric coating deposition	Anneal		
Ti/Au/Pt/Au		Anneal	
Lap-polish-Ge/Au/Ni/Au			
Back-side contact metal alloy	Anneal	Anneal	Anneal

Thermal Anneal

To assess changes induced by thermal processing, both SiO_2 test samples were annealed for 300 s at nine temperatures between 200°C and 1000°C followed by determination of refractive index and BHF etch rate. The change in BHF etch rate as a function of temperature is shown in Fig. 6. The change in measured film refractive index as a function of temperature is shown in Fig. 7. A clear change in refractive index and BHF etch rate for the LT-PECVD dielectric coating was observed with anneal temperature. The thermal SiO_2 dielectric coating

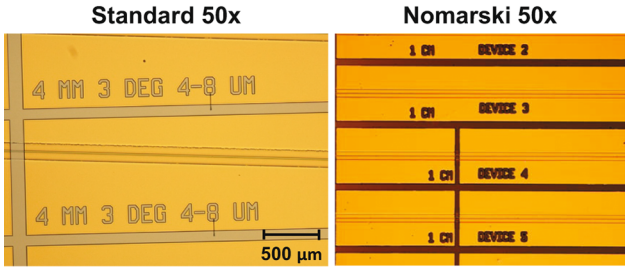

Fig. 3. Standard and Nomarski microscope images of sample A after back-side contact metal thermal anneal.

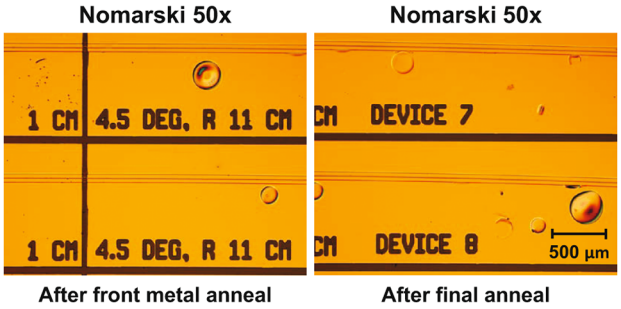

Fig. 4. Standard microscope images of sample B after front-side metal and final anneal steps.

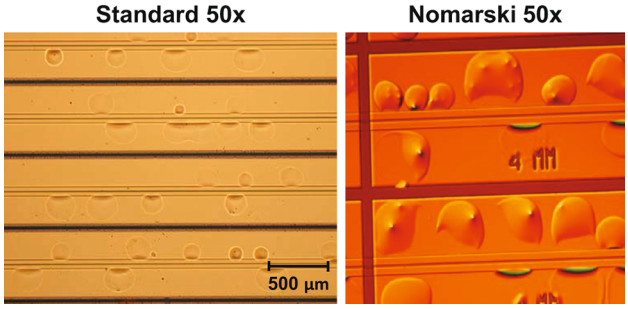

Fig. 5. Standard and Nomarski microscope images of sample C after back-side contact metal thermal anneal.

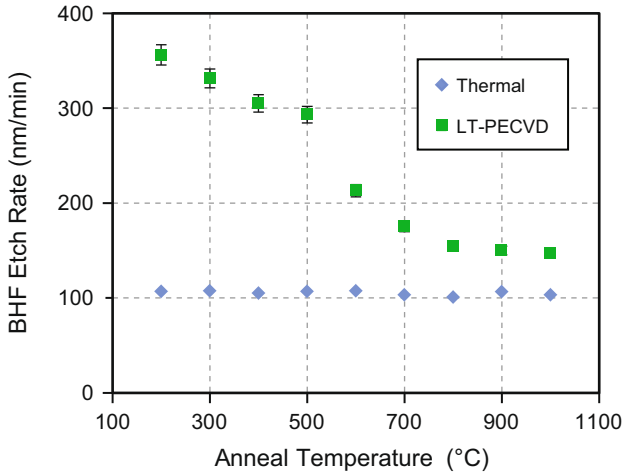

Fig. 6. Measured BHF etch rate of two SiO_2 dielectric coatings as a function of thermal-anneal temperature.

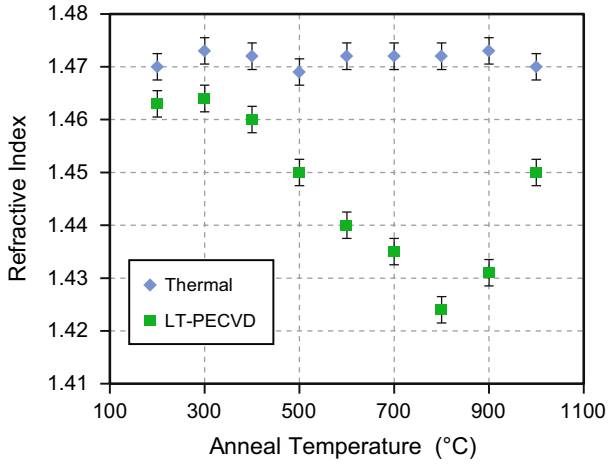

Fig. 7. Measured refractive index of two SiO_2 dielectric coatings as a function of thermal-anneal temperature.

Table II. SCOW anneal experiment results

Step	Sample A	Sample B	Sample C (Control)
ICP-RIE ridge etch	No change (NC)	NC	NC
SiO_2 dielectric coating deposition	Anneal-NC	NC	NC
Ti/Au/Pt/Au	NC	Anneal-blisters (0.5/cm^2)	NC
Lap-polish-Ge/Au/Ni/Au	NC	NC	NC
Back-side contact metal alloy	Anneal-NC	Anneal-blisters (2.0/cm^2)	Anneal-blisters (4.7/cm^2)

was stable throughout the anneal temperature range.

Previous studies of LT-PECVD coatings have documented changes in BHF etch rate and refractive index with increasing anneal temperature.[9,12,19] The change in BHF etch rate and refractive index of thermally annealed LT-PECVD SiO_2 dielectric coatings is a consequence of outgassing of loosely held components competing with physical changes such as increased bond density and improved quality of O–Si–O bonding.[9,12] At lower anneal temperatures, the refractive index declines. This is most likely a result of outgassing of N_2 and H_2. At higher anneal temperatures the refractive index levels off and begins to increase. This regime is most likely dominated by diminished outgassing and a physical reordering of the film. Similar changes in refractive index with anneal temperature have been reported for PECVD oxynitride coatings.[19]

Thermal Stress Bow

The thermal stress-bow experiment evaluated the LT-PECVD SiO_2-coated test wafers utilizing the Toho tool in stress–temperature measurement mode. The results of these measurements are shown in Fig. 8. Two stress–temperature measurement scans were performed, one immediately after LT-PECVD deposition to simulate the proposed postdeposition anneal procedure, and the second to simulate the back-side contact metal alloy anneal. The stress–temperature measurement employs a 45-min thermal ramp to reach maximum temperature,

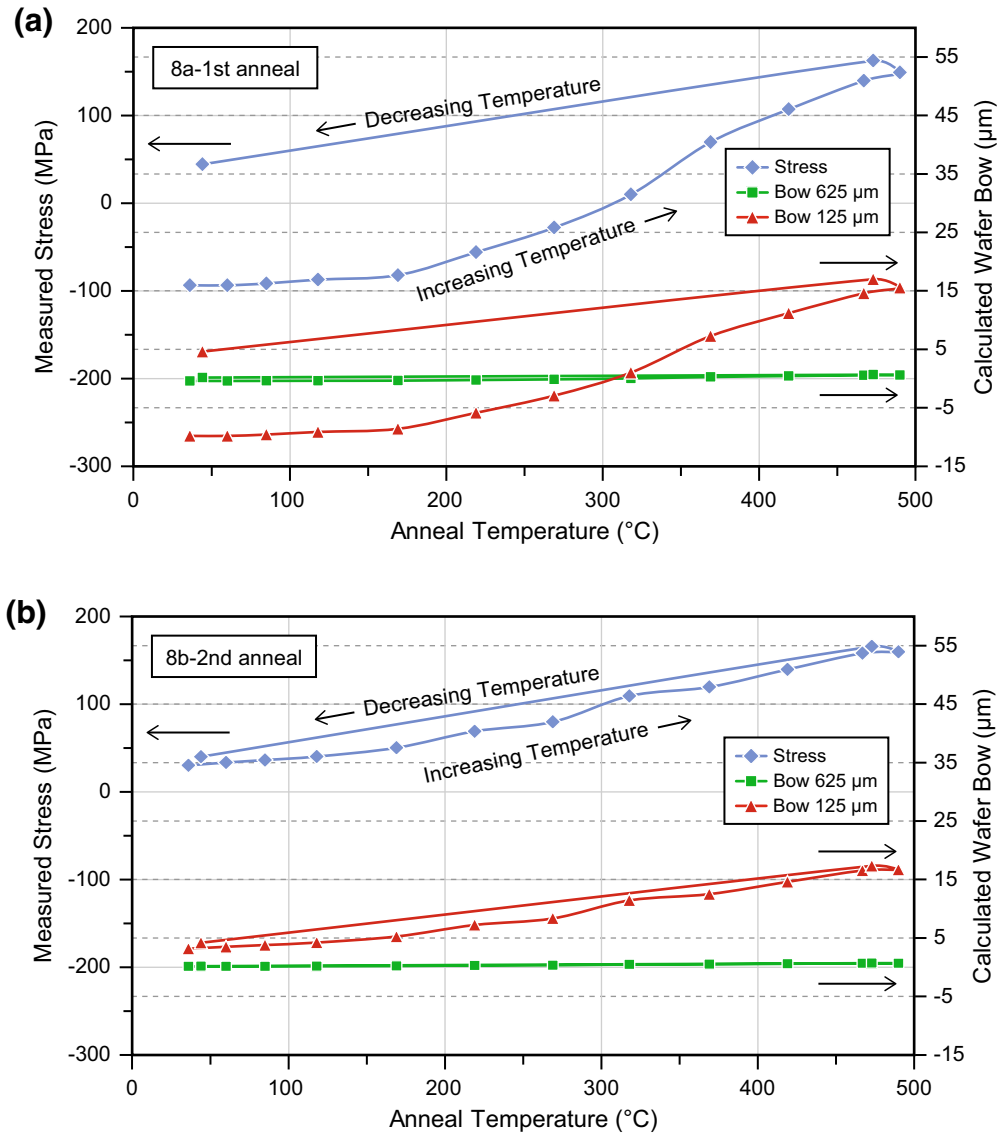

Fig. 8. Stress–temperature measurement of LT-PECVD SiO_2 dielectric coating deposited on a silicon wafer and the calculated wafer bow of a 30 mm × 30 mm GaAs wafer piece. Two thermal cycles are displayed: a first anneal (a) to simulate the postdeposition anneal and a second anneal (b) to simulate the back-side contact metal anneal.

compared with 45 s utilizing the RTA system. The measured change in coating stress for the stress–temperature measurements is similar in magnitude and direction (more tensile), when compared with wafers thermally processed utilizing the RTA system.

Stoney's equation describes the total stress of a deposited film based on measurement of the wafer radius of curvature before and after film deposition.[20,21] A common form of the equation relating thin-film stress to wafer bow is

$$\sigma = \frac{4}{3} \times \frac{E}{(1-\nu)} \times \frac{t_s^2 B}{t_f L^2}, \quad (1)$$

where σ is the total film stress, $E/(1-\nu)$ is the substrate elastic constant (E is Young's modulus and ν is Poisson ratio), t_s is the substrate thickness, t_f is the film thickness, B is the wafer bow, and L is the scan length.

Stress–temperature data presented in Fig. 8a show a large swing in SiO_2 dielectric coating film stress during the first anneal cycle, with a lasting change in stress as a result of changes in the coating properties. The stress data for the second anneal cycle presented in Fig. 8b point to a more modest thermal-stress-induced swing and minimal permanent change in coating stress. Differences in thermal expansion coefficient between the substrate and dielectric coating contribute to the measured stress values during each test cycle. These stress–temperature results substantiate a change in total film stress (σ) due to thermal processing. These stress data were used to approximate the impact of thermally induced changes on the bow of a 30 mm × 30 mm GaAs device wafer piece utilizing known substrate elastic constants for GaAs and standard SCOW fabrication SiO_2 dielectric coating (300 nm) and wafer thicknesses. Calculated bow values as a function of temperature are shown for 625 μm wafer thickness in Fig. 8a and b. The wafer bow variation throughout the two thermal-anneal cycles is minimal. The stress–temperature data were used to approximate the impact of thermally induced stress changes on the bow of a 125 μm thickness, 30 mm × 30 mm GaAs device wafer piece to simulate standard SCOW back-side processing. Calculated bow values as a function of temperature are shown for 125 μm wafer thickness in Fig. 8a and b. Performing the postdeposition first anneal on a thinned wafer is predicted to effect a >27 μm bow change on a 30 mm × 30 mm GaAs sample during thermal cycling.

Discussion

Based on process observations and experimental results we propose a blister formation mechanism for the initial fabrication sequence. Thermal cycling to facilitate back-side contact metal alloying was the final step after completion of front- and back-side wafer processing. The front-side SiO_2 dielectric coating sandwiched between the semiconductor surface and front-side contact metal layers outgassed when exposed to alloy temperatures, creating pockets of adhesion loss at the semiconductor and metal interfaces. During the thermal cycle, SiO_2 dielectric-coating stress changes would impact the bow of the thinned wafer. This flexing of the wafer in the direction of a more tensile profile caused metal-oxide layer deformation, stress relief by buckling, and loss of adhesion resulting in blister formation. Thus thermal cycling acts as the trigger for poor adhesion regions to release, creating blisters.

Thermal-annealing LT-PECVD SiO_2 dielectric coatings immediately after deposition on full-thickness device wafers results in preemptive outgassing, and coating stress reduction with minimal impact on the in-process wafer bow. During the final back-side contact metal alloy step, the thermally stabilized SiO_2 dielectric coating would not contribute to adhesion loss or extreme changes in wafer bow. GaAs SCOW devices fabricated with the additional anneal procedure show no degradation in performance or reliability when compared with samples processed with only one anneal cycle. The dielectric coating thermal stabilization procedure eliminates front-side contact metal adhesion loss as a primary failure mechanism and results in greatly improved wafer and device yield. The GaAs full-wafer rejection rate dramatically improved from $>50\%$ to $\sim 4\%$, and the individual device yield per wafer was $>80\%$. Process engineers considering the incorporation of a thermal-anneal procedure into a device fabrication flow should examine postdeposition thermal processing in order to establish an optimal anneal temperature.

CONCLUSIONS

Postdeposition thermal treatment of LT-PECVD SiO_2 dielectric coatings results in layer outgassing, along with a reduction in coating stress. This thermal-anneal procedure stabilizes the dielectric coating before additional device processing, eliminating a primary source of adhesion loss and blister generation. GaAs SCOW device wafers fabricated using this new procedure have a low rejection rate ($<4\%$) due to front-side contact metal and dielectric coating adhesion issues; individual device yields per wafer averaged $>80\%$.

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recommendations are those of the authors and are not necessarily endorsed by the US Government.

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