Modeling Gallium-Nitride based High Electron Mobility Transistors: Linking Device Physics to High Voltage and High Frequency Circuit Design

by

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Abstract

Gallium-Nitride-based high electron mobility transistor (HEMTs) technology is increasingly finding space in high voltage (HV) and high frequency (HF) circuit application domains. The superior breakdown electric field, high electron mobility, and high temperature performance of GaN HEMTs are the key factors for its use as HV switches in converters and active components of RF-power amplifiers. Designing circuits in both application regimes requires accurate compact device models that are grounded in physics and can describe the non-linear terminal characteristics.

Currently available compact models for HEMTs are empirical and hence are lacking in physical description of the device, which becomes a handicap in understanding key device-circuit interactions and in accurate estimation of device behavior in circuits. This thesis seeks to develop a physics-based compact model for GaN HEMTs from first principles which can be used as a design tool for technology optimization to identify device-performance bottlenecks on one hand and as a tool for circuit design to investigate the impact of behavioral nuances of the device on circuit performance, on the other.

Part of this thesis consists of demonstrations of the capabilities of the model to accurately predict device characteristics such as terminal DC- and pulsed-currents, charges, small-signal S-parameters, large-signal switching characteristics, load-pull,

source-pull and power-sweep, inter-modulation-distortion and noise-figure of both HV- and RF-devices.

The thesis also aims to tie device-physics concepts of carrier transport and charge distribution in GaN HEMTs to circuit-design through circuit-level evaluation. In the HV-application regime benchmarking is conducted against switching characteristics of a GaN DC-DC converter to understand the impact of device capacitances, field plates, temperature and charge-trapping on switching slew rates. In the RF-application regime validation is done against the large-signal characteristics of GaN-power amplifiers to study the output-power, efficiency and compression characteristics as function of class-of-operation. Noise-figure of low-noise amplifiers is tested to estimate the contributions of device-level noise sources, and validation against switching frequency and phase-noise characteristics of voltage-controlled oscillators is done to evaluate the noise performance of GaN HEMT technology. Evaluation of model-accuracy in determining the conversion-efficiency of RF-converters and linearity metrics of saturated non-linear amplifiers is carried out.

The key contribution of this work is to provide a tool in the form of a physics-based compact model to device-technology-engineers and circuit-designers, who can use it to evaluate the potential strengths and weaknesses of the emerging GaN technology.

Thesis Supervisor: Dimitri A. Antoniadis
Title: Ray and Maria Stata Professor of Electrical Engineering

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The Ph.D journey can only be successful and more importantly enjoyable if it is guided by an experienced Guru and I am grateful to my professor Dimitri Antoniadis for his invaluable support and mentorship during these years. The engineering skill sets and the approach to tackle problems that I have learnt from him will be valuable for the rest of my life. I am very thankful to my co-advisor Professor Tomas Palacios, whose efforts at advancing GaN-technology is an inspiration. I appreciate his ability to identify the big-picture, tackle essential bottlenecks to new technologies and his regular guidance to solve the key problems in GaN-modeling. I am also thankful to Professor David Perreault for his advise as my doctoral committee member.

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Chapter 1

Gallium-Nitride Technology: Current Status and Promise of Future

Silicon has been the undoubted driver behind the electronic industry's growth story since the invention of the integrated circuit (IC) in 1958. In terms of semiconductor devices for power processing, variants of bipolar junction transistors (BJTs) followed by power MOSFETs since 1976 have catered to the needs of switching power conversion applications in the industry [1]. Many innovative solutions such as lateral FETs, LDMOS, and vertical FETs have kept up with the demand in terms of efficiency, cost effectiveness, size, and reliability. Even though devices such as insulated bipolar junction transistors (IGBT) and super junction transistors (so called CoolMOS) surfaced as solutions to address concerns about diminishing returns in power processing efficiency with conventional technology evolution, recently alternate semiconductor materials such as SiC and Gallium Nitride (GaN) have emerged as attractive candidates for niche spaces within HV-market.

In the domain of power delivery at RF frequency range, III-V semiconductors based on GaAs and InP have been trying to elbow silicon ever since the discovery of the Gunn diode in 1962 [2]. Starting with the GaAs MESFETs, high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), devices have been pushing the RF frontiers both in terms of the frequency bands (from HF band to mm-wave) and power density levels at any given band. GaN is a new technology

that is promising because of its potential to deliver high power levels of about 30 dBm even in high frequency W-band (75-110 GHz) using fewer wide-periphery devices without significant power-combining circuitry due to its inherent high power-density properties [3]. GaN is a uniquely placed III-V system which exhibits wide bandgap, high heat capacity, high thermal conductivity together with low on-resistance and high carrier mobility in devices built with a heterostructure configuration using GaN and AlGaN. The first GaN material was produced by passing ammonia over hot Gallium

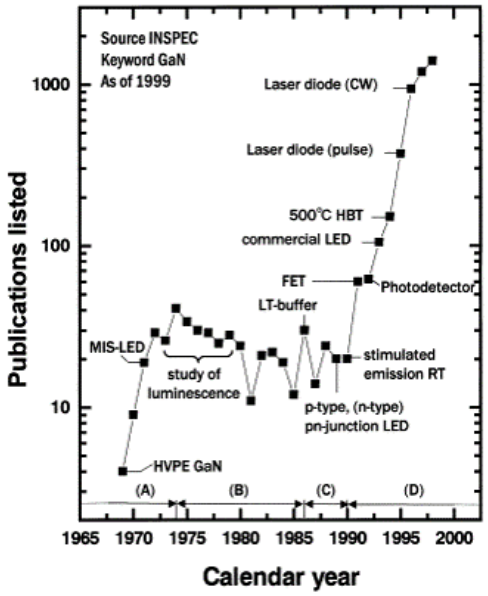


Figure 1-1: Milestones of GaN research [4]. GaN research in both optoelectronics and electronics progressed rapidly after demonstrating the growth of high quality GaN and conductivity control of both p- and n-type GaN in the early 1990s.

by Jusa and Hahn in 1938. Since then numerous research breakthroughs and progress have been made in GaN based electronics [3]. Originally, nitride semiconductors were considered as suitable candidates for optoelectronics due to their unique properties such as direct tunable bandgap from 6.2 eV (AlN) to 0.7 eV (InN), piezoelectricity, polarization and so on. Large area GaN was grown by hydride vapor phase epitaxy (HVPE) directly on sapphire by Maruska and Tietjen in 1969 [5] and in 1993 hig-brightness blue light-emitting-diodes (LEDs) was developed by Nichia. Since then this material system has become primary choice for blue LEDs, blue LASER diodes and other optoelectronic devices. Fig.1-1 shows some of the major milestones in early GaN research [4].

Semiconductor		Si	AlGaAs/ InGaAs	InAlAs/ InGaAs	SiC	AlGaN/ GaN
Characterisitic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm^2/Vs	1500	8500	5400	700	1500-2200
Saturated (peak) electron velocity	$\times 10^7$ cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0

Figure 1-2: Table showing properties of different material systems. GaN shows a combination of high electron mobility, electron velocity and breakdown field [5].

Demonstration of heterostructure device a.k.a *HEMT in GaN platform* by Mimura (1975) and M. A. Khan (1994) brought about a shift in the focus of GaN-technology-research from optoelectronics to electronics. Since then, GaN-HEMT has held the overall record in the performance indicators shown in Fig.1-2. The competitive advantage of GaN compared to other technology is due to its superior electron density ($\approx 1 \times 10^{13}\ cm^{-2}$), high electron mobility in two dimensional electron gas (2DEG) ($\approx 1500\ cm^2/Vs$), good thermal conductivity ($\approx 1.5\ W/cm.K$) and high breakdown field ($\approx 3.0\ MV/cm$). The electron mobility in GaN is significantly higher than the surface-mobility of electrons in Si-power-MOSFETs and SiC-FETs that enables GaN devices to have lower footprint, higher speed and efficiency as switches in power converters. The high breakdown field in GaN that is an order-of-magnitude higher than Si and GaAs material systems make it possible to deliver high power levels at higher operating frequency with significant linearity and power-added-efficiency (PAE) in RF-power amplifiers.

1.1 Status of GaN-HEMTs in power electronics

The key areas in power conversion industry where GaN insertion is imminent are AC-DC switching power supplies, variable speed motor drives, fluorescent lights, DC-DC converters etc. In these applications, the key device performance metrics are breakdown voltage (BV), specific on-resistance (R_{dson}) and total-gate-charge (Q_g) and in all the three metrics GaN-technology fares better than its competitors as shown in Fig. 1-3. The BV vs. R_{dson} plot demonstrates that for a given BV the R_{dson} and hence conduction losses in GaN-switches are much lower, while for a given

R_{dson} and BV, the device footprint is smaller. In addition, the absence of pn-junctions in the device unlike in Si-powerFETs leads to lower gate-charge and switching losses.

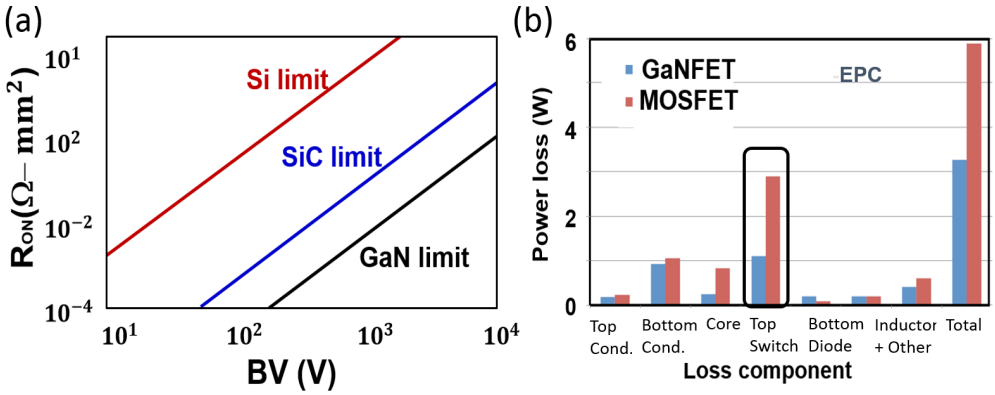


Figure 1-3: (a) The theoretical R_{dson} and BV plots for GaN, Si and SiC showing improved characteristics of GaN compared to other technologies. (b) The important loss components for a $12\ V - 1.2\ V$ buck converter operating at 1 MHz converter showing significantly lower switching loss due to lower gate charge in GaN switch (circuit board from EPC) [4].

These disruptive advantages have attracted some 15 technology manufacturers to invest in GaN-on-Si HEMT power device development. The full list can be found in [6] but includes IR, EPC, Transphorm, Fujitsu, Sanken, Toshiba, TI, Freescale among others. The key challenges in the adoption of the technology remains cost and reliability. While the use of inexpensive Si substrates and reduced cost of growth layers can offset the cost advantage of Si-technology in the long run, reliability of GaN-HEMTs under switching conditions at high stress voltage and temperature compliant with JEDEC standard currently seems to be the key bottleneck for GaN commercialization. On the other hand, second order effects such as gate breakdown, current collapse[1] and so on are being considerably mitigated through unique technology innovations. Meanwhile many products are beginning to emerge which offer single package solutions (CMOS driver + GaN switches) via flip-chip or dual package solutions [4] for $< 1000\ V$ power conversion applications. The advantages of GaN-technology can be visualized in Fig.1-4 by comparing these products against their competing solutions in Si in terms of form-factor and efficiency.

[1]Current collapse is a phenomenon caused by trap-states in GaN-HEMTs which results in an increase of R_{dson} of the device under switching conditions compared to its value under DC. The effect is discussed in detail in section 9 of chapter 3.

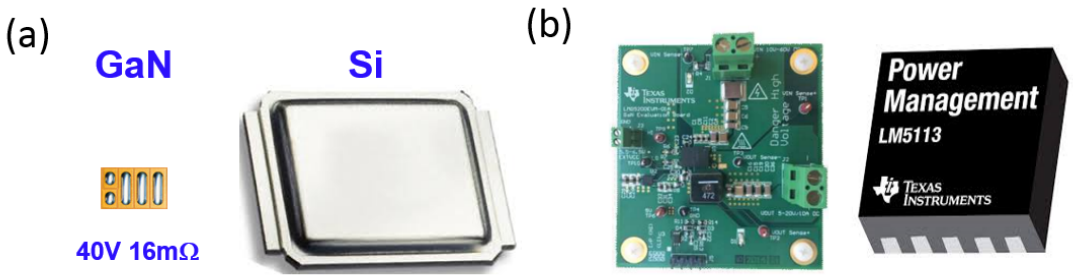


Figure 1-4: (a) Comparison of power MOSFET in package with eGaN-FETs from EPC showing the size difference for the same device-metrics [4] (b) The LMG5200 10 A, 80 V GaN half-bridge power module with integrated driver from TI which satisfies the JEDEC standards demonstrating the arrival of GaN-HEMTs in the power market.

1.2 Status of GaN-HEMTs in RF-electronics

The key advantage of GaN for RF applications is its ability to deliver high power densities of about 5 W/mm compared to 1 W/mm for GaAs and 0.3 W/mm for Si enabled by its high charge density and electron-saturation-velocity resulting in higher current densities [7]. In addition lower capacitances and power-combining losses facilitates the design of wider bandwidth power amplifiers (PAs) with higher gain and output power. The added advantage of high BV of GaN enables higher voltage of operation increasing the linear range of large-signal operation which means that even under high input-power levels, the output linearity is less compromised in comparison to Si-LDMOS solutions. The application regimes that can take advantage of these benefits range from radar, CATV, space applications, SatCom, 3G/4G base-stations, WIMAX/LTE PAs and other MMICs spanning L-band to mm-wave bands. Fig.1-5(a) shows the comparison of different technologies in terms of the figures-of-merit relevant to these RF applications. The inherent trade-off between BV and f_{max} (maximum frequency upto which FETs can deliver power-amplification) is shown in Fig.1-5(b) for GaN-technology and the strength of GaN-system to deliver power-amplification upto 200 GHz with BV of 100 V (a record among various RF-material systems) is evident from the figure, highlighting the overall advantage to GaN in satisfying the RF-application requirements.

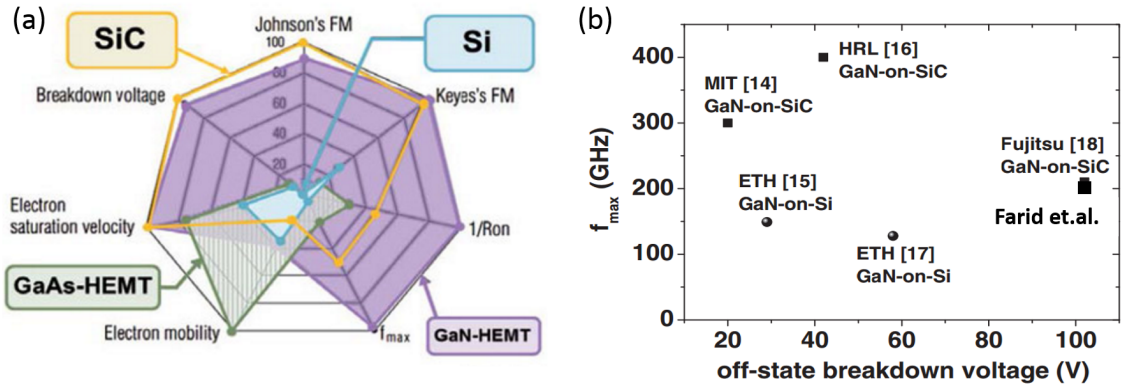


Figure 1-5: (a) Comparison of RF- performance metrics among different technologies and (b) state-of-the-art demonstrations of GaN-HEMTs showing f_{max} vs. BV metric. The high I_{max} and BV combination of GaN gives it the benefit of high power levels and linearity for transmitter PAs while good Johnson-FoM means that even receiver LNA noise figure performance improves with GaN technology.

These advantages have attracted many players such as HRL, Panasonic, STM, NXP, Cree [Wolfspeed], RFMD, Triquint [Qorvo] etc. in the RF market much earlier than in the power market [6]. The key challenges in the adoption of the technology are substrate power-losses, thermal management and reliability. GaN-on-SiC instead of GaN-on-Si is the answer to cut down substrate losses even though it raises the MMIC cost since cost is less of an issue for RF-applications compared to the HV-regime. The high power density in GaN causing localized heating requires dedicated cooling systems and impacts reliability which still is an active research area in the field. In spite of significant challenges that require constant device technology improvements,

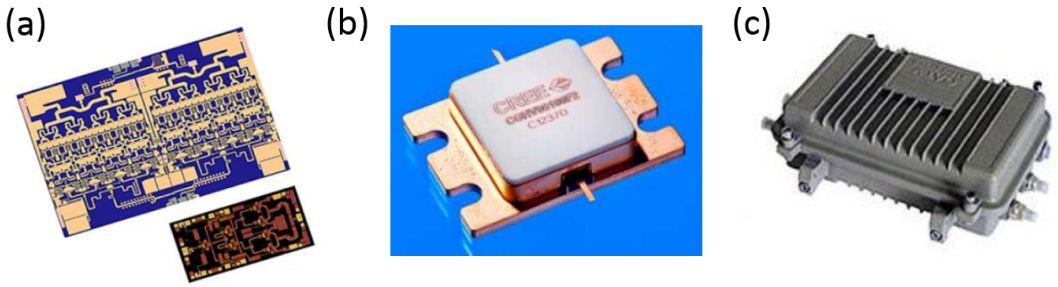


Figure 1-6: (a) Triquint's TGS2354 GaN-on-SiC switch die compared against their GaAs-MMIC (b) Cree (Wolfspeed) GaN-HEMTs offer higher bandwidth and power densities in the range of 10 MHz up to 18 GHz (c) GaN-based CATV system that provides wide-band power with same linearity compared to GaAs for 20% less current.

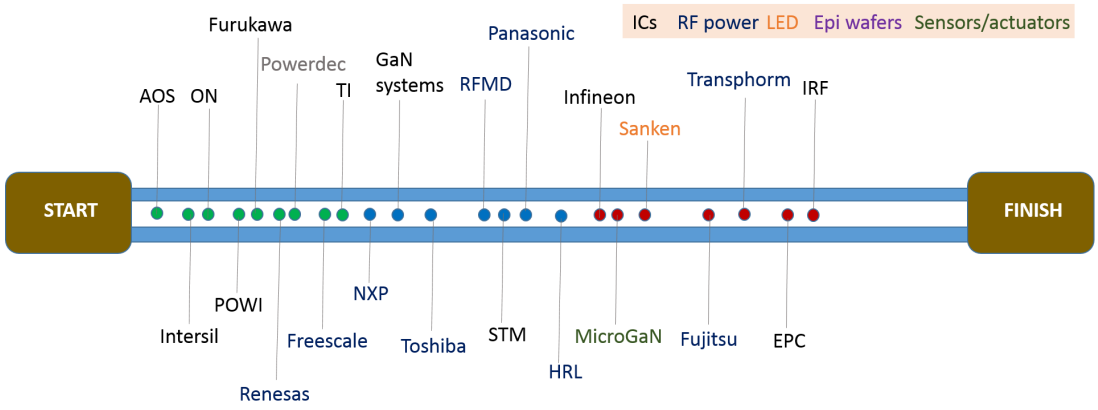


Figure 1-7: Venture-Qs [6] analysis of the positions of various technology companies in GaN technology ramp-up showing as many as 23 companies who are in advanced product development stage [2012 status].

a streamline of products have begun to emerge in the RF domain demonstrating the advantage of GaN over previous technologies in such products. Fig.1-6 shows a few products from leading companies showing improved form-factor and performance metrics when compared to earlier components.

The summary of the current status of GaN-HEMT in the semiconductor industry is highlighted in Fig.1-7. By looking at the position of industry players in the race for commercialization in GaN, it becomes clear that all the big players of both RF and power domains have invested resources in this technology indicating the widening adoption of GaN-HEMTs. Further device scaling, however requires that the outstanding issues in the device technology and circuit design be addressed and mitigated and will be discussed in the following sub-section.

1.3 Challenges and future of scaling GaN technology

Companies that are developing GaN technology have three big device-technology challenges ahead of them: containing the current collapse phenomenon, developing technologies for enhancement mode (E-mode) HEMTs, and improving device reliability [6]. Advances in surface treatments and passivation layers along with field plate engineering have shown promise in the fronts of device-reliability and current collapse. Fig.1-8(a) shows work in this direction [8] to mitigate the effects of current

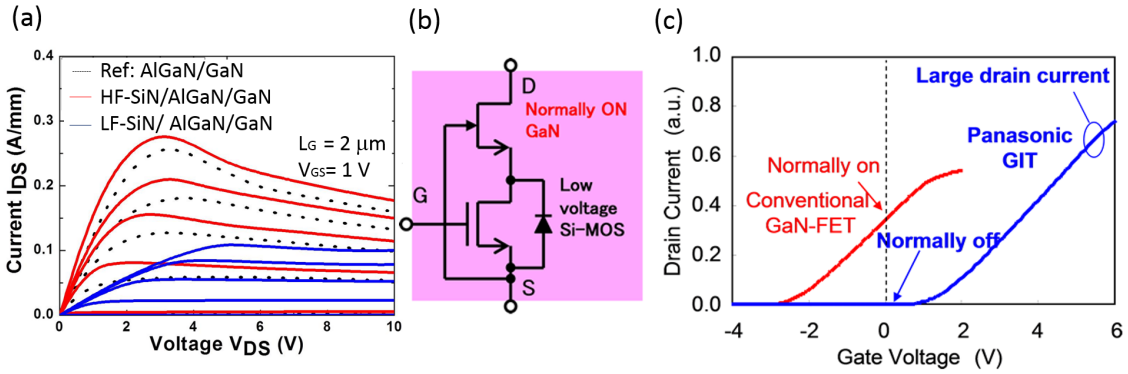


Figure 1-8: (a) Surface treatments by using SiN-passivation layers are shown to mitigate current collapse in [8]. (b) Casode-solution to obtain E-mode (positive threshold voltage) devices by using a low-voltage conventional Si-FET in series with a D-mode GaN-HEMT is currently provided by EPC. (c) An alternate solution to obtain E-mode devices is to use a p-GaN cap layer in the heterostructure under the gate to shift the threshold voltage to positive values and is provided by Panasonic.

collapse with surface treatment and show promise. Recent work on Cascode shown in Fig.1-8(b) by EPC, and p-GaN or the so-called gate-injection-transistor (GIT) shown in Fig.1-8(c) by Panasonic along with recessed gate technologies are some of the answers to the E-mode HEMT requirement. With this background the future of GaN technology seems to be in an upward swing.

In addition to improvements in device-technology, allied tools for circuit design need to be put in place as GaN-based systems are emerging in the market. Both HV and RF circuit design problems are highly non-linear, large-signal, specification-constrained design challenges. To aid such circuit design, accurate device-level compact models that describe the stand-alone device terminal characteristics as well as device behavior in circuits are critically required. The next section reviews the current state-of-the-art models in the industry and the justification for developing a new physics-based compact model for GaN HEMTs which is the topic of this thesis.

Chapter 2

Overview of State-of-the-art Compact Models for III-V HEMTs

Compact Modeling refers to the development of models for integrated semiconductor devices for use in circuit simulations. The models are used to reproduce device terminal behavior, which in the case of electronic devices consist of terminal-currents and charges. The key requirements are accuracy, computational efficiency, simple parameter extraction, and relative model simplicity for a circuit or system-level simulation. The users of compact models are typically IC designers, but sometimes the users also include device-technology engineers who use physics-based compact models as a substitute for intensive technology-computer aided design (T-CAD) for obtaining feedback on their device-design. Physical grounding in models is often preferred for the ease of statistical and PVT-corner (process-, voltage-, temperature-corner) simulations along with predictive capability for estimating the behavior of the next technology-node [9].

The importance of compact models in the semiconductor industry is growing because of the rise in analog content in modern ICs, increasing variation in advanced nodes of conventional technologies, scaling of frequency and device-counts, and hetero-integration of Si-devices with III-V heterostructure devices, MEMs and other sensors. A multitude of research activities in this area are responding to the growing demand for compact models, because of which streamlining and standardization of models for

industry-use becomes critical. The compact modeling coalition (CMC) is a working group in the electronic-design-automation (EDA) setup to promote the standardization of compact-semiconductor models across SPICE modeling platforms used in the industry. Realizing the increasing commercial potential of the upcoming GaN-technology, there is on-going initiative by the CMC to standardize GaN-model that requires models to satisfy standard qualification criteria, which will be briefly described in this chapter. The chapter also focuses on the available GaN-compact models that show promise and includes an analysis of their potential strengths and weaknesses in terms of their ability to capture device-physics and satisfying the CMC requirements. The models discussed in this chapter typically cater to RF-GaN-HEMTs (and indeed any RF-III-V HEMT) but could in principal be extended to the HV-device after substantial additions to the core model equations.

Historically III-V device models were formulated to cater to GaAs-based technologies for RF-applications with little modeling effort on III-V high voltage devices. Some of the conventional III-V RF-models are the Curtice model [10], the Angelov model [11], the EEHEMT (originally Eesof GaAs HEMT) [7] model which are now industry standards for high frequency III-V circuit design. As GaN technology matures in terms of process and fabrication technology, the focus of GaN research is shifting to modeling and circuit design. In this scenario, there is an increasing demand for accurate non-linear models which means that the standard III-V models for GaAs, InP technology are 'tweaked' to cater to the new GaN technology. On the HV side, there is a lack of accurate III-V models as GaN is one of the frontier III-V materials to be used for HV applications.

The aforementioned conventional models are severely lacking in capturing the physics of operation in GaN HEMTs as they are mostly empirical curve-fitting exercises. This results in the usage of a large number of non-physical fitting parameters whose extraction differs widely for devices based on different process techniques and even for different geometry variations within the same process. Separate model formulations become necessary for capturing different terminal characteristics such as currents, charges and capacitances. Furthermore no intuition can be learnt with re-

gard to the behavior of the device in circuits. The use of such models is to quickly evaluate and translate the technology to system-level via a rough description of the device at the expense of compromised accuracy. An overview of these models are given in the following section, highlighting the approach used and the resulting limitations.

2.1 Conventional empirical models

Look-up-tables and conventional empirical models act as the first-pass translational tools of information transfer from device-level measurements to circuit-design. Look-up tables or the so-called table-based models are tables obtained from device measurements spanning operational bias, temperature and frequency range of interest. Since the data is obtained from actual measurements, they are accurate in the measurement range but lack predictive capability and are not suitable for processes which have significant variation. The advantages include the ease of model development which only requires measurements and guaranteed accuracy of the model within the measurement range. The disadvantages are the need for repeated measurements, huge data processing, absence of physical intuition and learnings. Empirical models provide a step-up progress over table-based models, since they minimize the number of measurements to only those required to extract parameters and calibrate the model. The models are mathematical equations without any physical underpinnings but they can mimic the measured device-data over a wider range of temperature, bias and frequency once the model is extracted from fewer measurement points. The Angelov, Curtice and EEHEMT models are well-known empirical models described here.

2.1.1 Angelov model

The Angelov model (Chalmers U. model) is a popular empirical non-linear IV equivalent circuit type model suitable for GaAs, GaN, SiC and even CMOS technologies. Shown in Fig.2-1 is the equivalent circuit that is implemented by the model as given in [11]. While many of the elements in the circuit shown in Fig.2-1 capture parasitics at device nodes, the core model equations govern currents I_d, I_g, and capacitances

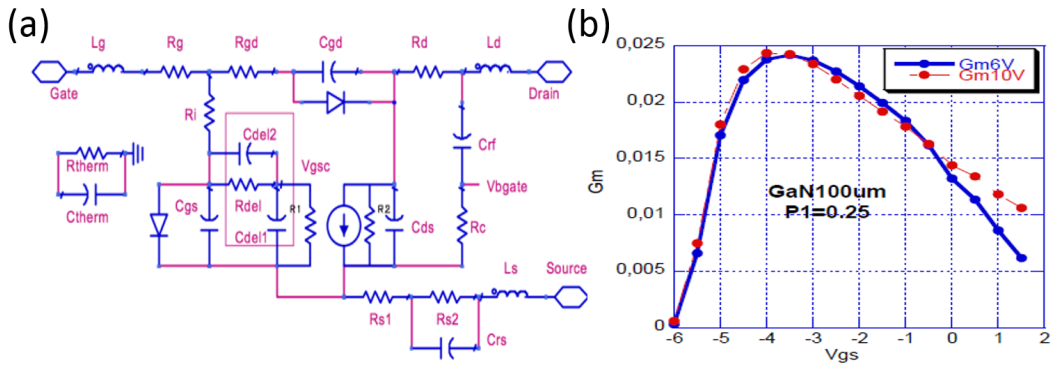


Figure 2-1: (a) Sub-circuit equivalent circuit of Angelov model and (b) 'bell-shaped' transconductance g_m characteristic which the Angelov model captures.

C_{gs}, C_{gs} and C_{ds}. The approach followed in the Angelov model is to capture the non-linearity in transconductance (g_m) observed in GaN, GaAs and other material technologies. This is shown in Fig.2-1 which shows the g_m plots exhibit the so called 'bell shaped' characteristic. Capturing this shape is the key idea around which Angelov model seems to have been built. The formulation for g_m (ignoring V_{ds} dependence) in the model is given by$g_m = g_{mpk}(1 - tanh^2[p_{1m}(V_{gs} - V_k)])$ (2.1)

where g_{mpk}, p_{1m} and V_k are fitting parameters. The reason for using $tanh()$ formulation as given in [11] is to ensure that current expressions have infinite derivatives and the model can be used with ease for harmonic-balance simulations. Clearly the core model is empirical in nature and is not physics based. The current then becomes,

$$I_{ds} = I_{pk}(1 + tanh(\psi))(1 + \lambda V_{ds})tanh(\alpha V_{ds}) \tag{2.2}$$

where I_{pk} is the drain current at which we have maximum transconductance, with the contribution from the output conductance subtracted. λ is the channel length modulation parameter and α is the saturation voltage parameter. The parameters α and λ are the same as those in the Statz and Curtice models. ψ is in general a power series function centered at V_{pk} with V_{gs} as a variable,

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 \tag{2.3}$$

where V_{pk} is the gate voltage for maximum transconductance g_{mpk}. The selected $I_d[V_{ds}, V_{gs}]$ function has well-defined derivatives. According to [11], the Angelov model has about 90 parameters with which it appears to capture the non-linear behavior and the resulting harmonics in power circuits. However the model is non- speculative since it is not physics based. Any changes to the device dimensions or process technology require that the model has to re-fitted to the characteristics. This increases the optimization time. In addition, it makes the model non-scalable with regard to geometry.

2.1.2 Statz and Curtice models

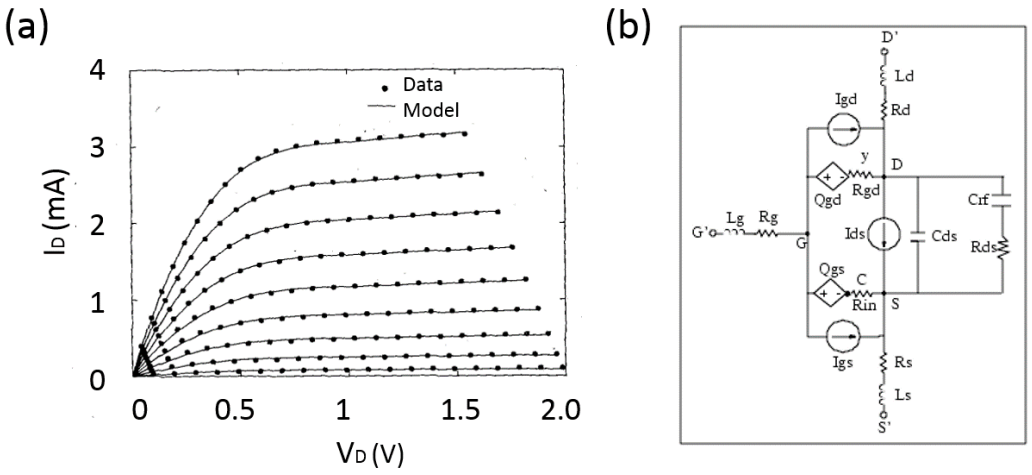


Figure 2-2: (a) The current-voltage characteristics of Statz model and (b) equivalent circuit in Curtice-3 model offered by Agilent.

The seminal papers by Curtice [10] in 1985 and Statz [12] in 1987 form the basis of many empirical-FET models that are used in commercial RF-simulations. The models are available in all commercial simulators and are adopted by power-amplifier designers. The Statz model was proposed for GaA-FET device that was compatible with U. C. Berkeley-SPICE simulators. The FET-drain current is similar to 2.1.1 with similar model parameter definitions and is given by

$$I_{ds} = \beta(V_{gs} - V_T)^2(1 + \lambda V_{ds})tanh(\alpha V_{ds}) \tag{2.4}$$

and is extended to include second-order effects such as velocity-saturation, channel-length-modulation, and higher-order differentiability as follows

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)}[1 - (1 - \frac{\alpha V_{ds}}{3})^3](1 + \lambda V_{ds}) \quad for \quad 0 < V_{ds} < \frac{3}{\alpha} \tag{2.5}$$

$$I_{ds} = \frac{\beta(V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)}(1 + \lambda V_{ds}) \quad for \quad V_{ds} > \frac{3}{\alpha} \tag{2.6}$$

There are several additional empirical equations for capacitances with some underlying physical grounding, but they require large number of additional non-physical parameters. In addition, unique effects in GaN cannot be captured unless the core-model is changed significantly. Furthermore the mathematical robustness of the model in case of GaN-HEMTs with field plates, access regions and charge trapping has not been verified.

There are several variants of Curtice model available currently such as CFET, CHEMT but the model was originally proposed for GaAs FETs and is extended to other material systems including recently to GaN HEMTs. Fig.2-2(b) is the equivalent circuit of Curtice model as depicted in [10]. Once again the terminal currents I_{ds}, I_{dg} and I_{gs} along with capacitances C_{gs} and C_{gd} are modeled through non-linear semi-empirical functions dependent on terminal voltages. The currents have a polynomial Volterra-series-like dependence on the input voltage as shown:

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) tanh(\gamma V_{out}(t)) \tag{2.7}$$

Here β is the current factor while the remaining parameters are fitting parameters. In a similar fashion, the capacitances are also non-linear functions of voltages. The small signal equivalent circuit elements such as g_m, g_{ds} etc. which are obtained from differentiating currents have to be tweaked to account for access region effects [10]. As given in [13], the Curtice model in its Curtice-3 form is not geometry scalable and has 59 parameters. It does not model self-heating effects. However the model variant submitted to the compact modeling council (CMC) has 55 parameters with geometry scalability and electro-thermal effects incorporated.

2.1.3 EEHEMT model

The Eesof HEMT model originally proposed for GaAs HEMTs is an extension of the Curtice model [14]. It is an empirical model that was developed by Agilent technologies for the express purpose of fitting measured electrical behavior of HEMTs. The model includes: isothermal I_{ds} model fits, flexible g_m formulation, self-heating correction for I_{ds}, charge model that fits measured capacitance values, dispersion model that permits fitting of both high-frequency conductances and DC characteristics, and breakdown model that describes I_{gd} as a function of both V_{gs} and V_{ds}. A thorough description of the model details is given in [7] but a few key equations governing I_{ds} and C_{gs} are repeated here. The EEHEMT model is defined for different regions of device operation based on V_{gs}. The different model equations with 75 parameters are then 'stitched' together to get the complete model. The different regions are based on g_m plot shown in Fig.2-3(a) with the equivalent circuit shown in Fig.2-3(b). The

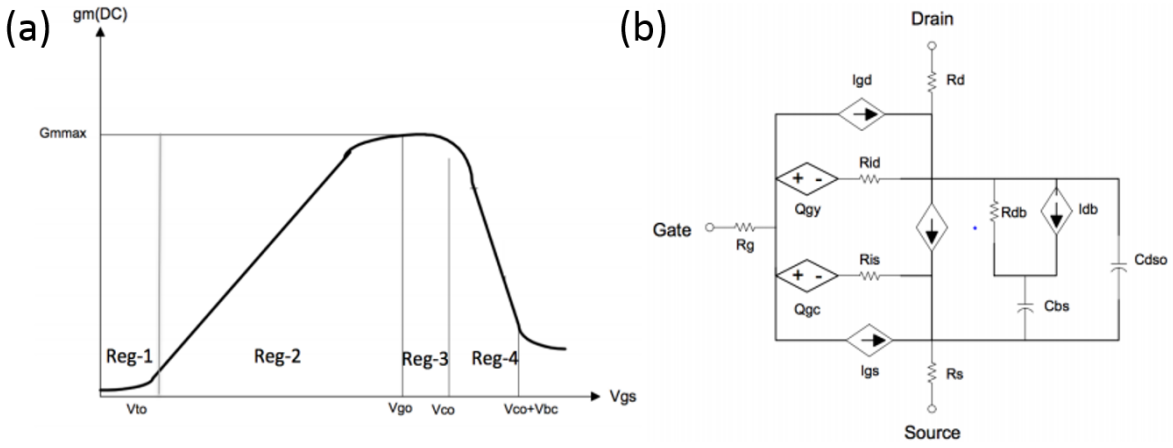


Figure 2-3: (a) Region-wise modeling of transconductance of EEHEMT and (b) equivalent circuit in EEHEMT model.

first region (Reg-1) is below threshold voltage, the second region (Reg-2) is the linear g_m region between maximum transconductance and threshold voltage, the remaining regions (Regs -3 and 4) are after maximum transconductance and include the compressed g_m effects at large V_{gs}. In Reg-3 and Reg-4 I_{ds} ($V_{gs} > V_g$) expressions are

given by

$$I_{ds} = g_{mmax}[V_x \frac{V_{go} + V_{to}}{2} + V_{ch}] \qquad V_x = (V_{gs}V_{ch})[1 + \gamma(V_{dso}V_{ds})] \tag{2.8}$$

In Reg-2 where $V_t < V_{gs} < V_{g0}$, the current equation is given by

$$I_{ds} = \frac{g_{mmax}}{2}[V_x - (V_{to} - V_{ch}) + \frac{(V_{to} - V_{go})}{\pi} sin(\pi \frac{(V_x - (V_{go} - V_{ch}))}{(V_{to} - V_{go})})] \tag{2.9}$$

In Reg-1, below-threshold, the drain current I_{ds} is equal to zero (which is problematic in simulating certain classes of power amplifiers which operate in moderate-accumulation). Additional equations are required to capture each of the terminal capacitances which makes the model end up with 75 parameters to fit a simple RF-device structure. From the brief overview of the above three models, it is clear that the industry-standard empirical models leave much to be desired in terms of capturing the device physics and hence accuracy, along with the ease of model parameter extraction for any given technology. None of the models is capable of including all the extraneous effects of GaN HEMTs outside the channel. Furthermore HV-device structures are not catered to in these models at all. GaN-based circuit-design therefore requires standard models across various simulator platforms with emphasis on physical models which will be discussed in the next section.

2.2 Physics-based compact models for GaN HEMTs

Physics-based device-models are of two variants: 'analytical-models' and 'compact-models', both of which are based on analytical expressions obtained from solutions to the laws governing relevant physical phenomena. However the key distinction between the two is that the former lays emphasis on physical-rigor and may be regional, and have clearly stated-assumptions on approximations while the latter variant: namely compact models are an adoption of the latter targeting circuit-simulations. The former is more broader in scope targeted to evaluate and study any new device/system and subsumes the latter. Usually corners have to be cut for going from first-to sec-

ond category so that we can ensure that the compact models are robust for complex circuit-simulations with ease of computational efficiency and the hope is that the compromise in physics is minimal with the use of minimum extent of empirical factors such as expressions and/or parameters. Developing such compact models is the goal of this thesis work. Physics-based compact models for GaN-HEMTs are obtained by analytical approximations to self-consistent solutions of channel electrostatics (Poisson equation) and carrier transport equations (drift-diffusion) that are either charge-based or surface-potential-based. The terminal characteristics in charge-based models are expressed as functions of channel-charge at source- and drain-end while they are expressed as functions of surface-potential at the two ends in the surface-potential models. Three well known physical compact models namely, the Tsinghua, the ASM-HEMT and the HSP-LETI models for GaN-HEMTs are briefly discussed and their performance is analyzed in this section.

2.2.1 Tsinghua model

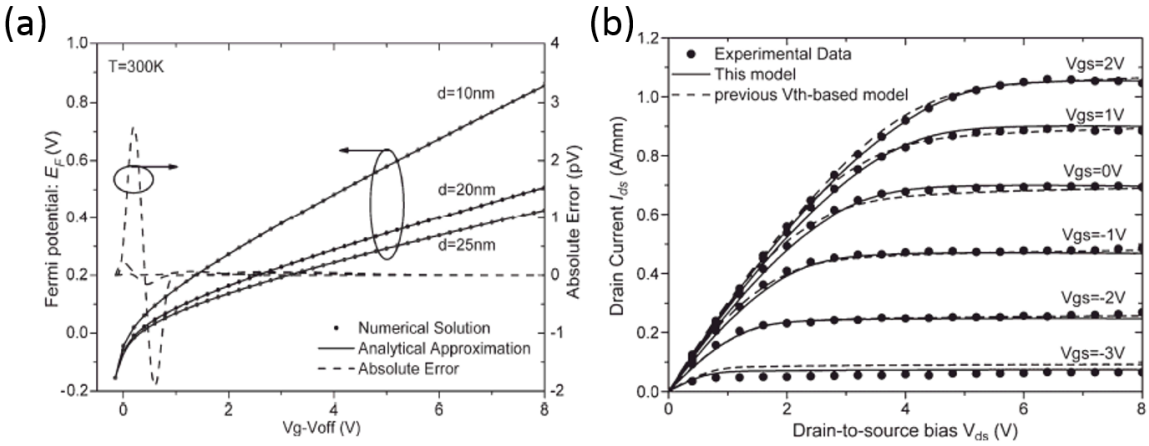


Figure 2-4: (a) Comparison of accuracy of Fermi-potential (E_F) with numerical solution (b) Model comparison against measurements [15].

The Tsinghua model is a surface-potential-based approach to capture terminal characteristics in GaN-HEMTs in which the Fermi-potential (E_F) is obtained in the form of closed-form analytical approximations to the charge-density-of-states (DOS) and Poisson equations. The formulation of terminal currents and charges is based

on this calculation and is found to be valid over a wide bias and temperature range as shown in Fig.2-4 and in detail in [15]. Unlike constant-threshold voltage based models in which the E_F is pinned, this methodology ensures improved accuracy even in moderate-accumulation regimes in the operation of the device as it self-consistently solves for E_F and the charge-density in the potential-well (n_s). Explicit approximations to the implicit-transcendental functions ensures fast and reduced computational requirements. The detailed model formulation can be found in [15] and the model equations are not reproduced here, but it is clear that the model is capable of including several second-order effects in the channel and is symmetric with respect to source and drain terminals (Gummel Symmetry).

However the model does not include the effect of access regions and field plates, channel-noise, small- and large-signal validation which is the main priority for RF-designers is not demonstrated. The number of parameters in the model seem to be large with several fitting parameters to combine linear-to-saturation regions.

2.2.2 ASM-HEMT model

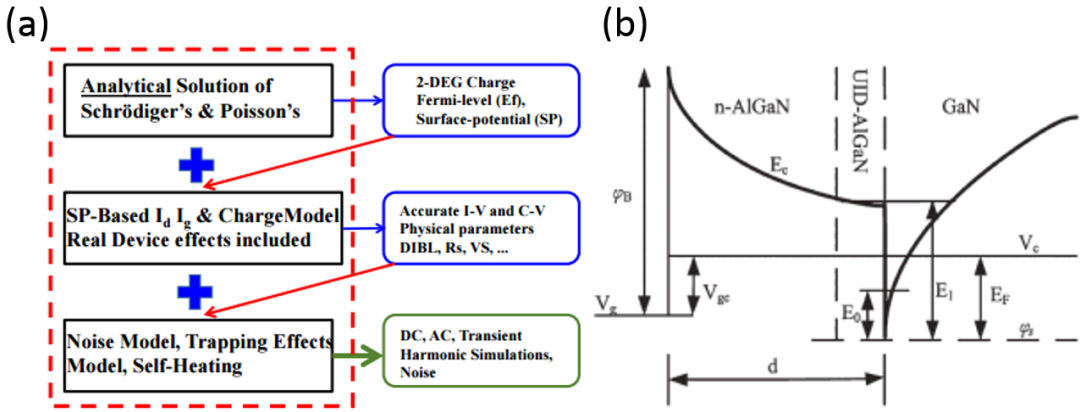


Figure 2-5: (a)The workflow for terminal characteristics and (b) the surface-potential calculation approach in ASM-HEMT model [16].

The ASM-HEMT model is also a surface-potential model which incorporates most of the requirements for an industry-standard model by computing a solution to the surface potential in the channel from Schrödinger-Poisson coupled equations making

reasonable assumption on band occupation. The work-flow of the model is highlighted in Fig. 2-5 which shows a complete flow of the model formulation. The ASM-HEMT model captures most of the device-level terminal characteristics [16] but is not tested for robustness at the circuit-simulation level which is another key cornerstone that must be achieved by any successful model. It is found to accurately model the RF-device characteristics (both small- and large-signal characteristics) but not the characteristics of HV-GaN-HEMT including non-linear capacitances.

2.2.3 HSP-LETI model

The HSP model (acronym for HEMT Surface-Potential model) claims to include: the effects of the spontaneous and piezoelectric polarizations, incomplete donor activation, temperature dependence of different parameters and self-heating effect. Other effects, like series resistances, velocity saturation and channel length modulation also appears to be incorporated in the model. Fig.2-6 shows the model flow with the various effects included. Resulting accuracy of the model fits against actual measurement data is however not quite clear from [17] and these device- and circuit-level validation steps are critical in gauging any model's usability in circuit design.

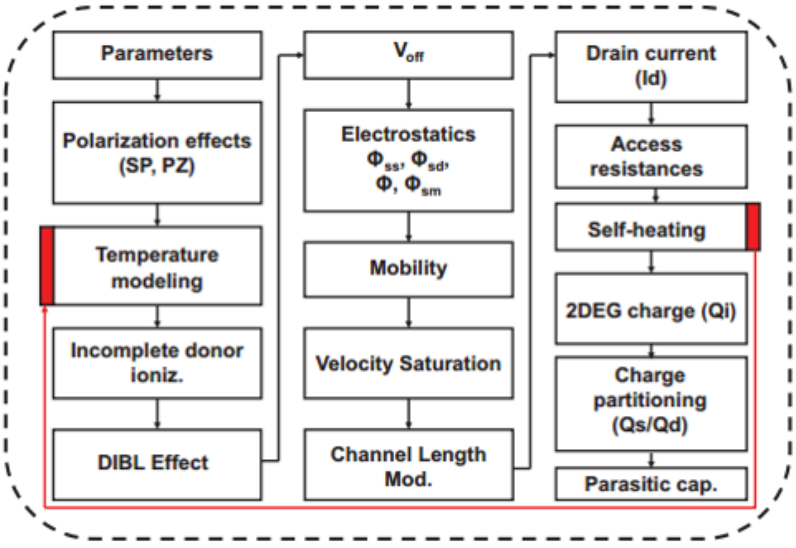


Figure 2-6: The HSP model flow indicating the various effects incorporated in the model [17].

2.3 Features of a standard GaN-HEMT model

The consortium of semiconductor foundries and design houses which selects standard models for different technologies, known as CMC, standardizes compact models for new device-technologies. The past standardization efforts have resulted in models such as BSIM, MEXTRAM, HiCUM, PSP etc. For the GaN standardization efforts which are to be held in 4 phases, the following technical requirements for the model were published [18]:

- The model needs to be physical, with a dependence on geometrical dimensions.
- It needs to accurately model the charges and currents at the terminals for all working modes, including the high-power and sub-threshold regions.
- The charge model needs to be charge based (in contrast to capacitance based) and charge conserving. Charge and current need to be self-consistently derived using the same charge formulation.
- An accurate model for the Schottky gate currents should be included, as well as all physical noise sources.
- The model should pass the Gummel and McAndrew symmetry tests.
- Charges and currents need to be modeled accurately across a wide temperature range, with self-heating enabled using a thermal node.
- The model has to be capable of capturing dynamic trapping effects.
- The model has to feature an accurate representation of the parasitic, bias-dependent resistances and capacitances, taking the true asymmetry of the device into account.
- The model needs to have capability to model field plates, and large periphery or unit gate width scaling for both trapping and mechanical stress effects.

The MIT Virtual Source GaN-HEMT (MVSG) model which is the contribution of this thesis attempts to address the above criteria as will be discussed in subsequent chapters. Since the model is physics-based, most of its parameters have physical meanings with easy extraction procedures. In addition, the current and charge expressions are self-consistently calculated from the same parameters. Unlike empirical models, no separate model equations are necessary for DC, large- or small-signal operation. The number of parameters required by the MVSG model is upto 35 depending on the phenomena that are to be captured as will be shown, which is on the lower-side among the prevalent compact models. The model is geometry scalable and includes self-heating effects. While not enough attention is paid to the access regions in all the GaN-HEMT models that were discussed above, these regions are modeled in detail in the MVSG model since they play an important role in device behavior.

In conclusion, the review of GaN models carried out in this chapter reveals that at the time of this writing all the existing empirical models are lacking, because of both the large number of required non-physical parameters, and failure to capture all the GaN-HEMT behavioral nuances. Some physical models fare better, with substantial behavioral nuances captured accurately but have not yet demonstrated their ability to be of use in circuit and system design. In this context, MVSG could prove to be an attractive candidate for GaN-HEMT compact modeling. In the next chapter, operation-details along with various physical effects in GaN-HEMTs will be discussed followed by the methodology in the MVSG model to capture them.

Chapter 3

GaN-HEMTs: Principle of Operation and Behavioral Nuances

Gallium-Nitride-based high electron mobility transistors (GaN-HEMTs) similar to other HEMTs, are field-effect-transistors having a hetero-junction formed between two or more materials (in this thesis AlGaN and GaN is considered) with different lattice constants. In order to develop compact models for GaN-HEMTs to describe the terminal-current and charge characteristics, it is critical to understand the device-operation under different bias and temperature conditions. This chapter focuses on the device-structure and origins of the charge, followed by the description of carrier flow, origins of gate-current in the device, modeling approach to account for access regions, and field-engineering using field plates. Behavioral nuances associated with the second-order effects specific to GaN such as localized heating, charge-trapping, and substrate-loss are highlighted.

3.1 Origins of the 2DEG charge

GaN-heterostructure is formed between two materials: AlGaN and GaN with different bandgaps that allow the formation of a quantum-well at their interface. Although similar band bending is achieved through inversion in MOSFETs, the key difference of GaN-HEMT-structure is that the two dimensional electron gas (2DEG: the equivalent

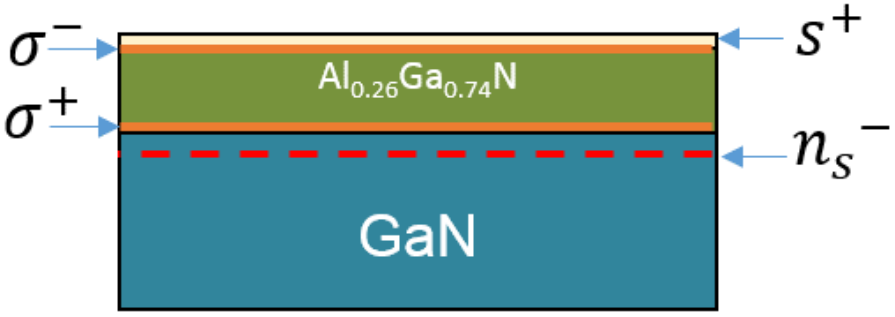


Figure 3-1: Cross-section schematic of GaN-HEMT showing two materials: GaN and AlGaN forming the hetero-structure. Piezoelectric-polarization charges ($\sigma^{+/-}$) present at the top and bottom faces of AlGaN create a built-in electric field that affects band-bending and the threshold-voltage of GaN-HEMTs. Donor-like surface states at the surface (s^+) of AlGaN are mirrored as 2DEG (n_s^-) at the GaN-AlGaN interface in the GaN substrate.

of inversion layer in MOSFET) in the GaN at this interface is formed a gate field or delta-doping the AlGaN. The presence of 2DEG in the absence of external bias condition is a consequence of the heterostructure and makes these devices depletion-mode (normally-on) with negative threshold voltage. A rough schematic of the device hetero-structure is shown in Fig.3-1 which illustrates different charges in the device giving rise to the 2DEG.

The charge density (n_s) in the 2DEG can be increased by adopting other GaN-heterostructures such as InGaN/ InAlGaN and GaN with increased Indium content in the gate-stack, in order to achieve higher current-density which is particularly useful for RF-applications [19]. The MVSG model developed in this thesis is agnostic to the heterostructure details since the parameters affected by it, namely: the areal-gate-capacitance (C_g) and the threshold voltage (V_T) are direct parameters to the model and are not calculated from first-principles. The analysis in the thesis assumes a standard AlGaN/GaN heterostructure which is typically common for both HV- and RF-applications in which the two materials with different lattice constants (GaN: 3.18 Å and AlN: 3.11 Å), electron affinity (χ) (GaN: 4.1 eV and AlN: 0.6 eV) and band gap (E_g) (GaN: 3.4 eV and AlN: 6.2 eV) exhibit formation of a potential well at the interface on the GaN-side where electrons can accumulate resulting

in a two-dimensional electron gas (2DEG) as shown in Fig.3-2. In addition to this effect, the polar nature of the AlGaN/GaN system results in spontaneous polarization and the difference in lattice constants of the two layers results in piezoelectric polarization which creates a further field in the AlGaN layer pushing the device into deep-accumulation at zero bias (hence negative threshold-voltage: V_T). The 2DEG density and V_T in GaN-based HEMTs are strong functions of the (AlGaN) barrier-thickness (d) due to the presence of these charges ($\sigma > 0$) at the interface of the barrier-layer as shown in Fig.3-2(a) and can be observed in the expression for V_T as given by

$$V_T = \phi_B - d\sigma - \Delta E_c - \frac{n_s}{C_g} \tag{3.1}$$

where ϕ_B is the work-function difference between the gate-metal and AlGaN, ΔE_c is the conduction-band offset and C_g is the areal-gate-capacitance. For AlGaN/GaN heterostructure, V_T is negative and the device requires a negative gate electrode voltage to reduce the 2DEG density and modulate the drain to source current (I_{DS}), eventually turning it off.

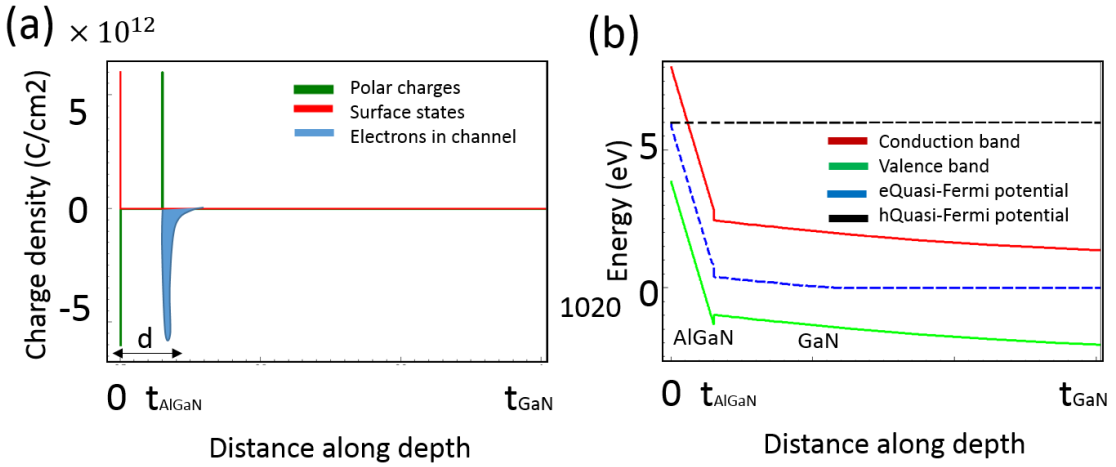


Figure 3-2: (a) The piezoelectric-polarization charges ($\sigma^{+/-}$) , the donor-like surface states at the surface of AlGaN (s^+) which are mirrored as 2DEG (n_s^-) at the GaN-AlGaN interface in GaN substrate are shown as a function of position in a cut-line along the depth of the device. (b) The difference in band gap and electron-affinity of the two materials results in the band-bending shown at a non-zero gate-voltage.

3.2 Device structure

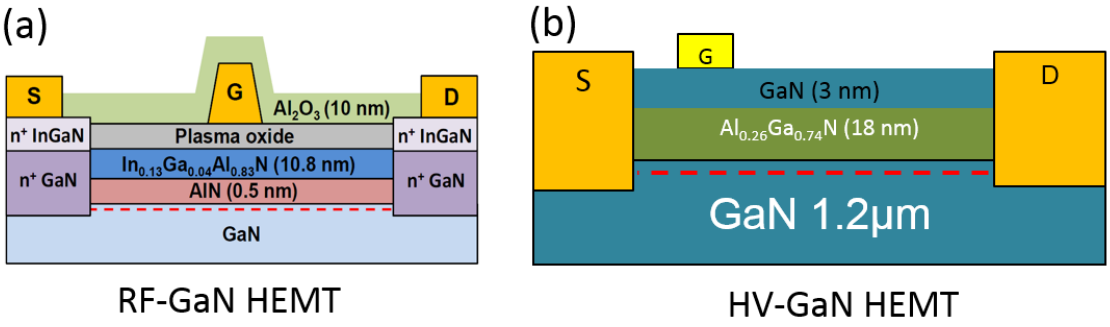


Figure 3-3: (a) RF-GaN-HEMT showing the heterostructure with Indium to increase n_s, access regions and epi-regrown source/drain contacts. AlN back-barrier is also present to reduce short-channel-effects at scaled gate-lengths [19] (b) HV-GaN-HEMT showing asymmetric access regions with longer drain access region to augment BV.

The heterostructure discussed in the previous section is typically grown on semi-insulating substrates such as Si (for power applications to reduce cost), SiC (for high efficiency RF applications) or sapphire (earlier demonstrations of the device) which requires several transition graded layers to keep low dislocation densities in the substrate. The gate metal (Ni/Au) can be deposited on AlGaN directly to form a Schottky gate with its work-function engineered to allow sufficient gate-overdrives without resulting in high gate-currents, or can be separated from the AlGaN layer by oxides (typically Al_2O_3) to reduce gate-leakage in HV-switching. The drain and source contacts are separated from the gate-metal in a non-self-aligned way by access regions (regions between gate and source/drain metal) and these can be engineered to obtain a specific BV and R_{on}. Typical RF- and HV-HEMT structure schematics are shown in Fig.3-3 highlighting the intrinsic transistor region under the gate-metal and the source- and drain-access regions next to the gate and source/drain contacts. The application of drain-to-source voltage controls the current flow exactly as in a MOSFET. In addition to the simple structure described here, additional complexities such as field plates are added especially in HV-applications to augment BV that is part of the discussion in the subsequent sections of this chapter. Fabricating enhancement-mode devices (positive V_T) is also an active research topic with several flavors such as

recessed gate, p-GaN and fluorine-treatment proposed to achieve it [20] which does not impact the modeling approach other than changes to model parameter values such as threshold voltage (V_T) and gate-capacitance (C_g). The transport of carriers in the 2DEG under lateral field is the topic of discussion in the next section.

3.3 Carrier transport in 2DEG channel

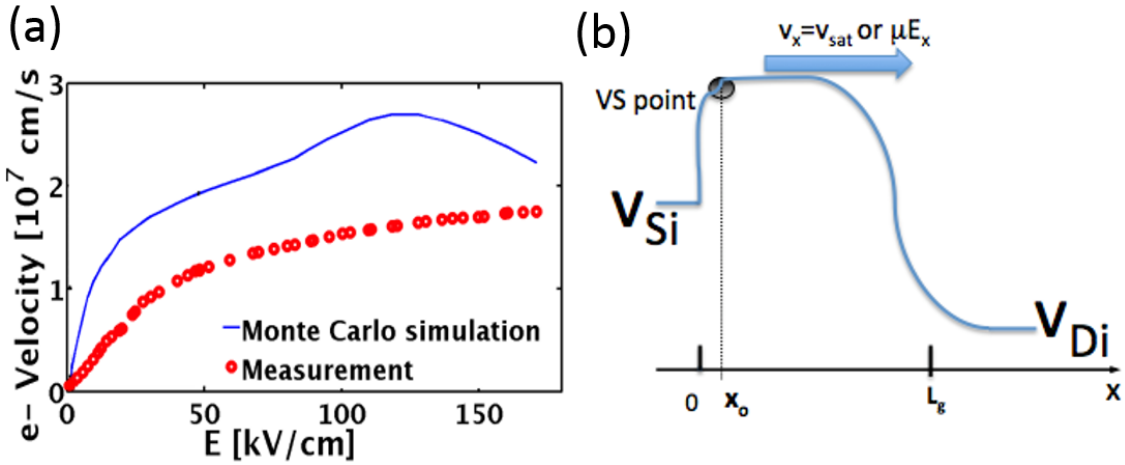


Figure 3-4: (a)Velocity-field profile from MC simulations in GaN-HEMTs [21] showing non-monotonicity at fields of 100 KV/cm which appears to be absent in the extracted velocity profile from device measurements [22]. (b) The band-profile along the channel under $V_{DS} > 0$ consistent with which the drift-diffusion equation must be solved for terminal-current-evaluation.

The transport of carriers in the 2DEG in above-threshold-condition is similar to that in the inversion layer of a MOSFET with the lateral field due to V_{DS} controlling the current at low-fields and carrier-saturation occurring at high lateral field either due to pinch-off or velocity-saturation. The carrier-velocity profile vs. field in GaN-HEMTs is reported widely to be non-monotonic exhibiting a 'hump and dip' characteristic with peak-velocity of 3×10^7 cm/s at 160 KV/cm from Monte-Carlo simulations shown in Fig.3-4(a) followed by true-saturation to 1×10^7 cm/s at a high-saturation-field of 250 KV/cm. Inter-valley scattering and non-quasi-static transport are some of the reasons given for this phenomenon [21]. However the extracted velocity-field relationship from measurements is often found to be monotonic as shown in Fig.3-

4(a) [22] and the MVSG formulation uses this simple velocity-saturation model for carrier transport in 2DEG to achieve a closed-form expression for current. The saturation velocity in the model is a fitting parameter and whose value lies in between the peak-velocity and saturation velocity of MC simulations. The non-monotonic effect is probable only in highly scaled-gate-length devices because of which the error between the assumed and actual profile in the low-field region of interest is quite small for practical gate-length regimes in the order of a few hundred nanometers or above for RF- and HV-device-modeling for circuit-applications. Moreover, even in very short-length scales for high-frequency-RF (THz) applications, the bias conditions are low enough, with fields below 160 KV/cm, that ensures that the device operates in below non-monotonic regime.

Solving drift-diffusion transport problem by assuming the measured velocity-field profile enables us to compute terminal-current expressions using a similar approach as in conventional MOSFETs. The band-profile along the channel assumed for this calculation is as seen in Fig.3-4(b) with the model solving for the injection velocity at the source-side using current-continuity along with gradual-channel-approximation (GCA). Transport in GaN-HEMTs is mostly diffusive even at highly scaled gate-lengths, suitable for very-high-frequency (VHF) RF-applications, because the gate length is much longer compared to the mean free path of electrons in GaN which is reported to be about 0.5 nm making ballistic carrier-transport less relevant for realistic devices of commercial interest. The saturation mechanism changes from pinch-off for longer gate-length devices used in HV-applications to saturated-velocity-limited transport in shorter gate-lengths used in RF-applications and the model has to account for the scalability of current spanning both regimes.

3.4 Bias-dependent channel charges

Channel-charges in GaN-HEMTs account for a significant portion of total terminal-charges and hence terminal-capacitances which impact the switching performance of these devices. The modulation of the 2DEG-channel due to both gate- and drain-

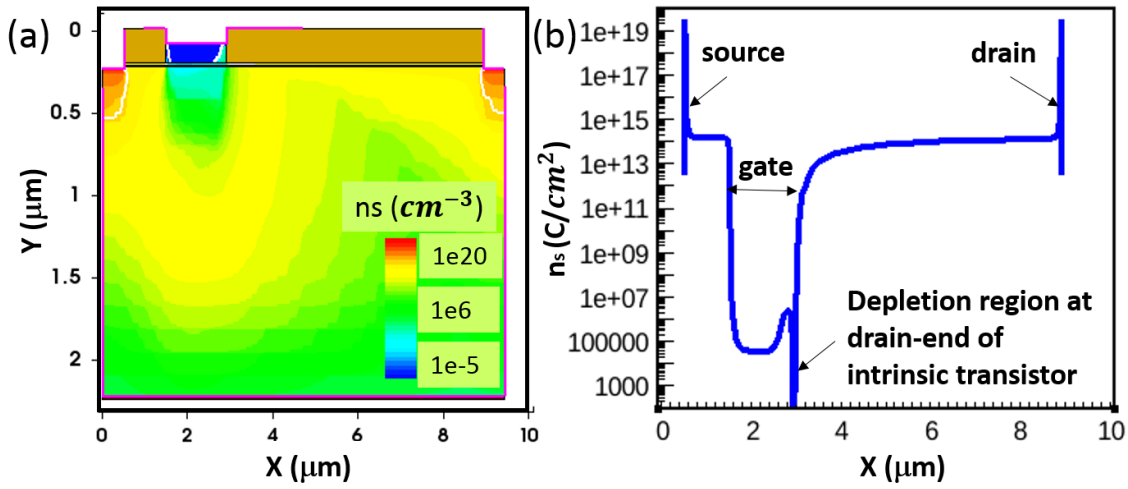


Figure 3-5: (a) Cross-section schematic of typical HV-GaN-HEMTs in saturation regime simulated in Sentaurus TCAD software. The electron density in the device is shown indicating non-uniform charge distribution (b) The lateral-charge profile (n_s) along the channel is shown, indicating different regions in the device of interest to compact modeling in order to capture non-linear channel charges.

bias is reflected in non-linear terminal capacitances which can vary widely from off-to-on state of the device-operation. Even in the on-state saturation-regime with $V_{DS} > 0$, the charge distribution along the channel is non-uniform as shown in Fig.3-5(b) in TCAD simulations of a typical HV-GaN-HEMT whose cross-section schematic is shown in Fig.3-5(a) under on-state-saturation. The channel charge under the gate is lower than in the access-regions indicating depletion-mode operation and reduces in the channel from the source- to the drain-end of the gate. In addition, depletion region is formed under the gate towards the drain-end with very low charge density and high-lateral field. The non-uniform charge is partitioned between source- and drain-terminals in MVSG model to accurately model the non-linear bias-dependent terminal charges.

Some of the key device-capacitance metrics of importance to HV-switching application regimes are the total input-capacitance (C_{iss}), output-capacitance (C_{oss}) and the reverse-transfer capacitance (C_{rss}) which are shown for a typical commercial HV-GaN-HEMT in Fig.3-6(a) in off-state. In a typical HV-converter (e.g. for automotive applications,) C_{iss} of GaN-HEMTs loads the gate-driver, C_{oss} and C_{rss} control the slew-rates of output switch-node and hence switching power losses and

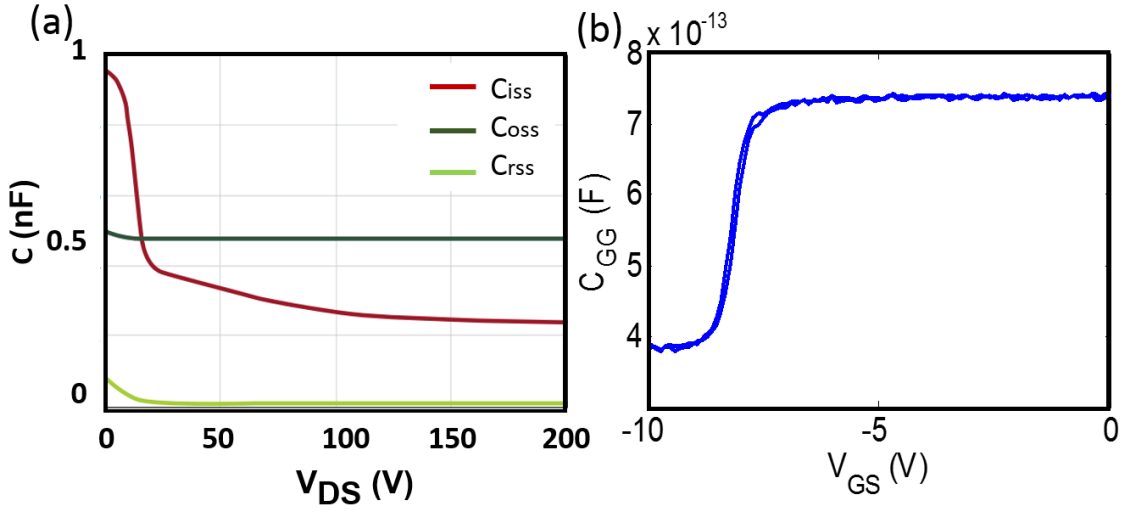


Figure 3-6: (a) Input-, output- and reverse transfer-capacitances in a commercial HV-GaN-HEMT in off-state (EPC2010 form EPC) (b) Gate-capacitance as a function of V_{GS} showing the transition of the capacitance from low-value in off-state to high-value in on-state at the V_T of the device due to the creation of 2DEG at $V_{GS} = V_T$.

will be explained in detail in chapter 5. Another significant contributor to the channel charge is the gate-voltage which controls the on-or-off-state of the device and results in significant increase in the gate-capacitance at threshold-voltage as shown in Fig.3-6(b). The discussion on non-linear capacitances in this section has important implications for large-signal RF-circuit design using GaN-HEMTs as it affects the maximum unity-power-gain frequency, transit-frequency, gain-compression, and linearity of GaN-HEMTs used in power amplifiers. The methodology to capture the channel-capacitances in MVSG model is to self-consistently compute them along with device-currents by employing charge-partitioning functions and will be discussed in detail in the next chapter. The model can also capture the fringing capacitances and constant metal-to-metal parasitic capacitances along with channel-charges associated with field plates which is the topic of discussion in the subsequent sections.

3.5 Gate current in GaN-HEMTs

Gate-currents in GaN-HEMTs are usually dominant in devices without a gate-oxide wherein the gate-metal forms a Schottky-contact with the channel; in this case

forward-biasing the gate-source and gate-drain junctions can increase the gate-currents exponentially due to the turn-on of the diodes. Schottky-gated devices therefore have a limitation on the maximum gate-overdrive voltage that can be sustained by the device without significantly affecting the device amplification performance. In addition to increased gate-current and input power loss associated with gate-currents, pumping charges into the hetero-structure degrades the device-reliability and leads to threshold-voltage drifts. Schottky-gated devices are common for RF-GaN-HEMTs since moderate gate-leakage is tolerable for power-amplification and absence of gate-oxide increases the areal-gate-capacitance (C_g) and hence increases charge-density (n_s) and drain-current (I_d) control by the gate voltage (e.g. transconductance). However gate-oxides (typically Al_2O_3) are often employed in HV-GaN-HEMTs since these applications cannot afford to have gate-leakage currents in wide-peripheral devices which can be significant enough to degrade the efficiency of converters under high operating voltages. Even in such devices there are several reports of charge pumping in oxides due to Poole-Frenkel effect resulting in non-zero gate-currents, but this is not part of the modeling work included in this thesis [23].

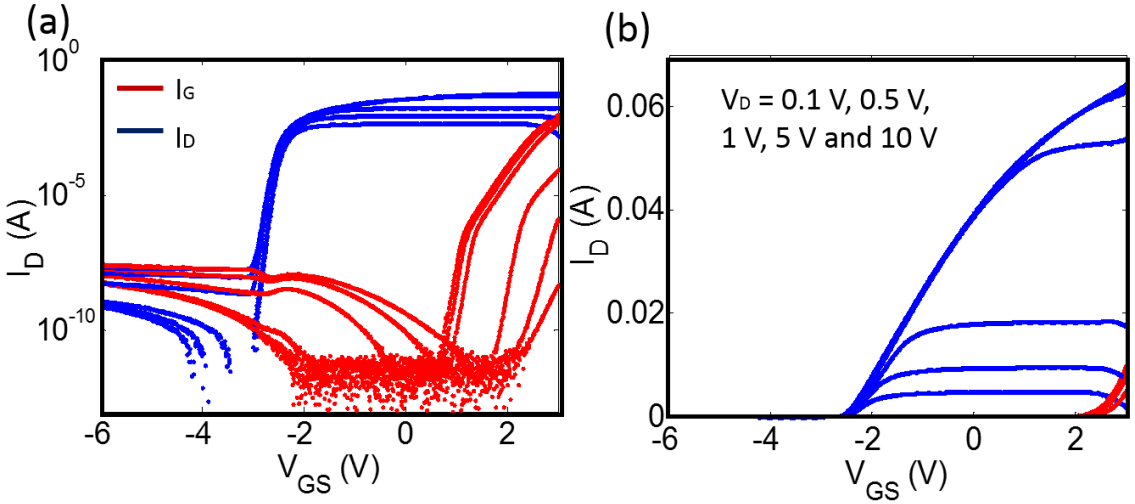


Figure 3-7: (a) The drain-currents (I_D) and gate-currents (I_G) of a Schottky-gated GaN-HEMT showing that the off-state leakage floor is predominantly leakage from drain-to-gate terminal with current flowing into drain-port and out from gate-port (b) The linear-scale plot of the transfer curves show the gate-current rising at high gate-overdrive voltage due to gate-Schottky-diode turn-on.

The significance of gate-current (I_G) relative to drain-current (I_D) can be observed from the measured transfer characteristics in Fig.3-7 where the characteristics are shown in logarithmic and linear scales. In the log-scale transfer curves, it becomes evident that the off-state leakage floor is dominated by drain-to-gate leakage that forms the gate-current out of the gate-terminal of the device. This current is contributed from recombination-components, surface-leakage, and gate-induced-drain-lowering (GIDL) along with the reverse-saturation Schottky-diode current and has unintended consequences in high-power-amplifiers where at high input-power (when the signal swings well into the off-regime with high drain-to-source voltages) a significant portion of the output power flows out of the input-port affecting the power-added-efficiency of the amplifier. In the high gate-bias regime, the turn-on of the gate-current can also be seen causing the reduction of drain current since the gate-current flowing from gate-to-source and gate-to-drain subtracts from the drain-to-source channel current at the drain-port. Modeling of gate-currents in MVSG model is carried out by employing two Schottky-diodes between gate-source and gate-drain terminals and will be explained in the next chapter.

3.6 Access regions: Charge depletion and non-linear behavior

GaN-HEMTs are not self-aligned devices because of process constraints (gate-last process is typically employed with E-beam lithography for defining the gate-line) and gate-leakage constraints (since gate-oxide is absent in Schottky-gated devices, source/drain contacts cannot overlap under the gate-metal); in the fabrication technology for RF-devices and in HV-devices these are intentional features to sustain high reverse voltages. The source and drain access regions are un-gated and are usually passivated as shown in Fig.3-3 without a gate-equivalent electrode present to modulate the 2DEG charge underneath. This would lead us to assume that the regions behave as ideal resistors whose resistivity is determined by the 2DEG sheet charge but

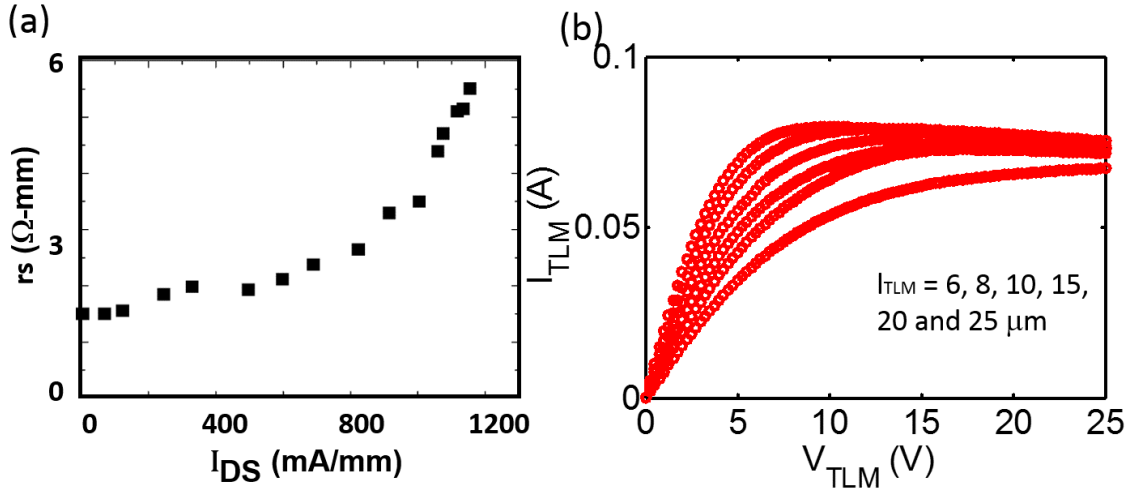


Figure 3-8: (a) Drain-current dependence of source resistance showing the increase of access regions in saturation conditions due to current-saturation in these regions [22] (b) Current-voltage characteristics of transmission-line-method (TLM) structures of different lengths exhibiting non-linear behavior with the saturation of currents at high-fields.

this is in contradiction to experimentally extracted source access resistances which show an increase in the resistance value with drain current as shown in [22] and reproduced in Fig.3-8(a).

In order to study the cause for the non-linear behavior of access regions, transmission-line-method (TLM) structures which are gateless resistors formed by 2DEG between two ohmic contacts are measured and the resulting IV-characteristics for different-length-TLMs are shown in Fig.3-8(b). The TLMs behave as ideal resistors which scale with channel length at low voltages but undergo saturation at high voltages as shown in the figure. The current-saturation is caused by a combination of device-self-heating, charge-depletion towards the drain-terminal and velocity-saturation of carriers. TCAD simulation of a typical TLM is shown in Fig.3-9 which shows the spatial variation in electron-density in the device along with band-bending along the channel showing voltage and field distribution similar to gated-FETs as in Fig.3-4. As in gated-FETs, pinch-off in longer-length TLMs and velocity-saturation in short-channel TLMs are responsible for the current-saturation as is evident from the measurements in Fig.3-8(b). This gating-effect even in intentionally gateless-resistive

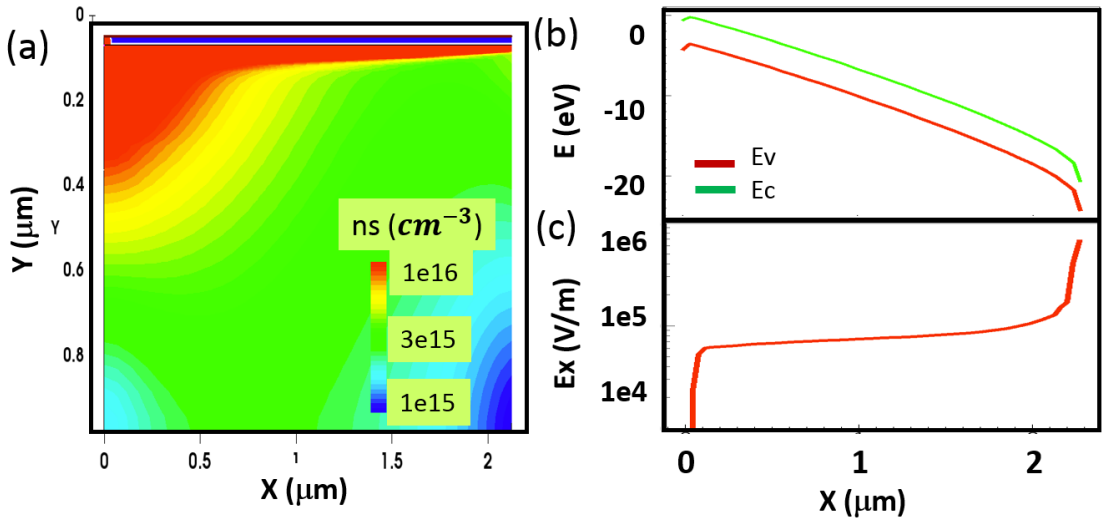


Figure 3-9: (a) Cross-section schematic of TLM structure simulated in Sentaurus-TCAD under a high-lateral field that shows the non-uniformity in channel-charge with reduced concentration towards the drain-end similar to regular-FET in saturation (b) The band-diagram of the TLM showing the band bending with uniform field in most of the channel but peaking at the drain-end (c) The lateral- electric field showing the field peaking at the drain-end due to pinch-off in the structures under high-field.

regions in GaN-technology could be due to surface trap-states, and higher-level metals and so these regions should be modeled as implicit-gate transistors using the MVSG model. Since it is difficult to determine a location for the implicit-gate, the areal implicit-gate-capacitance for the implicit-gate access regions (C_{Ig}) is a fitting parameter in the MVSG model and the value of the overdrive-voltage is linked to the 2DEG sheet charge density in the access regions as will be derived in the next chapter.

Access-region non-linearity is primarily responsible for quasi-saturation of GaN-HEMT currents at high gate-voltages where the terminal-currents are limited by carrier transport in access regions. This imposes an upper-limit on the on-current that can be extracted from a GaN-HEMT and has significant contribution to large-signal compression characteristics and linearity performance of certain classes of GaN-power amplifiers. Charge-depletion in access regions saturates the maximum voltage drop along the gated-region of the channel and it redistributes the field in the device thereby augmenting the BV in HV-applications. A detailed modeling methodology to capture the physics of carrier transport in the access regions of GaN-HEMTs is

described in the next chapter and another approach for field-engineering via field-plates is discussed in next section.

3.7 Field-plated regions: Non-linear charges and carrier-transport

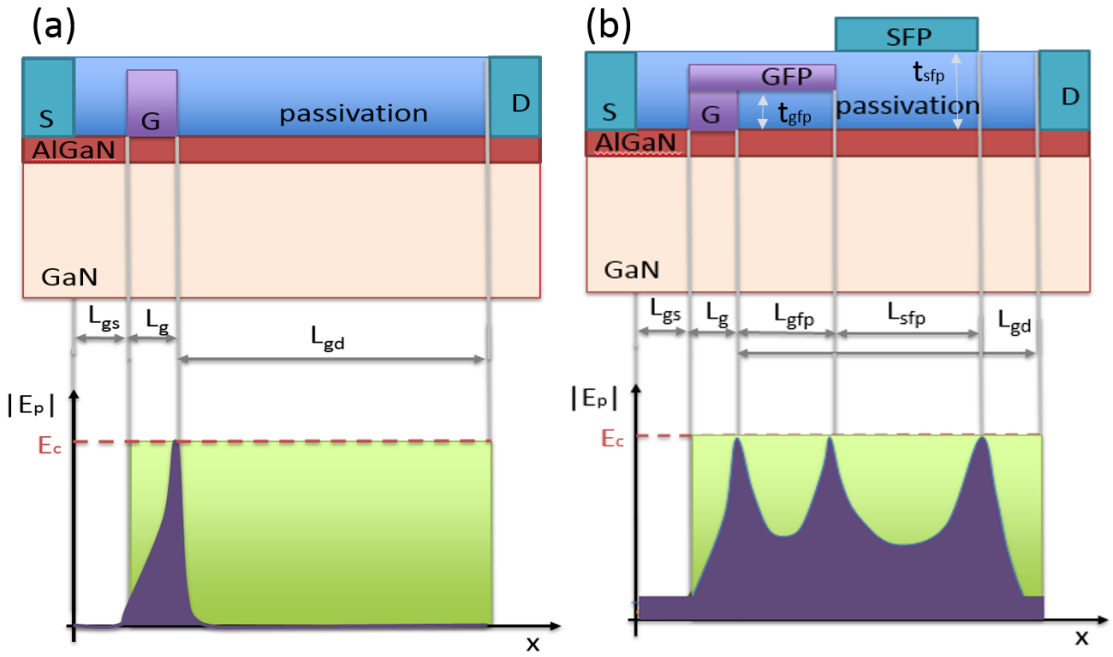


Figure 3-10: (a) Cross-section schematic of non-field plated device is shown along with the lateral electric-field strength along the channel from source-to-drain at breakdown drain-source voltage (BV) in off-state. As the voltage is the integral of the filed (blue area) it can be seen that only the gate area contributes to BV when the critical filed, (E_c), is reached. (b) A device field-plates (FP) where both gate-FP (GFP) and source-FP (SFP) cause additional field-distribution in the channel at the drain-side edge of each field-plate enhancing the area under the field profile and hence the BV.

Field-plates (FP) are secondary, weakly-gated regions of the transistor which along with the access-regions are designed to engineer the electric field and augment the breakdown-voltage of the device. Typically employed in HV-GaN-HEMTs they come in two variants: gate-connected FPs and source-connected FPs named on the electrical connection to the gate-terminal. The operational advantage of these regions is

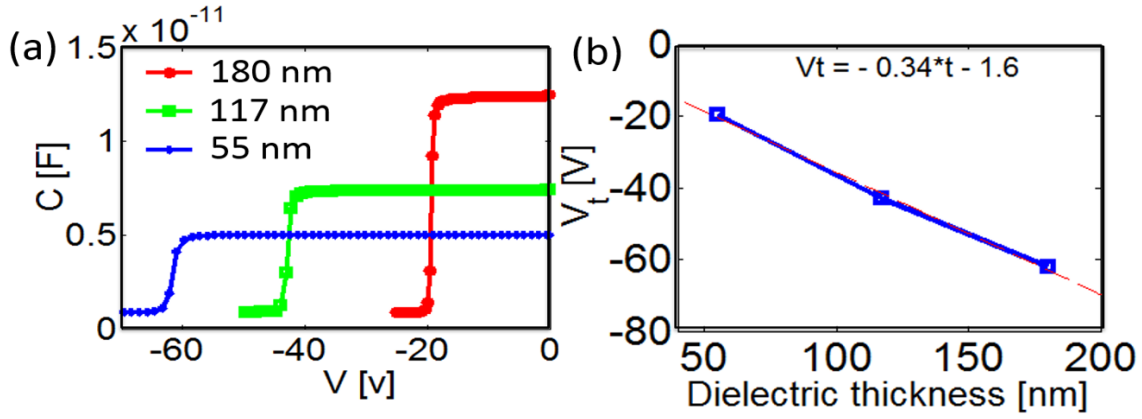


Figure 3-11: (a) CV measurements of fabricated CV structures between FP-metal and 2DEG-channel shows that the on-state capacitance value and voltage, $V_{T,fp}$, decrease with FP-dielectric thickness (t_{fp}) and (b) the $V_{T,fp}$ dependence on t_{fp} is linear. The relation can then be input as parameter to MVSG model to model the FP-regions as FETs. [CV-structures fabricated by Daniel Piedra, MIT]

explained with the sketch in Fig.3-10 which also shows the cross-section schematic of HV-GaN-HEMT with and without FPs in (a) and (b) respectively. The presence of FP-transistor-regions augment the BV by spreading the electric-field over longer lengths. Ideally the desired field-profile to maximize the BV for a given length is rectangular with field everywhere equal to the critical-breakdown field ($E_c = 3\ MV/cm$) as shown by the green-background region in the field profiles of the figure. In reality due to the limitation on the number and the minimum-length of the FPs, the resulting field-profile is as shown in Fig. 3-10(b). The lengths of FP-regions (L_{sfp} and L_{gfp} in the figure) along with their gate-capacitances or equivalently, dielectric-thicknesses (t_{sfp} and t_{gfp}) of FPs, for given dielectric permitivity, are design-parameters which are usually optimized to get the desired BV for a given gate-length (L_g) and drain-gate spacing (L_{gd}).

The field-plated regions are modeled as additional transistor elements in series with the intrinsic-gated FET in the MVSG model with the dielectric thicknesses, t_{gfp} and t_{sfp}, determining the areal-gate-capacitances and threshold voltages of the FP-transistors. By fabricating field-plated capacitance structures we can obtain the variation of $C_{g,fp}$ and $V_{T,fp}$ with dielectric-thickness (t_{fp}) as shown in Fig.3-11(a). As can be seen, $V_{T,fp}$ and $C_{g,fp}$ decrease with increasing t_{fp} and $V_{T,fp}$ decreases linearly

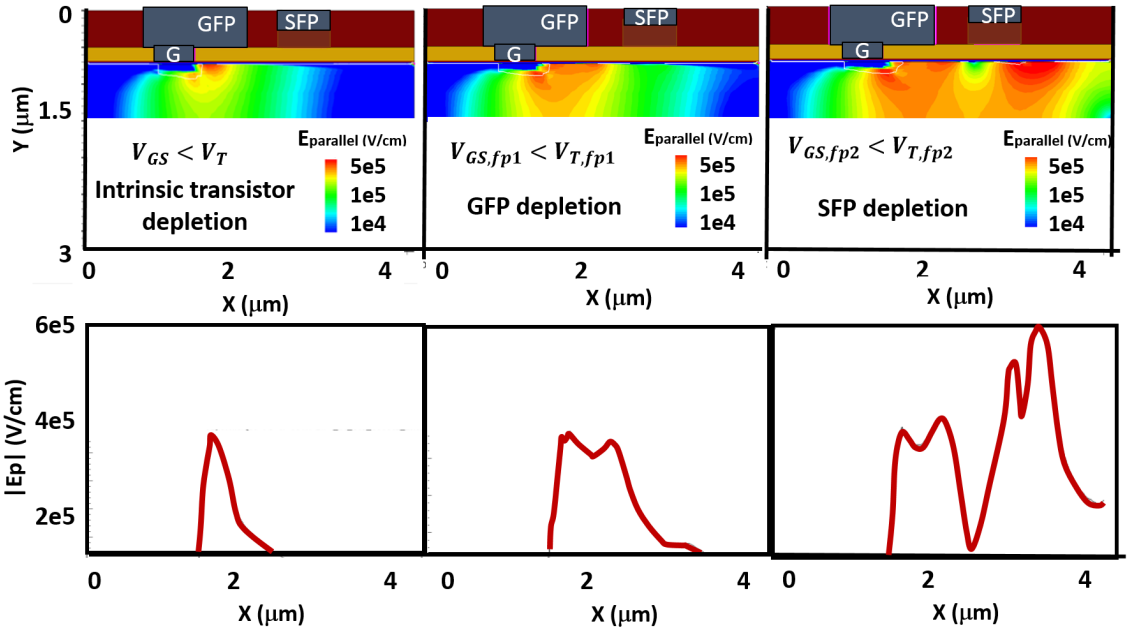


Figure 3-12: (a) Cross-section schematic of field-plated device simulated in Sentaurus TCAD is shown along with the lateral electric-field-strength (E_P) along the channel from source-to-drain as V_D is ramped up in off-state. The first-peak in E_P can be seen at the drain-edge of intrinsic-gate when $V_{GS} < V_T$. (b) When V_D is ramped further, a second-peak in E_P at the GFP-edge once $V_{GS,fp1} < V_{T,fp1}$ (c) A third-peak is formed in E_P at the SFP-edge when $V_{GS,fp2} < V_{T,fp2}$ resulting in a broader field-distribution and enhanced BV.

with t_{fp} observable from Fig.3-11(b) from the measured CV characteristics of ring-capacitors wherein one metal is the field-plate and the other is the 2DEG. Since the FP-metals are at an increasing distance from the 2DEG, as we progress from gate-towards-drain, the successive $V_{T,fp}$ increase in magnitude in this direction.

As drain voltage (V_D) applied to the device in off-state is increased, the peak-field at the drain-edge of intrinsic gate-metal rises and reaches the critical-field (E_c) in the absence of FP causing device-breakdown. However in the presence of FPs as shown in Fig.3-10(b) ramping V_D initially results in the rise of peak-field in the intrinsic-gated region but it soon saturates in value as a second peak is formed at the drain-edge of the first FP when its gate-to-source voltage $V_{GS,fp1}$ goes below its threshold voltage $V_{T,fp}$. Gate-to-source voltage (V_{GS}) of each FP-FET relative to its $V_{T,fp}$ determines the onset of turn-off and depletion-formation (or peak-field-profile in the FP). This happens as the intrinsic-drain-voltage of the intrinsic-gated FET

which is also the intrinsic-source-voltage of the first-FP rises with applied V_D until $V_{GS,fp1} < V_{T,fp1}$. This second-peak rises until the intrinsic-drain of FP1 (which is also the intrinsic-source of FP2) rises to a value such that $V_{GS,fp2} < V_{T,fp2}$. Thus the FPs undergo progressive 'domino-depletion' as V_D is increased such that the field-profile is now more spread-out enhancing the BV. The exact simulations of this phenomenon can be understood with the help of TCAD simulations of a HV-device with a gate- and source-connected FP as shown in Fig.3-12. As the channel underneath the FPs deplete at different V_{DS} in the off-state, the corresponding capacitance between gate-metal and channel of the FP (gate-to-channel capacitance C_{gc} for GFP and source-to-channel capacitance C_{sc} for SFP) exhibit a drop in value at each transition, similar to those seen in the capacitance plots of Fig.3-6(a). The sub-circuit approach taken in MVSG model to capture the charge-depletion and carrier transport in FP-regions is explained in more detail in the next chapter.

3.8 Thermal behavior of GaN-HEMTs

GaN-HEMTs with their high-voltage and current-density together with small-form factor result in very high power-density in the device. The generated heat is dissipated through the substrate which consists of several transition layers with high thermal resistance (dominated by boundary resistance between layers) causing significant temperature rise in the device [24]. The problem of self-heating and high-localized heating in the device is a severe issue that affects the device-reliability, degrades the terminal output-current and gain characteristics, affects the RF-performance and lowers the BV and switching-performance of HV-GaN-HEMTs. The temperature map in a gateless-TLM structures is shown in Fig.3-13 using thermoreflectance thermography by Banafsheh et. al., for 1 W power-dissipation and clearly illustrates that channel temperature as large as 110 $^{\circ}C$ can arise in room temperature operation. The power dissipation in TLMs is non-uniform with higher temperatures towards the drain contact due to the high-field, and hence highest power density at the pinch-off region near the drain as a result of channel pinch-off in these structures.

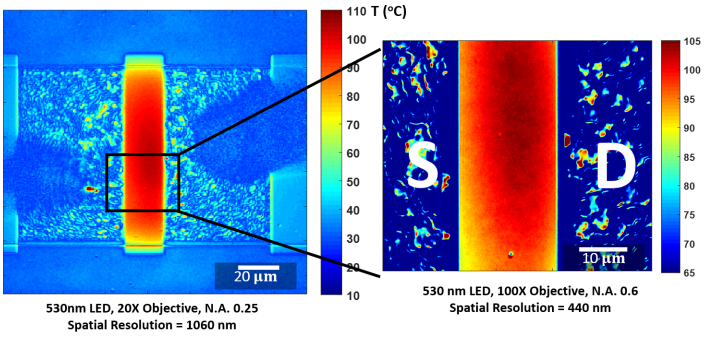


Figure 3-13: Thermoreflectance measurements using CCD technique showing the temperature rise and non-uniform heat-generation in ungated 20 μm TLM structure under 1 W power. The high temperature in this device, which is built in GaN-on-Si substrate is a consequence of high power-density and thermal conductance. [Thermoreflectance measurements by Dr. Banafsheh Barabadi, MIT]

The same observation can be extended to gated-HEMTs as seen in Fig.3-14 where high temperature due to device-self-heating can be seen both in devices fabricated at MIT and in industry in Fig.3-14 (a), (b), respectively. Wide-peripheral devices typically used in HV-low-R_{on}-devices or multi-finger RF-devices generate considerable power and thermal-coupling between different fingers results in non-uniform heating.

The degradation of electrical characteristics in the device due to temperature is attributed to transport parameters such as carrier mobility ($\mu(T)$) and carrier-saturation-velocity ($v_{sat}(T)$) due to increased phonon-scattering at elevated temperatures and results in reduced on-currents and higher R_{on} in I-Vs at 150 $°C$ compared to RT I-Vs as seen from Fig.3-15. Another key signature of elevated device-temperature

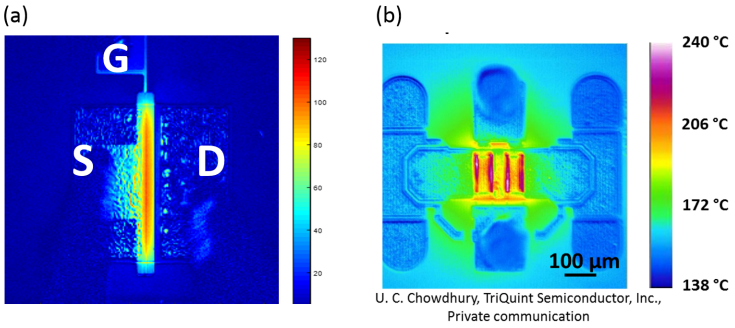


Figure 3-14: (a) Thermoreflectance measurement of single-finger GaN-on-Si HEMT showing temperature rise of 110 $°C$. (b) Multi-finger RF-devices from industry show much higher extent of heating with temperatures reaching 250 $°C$.

is the droop in the output-characteristics and negative output-conductance at high currents. Electrostatic parameters such as V_T and SS change with temperature which is reflected in the MVSG model as will be shown in next chapter. The approach taken to model self-heating is to compute the power-dissipation and a thermal resistance (R_{th}) is used to calculate the resulting temperature-rise which is fed-back into the electrical equations in the temperature-dependent part of transport parameters. Changes in operating temperatures in addition to self-heating are also accounted for using this approach. Furthermore transient temperature effects under switching conditions as a result of finite thermal time-constant are included using a thermal capacitance (C_{th}) along with R_{th} with different values, and hence time constants, depending on substrate material.

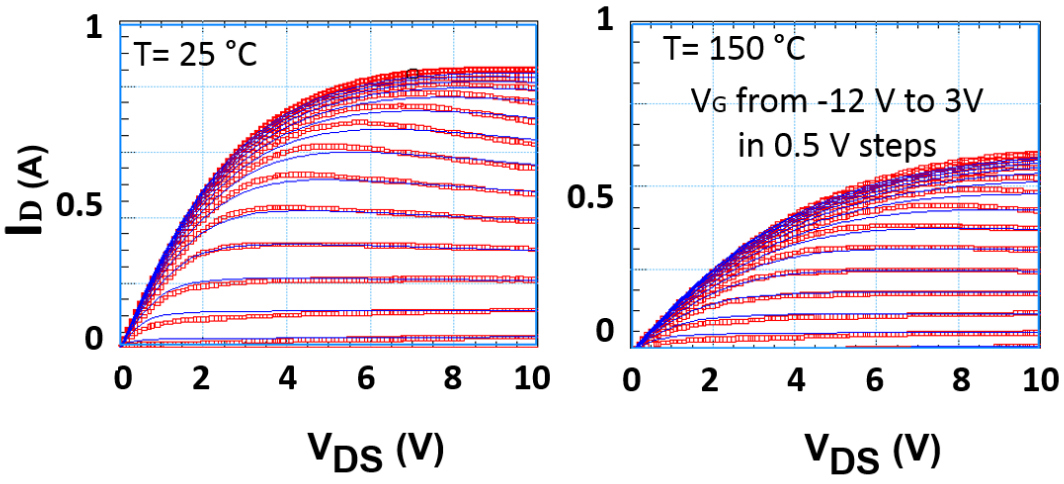


Figure 3-15: Comparison of output characteristics of wide-periphery industry-devices at RT and 150 $°C$ shows significant degradation in electrical-characteristics at elevated temperatures.

3.9 Device-level parasitics and RF-device behavior

The discussion on operating-principles of GaN-HEMTs so far is related to the performance of core-device suitable for DC and low-frequencies but at high-RF-frequency-range the performance of the device is affected by parasitic-elements associated with the device described in this section. The connection of GaN-HEMTs to the environ-

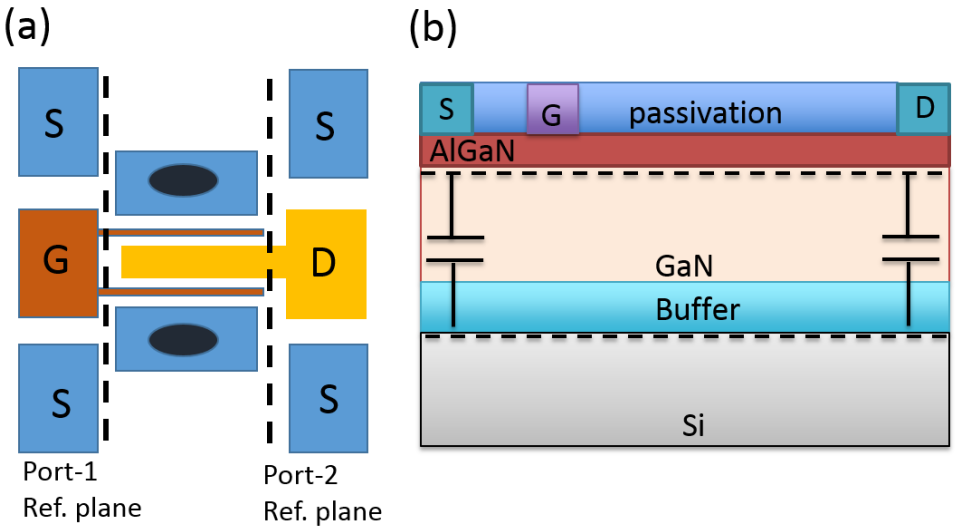


Figure 3-16: (a) Typical layout of a 2-finger RF-device showing the gate-input-port and drain-output-port along with the reference planes upto the gate-lines for small- and large-signal characterization. De-embedding structures are necessary to reach-upto the reference-planes exterminating the effect of pads and leads of the device. (b) In addition to the device-level-parasitics associated with the terminals, GaN-HEMTs have an additional parallel-RF-loss path between source and drain via the substrate.

ment is through terminal connections which introduce their own parasitic RLC elements. Terminal-leads introduce parasitic resistances and inductances, while terminal-pads contribute to parasitic pad-capacitances. The terminal-parasitics associated with the gate cause the amplitude and phase of input V_{GS} signal to change along the gate-line while pad-capacitances cause parallel signal-leakage path. To characterize the core-device restricted to the gate-line using the MVSG model, the effect of terminal connections is de-embedded using open- and short-structures such that the input- and output-reference planes are as shown in Fig.3-16(a) in a typical layout of the RF-device.

Along with the terminal-parasitic elements an additional parasitic network associated with the RF-device is the substrate-loss-network. GaN-HEMTs typically grown on Si- or SiC-substrates result in a parallel high-electron density channel in the substrate-transition layer-interface. The buried-channel in the substrate has lower charge-density in SiC (due to its larger bandgap and higher resistivity) compared

to Si but nonetheless results in non-negligible resistance which is coupled to the source and drain terminals via substrate capacitances as shown in Fig.3-16(b). At RF-frequencies, the parallel-loss network considerably lowers the transistor-gain and efficiency for power-amplification and it is included in the MVSG model.

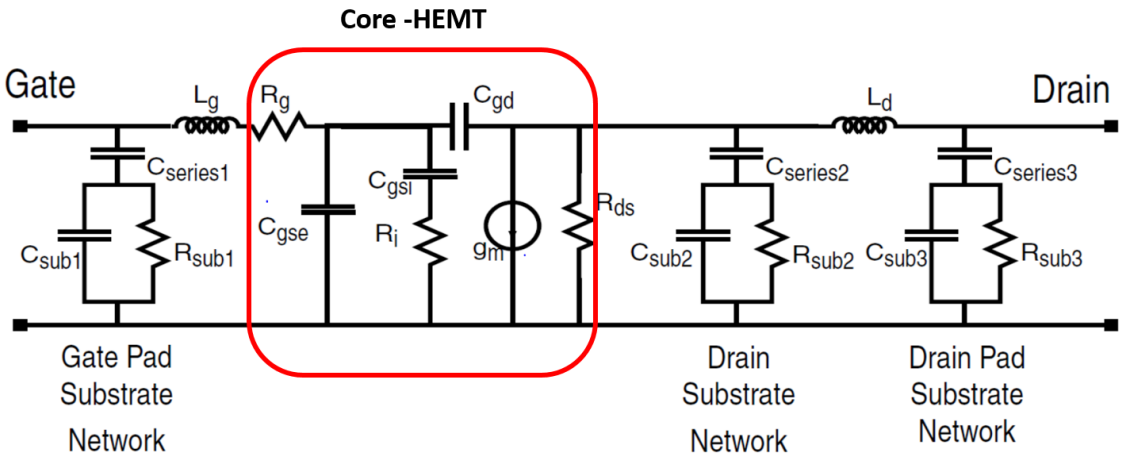


Figure 3-17: Equivalent small-signal equivalent sub-circuit (before de-embedding that includes pads and leads) of a typical RF-device indicating various device-parasitic network [25].

The equivalent-sub-circuit of the device suitable for RF-applications is shown in Fig.3-17 which includes both terminal- and substrate-parasitics [25]. The core-transistor model is a large-signal transistor model that captures the device-transport and charge distributions as a function of bias and temperature while the parasitic-network surrounding the core-model are bias-independent RLC elements that can be extracted from S-parameter measurements as will be described in subsequent chapters. For close to THz-range applications this lumped equivalent-circuit-model might not suffice and each finger of a multi-finger device or even a single-finger of the device may have to be modeled as a network of transistor elements in a distributed manner.

3.10 Noise performance of GaN-HEMTs

GaN-HEMTs similar to any FET are inherently noisy devices and amplifiers built using these devices not only amplify the input-signal and noise but also add intrinsic

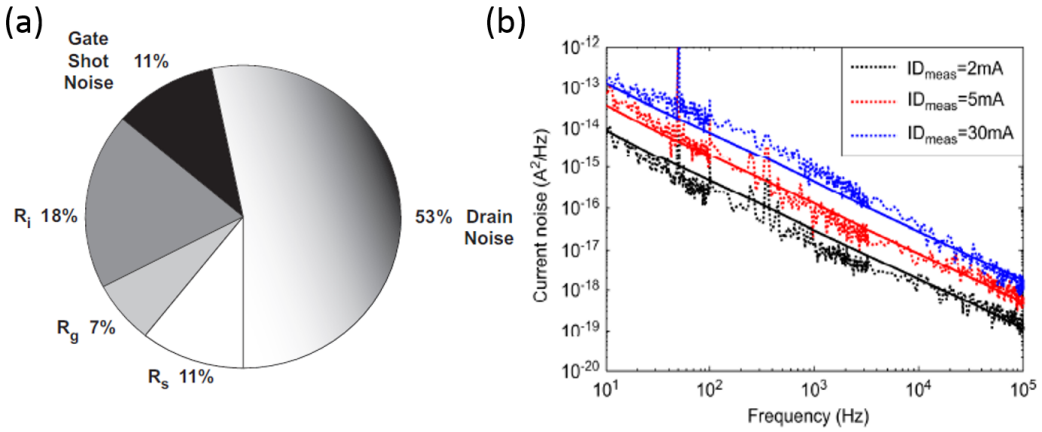


Figure 3-18: (a) The contributions of different noise source in the GaN-HEMT to the noise-figure [26] (b) Phase noise characteristics of a GaN-VCO as a function of drain current level as given in [27].

device-noise to the output signal. This makes the signal-to-noise ratio (SNR) at the output lower than the input SNR and is quantified by the metric of noise-figure (NF) defined as the ratio of input to output SNR. In this context, RF- and low-frequency noise-modeling is critical for the design of receiver-side components such as low-noise-amplifiers (LNAs) and voltage-controlled-oscillators (VCOs) since the input signal at the receiver-side usually has low SNR to begin with. The noise contributors of the device are mainly RF-noise sources associated with thermal- and shot-noise sources in the device with the extent of their contributions on noise-figure illustrated in Fig.3-19(a). Channel-thermal-noise, labeled $Drain-noise$, which is associated with carrier transport through the device and is essentially a voltage-controlled current source, is the biggest contributor to the device-noise. Since most of the RF-GaN-HEMTs are Schottky-gated devices with finite gate-current, the shot-noise associated with carrier transport over a barrier is another key contributor to device-noise. The rest of the sources are thermal-resistor noise sources associated with different resistive elements of the device. The noise-figure from the device due to the aforementioned sources can be simulated and compared against the noise-figure measurements where the load-impedance is fixed and the source-impedance is swept to obtain minimum noise-figure, source-side reflection-point (Γ) and associated-gain corresponding to the minimum noise-figure.

This thesis work also includes a model for phase-noise which is important to account for jitter and phase-noise of VCOs on the receiver-end. Typical phase-noise characteristics in GaN show $1/f^3$ noise behavior before hitting the white noise floor as given in Fig.3-19(b), which is the bandwidth-upconverted flicker-noise of the device. Trap defect states in the channel of the device that cause carrier trapping/detrapping are considered to be the primary flicker-noise sources whose noise-spectrum is inversely proportional to the frequency. Phase-noise is the reason for the frequency skirts in the output-spectrum of VCOs in the receiver stage and it causes signal spill-over to adjacent channels thus imposing restrictions on minimum bandwidth of communication channels. The MVSG model formulation to account for various device-noise phenomena is described in the following chapters along with demonstration of model accuracy to capture noise-performance of receiver components built using GaN platform.

3.11 Origins and implication of charge trapping and *knee-walkout*

Dynamic charge-trapping, current collapse or knee-walk-out is a much discussed non-ideality of GaN-HEMTs [28], [29], [30] which has impact on the device-behavior under large-voltage switching conditions. Simply put, current collapse is the increase in on-resistance and reduction in on-current during pulsed switching conditions. The effect is severe when the gate is biased to large negative voltages in the off-state ($V_G < V_T$) and the drain is biased to large positive voltages before switching to the on-state in time scales ranging from ms to μs, with significant reduction in on-current and on-conductance observed as shown in the pulsed-IV measurements of a non-passivated device using Auriga$^T M$ pulsed IV setup in Fig.3-19. In Fig.(a) the device is turned-off by applying a fixed quiescent gate-voltage (V_{GQ}) of $-8\ V$, the drain is stressed to different quiescent drain-voltages (V_{DQ}) and the on-current output-characteristic is measured immediately after the device is turned on at non-

quiescent gate-voltage ($V_{GNQ} = 0\ V$) and non-quiescent drain-voltage (V_{DNQ}) upto 20 V. The off-state drain stress degrades the on-state current characteristics relative to same-bias unstressed conditions with significant increase of on-resistance and knee-voltage. In Fig.(b) similar voltage switching stress conditions are applied but now on the gate-terminal in the off-state. The V_{GQ} is varied for the same V_{DQ} and the on-current after the device switches-on shows degradation in both on-currents and on-resistances. The effect in both cases is exacerbated by the magnitude of applied stress voltage in the off-state.

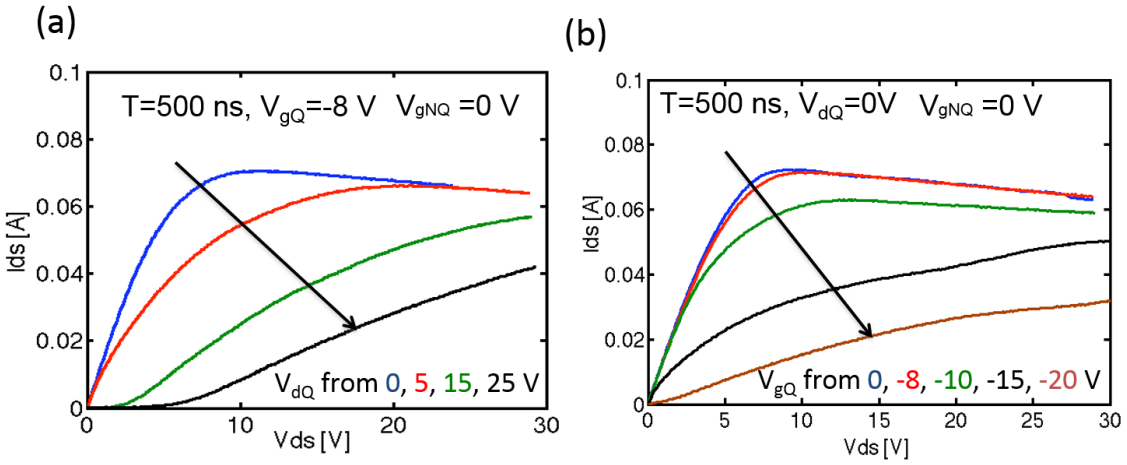


Figure 3-19: Pulsed IV measured for $V_{GNQ} = 0\ V$ under different off-state (a) drain-stress (V_{DQ}) and gate-stress (V_{GQ}) is shown. As the stress voltage is increased the R_{on} increases and the well-known knee-walkout phenomenon is observed.

Several mechanisms have been proposed for this effect. Some of them include charging of virtual-gate [30], gate-bias-induced nonuniform strain [29], and hot electron injection and trapping in the buffer [28]. The theories are still debated but the explanation of virtual-gate charging appears most convincing. Since the 2DEG in the channel of a GaN-HEMT is known to be created by donor type surface states, any impact on the surface states reflects in the 2DEG charge density. In the virtual gate-charging theory, the electrons from the gate compensate some of the surface states in the drain access region adjacent to the gate electrode. This results in the creation of a depletion layer in the channel next to the gate in the drain access-region. This region is therefore like a virtual gated region which increases the drain-access-region-

resistance causing current collapse. The MVSG approach to capture this dynamic large-signal effect is to incorporate a drain-to-gate voltage stress-dependence on the threshold-voltage (and or sheet resistance) of the implicit-gate transistor corresponding to the drain-access region to mimic the charge-depletion under high off-state voltage stress conditions. The time associated with the charge-trapping and de-trapping mechanisms are incorporated by using RC filters on the input-stress voltage functions which are then fed into the threshold-voltage calculation of access -regions transistors.

The current-collapse phenomenon is empirically known to scale-up with temperature, frequency and drain-to-gate field and can be mitigated through field engineering (to reduce fields), passivation layers to prevent the formation of surface traps, and using high quality buffer layer to minimize substrate traps, but it cannot be completely eliminated. Any compact model targeted to be used in circuit simulations using real devices must emulate the effect since it impacts the onset of gain compression and maximum output power in RF-HEMTs and slew rates along with static and dynamic power losses in HV-converters. Since the effect appears to be technology dependent with the exact mechanism for charge trapping and de-trapping heavily dependent on process conditions, a physical modeling approach is difficult. In this thesis the effect is captured in an empirical fashion using RC networks to model the charge trapping and release processes with full model validated the model against pulsed-IV measurements as shown in subsequent chapters.

In this chapter, a brief overview of the operating principle along with behavioral nuances of GaN-HEMTs relevant to both RF- and HV-applications were given. With this background on the various phenomena related to the workings of the device, the physics-based compact model, named MVSG model, which is the key contribution of this thesis is formulated in the next chapter. The model formulation will be shown to encompass all the described effects highlighted in this chapter.

Chapter 4

MIT Virtual Source GaN-HEMT (MVSG) Model Formulation

This chapter deals with the model formulation for the terminal characteristics of GaN-HEMTs encompassing the various physical-phenomena in the device highlighted in the previous chapter. Since the key contribution of this thesis-work is the development of physics-based compact-model for GaN-based-HEMTs that can be used for both RF- and HV-circuit design, the model description in this chapter forms the heart of this thesis. The chapter is organized as follows: Brief introduction into the charge-based approach adopted for MVSG model is given, elucidating its advantages, The key equations for channel-current in the intrinsic-gated-region is formulated followed by the derivation of channel-charges valid over the full-bias and gate-length ranges. This is followed by gate-current formulation and modeling approach to include physical effects in access-regions and field-plated regions. The extension of core-equations to make the model RF-circuit-design compatible by including small-signal, noise, static- and dynamic-thermal effects is done and in the concluding sections a derivation of charge-trapping-model along with an outline of the mathematical requirements for an industrial compact model is provided.

4.1 Charge-based modeling: History and merits

The genealogy of compact models for MOSFETs starts around 1960s with threshold-voltage (V_T)-based models where the channel-potential is assumed to be pinned after turn-on yielding simple but elegant closed-form expressions for drain-current. This modeling approach results in the well-known 'text-book' square-law expressions that are used to evaluate the device-behavior in circuits. Firstly started by Ihantola and Moll [31] the approach was extended for circuit-analysis by Sah[32] who later along with Pao [33] extended the drain-current expressions under various bias-conditions in terms of a physical parameter called the surface-potential (ψ_s) computed iteratively solving Poisson and Gauss' law. This approach gave rise to a class of models called surface-potential-based models. The inherent iteration was eliminated by approximations in MOS-level 1 and level-2 SPICE models [34] and continue to evolve as device complexities increase.

After the establishment of scaling rules in 1974 [35], the increased circuit-density in ICs promoted the vigor in the evolution of MOS-compact models with Brews [36] reporting in 1978, a simplified model based on charge-sheet-approximation of the inversion-charge (Q_i) along with depletion approximation which could be easily integrated with Computer-Aided-Design (CAD) in Electronic-Design-Automation (EDA) environment. During the late 1980s these 'charge-based' compact-models emerged as viable alternatives to the V_T-based models as the latter had increased in complexity while the ψ_s-based models continued to demand computational power. Many variants of charge-based models have been proposed since then, starting with the unified-charge-control model (UCCM) in 1990s [37], EKV model [38] in 1995, and Gummel-USIM model in 2001 [39] to name a few.

The advantage of charge-based models is that the independent variable namely: charge-density (Q_i) that requires to be computed at the source- and drain-terminals at each external bias point is computationally efficient to solve compared to ψ_s while retaining more accuracy than the simplistic V_T-based approach. The primary reason is that the current is an exponential function of ψ_s while it is only linear or quadratic

function of charges, thereby imposing lesser accuracy constraint on the computation of Q_i compared to ψ_s. In models for conventional FETs which may count in the tens or hundreds of thousands in modern logic circuit simulations or in models for the more recent III-V HEMTs which are themselves inherently sub-circuits of FETs even at the device-level, it is critical that the computational demand is minimal while preserving accuracy. In this context the charge-based modeling approach for FET-currents is suitable and it is the methodology adopted in the MIT-Virtual Source GaN-HEMT model (MVSG) in this thesis.

4.2 Carrier transport: Intrinsic-gate region

Intrinsic-gate region in GaN-HEMTs have gate-length ranging from tens of nm to few 100 nm for RF-HEMTs while for HV-HEMTs the gate-lengths are typically longer in the range of few micrometers. Besides, the short inelastic-mean-free-path of the order of a few Å for electrons in the 2DEG in GaN-HEMTs results in scattering-dominated diffusive transport in both application-regimes. The MVSG model therefore adopts drift-diffusive transport physics which could approach quasi-ballistic limit towards highly-scaled RF-gate-length-regimes. The earlier concept of virtual-source (VS)-based transport-approach developed at MIT and applicable for ballistic-motion in the channel is extended to diffusive-transport regime in this thesis. Since the core-underlying principles are adopted from the VS formulation, its principles are first elucidated before beginning the discussion on MVSG-core equations [40].

4.2.1 Origins of virtual-source concept

The intrinsic-transistor model in MVSG is based on the Virtual-Source (VS) concept formulated at MIT [41] which was originally developed for highly scaled Si-FETs with near-ballistic (quasi-ballistic) mode of transport. The model is based on "top-of-the-barrier-transport" in devices in which the channel-length is a few mean-free-paths or lower such that there is insignificant scattering in the channel. The physical picture of carrier transport in the intrinsic-transistor-region of scaled Si-devices with gate-

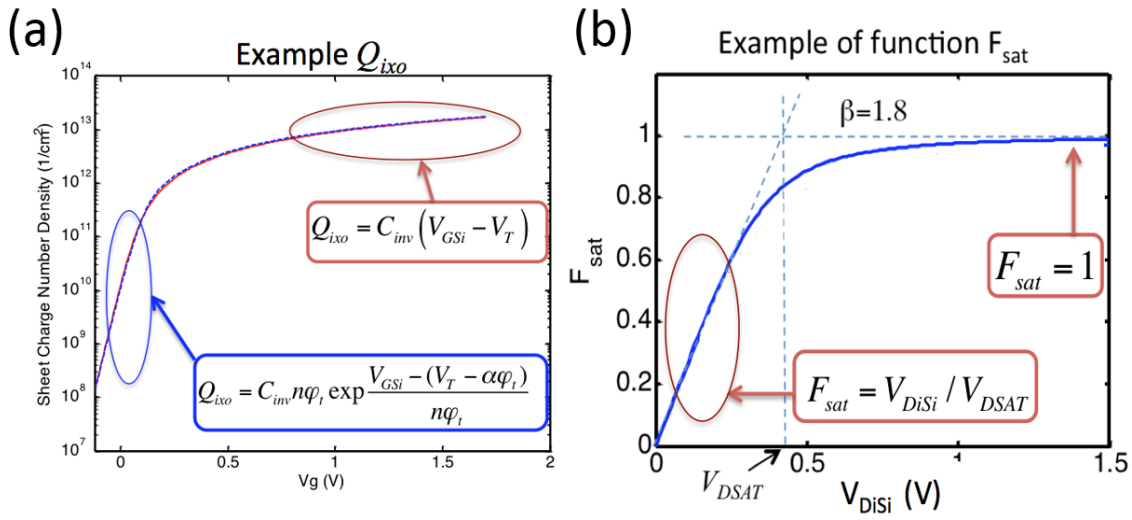


Figure 4-1: (a) An example for VS-point charge Q_{ixo} described by the model showing simplified expressions in strong and weak inversion. (b) An example for VS-point charge Q_{ixo} described by the model showing simplified expressions in strong and weak inversion.

lengths in the order of 10-100 nanometers can be explained with this concept in saturation-regime. Carriers are injected from source-terminal which is a thermal-equilibrium reservoir and on reaching the channel, face the potential energy barrier in the channel whose height is modulated by the gate voltage. In highly scaled devices, this barrier peaks at the beginning of the channel at $x = x_o$ (also known as the virtual-source point). Beyond this point, for sufficiently high drain-bias, the lateral-field in the channel is large enough to invalidate the application of gradual-channel-approximation (GCA) but the density of carriers at the top of the barrier can still be set by 1D-MOS electrostatics by the application of GCA.

Saturation regime (High V_{DSi})

In the 'charge-sheet approximation', the drain current normalized by width ($I_{DS}/(Wngf)$) can be described by the product of the local-areal-charge-density times the local carrier velocity anywhere in the channel. It is particularly useful to write this expression (4.1) at the location of the top of the energy barrier ($x = x_o$) where the channel charge density Q_{ixo}, is easiest to model by applying gradual-channel-approximation

(GCA):

$$I_{DS} = W n_{gf} Q_{ixo} v_{xo} \tag{4.1}$$

where $\boldsymbol{W}$ is the width of each finger of a FET, $\boldsymbol{n_{gf}}$ is the number of gate-fingers, and the average carrier velocity at VS-point is v_{xo}. The maximum possible value of v_{xo} is approximately the uni-directional thermal velocity and occurs when all the positive-velocity-carriers at the beginning of the channel are injected from the thermal-equilibrium-source [42]. Backscattering over a very short distance into the channel determines how close to this upper limit the device operates. In saturation, v_{xo} is empirically found to be a bias independent parameter [41]. The virtual-source charge density is given by the empirical form as in [41]. This expression allows for a continuous expression for the inversion charge density at the virtual source from weak- to strong-inversion. The basic form of the expression was first proposed by Wright [43] with the αF_f term introduced in [41] as follows:

$$Q_{ixo} = C_{inv} n \phi_t ln \left(1 + exp\left(\frac{V_{GSi} - (V_T - \alpha \phi_T F_f)}{n \phi_T}\right)\right) \tag{4.2}$$

Fig.4-1(a) depicts the way in which (4.2) captures the charge behavior in both strong- and weak-inversion along with the asymptotic forms of (4.2) in the two regimes. $\boldsymbol{C_{inv}}$ is the effective gate-to-channel capacitance per unit area in strong-inversion, $\boldsymbol{\phi_t}$ is the thermal voltage, V_{GSi} is the internal gate-source voltage corrected for source-resistance, n is the sub-threshold coefficient, which is related to the sub-threshold swing ($\boldsymbol{SS}$) as:

$$n = \frac{S}{\phi_t ln 10} + n_d V_{DSi} \tag{4.3}$$

where modest punch-through is modeled using the parameter $\boldsymbol{n_d}$. V_T is the threshold voltage corrected for drain-induced barrier lowering, DIBL, a well-known short channel effect as given by:

$$V_T = V_{To} - \delta V_{DSi} \tag{4.4}$$

Here $\boldsymbol{\delta}$ is the DIBL parameter and $\boldsymbol{V_{To}}$ is the threshold voltage at $V_{DSi} \approx 0$. The term following V_T in (4.2) allows for the requirement of different values of threshold

voltage in the strong and weak inversion standard textbook expressions (a shift of V_T by $\boldsymbol{\alpha\phi_t = 3.5\phi_t}$ for Si-FETs). The function F_f is a Fermi function that allows for a smooth transition between the two values of V_T and is centered at the point halfway between them [41]:

$$F_f = \frac{1}{\left(1 + exp\left(\frac{V_{GSi} - (V_T - \alpha\phi_T/2)}{\alpha\phi_T}\right)\right)} \tag{4.5}$$

Non-saturation regime

The description of current with v_{xo} as a bias-independent parameter is valid only for saturation regime of device operation where the carrier velocity is independent of lateral-electric-field. To account for the non-saturation region, the velocity v_{xo} in (4.1) is multiplied with the empirical saturation function F_{sat} [41]. F_{sat} increases smoothly from 0, at $V_{DSi} = 0$, to 1, at $V_{DSi} >> V_{DSAT}$, where V_{DSAT} is the saturation voltage. F_{sat} is similar to the Caughey and Thomas [44] formulation for carrier velocity saturation.

$$F_{sat} = \frac{V_{DSi}/V_{DSAT}}{\left(1 + (V_{DSi}/V_{DSAT})^{\beta}\right)^{1/\beta}} \tag{4.6}$$

An example depiction of F_{sat} is given in Fig.4-2(b) which shows how V_{DSAT} influences the linear-to-saturation transition for a particular value of $\boldsymbol{\beta}$. The current from linear to saturation is then given by the single expression

$$I_{DS} = W n_{gf} Q_{ixo} v_{xo} F_{sat} \tag{4.7}$$

While $\boldsymbol{\beta}$ is a fitting parameter, it is found over many fits to experimental devices, from Si MOSFETs to GaN HEMTs that β=1.0-3.0 provides excellent fit. Finally, to allow a smooth transition between the strong- and weak-inversion values of the saturation voltage V_{DSAT}, a generalized form of the saturation voltage, is introduced by employing F_f again using,

$$V_{DSAT} = V_{DSATS}(1 - F_f) + \phi_t F_f \tag{4.8}$$

$$V_{DSATS} = \frac{v_{xo} L_g}{\mu} \tag{4.9}$$

Here μ is the low lateral field apparent mobility of the carriers, which comprehends both diffusive and ballistic mobilities [45], and L_g is the gate-length. Note that equations governing linear-to-saturation transition are heuristic in nature [41] but the model is validated successfully against several scaled-Si and III-V devices [46]. The analysis so-far is targeted to the near-ballistic regime while the model for intrinsic-transistor-current in GaN-HEMTs needs to extend the VS-model described in this subsection to the diffusive-transport regime and will be shown next.

4.2.2 MVSG formulation for drift-diffusive transport

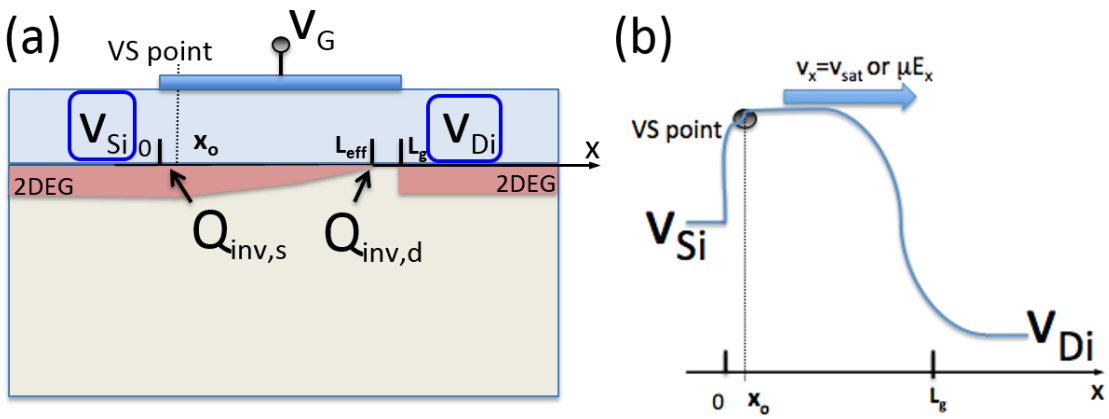


Figure 4-2: (a) Cross-section schematic of the intrinsic-gated region of GaN-HEMTs showing the intrinsic potential and charge metrics used for the terminal-current model along with their location. (b) The band-profile in saturation-regime which is assumed for the model-development is shown and the velocity at the VS-point now is a function of lateral-field and hence the applied bias unlike in ballistic-regime.

In GaN-HEMTs, small electron mean-free-path means that transport is not ballistic even at highly scaled-gate-lengths, which means that the velocity at the virtual source (v_{xo}) in the model described in detail in the previous section for highly scaled Si-FETs in the near-ballistic regime can no longer be assumed to be bias-independent in the saturation-regime. RF- HEMTs with highly scaled gate-length (but gate-lengths still many times the mean-free-path), could operate in quasi-ballistic-regimes at best,

wherein backscattering reduces the velocity from the ballistic-thermal-velocity-limit ($v_{xo} = Bv_T$, where B(<= 1) is the backscattering coefficient). In the most prevalent diffusive-length-scales, the velocity at the virtual source (v_{xo}) in saturation is no longer a bias independent quantity but is dependent on the local lateral-field as $v_{xo} = \mu E_{xo}$. The current in such devices is evaluated using the following procedure which can be viewed as an extension of the VS-model described in the previous section:

$$I_{DS} = Wn_{gf}Q_i(x)v(x) = Wn_{gf}Q_i(x)\mu E(x) = Wn_{gf}Q_i(x)\mu\frac{d\psi(x)}{dx} \tag{4.10}$$

Here $Q_i(x)$ is the channel charge at location x in the channel, $\psi(x)$ is the potential at that position and μ is the carrier mobility (μ could include several second-order scattering effects described in next section). To account for carrier velocity-saturation-effects, (4.10) is modified as below:

$$I_{DS} = Wn_{gf}Q_i(x)\mu\frac{\frac{d\psi(x)}{dx}}{\left(1+\left(\frac{\frac{d\psi(x)}{dx}}{\frac{v_{sat}}{\mu}}\right)^{\beta}\right)^{1/\beta}} \tag{4.11}$$

Here v_{sat} is the carrier-saturation-velocity and the form of carrier-velocity-saturation is the Caughey-Thomas form [44]. To enable a charge-based rather than potential-based formulation for current, a procedure similar to [47] is followed by relating $\psi(x)$ and $Q_i(x)$ as

$$\frac{dQ_i(x)}{d\psi(x)} = C_{inv} \tag{4.12}$$

Here $\boldsymbol{C_{inv}}$ is the channel-to-gate-capacitance which in our case is the areal-gate-capacitance of the intrinsic-transistor. Eq. (4.11) is valid at all x provided GCA holds, which is reasonable for a major portion of the channel except in the pinch-off or velocity-saturated region at the drain-end of the gate. Substituting for $\psi(x)$ in (4.11) using (4.12), integration of (4.11) can be done from $x = 0$ (source) to $x = L$ (drain). Here L is not necessarily the physical-gate-length (L_g) but has to be corrected for short-channel-effects described later. Substituting $Q_i(0) = Q_{is}$ and $Q_i(L) = Q_{id}$ along with employing current-continuity we get the following expression for current

in intrinsic-gate-transistor:

$$I_{DS} = W n_{gf} \frac{\mu}{2C_{inv}L} \frac{Q_{is}^2 - Q_{id}^2}{\left(1 + \left(\frac{Q_{is}-Q_{id}}{\frac{C_{inv}vL}{\mu}}\right)^{\beta}\right)^{1/\beta}} \tag{4.13}$$

Here v_{sat} has been replaced by v which is the carrier velocity combining strong- and weak-accumulation regimes in GaN-HEMTs, as discussed below. In order to make the current expression look similar to that of VS-model expression in (4.1), the current expression can be re-formatted as

$$I_{DS} = W n_{gf} \frac{v}{2C_{inv}V_{DSAT}} \frac{Q_{is}^2 - Q_{id}^2}{\left(1 + \left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{1/\beta}} = W n_{gf} v \frac{Q_{is} + Q_{id}}{2} F_{vsat} \tag{4.14}$$

where F_{vsat} is given by

$$F_{vsat} = \frac{\frac{Q_{is}-Q_{id}}{C_{invi}V_{DSAT}}}{\left(1 + \left(\frac{Q_{is}-Q_{id}}{C_{inv}V_{DSAT}}\right)^{\beta}\right)^{1/\beta}} \tag{4.15}$$

F_{vsat} governs the transition from non-velocity-saturation to velocity-saturation-regime of carrier-transport as channel-length is scaled down. F_{vsat} has a form similar to the Caughey-Thomas form [44] which was employed for F_{sat} in the VS-model (4.4). V_{DSAT} and v are saturation-voltage and saturation-velocity respectively and have the form below to account for both strong- and weak-accumulation.

$$V_{DSAT} = \frac{v_{sat}L}{\mu}(1 - F_f) + 2n\phi_T F_f \tag{4.16}$$

$$v = v_{sat}(1 - F_f) + 2\phi_T \frac{\mu}{L} F_f \tag{4.17}$$

where $\boldsymbol{\phi_T}$ is the thermal-voltage, F_f is the Fermi-function described in the previous section (but with a subtle-difference which is explained a little later), n is the sub-threshold-factor related to sub-threshold slope by $\boldsymbol{SS = n\phi_T ln(10)}$. The charges themselves have a form close to that of the VS-charges in the VS-model of previous

section. The source-end and drain-end charges given as:

$$Q_{is} = C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GDi} - V_{SX} - (V_T - \alpha\phi_T F_{fs})}{2n\phi_T}\right)\right) \tag{4.18}$$

$$Q_{id} = C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GSi} - V_{DX} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right) \tag{4.19}$$

The key distinction of the charge expressions here from that in (4.2) is that the charge expressions have additional factors of 2 to ensure correct sub-threshold current behavior, but this creates inconsistency in sub-threshold slope for charges in weak-accumulation. This issue needs further study but since capacitances in sub-threshold-regime are dominated by parasitic-capacitances, the discrepancy in weak-accumulation channel-capacitances can be ignored safely. In the expressions for charges, the terms F_{fs} and F_{fd} are the same Fermi-functions but referenced to source- and drain-terminals respectively which will be described later. In addition, the above charge-expressions contain V_{SX} and V_{DX} which are given by

$$V_{SX} = \frac{-V_{DiSi}}{\left(1 + \left(max\left(0, \frac{-V_{DiSi}}{V_{DSAT1}}\right)\right)^{\beta}\right)^{1/\beta}} \tag{4.20}$$

$$V_{DX} = \frac{V_{DiSi}}{\left(1 + \left(max\left(0, \frac{V_{DiSi}}{V_{DSAT1}}\right)\right)^{\beta}\right)^{1/\beta}} \tag{4.21}$$

These terms ensure that the drain(source)-charge saturates under velocity-saturation in forward(reverse)-mode and thereafter remains independent of applied drain-to-source voltage. The max() function ensures correct operation in both forward ($V_{DS} > 0$) and reverse ($V_{DS} < 0$) directions. The above formulation for Q_{is} and Q_{id} expressions are completely symmetric and can seamlessly flip current-direction as we go from forward-to-reverse modes. To explain further, when source is grounded and drain is ramped to positive values the charge-expressions simplify to:

$$Q_{is} = C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GSi} - (V_T - \alpha\phi_T F_{fs})}{2n\phi_T}\right)\right) \tag{4.22}$$

$$Q_{id} = \begin{cases} C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GDi} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right), \text{in linear regime.} \\ C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GSi} - V_{DSAT1} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right), \text{in saturation regime.} \end{cases} \tag{4.23}$$

In the reverse-mode when the source is still grounded but the drain is ramped to negative values, the physical-source-terminal becomes the electrical-drain and the physical-drain becomes the electrical-source-terminal and saturation-onset starts at the physical-source with the charge expressions given by

$$Q_{is} = \begin{cases} C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GSi} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right), \text{in linear regime.} \\ C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GDi} - V_{DSAT1} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right), \text{in saturation regime.} \end{cases} \tag{4.24}$$

$$Q_{id} = C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{V_{GDi} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right) \tag{4.25}$$

The saturation voltage-term V_{DSAT1} that appears in these expressions includes the effect of both pinch-off in long-channel-length-regimes and velocity-saturation in shorter-length-regimes and is given by:

$$V_{DSAT1} = V_{SAT}(1 - F_f) + 2n\phi_T F_f; \quad V_{SAT} = \frac{v_{sat} L}{\mu}\left(\sqrt{(1 + 2\frac{Q_{isd}\mu}{C_{inv} v_{sat} L})} - 1\right) \tag{4.26}$$

where $Q_{isd} = C_{inv} 2n\phi_t ln\left(1 + exp\left(\frac{max(V_{GSi}, V_{GDi}) - (V_T - \alpha\phi_T F_{fs})}{2n\phi_T}\right)\right)$ to ensure that the symmetry is retained in the current-formulation even when source- and drain-terminals are flipped. Finally, the Fermi-functions used in the current formulation are given by:

$$F_f = \frac{1}{\left(1 + exp\left(\frac{max(V_{GSi}, V_{GDi}) - (V_T - \alpha\phi_T/2)}{\alpha\phi_T}\right)\right)} \tag{4.27}$$

$$F_{fs} = \frac{1}{\left(1 + exp\left(\frac{V_{GSi} - (V_T - \alpha\phi_T/2)}{\alpha\phi_T}\right)\right)} \tag{4.28}$$

$$F_{fd} = \frac{1}{\left(1 + exp\left(\frac{V_{GDi} - (V_T - \alpha\phi_T/2)}{\alpha\phi_T}\right)\right)} \tag{4.29}$$

The formulation for intrinsic-transistor-current given in this section not only captures

the transport-physics in the channel that ensures accuracy in capturing the terminal current-characteristics encompassing the entire bias-regime from linear-to-saturation and below-turn-on to above-turn-on condition, but also ensures that the model is able to capture both forward-and reverse-modes of operation seamlessly preserving continuous derivatives of any order. The mathematical requirements imposed in addition to the requirements on accuracy is one of the key differentiating factors between circuit-design-compatible compact-models and physical-models used for device-study. The ability to produce infinite derivatives and accommodate source-drain flipping and passing symmetry-tests in current and charges are some of the normal qualification standards that any compact model should pass to qualify for industry-standard and will be explained in the last section of this chapter.

4.2.3 Thermal modeling of electrical quantities

The transport and electrostatic parameters of GaN-HEMT can change substantially with operating temperatures which manifest in the terminal-scharacteristics of the device especially in terms of increased R_{on} and reduced channel-currents as explained in chapter 3.8. The key electrostatic parameters that change with temperature are $\boldsymbol{SS}$ and $\boldsymbol{V_{T0}}$ which are captured as follows:

$$SS(T) = SS(T_0)\frac{T}{T_0} \tag{4.30}$$

$$V_{T0}(T) = V_{T0}(T_0) + V_{T\zeta}(T - T_0) \tag{4.31}$$

where $\boldsymbol{V_{T\zeta}}$ is the temperature-coefficient of threshold-voltage indicating a linear variation of V_{T0} with temperature. The key transport parameters that degrade with rising temperature are mobility and carrier-saturation-velocity whose thermal-dependence is modeled as [48]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-\epsilon} \tag{4.32}$$

$$v_{sat}(T) = v_{sat}(T_0)\frac{(1 + v_\zeta T_0)}{(1 + v_\zeta T)} \tag{4.33}$$

where $\boldsymbol{\epsilon}$ and $\boldsymbol{v_\zeta}$ are the temperature-coefficients of mobility and saturation-velocity respectively. In addition to the degradation of these transport parameters with temperatures, carrier-scattering at increased channel-charge results in a further reduction of these parameters, and are modeled by following the approach in [49]:

$$\mu = \frac{\mu_0}{\left(1 + \theta_\mu \frac{Q_{isd}}{C_{inv}}\right)} \quad ; \quad v_{sat} = \frac{v_{sat,0}}{\left(1 + \theta_v \frac{Q_{isd}}{C_{inv}}\right)} \tag{4.34}$$

where $\boldsymbol{\mu_0}$ and $\boldsymbol{v_{sat,0}}$ are low-field-mobility and low-field-saturation-velocity respectively and $\boldsymbol{\theta_\mu}$ and $\boldsymbol{\theta_v}$ are the scattering-coefficients of mobility and saturation-velocity respectively, which degrade these transport parameters at high vertical-fields. Even though the last equation is not due to thermal-effect, it is included here for the sake of completeness. This completes the description of core-channel-current-model formulation for intrinsic-gated region in the MVSG-model including thermal and scattering effects in the 2DEG-channel. In the next section, channel-charge partitioning of the intrinsic-gated-region is carried out to model the large-signal device-capacitances.

Table 4.1: **Summary of parameters used for intrinsic-transistor-current**

Parameter	Unit	Description
W	m	Width-per-finger
n_{gf}		Number of fingers
L_g	m	Gate-length
C_{inv}	F/m^2	Areal-gate-capacitance
SS	V/dec	Sub-threshold slope
V_{T0}	V	Threshold-voltage (at $V_D \approx 0$)
δ	V/V	DIBL
n_d		modest punch-through-factor
ϕ_T	V	Thermal-voltage
α		Empirical parameter to model surface-potential
β		linear-to-saturation transition parameter
$V_{T\zeta}$	V/K	Temperature-coefficient of V_T
ϵ		Temperature-coefficient of μ
v_ζ		Temperature-coefficient of v_{sat}
μ_0	m^2/Vs	Low-field mobility
$v_{sat,0}$	m/s	Low-field saturation-velocity
θ_μ	V^{-1}	Mobility-reduction parameter
θ_v	V^{-1}	Velocity-reduction parameter

4.3 Channel-charge: Intrinsic-gated-region

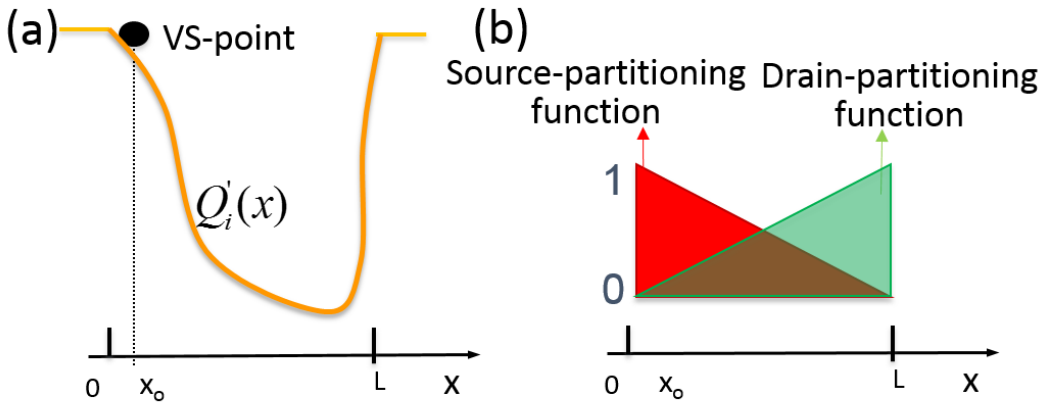


Figure 4-3: (a) The charge profile along the channel of intrinsic-gated-region under saturation along with (b) the linear Ward-Dutton source/drain charge-partitioning functions.

The channel-charges in any FET vary significantly and non-linearly with the applied gate-and drain-bias from both linear-to-saturation regimes and from off-to-on-state of the device which results in non-linear large-signal charges and hence non-linear small-signal capacitances. The saturation mechanisms including pinch-off and velocity-saturation cause the charge in the 2DEG to change substantially from source-towards-drain as shown in Fig.4-3(a). The non-uniform channel-charge should be partitioned between source- and drain-terminals to generate the gate-to-source and gate-drain charges and the MVSG model accomplishes this in a self-consistent manner with current (transport)-formulation using current-continuity and linear Ward-Dutton charge partitioning [50]. The linear partitioning functions for source- and drain-end-charges are highlighted in Fig.4-3(b) and the expressions for charge partitioning along with the total-gate-charge are given by:

$$Q_S = WL\int_{x=0}^{x=L}\left(1-\frac{x}{L}\right)Q_i(x)dx \tag{4.35}$$

$$Q_D = WL\int_{x=0}^{x=L}\left(\frac{x}{L}\right)Q_i(x)dx \tag{4.36}$$

$$Q_G = WL\int_{x=0}^{x=L}Q_i(x)dx \tag{4.37}$$

where $Q_i(x)$ is the areal-charge density in the channel as a function of position with the boundary conditions being $Q_i(0) = Q_{is}$ and $Q_i(L) = Q_{id}$ defined in the last section. Since the MVSG-model is charge-based, the closed-form expressions are obtained by changing variable of integration from position, x, to charge, Q_i, by using equations (4.10)-(4.12) which are repeated here.

$$I_{DS} = W n_{gf} Q_i(x) \mu \frac{d\psi(x)}{dx} \quad ; \quad \frac{dQ_i(x)}{d\psi(x)} = C_{inv} \tag{4.38}$$

$$dx = \frac{W n_{gf} Q_i(x) \mu}{I_{DS} C_{inv}} dQ_i(x) \tag{4.39}$$

The position x can be expressed in terms of $Q_i(x)$ by integrating the above expression and is substituted in (4.36-4.38) to get the integrals in terms of charges as follows:

$$x = \frac{W n_{gf} \mu}{2 I_{DS} C_{inv}} \left(Q_i(x)^2 - Q_{is}^2 \right) \tag{4.40}$$

$$Q_S = WL \int_{Q_i=Q_{is}}^{Q_i=Q_{id}} \frac{W n_{gf} \mu}{I_{DS} C_{inv}} \left(1 - \frac{W n_{gf} \mu}{2 I_{DS} C_{inv} L} \left(Q_i(x)^2 - Q_{is}^2 \right) \right) Q_i^2(x) dQ_i(x) \tag{4.41}$$

$$Q_D = WL \int_{Q_i=Q_{is}}^{Q_i=Q_{id}} \frac{W^2 n_{gf}^2 \mu}{2 I_{DS}^2 C_{inv}^2 L} \left(Q_i(x)^2 - Q_{is}^2 \right) Q_i^2(x) dQ_i(x) \tag{4.42}$$

$$Q_G = WL \int_{Q_i=Q_{is}}^{Q_i=Q_{id}} \frac{W n_{gf} \mu}{I_{DS} C_{inv}} Q_i^2(x) dQ_i(x) \tag{4.43}$$

Plugging in the drain-current expression of MVSG model of (4.13) in the long-channel-limit and solving the above integrals gives closed-form expressions to the terminal-charges in the MVSG approach as follows:

$$Q_S = \frac{2WL}{\left(Q_{is}^2 - Q_{id}^2 \right)^2} \left[-Q_{id}^2 \frac{Q_{is}^3 - Q_{id}^3}{3} + \frac{Q_{is}^5 - Q_{id}^5}{5} \right] \tag{4.44}$$

$$Q_D = \frac{2WL}{\left(Q_{is}^2 - Q_{id}^2 \right)^2} \left[Q_{is}^2 \frac{Q_{is}^3 - Q_{id}^3}{3} - \frac{Q_{is}^5 - Q_{id}^5}{5} \right] \tag{4.45}$$

$$Q_G = \frac{2WL}{\left(Q_{is}^2 - Q_{id}^2 \right)} \left[\frac{Q_{is}^3 - Q_{id}^3}{3} \right] \tag{4.46}$$

It should be noted that long-channel-limit (quadratic-charge-dependence) for I_{DS} was

used in the above derivation (without the charge-terms in the denominator inside the exponent of $(1/\beta)$ in (4.13)) to keep the expressions simple without introducing much error as will be shown in the next chapter. The contribution of these derived-channel-charges to terminal-capacitances is as follows:

$$C_{gs} = -\frac{\partial Q_S}{\partial V_G} \tag{4.47}$$

$$C_{gd} = -\frac{\partial Q_D}{\partial V_G} \tag{4.48}$$

$$C_{gg} = C_{gs} + C_{gd} \tag{4.49}$$

Asymptotic values of these capacitances in different bias-regimes are correctly modeled using MVSG-approach and resembles the conventional FET-model-values under these bias conditions: Linear regime at $V_{ds} \approx 0\ V$ ensures that $Q_{is} = Q_{id}$ such that $C_{gg}/2 = C_{gs} = C_{gd}$ and is equal to $WLC_{inv}/2$ in the on-state. Similarly in saturation-regime in on-state, in the long-channel-limit: $C_{gs} = 6WLC_{inv}/15$, $C_{gd} = 4WLC_{inv}/15$, and $C_{gg} = 2WLC_{inv}/3$, which are similar to the EKV formulation for long-channel-FETs [47]. In conclusion, the charge-terms depend on the source-and drain-end areal-charges (Q_{is} and Q_{id}) which are also used for I_{DS} that includes the effects of pinch-off and velocity-saturation as explained in the previous section. The derivation for terminal-charges associated with the channel **do not** require additional parameters after the terminal-currents are matched against measurements as a consequence of self-consistency between transport and electrostatics. The core-transistor equations for currents and charges developed up to this point can be repeated with minor modifications for other regions of the device as will be explained in the next sections.

4.4 Access regions: Implicit-gate transistors

Access-regions in GaN-HEMTs are important because even state-of-the-art GaN-HEMTs are not self-aligned, as these regions are often used to augment the BV and end-up impacting the on-state current-drive of the device. Device-level TCAD

simulations were shown in the previous chapter which indicate that spatial-charge-distribution at high-lateral-fields resemble the profile in a normal FET in saturation. The simulations were also corroborated from measurements of TLM structures which show saturation of currents and thermal-mapping of these TLMs demonstrate non-uniform temperature distribution that correlates with the field-distribution similar to gated-FETs. From these observations, it becomes clear that carrier-transport through the access-regions can be best captured by modeling them as transistor-like elements that can accommodate carrier-pinch-off and velocity-saturation mechanisms under high-lateral-fields. The MVSG modeling approach is to model these regions as implicit-gate-transistors in series with the intrinsic-gated-regions as a sub-circuit as shown in Fig.4-4(b). These regions may be symmetric or asymmetric for RF- and HV-HEMTs respectively, as illustrated in Fig.4-4(a) that highlights these regions next to gate-metal. In this section, the relevant model equations for the regions are given.

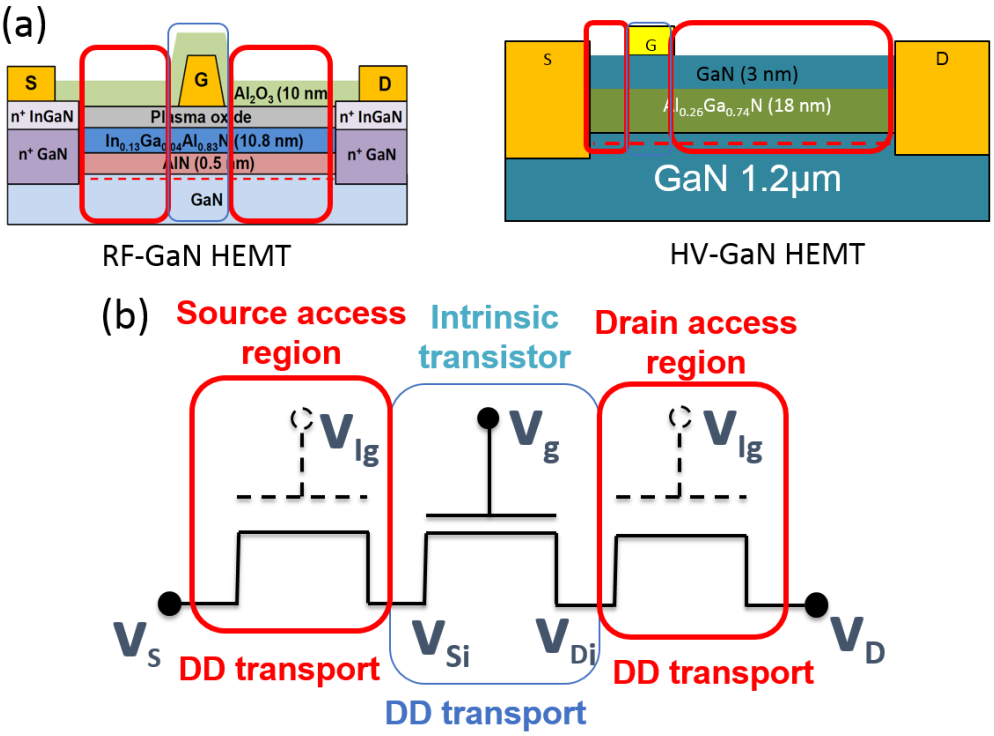


Figure 4-4: (a) Different-regions in both RF- and HV-GaN-HEMTs that require modeling-attention. (b) The sub-circuit approach taken in the MVSG-model that shows the series-transistor topology with the intrinsic-transistor-region along with implicit-gate-transistors for source- and drain-access regions.

Access-regions are usually asymmetric with the gate-to-source spacing ($\boldsymbol{L_{gs}}$) much shorter than the gate-to-drain spacing ($\boldsymbol{L_{gd}}$) since source-access-regions are usually the result of process-constraints while the drain-access-regions are intentional features for BV-enhancement. Typical lengths of access-regions range from few micrometers for HV-devices to few hundred nanometers for RF-devices (even for source-access regions for RF-devices) resulting in diffusive carrier-transport in them since the length-scale is much longer than the ballistic-mean-free-path of a few Angstroms. Therefore the transistor-model developed in the previous section can be adopted to model the access-regions as implicit-gate-transistors by suitable modifications to the electrostatics to capture the correct implicit-gate overdrive. Since there is no physical-gate metal in access-regions as shown in Fig. 4-4, modeling them as implicit-gate transistors warrants further explanation. Vertical-field lines that terminate at the 2DEG in the access-regions could originate from somewhere in the device (donor states at AlGaN surface, metal layers running above etc.) as explained in the previous chapter. In the limiting case, one could assume, that the field originates at infinity, in which case the implicit-gate is at infinity. The location of the origin of this vertical-field is the implicit-gate electrode. Since it is difficult to determine a location for the implicit-gate, the areal implicit-gate-capacitance (C_{Ig}) is a fitting parameter in the MVSG model. The value of the implicit-gate voltage (V_{Ig}) is linked to the 2DEG sheet-charge-density in the access regions. Under very low drain-bias conditions, access-regions are nothing but linear resistors. The current through the access regions under these conditions is given by:

$$I_{access} = \frac{V_{access}}{R_{access}} = \frac{V_{access}}{\frac{R_{sh} L_{access}}{W}} \tag{4.50}$$

Where I_{access} is the access-region-current, V_{access} is the voltage-drop across the access-region, L_{access} is the length of access-region ($\boldsymbol{L_{gd}}$ for drain-access -region and $\boldsymbol{L_{gs}}$ for source-access-region) and $\boldsymbol{R_{sh}}$ is the access-region sheet-resistance (the analysis holds for both source- and drain-access regions). From the implicit-gate-transistor model, the access-region-current at low-drain-voltages corresponding to linear-regime in on-

state can be obtained from the current expression given from (4.13) as

$$I_{access} = \frac{W}{L_{access}} \mu C_{Ig} (V_{Ig} - V_{T,Ig}) V_{access} \tag{4.51}$$

Equating the two forms of currents we get the following expression for implicit-gate-overdrive voltage:

$$(V_{Ig} - V_{T,Ig}) = \frac{1}{R_{sh} \mu C_{Ig}} \tag{4.52}$$

Thus implicit-gate overdrive can be computed from $\boldsymbol{\mu}$, $\boldsymbol{R_{sh}}$ and $\boldsymbol{C_{Ig}}$. This gate-overdrive-voltage and $\boldsymbol{C_{Ig}}$ is used in the Q_{is} and Q_{id} charge expressions of source and drain access regions to compute the channel-current in these regions using (4.13). The table of key parameters to model the current in these physical-regions are given at the end of this section. They include transport- and electrostatic-parameters with the same meaning as those used for the intrinsic-transistor-current and among them the transport-parameters usually have the same values as well. Flexibility to allow the use of different values to these transport-parameters is to ensure retention of accuracy even in rare scenarios where the channel-scattering could result in substantially different channel-mobility and saturation-velocity in access-regions compared to the intrinsic-transistor. Electrostatic parameters are usually different due to different gate-lengths of access-regions compared to the intrinsic-gate-length and among them $\boldsymbol{C_{Ig}}$ is one of the key parameters needed for the access regions in the MVSG model. The access-region model described in this section captures the observed non-linear behavior of these regions [51] and by modeling as implicit-gate transistors, the non-linear behavior of these regions is captured as pinch-off and velocity-saturation. The model is validated against gateless-TLMs and is discussed in the next chapter.

From the sub-circuit model of Fig. 4-4(b) it is clear that the intrinsic-transistor and access-region transistors are connected in series, which implies that at the intrinsic nodes Di and Si, carriers undergo complete thermalization by losing kinetic energy. However in these devices, carriers reaching the intrinsic transistor (at Si) have non-zero kinetic energy which is gained while traveling through the source-access-region and carriers reaching the intrinsic-drain-node (Di) may have sufficient kinetic energy

which is gained in the channel (Although the issue becomes less severe due to short mean-free-path for optical phonon emission). This physical effect is ignored in the MVSG compact model and carriers reaching intrinsic-transistor and drain-access-transistor are assumed to have no kinetic energy. In other words, the continuity of potential is ensured in the model using this approach but not that of electric-field which is a simplification done in order to ensure robustness in the compact model targeting circuit-design. This assumption can be relaxed and pseudo-2D Poisson equation near the drain-edge of each transistor can be solved to ensure field-continuity but at the cost of mathematical-robustness. This is added on to the model as an option for running device-level optimization that will be explained further in chapter 6. The assumption of thermalized carriers at Si is reasonable since the field in source-access-region is relatively low and does not impart significant energy to carriers. The assumption though might not be reasonable for carriers at Di as the field in the channel is quite high at large V_{DSi} and carriers have significant kinetic energy but carrier-velocity-saturation ensures that the error in currents is not severe.

Table 4.2: **Summary of parameters used for S,D-implicit-gate-transistors**

Parameter	Unit	Description
C_{Ig}	F/m^2	Implicit-gate-capacitance
$L_{gs},\ L_{gd}$	m	length of access-regions
R_{sh}	$\Omega/square$	Sheet-resistance of 2DEG
$SS_{rs},\ SS_{rd}$	V/dec	Sub-threshold slope
$\delta_{rs},\ \delta_{rd}$	V/V	DIBL
$n_{d,rs},\ n_{d,rd}$		modest punch-through-factor
$\alpha_{rs},\ \alpha_{rd}$		Empirical parameter to model surface-potential
$\beta_{rs},\ \beta_{rd}$		linear-to-saturation transition parameter
$\mu_{0,rs},\ \mu_{0,rd}$	m^2/Vs	Low-field mobility
$v_{sat,0rs},\ v_{sat,0rd}$	m/s	Low-field saturation-velocity

4.5 Field-plates: current and charge-modeling

Field-plated regions are secondary weakly-gated regions used to augment BV in the device with their own areal-gate-capacitances ($\boldsymbol{C_{g,gfp}}$ for GFP and $\boldsymbol{C_{g,sfp}}$ for SFP) and threshold-voltages ($\boldsymbol{V_{T,gfp}}$ for GFP and $\boldsymbol{V_{T,sfp}}$ for SFP) which can be extracted

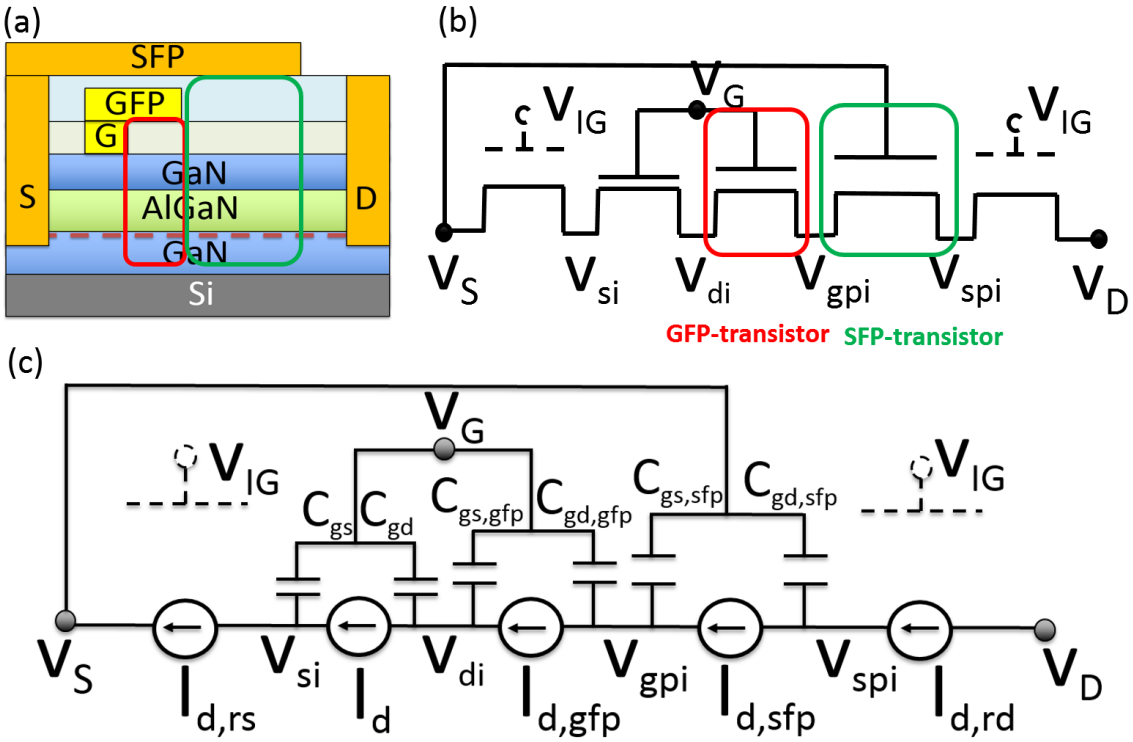


Figure 4-5: (a) Schematic of GaN-HEMT showing a gate-connected (GFP) and source-connected (SFP) field-plates (b) The series-transistor-modeling approach used in the MVSG-model and (c) the current-sources and distributed-charge modeling corresponding to each FET-region is shown in the form of a sub-circuit approach taken in MVSG is shown. This approach enables to capture carrier-transport physics, depletion-effects in the transistor and non-quasi-static effects in the device as will be shown later.

from CV-structures as explained in the previous chapter along with the operation of the FP-regions in terms of spatial-broadening of electric-fields and the 'domino-depletion' in successive FP-regions. The cross-section schematic of a typical GaN-HEMT that has both GFP and SFP is shown in Fig.4-5(a) along with the series-transistor sub-circuit approach taken in the MVSG model, as shown in Fig.4-5(b). The behavior of each region of the device in terms of the current (modeled using dependent-current-sources in series) and charges (modeled as large-signal-gate-source and gate-drain capacitances) in a distributed-fashion is adopted in the MVSG model as shown in Fig.4-5(c). Model-formulation for the current-sources as well as the capacitances are same as that of the intrinsic-transistor-model explained in equations

(4.10)-(4.19). Even though the formulation is identical, the associated parameter-sets are different as listed in the table at the end of this section. The difference in transport-parameters is not usually necessary (though they are kept independent for reasons of flexibility as described earlier) but electrostatic-parameters starting with V_T are different primarily because the design of FPs requires the V_T to decrease as we move towards the drain. The gate-lengths ($\boldsymbol{L_{g,gfp}}$ for GFP and $\boldsymbol{L_{g,sfp}}$ for SFP) are another set of design-parameters which also change the electrostatic-parameters and are typically different from the intrinsic-transistor-parameters. Another obvious difference is the terminal-voltages used for each FET-element, with the gate-to-source voltages for each FET-element given by: $V_G - V_{Di}$ for GFP-transistor and $V_S - V_{GPi}$ for SFP-transistor, the gate-to-drain voltages are: $V_G - V_{GPi}$ for GFP-transistor and $V_S - V_{SPi}$ for SFP-transistor and the drain-to-source voltages are: $V_{GPi} - V_{Di}$ for GFP-transistor and $V_{SPi} - V_{GPi}$ for SFP-transistor. In addition to current and non-linear gate-capacitances associated with the FPs, a capacitance arising out of the fringing-fields between FPs is modeled in each region as explained next.

4.5.1 Cross-coupled charges

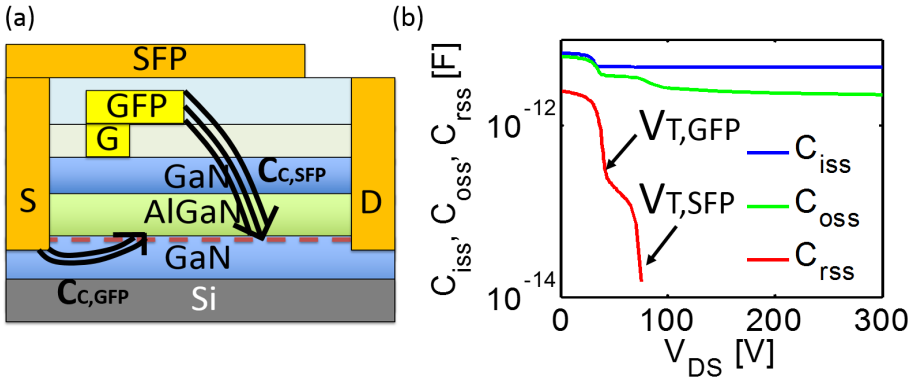


Figure 4-6: (a) Fringing-fields from gate-metal of GFP to the channel of adjacent SFP along with the fringing-fields from SFP-metal to the channel of GFP is shown in the schematic (b) The transition in the input- (C_{iss}), output- (C_{oss}) and reverse-transfer-(C_{rss}) CV characteristics at the threshold-voltage of each FP ($V_{T,gfp}$ for GFP, and $V_{T,sfp}$ for SFP) and the reduction in capacitance due to channel-depletion in the corresponding-FP is shown. The transition is visible in both capacitances associated with gate- and source-terminals at each FP-V_T indicating that the non-linear capacitances are not just gate-to-channel capacitances described earlier but also due to fringing fields in (a).

Fringing-fields arising from the gate-metal of each FP to the channel in the adjacent FP-region as shown in Fig.4-6(a) cause a transition in device-terminal capacitances associated with both gate- and source-terminals at each V_T of FPs present in the device. So it becomes necessary to add another non-linear, cross-coupled charge-term with each FP but associated with the other metal-type (source-metal if it is GFP and gate-metal if it is SFP). Since the EOT associated with the fringing-fields are difficult to estimate, the width-normalized-capacitances are extracted from 'steps' in the measured CV-characteristics in off-state of the device as shown in Fig.4-6(b) and are denoted as $\boldsymbol{C_{c,gfp}}$ for fringing-capacitance linked with GFP (between source-metal and GFP-channel) and $\boldsymbol{C_{c,sfp}}$ for fringing-capacitance linked with SFP (between gate-metal and SFP-channel). The formulation for the cross-coupled-capacitances are given by:

$$Q_{c,gfp} = W n_{gf} C_{c,gfp} 2 n_{gfp} \phi_t ln \left(1 + exp\left(\frac{V_S - V_{Di} - V_{T,gfp} - \alpha_{gfp}\phi_T F_{f,gfp}}{2 n_{gfp}\phi_T}\right)\right) \tag{4.53}$$

$$Q_{c,sfp} = W n_{gf} C_{c,sfp} 2 n_{sfp} \phi_t ln \left(1 + exp\left(\frac{V_G - V_{GPi} - V_{T,sfp} - \alpha_{sfp}\phi_T F_{f,sfp}}{2 n_{sfp}\phi_T}\right)\right) \tag{4.54}$$

where n_{gfp}, n_{sfp} are the sub-threshold-factors, $\boldsymbol{\alpha_{gfp}}$, $\boldsymbol{\alpha_{sfp}}$ are the α-factors and $F_{f,gfp}$, $F_{f,sfp}$ are the Fermi-functions for GFP-and SFP-transistors as discussed earlier. This cross-coupled-term associated with each FP ensures that the V_T of each FP we see a transition in the CV-characteristics with respect to all terminal-nodes. The last detail in the FP-modeling is the body-to-FP-channel charge modeling and is discussed next.

4.5.2 Body-coupled charges

The discussion so-far in the thesis assumes that GaN-HEMT is a 3-terminal device with the body-terminal either absent or tied to the source which may not be the case in some devices. The body-terminal acts as a secondary weak-gate linked to the channel throughout the source-to-drain region, in which case non-linear capacitances linking the body-to-channel are reflected in capacitance between body and the other

three terminals. The junction capacitances that are typically associated with the body-terminal due to channel-depletion and source/drain-to-body-junctions in Si-FETs are absent in GaN-HEMTs but the body-to-channel capacitance decreases once the channel underneath the FP-region undergoes depletion under lateral-field. To model this effect, a capacitance is added between the body and the intrinsic-source-node of each FP-transistor whose charge-formulation is as follows:

$$Q_{b,gfp} = W n_{gf} C_{b,gfp} 2 n_{gfp} \phi_t ln \left(1 + exp\left(\frac{V_B - V_{Di} - V_{T,gfp} - \alpha_{gfp}\phi_T F_{f,gfp}}{2 n_{gfp}\phi_T}\right)\right) \tag{4.55}$$

$$Q_{b,sfp} = W n_{gf} C_{b,sfp} 2 n_{sfp} \phi_t ln \left(1 + exp\left(\frac{V_B - V_{GPi} - V_{T,sfp} - \alpha_{sfp}\phi_T F_{f,sfp}}{2 n_{sfp}\phi_T}\right)\right) \tag{4.56}$$

where $\boldsymbol{C_{b,gfp}}$, $\boldsymbol{C_{b,sfp}}$ are the width-normalized body-to-channel capacitance in each FP-region and the rest of the parameters have similar meanings as explained earlier.

Table 4.3: **Summary of parameters used for FP-transistors**

Parameter	Unit	Description
$C_{g,gfp}$, $C_{g,sfp}$	F/m^2	Areal-FP-gate-capacitance
$V_{T0,gfp}$, $V_{T0,sfp}$	V	FP-threshold-voltage (at $V_D \approx 0$)
$L_{g,gfp}$, $L_{g,sfp}$	m	FP-gate-length
SS_{gfp}, SS_{sfp}	V/dec	FP-sub-threshold slope
δ_{gfp}, δ_{sfp}	V/V	DIBL of FP-transistor
$n_{d,gfp}$, $n_{d,sfp}$		FP-modest punch-through-factor
α_{gfp}, α_{sfp}		Empirical parameter to model surface-potential in FPs
β_{gfp}, β_{sfp}		linear-to-saturation transition parameter for FPs
$\mu_{0,gfp}$, $\mu_{0,sfp}$	m^2/Vs	Low-field mobility for FPs
$v_{sat,0gfp}$, $v_{sat,0sfp}$	m/s	Low-field saturation-velocity for FP

The formulation of FP-regions described in this section is restricted to one GFP and one SFP as can be seen from Fig.4-5(a) but an actual HV-GaN-HEMT can employ any number of FPs of both configurations depending on the voltage-range of interest. The MVSG model can support upto four FPs where each one can be either GFP or SFP in a modular way, using function-calls as explained later in chapter 8 and observable from Verilog-A code given in Appendix. A. This modularity enables the extension to more than four FPs using additional function-call statements but at the same time fewer-than-four FPs can be handled as well by setting the gate-length

to zero for the FPs which are not in use. Zero gate-length ensures the collapse of the source-drain nodes in the corresponding FP as given in the verilog-A code in Appendix. A. Modeling of currents in intrinsic-, field-plate-, access-regions completes the formulation for total drain-source-current in the device. The next step in compact model-development is the modeling of the gate-currents in Schottky-gated HEMTs which is the topic of the next section.

4.6 Gate-current-modeling in Schottky-gated HEMTs

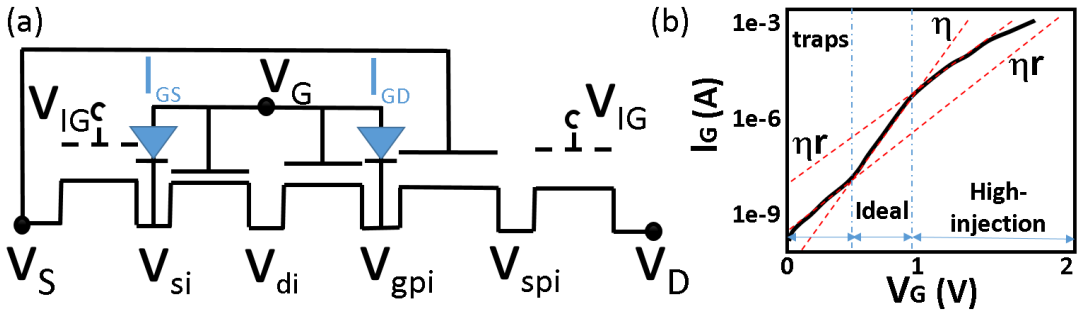


Figure 4-7: (a) Equivalent-circuit diagram for the GaN-HEMT described in the previous section with additions of gate-Schottky-barrier diodes (b) Typical gate-current plot against gate-voltage indicates the different non-idealities in gate-bias range which causes change in the diode-ideality factor. Charge-trapping and recombination results in higher ideality-factor just after turn-on and high-level injection results in a similar high-ideality-factor at high-positive gate-bias before saturation arising due to gate-resistance.

GaN-HEMTs used for RF-applications usually avoid employing oxides in the gate-stack since the gate-dielectric needs to be thin to maximize the charge-density n_s and high-frequency performance metrics such as transit-frequency (f_T) and maximum power-gain frequency (f_{max}). The consequence of this is that the gate-metal (Ni/Au-alloy) forms Schottky-contact with the AlGaN barrier-layer that restricts the gate-overdrive voltage due to the Schottky-gate-diode turn-on. The gate-currents contribute to input-power-dissipation in the gate-resistance especially in class-A saturated-power-amplifiers where the gate-voltage is significant for positive values resulting in non-negligible gate-current and input-power dissipation that affects the power-added-

efficiency (PAE). In addition, drain-to-gate leakage limits the off-state-current and hence the the ratio $\frac{I_{on}}{I_{off}}$ as demonstrated in chapter 3. Accurate modeling of the gate-current requires the inclusion of Schottky-barrier-diodes between gate and internal source and drain nodes in the equivalent-circuit of the MVSG-HEMT as shown in Fig.4-7(a).

4.6.1 Forward-mode currents

Because of different non-idealities associated with the gate-stack as observed from a typical log-scale gate-current plot in Fig.4-7(b) it is not enough to model the gate-current in the forward-mode through the ideal diode equation. Recombination in charge-trap-centers in the gate-stack typically results in high-ideality factor just after turn-on and a similar increase in the ideality-factor at high V_G due to high-injection effects is included in the model as follows:

$$I_{GSi} = W n_{gf} I_{gss} e^{-\frac{\phi_B}{\eta \phi_T}} \left(e^{\left(\frac{V_{GSi}}{\eta_{fs}\phi_T}\right)} - 1 \right) \tag{4.57}$$

$$I_{GDi} = W n_{gf} I_{gds} e^{-\frac{\phi_B}{\eta \phi_T}} \left(e^{\left(\frac{V_{GDi}}{\eta_{fd}\phi_T}\right)} - 1 \right) \tag{4.58}$$

where $\boldsymbol{I_{gss}}$ and $\boldsymbol{I_{gds}}$ are the reverse-saturation currents. $\boldsymbol{\phi_B}$ is the Schottky-barrier-height, η_{fs} and η_{fd} are the formulations for the ideality-factors that can model their change from $\boldsymbol{\eta}$ at low V_G to $\boldsymbol{r\eta}$ at high V_G mimicking the high-injection effect. It employs Fermi-functions similar to those use for currents to shift the ideality-factors between the two limits as a function of V_G as follows:

$$\eta_{fs} = \eta\left(r + (1-r)FF_{fs}\right) \;;\; \eta_{fd} = \eta\left(r + (1-r)FF_{fd}\right) \tag{4.59}$$

$$FF_{fs} = \frac{1}{1 + e^{\frac{V_{GSi} - V_{GSAT} + \alpha_G \phi_T/2}{\alpha_G \phi_T}}} \;;\quad FF_{fd} = \frac{1}{1 + e^{\frac{V_{GDi} - V_{GSAT} + \alpha_G \phi_T/2}{\alpha_G \phi_T}}} \tag{4.60}$$

where $\boldsymbol{V_{GSAT}}$ is the V_G at which the ideality-factors change from one limit-to-the-other, and $\boldsymbol{\alpha_G}$ is the α-factor. In addition to forward-mode currents, the reverse-mode current arising out of recombination-sources and gate-induced-drain-lowering (GIDL) are modeled using the formulation described next.

4.6.2 Reverse-mode currents

The drain-to-gate current in GaN-HEMTs in negative V_G determines the off-state floor of I_D as shown in the previous chapter. This flow of current from output-port to the input-port causes the power-flow out of the gate as opposed to into it and affects power-amplifier performance which needs modeling attention. This is captured in MVSG-model using the empirical-formulation below:

$$I_{GSi,rec} = -Wn_{gf}I_{recs}\left(e^{\left(\frac{F_{sat,GSi}}{\eta_{rec}\phi_T}\right)} - 1\right) \tag{4.61}$$

$$I_{GDi,rec} = -Wn_{gf}I_{recd}\left(e^{\left(\frac{F_{sat,GDi}}{\eta_{rec}\phi_T}\right)} - 1\right) \tag{4.62}$$

$$Fsat,GSi = -\frac{V_{GSi}}{\left(1+\left(\frac{|V_{GSi}|}{V_{GSAT,rec}}\right)^{\beta_{rec}}\right)^{1/\beta_{rec}}} \;;\; Fsat,GDi = -\frac{V_{GDi}}{\left(1+\left(\frac{|V_{GSi}|}{V_{GSAT,rec}}\right)^{\beta_{rec}}\right)^{1/\beta_{rec}}} \tag{4.63}$$

where $\boldsymbol{I_{recs}}$ and $\boldsymbol{I_{recd}}$ are the reverse-saturation-current, $\boldsymbol{\eta_{rec}}$ is the ideality-factor for the reverse-current of the diodes, $\boldsymbol{V_{GSAT,rec}}$ and $\boldsymbol{\beta_{rec}}$ are the empirical-parameters involved with the modeling of the saturation of reverse-current with V_G. The total-gate-current between gate-source (I_{GS}) and gate-drain (I_{GD}) is the sum of the forward and reverse-current expressions described so far. This model's accuracy in matching the measured gate-current-characteristics is highlighted in the next chapter.

4.6.3 Thermal-modeling of gate current

The gate-current model described so far has temperature-dependence primarily on account of $\boldsymbol{\phi_T}$ but also due to the temperature-dependence of the reverse-saturation-currents occurring in the pre-factor of the thermionic-emission model (the pre-factor of the current is proportional to $A^*T^{\epsilon_G}$, with A^* being the Richardson constant) which is formulated in power-law expressions of temperature with ϵ_G the power-law-coefficient of the diode currents:

$$I_{GSi}(T) = I_{GSi}(T_0)\left(\frac{T}{T_0}\right)^{\epsilon_G} \;\;;\;\; I_{GDi}(T) = I_{GDi}(T_0)\left(\frac{T}{T_0}\right)^{\epsilon_G} \tag{4.64}$$

$$I_{GSi,rec}(T) = I_{GSi,rec}(T_0)\left(\frac{T}{T_0}\right)^{\epsilon_G} \quad ; \quad I_{GDi,rec}(T) = I_{GDi,rec}(T_0)\left(\frac{T}{T_0}\right)^{\epsilon_G} \tag{4.65}$$

4.6.4 Breakdown of Schottky-diode

The final component of the gate-current model is due to the breakdown of the Schottky-junction under large-reverse-bias which is modeled by adopting a procedure similar to the Angelov-model [11] as follows:

$$I_{GSi,bd} = I_{GSi}\left(1 + K_{bd}e^{\frac{V_{SiG}-V_{bd}}{\phi_{bd}}}\right) \tag{4.66}$$

$$I_{GDi,bd} = I_{GDi}\left(1 + K_{bd}e^{\frac{V_{SiG}-V_{bd}}{\phi_{bd}}}\right) \tag{4.67}$$

where $\boldsymbol{K_{bd}}$ and $\boldsymbol{\phi_{bd}}$ are the empirical-fitting parameters to capture the exponential rise in the gate-diode-current at the reverse-breakdown-voltage of $\boldsymbol{V_{bd}}$.

Table 4.4: **Summary of parameters used for gate-current**

Parameter	Unit	Description
I_s	A/m^2	Reverse-saturation-current-density of forward-gate-currents
ϕ_B	V	Schottky-barrier-height of the gate-diodes
η		Ideality-factor (lower) of the ideal-Schottky-diode
r		Ratio by which η increases at high-injection-regime
α_G		Alpha-factor of the forward-gate-current model
V_{GSAT}	V	V_G at which transition into the high-injection-regime begins
I_{rec}	A/m^2	Reverse-saturation-current-density of reverse-gate-currents
η_{rec}		Ideality-factor of the reverse-diode-current
β_{rec}		linear-to-saturation transition parameter for reverse-gate-current
$V_{GSAT,rec}$	V	Saturation-voltage for reverse-gate-current
ϵ_G		Thermal-coefficient for gate-current
β_{rec}		linear-to-saturation transition parameter for reverse-gate-current
K_{bd}		Pre-factor to the breakdown-current
ϕ_{bd}	V	Exponential-factor of breakdown-current
V_{bd}	V	BV of Schottky-diodes

4.7 Modeling static- and dynamic-thermal effects

Significant temperature-rise due to power-dissipation during the device-operation was described in the last chapter and can be modeled in an average-sense (because 3D-

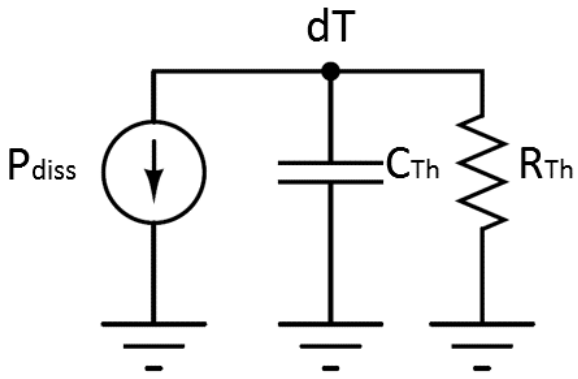


Figure 4-8: The standard-approach to capture device-self-heating is to use an RC-network as shown, in order to obtain the temperature-rise (dT) as a function of the power-dissipated (P_{diss}) in the device and including the dominant thermal-time-constant using the RC-network.

distributed heat flow from channel-to-substrate that requires geometric-modeling is not included in compact model) by computing the product of the power-dissipation (P_{diss}) and the thermal-resistance $\boldsymbol{R_{th}}$ of the device under static-conditions. The P_{diss} in the device is the sum of the current-voltage product across each branch in the sub-circuit shown in Fig.4-5(c) and is given by:

$$P_{diss} = I_D V_{DiSi} + I_{D,gfp} V_{GPiDi} + I_{D,sfp} V_{SPiGPi} + I_{D,rs} V_{SiS} + I_{D,rd} V_{DSPi} \tag{4.68}$$

$$dT = R_{th} P_{diss} \tag{4.69}$$

The temperature-rise given by the above expression is valid only under steady-state conditions but needs modifications for transient operation of the device where the applied-bias has significant large-signal time-variation. To achieve the 'average' rise in the temperature of the device under dynamic-operating conditions, the thermal-network shown in Fig.4-8 is used. The RC-network in the figure composed of the thermal-resistance ($\boldsymbol{R_{th}}$) and thermal-capacitance ($\boldsymbol{C_{th}}$) is essentially a low-pass filter whose input is the instantaneous-power dissipated in the device as described before and the $R_{th}C_{th}$ is the thermal-time constant. A single RC-network used in this approach mimics the dominant-time-constant of device-heating and is a com-

promise done with respect to limiting the number of additional internal-nodes in the model to improve computational robustness on one-hand and including higher-order time-constants (poles) to improve accuracy. The calculated dT is added to the operating-temperature (which is the substrate-temperature) which is then plugged into the thermal-model of electrical parameters for the different-transistor-regions and Schottky-gated-regions.

Device-self-heating significantly changes the channel-temperature that affects the electrical-characteristics as explained earlier and in turn changes the device-behavior in the circuits significantly impacting the circuit-performance both in power-amplifiers and HV-converters as will be explained in the next chapter. The core-transistor equations discussed upto this point are suitable for DC- and low-frequency operation-regimes but for VHF-applications which is an important class for GaN-HEMTs, inclusion of device-level parasitic elements is critical to accurately describe the device-behavior in frequencies comparable to f_T amd f_{max} as will be explained in the next section.

4.8 Small-signal model: Device-behavior at RF

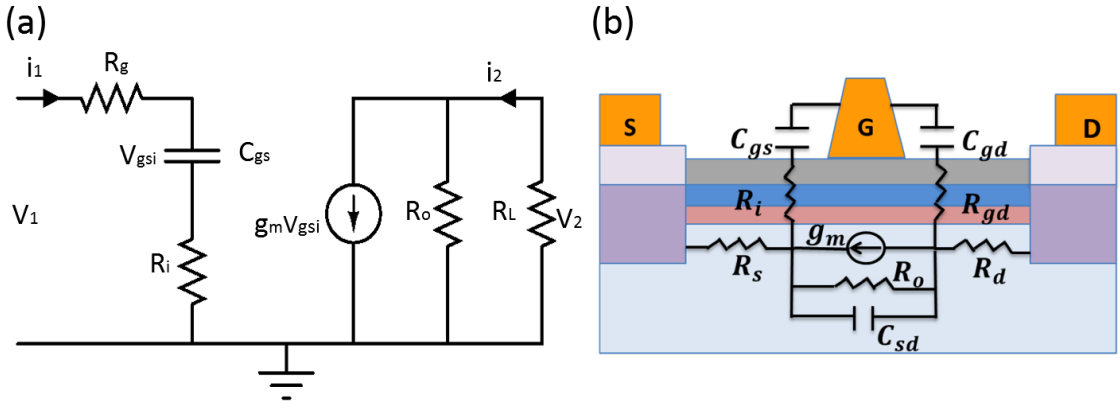


Figure 4-9: (a) A simple-small-signal saturated-HEMT circuit to extract the small-signal RF-figures-of-merit (FoMs) namely: f_T and f_{max} from small-signal device-parameters (b) The circuit-schematic is shown inside a cross-section of the GaN-HEMT device for clarity.

At microwave frequencies of device-operation (300 MHz to 300 GHz), standard

circuit theory fails as the signal wavelength approaches device dimensions. Phase shifts in signal voltages across the device can be accounted for by assuming two-port network-theory model with a simple small-signal equivalent circuit for the device in on-state saturation-regime as shown in Fig.4-9(a) along with the regions of the device that accounts for each element in (b). This enables the extraction of RF performance parameters such as unity-current-gain-cutoff frequency (f_T), and Unity-power-gain-cutoff frequency (f_{max}) given by:

$$h_{21} = \frac{i_2}{i_1} = \frac{g_m}{j\omega C_{gs}} \tag{4.70}$$

where h_{21} is the small-signal-current-gain of the device, g_m is the transconductance, and C_{gs} is the total-small-signal gate-to-source capacitance of the device. f_T is then given by:

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{4.71}$$

Similarly voltage-gain (A_v) can be computed as

$$A_v = \frac{v_2}{v_1} = \frac{g_m(R_o||R_L)}{\sqrt{1+\omega^2 C_{gs}^2 R_g^2}} \approx \frac{g_m(R_o||R_L)}{\omega C_{gs} R_g} \tag{4.72}$$

The power-gain then becomes

$$A_i A_v = \frac{i_2 v_2}{i_1 v_1} \approx \frac{g_m}{\omega C_{gs}} \frac{g_m(R_o||R_L)}{\omega C_{gs} R_g} \tag{4.73}$$

For the load matched case with $R_o = R_L$, maximum power delivered to the load is given as

$$G_p = A_i A_v/2 \approx \frac{g_m}{\omega C_{gs}} \frac{g_m(R_o)}{4\omega C_{gs} R_g} \tag{4.74}$$

The unity-power-gain-frequency (f_{max}) is then given by

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_o}{R_g}} \tag{4.75}$$

From the above equations it is clear that for maximizing f_T and f_{max}, device-scaling is

a straightforward solution. In addition to scaling, device-engineering to reduce device parasitics and gate-resistance also improves the RF-FoMs. The f_T values for GaN FETs are much higher than in Si FETs for the same breakdown voltage, which is a key advantage of GaN. To characterize these RF-FoMs accurately, the MVSG-model includes all the parasitic elements associated with the terminal pad-capacitances and lead- and via-inductances as described in last chapter. The small-signal equivalent-circuit shown in Fig.4-9 is a linear-circuit that is valid for a single-bias-point. The MVSG-model described so far is a large-signal device-model that captures all the elements of the equivalent-circuit including the change in their values with V_G and V_D. This core-model is then embedded inside a network that includes the device-parasitic elements as shown in Fig.4-10.

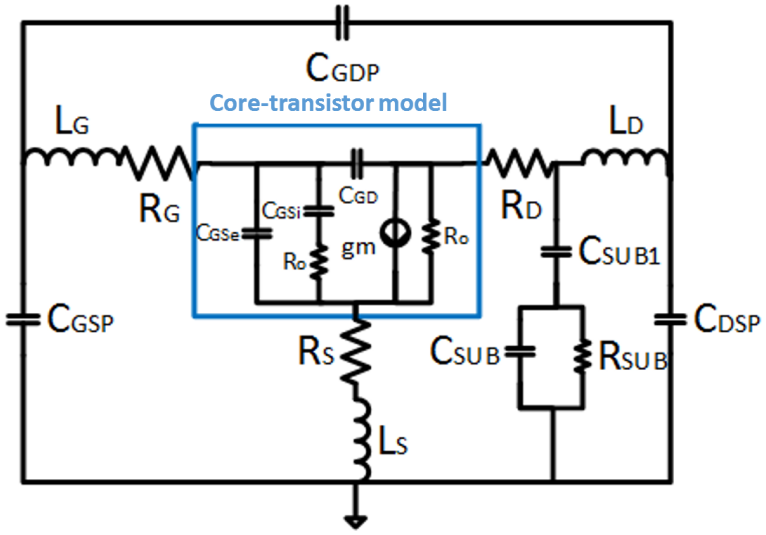


Figure 4-10: The full-equivalent-circuit of GaN-HEMTs that includes the core-transistor described by the formulation mentioned so far which is embedded inside a parasitics-network linked to the pad-capacitances, lead-inductances and substrate-loss-network. The circuit is the re-formatted version of Fig.3-19 and is adopted from the well-known Kondoh-model [52].

In the circuit-schematic shown in Fig.4-10, $\boldsymbol{C_{GSP}}$, $\boldsymbol{C_{GDP}}$ and $\boldsymbol{C_{DSP}}$ are the connection-pad capacitances, $\boldsymbol{L_G}$, $\boldsymbol{L_D}$ and $\boldsymbol{L_S}$ are the lead-inductances associated with the metal-lines or vias connecting the device-contacts to the connection-pads, and R_G, R_S and R_D are the contact-resistances of the device-contacts which include

their scaling with width and change with temperature as follows:

$$R_G = R_{gc}/(W n_{gf})\,(1 + r_{cg\zeta}\Delta T) \tag{4.76}$$

$$R_S = R_{sc}/(W n_{gf})\,(1 + r_{c\zeta}\Delta T) \quad ; \quad R_D = R_{dc}/(W n_{gf})\,(1 + r_{c\zeta}\Delta T)\,; \tag{4.77}$$

where $\boldsymbol{R_{gc}}$, $\boldsymbol{R_{sc}}$ and $\boldsymbol{R_{sd}}$ are specific-contact resistances and $\boldsymbol{r_{cg\zeta}}$, $\boldsymbol{r_{c\zeta}}$ are the temperature-coefficients of contact-resistances. Lastly the substrate-loss-path mentioned in the last chapter is modeled using the elements $\boldsymbol{C_{SUB}}$, $\boldsymbol{C_{SUB1}}$ and $\boldsymbol{R_{SUB}}$ shown in the figure. The extraction of these parameters require dedicated measurements of the device along with measurements of de-embedding structures that are necessary to get meaningful values for the parasitic-elements. These measurements include the multi-bias and multi-frequency scattering-parameters (S-parameters) using vector-network-analyzer (VNA). The details of the measurements are explained in detail in the next chapter and here the procedure to extract the parameters from the measurements that can be included in the MVSG-model is highlighted.

The S-parameters of the transistors are measured from low-frequencies ($100\ MHz$) to high-RF-frequencies (larger than f_T and f_{max} that could potentially be up to few-hundred GHz) at various bias points that span on-to-off and linear-to-saturation regimes. In addition, the measured S-parameters are de-embedded using on-wafer open and short test-structures as described in [53]. S-parameters of open-pad-structures can be used to obtain the values of the pad-capacitances: $\boldsymbol{C_{GSP}}$, $\boldsymbol{C_{GDP}}$ and $\boldsymbol{C_{DSP}}$, and with these values extracted the S-parameter measurements of short-structures yield the terminal inductances and resistance values: $\boldsymbol{L_G}$, $\boldsymbol{L_D}$ and $\boldsymbol{L_S}$ and $\boldsymbol{R_G}$, $\boldsymbol{R_S}$ and $\boldsymbol{R_D}$. The de-embedded S-parameters (with effects of pad capacitances and terminal resistance and inductance parasitics removed) are converted to Y-parameters so that the key-circuit elements can be then extracted from the resulting Y-parameters at each bias-point as given by [53]:

$$C_{gs} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega}\left(1 + \left(\frac{Re(Y_{11}) + Re(Y_{12})}{Im(Y_{11}) + Im(Y_{12})}\right)^2\right) \tag{4.78}$$

$$C_{gd} = -\frac{Im(Y_{12})}{\omega}\left(1 + \left(\frac{Re(Y_{12})}{Im(Y_{12})}\right)^2\right) \tag{4.79}$$

$$C_{gg} = C_{gs} + C_{gd} \tag{4.80}$$

$$C_{ds} = \frac{Im(Y_{22}) + Im(Y_{12})}{\omega} \tag{4.81}$$

$$g_o = Re(Y_{22}) + Re(Y_{12}) \tag{4.82}$$

$$g_m = \sqrt{(Re(Y_{21}) - Re(Y_{12}))^2 + (Im(Y_{21}) - Im(Y_{12}))^2} \tag{4.83}$$

The values of these small-signal parameters can be compared against the values resulting out of the S-parameter simulations of the core-transistor model so as to verify the accuracy of the MVSG-approach to capture the RF-behavior of the device and will be shown in next chapter. Lastly in order to ensure accuracy of the core-transistor small-signal-parameters at every-bias point, the capacitances associtaed with the fringing fields of the gate-lines must be included in the MVSG-model as follows.

4.8.1 Fringing-capacitances of core-transistor

The sub-circuit of the core-transistor MVSG-model shown in Fig.4-5 includes non-linear bias-dependent channel-capacitances but does not include the bias-independent fringing-capacitances associated with the four-terminals as follows:

$$Q_{fs} = C_{ofs}\,(V_G - V_S) \;\; ; \;\; Q_{fd} = C_{ofd}\,(V_G - V_D) \;\; ; \;\; Q_{fds} = C_{ofds}\,(V_D - V_S) \tag{4.84}$$

$$Q_{fbs} = C_{ofbs}\,(V_B - V_S) \;\; ; \;\; Q_{fbd} = C_{ofbd}\,(V_B - V_D) \;\; ; \;\; Q_{fbg} = C_{ofbg}\,(V_B - V_G) \tag{4.85}$$

Here $\boldsymbol{C_{ofs}}$, $\boldsymbol{C_{ofd}}$, $\boldsymbol{C_{ofds}}$, $\boldsymbol{C_{ofbs}}$, $\boldsymbol{C_{ofbd}}$ and $\boldsymbol{C_{ofbg}}$ are the fitting parameters to the fringing-capacitances in the MVSG-model which can be extracted from low-frequency CV measurements as explained in detail in next chapter. The model that is calibrated up to small-signal S-parameters at various bias- and frequency-ranges becomes capable of capturing the large-signal device behavior since the model has physical-grounding that ensures that the small-signal device metrics at each local-bias-point are derivatives of 'global'-large-signal device metrics. Key large-signal characteristics

include the transducer-gain (G_t), output-power (P_{out}), power-added-efficiency (PAE), linearity and harmonic-behavior along with inter-modulation-distortion (IMD) which form the design-specifications for RF-transmitter-power-amplifiers, and the model's capability to estimate them are verified against various measurements described in subsequent chapters.

Table 4.5: **Summary of parameters used for RF-parasitics**

Parameter	Unit	Description
$C_{GSP}, C_{GDP}, C_{DSP}$	F	Terminal-pad-capacitances
L_S, L_D, L_G	H	Terminal-lead-inductances
R_{gc}, R_{sc}, R_{dc}	$\Omega - m$	Terminal-specific-contact-resistances
$r_{gc\zeta}, r_{c\zeta}$	K^{-1}	Temperature-coefficient of contact-resistance
C_{SUB}, C_{SUB1}	F	Substrate-capacitances
R_{SUB}	Ω	Substrate-resistances
$C_{ofs}, C_{ofd}, C_{ofds}, C_{ofbs}, C_{ofbd}, C_{ofbg}$	F	Terminal-fringing-capacitances

4.9 Device-noise: RF- and phase-noise modeling

Device-noise in GaN-HEMTs impacts the noise-figure of amplifiers built using these devices and is critical for the design of low-noise-amplifiers (LNA) at the front-end of receiver stages, while the low-frequency-noise of the device impacts the phase-noise and skirt-characteristics of the oscillators for the VCOs at the mixer-stages. The noise sources are hence of two variants: The RF-white noise associated with the device-level-noise sources and low-frequency noise sources associated with charge-states in the device, both of which are explained in this section along with the MVSG-modeling approach to capture them.

4.9.1 RF-device-noise

The white-noise sources present in GaN-HEMTs are highlighted in the small-signal equivalent circuit of Fig.4-11 and are of two types, namely: the thermal-noise linked with various resistive elements of the device and the shot-noise sources linked to the Schottky-barriers of gate-source and gate-drain junctions. The noise-power-spectral-

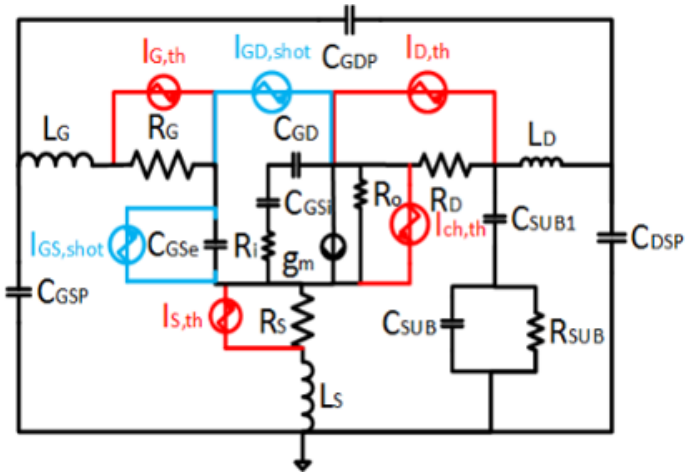


Figure 4-11: The full-equivalent-circuit of GaN-HEMTs that includes the various RF-noise sources that contribute to the device-noise-figure and are part of the MVSG-model.

density linked to the parasitic-resistances are given by the Johnson-Nyquist thermal noise formulation given by:

$$I_{S,th}^2 = 4KT/R_S \quad ; \quad I_{D,th}^2 = 4KT/R_D \quad ; \quad I_{G,th}^2 = 4KT/R_G \tag{4.86}$$

where $\boldsymbol{K}$ is the Boltzmann constant and the resistances are extracted from S-parameter measurements described in the previous section. Unlike the resistive thermal-noise the thermal-noise linked to the device-channel is bias-dependent and is a modified-formulation of the device-channel-noise given in [26] as follows:

$$I_{ch,th}^2 = 4KT\left(g_m F_{sat} + g_{ds}\left(1 - F_{sat}\right)\right)\Gamma \tag{4.87}$$

where g_m and g_{ds} are the small-signal-transconductance and output-conductance which are bias-dependent, F_{sat} is the linear-to-saturation parameter given by equation (4.6) and Γ is given by:

$$\Gamma = \frac{Q_G}{W n_{gf} L C_{inv}} \tag{4.88}$$

with Q_G given by (4.46). Γ transforms from 1 in the linear-regime to the factor of $2/3$ in saturation as required by conventional channel-thermal noise models. Moreover this approach enables the channel-thermal-noise in the linear-regime to be caused by the channel-resistance at $V_D \approx 0$ which is given by g_{ds} and in saturation the

thermal-noise is proportional to g_m. It is to be noted that none of the thermal-noise sources in the model need additional parameters since they are based on DC, AC and small-signal model-parameters which are already described in previous sections. The second category of white-noise sources are the shot-noise sources associated with gate-Schottky diodes and are modeled as follows:

$$I^2_{GS,shot} = 2q\left(I_{GS} + 2\left(Wn_{gf}I_{gss}e^{-\frac{\phi_B}{\eta\phi_T}} - Wn_{gf}I_{recs}\right)\right) \tag{4.89}$$

$$I^2_{GD,shot} = 2q\left(I_{GD} + 2\left(Wn_{gf}I_{gds}e^{-\frac{\phi_B}{\eta\phi_T}} - Wn_{gf}I_{recd}\right)\right) \tag{4.90}$$

This formalism is consistent with the approach taken in [54] and reduces to the conventional $2qI$ limit in forward-active mode where I is the gate-source (I_{GS}) or gate-drain (I_{GD}) current. The second terms in the parentheses in the above equations are nothing but the reverse-saturation currents (I_{sat}) of the diodes and at large reverse bias, the model formulation reduces to $2qI_{sat}$. At zero-voltage across the diodes, the Nyquist-limit of the shot-noise-source is $4KTg$ where $g = \frac{dI}{dV}$ is the diode-conductance which is given by $g = I_{sat}/\phi_T$ and the noise-source at zero voltage therefore reduces to $4qI_{sat}$ which is correctly modeled in the above expressions. Once again, the shot-noise-modeling in the MVSG-approach **does not** need additional parameters once the gate-current model is calibrated. Both thermal- and shot-noise-sources account for the RF-device noise that is relevant to the design of RF-LNAs on the receiver-side of a transceiver system and a detailed procedure to device-level noise-figure measurements and model validation is provided in the next section.

4.9.2 Device-phase-noise

The second category of device-noise sources are low-frequency flicker-noise sources associated with the various charge-capture and -release processes in the device. The well-known Leeson's phase-noise model is adopted in the MVSG approach to capture the phase-noise in GaN-HEMTs and is given by [55]:

$$I^2_{1/f} = K_f\frac{Wn_{gf}}{L}\frac{\left(\frac{|I_{DS}|}{Wn_{gf}}\right)^{af}}{f^{ffe}} \tag{4.91}$$

where the parameters $\boldsymbol{K_f}$, $\boldsymbol{af}$ and $\boldsymbol{ffe}$ are flicker-noise fitting parameters. The I_{DS} used in the above formulation is obtained from the (4.13) and captures the bias-dependence of the flicker-noise in the device. The width-dependency adopted in the MVSG-model makes it geometry-scalable and is based on the approach given in [56].

Table 4.6: **Summary of noise-model-parameters**

Parameter	Unit	Description
K_f	$Hz^{-1}m^{-2}$	pre-factor of the flicker-noise-model
af		Current-exponent of flicker-noise
ffe		Frequency-dependence of flicker-noise

4.10 Modeling charge-trapping

A significant non-ideality present in the emerging GaN-HEMT technology is the so-called 'dynamic-current-collapse' or 'knee-walkout' that was described in the last chapter. The effect manifests itself in reduced on-currents and increased R_{on} under switching-conditions compared with DC characteristics, and also sometimes as dynamic V_T shifts during switching conditions. The origins of charge-trapping was discussed in detail earlier and is attributed to surface and/or bulk donor trap-states that are filled during switching causing a reduction in n_s either under the gate (causing V_T shifts) or in the drain-access region (increasing R_{on}) and with the effect seemingly aggravated by high drain-to-gate fields, and increases with switching-frequency and temperatures. The precise location and trapping mechanisms are still a topic of research and varies widely over technology-recipes because of which the MVSG-model accounts for the effect in an empirical-fashion that can be fitted to specific outcomes.

An average charge-trapping module that can mimic the observed knee-walk-out can be an RC-filter whose output is the extent to which the R_{sh} in the drain-access transistor is increased during switching. The input source-function is dependent on V_{DG} and T and is shown in Fig.4-12(a). The source-function is given by:

$$f(V_{DG}) = \alpha_{T1}|V_{GD}| + \alpha_{T2}e^{\frac{V_{DG}-V_{trap}}{\alpha_{T3}}} \tag{4.92}$$

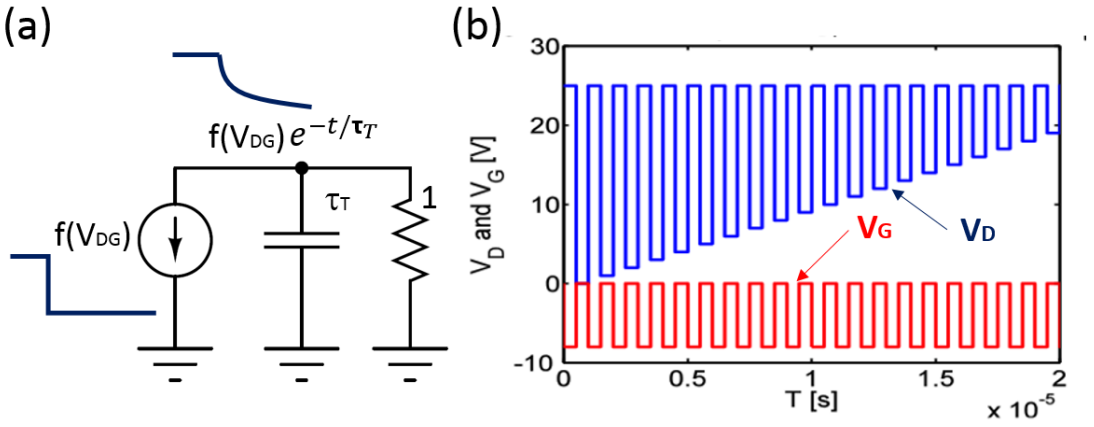


Figure 4-12: (a) The RC-time sub-circuit that models the charge-de-trapping time-constant (τ_T) and whose input $f(V_{DG})$ function is a temperature and field-dependent step-function while the output is a decaying function that can raise the sheet-resistance, R_{sh}, of drain-access-region (b) Typical gate- and drain-switching waveforms that mimic the Auriga^{TM}-pulsed-IV setup. The drain is switched from high-value in quiescent-state to low-value in non-quiescent-state. The gate is switched correspondingly from off-quiescent-state to on-non-quiescent-state as shown.

where $\boldsymbol{\alpha_{T1}}$, $\boldsymbol{\alpha_{T2}}$, $\boldsymbol{\alpha_{T3}}$, and $\boldsymbol{V_{trap}}$ are the empirical fitting-parameters to mimic the dependency of the extent of charge-trapping on V_{DG}. The nature of the function is such that as V_{DG} increases (either by stressing the device to high V_D in off-state or by applying large-off-state V_G), increases initially linearly and if the V_{DG} stress-voltage exceeds V_{trap} it increases significantly due to the exponential-function. The output node-voltage of the stress-RC-network shown in Fig.4-12(a) is then fed into the drain-implicit-gate-transistor model as follows:

$$dR_{sh}(V_{DG}, T) = 1 + f(V_{DG})e^{-t/\tau_T}(1 + \theta_T \Delta T) \tag{4.93}$$

Here $\boldsymbol{\theta_T}$ is the temperature-coefficient of trapping. The dR_{sh} is the ratio by which the sheet-resistance (R_{sh}) of the drain-access-region increases dynamically which results in the dynamic-currents shown in Fig.3-12 and will be shown in the next chapter. The approach followed here only increases the R_{on} and the knee-voltage and assumes same trapping and de-trapping time-constants due to the simple sub-circuit configuration (the RC-time-constant has the similar response to both high-to-low (de-trapping)

or low-to-high (trapping) $f(V_{DG})$-source-function). Another approach with different time-constants which shifts V_T dynamically is described next.

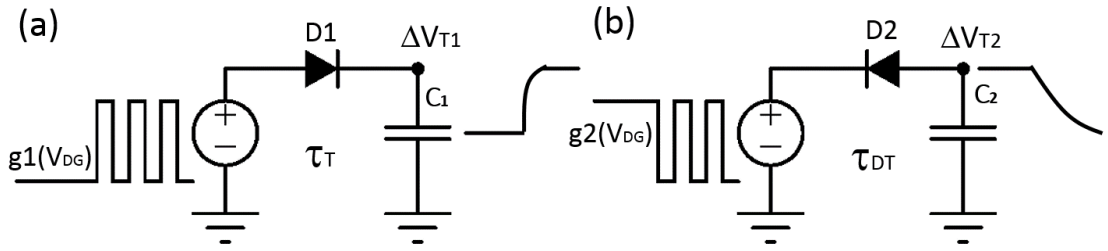


Figure 4-13: (a) The diode-capacitance-network associated with charge-trapping with time-constant τ_T whose output-voltage ΔV_{T1} is non-zero only when the input-source-function V_{DG} goes from low-to-high (when the device is stressed to the high-value) due to the forward-connected diode D1. (b) The diode-capacitance-network associated with charge-de-trapping with time-constant τ_{DT} whose output-voltage ΔV_{T2} is non-zero only when the input-source-function V_{DG} goes from high-to-low (when the device is de-stressed to the low-value) due to the reverse-connected diode D2.

Fig.4-13 shows the two diode-capacitance sub-circuits where the diodes D1 and D2 are used instead of the resistor in the previous approach. This ensures that each network is relevant to only one-edge-transition of the input-source-function $g(V_{DG})$. The low-state of $g(V_{DG})$ represents non-stressed condition (since here $V_{DG} < 0$) and the high-state of $g(V_{DG})$ represents stressed condition (since here $V_{DG} > 0$). In (a) the output-voltage ΔV_{T1} is ramped to non-zero values only when $g(V_{DG})$ switches from low-to-high while in (b) the output-voltage ΔV_{T2} is ramped to non-zero values only when $g(V_{DG})$ switches from high-to-low. Here the charging-time-constant τ_T is determined by the on-resistance of **D1** and **C1** while the de-trapping time-constants are determined by the on-resistance of **D2** and **C2** both of which can be independently set in the empirical model. The flip-side is that the approach requires two additional nodes for modeling the dynamic-V_T shifts. The source function is roughly proportional to V_{DG} given by:

$$g1(V_{DG}) = \alpha_{VT1} V_{DG} \quad ; \quad g2(V_{DG}) = \alpha_{VT2} V_{DG} \tag{4.94}$$

where $\boldsymbol{\alpha_{VT1}}$, $\boldsymbol{\alpha_{VT2}}$ are the empirical source-function-parameters and the dynamic V_T of the device is given by:

$$V_{T,trap} = V_T + \Delta V_{T1} + \Delta V_{T2} \tag{4.95}$$

Both the approaches have no effect in DC-conditions and change the current characteristics under large-signal transient simulations by affecting either R_{on} or V_T dynamically. While technology innovation at the process-level has mitigated this effect with reported R_{on} rise limited to less than 10% by employing passivation-techniques or field-engineering, it might not be completely eliminated and it requires the empirical modeling-approach. The two approaches formulated in this thesis are based on observations in available devices that were modeled. New processes or device-technologies may exhibit other forms of charge-trapping manifestations but can be modeled with same approach of employing RC or diode-capacitance networks but with different source-functions and/or outputs affecting different parameters of the MVSG-model.

This completes the physical-description of the MVSG-model-formulation that governs various phenomena in GaN-HEMTs suitable for both RF- and HV-applications. In the last section of this chapter, the mathematical requisites of a compact model for industrial-use is highlighted along with the properties of MVSG-model that enables it to meet these requirements.

Table 4.7: **Summary of charge-trapping-parameters**

Parameter	Unit	Description
α_{T1}		Charge-trapping empirical coefficient
α_{T2}, α_{T3}	V	Charge-trapping empirical coefficients
V_{trap}	V	Empirical-voltage which beyond which trapping aggravates
θ_T	V	Trapping temperature-coefficient
τ_T	s	Trapping and de-trapping time-constants in approach-1
$\alpha_{VT1}, \alpha_{VT2}$		Charge-trapping empirical coefficients
$D1\ C1$	s	Trapping time-constant parameter in approach-2
$D2\ C2$	s	De-trapping time-constant parameter in approach-2

4.11 Mathematical robustness of compact model

The rigor of physics is not the only challenge that compact models for semiconductor-devices face since modeling various physical-phenomena present in the device with im-

pressive accuracy at the expense of mathematical robustness of the model in involved-circuit-simulations can render the compact model useless for practical circuit-simulation-use. Highly accurate models have their own place in the device-technology-to-design-system workflow but they are mostly used to evaluate a new technology at the device-level and involve running single-device simulations without significant restrictions on simulation-time and/or computational-cost. Discretized TCAD models with finite-element-analysis (FEA) are the extreme-case examples of this approach and are not the primary topic of discussion of this thesis. On the other extreme are the table-based/empirical models that ensure mathematical rigor and speed of computation at the expense of accuracy to run detailed-circuit-simulations for new-technology evaluation at its initial stages. Physical compact models are an acceptable compromise between the two varieties and embody reasonable accuracy along with mathematical-rigor.

Several criteria to ensure mathematical-robustness of compact models are laid down by the compact-model-coalition (CMC) which are the result of industry consensus on the different types of circuit/system-level simulations that need to be run using the device-models with emphasis on the type of simulations (DC, AC, transient, periodic-steady-state, harmonic-balance, noise to name a few) and the complexity of circuit (number of transistor, their region of operation, layout-electro-magnetic simulation and so on). Some of these requirements for GaN-HEMT were pointed out in chapter 2 and this section deals with the requirement of differentiability and symmetry of core-model-formulation.

4.11.1 DC Gummel symmetry

Most FETs designed purposely for logic are structurally symmetric with respect to source and drain terminals and the compact-models must have symmetric-formulation around $V_{DS} = 0$ to reflect this. In addition to modeling currents, first- and higher-order derivatives such as g_{ds}, $g_{ds}^{'}$, $g_{ds}^{''}$ and so on must be continuous to ensure accuracy in distortion-simulations for RF-circuit-design such as RF-mixers. Seeking symmetry with respect to DC-characteristics in GaN-HEMTs is non-physical since the device is

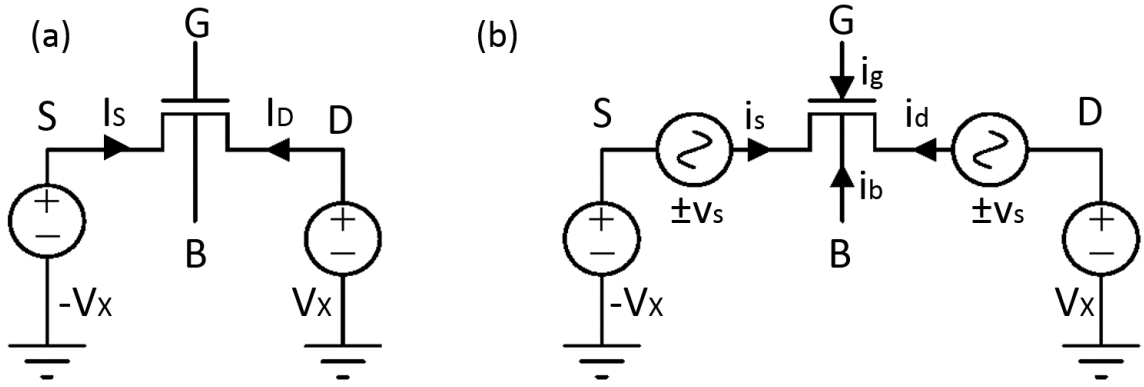


Figure 4-14: (a) Standard Gummel-symmetry test set-up to evaluate the DC-current S/D-symmetry and differentiability (b) McAndrew symmetry test set-up to evaluate the small-signal-capacitance symmetry and differentiability as in [57].

inherently not symmetric due to the presence of FPs, and asymmetric source, drain-access regions. However the differentiability of GaNFET compact models can be evaluated by making the device 'artificially'-symmetric by removing FPs and making the source-drain access-regions identical. This symmetric model is subjected to the DC-Gummel-symmetry-test that was proposed first in [58] with the test-setup given in the circuit of Fig.4-14(a). In this test, the source and drain are differentially biased with $-V_X$ and V_X respectively while the gate- and body-terminals are fixed in voltage. The test is a tool to evaluate the symmetry properties of all terminal-currents including gate-and body-current in addition to drain-source-channel-currents.

As V_X is ramped from negative to positive values the metric $I_X = \frac{I_D - I_S}{2}$ and its derivatives $\frac{\partial^N I_X}{\partial^N V_X}$ are evaluated. A symmetric-model that is non-singular yields continuous I_X and $\frac{\partial^N I_X}{\partial^N V_X}$ for all N around V_{DS}. Furthermore I_X and even-derivatives at $V_{DS} = 0$ are zero and are odd-functions around this point while the odd-derivatives are symmetric around $V_{DS} = 0$. The MVSG-model has symmetric-formulation of core-transistor equations with respect to source and drain which results in well-behaved currents and derivatives at all bias-points including $V_{DS} = 0$ and will be demonstrated in next chapter.

4.11.2 AC McAndrew symmetry

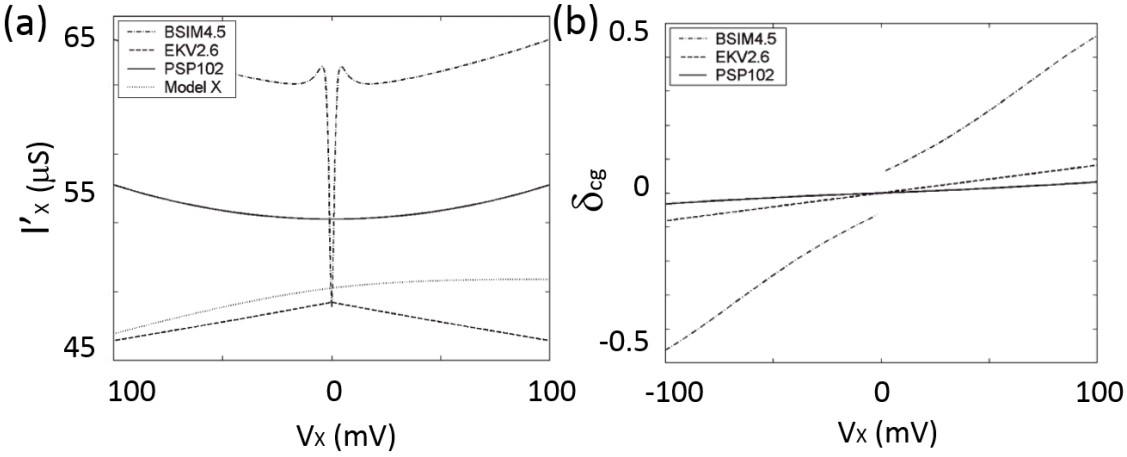


Figure 4-15: (a) The results of standard Si-FET compact-models in response to the DC-symmetry-test show that some of them fail in continuity of first-derivative of I_X (b) Similar outcomes of the AC-symmetry test shows that charge-formulation in some of the well-known compact-models have singularity even in first-derivatives indicating the severity of the problem of mathematical-robustness that is not focused in compact-model-development. These figures are from [57] and are reproduced here for convenience.

A rigorous capacitive-continuity test was proposed in 2006 [57] that evaluates the charge-continuity and symmetry around $V_{DS} = 0$ and can accurately determine the order of discontinuity and the exact charge that results in the discontinuity. The test-setup is given in Fig.4-14(b) that has the same differential DC-voltage source V_X applied to source-drain terminals and ramped from negative-to-positive values as in the Gummel-test-setup. In addition, in the AC-test a common-mode in-phase small-signal voltage-source and a differential small-signal-voltage v_s is also applied to both the terminals. The resulting small-signal terminal currents ($i_g,\ i_b,\ i_d,\ i_s$) in response to the AC-input is measured for both common-and differential-model input. The following metrics given in [57] are evaluated and their behavior around $V_{DS} = 0$ is tested to evaluate the charge-continuity of MVSG-model.

$$\partial_{cg} = \frac{i_{g-}}{i_{g+}} = \frac{C_{gs} - C_{gd}}{C_{gs} + C_{gd}} \tag{4.96}$$

where δc_g evaluates the continuity of gate-charges, with $i_{g-} = imag(ig)$ for differential-input and $i_{g+} = imag(ig)$ for common-mode input.

$$\partial_{cb} = \frac{i_{b-}}{i_{b+}} = \frac{C_{bs} - C_{bd}}{C_{bs} + C_{bd}} \tag{4.97}$$

where ∂_{cb} evaluates the continuity of body-charges, with $i_{b-} = imag(ib)$ for differential-input and $i_{b+} = imag(ib)$ for common-mode input, and,

$$\partial_{csd} = \frac{(i_{s-} + i_{d-}) + (i_{s+} - i_{d+})}{(i_{s-} - i_{d-}) + (i_{s+} + i_{d+})} = \frac{C_{ss} - C_{dd}}{C_{ss} + C_{dd}} \tag{4.98}$$

where ∂_{csd} evaluates the continuity of source/drain-charges, with $i_{s-} = imag(is),\ i_{d-} = imag(id)$ for differential input and $i_{s-} = imag(is),\ i_{d-} = imag(id)$ for common-mode input. The metrics ∂_{cg}, ∂_{bg}, and ∂_{csd} need to be odd-functions of V_X around $V_{DS} = 0$ and their derivatives should exist in order to pass the AC-symmetry-test.

The results from these symmetry-tests for standard-compact models are shown in Fig.4-15 which shows that some of the models fail the test and hence may not be appropriate tools for RF- or HV-simulations. The results of MVSG-model with regard to these tests are described in the next chapter.

Chapter 5

Device-Level Characterization and Model-Validation

The MVSG model formulated in the last chapter is validated against several device-level measurements in order to verify the validity of the underlying physical assumptions that were made in the derivation of the model-equations in the last chapter. The First assumption is: Quasi-ballistic/velocity-saturated transport at scaled gate-lengths and mobility dependent transport at longer gate-lengths, which manifests as near-linear charge dependence to quadratic charge dependence of the channel-current from short to long gate-lengths. The second assumption is charge depletion effects in the access-regions that is captured as implicit-gate transistors, and negligible energy of carriers as they enter from channel-region to FP-region and to the drain-access region. The other key assumptions are forward- and reverse-mode gate-current non idealities, linear-charge partitioning for charge formulation, a fixed bias independent RF-parasitic network, charge-trapping methodology and so on. Benchmarking the model against the device-level terminal-characteristics helps in determining the validity of these assumptions and demonstrates the ability of the MVSG model to capture the device-characteristics accurately.

In this chapter, the model comparison against measured terminal-currents, charges (capacitances), S-parameters, large-signal-metrics, device-noise-metrics, and pulsed-IV measurements for charge-trapping model characterization are demonstrated first

for HV-devices followed by RF-devices. Both these types of devices include devices fabricated at MIT and also a variety of industry-devices. The values of parameters used for these fits are demonstrated to be reasonable with straightforward physical meanings and most of them are extracted from independent device-measurements.

5.1 Modeling requisites for HV-circuit design

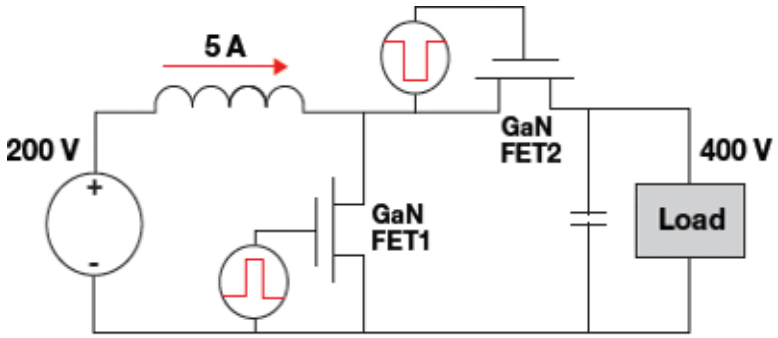


Figure 5-1: Simple boost-converter topology [59] employing two GaNFETs in hard-switching configuration. The source-inductance determines the current sunk by FET1 when on, and the off-state voltage is determined by input- and output-voltages.

GaN HEMTs employed in HV-switching circuits such as the one shown in Fig.5-1 typically operate as switches in off-state in the reverse-mode sustaining a large V_{DS} and are pushed to the linear-region in the on-state with a low V_{DS} voltage that is determined by the on-resistance and the load-current of the converter. The key requirements for an accurate high-voltage model is its ability to accurately capture the gate-charge stored in the off-state (which requires accurate capacitances associated with gate-terminal of the device) and the on-resistance of the device. However the picture is not as simple since the transistor moves all the way from off-state ($V_G < V_T, V_{DS}$) to on-state with reduced V_{DS} until it hits the R_{on}-limit of the device along the device-loadline-trajectory spanning a significant portion of the output-characteristics determined by the inductor-current and the passive elements associated with the switch-node. Typical current and voltage waveforms at this switch-node is shown in Fig.5-2(a). The spike in the current-profile is due to the addition of displacement-currents to the DC FET current during switching in hard-switched converters that results in significant power-dissipation. Even though the load-current is 5 A, the $C\frac{dV}{dt}$

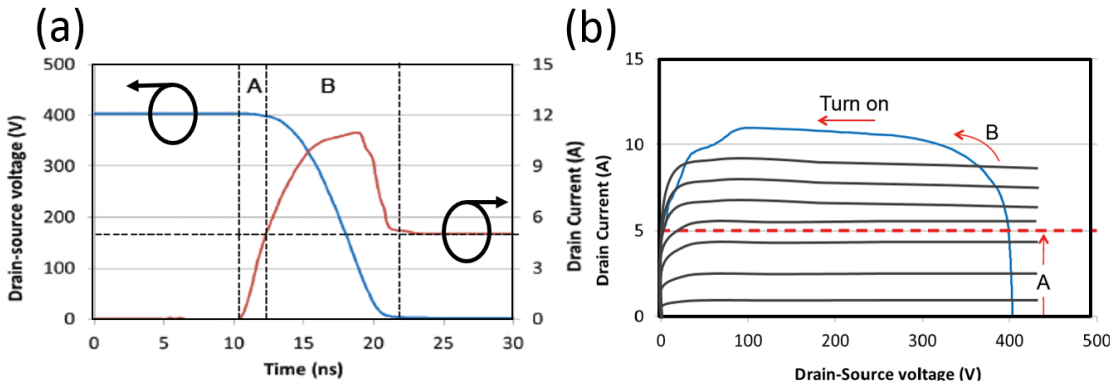


Figure 5-2: (a) Turn-on transition for a hard-switched switch-node-voltage transition showing both the switch-node-voltage and inductor-current. The FET1 is initially off in region A and turns on during the time correpsonding to region B (b) V-I locus of the inductive-switching-transition (from A to B) shows considerable current flow at high V_D. The discharge of the FET drain-capacitance in region B adds additional channel-current [59].

capacitive-displacement-currents are quite significant and the total-current can reach up to twice the load-current. The FET in the meanwhile traverses the trajectory shown in Fig.5-2(b) going from off- to on-state spending considerable amount of time in the saturation on-condition which tells us that the RC treatment of GaN-FETs in circuit-design is a highly simplistic approximation and cannnot yield accurate results vs. operating-temperatures, boost-ratio and conversion-efficiency. Accurate compact models which can estimate the device behavior in terms of currents and distributed-charges spanning off-state and on-state, and linear-to-saturation regimes are evidently critical, in addition to thermal modeling to account for temperature-rise in the device due to local-power-dissipation. The presence of field-plates further complicates the charge-distribution-picture due to voltage distribution within the device among FPs which affect the charge-partitioning of individual FP-charges.

The next few sections describe the relevant measurements required to validate the MVSG-model and extract relevant parameters for HV-circuit applications. Device-characteristics that are calibrated against the MVSG-model includes the DC-current-characteristics and extraction followed by charge-(capacitance) modeling, extraction of temperature-dependent coefficients and the incorporation of current-collapse to model dynamic R_{dson}.

5.2 Terminal-current benchmarking

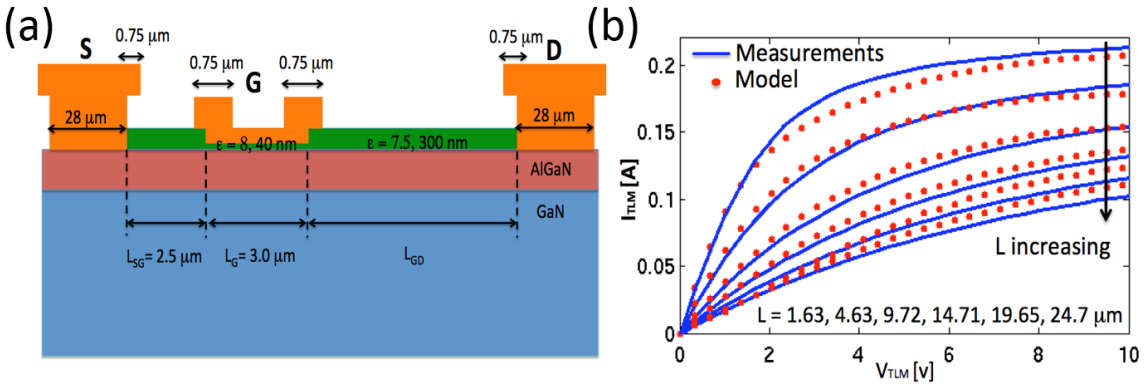


Figure 5-3: (a) The cross-section schematic of Fujitsu HV-GaN-HEMT showing key geometry parameters: $L_g = 3\ \mu m$, $L_{gs} = 2.5\ \mu m$ and $L_{gd} = 9.5\ \mu m$. (b) The implicit-gate-transistor-model for the access regions is validated by comparison against ungated -TLM structures. For the fits shown, no parameter other than the length of the TLM structure (L_{TLM}) was varied. Ideally TLMs should behave as simple resistors but the observed non-linear behavior is due to both pinch-off and velocity-saturation.

The terminal-current characteristics of HV-GaN-HEMTs are measured using on-wafer 4-probe-method (Kelvin-method) in a DC-probe-station using Agilent B1505A power-device analyzer. The measured room-temperature terminal-drain characteristics are compared against the MVSG model for various bias-points spanning moderate-to-strong accumulation, linear-to-saturation regimes. Validations of the MVSG model against three HV-devices are shown in this section of the thesis: (i) Fujitsu Laboratories LTD. non-field-plated devices (ii) Two devices fabricated at MIT that have a GFP and a SFP each (iii) a Toshiba Semiconductor HV-device that has both a GFP and a SFP.

The first set of measurements pertain to non-FP GaN-HEMTs from Fujitsu which have gate-length: $L_g = 3\ \mu m$ which is long-enough to sustain non-velocity-saturation transport-regime in the device-channel. The key geometry parameters are presented along with the device cross-section schematic in Fig.5-3(a) and further details can be found in [60]. The first step in characterizing the drain-current model is to extract the access-region implicit-transistor parameters from fits to gateless-TLM current-characteristics which are shown in Fig.5-3(b) for different lengths spanning from

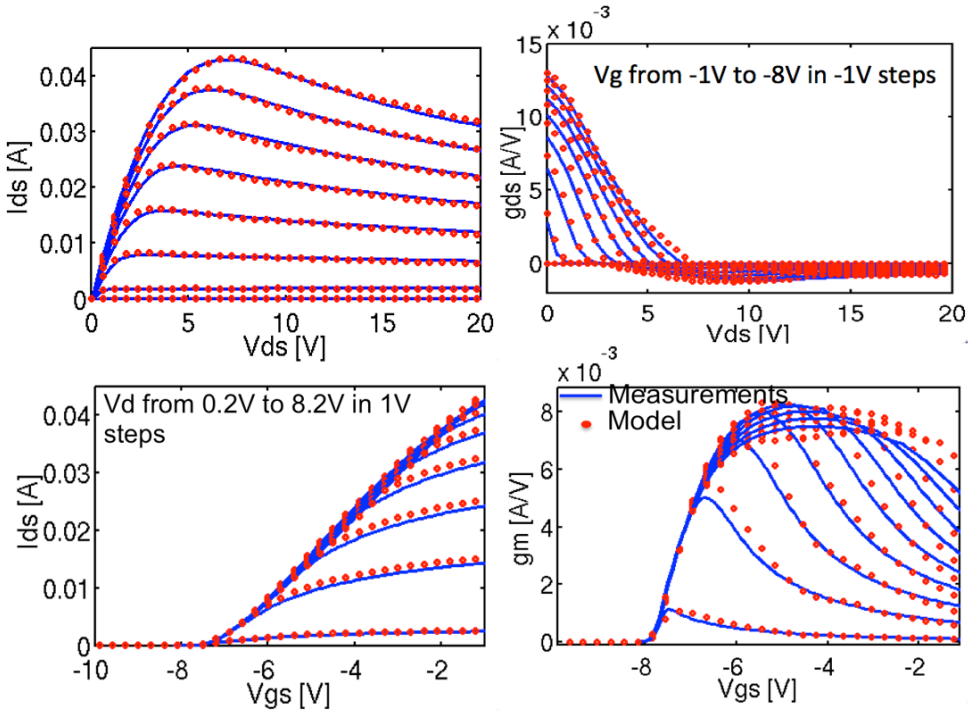


Figure 5-4: (a) Output I-Vs, (b) output-conductance, (c) transfer I-Vs and (d) transconductance plots of $L_g = 3\ \mu m$ and $L_{gd} = 9.5\ \mu m$ device. Good agreement is achieved between the model (curves) and measurement (circles). Device courtesy: Fujitsu.

2 μm-to-25 μm which show good match of the implict-gate-transistor model for these length-scales where mobility-dependent transport is dominant and current saturation is primarily due to pinch-off under high-lateral-fields at high V_{TLM}. The extracted implicit-transistor parameters such as C_{Ig} are then used in the model for source- and drain-access-regions of the gated-HEMT whose terminal current-characteristics along with its derivatives (g_m and g_{ds}) are measured and compared against the model in Fig.5-4. The output-characteristics in Fig.5-4(a) show significant droop at high V_{DS} due to device-self-heating which results in the negative-output-conductance in saturation in (b). The V_T of the device is $-7\ V$ evident from the transfer-characteristics. The transconductance, g_m, fits are shown illustrating the accurate estimation of peak-g_m around $V_G = -5\ V$ by the MVSG model and degradation in g_m at V_G beyond this point due to de-biasing of the main device as voltage drop in the access-regions increases, which is captured in the MVSG model. The list of relevant- parameters

used for the model-fits shown above are given in Table.5.1.

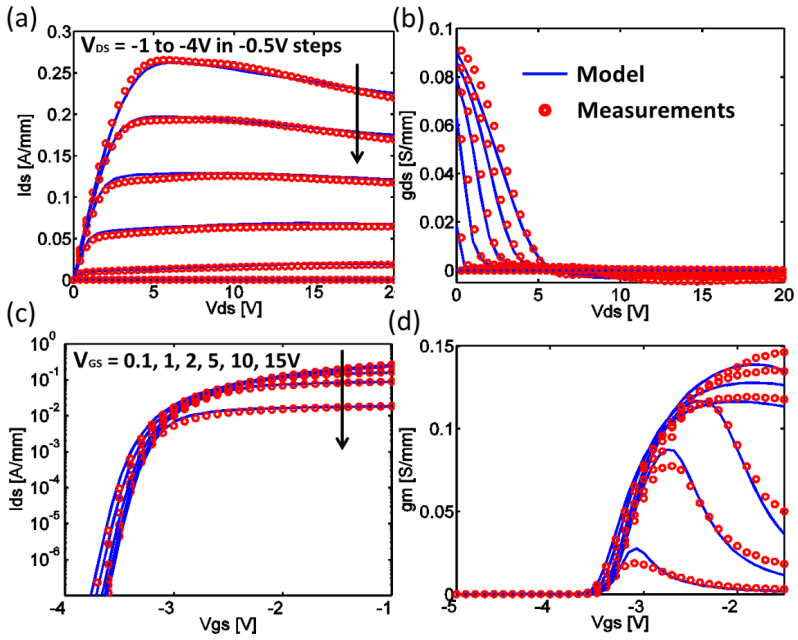


Figure 5-5: The device fits for a source-connected field plated device with L_g = 2 μm and L_{gd} = 16 μm and L_{sfp} = 6 μm. The above fits were obtained using the same set of parameters used for the non-field-plated-device shown in [51] along with additional FP-transistor parameters namely: The gate-capacitance of source-field-plate-transistor (C_{gsfp}) and its threshold-voltage (V_{Tsfp}) which are extracted though independent measurements. Device courtesy: Daniel Piedra, MIT.

Next, the terminal-currents of HV-device that employs a single-FP of each kind (a GFP-device and a SFP-device) fabricated at MIT (by Daniel Piedra, MIT) are measured and compared against the MVSG model which includes these FP-elements with relevant FP-transistors in the sub-circuit shown in Fig.4-5(c) [51]. The implicit-gate model is compared against TLM structures as explained above, on structures that are fabricated on the same die as the gated-devices. The parameters used to fit the TLM IV-curves are then used in the model to calibrate against non-FP-device in the technology, and gives good match with measurements as shown in [51]. The field plated version of the model is compared against source- and gate-connected field-plated devices (the schematic shown in Fig. 5 of [51]) on the same die. The fits are shown in Figs.5-5 and 5-6 and show accurate estimation of the currents and derivatives with measurements employing the same set of parameters that were used for the fits of TLMs and non-FP-FETs. For the FP-regions the areal-gate-capacitances and

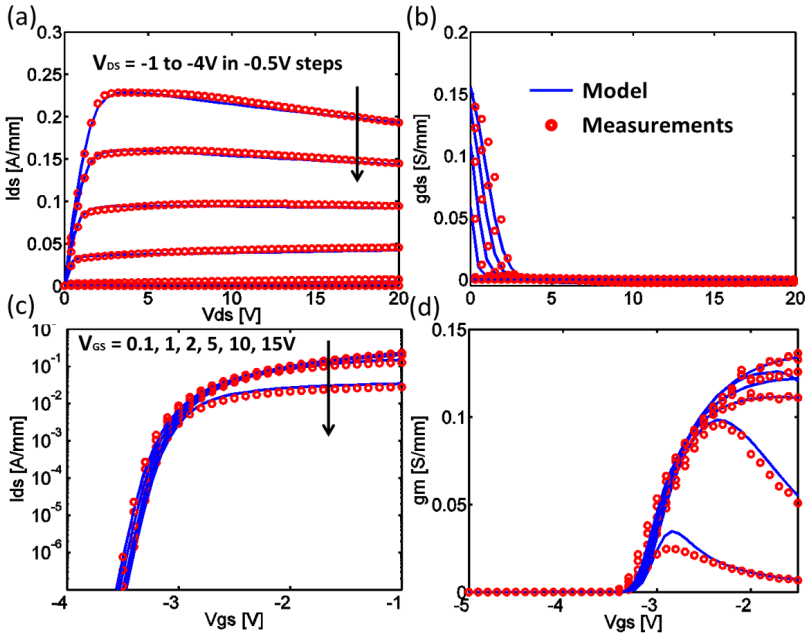


Figure 5-6: The device fits for a gate-connected field-plated device fabricated at MIT with $L_g = 2\ \mu m$, $L_{gd} = 16\ \mu m$ and $L_{gfp} = 3\ \mu m$. The gate capacitance of gate-field-plate-transistor (C_{ggfp}) and its threshold-voltage (V_{Tgfp}) are the additional parameters. Device courtesy: Daniel Piedra, MIT.

threshold-voltages are extracted from measuring the CVs of ring-capacitors fabricated on the same-die as shown in Fig.3-11. FPs not only change the BV but also affect the R_{on} as can be seen from the output-conductance (g_{ds}) plots in the figures. The FP-transistors in the sub-circuit modeling approach in the MVSG model are able to match the change in R_{on} with L_{ggfp} and L_{gsfp} for the same $L_{gd} = 16\ \mu m$ in these devices. The list of relevant- parameters used for the model-fits shown above are given in Table.5.2.

Finally the MVSG-model-sub-circuit shown in Fig.4-5(c) that employs one-GFP and one-SFP is validated against Toshiba-HV-device with $L_g = 1\ \mu m$, $L_{gs} = 2\ \mu m$, $L_{gd} = 14\ \mu m$, $L_{ggfp} = 3.5\ \mu m$, and $L_{gsfp} = 7\ \mu m$. The device-characteristics in both forward-mode ($V_{DS} > 0\ V$) and reverse-mode ($V_{DS} < 0\ V$) are compared against the model for realistic-HV-circuit applications. The absence of PN-junctions between source/drain and the body in GaN-HEMTs results in the reverse-mode-characteristics as shown in Fig.5-7. The resulting significant reverse-mode currents with low R_{on} in reverse-mode enable GaN-HEMTs to sustain the inductor-current in one of the

switching-half-cycles in converter-circuits without requiring a parallel diode connection to the HEMT (the free-wheeling diode). The added advantage is the absence of reverse-recovery-charge associated with the free-wheeling diode. Since in practical circuits, HV-HEMTs when in reverse-mode in are operating in the linear-region, the validations shown in output-currents and output-conductance in reverse-mode as shown in Fig.5-7(e)-(f) are relevant. In the forward-mode output-characteristics as before, significant device-heating can be observed that results in droop in the current-characteristics in the saturation-regime in Fig.5-7(a), and in the associated negative-output-conductance in Fig.5-7(b). Also seen from Fig.5-7(d) is the non-linear g_m at high-V_{GS} due to the access-region and FP-region debiasing. The model-calibration-procedure is identical to that explained for the previous sets of fits and can be found in [61] while the parameter list used for the fits is given in Table.5.3.

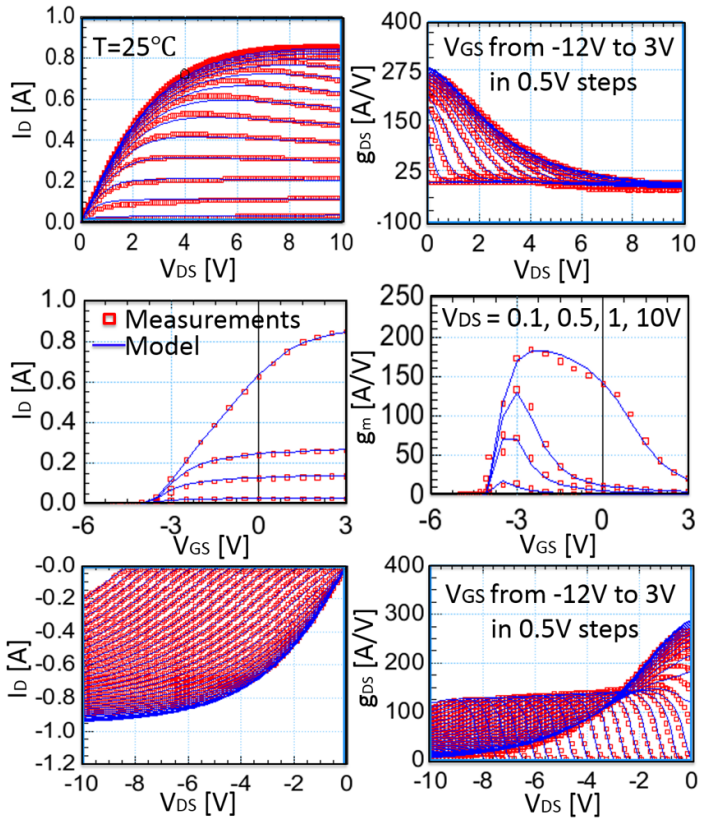


Figure 5-7: (a) The output I-Vs, (b) output-conductance, (c) transfer I-Vs, (d) transconductance, (e) reverse-mode output I-Vs and (f) output-conductance plots shown comparing the MVSG model against Toshiba device data. The model captures linear-to-saturation, depletion-to-accumulation conditions accurately in both forward- and reverse-modes. Self-heating in the device is captured as well [61].

5.3 Terminal-capacitance and charge characterization and benchmarking

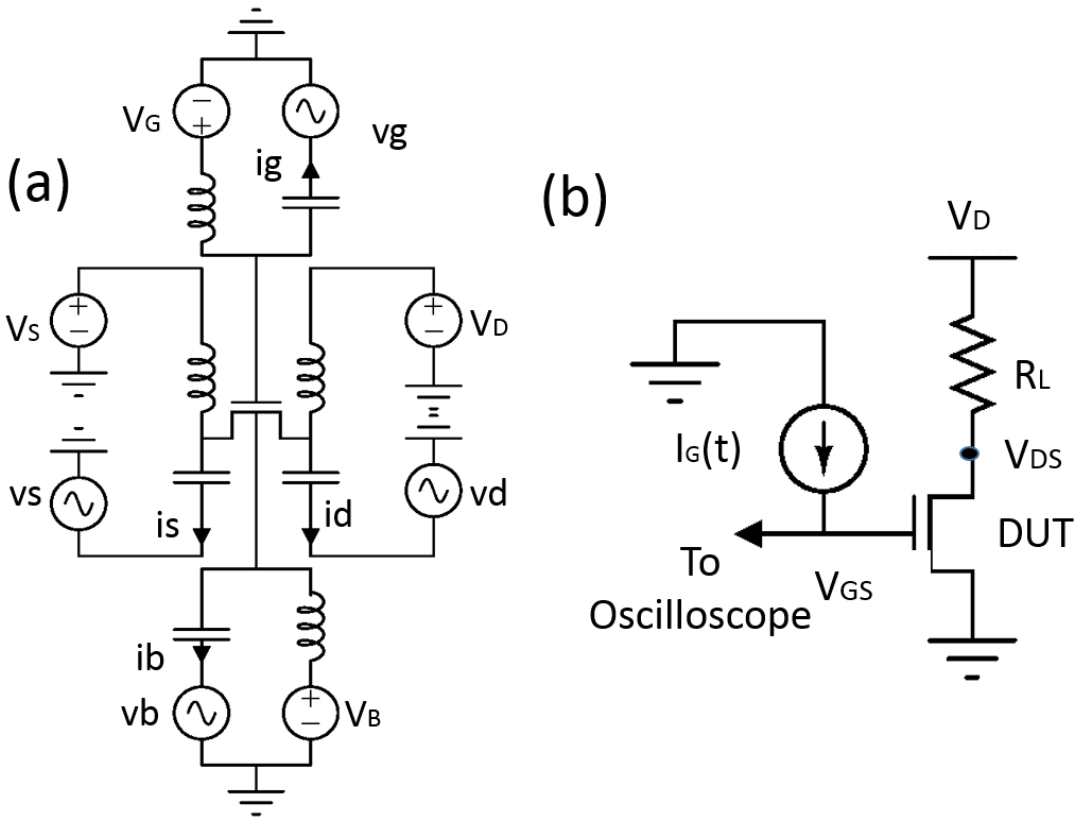


Figure 5-8: (a) The circuit-setup to measure the complete set of terminal-capacitances as a function of bias. The DC-choke and AC-capacitances are part of the commercial bias-Tees that are connected to each terminal to isolate the DC bias from the small-signal AC-current through any terminal in response to an AC-excitation voltage in one-of the terminals. (b) The setup to extract the gate-charge (Q_G) as a function of V_{GS} as described in [62]. The gate-current is applied through a current-source in pulsed-mode and the change in V_{GS} and V_{DS} as a function of time is recorded in the oscilloscope.

The MVSG-model that is calibrated against terminal-current measurements as discussed in the previous section is able to model the terminal-charges and capacitances due to the self-consistent transport and electrostatic approach adopted in MVSG-model. The low-frequency terminal CV-measurements are done using the setup shown in Fig.5-8(a) in which the DC-bias to each terminal (including DC-

ground) is applied through the DC-choke and the AC-excitation-voltage is applied through the AC-coupling capacitance (both of whose values are large enough to not affect measurements at the frequency of interest). Each capacitance $C_{ij} = \frac{1}{\omega} imag\left(\frac{\delta i_i}{\delta v_j}\right)$ can then be measured yielding a total of 9 independent capacitances (less than 16 due to charge-conservation).The measurements are also done using the Agilent B1505A capacitance-measurement-unit (CMU) (with proper open and phase calibration) and the resulting capacitances are compared against the CV-simulations using the MVSG-model.

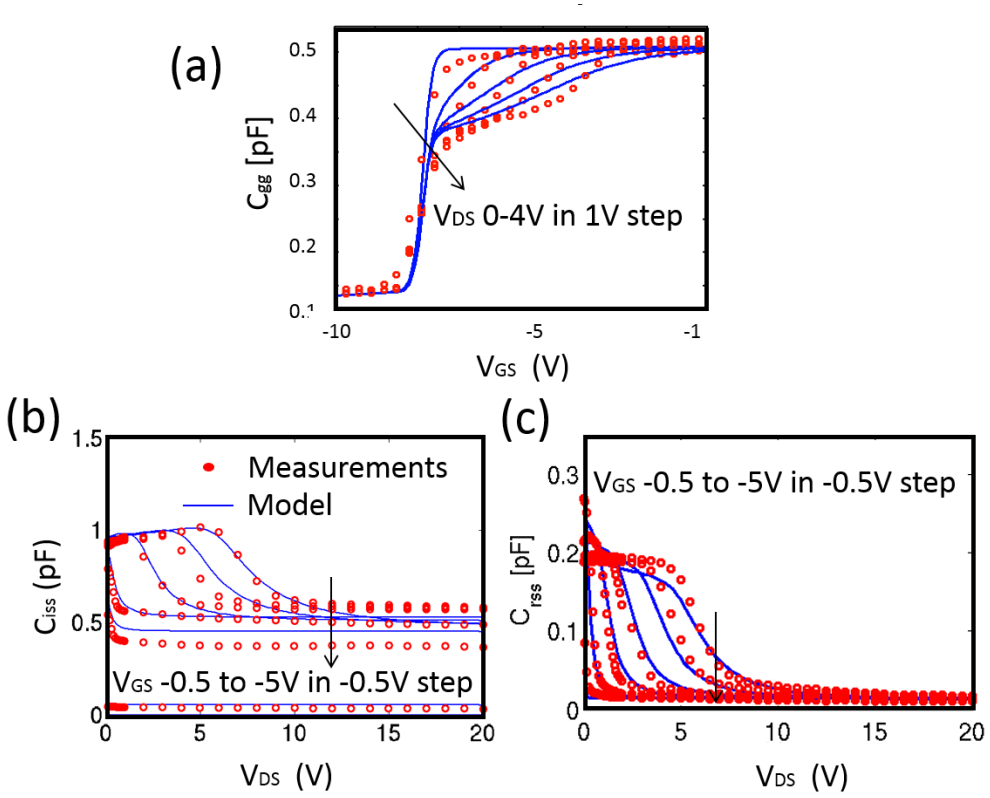


Figure 5-9: (a) The input-capacitance (C_{gg} or C_{iss}) plotted as a function of the applied V_{GS} for different V_{DS} spanning linear-to-saturation and off-to-on-state of the Fujitsu-device. (b) The input-capacitance (C_{iss}) as a function of V_{DS} for different V_{GS} for devices fabricated at MIT compared against the MVSG-model simulations. (c) The reverse-transfer-capacitance (C_{rss}) as a function of V_{DS} for different V_{GS} for the MIT-device compared against MVSG-model. The off-state fringing capacitances are extracted and used as fitting parameters in the model.

The input capacitance $C_{iss} = C_{gg} = \frac{1}{\omega} imag\left(\frac{\delta i_g}{\delta v_g}\right)$ and reverse-transfer-capacitance $C_{rss} = C_{gd} = \frac{1}{\omega} imag\left(\frac{\delta i_g}{\delta v_d}\right)$ are shown for both (i) Fujitsu and (ii) MIT-devices are shown in Fig.5-9 where the CV-measurements are compared against simulations with

the MVSG model calibrated against the IV-data on both devices (using the parameter sets in Tables. 5.1 and 5.2 respectively). As can be seen, the model matches the measured data in the entire V_{GS} and V_{DS} bias-regimes. In (a) the turn-on of the device and the formation of the channel yields a rise in the capacitance of the device at $V_{GS} = V_T$ which is about $-7\ V$ for the Fujitsu-device. In (b) and (c) the reduction in the C_{iss} and C_{rss} for $V_{DS} > V_{DSAT}$ in the saturation-regime due to the reduction in C_{gd} of the channel is consistent with the traditional charge-distribution theory in MOSFETs [47] and is correctly captured in the MVSG-model.

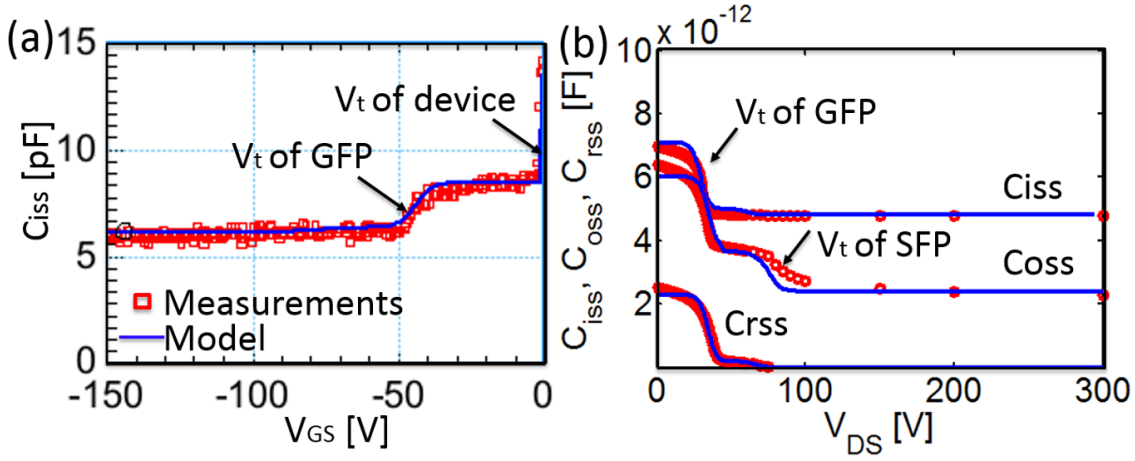


Figure 5-10: (a) C_{iss} vs. V_{GS} showing the transitions due to threshold voltage of the GFP and intrinsic-gate (b) C_{iss}, C_{oss} and C_{rss} vs. V_{DS} in off-state show all the non-linear transitions due to pinch-off of the different transistor-elements in the device at different V_{DS} and are captured by the distributed-charge-model in MVSG.

The capacitance-measurements of the Toshiba-HV-GaN-HEMTs that have a GFP- and an SFP-transistor element in the device-design are shown in Fig.5-10 compared against the MVSG model calibrated against device-IVs using the parameters in Table.5.3. The C_{iss} vs. V_{GS} plot in (a) shows two transitions in the CV corresponding to the V_Ts of the GFP ($V_{Tgfp} = -50\ V$) and intrinsic-gate ($V_T = -4\ V$) and the MVSG-model is able to capture these transitions due to the distributed charge-modeling approach shown in Fig4-5(c). The off-state C_{iss}, C_{oss} and C_{rss} plots in the off-state vs. V_{DS} also show transitions in CV-characteristics at the $V_{Tgfp} = -50\ V$ and $V_{Tsfp} = -100\ V$ due to the distributed channel and cross-coupled-charges in the MVSG-model. The distributed-charge model can capture the non-quasi-statc

(NQS) effects under dynamic-large-signal switching-applications as will be discussed in subsequent chapters.

A second approach to validate the charge model for any HV-device is using gate-charge measurements with the measurement setup highlighted in Fig.5-8(b). In this setup the device-under-test (DUT) is connected to a drain-load-resistance and the gate is connected to a pulsed-current-source that can inject a determined amount of current as a function of time to yield a known amount of charge on the gate-electrode vs. time which is distributed among the device-capacitances associated with the gate-terminal. As the gate-current is applied, the resulting rise in the gate-node-voltage is measured using an oscilloscope.

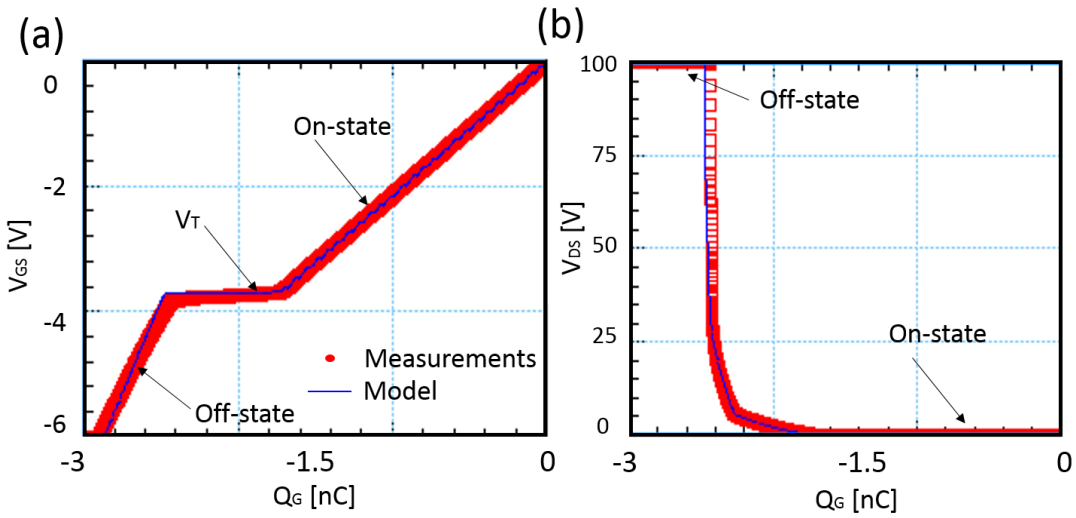


Figure 5-11: (a) V_{GS} vs. Q_G plot in which the drain supply voltage of 100 V is applied to the device through load-resistance. As the gate-current-source is applied, the gate-charge collected by the off-state gate-capacitance increases the V_{GS} eventually turning the device-on. At $V_{GS} = V_T$ the rise in the gate-charge is due to the falling V_{DS} across the device as it is pushed into the on-state-linear-regime and the resulting plateau is the integral of $C_{gd}dV_{DS}/dt$. Thereafter the rise in the gate-voltage is caused by on-state gate-capacitance. (b) The corresponding V_{DS} across the device is plotted showing the fall in V_{DS} as the device turns-on which eventually reaches the linear on-state value determined by the R_{on} of the device. Measurement approach details are based on [62].

The measured gate-voltage plotted as a function of gate-charge ($Q_G = I_G t$) is shown for a wide MIT-device in fig.5-11(a) indicating three-regions. Initially the device is off and sustains the full applied $V_{DD} = 100\ V$ and the rise of V_{GS} is determined by the off-state gate-capacitance, which is the slope of the V_{GS} vs. Q_G plot in (a)

in the off-state. As the V_{GS} eventually reaches the V_T of the device, it turns on the gate and causes the V_{DS} to drop as can be seen in Fig.5-11(b) at $V_{GS} = -2.7\ V$. The plateau at V_T seen in (a) is due to the gate displacement current that results from the drop in V_{DS} through C_{GD} of the device. After the device is pushed into the on-state-linear-region, V_{DS} drops to the on-value in (b) and the V_{GS} rises at a rate determined by the on-state-capacitance of the device. The gate-charge measurements are another way to calibrate the gate-charge component of MVSG-model and test the accuracy of CV-measurements.

5.4 Thermal-model validation

HV-GaN-HEMTs used as HV-switches in converters typically have wide total-width (often in the mm range) to reduce the R_{on} and hence static-power-losses. This means that the power dissipation under hard-switching conditions is significant during switching-transitions resulting in significant self-heating. The thermal model in the MVSG model described in the last chapter models this effect using an RC time-constant and captures the degradation in the transport parameters in the device causing degraded terminal-current characteristics. In addition, HV-applications require the operation of the converter-circuit at a range of ambient temperatures which may typically vary from 0 °C to 150 °C and the temperature coefficients of key transport parameters extracted using a couple of temperature measurements must be able to determine the device-behavior over this entire temperature-range.

The thermal module in the MVSG model is tested against terminal-IV measurements of wide devices from Toshiba, taken at different ambient temperatures in this range shown in Figs.5-12-5-16. Four different temperatures in the range are chosen and the device-model-fits are compared against measurements (The measurements are similar to the DC-measurements except the temperature of the chuck on which the DUT is placed is now controlled using a temperature controller) as seen in the figures. The temperature-coefficients for mobility and velocity of carriers are extracted from 0 °C and 25 °C and the model is then capable of estimating the device-behavior accurately for the other temperatures as can be seen.

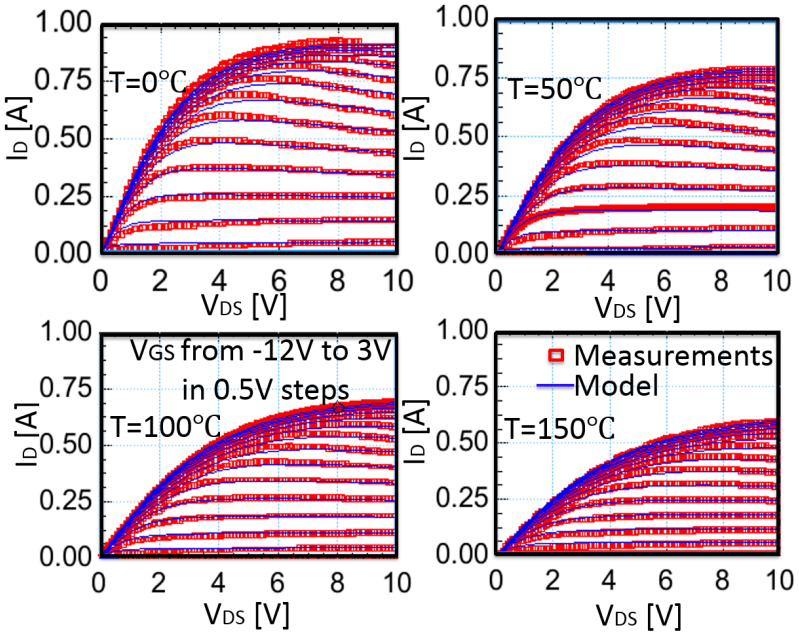


Figure 5-12: The thermal modeling accuracy can be seen from the fits to output-curves at temperatures from 0 °C to 150 °C. The on-conductance and currents reduce with temperature and are modelled well using the temperature dependent equations for μ and v_{x0} (equations (4.30)-(4.33)) with the temperature-coefficients extracted from 0 °C and 25 °C.

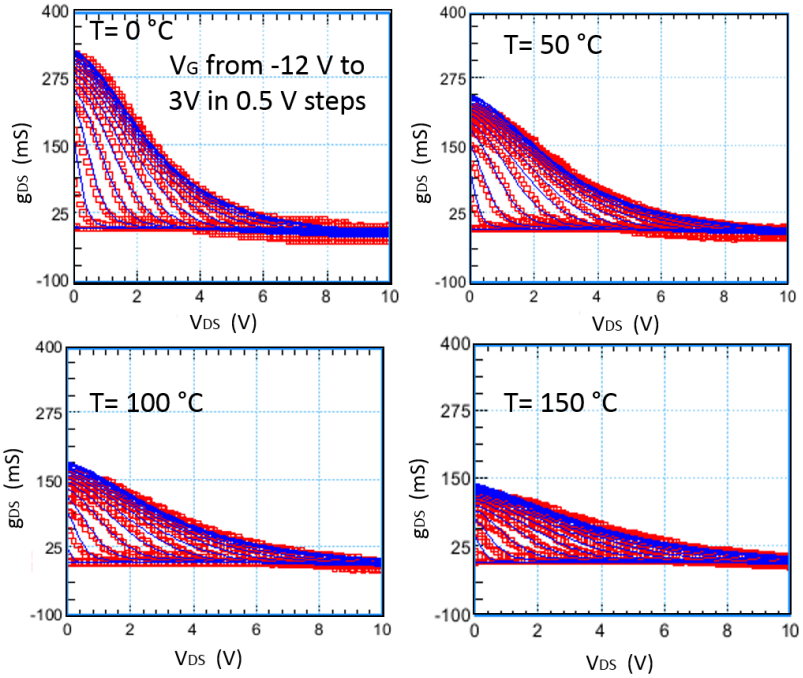


Figure 5-13: The corresponding output-conductance characteristics are shown for different temperates depicting the increase in R_{on} and increase in negative-output-conductance with temperature.

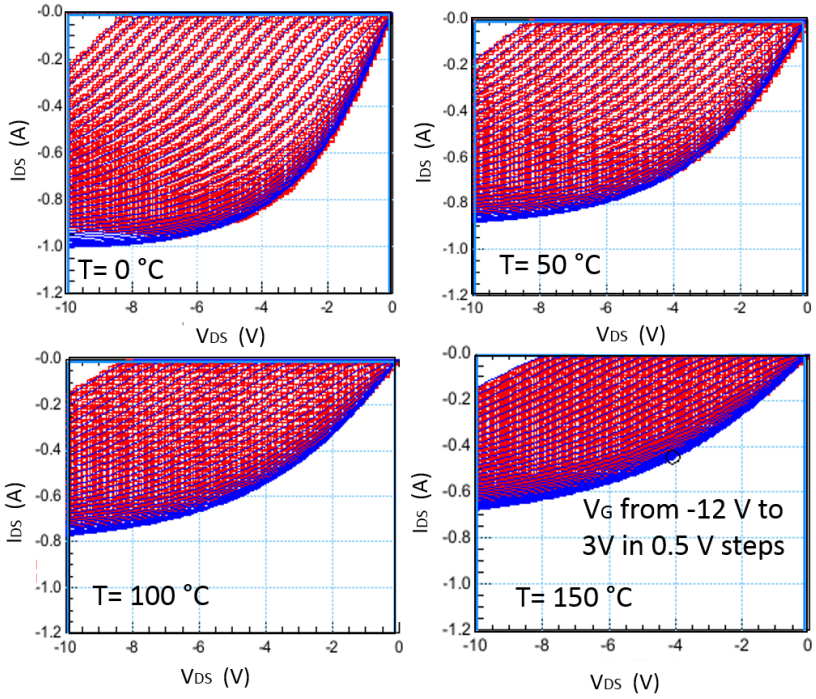


Figure 5-14: The reverse-mode currents exhibit a significant reduction in saturated-currents and on-resistance along with a shift in the turn-on voltage due to V_T shift with temperature.

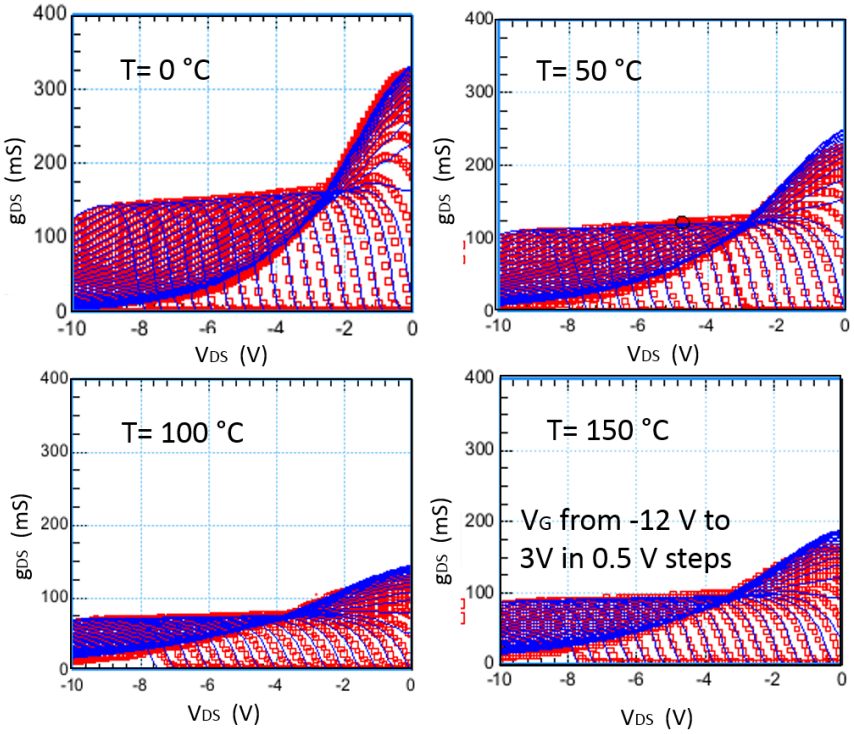


Figure 5-15: The corresponding output-conductance plots show consistent reduction in conductance and shifts in V_T with temperature.

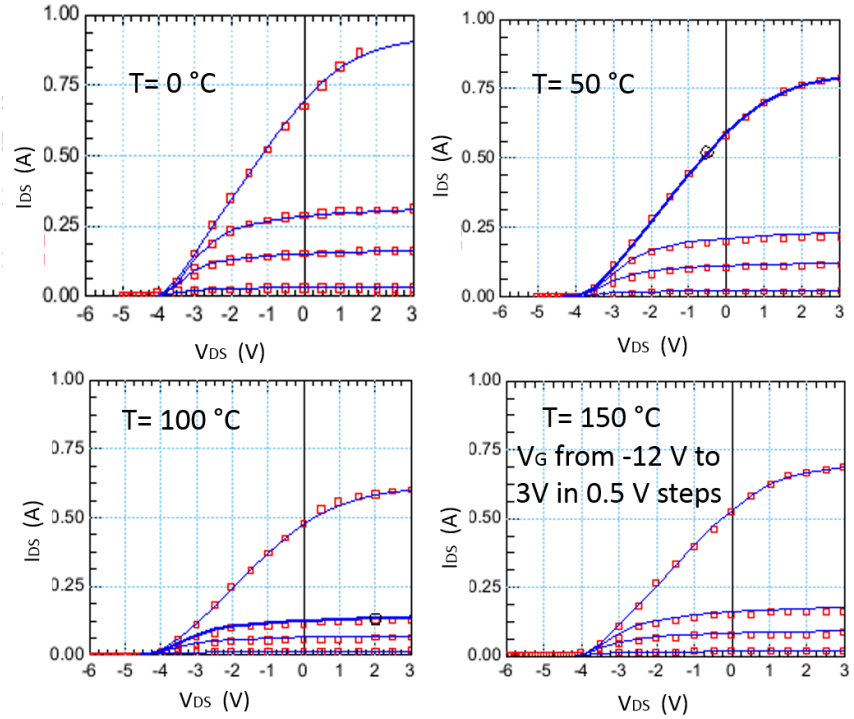


Figure 5-16: Transfer-characteristics exhibit a reduction in on-currents and negative-shift in V_T with temperature which is accurately captured in the MVSG-model.

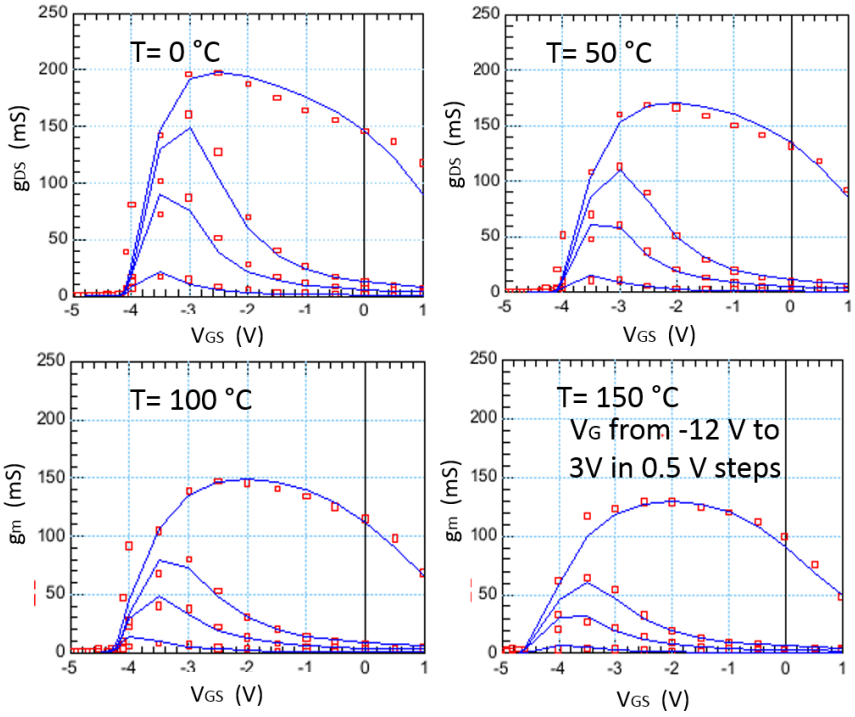


Figure 5-17: The transconductance g_m showing reduction at elevated temperature thereby decreasing the intrinsic-gain of the device.

The increase in R_{on} in both forward-and reverse-modes that causes the decrease in on-currents in the device are captured in MVSG-model. The electrostatic-parameter such as V_T shift with temperature and are incorporated as seen from the transfer-curve-fits. In addition to benchmarking the temperature-dependence of key transport parameters from the temperature-dependent IV-measurements, CV-measurements are made at different device temperatures and are shown in Fig.5-18 showing significant shifts in V_T of the different transistor-elements of the device especially the FP-V_T which is modeled by the temperature-dependence of V_T model explained in the last chapter. There is no significant change in the capacitance values themselves as the 2DEG-charge as well as its location are not affected heavily by temperature. Along with V_T, the SS of the device also changes with temperature resulting in degraded swing at elevated temperatures and is included in the MVSG model.

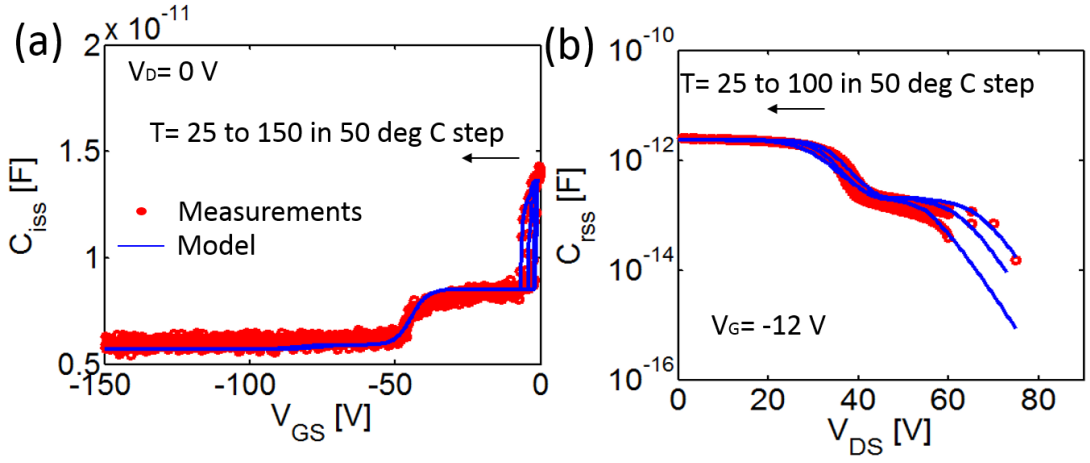


Figure 5-18: (a) C_{iss} vs. V_{GS} at different temperatures showing the shift in the capacitance-transitions due to shift in the $GFP - V_T$ and intrinsic-V_T (b) Plots of C_{rss} vs. V_{DS} at different T in the off-state show the V_T-shifts but more prominently the degraded SS of each-transistor element which are captured by the distributed-charge-model in MVSG.

The model-validation illustrated so far demonstrates the ability of MVSG-model to accurately describe HV-GaN-HEMT-behavior in HV-circuit applications. However GaN is still a newly-emergent technology and has a few non-idealities such as current-collapse as described earlier, that are currently being tackled and it is uncertain as to what extent they can be mitigated (if not completely eliminated) in practical

devices. Hence it becomes imperative to include these effects in the model, albeit in an empirical fashion as shown in the last chapter and the validation of this effect is discussed in the next section.

5.5 current-collapse: characterization and validation

The current-collapse phenomenon was presented in chapter 3 in detail along with a discussion of the plausible causes for the origin of this effect and in chapter 4, two approaches were formulated that capture this effect empirically: (i) By increasing the R_{sh} of drain-access-region dynamically under large-signal switching conditions and,(ii) by shifting the V_T dynamically under similar stress-conditions. In this section, characterization of dynamic-current-collapse is explained along with the validation of the empirical methodology adopted in MVSG-model to capture this effect.

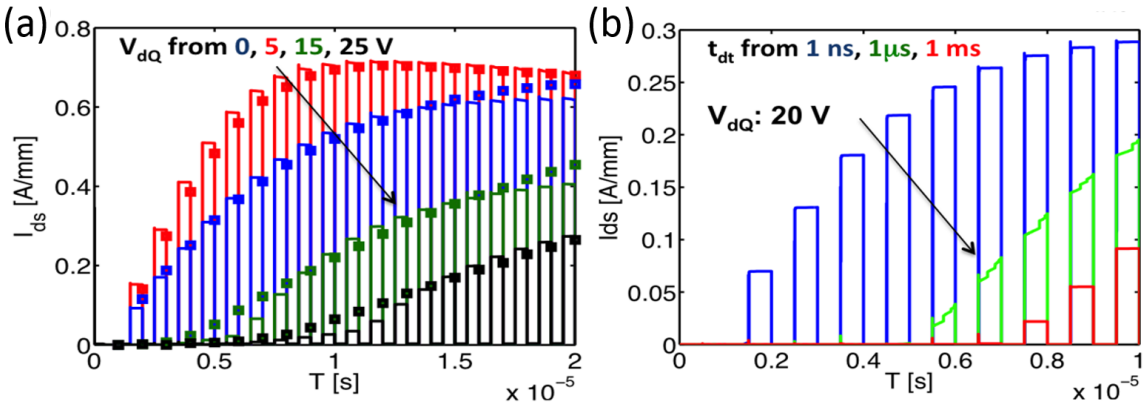


Figure 5-19: (a) The model results (lines) are compared against pulsed-IV measurements (data points) for different V_{DQ} as in Fig.3-11(a) and shows similar behavior as measurements. (b) The effect of de-trapping lifetime (τ_{DT}) on I_{on} is shown using the model as proof-of-concept using the simple $RC(=\tau_{DT})$ network. The Model is not calibrated, as measurements of fabricated devices do not show significant lifetime dependencies for pulse widths from 500 ns to 10 μs indicating larger τ_{DT}. The model can demonstrate significant increase in R_{on} with τ_{DT} which is typically observed [51].

In chapter 3, Fig.3-11 shows the measured pulsed-IV characteristics of MOS-HEMTs fabricated at MIT, without post-gate SiN passivation (but with 20 nm Al_2O_3 gate-oxide covering the access regions) obtained with an Auriga-4750 system and the effect of drain (V_{DQ}) and gate (V_{GQ}) off-state stress-voltages on the on-state-current

are observed with the currents exhibiting $knee - walkout$ resulting in increasing R_{on} and reduced I_{on}. In this section, the charge-trapping-module-(i) (which was discussed in chapter 4.10) in the MVSG model is activated and the Auriga-pulse system measurement is simulated in Spectre. The model with the R_{sh} of drain-access-region changed dynamically exhibits $knee - walkout$ behavior with stress voltages, which matches well with measurements as can be seen from Fig.5-19(a). Since complete de-trapping effects cannot be seen from pulsed-IV measurements between 500 ns to 10 μs, the effect is shown using the model with a time-constant (τ_{DT}) of 100 μs. Other key parameters for the fits are given in Table. 5.2. In Fig.5-19(b), the impact of the value of de-trapping-time-constant (τ_{DT}) on the current-collapse behavior is observed for pulsed-switching with period of 500 ns. If $\tau_{DT} = 1$ ns then the charges are completely de-trapped from the trap-states, thus completely removing the current-collapse-effect during 500 ns switching but as the τ_{DT} is increased, significant $knee - walk - out$ is observed for 500 ns switching.

Another approach to characterize the effect of current-collapse is to use a switching-circuit shown in Fig.5-20(a). Since the dynamic $knee - walkout$ effect increases the device R_{on} and knee-voltage (V_K) from its DC-value during switching, the effect is characterized by the pulsed measurement setup shown using the metric, $V_{ratio} = V_{k,switching}/V_{k,DC}$. In the circuit-setup, the gate of the DUT is pulsed from off-to-on-state at different-frequencies spanning $1 - 10$ KHz while the drain is connected through R_L with the rail-voltage determining the V_{DQ} stress-voltage in the off-state. The knee-voltage across the DUT just after the gate-turn-on is measured using the zener-diode and the quantity V_{ratio} is measured at various conditions: (i) temperatures of 25 °C- 100 °C (ii) frequencies of $1 - 10$ KHz with V_{DQ} of $100 - 320$ V. The DUT is the Fujitsu HV-GaN-HEMT whose IV- and CV-characteristics were used to calibrate the MVSG-model (parameter set in Table.5.3). The V_{ratio} of these industry devices increases from 1 at DC up to 3 at V_{DQ} of 320 V along with breakdown at higher temperature of 100 °C, indicating significant collapse which is estimated reasonably in the MVSG model as shown in Fig.5-20(b)-(d).

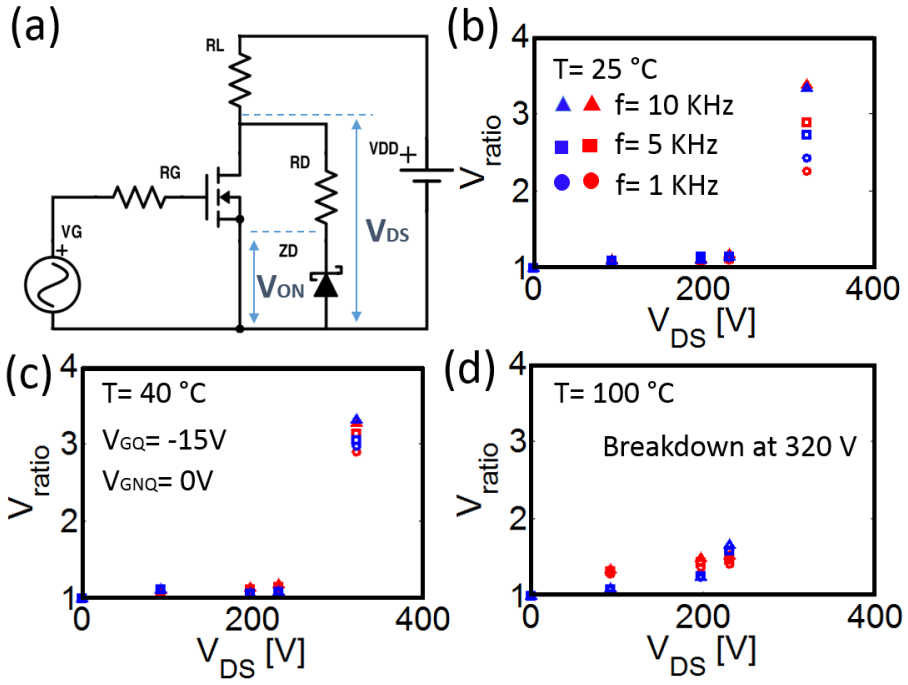


Figure 5-20: (a) The switching circuit used to characterize $knee - walkout$ in the devices as a function of stress-V_{DQ}, temperature and switching frequency. (b)-(d) The extent of $knee - walkout$ is characterized by V_{ratio}, measured at temperatures of 25, 40 and 100 °C, at V_{DQ} of 100, 200, 230, 320 V and at frequencies of 1, 5, 10 KHz. $Vratio = 1$ under no-stress, indicating absence of collapse and increases with V_{DQ}, temperature and frequency and is captured by the MVSG model. $Vratio \approx 3$ at $V_{DQ} = 320\ V$, indicating severe collapse and the devices breakdown at 100 °C at this V_{DQ} even though their rated $DC - BV$ is 600 V, highlighting the significance of knee-walkout in HV-switching [61].

This concludes the MVSG-model validation for HV-application-regime that takes into account static, dynamic and non-quasi-static effects of a HV-GaN-HEMT in switching-converter applications. Thermal and charge-trapping-effects are also included to aid realistic circuit effects and are explained in chapter 8. In the next part of this chapter, model validation against device-level measurements relevant to RF-circuit-design are discussed.

5.6 Modeling requisites for RF-circuit design

Typical high-frequency circuits that employ GaN-devices are the transceiver-circuits operating in the range of 1 GHz to 150 GHz with components such as power-

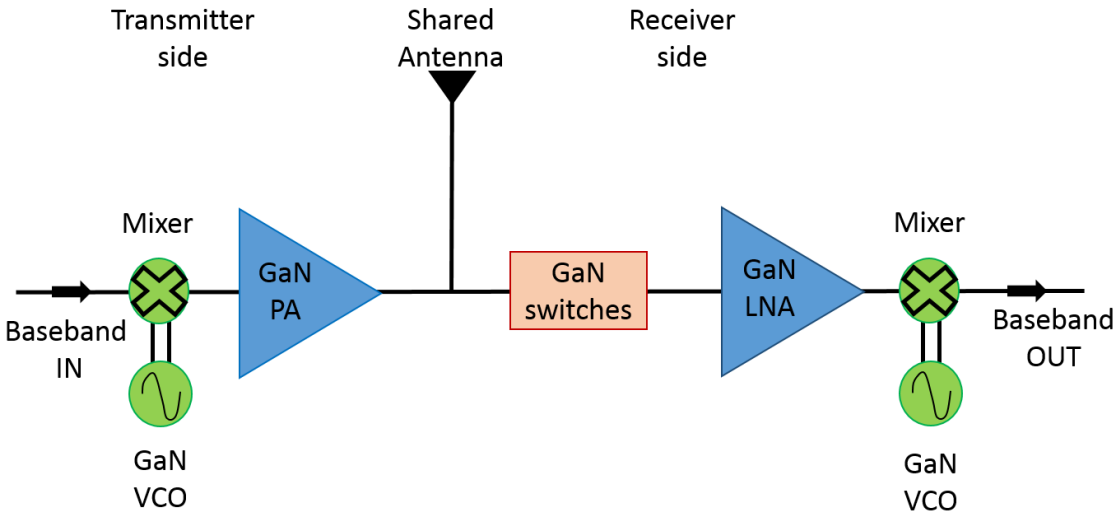


Figure 5-21: Schematic of a an integrated GaN-based RF-transceiver front-end stage that shares a common antenna between transmitter- and receiver-side. The transmitter components such as VCO, PA employ GaN-HEMTs while on the receiver-side, LNA and VCO have GaN-HEMTs in their circuit-elements. In addition, the isolation switches between transmitter-and receiver-side due to the shared antenna are also built using GaN-HEMTs. Accurate models for GaN-HEMTs present in each of these components is critical and a part of this thesis.

amplifiers (PA) at the transmitter-stage, low-noise-amplifier (LNA), voltage-controlled oscillators (VCO) at the receiver-stage and RF-GaN switches for isolation between RF-components. The schematic of a RF-transceiver stage is shown in Fig.5-21 which highlights the various RF-components that can employ GaN-HEMTs. Design of each of these components using GaN-technology imposes challenges to non-linear GaN-device-models. On the transmitter-side, the key requirement is to capture the various PA-device non-linearities that impact the onset of power-compression and to model higher-order current- and charge-derivatives (minimum of 3) to capture inter-modulation-distortions (IMD). As shown in Fig.5-22(a) the load-line for a typical class-A PA spans the off-to-on-state of the device ranging from sub-threshold-to-saturation-to-linear regimes hitting current-compression at both-ends forcing more stringent requirements on the model than for power-applications. On the receiver-side, the LNA-circuit requires accurate noise-figure estimate along with the modeling of small-signal S-parameters for source-impedance-matching at the quiescent-point as shown in Fig.5-22(b), while the VCO-circuit requires large- and small-signal-modeling

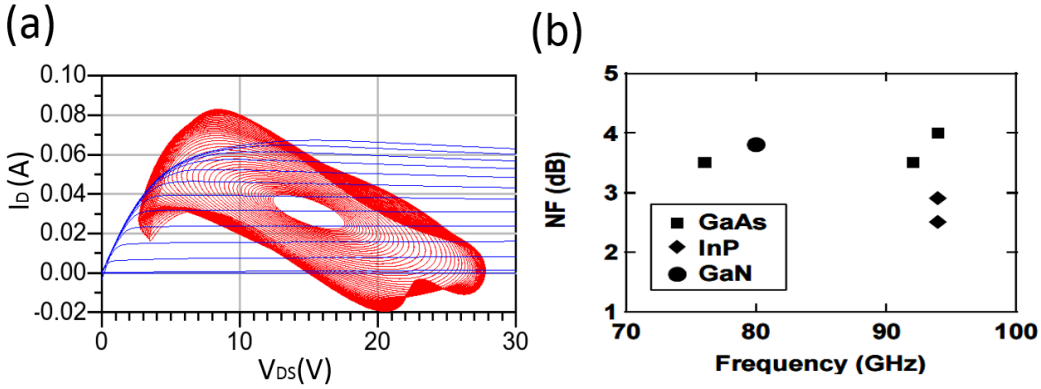


Figure 5-22: (a) Typical load-line contours spanning the IV safe-operating-area (SOA) of the GaN-HEMT for a typical power-amplifier. Each contour corresponds to one input-power (P_{in}) value and the load-current includes both DC- and device-capacitive-currents. (b) The noise-figure (NF) metrics of receiver-LNA for W-band application showing comparable performance of GaN with other GaAs-based technologies [63]. Compact-models are required to estimate the NF accurately as a function of bias and frequency for a range of RF-applications.

and low-frequency phase-noise characteristics of the device.

The MVSG-model calibration and benchmarking against various device-level measurements to meet these circuit demands are highlighted in the following section. Starting with the I-V characterization of scaled gate-length devices suitable for RF-applications, the S-parameter validation, large-signal load- and source-pull, power-sweep, linearity, noise-figure and phase-noise validation of GaN devices using the model will be described.

5.7 Drain-current benchmarking

The process of extracting the MVSG-model for a device targeted for RF-applications starts with the model-calibration against DC-current characteristics similar to the extraction-flow for the HV-application domain. The validation of MVSG-model in this thesis is done against three types of RF-devices: (i) Devices fabricated at MIT with gate-lengths: $L_g = 42\ nm$ and $L_g = 105\ nm$ (ii) industrial-RF-devices from Qorvo Inc. and (iii) industrial-RF-devices from Wolfspeed^{TM} (Cree Inc.) with $L_g = 250\ nm$.

The calibration of the DC terminal-current model starts with the modeling of access-region to extract parameters such as C_{Ig} of implict-gate-transistor and is done with TLMs on the same die as the active-devices as described in section 2 of this chapter. The implicit-gate transistor model for access-regions is tested using TLMs, which are un-gated resistive structures of different lengths that are typically used to extract sheet-resistance (R_{sh}) and contact resistance by plotting the low-field-resistance as a function of the length of TLMs (L_{TLM}). R_{sh} and R_{sc}, R_{dc} are extracted from the low-field-resistance's scaling with L_{TLM} as shown in Fig.5-23(a), . These parameters are then used in the implicit-gate-transistor model to extract the high-field-region-parameters such as C_{Ig} that can model the saturation behavior of TLMs spanning the entire length-regimes as shown in Fig.5-23(b).

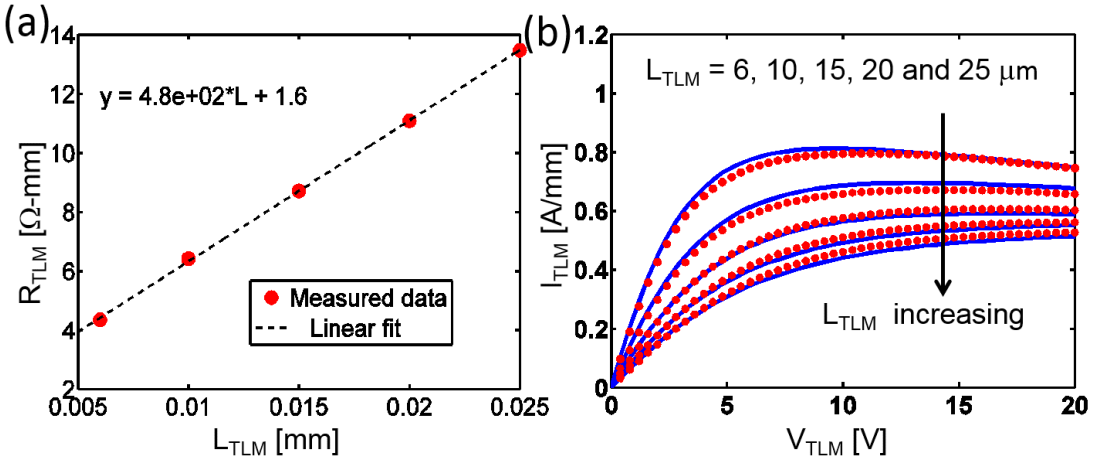


Figure 5-23: (a) Low-field-resistance as a function of L_{TLM} from which the R_{sh} can be extracted from the slope and the value of contact-resistance R_{sc} and R_{dc} can be extracted from the intercept. (b) In addition to the extraction of the low-field-parameters, fits to the TLMs in high-field-saturation regimes over the entire span of L_g enable the extraction of implicit-gate-capacitance (C_{Ig}). The implicit-gate-transistor model gives good fits to the IV-measurements over the L_g range.

The next step in the DC-model-validation is comparison against measured terminal-drain-current characteristics for bias-regimes spanning linear-to-saturation and off-to-on-state of the device which is illustrated for the scaled-gate-length devices fabricated at MIT in Figs.5-24 and 5-25 for $L_g = 42\ nm$ and $L_g = 105\ nm$ respectively. The device-heterostructure is described in detail in [19] and employs In in

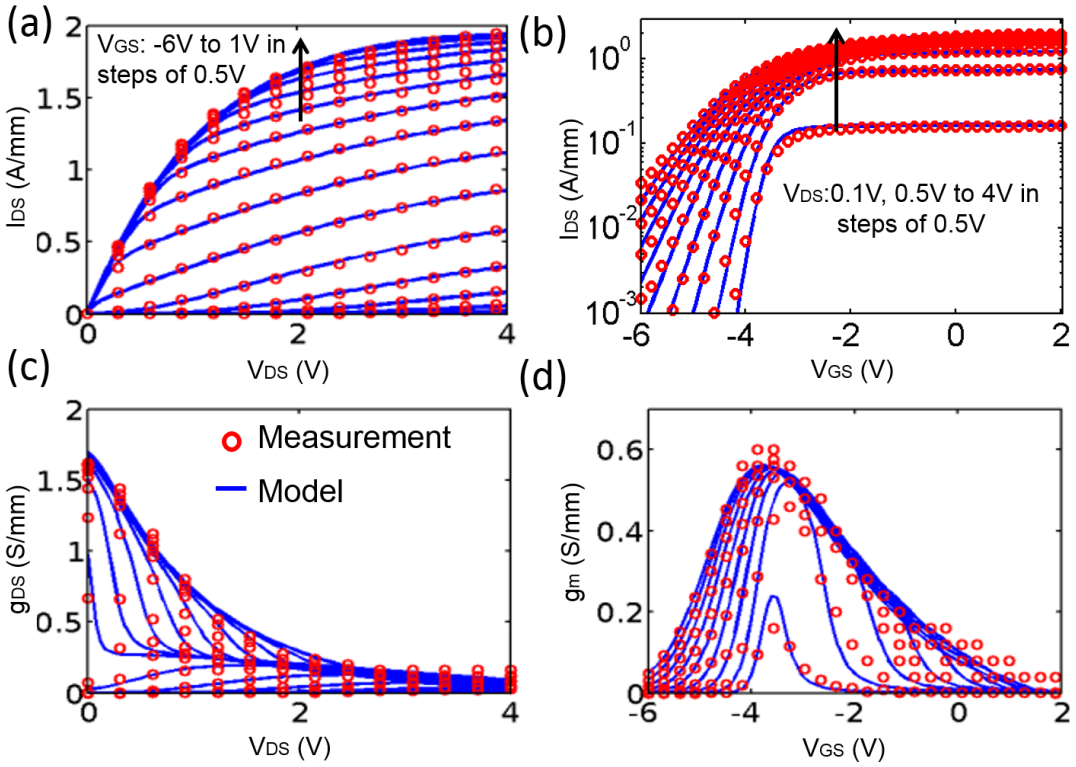


Figure 5-24: (a) Output-characteristics (b) transfer-characteristics (c) output-conductance and (d) transconductance measurements for the scaled 42 nm gate-length-device that is compared against the MVSG-model. The upper-bound on the on-currents (or the so-called 'quasi-saturation') at high V_{GS} is captured by the non-linear-access-region with implicit-gate-transistor-elements. The SCE are captured in the model-well. Device courtesy: Dr. Dong Seup Lee, MIT.

the heterostructure to increase n_s and boost the f_T and f_{max} of the device which are in the range of $200-300\ GHz$. In Fig.5-24(a), the output-characteristics of the 42 nm-gate-length-device shows significant short-channel-effects (SCE) that are captured using the DIBL-parameter (δ) and moderate-punch-through (n_d) parameters as explained in chapter 4. The transfer-characteristics in (b) also exhibit significant degraded SS in the moderate-accumulation-regime due to the scaled-gate-length and the absence of back-barriers in the device to curb the SCE. The compression in the output-characteristics have significant implications in the linear-behavior of the device that is evident from the sharp non-linear transconductance characteristics in (d) that show degradation in the intrinsic-gain of the device both due to access-region-resistive-debiasing and charge-depletion in these regions which is captured by the MVSG-model.

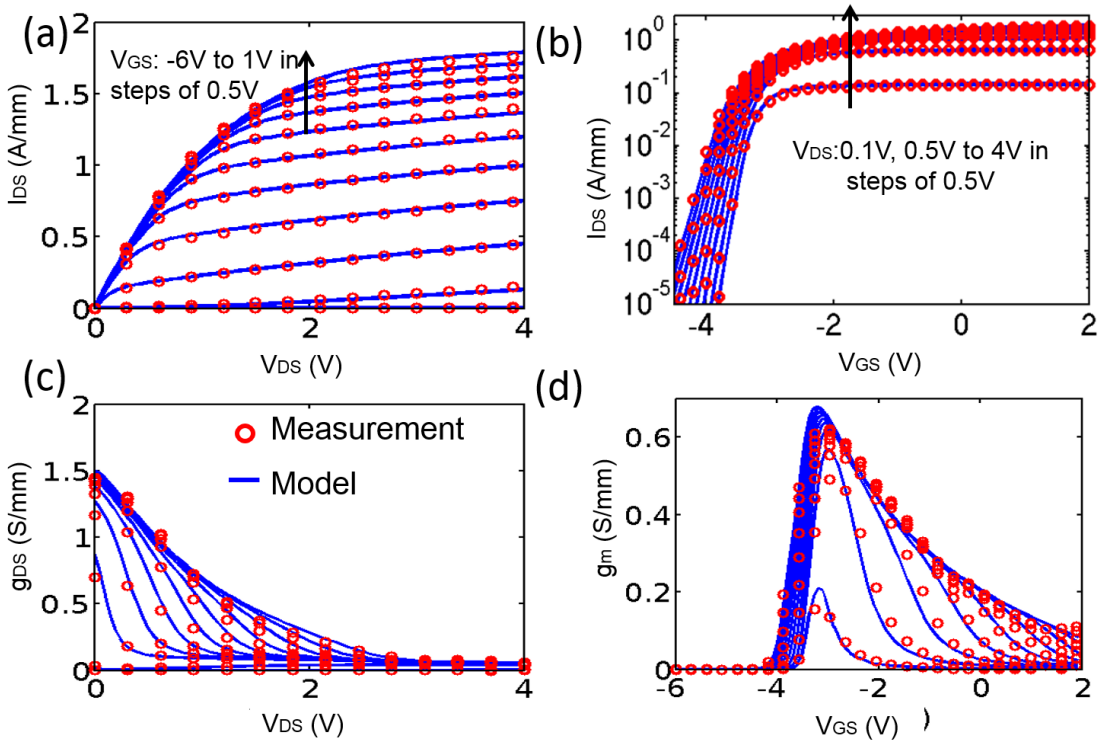


Figure 5-25: (a) Output-characteristics (b) transfer-characteristics (c) output-conductance and (d) transconductance measurements for the scaled 105 nm gate-length-device that is compared against the MVSG-model. The SCE are less severe compared to the 42 nm gate-length-device with different electrostatic parameters. The transport parameters used for both device-fits are same indicating the physical-strength of the underlying physical-transport-principles. Device courtesy: Dr. Dong Seup Lee, MIT

To test the scalability of the MVSG-model and determine the physical-accuracy of the model parameters used for the fits to the measured-DC-characteristics, another gate-length device is chosen on the same die with $L_g = 105\ nm$. The same values for transport parameters such as mobility μ_0 and velocity v_{x0} of carriers are used for the fits shown against measured terminal-current-characteristics and their derivatives shown in Fig.5-25 and the accuracy of fits for both device-measurements indicates that a substantial extent of transport-physics is correctly incorporated in the MVSG model. The electrostatic parameters such as V_T, SS, δ and so on are obviously different since the gate-lengths and hence the electrostatic-integrity of the channel is different for the two devices. The detailed list of parameter-set used for the two-devices is shown in Table.5.4. Finally, the $L_g = 42\ nm$ is one of the record-scaled-gate-

length device among GaN-based-HEMTs and represents the limit of short-channel-RF device-design and accuracy of MVSG-model fits in this length-scale indicates that model is useful for the entire spectrum of GaN-device technology.

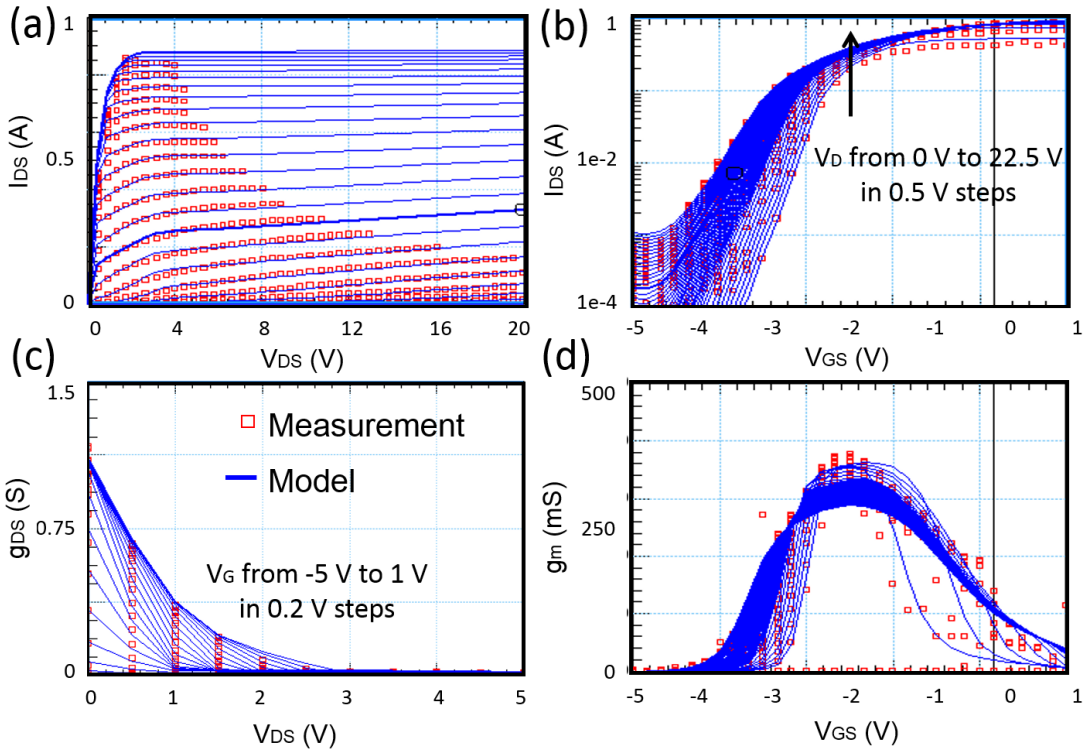


Figure 5-26: (a) Output-characteristics (b) transfer-characteristics (c) output-conductance and (d) transconductance measurements for the scaled RF-GaN HEMTs from Qorvo (formerly Triquint) that is compared against the MVSG-model. The measured output-characteristics are limited at high currents by a fixed-power-compliance. The model gives accurate match to the fits and the change in the slope of output-curves in saturation in (a) and hence the output-conductance is due to the depletion in drain-access-region which is captured in the MVSG model. SCE observed in the sub-threshold-regime is captured accurately in the model as well along with the floor in the off-state drain-current due to the gate-currents that are included in the model.

The second set of validations of the MVSG-model against RF-devices are done on scaled-L_g multi-finger RF GaN-HEMTs fabricated at Qorvo with the parameter set tabulated in Table.5.5. The resulting model comparison against measurements is shown in Fig.5-26. The access-region model is very important in these devices as they impact the output-conductance or the slope of the output-characteristics that can be seen in (a). The initial slopes in the output-curves are high due to the SCE (i.e. high DIBL) in the intrinsic-transistor-region but as V_{DS} increases, the

drain access-region starts to exhibit non-linearity which reduces the rate at which the internal drain-node voltage V_{Di} increases with external V_D. This 'smears-out' the DIBL effect in the intrinsic-transistor as V_{Di} gets pinned and does not change V_T of the intrinsic-transistor significantly through DIBL beyond this point which manifests as reduced slope (or output-conductance) in the output-characteristics. The transfer-characteristics, and the g_0 and g_m plots show good agreement between model and measurements.

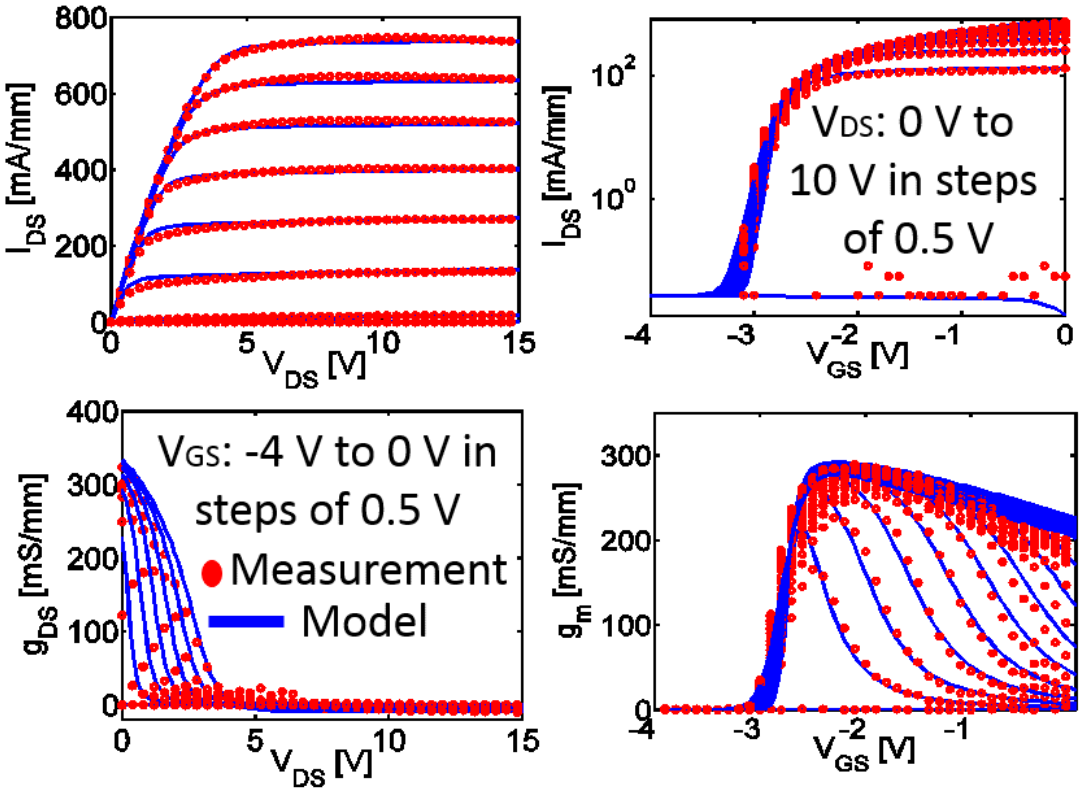


Figure 5-27: Output, transfer, output conductance, transconductance and gate current plots of $L_g = 250\ nm$ RF device from Wolfspeed (formerly Cree). Good agreement is achieved between the model and measurements. The drop in g_m beyond the V_T is caused in the model by the non-linear-access-region behavior and device self-heating.

The third set of device-model extraction is against a 250 nm-state-of-the-art industrial-RF-device from Wolfspeed (Cree) which is demonstrated in Fig.5-27. The full parameter-set for these fits is listed in Table.5.6 and many of these parameters are consistent with the typical values for RF-GaN-HEMTs. Fig.5-27 shows the model

comparison against terminal-current and current-derivative-measurements and as explained earlier, the various manifestations of behavioral nuances in GaN-HEMTs are correctly captured by the MVSG model. The model extracted against the DC-drain-current characteristics of three technologies can be used for further benchmarking relevant for RF-circuit-applications. In the remainder of this section, the non-negligible gate-currents in RF-GaN-HEMTs are validated using the model using Schottky-gated diode elements.

5.8 Gate-current benchmarking

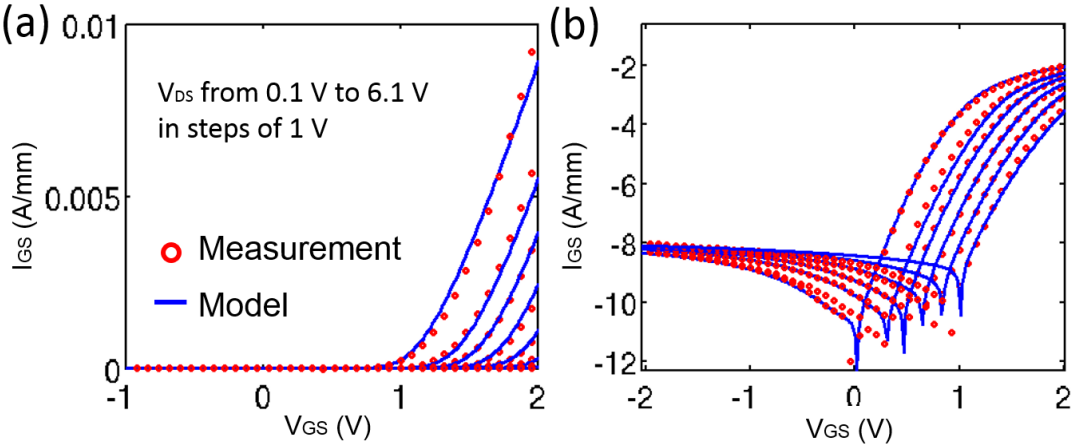


Figure 5-28: a) Gate-current (I_G) vs. gate-voltage (V_{GS}) in linear-scale for different V_{DS} for a Schottky-gated RF-GaN-HEMT. (b) Gate-current (I_G) vs. gate-voltage (V_{GS}) in the semilog-scale for different V_{DS} showing the forward-bias-current of the diode from both low- to high-injection regime along with the reverse-bias-current with recombination and GIDL-currents.

The Schottky-gate model formulated in the last chapter against the gate-current measurements for the Wolfspeed-devices is shown in Fig.5-28 where the forward- and reverse-bias regimes are compared against the GS- and GD-diode module in the MVSG-model formulation. In the forward-mode, the model accurately captures the diode-turn-on with cut-in voltage of about 1.0 V (Schottky-barrier-height) and the low-injection regime along with the increase in the ideality-factor at high-injection-regimes. The saturation of gate-current due to R_G at high-gate-current-

levels is included as well. In the reverse-bias-regime, the gate-currents are much higher than the reverse-saturation-currents of an ideal-diode and show saturation at about $V_{GS} = -1\ V$ which is modeled accurately by the MVSG-model through the recombination and GIDL-current equations described in chapter 4. The parameters used for these fits are listed in Table.5.6.

5.9 Capacitance characterization and benchmarking

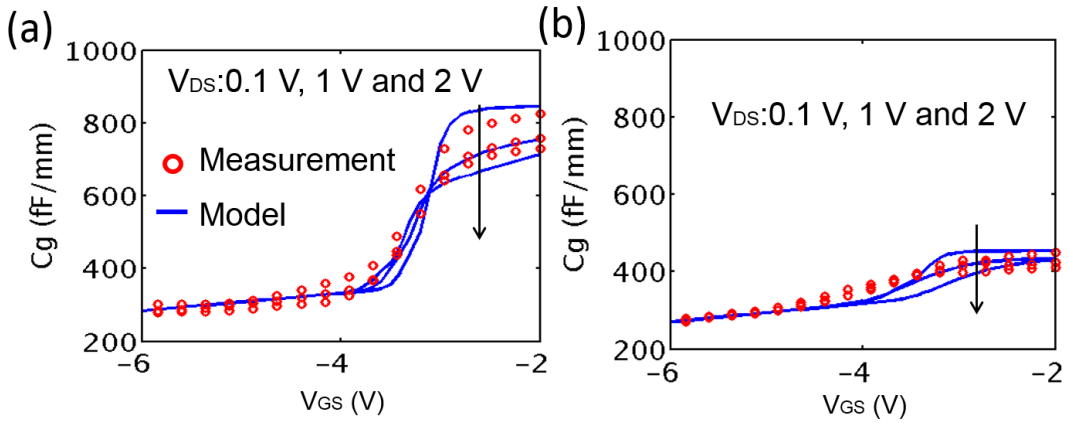


Figure 5-29: Gate-capacitance comparison for (a) 105-nm and (b) 42-nm MIT-devices: model vs. measurements. The CV-measurements are derived from S-parameter measurements explained in the next section [64].

Low-frequency-capacitance benchmarking is the next step in the MVSG-model extraction for RF-devices which can be done in a similar fashion to that of the CV-measurements for HV-devices explained in the previous section of this chapter. This involves the test-setup shown in Fig.5-8(a) with bias-Tees connected to each device-terminal to supply the both DC-bias and small-signal voltages and to measure the small-signal current. However since RF-devices do not typically are wide and have highly-scaled gate-lengths which yield terminal-capacitances whose values are typically in the fF-range and are often difficult to measure using the CV-measurement-setup using B1505A. Hence the low-frequency-CVs discussed in this section are obtained indirectly from S-parameter measurements as explained in the next section. The model-fits against derived-capacitance measurements are given.

The measured gate-capacitance (C_{iss}) is compared against model gate-capacitance (with added fringing-capacitances in the off-state) as shown in Fig.5-29 for 105-nm and 42-nm gate-length devices. The model gives a reasonable match with measurements confirming the validity of the gate-charge model. Since the capacitance in the on-state is dominated by the channel-capacitance, which scales with L_g, the gate-capacitance for the 42-nm device is lower than that of the 105-nm device. The off-capacitance in this case is dominated by outer-fringing-capacitances ($C_{ofs}, C_{ofd}, C_{ofds}$). The list of parameters used for these fits is tabulated in Table.5.4.

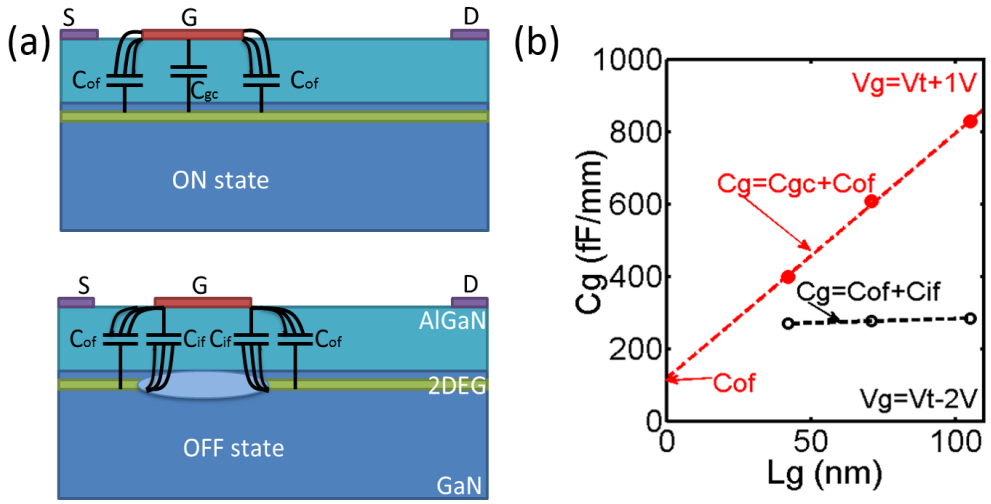


Figure 5-30: (a) Schematic showing different capacitances in on- and off-states. The channel screens inner-fringing C_{if} in the on-state. (b) C_{if} and C_{of} extraction-procedure from gate-capacitance measurements in off-and on-state vs. L_g [64].

The gate capacitances that are obtained from S-parameters include fringing capacitances in addition to gate-to-channel capacitances. These are extracted and included in the model for proper description of the dynamic-device-behavior. There are two types of fringing capacitances as shown in Fig.5-30(a): (i). Outer-fringing capacitances (C_{of}): These are capacitances that are due to the fringing-fields from the gate-metal to the 2DEG in the access regions whose model-formulation is explained in the previous chapter. The fringing-fields and associated capacitance exist in both strong- and weak-inversion. (ii) Inner-fringing capacitances (C_{if}): These are capacitances present only in the sub-threshold (off-state) when there is no significant charge in the channel. The inner-fringing capacitance is due to the inner-fringing field

from the gate-metal to the access region-2DEG through the channel region which are screened by channel-2DEG-field in the on-state. To mimic this behavior, the MVSG-model uses screening functions on inner-fringing-charges that employ Fermi-functions (F_f) [64]. Extraction of these parasitic-capacitances can be done using on-state and off-state capacitances of devices over a range of gate-lengths as shown in Fig.5-30(b). The off-state capacitance is the sum of C_{of} and C_{if} while the on-state capacitance is the sum of C_{gc} and C_{of} as shown. Both C_{gc} and C_{if} scale with gate-length and can be extracted from the slopes of the capacitance plots in on- and off-state as shown while the intercept of the on-state curve gives C_{of} whose values are used for the fits of capacitances in the MVSG-model.

5.10 Small-signal model verification

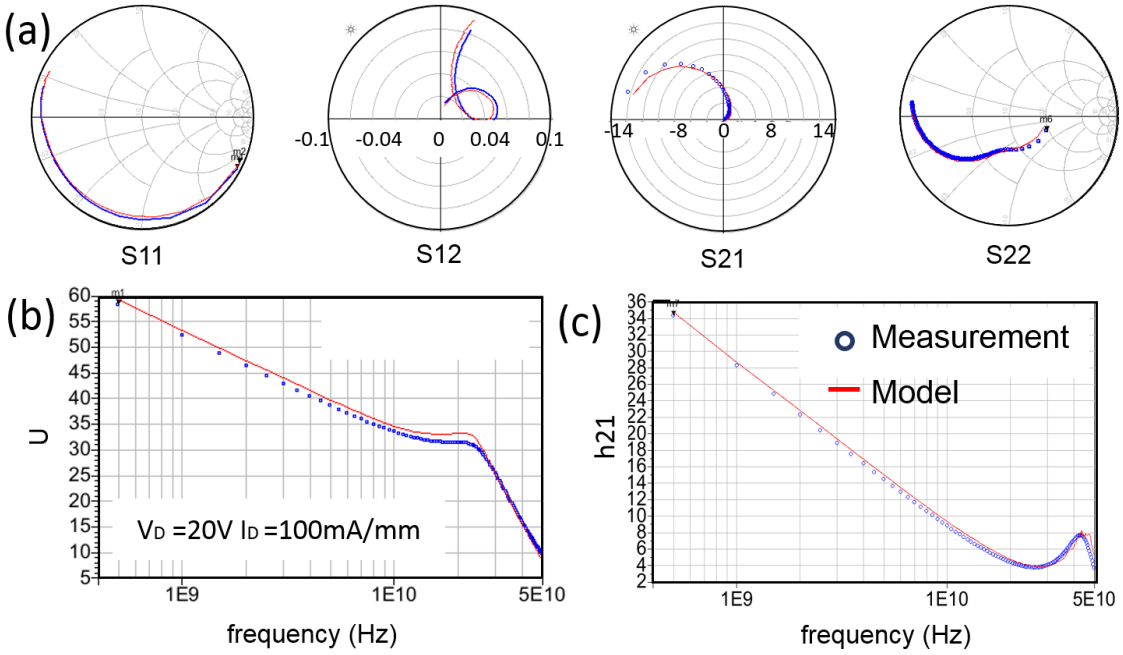


Figure 5-31: (a) S-parameters of a Qorvo device measured at $V_D = 20\ V$ and $I_D = 100\ mA/mm$ (Class-A) compared against S-parameter simulations of MVSG-model. (b) The unitary-gain (U) of the device plotted as a function of frequency gives an estimate of f_{max} (from the zero-intercept on the frequency-axis) (c) Small-signal current-gain (h_{21}) vs. frequency plot gives an estimate of f_T (from the zero-intercept on frequency-axis). Both f_T and f_{max} are estimated accurately by the MVSG model.

The S-parameters of the transistors are characterized from 100 MHz to 50 GHz using an Agilent-N5250C network analyzer. The system is calibrated with an off-wafer line-reflect-match (LRM) calibration standard. The device S-parameters are de-embedded from the measured ones using on-wafer open and short test structures as described in [53]. The equivalent circuit assumed to fit the device-level small-signal S-parameters obtained after de-embedding has been shown in Fig.4-9(b). The

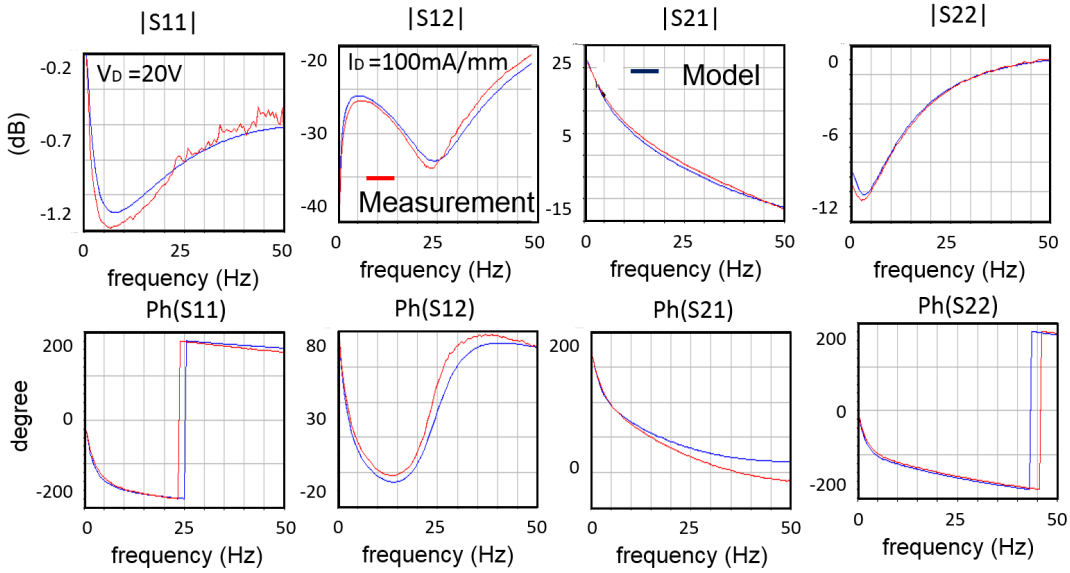


Figure 5-32: Magnitude and phase of S-parameters of the Qorvo device measured at different frequencies at class-A quiescent-bias condition compared against the MVSG-model showing the accuracy of the model.

MVSG-model calibrated against DC- and low-frequency CV-measurements is used as the core large-signal, bias-dependent, transistor-model which is embedded within a bias-independent device-parasitic network as explained in chapter 4. The element values of this device-level RLC parasitic-element network is extracted from S-parameter measurement fits at a typical bias-point shown in Fig.5-31 with the parameters listed in Table.5.5. The measured S-parameters of Qorvo-devices are accurately computed by the MVSG-model including the behavior of the small-signal current-gain (h_{21}) and unitary-gain (U) at frequency points beyond the f_T and f_{max}. In addition, the magnitude and phase of the 4 S-parameters are also correctly computed by the model as shown in Fig.5-32 with the input parasitic-elements such as R_G and L_G determining $S11$, source-via-inductance L_S and C_{ofd} determining $S12$, the core-transistor g_m determining $S21$, and g_0, L_D, R_D, C_{SUB} determining the $S22$.

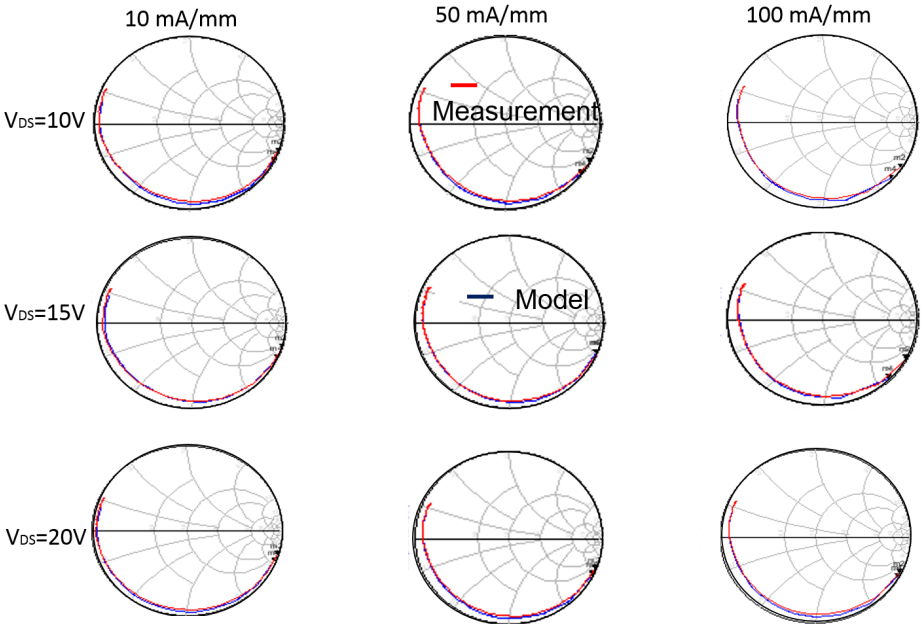


Figure 5-33: Measured S11-parameter compared against the model plotted on the Smith-chart for different bias conditions with $V_D = 10, 15, 20\ V$ and $I_D = 10, 50, 100 mA/mm$ after the model is extracted against one-bias-point. Accuracy spanning a wide-range of bias indicates the large-signal accuracy of the model with ability to capture bias-dependence correctly.

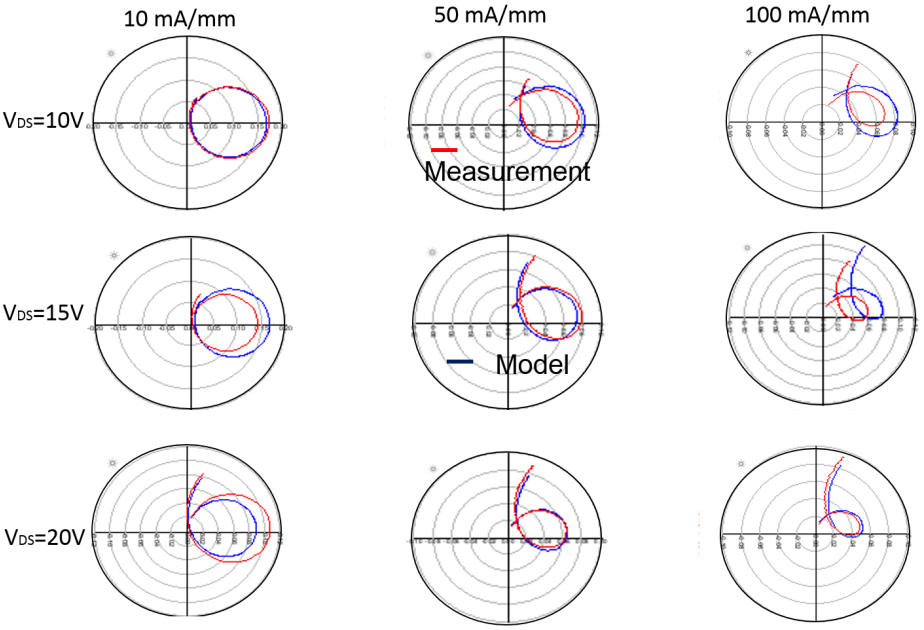


Figure 5-34: Measured S12-parameter compared against the model plotted on the Smith-chart for different bias conditions with $V_D = 10, 15, 20\ V$ and $I_D = 10, 50, 100 mA/mm$ after the model is extracted against one-bias-point. The device under study is Qorvo-industrial RF-device.

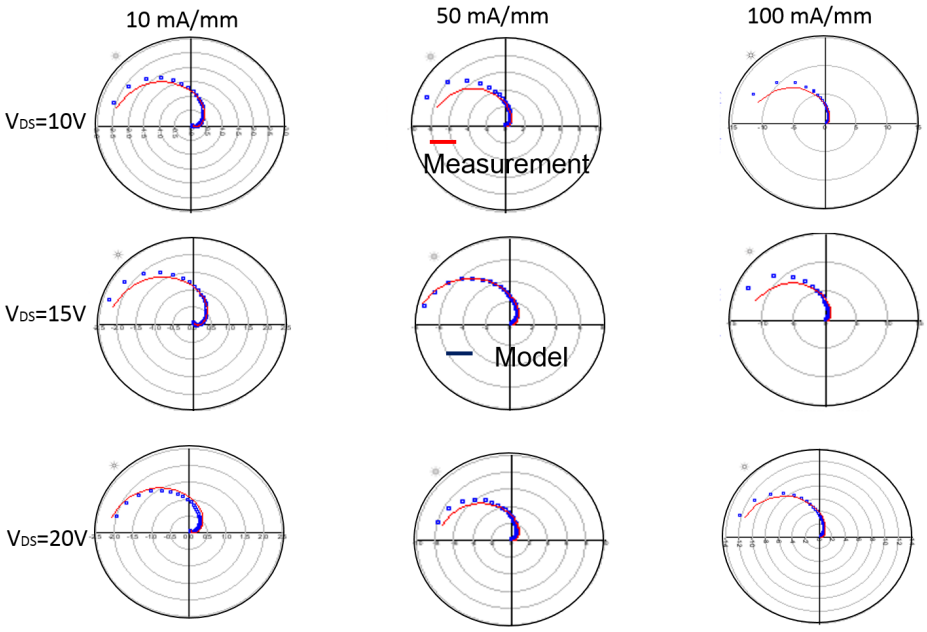


Figure 5-35: Measured S21-parameter of Qorvo-RF-device compared against the model plotted on the Smith-chart for different bias conditions with $V_D = 10, 15, 20\ V$ and $I_D = 10, 50, 100 mA/mm$. The gain is accurately captured across bias-points indicating the accuracy of MVSG-model.

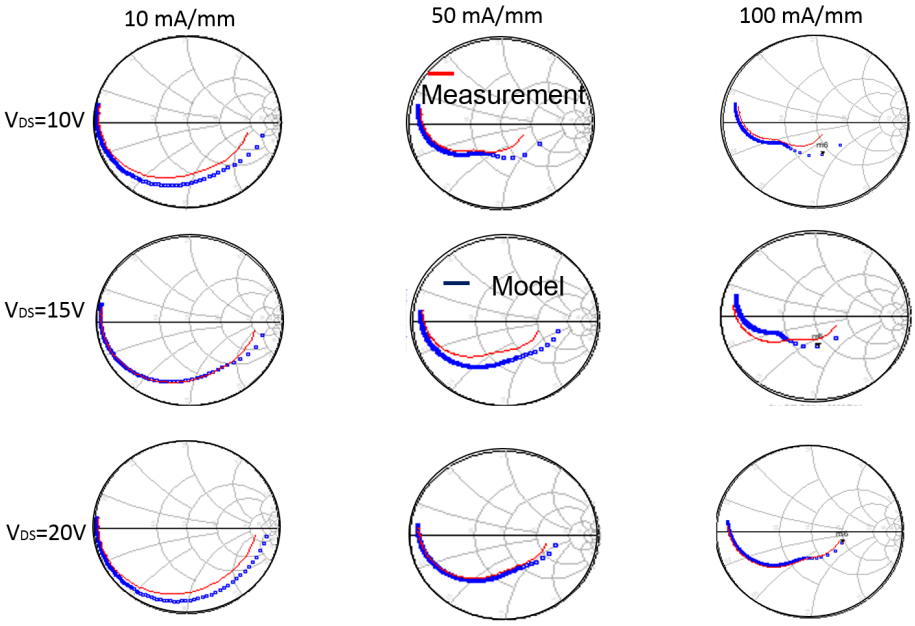


Figure 5-36: Measured S22-parameter of Qorvo-RF-device compared against the model plotted on the Smith-chart for different bias conditions with $V_D = 10, 15, 20\ V$ and $I_D = 10, 50, 100 mA/mm$.

Once the device-level parasitic-elements are extracted from the fits against the measured S-parameters at a couple of bias-points, the calibrated MVSG-model is used to simulate S-parameters against measured small-signal parameters at other bias points spanning the full-bias-regime of interest for practical RF-circuit-design. The 'global'-S-parameter fits for Qorvo-RF-device are shown in Figs.5-33-5-36 for class-A, Class-B and class-AB quiescent-bias-conditions with V_D ranging from $5\ V - 20\ V$. Reasonable accuracy is obtained from the MVSG-model fits against measurements spanning the full-bias-regimes demonstrating the large-signal-validity of the MVSG-model. Second set of validation of the MVSG-model against small-signal S-parameters is done using the 250 nm-Wolfspeed-RF-device with the parameter list tabulated in Table.5.6. Comparison of measured S-parameters against the model spanning the bias-regime from off-to-on-state and linear-to-saturation along with frequency ranging from low (100 MHz)-to-high ($f > f_{max}$) values is shown in Fig.5-37. The model calibrated upto small-signal measurements can be used directly to predict the large-signal device-performance as explained in the next section.

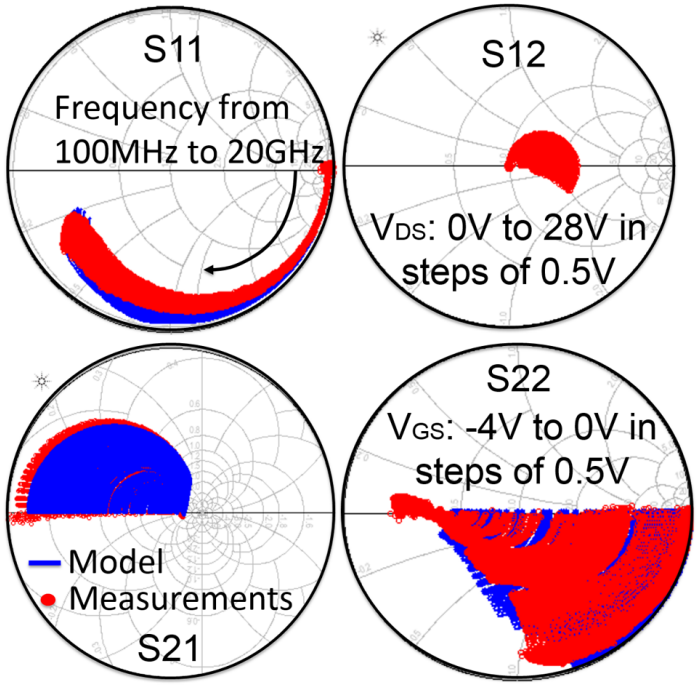


Figure 5-37: The comparison of small signal S-parameter fits over the desired bias and frequency ranges required for RF-circuit-design. The input gate-parasitics affect S11 parameter and output drain-parasitics including substrate-parasitics can be extracted from S22 parameters. The g_m of the device primarily determines the S21 parameter.

5.11 Large-signal device-characterization

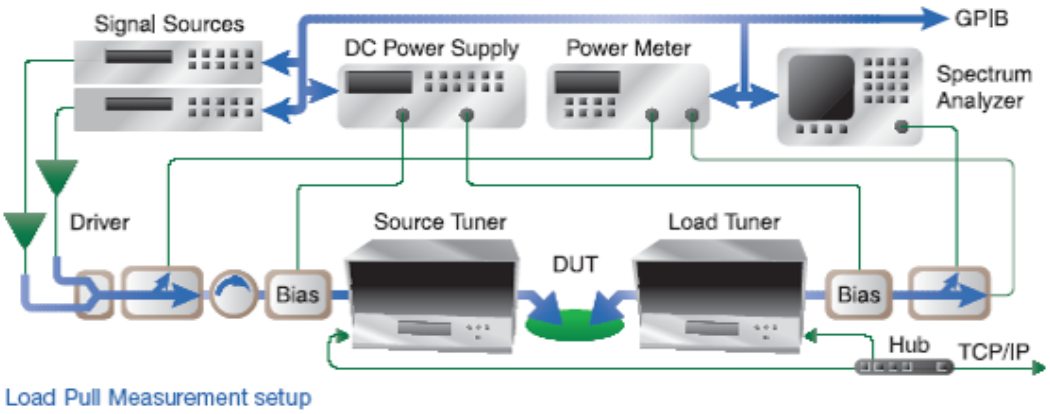


Figure 5-38: Typical large-signal measurement setup showing the different components for sourcing and sensing power, bias along with the impedance tuners from Focus microwave.

The large-signal modeling of GaN-HEMTs is critical for PA-design and the model extracted from DC- and S-parameter fits is capable of capturing the large-signal behavior of the device due to its physical nature. The key large-signal model benchmarking before using it for circuit-design are load- and source-pull along with power-sweep calibration. The load-/source-pull setup is used for these measurements as shown in Fig.5-38 in which the gate- (input) and drain- (output) terminal impedances can be changed to tune out the device passives so as to maximize the output-power transfer for a given input. DC bias-Tees at the input- and output-ports are used to bias the device in a particular class of operation and input power is applied through a signal source (2 signal sources can be used at the input combined using an RF-combiner to do two-tone measurements). Output-power and the available source-power are measured using a power-meter as shown in the circuit-setup. In this section, the measurements of large-signal characteristics are compared against the model-simulations to test the accuracy of the MVSG model.

5.11.1 Source-pull validation

In source-pull measurements, the device is biased in a particular-class, a fixed input-power is applied through the input-power-source and the source-impedance is swept

by sampling on the smith-chart at a given load-impedance to determine the optimum source-impedance to achieve maximum output-power or power-added-efficiency. Maximum power is transferred from the input-power-source to the device when the source-impedance is conjugate matched to the input-impedance of the device. Since the gate-input of a GaN-HEMT typically offers a capacitive-reactance (due to C_g) along with gate-resistance (R_G), the optimum source-impedance in the source-pull setup is usually inductive.

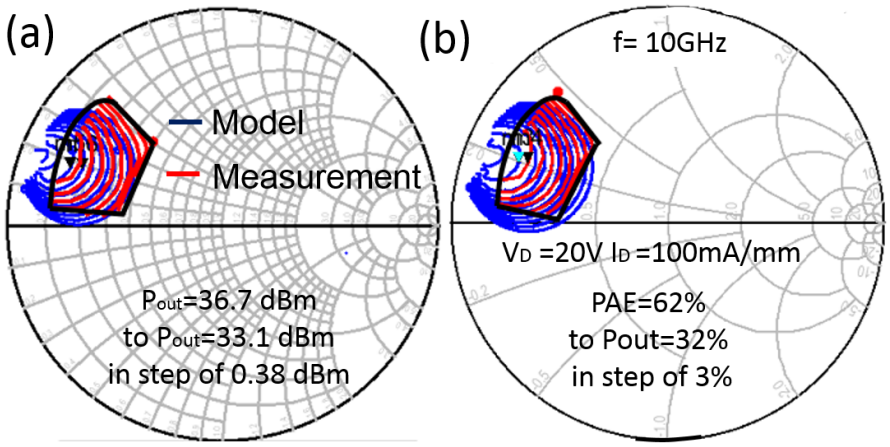


Figure 5-39: (a) The measured output-power contours plotted on the Smith-chart for different input-reflection points are compared against harmonic-balance simulations using the MVSG-model. (b) The measured power-added-efficiency at the output of the device plotted on the Smith-chart for different input-reflection points compared against MVSG-model-simulations.

The results of source-pull measurements done on Qorvo-RF-device are shown in Fig.5-39 where the source-impedance is tuned at the input-port using the source-tuner and the load-impedance is fixed using the load-tuner ($Z_{L,fundamental} = 24 + j24$, $Z_{L,secondharmonic} = 126 - j115$, $Z_{L,thirdharmonic} = 15 - j15$) upto the third-harmonic in addition to the fundamental-load-impedance. The input available-source-power is set to 23 dBm at a fundamental frequency of 10 GHz for these measurements and the quiescent-bias is set to class-A mode of operation. Contours are generated for both the output-power (P_{out}) and power-added efficiency ($PAE = \frac{P_{out}-P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G_T}\right)$) and plotted on the Smith-chart for different source-reflection-coefficient (Γ_S) values as showni in Fig.5-39. Each Γ_S is obtained for a set-value of the source-

tuner given by: $\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}$ where Z_S is the tuner-source-impedance and $Z_0 = 50\ \Omega$ is the characteristic-impedance. The simulations using the MVSG-model are done in the ADS-circuit-simulator using harmonic-balance (HB) simulations upto third-harmonic and give a good match to the measured P_{out} and PAE contours as seen from the Figure. The values of P_{out} and PAE not only match in terms of the values but also correspond to the same Γ_S values that is evident form the Fig.5-40, which shows the model-validation in terms of P_{out}, PAE, transducer-gain G_t and RF-output-current I_{out} as function of real and imaginary parts of the input-reflection-coefficient (Γ_S). From Fig.5-40 it is clear that the MVSG-model is able to capture the device-

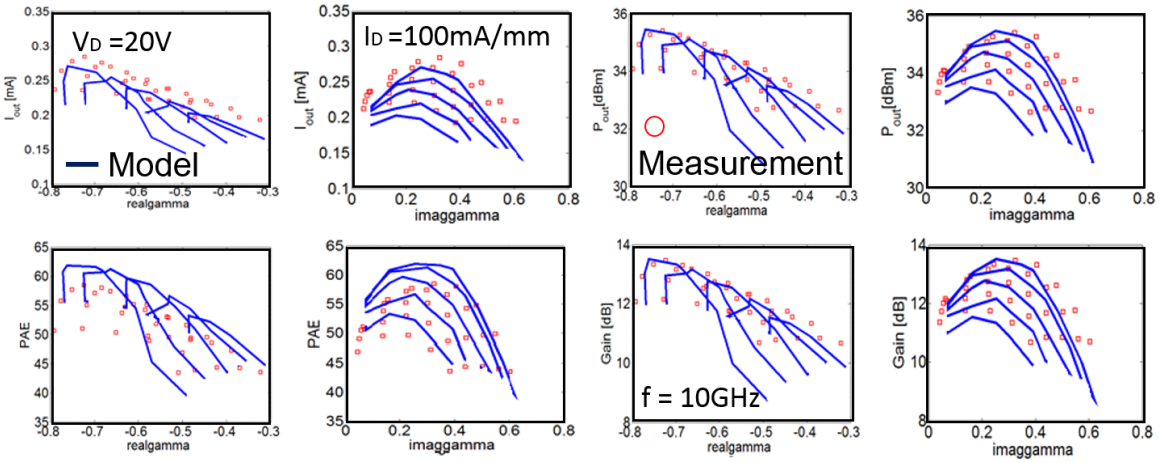


Figure 5-40: I_{out}, P_{out}, PAE and G_t plotted for the RF-Qorvo-device as a function of real and imaginary components of Γ_S.

large-signal metrics accurately in response to changing input-impedance presented to the DUT by the source-tuner. The MVSG-model used for this evaluation is calibrated against DC- and small-signal parameters and **does not** require additional parameters to estimate the large-signal source-pull behavior because of its physical-underpinning. The next step in large-signal validation is the load-pull measurement which is discussed below.

5.11.2 Load-pull validation

In load-pull measurements, for a given source-impedance and input-power level, the load-impedances are sampled on the Smith-chart to record the impedances at which

the maxima of output-power and power-added-efficiency occur. At any given input-impedance, maximum output-power can be extracted from the DUT when the output-tuner-impedance is conjugately matched to the output-impedance of the DUT, which is dominated by g_0 and $C_{gd} + C_{ds}$ of the device.

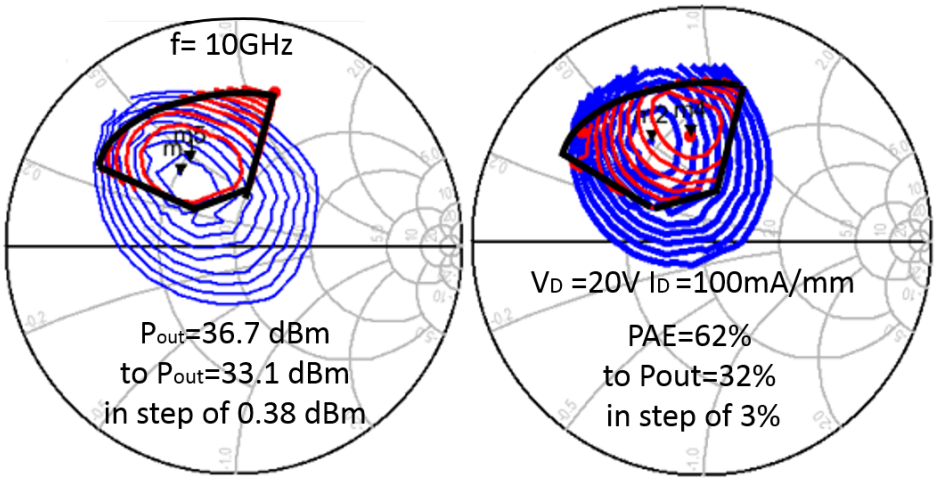


Figure 5-41: (a) The measured output-power contours plotted on the Smith-chart for different output-reflection points are compared against harmonic-balance simulations using the MVSG model. (b) The measured power-added-efficiency at the output of the device plotted on the Smith-chart for different output-reflection points compared against MVSG model simulations.

The results of load-pull measurements are shown in Fig.5-41 where the load-impedance is tuned at the output-port using the load-tuner and the source-impedance is fixed using the source-tuner ($Z_{S,fundamental} = 6 + j10$, $Z_{S,secondharmonic} = 11 + j53$, $Z_{S,thirdharmonic} = 58 + j130$) upto the third-harmonic-source-impedance. The input available-source-power is set to 23 dBm at a fundamental frequency of 10 GHz and the quiescent-bias is set to class-A mode as before. Contours are generated for both the output-power (P_{out}) and power-added efficiency (PAE) and plotted on the Smith-chart for different load-reflection-coefficients ($\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$) as shown, where Z_L is the tuner-load-impedance. The simulations using the MVSG model done in the ADS-circuit-simulator using harmonic-balance (HB) simulations upto third-harmonic, give a good match to the measured P_{out} and PAE contours as seen from the Figure. The values of P_{out} and PAE also match in terms of the values and the Γ_L at which they are obtained. Fig.5-42 shows the model-validation in terms of P_{out}, PAE,

transducer-gain G_T and RF-output-current I_{out} as a function of real and imaginary parts of the output-reflection-coefficient (Γ_L) in which the MVSG-model is able to capture the device-large-signal metrics accurately in response to changing output-impedance offered to the DUT from the load-tuner without requiring any additional parameters for the model-fits to the measurements. The sequence of source-pull and

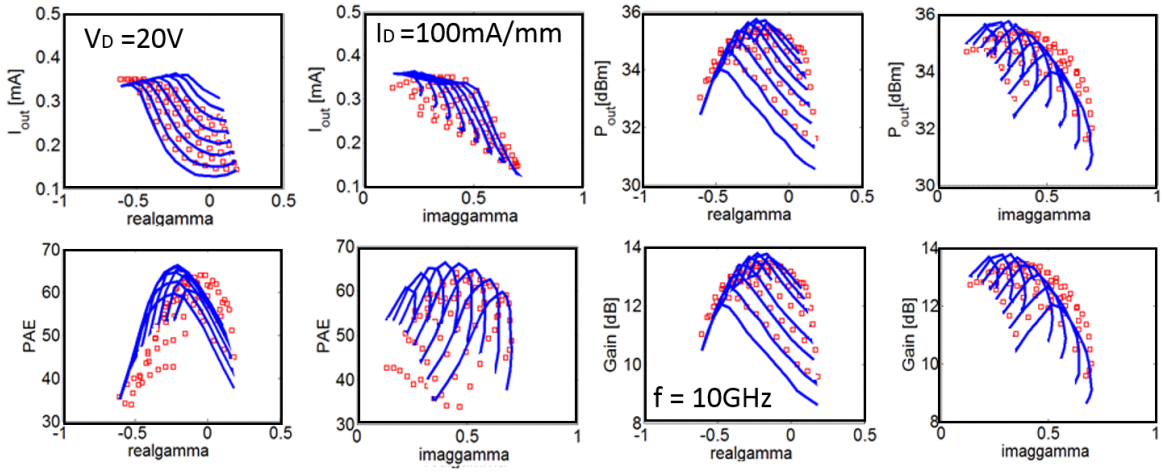


Figure 5-42: I_{out}, P_{out}, PAE and G_T plotted for the RF-Qorvo-device as a function of real and imaginary components of Γ_L.

load-pull measurements are done alternatively in iteration so that overall optimal source- and load-impedances for the DUT are obtained and once the impedances are optimized, the input-power is swept to find the gain, efficiency and output-power levels and to study the onset of compression in the device for a given class as described in the next sub-section.

5.11.3 Power-sweep validation

Typical large-signal measurement results are compared against the model-simulations in Figs.5-43 and 5-44 for optimum source- and load-impedances. The accuracy demonstrated by the MVSG-model calibrated from S-parameter measurements to get the fits of the quality shown here indicates the strength of a physical model.

Both class-A and class-AB operating modes are shown for the Qorvo-device indicating the different trade-offs involved in each class of amplifier-design. In class-A, the device is linear over a large P_{in} range with high-gain and output-currents while in

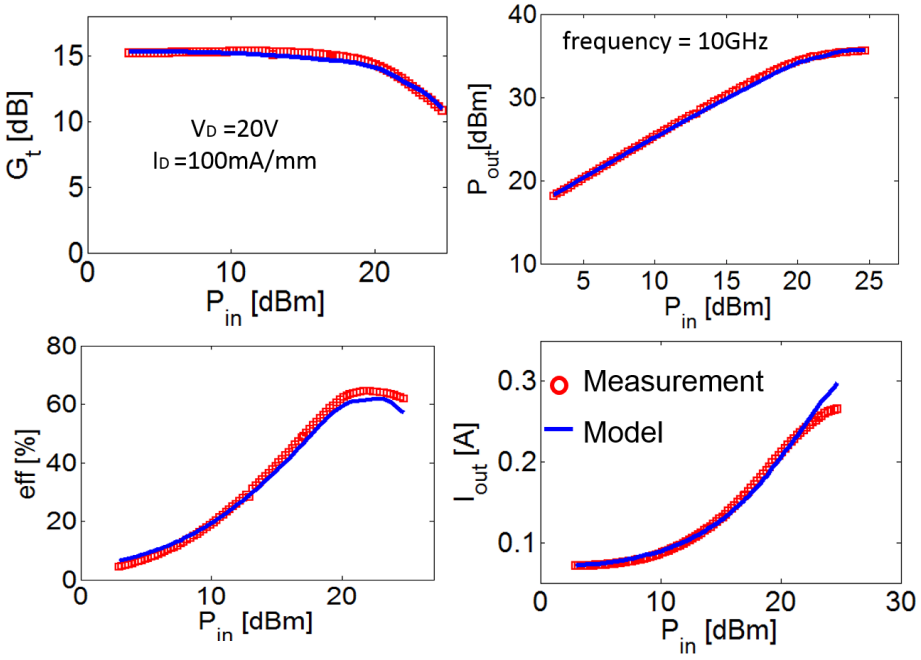


Figure 5-43: Measured G_t, P_{out}, PAE, and I_{out} vs. P_{in} are plotted for the RF-Qorvo-device and compared against power-sweep simulations for a class-A mode of operation. The model is able to accurately describe the low-power linear-region as well as the high-power compression-regime accurately.

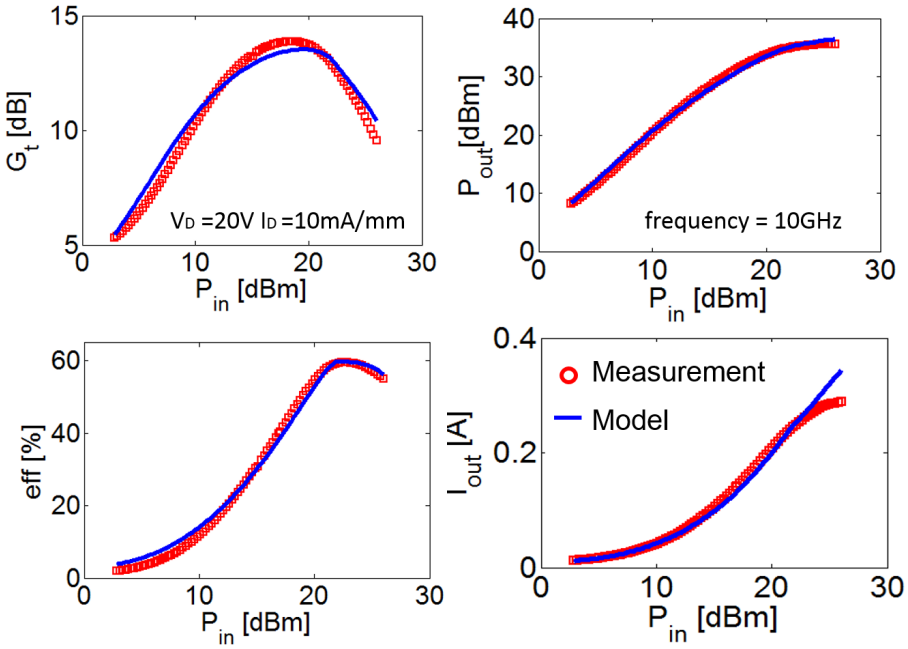


Figure 5-44: Measured G_t, P_{out}, PAE, and I_{out} vs. P_{in} are plotted for the RF-Qorvo-device and compared against power-sweep simulations for a class-AB mode of operation. The model is able to match well the large-signal metrics including compression regimes for different quiescent-conditions.

class-AB, the device has more non-linearity (evident from the G_T plot) but consumes less DC-power due to the lower I_{out} as a consequence of near V_T-operation. The G_T is about 15 dB in class-A while the peak-G_T is about the same in class-AB. The compression characteristics in both classes along with the values of the different large-signal metrics are accurately estimated by the MVSG model calibrated against S-parameter measurements using parameters listed in Table.5.5. A second set of validation is done

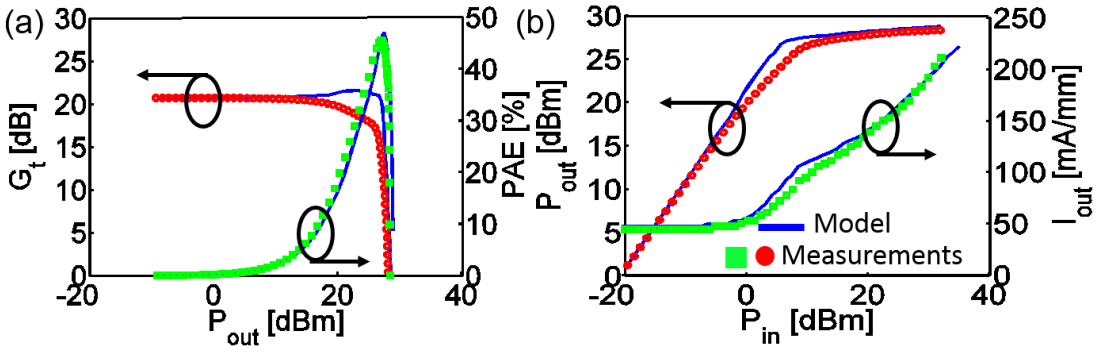


Figure 5-45: (a) Large signal metrics such as P_{out}, G_t, PAE and I_{out} of the commercial Wolfspeed-GaN-HEMT is compared against the model. The measurements were made using the on-wafer Maury load-pull setup. The transistor is biased in class-AB mode which resulted in $G_T = 20dB$, $PAE = 50\%$.

using on-wafer-load-pull measurements on a commercial Wolfspeed RF-GaN-HEMT whose characteristics upto S-parameters are measured and the MVSG-model is extracted as described earlier. The device-level large-signal metrics are measured using the wafer-level load-pull measurement setup from Maury Microwave and the measured power-sweep data are compared against the model in Fig.5-45. The Wolfspeed GaN-on-SiC device biased at class-AB ($V_{DS} = 28\ V$ and $V_{GS} = V_T + 0.25\ V$) and the power-sweep simulations show correct prediction of $P_{out} = 28\ dBm$ and $PAE = 45\%$ at 6 GHz. The calibrated model can also be used to make projections linking key device-level bottlenecks to RF device performance, as will be shown in the next chapter. The large-signal validation done in this section makes the MVSG-model suitable for transmitter-PA-design. However for the design of saturated-non-linear-PAs under stringent channel-bandwidth-constraints, physical compact-models are required to capture the large-signal device-non-linearities accurately which is the topic of discussion in the next section.

5.12 Device-non-linearity validation

The requirements of efficiency and linearity on power-amplifiers at the transmitter-side of any communication-system directly trade-off with each other and recently the cellular-market with its increasing demand for spectral-efficiency (in 3G-technologies and beyond) has initiated research on the linearity-implications of PAs on the overall-telecommunication system efficiency. The core-FET used in the design of any RF-PA makes it inherently non-linear in the large-signal operation-regime which means that the output-spectrum from the PA for a given input-spectrum is spread-out (spectral-regrowth) thus degrading the spectral efficiency of the system [65]. The spectral-spreading causes interference with adjacent channels and therefore imposes wider-bandwidth constraints on the channel which is undesirable since spectrum is a priced scarce commodity. There are techniques developed at the circuit-and system-level such as designing linear-circuit-topologies (Doherty scheme), and digital-pre-distortion-schemes but it is educational to look at the fundamental root-cause for this non-ideality namely: the non-linear-behavior of the FET used in the PA, which is the topic of this section.

A FET and the GaN-HEMT in particular is inherently non-linear in the moderate-accumulation and high-V_G-compression-regions along with mild-non-linear behavior in the region in between. This is evident from the intrinsic-transistor-gain determined by g_m shown in Fig.5-46(b). The g_m is not constant across (V_D, V_G) and has significant non-linear components depicted by its derivatives g'_m and g''_m in the figure. The output-RF-current and hence gain of the device can then be expressed in the well-known Volterra-series formulation as:

$$i_{out}(v_{gs}) = g_m(V_{GS}, V_{DS})v_{gs} + g'_m(V_{GS}, V_{DS})v_{gs}^2 + g''_m(V_{GS}, V_{DS})v_{gs}^3 + ... \tag{5.1}$$

and the output power for a given constant load-impedance Z_L is given by:

$$P_{out}(v_{gs}) = |i_{out}(v_{gs})|^2 Z_L/2 = A_0(V_{GS}, V_{DS})v_{gs}^2 + A_1(V_{GS}, V_{DS})v_{gs}^3 + A_2(V_{GS}, V_{DS})v_{gs}^4 + ... \tag{5.2}$$

where $A_0 = g_m^2 Z_L/2$, $A_1 = g_m g_m' Z_L$, $A_2 = g_m g_m'' + g_m'^2/2$ and so on. Even if the input-power applied to the FET ($P_{in} = |v_{gs}|^2/(2Z_S)$) is at a single-frequency (with $v_{gs} = A_{in}cos(\omega t)$) the output-power via Fourier-transform of Eq. (5.2) has significant-harmonic components:

$$P_{out}(\omega) = P_0(V_{GS}, V_{DS}, \omega) + P_1(V_{GS}, V_{DS}, 2\omega) + P_2(V_{GS}, V_{DS}, 3\omega) + ... \tag{5.3}$$

where P_0, P_1 and P_3 are the fundamental, second- and third-harmonic output-power-levels from the device in response to a single-tone-input-signal. So the ability of physical-models to estimate the g_m-non-linearity of the device is critical in order to estimate the harmonic-output-power-levels of the device in a PA and is shown for the MVSG-model calibrated against Wolfspeed-devices in Fig.5-46.

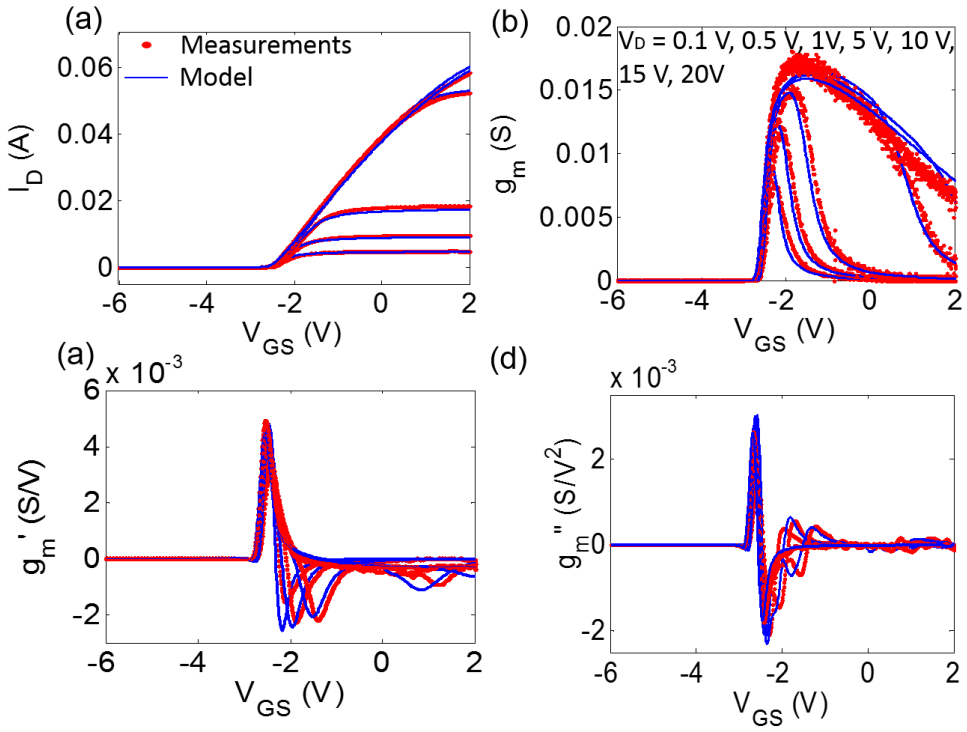


Figure 5-46: (a) Transfer characteristics, (b) transconductance, (g_m) (c) first-derivative of g_m (g_m') and (d) second-derivative of g_m (g_m'') for Wolfspeed-device compared against the MVSG-model. The non-linearity in g_m and hence the device-gain can be observed and captured by the model for V_D spanning linear-to-saturation-regimes. The non-linearity in g_m is the primary-reason for device-non-linearity.

As can be seen, the second-and third-derivatives are non-zero with significant g_m''

in the region just beyond $V_G = V_T = -3\ V$ and upto $V_G = -1\ V$ (gate-overdrive voltage corresponding to peak g_m is related to V_{DSAT}). This is the region of transition from moderate-accumulation to strong-accumulation in on-state and is generic to any FET. Although g_m reduces beyond the V_G corresponding to the peak-g_m-point due to device-heating and non-linear-access-regions, the values of higher-order-derivatives in this region are negligible. Therefore the cause for non-linearity in GaN-HEMTs is the same as for any regular-FET and is between $V_T < V_G < V_{DSAT} + V_T$ determined primarily by the device-parameters such as C_g, v_{x0} and μ_0 as will discussed in detail in the next chapter. The MVSG-model can estimate the large-signal non-linearities associated with g_m as can be seen over a wide bias regime. The analysis done so far assumes that the reactive components of the device (gate-capacitances) are linear but in reality they are non-linear as well, as seen from the discussion on device-capacitances in this chapter which are modeled accurately by the MVSG-model.

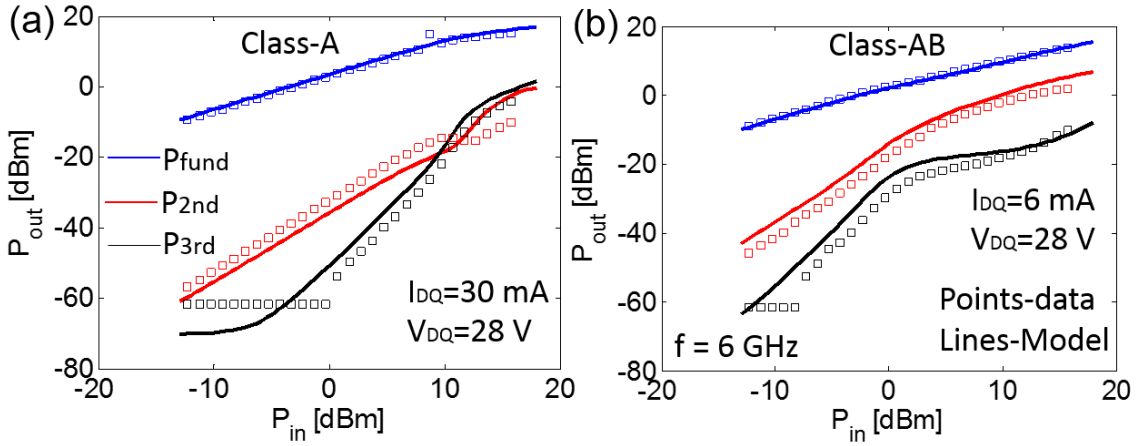


Figure 5-47: Fundamental, second and third-harmonic output-power-levels for a single-tone-input (at $f = 6\ GHz$) whose value is swept with the DUT biased in (a) class-A and (b) class-AB mode. The measured power-levels for both modes match-well with Harmonic Balance simulations using the MVSG model.

The calibrated MVSG-model is capable of estimating the harmonic-components of the device-output-power in response to a single-tone-input which is determined by measuring the output-power from the DUT using a spectrum-analyzer for a single-tone input whose power-level is swept. The source- and load-tuners shown in the setup of Fig.5-38 are set to Z_0 for ease of system-calibration and the results are shown in

Fig.5-47 for two classes of operation. in both class-A and class-AB quiescent-bias-conditions, the MVSG-model can estimate the output-power-levels accurately both in low-input-power-linear-regimes and in high-input-power compression-regimes. Significant portion of the output-power is dispersed in the harmonic-frequencies causing compression at output-power-levels. The linearity performance in class-A is better than class-AB as expected and the linearity sweet-spot at $P_{in} = 10\ dBm$ in class-A is accurately estimated by MVSG-model as well. The resolution of the output spectrum-analyzer is limited by the noise-floor at $-60\ dBm$ but the model-results fare well with measurements above this limit.

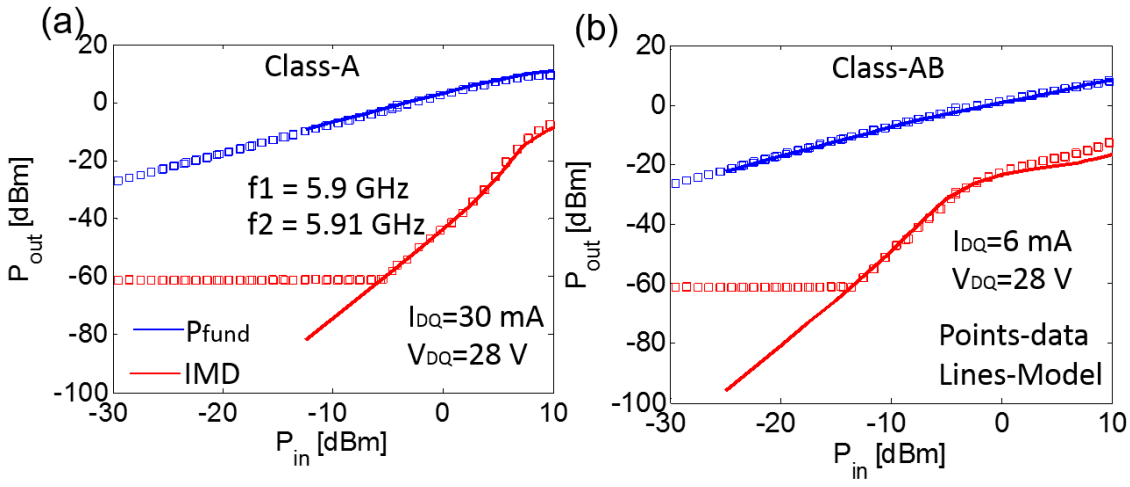


Figure 5-48: Fundamental and third-order-intermodulation output-power-levels for a two-tone-input (at $f = 6\ GHz$) whose value is swept with the DUT biased in (a) class-A and (b) class-AB mode. The measured power-levels for both modes match-well with HB-simulations using MVSG-model.

While single-tone-input-response is a good method to characterize the device-level-non-linearities, in practical circuit-applications the harmonic-frequency-components can be eliminated by using a filter in the transmitter or receiver-side of the communication system. However, the RF-amplifier-non-linearity is also manifested in the response to multi-tone input-power-signals applied to the PA, which is a realistic scenario since multiple input-powers closely-spaced in frequencies can be applied to the PA to squeeze in information in the narrow-BW-channel of a communication system. Device non-linearity causes 'mixing' between the multiple input-tones at the output, with significant output-power at these mixed frequencies that lie within the

BW of the channel and cannot be filtered-out. Characterization of this effect known as inter-modulation is done by using two signal-generators at the input with slightly different frequencies (f_1) and (f_2) which are combined and applied to the DUT with the tuners set to Z_0 and the output-power measured at different frequencies using a spectrum-analyzer. The total input-power is given by:

$$P_{in}(v_{gs}) = P_0\left(cos(\omega_1 t) + cos(\omega_2 t)\right) = 2P_0 cos(\omega_c t)cos(\omega_d t) \tag{5.4}$$

where $\omega_c = 2\pi(f_1 + f_2)/2$ and $\omega_d = 2\pi(f_1 - f_2)/2$ and the resulting output-power from the DUT is given by:

$$P_{out}(\omega_1, \omega_2) = P_{fund}(\omega_1) + P_{fund}(\omega_2) + P_{lowsideband}(2\omega_1 - \omega_2) + P_{uppersideband}(2\omega_2 - \omega_1) + ... \tag{5.5}$$

Since the amplitude of the two-input-powers are equal, $P_{lowsideband}$=$P_{uppersideband}$, and the results of this measurement on RF-Wolfspeed-device are shown in Fig.5-48 in which the HB-simulations using the MVSG-model are compared against measurements for both class-A and class-AB operating-classes. The input-two-tones are spaced $10MHz$ apart with $f_1 = 5.9\ GHz$ and $f_2 = 5.91\ GHz$ and the input-power is swept from low-to-high compression-regime. The measured output-powers at f_1, f_2 and $2f_1 - f_2$ and $2f_2 - f_1$ are plotted against simulations in the figure (the two output-tones at f_1 and f_2 are on-top of each other and the two-inter-modulated signals are on-top of each other as well) and the MVSG model gives an accurate estimate of IMD-behavior of the device (above the measurement limit of -60 dBm) and estimates the change in IMD with operating-class as well.

The large-signal behavior of the device along with the estimation of non-linearities (both harmonics and IMD) can be estimated by the MVSG-model that is calibrated against device-level-measurements done upto small-signal S-parameter measurements without needing additional parameters for the large-signal-modeling. The device-level-validation described so far makes the model suitable for RF-transmitter-design. However, designing receiver RF-components also requires accurate estimation of device-level noise-power-spectrum-densities which is described in the next section.

5.13 Device-noise model validation

The noise-source characterization of the device is required to ensure that the MVSG-model can be used as a tool for RF-LNA-design. The white-noise-sources associated with the device-resistances (both channel and parasitic-resistances) and shot-noise associated with gate-diodes, discussed in the last chapter, are relevant for estimating device-level noise-figure (NF). The on-wafer measurement of this device-NF is done using the methodology highlighted in [26] whose circuit-setup is shown in Fig.5-49.

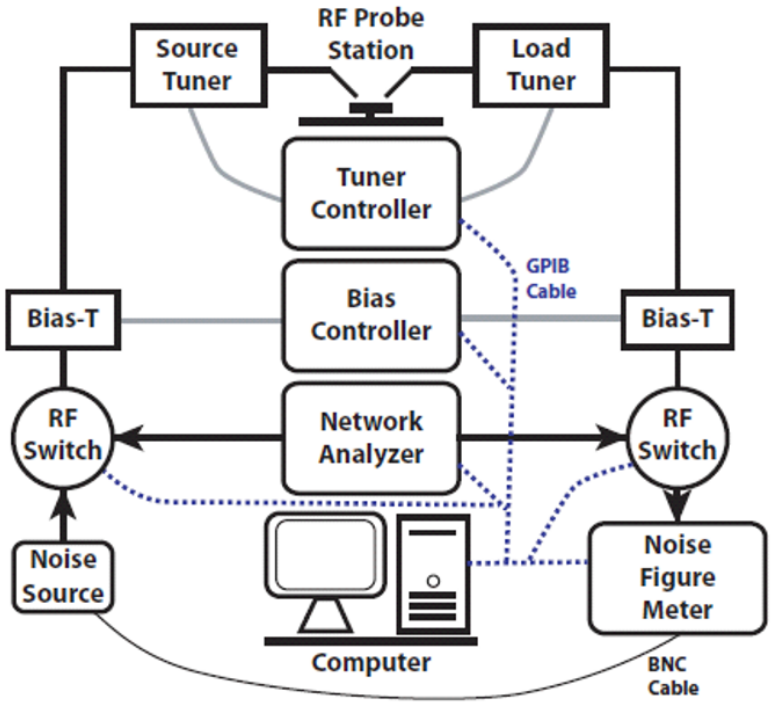


Figure 5-49: The device-level NF measurement-setup which employs source- and load-tuner to optimize the impedance to achieve NF_{min} and bias-Tees to apply required-bias [26]. The input is connected to a calibrated-noise-source and the output is connected to a noise-figure-meter. The noise-figure at each source-impedance can be calculated at different frequencies and bias-conditions.

The device-level noise-figure is dependent on the input-impedance and the source-impedance connected to the DUT. Minimum noise-figure (NF_{min}) is achieved when the input-impedance is conjugately-matched given by [26]:

$$NF = NF_{min} + 4\frac{R_n}{Z_0}\frac{|\Gamma_S - \Gamma_{matched}|^2}{(1-|\Gamma_S|^2)\,|1+\Gamma_{matched}|^2} \tag{5.6}$$

where R_n is the 'effective-slope' of the noise-paraboloid, Γ_S is the input-reflection-coefficient (determined by the Z_S) and $\Gamma_{matched}$ is the input-reflection-coefficient when the input-tuner-impedance is conjugately-matched to the input-impedance of the DUT ($Z_S = Z_{in}^*$) and $NF = NF_{min}$ under this input-matching. The setup described in Fig.5-49 enables to sweep the Z_S on the Smith-chart to find the NF_{min} at each bias-point and frequency.

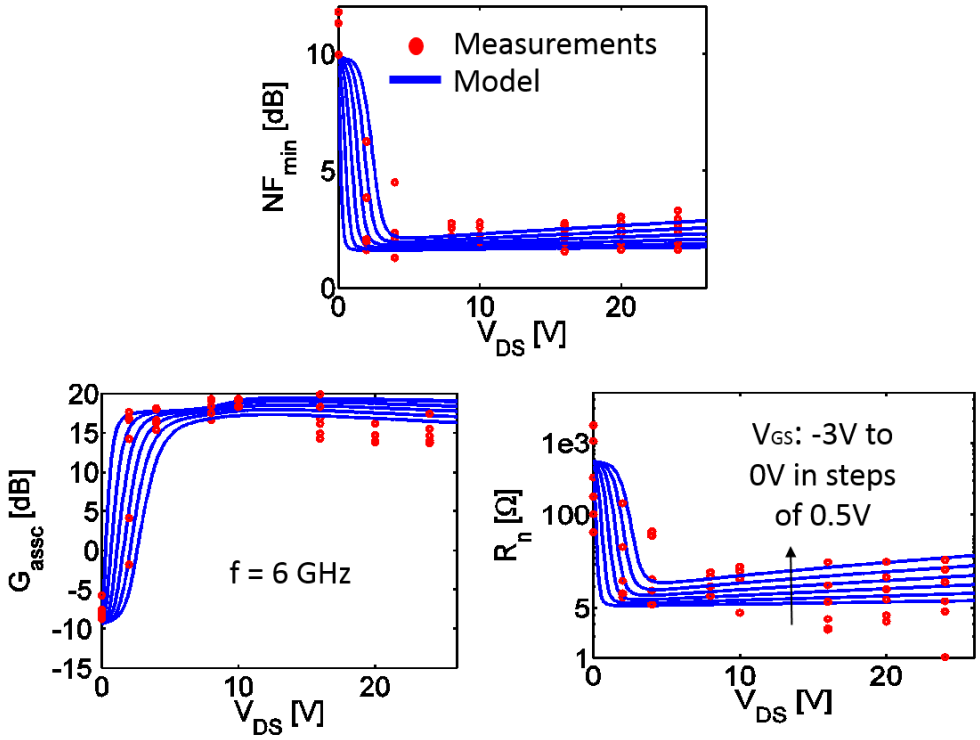


Figure 5-50: Device minimum-noise-figure (NF_{min}), associated-gain (G_{assc}) and noise-resistance (R_n) comparing the model results with measurements for the Wolfspeed-device are shown. At $V_{DS} = 12\ V$ and $V_{GS} = V_T + 0.15\ V$, $NF_{min} = 2\ dB$ and $G_{assc} = 15\ dB$ which is correctly predicted by the model.

The NF_{min} measurements are made on the Wolfspeed-RF-device using on-wafer Maury-Microwave noise-measurement-setup at 6 GHz. The noise-elements employed in the MVSG-model shown in Fig.4-11 are activated with the model-formulation described earlier used to describe these elements. The MVSG-model is benchmarked against measured minimum-noise-figure at various bias-points. Aside from the bias-dependent device-noise-figure (NF_{min}), gain (G_{assc}) and noise-resistance (R_n), the model is able to estimate the $NF_{min} = 2\ dB$ and $G_{assc} = 15\ dB$ at $V_{DS} = 12\ V$ and $VGS \approx V_T + 0.15\ V$ (Typical bias-points for LNA-design).

The validation of device-noise done in this section consists of only RF-noise sources which while sufficient for LNA-design is not enough for designing RF-receiver-components such as VCOs which also require low-frequency phase-noise characterization. The measurements of on-wafer device-level-phase-noise is challenging without a frequency-up-conversion and decoupling power-supply-noise (that requires batteries) and therefore the phase-noise validation is directly done at the circuit-level and is deferred to chapter 8.

5.14 Validation of mathematical-robustness

Model-validation against several device-level measurements spanning both HV- and RF-application-regime carried out upto this point indicates the ability of MVSG-model to estimate GaN-HEMT device-characteristics accurately making it a suitable tool for circuit-design. However a second requirement for a circuit-compatible compact-model is mathematical-robustness and convergence robustness. This issue was dealt with in the last-section of the previous-chapter and the results for the DC- and AC-symmetry tests for GaN-HEMT using MVSG-model are discussed here.

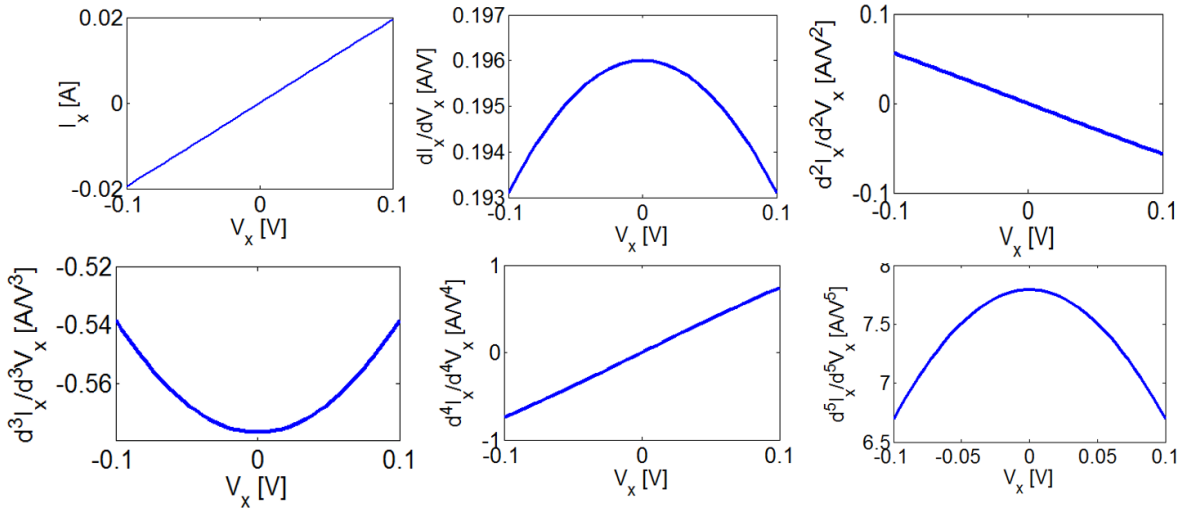


Figure 5-51: The results of DC-Gummel-symmetry tests for a symmetric-GaN-HEMT device (artificially constructed by setting $L_{gs} = L_{gd}$ showing continuity of I_X (described in the last chapter) and its higher-order derivatives around $V_{DS} = 0\ V$ indicating that the MVSG-model has no discontinuity issues.

The DC-Gummel-symmetry test results are shown in Fig.5-51 employing the test-circuit of Fig.4-14(a) for the MVSG-model calibrated against a typical GaN-HEMT but subsequently made symmetric by enforcing drain-access-region-parameters to have the same values as the corresponding source-access-region-parameters. As can be seen, the symmetric current-formulation adopted in the MVSG-model wherein the current-expressions depend on Q_{invs} and Q_{invd} in a symmetric-fashion, yields I_X of Fig.5-51 which has infinite-derivatives and thus passes the Gummel-symmetry-test. It is to be noted that I_X is an odd-function of V_X, and so are the odd-order-derivatives while the even-ordered-derivatives are even-functions of V_X with non-zero values at $V_X = 0$.

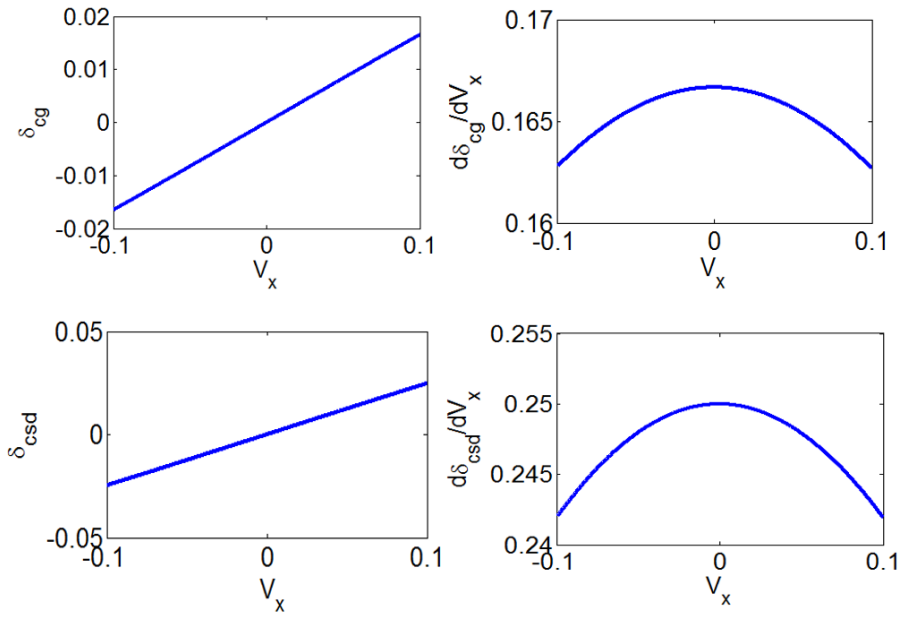


Figure 5-52: The results of AC-McAndrew-symmetry tests for a symmetric-GaN-HEMT device showing continuity of δ_{cg} and δ_{csd} (described in the last chapter) and its derivatives around $V_{DS} = 0\,V$ indicating that the MVSG-model has no discontinuities.

The second-set of mathematical-robustness-test pertains to the AC-symmetry tests (proposed by Colin McAndrew) as described in the last section of the previous chapter, and whose test-setup is given in Fig.4-14(b). The AC-tests determine the continuity-behavior of the charge-formulation in MVSG-model and hence the mathematical robustness of the model for dynamic-circuit-simulations. Both the gate-capacitance formulation (through δ_{cg}) and the drain-to-source capacitance for-

mulation (through δ_{csd}) are verified to be continuous from the results of these metrics and their derivatives shown in Fig.5-52.

The discussion on MVSG-model-validation in this chapter covers a broad-range of device-level characterization techniques and model-calibration against these measurements. Conclusions with regard to the accuracy and robustness of the MVSG-model can be verified through these validation steps. However true test of the usefulness of a compact model is its ability to accurately simulate realistic circuits and demonstrate accuracy against real-circuit-level measurement data which is a topic of discussion in Chapter 7. The added advantage of physical-models is that they can be used as tools for device-design by linking the performance bottlenecks to technology-parameters and providing feedback to device-engineers for a better device-design that has a positive impact at the circuit-level, which is discussed in the next Chapter.

Table 5.1: **Table 5.1: Key parameters for Fujitsu-HV-GaN-HEMT**

Parameter	Value	Description
W	100 μm	Gate-line-width
L_g	3 μm	Gate-length
L_{gd}	9.5 μm	Gate-to-drain access-region-length
L_{gs}	1 μm	Gate-to-source access-region-length
C_g	$1.3e-3$ F/m^2	Areal-gate-capacitance
v_{x0}	1.5e5 m/s	Velocity of carriers
R_{sh}	315 $\Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$1e-3$ $\Omega-m$	Contact-resistance of source/drain
V_{T0}	-7.78 V	Threshold-voltage
C_{ofs}, C_{ofd}	1.4 $fF/\mu m$	Fringing-capacitance
β	3	Linear-to-saturation parameter

Table 5.2: **Table 5.2: Key parameters for MIT-HV-GaN-HEMT**

Parameter	Value	Description
W	100 μm	Gate-line-width
L_g	2 μm	Gate-length
L_{gd}	16 μm	Gate-to-drain access-region-length
L_{gs}	1.5 μm	Gate-to-source access-region-length
C_g	$3.5e-3$ F/m^2	Areal-gate-capacitance
v_{x0}	1.1e5 m/s	Velocity of carriers
μ_0	0.16 m^2/Vs	Mobility of carriers
R_{sh}	480 $\Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$6e-4$ $\Omega-m$	Contact-resistance of source/drain
V_{T0}	-3.3 V	Threshold-voltage
δ	0.01	DIBL-parameter
SS	0.14 V/dec	Sub-threshold slope
β	1.5	Linear-to-saturation parameter
$C_{g,gfp}, C_{g,sfp}$	$3.0e-4$ F/m^2	Areal-gate-capacitance of GFP and SFP
$L_{g,gfp}$	3.0 μm	Gate-length of GFP
$L_{g,sfp}$	6.0 μm	Gate-length of SFP
$V_{T0,gfp}, V_{T0,sfp}$	-39 V	Threshold-voltage of FP
R_{th}	100 W/K	Thermal-resistance
C_{th}	100 sK/W	Thermal-capacitance
α_{T1}	1.9	Trap-voltage coefficient-1
ϵ	2.3	Mobility-self-heating-parameter

Table 5.3: **Table 5.3: Key parameters for Toshiba-HV-GaN-HEMT**

Parameter	Value	Description
W	$3e-3\ m$	Gate-line-width
L_g	$1\ \mu m$	Gate-length
L_{gd}	$7\ \mu m$	Gate-to-drain access-region-length
L_{gs}	$2\ \mu m$	Gate-to-source access-region-length
C_g	$1.7e-3\ F/m^2$	Areal-gate-capacitance
C_{ofs}	$1.6e-9\ F/m$	Gate-source fringing capacitance
C_{ofd}	$5.0e-12\ F/m$	Gate-drain fringing capacitance
C_{ofds}	$8.0e-10\ F/m$	Drain-source fringing capacitance
C_{ofgsub}	$3.0e-10\ F/m$	Gate-substrate fringing capacitance
v_{x0}	$1.2e5\ m/s$	Velocity of carriers
μ_0	$0.1\ m^2/Vs$	Mobility of carriers
R_{sh}	$100\ \Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$2.1e-3\ \Omega-m$	Contact-resistance of source/drain
V_{T0}	$-3.9\ V$	Threshold-voltage
δ	0.005	DIBL-parameter
SS	$0.1\ V/dec$	Sub-threshold slope
β	1.16	Linear-to-saturation parameter
C_{Igrs}	$8.0e-4\ F/m^2$	Areal- Implicit-gate-capacitance of source-access-region(SAR)
δ_{rs}	$4e-4$	DIBL-parameter of SAR
SS_{rs}	$0.065\ V/dec$	Sub-threshold slope of SAR
C_{Igrd}	$7.0e-4\ F/m^2$	Areal- Implicit-gate-capacitance of drain-access-region(DAR)
δ_{rd}	$4e-4$	DIBL-parameter of DAR
SS_{rd}	$0.08\ V/dec$	Sub-threshold slope of DAR
$C_{g,gfp}$	$2.0e-4\ F/m^2$	Areal-gate-capacitance of GFP
$C_{c,gfp}$	$9.00e-11\ F/m$	Cross-coupled-capacitance of GFP
$L_{g,gfp}$	$3.5\ \mu m$	Gate-length of GFP
$V_{T0,gfp}$	$-45\ V$	Threshold-voltage of GFP
$\mu_{0,gfp}$	$0.2\ m^2/Vs$	Mobility of carriers in GFP
SS_{gfp}	$0.2\ V/dec$	Sub-threshold slope of GFP
$C_{g,sfp}$	$9.0e-5\ F/m^2$	Areal-gate-capacitance of SFP
$C_{c,sfp}$	$6.5e-11\ F/m$	Cross-coupled-capacitance of SFP
$L_{g,sfp}$	$3.5\ \mu m$	Gate-length of SFP
$V_{T0,sfp}$	$-60\ V$	Threshold-voltage of SFP
$\mu_{0,sfp}$	$0.29\ m^2/Vs$	Mobility of carriers in SFP
SS_{sfp}	$4.1\ V/dec$	Sub-threshold slope of SFP
R_{th}	$15\ W/K$	Thermal-resistance
C_{th}	$1e-4\ sK/W$	Thermal-capacitance
$V_{T\zeta}$	$-1e-3\ 1/K$	Temperature-coefficient of threshold-voltage
v_ζ	$4e-3\ 1/K$	Temperature-coefficient of velocity
ϵ	3	Mobility-self-heating-parameter
τ_T	$3e-5\ s$	Trap-time-constant
V_{trap}	$230\ V$	Trap-threshold-voltage
α_{T1}	$1e-4$	Trap-voltage coefficient-1
α_{T3}	$21\ V$	Trap-voltage coefficient-3
θ_T	$1e-4\ 1/K$	Trap-temperature-coefficient

Table 5.4: **Table 5.4: Key parameters for MIT-RF-GaN-HEMT**

Parameter	Value	Description
W	$100\ \mu m$	Gate-line-width
L_g	$42\ nm, 105\ nm$	Gate-length
L_{gd}	$0.43\ \mu m, 0.46\ \mu m$	Gate-to-drain access-region-length
L_{gs}	$0.56\ \mu m, 0.46\ \mu m$	Gate-to-source access-region-length
C_g	$6.5e-3\ F/m^2$	Areal-gate-capacitance
C_{ofs}	$3.5e-2\ fF/\mu m$	Gate-source fringing capacitance
C_{ofd}	$3.5e-2\ fF/\mu m$	Gate-drain fringing capacitance
v_{x0}	$1.6e5\ m/s$	Velocity of carriers
μ_0	$0.165\ m^2/Vs$	Mobility of carriers
R_{sh}	$205\ \Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$0.24e-3\ \Omega-m$	Contact-resistance of source/drain
V_{T0}	$-3.5\ V, -3.19\ V$	Threshold-voltage
δ	$0.31, 0.12$	DIBL-parameter
SS	$0.26\ V/dec, 0.14\ V/dec$	Sub-threshold slope
n_d	$3.3, 0.4$	Punch-through factor
β	1.5	Linear-to-saturation parameter
R_{th}	$1.9\ W/K, 1.4\ W/K$	Thermal-resistance
θ_v	$0.21\ 1/V, 0.28\ 1/V$	Field-reduction of velocity
v_ζ	$0.28\ 1/K$	Temperature-coefficient of velocity
ϵ	2.3	Mobility-self-heating-parameter

Table 5.5: **Table 5.5: Key parameters for Qorvo-RF-GaN-HEMT**

Parameter	Value	Description
W	$90e-6\ \mu m$	Gate-line-width
n_{gf}	10	Gate-fingers
L_g	$150\ nm$	Gate-length
L_{gd}	$1.6\ \mu m$	Gate-to-drain access-region-length
L_{gs}	$1\ \mu m$	Gate-to-source access-region-length
C_g	$6.3e-3\ F/m^2$	Areal-gate-capacitance
C_{ofs}	$0.7pF$	Gate-source fringing capacitance
C_{ofd}	$0.06pF$	Gate-drain fringing capacitance
C_{ofds}	$0.2pF$	Drain-source fringing capacitance
v_{x0}	$1.0e5\ m/s$	Velocity of carriers
μ_0	$0.14\ m^2/Vs$	Mobility of carriers
R_{sh}	$150\ \Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$1e-4\ \Omega-m$	Contact-resistance of source/drain
V_{T0}	$-2.5\ V$	Threshold-voltage
δ	$8e-2$	DIBL-parameter
SS	$0.39\ V/dec$	Sub-threshold slope
β	2	Linear-to-saturation parameter
C_{Igrs}	$4.5e-2\ F/m^2$	Areal- Implicit-gate-capacitance of source-access-region(SAR)
δ_{rs}	0.1	DIBL-parameter of SAR
SS_{rs}	$0.065\ V/dec$	Sub-threshold slope of SAR
C_{Igrd}	$8.0e-3\ F/m^2$	Areal- Implicit-gate-capacitance of drain-access-region(DAR)
δ_{rd}	0.2	DIBL-parameter of DAR
SS_{rd}	$1.8\ V/dec$	Sub-threshold slope of DAR
R_{th}	$2\ W/K$	Thermal-resistance
C_{th}	$1e-4\ sK/W$	Thermal-capacitance
$V_{T\zeta}$	$-4e-4\ 1/K$	Temperature-coefficient of threshold-voltage
v_ζ	$1e-3\ 1/K$	Temperature-coefficient of velocity
ϵ	0.1	Mobility-self-heating-parameter
ϕ_B	$5\ V$	Schottky-barrier height
η	2	Low-injection ideality-factor
I_{gss}	1	Forward-current-reverse-saturation current of GS-diode
I_{gds}	1	Forward-current-reverse-saturation current of GD-diode
I_{recs}	$1e-18$	Reverse-current-reverse-saturation current of GS-diode
I_{recd}	$1e-18$	Reverse-current-reverse-saturation current of GD-diode
$V_{GSAT,rec}$	5	Saturation-current for reverse gate-current of GS-diode
η_{rec}	2	Low-injection ideality-factor of reverse-diode
R_G	0.92Ω	Gate-resistance
L_G	$11pH$	Gate-inductance
L_D	$17pH$	Drain-inductance
L_S	$21pH$	Source-inductance

Table 5.6: **Table 5.6: Key parameters for Wolfspeed-RF-GaN-HEMT**

Parameter	Value	Description
W	$180e-6\ \mu m$	Gate-line-width
n_{gf}	2	Gate-fingers
L_g	$250\ nm$	Gate-length
L_{gd}	$4.85\ \mu m$	Gate-to-drain access-region-length
L_{gs}	$3\ \mu m$	Gate-to-source access-region-length
C_g	$4.0e-3\ F/m^2$	Areal-gate-capacitance
C_{ofs}	$80fF$	Gate-source fringing capacitance
C_{ofd}	$20fF$	Gate-drain fringing capacitance
C_{ofds}	$40fF$	Drain-source fringing capacitance
v_{x0}	$1.3e5\ m/s$	Velocity of carriers
μ_0	$0.15\ m^2/Vs$	Mobility of carriers
R_{sh}	$150\ \Omega/square$	Sheet-resistance of channel
R_{cs}, R_{cd}	$8e-4\ \Omega-m$	Contact-resistance of source/drain
V_{T0}	$-2.79\ V$	Threshold-voltage
δ	$4e-3$	DIBL-parameter
SS	$0.08\ V/dec$	Sub-threshold slope
β	1.5	Linear-to-saturation parameter
C_{Igrs}	$1.0e-3\ F/m^2$	Areal- Implicit-gate-capacitance of source-access-region(SAR)
C_{Igrd}	$1.0e-3\ F/m^2$	Areal- Implicit-gate-capacitance of drain-access-region(DAR)
R_{th}	$30\ W/K$	Thermal-resistance
C_{th}	$1e-4\ sK/W$	Thermal-capacitance
$V_{T\zeta}$	$-4e-4\ 1/K$	Temperature-coefficient of threshold-voltage
v_ζ	$1e-3\ 1/K$	Temperature-coefficient of velocity
ϵ	2.3	Mobility-self-heating-parameter
ϕ_B	$1\ V$	Schottky-barrier height
η	2	Low-injection ideality-factor
I_{gss}	$0.49A/m$	Forward-current-reverse-saturation current of GS-diode
I_{gds}	$0.49A/m$	Forward-current-reverse-saturation current of GD-diode
R_G	1Ω	Gate-resistance
L_G	$10pH$	Gate-inductance
L_D	$10pH$	Drain-inductance
L_S	$10pH$	Source-inductance
K_f	$7e-16$	Flicker-noise pre-factor
af	2	Flicker-noise drain-current parameter
ffe	1.4	Flicker-noise frequency-exponent

Chapter 6

Device Technology Optimization Using the MVSG Model

Compact models for semiconductor devices primarily serve as tools that enable circuit design but models that are based on device physics have an added advantage as they link the device behavior to technology parameters. This feature can prove to be advantageous in linking the process-technology conditions to device behavior and ultimately to circuit performance. In this chapter, the MVSG model that is calibrated against a wide range of HEMTs fabricated using both academic and industrial process-technologies described in chapter 5, is used to analyze technology-bottlenecks to the device performance metrics. This can be valuable feedback to technology-engineers to improve their device-design targeting either RF- or HV-applications.

The HV-applications demand power-FETs that have good switching figures-of-merit (FoMs) that require optimizing the device-geometry and FP-parameters to lower the R_{on}, Q_g and enhance BV. The MVSG model is used to accomplish this and is described in the first-half of this chapter. The second-half of the chapter deals with the optimization of RF-device geometry parameters such as access-region lengths, device-capacitances and back-barriers on the small- and large-signal device behavior targeted to amplifier design. Additionally, the impact of thermal and trapping effects on both RF- and HV-device behavior is analyzed.

6.1 Modification of MVSG model to aid FP-design

The MVSG model developed in the thesis so far captures the carrier-transport in different regions of the device by adopting a sub-circuit modeling approach with transistor elements connected in series as shown in Fig.4-5(c). The consequence of this method is that, while potential-continuity is ensured at each internal-node, the carriers are assumed to undergo complete thermalization, thus losing their kinetic energy at the nodes. This assumption is not realistic since the carriers entering each transistor-region have non-negligible energy, particularly when entering the drain-access region after gaining significant energy in the depletion-region at the drain-edge of the intrinsic-transistor region. Field-continuity in addition to the potential-continuity is therefore necessary to accurately estimate the field-profile in different regions of the device thereby enabling the MVSG model as a tool for optimizing the FP-parameters. Field-continuity is not expected from standard compact models for circuit-design since formulations to meet the field-continuity requirements are typically computationally expensive and not robust from a convergence point-of-view. Therefore the formulation derived in this chapter, which ensures field-continuity in the MVSG model is an additional feature only to be used for device-level simulations for technology-optimization. The computation of lateral-field in the channel is

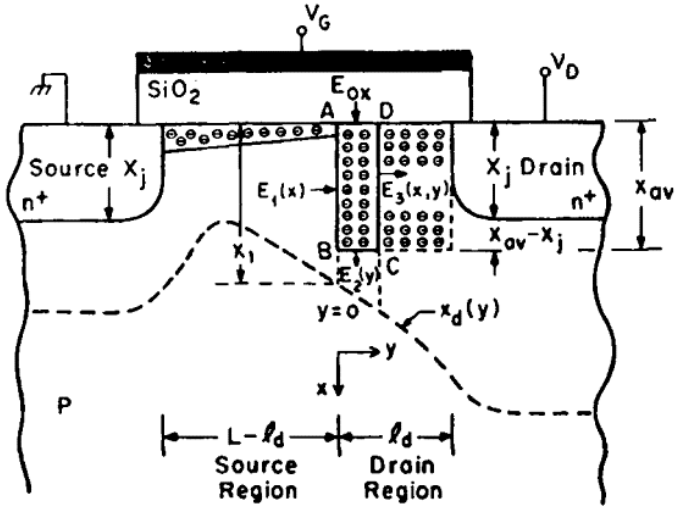


Figure 6-1: The Gaussian-pill-box (ABCD) chosen in [66] to solve for the electric-fields in the depletion-region near the drain-edge of the gate in a FET by simplifying the 2D-Poisson equation in the region. The analysis done for classic-FETs in [66] is modified for GaN-HEMTs in this thesis.

straightforward in the regions where gradual-channel-approximation (GCA) is valid and can be obtained from the channel-current formulation derived in chapter 4. However the derivation of lateral-field at the drain-end of each transistor-element in the device where the GCA fails, requires solution to the 2D-Poisson equation in the depletion and velocity-saturated regions. In this section, an analytical approximate solution to the 2D-Poisson equation in such depletion regions is derived with suitable modifications to the approach followed in [66] to be consistent with the physics of GaN-HEMTs. The Gaussian pillbox in the depletion region is drawn as shown in Fig.6-1 where y is the direction along the channel and x is the direction along the heterostructure. The total electric-flux from the Gaussian-pillbox of the figure is:

$$\begin{aligned} F_E = \int_{x=0}^{x=xav} \epsilon_s E_y(y_0+dy)dx - \int_{x=0}^{x=xav} \epsilon_s E_y(y_0)dx \\ + \int_{y=y_0}^{y=y_0+dy} \epsilon_s E_x(x=xav)dy - \int_{y=y_0}^{y=y_0+dy} \epsilon_{ox} E_x(x=0)dy \end{aligned} \tag{6.1}$$

where ϵ_s is the permitivity of the channel-material (GaN) and ϵ_{ox} is the permitivity of the heterostructure-insulator (AlGaN). The Guassian-pillbox starts at $x = 0$ which is the heterostructure interface in the insulator and ends at $x = xav$ with $\boldsymbol{xav}$ representing the thickness of the depletion region and is a fitting parameter in the MVSG model. $\boldsymbol{xav}$ unlike in MOSFETs is not determined by the junction-depth of source- and drain-contacts in GaN-HEMTs. y_0 is the starting co-ordinate of the pillbox along the channel-direction and dy is its width. The total charge enclosed in the pillbox is given by

$$Q = -q \int_{x=0}^{x=xav} \int_{y=y_0}^{y=y_0+dy} (n+N_A)dxdy \tag{6.2}$$

Here the positive charges (such as the concentration of holes p) are assumed to be low in the GaN-channel. Equating the two sides and differentiating with respect to y yields:

$$\epsilon_s xav \frac{E_y}{dy} - \epsilon_{ox} E_x(x=0) + \epsilon_s E_x(x=xav) = -qxav(n+N_A) \tag{6.3}$$

In the above equation $\epsilon_{ox}E_x(x=0) = C_g(V_G - V_y)$. In order to obtain analytical closed form solution to E_y in the depletion region, we have to make the simplifying assumption that $E_x(x = xav)$ is constant along the channel in the depletion region, which reduces the above equation to a pseudo-2D-Poisson equation. If L_{clm} is the length of the non-GCA region and the effective gate-length where GCA is valid is given by $L_{eff} = L_g - L_{clm}$, then at $y = L_{eff}$ (i.e. at the beginning of the depletion region) the above equation can be written as:

$$\epsilon_s xav \frac{E_y}{dy}|_{y=L_{eff}} - C_g(V_G - V_{y=L_{eff}}) + \epsilon_s E_x(x = xav) = -qxav(n + N_A) \tag{6.4}$$

Since GCA is still valid at the beginning of the depletion region, the first term in the above expression is zero and $V_{y=L_{eff}} = V_{DSAT}$. Combining the above two expressions we get:

$$\epsilon_s xav \frac{E_y}{dy}|_{y=L_{eff}} - C_g(V_y - V_{DSAT}) = 0 \tag{6.5}$$

The solution to this pseudo-2D-Poisson equation is given by:

$$E_y = E_{sat} cosh(\frac{y - L_{eff}}{\Lambda}) \tag{6.6}$$

where $E_{sat} = I_D/(W n_{gf} \mu)$ is the saturation-field at the beginning of the depletion region with $\Lambda = \sqrt{(xav\epsilon_s/C_g)}$ and the potential along the channel is given by:

$$V_y = V_{DSAT} + E_{sat}\Lambda sinh(\frac{y - Leff}{\Lambda}) \tag{6.7}$$

and the total voltage drop across (V_{clm}) the depletion region is given by:

$$V_{clm} = E_{sat}\Lambda sinh(\frac{L_{clm}}{\Lambda}) \tag{6.8}$$

The analysis done here is applicable to each transistor-element in the device and is shown for the intrinsic-transistor and the drain-access transistor in Fig.6-2. For the intrinsic-transistor, $V_{clm} = V_{DiSi} - F_{sat}V_{DSAT}$ and the length of depletion region is

given by:

$$L_{clm} = \Lambda sinh^{-1}(\frac{V_{DiSi} - F_{sat}V_{DSAT}}{E_{sat}\Lambda}) \tag{6.9}$$

The physical gate-length (L_g) used in the current-formulation of intrinsic-transistor that is derived in chapter 4 is replaced with L_{eff} and L_{clm} and their increase with V_{DS} captures the channel-length-modulation in GaN-HEMTs. The carriers reaching the drain-edge of the intrinsic-transistor face an electric-field given by:

$$E_{y=L_g} = E_{Di} = E_{sat}cosh(\frac{L_{clm}}{\Lambda}) \tag{6.10}$$

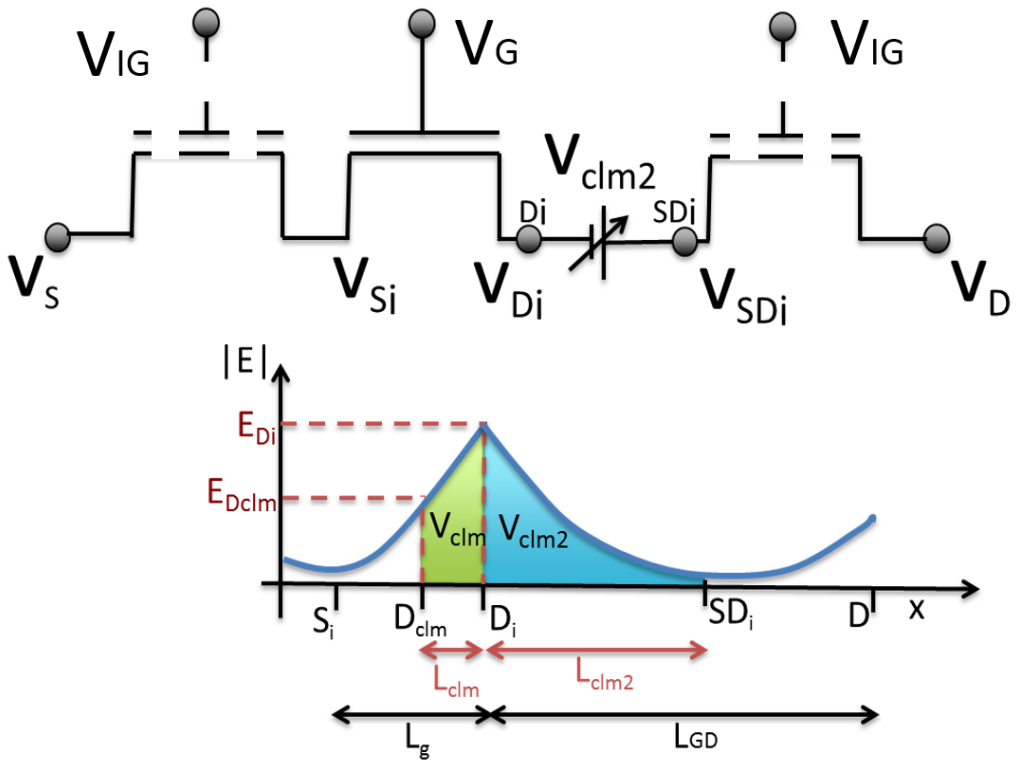


Figure 6-2: Equivalent-circuit implementation of the model that enables field-continuity between intrinsic-transistor and drain-side implicit-gate transistor. The lateral field profile between these two regions showing a non-GCA region in the drain access-region which is modeled with the help of a dependent voltage source V_{clm2}.

Since these electric-fields are high, the carriers have sufficient kinetic energy while entering the drain-side implicit-gate transistor and require a finite-length (L_{clm2}) to thermalize to velocities that are small enough for the validity of GCA. The length

L_{clm2} is given by:

$$L_{clm2} = L_{clm}\sqrt{\frac{C_g}{C_{Ig}}} \tag{6.11}$$

this length is subtracted from the gate-length (L_{gd}) of the drain access-region for the current-formulation in this transistor-element and the voltage drop in this region is given by V_{clm2} as below:

$$V_{clm2} = V_{clm}\sqrt{\frac{C_g}{C_{Ig}}} \tag{6.12}$$

This approach ensures field-continuity between different transistor elements in the device and is extended to other transistor elements including the FP-transistors. The MVSG model that includes field-continuity formulation discussed in this section can be used to perform device-level optimization for HV-devices described in the next section.

6.2 Optimization of FP-parameters for switching-FoM

HV-GaN HEMTs often employ multiple FPs in the drain-access region to augment the BV of the device by engineering the electric-fields. The principle of operation of these FPs along with the approach to capture their behavior using the MVSG sub-circuit method were discussed in chapters 3 and 4. It was also shown that the thickness of dielectric-layers in the FPs (t_d) and the length of FPs (L_{fp}) are key design parameters that determine the turn-off of the FP-transistors and hence their BV augmentation capability.

Optimization of FP-parameters for a given process-recipe and a target-BV is critical to yield devices with the desired performance, which can be done by varying the device-layout and heterostructure (by trial and error) and choosing the structure that yields the best FoM. However optimizing L_{fp} for a given L_{gd} requires laying out test-structures with varying L_{fp} on the same die while optimizing t_d requires different deposition-thickness of FP-dielectric and is expensive to fabricate in a single run (as it requires multiple masks). For a device with n-FPs, a total of 2^n variables (L_{fp} and t_d for each FP) are to be optimized that further increase the optimization-complexity.

An alternative is to run TCAD-simulations which requires accurate calibration with the right set of physics-parameters and validation against a few experimental data points, but these simulations are computationally expensive and time consuming. In this context, the MVSG model with modifications highlighted in the previous section to model the electric-field in the device, can be used as a simple optimization tool to determine the best FP-parameters to maximize the FoM.

6.2.1 Optimization of FP-lengths

The FP-length (L_{fp}) is an important device-design parameter since FP-transistor with highly scaled L_{fp} would suffer from SCE and punch-through making it incapable of blocking significant off-state voltage. On the other hand, longer L_{fp} comparable to L_{gd} can also result in premature breakdown in the device due to the close proximity between drain- and gate-metal of the FP-transistor. Therefore from the BV point-of-view there is clearly an optimum L_{fp}. The R_{on} of the device has a direct dependence on the L_{fp} since the n_s in the channel beneath the FP-metal is lower than in the un-gated access-region, thus causing R_{on} to increase with the L_{fp}. A similar dependence is observed on the Q_g-dependence on L_{fp}, particularly for the GFP-transistor as it adds to the gate-capacitance of the device, which increases with L_{fp}. The switching figure-of-merit of the HV-HEMT that takes into account both static-power loss (due to R_{on}) and dynamic-power loss (due to Q_g) in HV-switches is given by [1]:

$$FoM = \frac{BV^2}{R_{on}Q_g} \tag{6.13}$$

From the above equation it is clear that the best-optimized HV-GaN-HEMT is the one with the highest BV, the lowest Q_g and R_{on} that maximizes the FoM. The MVSG model that is calibrated against HV-GaN-HEMT with the parameters listed in Table.5.2 is used to demonstrate the device FP-optimization to minimize R_{on}, Q_g and maximize BV, and FoM as a function of L_{FP} as shown in Fig.6-3.

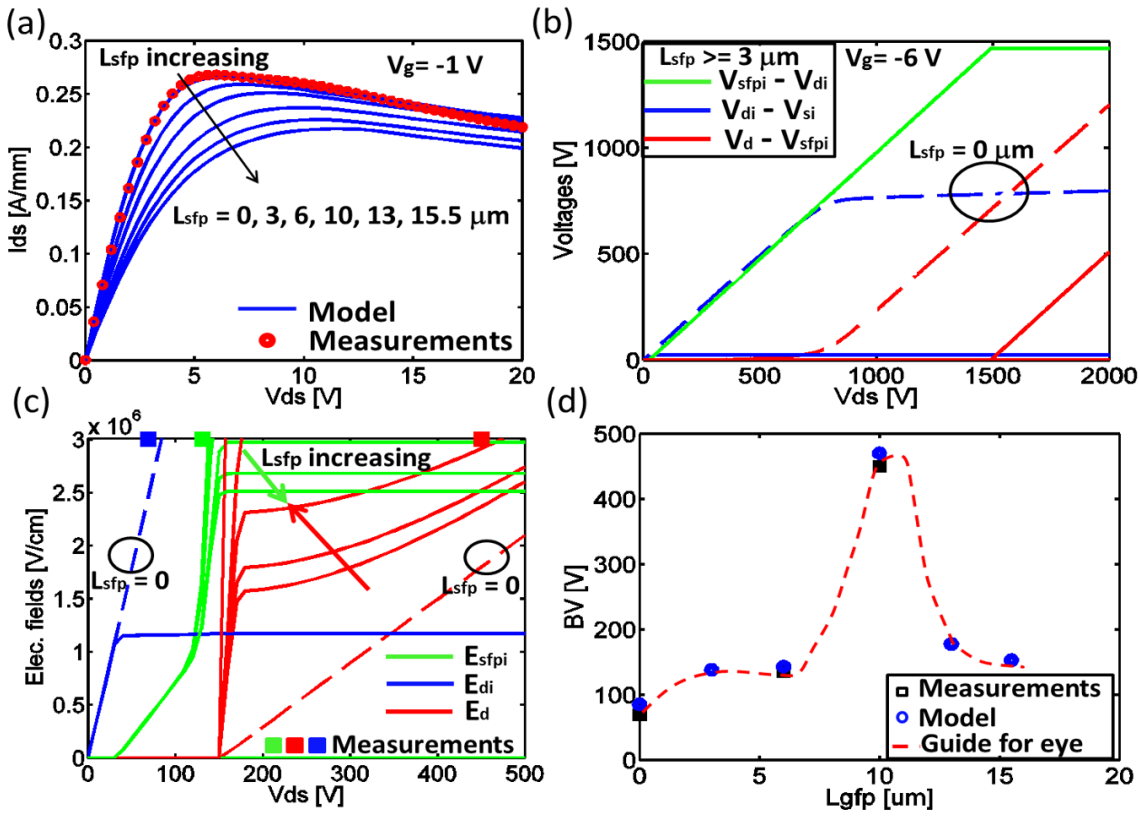


Figure 6-3: (a) The increase in R_{on} with increasing FP-length is demonstrated using the model for the SFP-device fabricated at MIT with $L_{gd} = 16\ \mu m$. As L_{sfp} is made longer, the drain access-region resistance increases due to the 2DEG depletion below the increasingly longer FP-region. (Here $V_{T0,sfp}$ is increased from $-39\ V$ to $-19\ V$ to show a clear increase of R_{on}) (b) The off-state voltage distribution in different regions of the device is affected by FP but shows no change for $L_{sfp} >= 3\ \mu m$. (c) The peak electric-field distribution changes significantly with L_{sfp}. As L_{sfp} is increased, the BV field ($\approx 3\ MV/cm$) shifts from the SFP-edge (with $E_{sfpi} = 3\ MV/cm$) to the drain-edge (with $E_d = 3\ MV/cm$), increasing the BV. (d)The BV predicted by the model matches closely with the measured BV (data-points). Since there is a trade-off between R_{on} and BV, the FoM ($BV^2 G_{on}$) has an optimum maximum point at $L_{sfp} = 10\ \mu m$. Device courtesy: Daniel Piedra, MIT

The benchmarked model with a SFP-transistor is used in Fig.6-3 to study the R_{on} vs. BV trade-off that exists in FP-design. From Fig.6-3(a) it is clear that R_{on} increases with FP-length (L_{sfp}) for a given L_{gd} as more of the drain access-region is covered by the field plate with lower 2DEG density (n_s). The potential distribution in different regions of the device shown in Fig.6-3(b) are significantly affected by the presence of FPs but show no change with the length of the field plate (L_{sfp}) due

to pinch-off in different regions. The peak fields however, change with L_{sfp} and can be used to estimate the BV as a function of L_{sfp} (BV is the voltage when peak electric-field in the device reaches 3 MV/cm). Without FP, the device breaks at the gate-edge at a low BV of about 65 V as seen in Fig.6-3(c) and the BV is about 110 V for $L_{sfp} = 6$ μm, with the breakdown field occurring at the FP-edge. As L_{sfp} is increased, the peak-field in the FP-region (E_{sfpi}) drops while the field at drain-edge (E_d) rises. At $L_{sfp} = 10$ μm, breakdown shifts to the drain-edge and $BV = 450$ V can be achieved. Beyond this length, E_d continues to rise, causing breakdown to be reached at lower voltage. The optimum L_{sfp} of 10 μm in this particular case, can be found from the plot of BV, as shown in Fig.6-3(d).

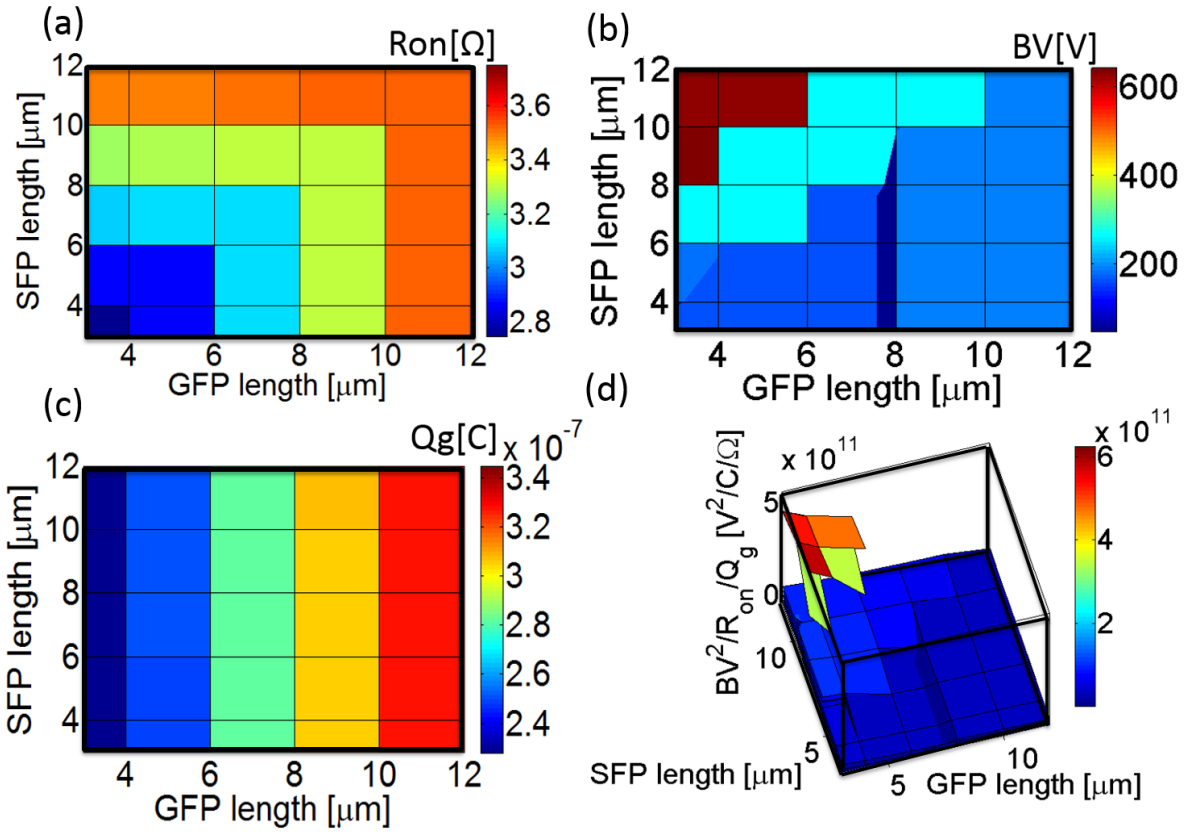


Figure 6-4: Two-parameter optimization of the device switching performance metrics as a function of GFP- and SFP-lengths. (a) R_{on} increases as GFP-gate-length (L_{gfp}) and/or SFP-gate-length (L_{sfp}) increases due to the reduction in 2DEG in FP-regions. (b) BV has a narrow window of optimum L_{sfp} and L_{gfp} when it is maximum. (c) Q_g is highest at the longest GFP gate-length due to higher gate-capacitance. (d) The resulting $BV^2/R_{on}Q_g$ FoM vs. GFP- and SFP-lengths from the model can give the optimum values of FP-lengths for device design.

The optimization is extended to HV-GaN-HEMTs with multiple FP-regions by using the MVSG model that is calibrated against Toshiba HV-GaN-HEMT with parameters listed in Table.5.3. Since the device has a GFP- and SFP-transistor, the optimization is dependent on two-variables; as a function of L_{gfp} and L_{sfp}. By running the off-state V_D-sweep simulations for the device for each combination of L_{fp} and recording the V_{DS} when the electric-field at any point in the device reaches 3 MV/cm (this V_{DS} is considered as the BV), the variation of BV as a function of L_{gfp} and L_{sfp} can be obtained. The on-state ($V_{GS} = 0\ V$) simulations are done in a similar fashion to obtain R_{on} and Q_g as a function of L_{gfp} and L_{sfp} and the results are highlighted in the plots of fig.6-4.

The R_{on} increases with L_{fp} for both GFP- and SFP-transistors as the effective-R_{sh} in the drain access-regions increases with L_{fp}. Highest R_{on} is obtained at the longest L_{fp} as can be seen in Fig.6-4(a). The Q_g also increases with L_{fp} especially with L_{gfp} since the increase in effective gate-capacitance in the GFP-transistor adds to the total Q_g of the device as shown in Fig.6-4(c). The BV of the device has a narrow-range of L_{fp} when it is maximized, as observed from Fig.6-4(b). For very short L_{gfp} there is premature-breakdown in GFP and the same is the case for short L_{sfp}. Long L_{sfp} reduces the BV due to breakdown in the drain access-region as explained for MIT-devices. The switching FoM is maximized at a narrow range of L_{fp} for a given L_{gd} as can be seen from Fig.6-4(d).

6.2.2 Optimization of FP-dielectrics

The optimization of BV, R_{on}, Q_g and switching FoM as a function of FP-t_d is demonstrated using Toshiba devices with the MVSG model calibrated against the measured IV and CV-characteristics as described in the last chapter with the parameters given in Table.5.3. Compared to the optimization using the method of trial-and-error fabrication-process, using the MVSG-model as a tool to perform the optimization is faster and hence can be employed to narrow-down the design-range for the final-fabrication. The dielectric-thickness of GFP (GFP-t_d) determines $V_{T0,gfp}$ while the dielectric-thickness of SFP (GFP-t_d + SFP-t_d in the figure) determines $V_{T0,sfp}$ which

set the depletion of these regions and hence the BV of the device. Optimization of Toshiba HV-GaN-HEMTs with respect to t_d of GFP- and SFP-transistors are shown in Fig.6-5. Here the R_{on} is seen to increase as t_d decreases since the n_s in the FPs reduce as the FP-gate-metal is placed closer to the 2DEG. The gate-charge (Q_g) in Fig.6-5(c) also increases as t_d decreases since the effective-gate-capacitance of the FP increases thus adding to the gate-capacitance and Q_g. GFP has a more significant contribution to the Q_g compared to SFP as can be seen. The BV shown in Fig.6-5(b) has a narrow optimization-window in terms of FP-t_d, where it is maximum. If the FP-t_d are high, the V_T of the FP are large-negative in value which means the FPs do not deplete in the off-state and low-BV is observed in the intrinsic-transistor-region (as if the FPs are absent). If t_d are very thin, the V_T of the FPs are low in magnitude and hence the FPs undergo premature depletion and BV as seen from the figure.

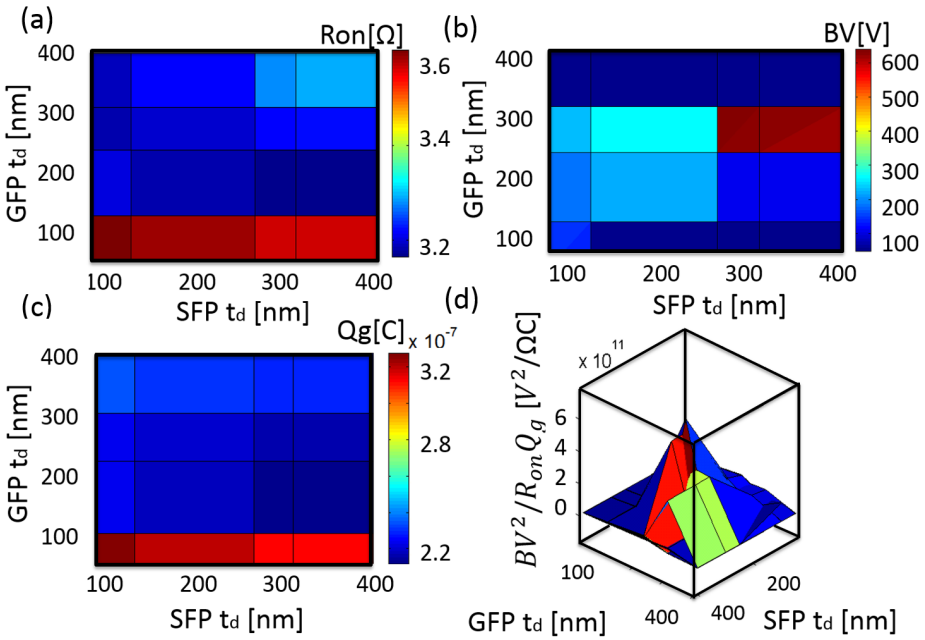


Figure 6-5: Two-parameter optimization of the device switching performance metrics as a function of GFP- and SFP-t_d. (a) R_{on} increases as FP-t_d decreases due to reduction in 2DEG in FP-regions. (b) BV has a narrow window of FP-t_d when it is maximum (600 V). Very thin FP- t_d causes premature pinch-off in those regions, reducing BV and thick t_d makes FPs ineffective causing premature-breakdown of the intrinsic-gated-region. (c) Q_g is highest at the lowest t_d due to higher gate-capacitance. (d) The resulting $BV^2/R_{on}Q_g$ FoM vs. GFP- and SFP- t_d from the model can give the optimum values of FP t_ds for device-design.

6.3 Optimization of device-geometry for small-signal performance

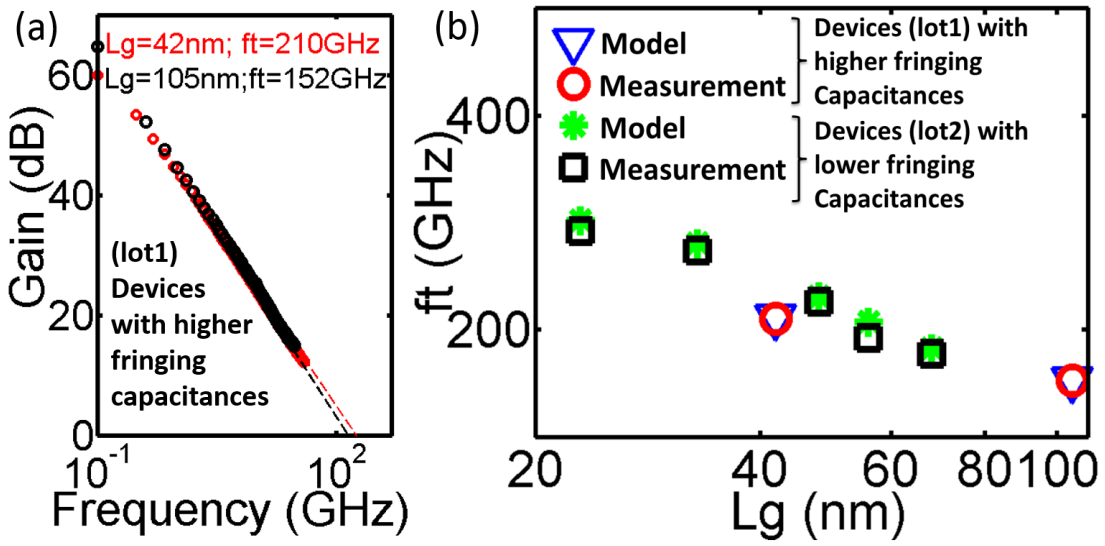


Figure 6-6: (a) Current-gain (h_{21}) dependence on frequency. De-embedded f_T from S-parameters are extracted for $L_g = 42 - nm$ and $105 - nm$ devices (lot 1). (b) De-embedded f_T obtained from S-parameters are compared with f_T estimated by model for $L_g = 42 - nm$ and $105 - nm$ devices (lot 1). The model also fits well with another set of similar devices with somewhat lower fringing capacitances (lot 2). Details of fringing capacitances can be found in [64]. (Passivation layer thickness is 10 nm) Device courtesy: Dong Seup Lee, MIT

In the RF-application regime, the MVSG model can be used to study the effect of different device-technology parameters on the devices' small- and large-signal behavior. The devices used for this study are the MIT RF-devices of $L_g = 42\ nm$ and $L_g = 105\ nm$ discussed in the last chapter against whose device-characteristics the MVSG model is calibrated, with the parameters listed in Table.5.4. The small-signal device performance metrics for HF RF-devices are f_T and f_{max} and the MVSG model is first tested in its ability to accurately estimate f_T measurements of fabricated devices as shown in Fig.6-6(a). As can be seen from the figure, $42 - nm$ and $105 - nm$ devices exhibit f_T of 210 GHz and 152 GHz respectively which at the time of publication set a record in f_T among high-speed GaN-based HEMTs. The model is capable of accurately estimating the f_T of this technology of devices as evident from Fig.6-6(b) for two lots of devices. Lot 1 has higher fringing-capacitances due to the

process-technology used while lot 2 has lower fringing-capacitances thus yielding high f_T for the same L_g. The calibrated MVSG model is able to estimate the f_T of these devices from $152 - 300\ GHz$ for $L_g = 28 - 105\ nm$ and can be used to study the impact of device-technology parameters on the f_T.

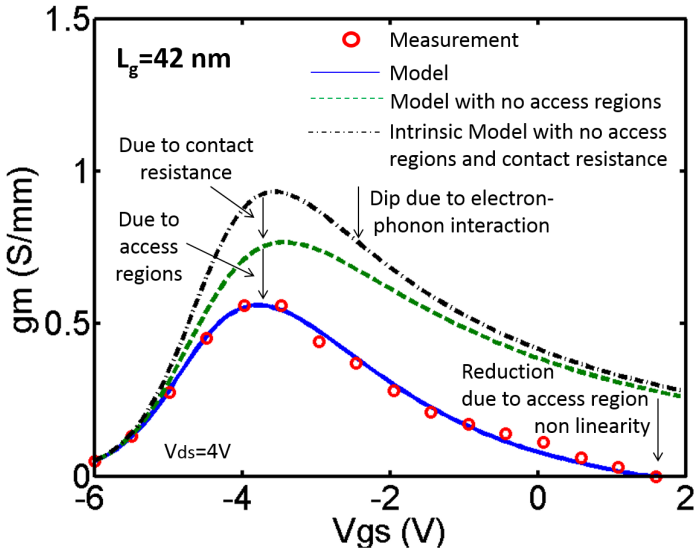


Figure 6-7: Effect of access-region and contact-resistances on g_m. Intrinsic, $g_{m,int}$ (black dot-dash line) has 66% higher peak value than extrinsic g_m (blue solid line). Dip after the peak in g_m is present even in the intrinsic g_m due to Q_{ixo}-dependent velocity. Extrinsic peak g_m is reduced from the peak of intrinsic g_m due to both contact and access resistances. The increased resistance due to the non-linearity of access-regions at high V_{GS} causes sharper g_m reduction.

From the analysis of f_T in chapters 3 and 4, it is clear that the g_m of the device is an important determinant of the device-f_T and hence technology parameters that affect g_m also impact the f_T. The g_m fits for the MIT-devices shown in chapter 5 indicate that there is a slight reduction in the peak g_m in the $42 - nm$ device when compared with the $105 - nm$ device, due to increased short-channel-effects (SCE) such as DIBL, degraded SS and modest punch-through. f_T improvement with scaling would therefore require suppression of SCE. Contact- and access-region resistances also have a significant impact on the peak g_m as shown in Fig.6-7. The model shows 66% reduction in the peak g_m compared to intrinsic, $g_{m,int}$, which can be decreased by reduction of contact resistance and gate self-alignment. However, sharp drop in g_m above certain V_g is due to depletion-effects in the access-regions

along with Q_{ixo}-dependent v_{x0}, which could be due to interface-scattering and optical-phonon effects [67]. The latter is a GaN-material specific phenomenon and cannot be eliminated through device scaling. The key-learning from Fig.6-7 is that g_m and hence f_T decreases sharply with V_G in the on-state and cannot be made uniform with gate-bias since part of it is material-dependent property. The peak g_m and hence peak f_T can be boosted through self-alignment and suppression of SCE. In addition to g_m, the device-capacitances also play a significant role in determining the device-f_T and the technology-innovations that can boost f_T in this regard are explained next.

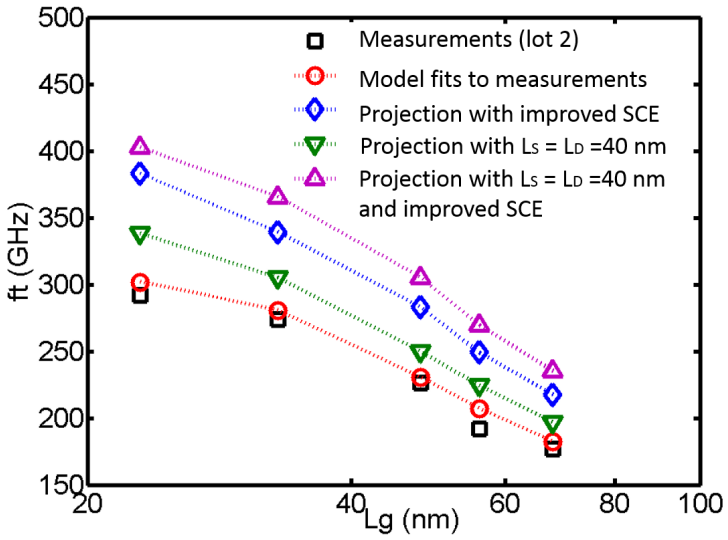


Figure 6-8: Projection of f_T assuming suppressed SCE and/or scaled L_S and L_D with lot 2 devices as baseline devices. At $L_g = 23\ nm$, f_T of 338 GHz is achieved if L_S and L_D are scaled down to 40 nm to reduce the source/drain resistance while maintaining the same SCE as in the baseline technology. On the other hand, if SCE could be improved ($DIBL = 150\ mV/V$ and $SS = 150\ mV/dec$) by possible technology innovations such as back barrier[19] while L_S and L_D are kept identical as in the baseline devices, f_T is boosted to 383 GHz. Assuming a scenario with both suppressed SCE and scaled L_S and L_D, f_T at $L_g = 23\ nm$ can be further increased to 402 GHz, according to the model.

Since f_T is an important FoM for RF-applications, it is possible to study the impact of the various technology innovations using the model, that could result in improved f_T in the device without having to resort to L_g scaling. This is explained in Fig.6-8; as shown, scaling-down source access-region (L_S) and drain access-region (L_D) along with suppressing short-channel-effects (SCE) can both effectively improve

f_T. Scaling-down L_S and L_D reduces R_S and R_D, which essentially decreases parasitic delay and thus improves f_T. Suppressing SCE, on the other hand, enhances f_T by increasing $g_{m,int}$ while reducing g_o. With $L_S + L_D = 1\mu m$, and poor SCE ($DIBL = 380\ mV/V$ and $SS = 260\ mV/dec$) at $L_g = 23\ nm$, the baseline technology (lot 2) provides f_T of 290 GHz. Scaling L_S and L_D to 40 nm, which can be potentially achieved by adopting self-aligned structure [68], would help in boosting f_T to 340 GHz. Recent technology advancements such as the use of back-barriers have resulted in suppression of SCE [19]. Using the model and assuming improved $DIBL = 150\ mV/V$ and $SS = 150\ mV/dec$, f_T can be increased to 380 GHz. Devices combining the two improvements are expected to show f_Ts of above 400 GHz at $L_g = 23\ nm$. The physical-grounding of the MVSG model enables these kind of technology projections on device performance which can be extended to large-signal device behavior as discussed in next section.

6.4 Optimization of device-geometry for large-signal performance

GaN-HEMTs used in power-amplifier design should deliver high P_{out} with high PAE together with good-linearity but these requirements directly trade-off against each other. At high P_{out} conditions, the signals at the output are pushed into device-compression regimes thus compromising linearity. Technology innovations to improve the design space of high P_{out} and linearity PAs require physical models such as the MVSG model to link technology parameters to circuit performance. This is demonstrated in this section by using the model calibrated against Wolfspeed (a Cree company) devices with parameters listed in Table.5.6. The calibrated model is used to make projections linking key device-level bottlenecks to the RF-device performance, as shown in Fig.6-9. The device access-regions are responsible for gain-compression at high input-power and the model predicts that self-aligned devices could potentially boost PAE by 40% by increasing P_{out} in compression. The onset of compression

is delayed in such self-aligned devices and is pushed to higher P_{out} as can be seen. Fabrication technologies that yield lower gate-parasitic fringing capacitances are beneficial as well, with the limiting case of zero fringing capacitances yielding enhanced $G_t = 33\ dB$ and $PAE = 60\%$. Reducing device-capacitances boost the low-power-G_t and hence P_{out} in the linear-regime thereby improving the device large-signal performance.

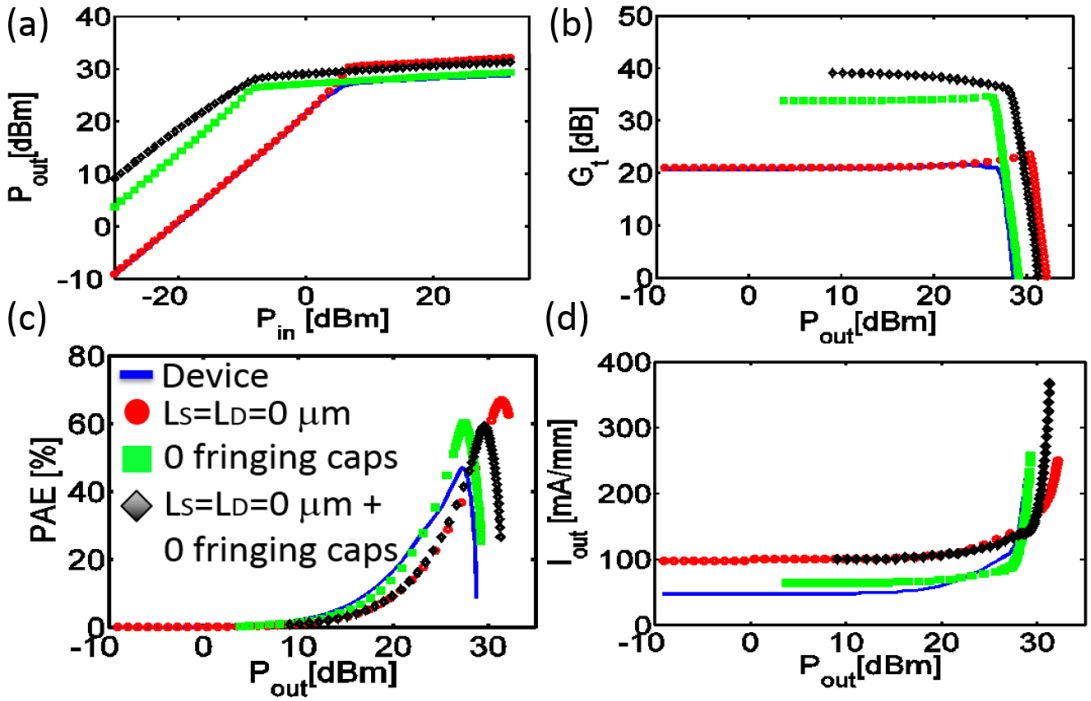


Figure 6-9: Large signal metrics such as P_{out}, G_t, PAE and I_{out} of commercial GaN-HEMT compared against the model. The measurements were made using the on-wafer load-pull setup. The transistor is biased in class-AB mode which results in $G_t = 20\ dB$, $PAE = 50\ \%$ as shown in Fig.5-45. The benchmarked model is then used to study the effect of access-regions and fringing-capacitances on the large signal device performance. In class-AB mode, a self-aligned device would result in 40% higher PAE due to increased P_{out} in compression, while removing fringing-capacitances would cause a significant increase in G_t by 50%. A self-aligned device with no parasitics would accrue both benefits.

In this chapter, the analysis of the impact of device-level technology parameters on the various performance metrics that are relevant to HV- and/or RF-applications is made possible by the physical-nature of the MVSG model that results in model parameters which are related to device geometry or device process-technology. Key

insights can be drawn using the model about performance bottlenecks in the device architecture or process parameters that can be changed suitably to improve device performance. Thus the MVSG model can serve as a valuable technology design tool that can aid in the improvement of GaN device technology as demonstrated in this chapter. In the next chapter, detailed validation of the model against circuit-level measurements and the study of device-circuit interactions is discussed.

Chapter 7

Circuit Design and Validation

The final focus area of this thesis work is benchmarking the MVSG model with circuit-level measurements comprising both RF- and HV-application regimes. This is a logical final step in linking the physics of carrier transport in the device to its terminal behavior and ultimately to the circuit-level performance. The full validation flow is necessary in order to benchmark any new compact model, particularly one developed for an emerging technology such as GaN-HEMTs. This process enables observation of the circuit performance metrics to evaluate both the new technology and the compact model. As described earlier in the thesis, the prime objective of compact models is to aid circuit design and the circuit-level characterization illustrated in this chapter serves as an evaluation for the usefulness of the MVSG model.

Since GaN-HEMTs are used in both HV-switching applications and RF-transceiver applications, circuits spanning both application domains are considered, with the MVSG model either used in the design of such circuits or validated against circuit-level measurements. Qualification of the model is done in this chapter, both in terms of its accuracy to estimate circuit-level behavior and its robustness in terms of convergence characteristics in involved-circuit simulations, is done in this chapter. The added advantage of the MVSG model is its physical nature which is beneficial for studying interesting device-circuit interactions and is demonstrated for both HV- and RF-circuits. First part of the chapter deals with model-validation against HV-converters and studying the impact of the device nuances on slew-rates at the circuit-level. The

second part of the chapter describes a variety of RF-circuits both designed using the MVSG model and benchmarked against circuit-level measurements along with studying the impact of device non-idealities on circuit performance.

7.1 HV-regime: HV-GaN DC-DC converters

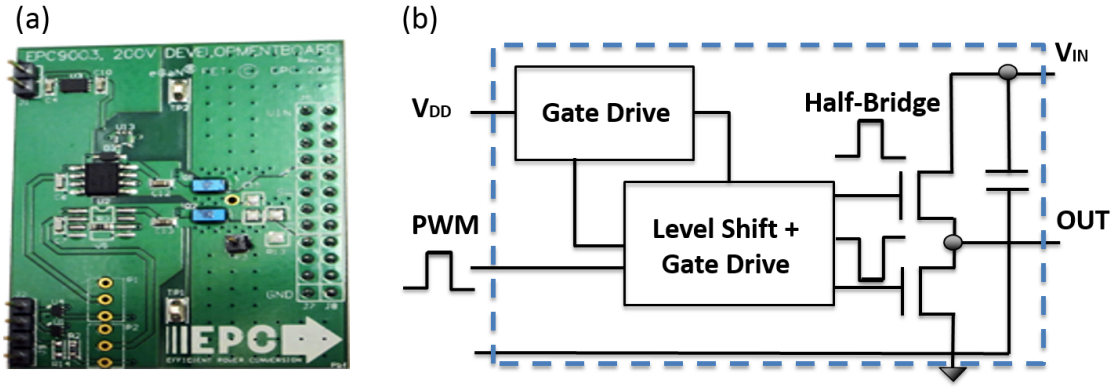


Figure 7-1: (a) Circuit-level validation of the MVSG model is carried out using a commercial 170 $V/5$ V hard-switched buck-converter evaluation board (EPC9003) which employs two E-mode GaN-HEMTs (EPC2010) in half-bridge configuration. (b) The equivalent circuit diagram is shown with the two GaN-HEMTs used in the half-bridge along with the gate-drive circuitry.

GaN-HEMTs are poised to become incorporated into the HV-power conversion market in the voltage range of $200 - 400$ V that target automotive drives, solid state lighting, motor control, power supply applications among others. The key circuit at the heart of most of these applications is the AC-DC or DC-DC converters that employ HV-GaN-HEMTs as switches. Therefore studying the switching performance of GaN-HEMTs and the MVSG model's capability to accurately capture the device switching transients are important to both understand this emergent-device behavior in practical switching scenario and the MVSG model's usability in this application regime.

The HV-switching circuit validation is done using a commercial evaluation board from EPC (EPC9003) [69] shown in Fig.7-1. The board is a 170 $V/5$ V hard-switched buck-converter that employs two commercial E-mode GaN-HEMTs (EPC2010) employed in half-bridge configuration. The circuit is capable of operating at frequency of 10 KHz with ports available to apply the pulse-width-modulation (PWM) waveform

to the gate-drive circuitry as shown, and terminals available on the board to measure voltages at various nodes (such as the switch-node (V_{SN}: the output-node of the board that is connected to the load). Sense resistors are present at the gate-terminal of each FET to measure the gate-voltage waveforms and the board can be connected to the desired output load resistances through an inductance. The input-gate voltages, as well as the output-V_{SN} are measured using a high-bandwidth oscilloscope and are compared against circuit simulations that employ the MVSG model for the HV-GaN-HEMTs.

7.2 Circuit simulation vs. measurements

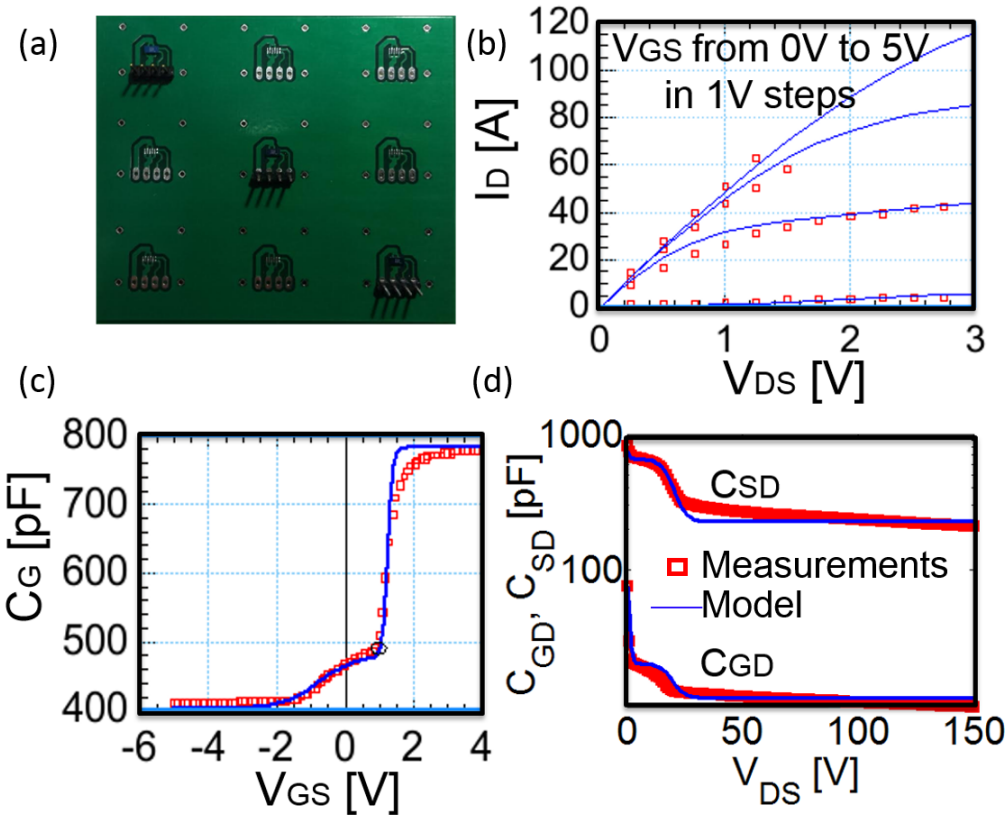


Figure 7-2: (a) The commercial EPC2010 devices used in the half-bridge converter is soldered on the PCB board to extract device-level characteristics. (b) The MVSG model parameters are extracted from IV-measurements made on these devices. (c)-(d) The comparison with measured device-level capacitances (C_{iss} and C_{oss}, C_{rss}) show that the model can capture the EPC2010-device characteristics and the calibrated model can be used for circuit simulations.

The first step in the circuit-level benchmarking against the HV-board is to calibrate the MVSG model against the EPC2010 devices that are commercially available. The devices can be soldered onto a custom-built printed circuit board (PCB) shown in Fig.7-2(a). The IV-characteristics are calibrated as shown in Fig.7-2(b) and since the device has 4 terminals (G, S, D, B), the capacitance between each terminal-pair is measured using a B1505 CMU with C_{iss} vs. V_G and C_{oss}, C_{rss} vs. V_D in the off-state benchmarked as shown in Fig.7-2(c)-(d). The EPC2010 devices are E-mode devices with $V_T = 1\ V$ and the MVSG model is extracted against the measurements that are demonstrated to capture terminal-current characteristics accurately as can be seen. It is clear that the device has a gate-field plate (GFP) with $V_T = -2\ V$ and a source-field plate (SFP) with $V_T = -25\ V$ from the transitions in the CV-measurements as described in chapters 3 and 4 and the MVSG model using the sub-circuit approach that employs GFP- and SFP-transistor elements with the distributed charges that can capture the non-linear capacitance behavior accurately.

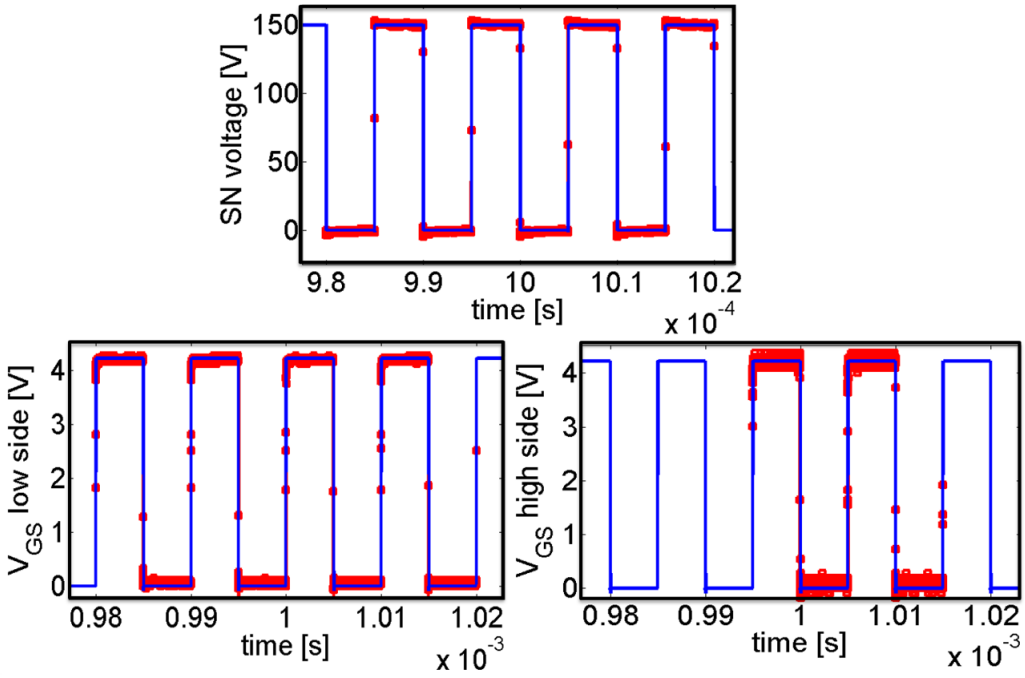


Figure 7-3: The switch node voltage (V_{SN}) at the output, along with the high-side (HS) and low-side (LS) V_{GS} waveforms from measurements with $D = 50\%$ duty cycle at 10 KHz and $V_{IN} = 150\ V$ agree well with the simulated results, demonstrating the accuracy of the MVSG model in HV-circuit simulations.

The calibrated model is used in the half-bridge circuit simulation in Cadence^{TM}, which can accurately capture the output switch-node (SN) waveforms along with the high-side (HS) and low-side (LS) gate-input waveforms as shown in Fig.7-3. The duty cycle is 50% at 20 KHz switching frequency under 150 V input voltage. The gate-drive circuitry is responsible for complementary gate-switching waveforms and the buffers in the path of the gate-drive of the LS-FET introduce delay in gate-voltage waveform of the LS-FET as shown in the datasheet [69]. The physical nature of the MVSG model can then be used to study the impact of device behavior on the calibrated switching waveforms.

7.3 Analysis of slew rates in converters

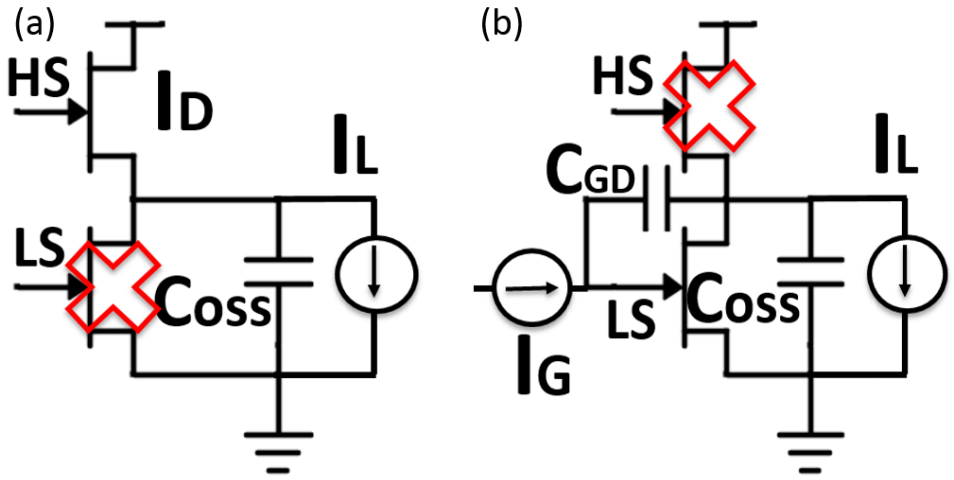


Figure 7-4: (a) Equivalent circuit-state of the half-bridge during low-to-high switching transition in which the LS-FET is off and HS-FET is completely on. The slew-rate (SR_{L-H}) is therefore determined by the net current charging the output-capacitance (C_{oss}). (b) The equivalent circuit-state in the high-to-low switching transition in which the HS-FET is off while the LS-FET is turning-on during switching causes the SR_{H-L} to depend on both C_{gd} and C_{oss}.

The slopes of the V_{SN} during transition are called slew-rates ($SR = \frac{dV_{SN}}{dt}$) and can be studied by looking at the state of the half-bridge circuit as shown in Fig.7-4. In Fig.7-4(a), the state of the circuit is shown during low-to-high transition of the SN wherein the high-side FET (HS-FET) is completely turned-on due to the $HS - V_{GS}$

while the low-side FET (LS-FET) is completely turned-off due to the $LS - V_{GS}$. The low-to-high SR (SR_{L-H}) is therefore determined by the rate at which the output-SN capacitance is charged by the net-current ($I_D - I_L$) flowing into the node which is given by:

$$SR_{L-H} = \frac{I_D - I_L}{2C_{oss} + C_{SN,board}} \tag{7.1}$$

where the output SN-capacitance is the sum of C_{oss} of the two-FETs and the board capacitance at SN ($C_{SN,board}$). In Fig.7-4(b), the state of the circuit is shown during high-to-low transition of the SN wherein the high-side FET (HS-FET) is completely turned-off due to the $HS - V_{GS}$. The low-side FET (LS-FET) is turned-on during the switching transition due to the design of the gate-driver circuitry whose LS-path delay ensures that the $LS - V_{GS}$ is pulled-up to the on-state, in a synchronous fashion with the high-to-low transition of V_{SN}. The high-to-low SR (SR_{H-L}) is therefore determined by the rate at which the output SN-capacitance is discharged via net-current ($I_D + I_L$) flowing out of the switch-node and the discharge through C_{gd} resulting in finite gate-current I_G as shown in the Fig.7-4(b) and SR_{H-L} is given by:

$$SR_{H-L} = (\frac{2C_{oss} + C_{SN,board}}{I_D + I_L} + \frac{C_{gd}}{I_G})^{-1} \tag{7.2}$$

In the EPC9003-board, the total current $I_D + I_L$ discharging C_{oss} of the SN is much higher than the I_G which means that the SR_{H-L} is primarily determined by the C_{gd} of the LS-FET given by:

$$SR_{H-L} \approx \frac{I_G}{C_{gd}} \tag{7.3}$$

The SRs that are related to the device- and circuit-level parameters as described above are measured by using high-bandwidth oscilloscope and special probes that cut down probe-inductances and hence oscillations resulting out of them as described in [69]. The SRs are slopes of the SN-voltage transition waveforms that are magnified plots of Fig.7-3 at the voltage transitions. These are compared against the SRs estimated by simulations with the low-to-high transition studied in Fig.7-5(b). Since the LS-FET is off during this transition, the extension of depletion region in the device extends throughout the device from source to drain as shown in the schematic of Fig.7-5(a)

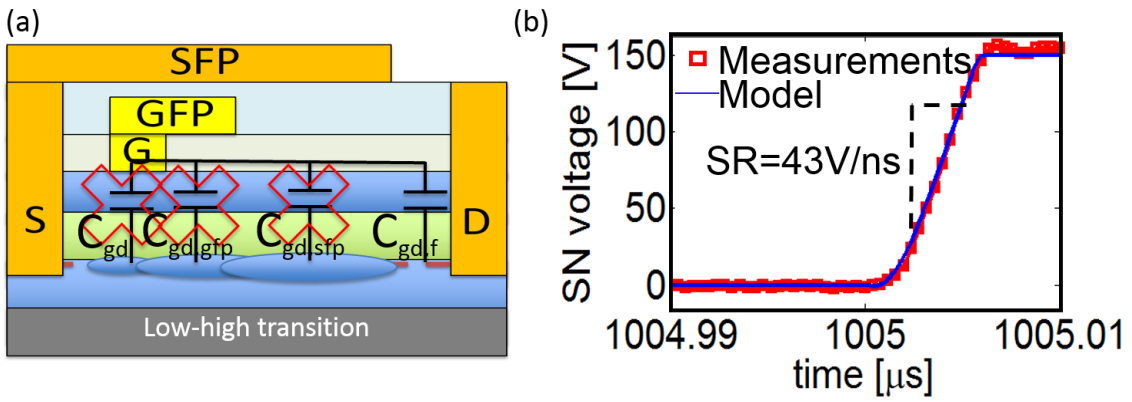


Figure 7-5: (a) The cross-section schematic of the HV-GaN-HEMT showing the contribution from various device capacitances to the off-state C_{gd}. During L-H transition, LS-FET is off and the total C_{gd} is dominated by the off-state fringing capacitance between the gate-drain contact-metals. (b) The measured SN-waveform during L-H transition is compared against measurement and gives a good agreement with $SR_{LH} = 43\ V/ns$.

with the distribution of device-capacitances also depicted in the figure. The device capacitances are primarily due to the parasitic fringing capacitances in the off-state as observed from the static-CV measurements of Fig.7-2. The C_{gd} is dominated by gate-to-drain metal capacitances as shown in the cross-section schematic of Fig.7-5(a). The measured SR_{L-H} matches well with the simulated waveforms as seen from Fig.7-5(a) with $SR_{L-H} = 43\ V/s$ and is consistent with the measured inductor-current and the off-state capacitances at the SN.

The high-to-low SR which is primarily determined by the C_{gd} and I_G for this board can be matched accurately in simulations if these two metrics can be estimated. The gate-drive circuitry determines the I_G and its accuracy is usually guaranteed but compact models can estimate SR_{H-L} only if the device-C_{gd} can be correctly captured during switching. The modeling approach adopted by conventional empirical models discussed in chapter 2 to capture C_{gd} is compared with the distributed modeling approach followed by the MVSG model in Fig.7-6. Typical empirical models lump device-capacitances including C_{gd} as non-linear functions of external gate- and drain-bias as shown in Fig.7-6(a). In the MVSG modeling approach, the device is modeled as a sub-circuit of series-connected transistors, with each transistor-capacitance connected to internal-nodes and functions of internal-voltages as opposed to external-

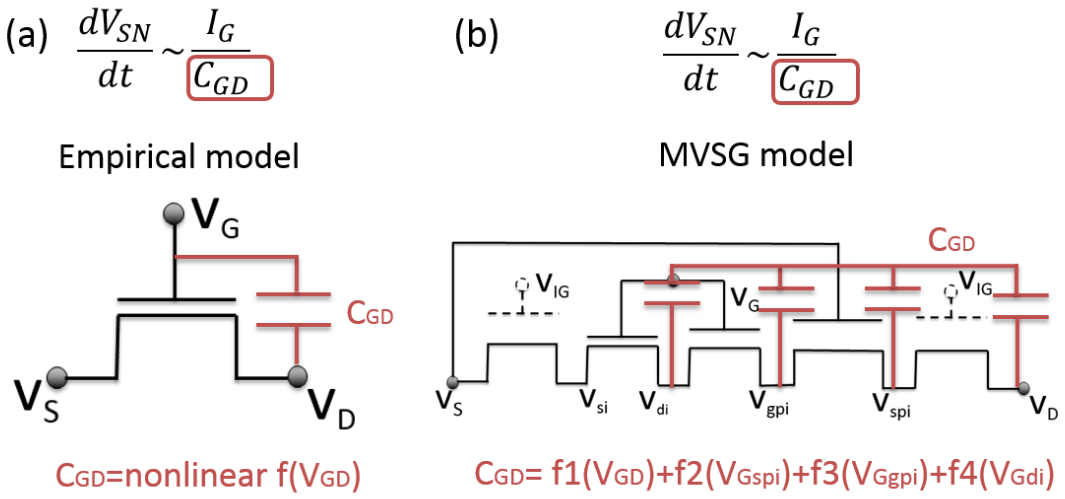


Figure 7-6: (a) Typical modeling approach followed by empirical models to capture the C_{gd} of the device where the capacitance is defined as a non-linear function of the external gate- and drain-voltages (V_G and V_D). The C_{gd} calculated this way plays a role in determining the SR_{H-L}. (b) The distributed modeling approach to capture channel-charges in the MVSG model in which the charges in each transistor element including FP-regions are captured as shown. The total C_{gd} is determined by several capacitance terms of the transistor-elements that depend on internal-node voltages. The C_{GD} during switching can be different from the off-state C_{GD} of the device since the internal-node voltages can be different from the external V_D during slewing,.

voltages as shown in Fig.7-6(b). The C_{gd} in the MVSG model therefore changes in response to changes in internal node-voltages even if the external voltages are unchanged and this property is critical to capture SR_{H-L} as discussed next.

During high-to-low transition of the SN-voltage, the LS-FET turns-on as $LS-V_{GS}$ is switched-on by the gate-driver circuitry making it a hard-switched converter while the V_{DS} still remains at high value. Hence during switching, there is on-state current flow in the device with more than hundred volts of V_{DS} across it causing active power dissipation during slewing making it a hard-switched converter. The distribution of depletion regions in the device are as depicted in the cross-section schematic of Fig.7-7(a) where the depletion region does not span the full source-to-drain distance. The non uniform voltage distribution is the result of the turn-on of intrinsic and GFP-transistors and biased in the linear-regime with low voltage-drops across their respective internal drain-to-source voltages (V_{DiSi}, V_{GFPiDi}). The applied high-V_{DS} is sustained almost completely by the SFP- and drain access-transistors.

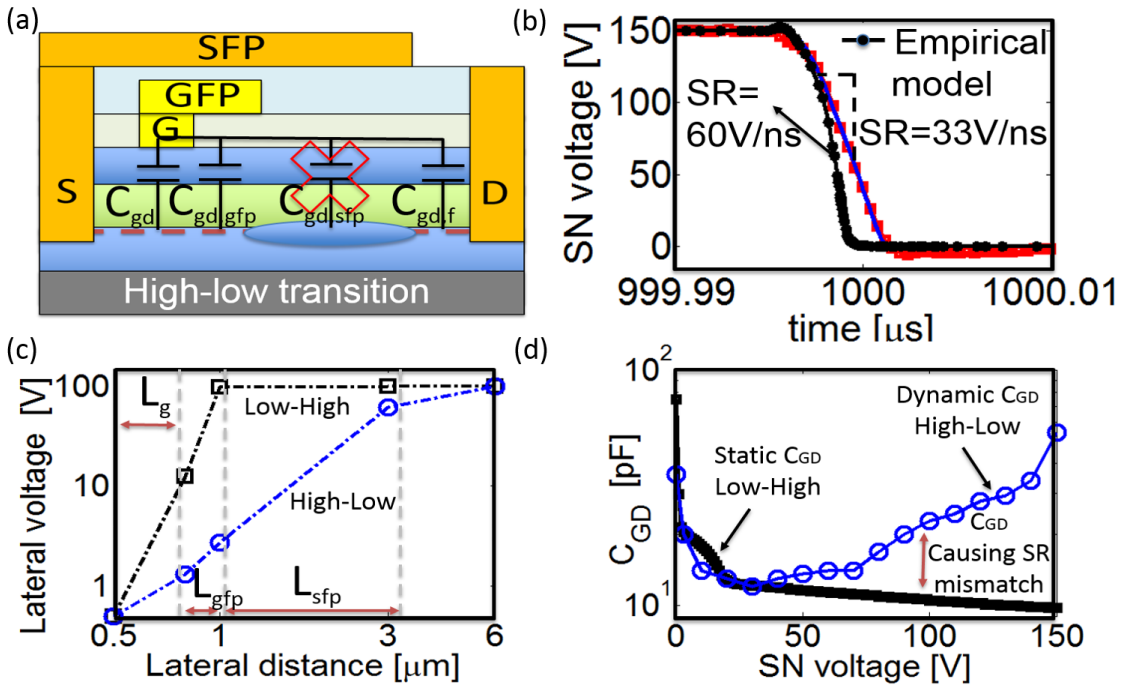


Figure 7-7: (a) Cross-section schematic of GaN-HEMT during SN-voltage transition from high-to-low state. Since the device turns-on with $V_{GS} > V_T$ during switching with V_D still at the high value, there is significant voltage redistribution in the channel compared to the off-state. The depletion region is 'pushed-out' to the SFP- and drain access-regions with the intrinsic-and GFP-transistors biased in the linear regime. (b) The SR_{H-L} of SN-voltage is compared against simulation results from both the empirical model and the MVSG model. The MVSG model accurately captures the measured $SR_{H-L} = 33\ V/ns$ while the empirical model predicts a much faster SR of 60 V/ns since it underestimates the C_{gd} of the device during switching (it predicts that C_{gd} is the off-state C_{gd} value of static-CV measurements). (c) The voltage redistribution in the device along the channel is compared against the voltage profile in off-state, where the voltage drop in the intrinsic- and GFP-regions decrease, pushing these transistors into the linear-regime while the SFP-voltage drop increases and the SFP-transistor blocks most of the V_{DS}. (d) The $C_{gd} = \frac{\delta Q_g}{\delta V_{DS}}$ during switching is higher than the off-state static C_{gd} and the higher 'dynamic-C_{gd}' is responsible for the reduced SR_{H-L} which is correctly captured by the MVSG model.

The measured SR of $SR_{H-L} = 33\ V/ns$ is compared against simulations that use both empirical and the MVSG models as shown in Fig.7-7(b). The SR_{H-L} estimated by the empirical model is twice the measured value while the MVSG-model simulations estimate the SRs accurately as shown. The reason for the difference in SR between the two models is the difference in estimated C_{gd} from the two models. Since

empirical models determine C_{gd} from external voltages as shown in Fig.7-6(a) and $V_{DS} \approx 100\ V$, they estimate C_{gd} as the off-state capacitance obtained from static-CV measurements which are low in value ($= 1\ pF$ per FET) and hence yield incorrect high-SR_{H-L}. The MVSG model on the other hand, models C_{gd} in a distributed manner as shown in Fig.7-6(b) with the voltage distribution during switching as shown in Fig.7-7(c) compared against the off-state. It is clear that the intrinsic- and GFP-transistors sustain low-voltages which yield high capacitances corresponding to linear-region on-state contributions from these transistor elements to the total C_{gd}. The dynamic-C_{gd} due to this non-quasi-static voltage redistribution in the device during switching is shown in Fig.7-7(d) which is higher than the static-CV measurements as shown in the figure. The high-C_{gd} is the cause for the observed SR_{H-L} from the measurements which can be modeled by the physical MVSG model.

The validation of the MVSG model simulations against HV-circuit measurements described in this section confirms that the model is capable of accurately capturing the device behavior in HV-application domain and can be used as a tool for HV-circuit design. The physical nature of the model, together with the distributed approach to capture carrier-transport and charge in different regions of the device enables the model to serve as an investigative tool to understand the key device-circuit interactions under large voltage switching in converters. The next section of this chapter deals with the circuit-level validation pertinent to RF-applications.

7.4 RF-application regime: RF-front end circuits

The second key area of insertion of the emergent GaN technology is in RF-applications ranging from cellular-communication systems, radars, SatComs etc. The ability of GaN-HEMTs to deliver high power densities at medium- to high-frequency ranges is due to the high device-I_{on} and g_m along with low C_g. These are the reasons for record P_{out} at high f_T and f_{max} which make GaN-technology an attractive alternative to conventional LDMOS for RF-transmitter power amplifiers. The absence of junctions and good RF-noise properties of the device also qualify its use at the receiver stage

LNA and VCO-design. A full transceiver system can therefore be built using GaN-technology and the MVSG model is demonstrated as a design-tool to build such RF-systems in this section.

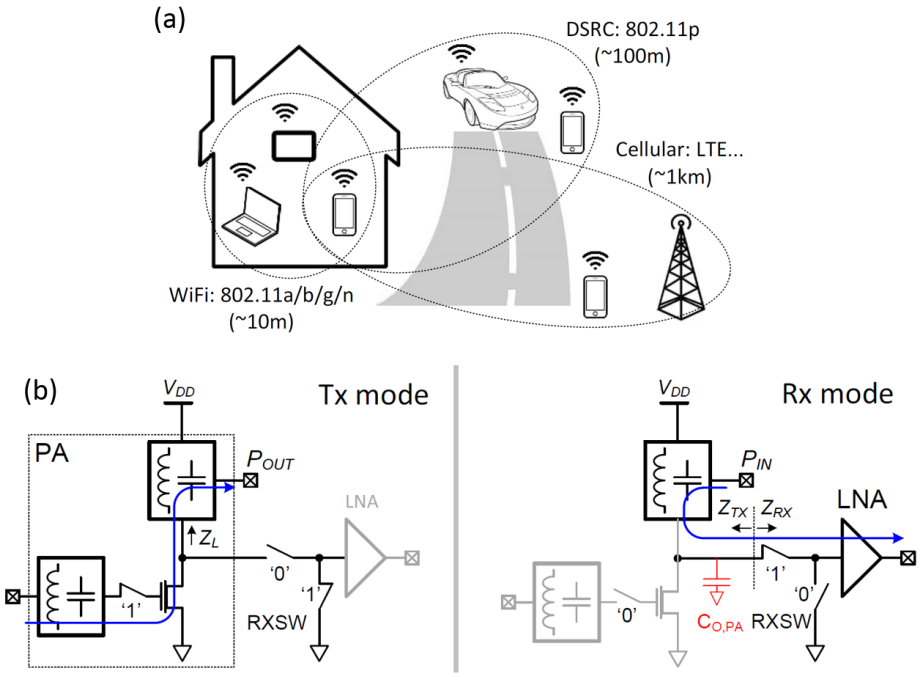


Figure 7-8: Comparison of the ranges of dedicated short range communication (DSRC), WiFi, and Cellular networks [70]. Courtesy: Dr. Pilsoon Choi, MIT.

The rapid growth of direct device-to-device (D2D) communication in recent times as opposed to a more centralized base-station based cellular networks is primarily to improve responsiveness and in-situ computation among a variety of devices. The emerging "dedicated short range communication" (DSRC) based on IEEE 802.11p [70], was originally targeted for car safety and congestion control, but it is actually a form of D2D communication with long range and fast response time compared to the current protocols such as WiFi Direct that cannot effectively handle the demands of range and reliability. As described in [70], Fig.7-8(a) illustrates D2D systems such as WiFi, DSRC, and Cellular networks with different coverage-ranges. To be suitable for highly mobile networks that change topologies very rapidly, the design-specifications of the IEEE 802.11p standard require maximum allowed output power (P_{out}) of 28.8 dBm at 5.9 GHz frequency band. However, CMOS-circuits cannot achieve such high P_{out} at 5.9 GHz while maintaining linearity or good error-vector-

magnitude (EVM) and thus suitable ground for the use of GaN-HEMTs in the implementation of this protocol emerges, since they outperform CMOS devices for PAs in terms of output power and efficiency.

The fully integrated RF front-end system architecture implementing the protocol is shown in Fig.7-8(b) wherein an explicit antenna-switch is employed in both the transmitter (Tx) and receiver (Rx) branches in order to switch between the two modes. The architecture proposed in [70] employs series-switches (at the input of both transmitter-PA and receiver-LNA) and shunt-switches (at the input of receiver-LNA) to toggle between the two modes with GaN-HEMTs of high power handling capability, small on-resistance, and high isolation characteristics used for building the switches. The receiver-LNA is built using GaN-HEMTs both for ease of integration and because of the good-noise-figure and linearity characteristics of GaN-HEMTs.

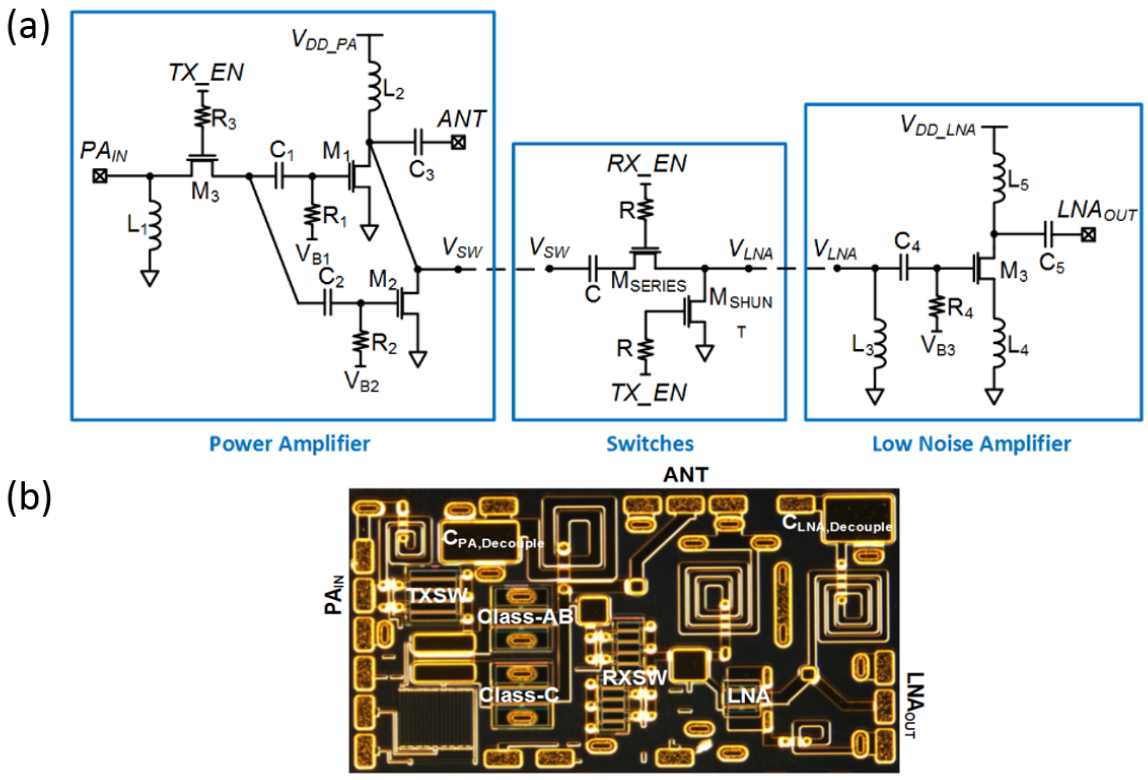


Figure 7-9: (a) The circuit schematic for a high-efficiency high-power RF front-end design that employs dual-biased GaN-HEMTs for Tx-PA and a GaN-HEMT for Rx-LNA, integrated with GaN-HEMT switches. (b) The die-micrograph image of the circuit fabricated using the Wolfspeed 0.25 μm GaN-on-SiC process. Circuit design courtesy: Dr. Pilsoon Choi, MIT.

Fig.7-9(a) illustrates the entire RF-front-end circuit schematic including PA, antenna switch, and LNA, which are integrated on a single die as shown in the die-micrograph of Fig.7-9(b) using the commercial Wolfspeed process-technology. All the circuits of the figure are designed with the MVSG model which is calibrated against device-level measurements, described in chapter 5.

The transmitter-PA compliant with the IEEE 802.11p standard should accommodate orthogonal frequency-division-multiplexing (OFDM) modulation, which should satisfy the linearity requirement to accommodate the high peak-to-average power ratio (PAPR) of complex modulated signals, as well as high efficiency. Considering additional constraints of high level of integration and minimization of the die area, a Class-C GaN HEMT device with its input and output combined in phase with a Class-AB GaN-HEMT device is adopted for higher linearity with enhanced efficiency. The optimal source- and load-impedances are found through large-signal load-pull simulation for the dual-biased GaN-HEMT devices, with up to third frequency harmonics. The input- and output-isolation switches are included as part of the impedance matching network with the on-resistance of the PA-input switch in the Tx-mode acting as a series stabilization resistance. The final load- and source-impedances at 5.9 GHz along with the values of input and output L-C matching networks used in the design are tabulated in [70]. These passive component values are adjusted after rigorous post-layout electromagnetic (EM) simulations in Momentum^{TM} module in ADS with the MVSG model used for the dual-GaN-HEMTs.

The series-shunt switches on the receiver-side, that are placed in the Rx-path protect the LNA from the high-power PA in the Tx-mode while providing low insertion-loss in the Rx-mode, and are part of the input matching network of the LNA to optimize its NF. In the Tx-mode, the LNA-input is grounded through the shunt-switch, as shown in Fig.7-9(b) while the series-switch is directly connected to the drain of the PA, and the switch-states are toggled in the Rx-mode to connect the antenna-port to the input of the LNA. An inductively degenerated topology is chosen for independent control of real and imaginary parts of the input impedance as well as for obtaining good NF from the LNA. The GaN-HEMT used in the LNA is biased close to class-AB

mode which is modeled using the MVSG model for the LNA-design. The component values of the circuit parameters are tabulated in [70] and are not repeated here. 12 V supply is used for the LNA while the PA is designed with more than 28 V as per the specifications of the IEEE802.11p protocol for vehicular communications. The results of the Tx and Rx simulations such as small- and large-signal simulation on the Tx-stage and small/large-signal along with 3rd-order inter-modulation performance of the Rx-stage with the MVSG model are shown and compared with measurement data in the next section.

7.5 Circuit-simulation vs. measurements

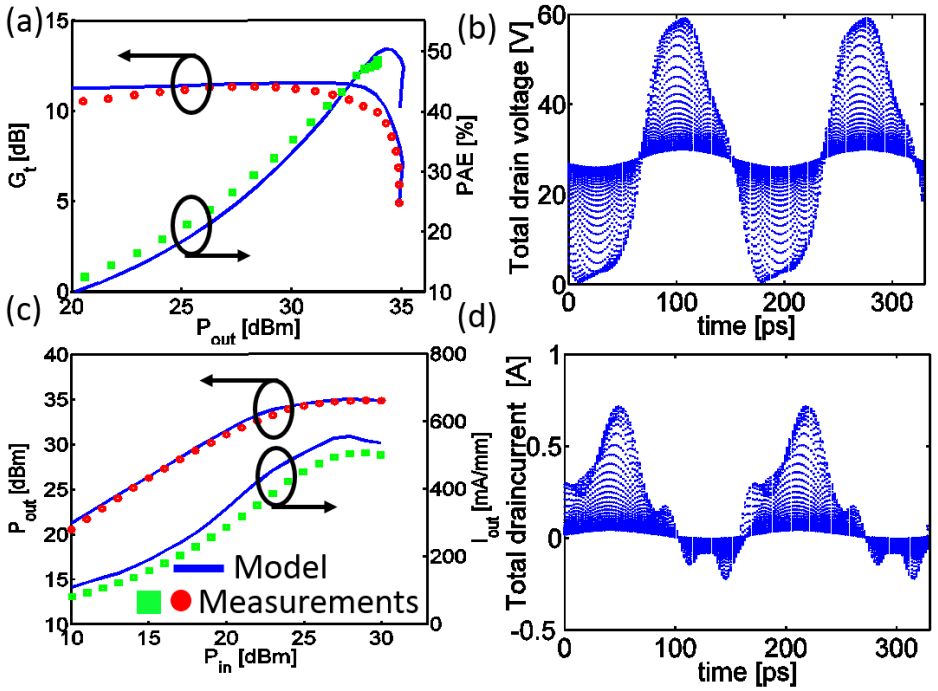


Figure 7-10: The Tx PA-circuit power-sweep measurements with the optimized class AB/C bias conditions with $V_{DS} = 28\ V$ at 5.9 GHz are compared against the model. The Tx configuration achieves $P_{sat} = 34\ dBm$ with 40% PAE. The model matches these values along with a correct prediction of $PAE = 30\%$ and $G_t = 10\ dB$ at back-off output-power of 28 dBm as required in the IEEE 802.11p standard. The corresponding time-domain drain voltage and current waveforms obtained by the MVSG model show that the current is maximum when the voltage is minimum and vice versa, confirming the high-efficiency class-AB/C operation [52].

The MVSG model is calibrated against measurements of modeling structures that include FETs with multiple widths spanning the width-range of devices in the circuit and open/short-structures for parasitic de-embedding as explained in chapter 5. The associated parameters are listed in Table. 5.5. The extracted model is used to simulate the active elements of the front-end circuit with the commercial PDK employed to capture the behavior of the passives and switch-elements. Electromagnetic simulations in Momentum^{TM} are co-simulated with the MVSG-model and the parasitics are extracted from the layout to get accurate results. On the Tx-side, the results of large-signal HB-simulations (up to 3rd harmonics) of the PA are compared against measurements as shown in Fig.7-10, wherein the P_{out}, G_t, PAE and I_{out} vs. P_{in} along with the time-domain-waveforms of the output current- and voltage-waveforms of the PA are given. From the figure it is clear that the model is capable of accurately estimating the device-behavior in Tx-circuits and that it exhibits convergence robustness in involved non-linear circuit-simulations. The Tx-P_{out} at the saturated-region is about 35 dBm which is greater than the required 28.8 dBm and hence the PA can be operated in back-off mode to preserve linearity. The Tx also complies with the general WLAN spectral mask, achieving an average efficiency of 30% at 28.8 dBm-P_{out} with the orthogonal current-voltage waveforms shown in fig.7-10 confirming the class-AB/C operation responsible for the high-PAE due to low P_{DC}.

In the Rx-mode, good agreement is achieved with measured S11/S12, 3rd-order inter-modulation (IM3), and NF (3.7 dB at 5.9 GHz including switches) as shown in Fig.7-11. S11 shows high-gain of 10 dB at 5.9 GHz and low-S12 of -25 dB at this frequency due to the optimization of the input-impedance. The Rx-nonlinearity is tested against simulations and the large-signal two-tone response with 5.5 mA currents at 12 V supply is depicted in Fig.7-11(c), showing $OIP3$ of 22.0 dBm. As shown in Fig.7-11(d), 3.7 dB-NF at 5.9 GHz is also predicted by the simulation with the MVSG model. The NF measured with a calibrated noise-source is found to be $3.7-4.0$ dB in band, which is reasonable considering 2.0 dB-NF_{min} of the GaN-HEMT as discussed in chapter 5. Accurate prediction of NF spanning the frequency-range is an indication of the accuracy of the RF-noise formulation in the MVSG model.

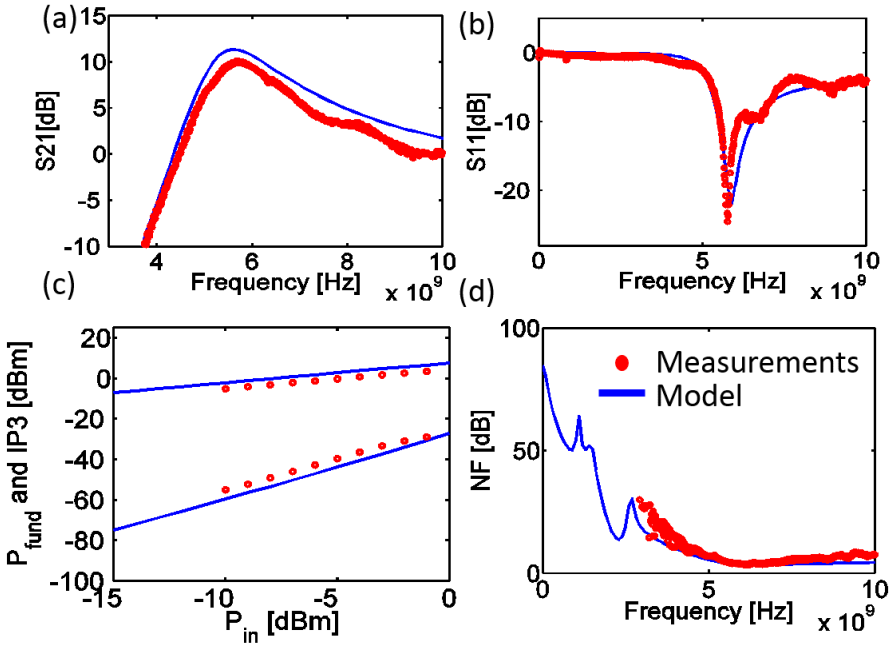


Figure 7-11: The small-signal response of the Rx-LNA is compared against the MVSG model. The small-signal gain, S21, is about 10 dB and S11 is less than -20 dB at 5.9 GHz, which meets the design requirements, with the model accurately predicting the S-parameters. The non-linearity of LNA is tested with a two-tone signals (5.865 GHz + 5.885 GHz) and the resulting fundamental and third-order inter-modulation signals are correctly predicted by the model. The resulting OIP3 is around 22 dBm. The NF-measurements with calibrated noise-source match the model-simulation-results closely with $NF = 3.7$ dB at 5.9 GHz.

The analysis and model-validation done against the RF-front-end circuit described in this section demonstrates the usability of the MVSG model in practical RF-transceiver system design. The involved large-signal multi-harmonic circuit simulations along with the noise simulations impose stringent convergence requirements in addition to accuracy that the MVSG model satisfies. The model is used in the design and benchmarking against the VCO used in typical RF-transceiver systems along with the phase-noise characterization, in the next section.

7.6 RF-application: Voltage-controlled oscillators

The RF-transceiver architecture described in chapter 5 shows that VCOs are an important component in the system that is employed in both the Tx- and Rx-stages

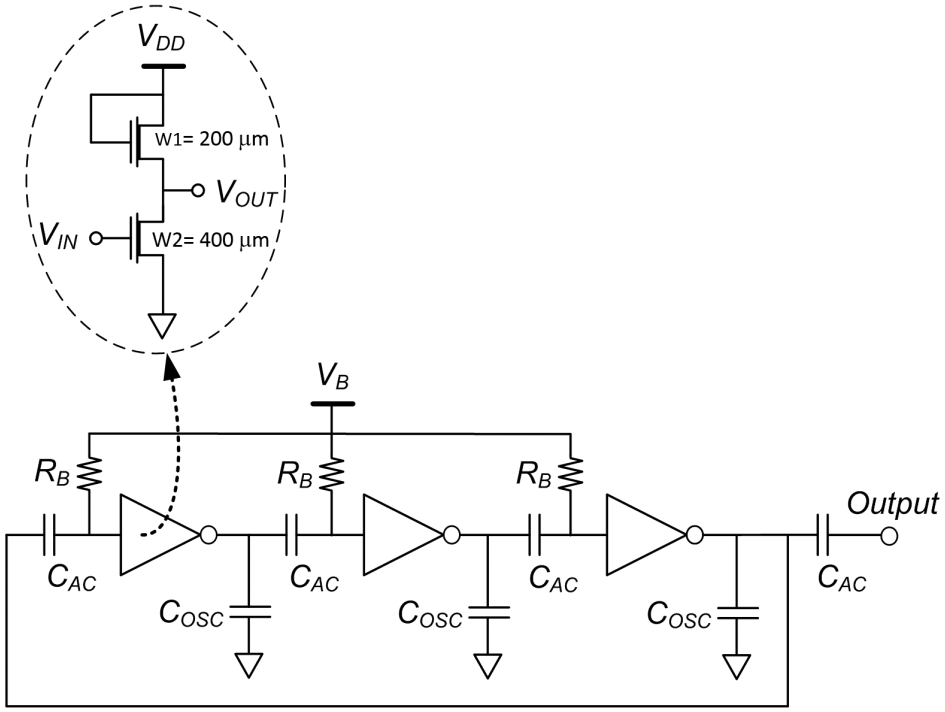


Figure 7-12: The circuit-schematic of a three-stage ring-oscillator showing the details of each inverter-stage. The absence of P-HEMTs forces a pseudo-inverter topology and the negative-V_T requires AC-coupling capacitors C_{AC} to apply to the gate-voltage (V_B) at the input of each inverter-stage to shift the voltage-transfer-curves.

to generate the HF-carrier that is mixed with the base-band data signal. The voltage control of oscillations is usually achieved by employing tuned-varactors in an LC-based oscillator that is the circuit of choice due to the controllability of oscillation-frequency and simplicity of circuit-architecture. However in this section, a three-stage ring-oscillator (RO) is chosen since it does not require large on-chip inductors and imposes the greatest modeling-challenge due to the large-signal oscillation characteristics of the RO. The voltage dependence of oscillation-frequency is achieved by tuning the voltage supply that requires the model to accurately capture the large-signal device characteristics along with the bias-dependence of device-level reactive elements. An additional use of the RO is to study the low-frequency phase-noise characteristics in GaN-HEMT technology and the ability of the phase-noise formulation in the MVSG model, as described in chapter 4, to estimate it accurately.

The circuit-topology adopted in the design of the three-stage RO fabricated using the Wolfspeed process technology is shown in Fig.7-12. The process allows N-channel

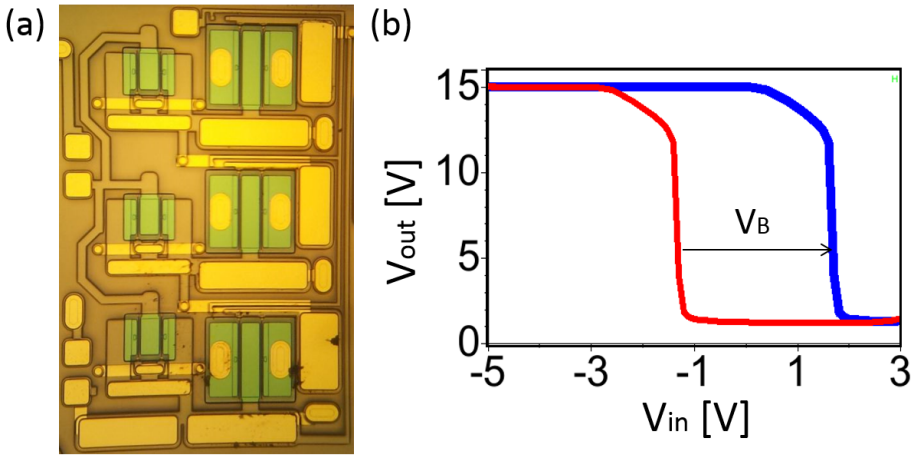


Figure 7-13: (a) Die-micrograph image of the fabricated RO that uses the Wolfspeed process-technology is shown [71]. (b) The voltage transfer characteristic (VTC) shows a transition at negative input-voltage (V_{in}) (red) due to the negative-V_T of depletion-mode GaN-HEMTs. To shift the transition to a positive V_{in} (blue), a negative gate-bias (V_B) through R_B and AC-coupled capacitor (C_{AC}) is required.

D-mode GaN-HEMTs with the V_T of $-2.8\ V$ as can be seen from the device-level characteristics in chapter 5. The absence of P-channel devices does not allow for complementary inverter-design and pseudo-inverters with diode-connected active load is used for the inverter-stage design as shown in Fig.7-12. The widths of these devices are chosen to minimize the static power loss and maximize signal-swing from V_{DD}-to-ground. Another concern is that the negative V_T of GaN-HEMTs yields voltage-transfer-characteristics with negative transition voltage as shown in Fig.7-13(b). This makes it impossible to cascade the inverter-stages to form the RO and necessitates shifting the input-voltage of each stage by V_B through AC-coupling capacitors as shown in Fig.7-12. The resulting VTC is shifted to the regular-characteristic with positive-transition-voltage as also shown in Fig.7-13(b).

The die-micrograph of the fabricated RO is shown in the Fig.7-13 and the circuit-performance is probed using on-wafer probe-station to apply the V_{DD} and V_B voltages through B1505A and the output-waveforms of oscillations are measured using a HF-digital oscilloscope or spectrum analyzer. The RO enables the evaluation of the MVSG model's ability to estimate the large-signal oscillation-waveforms and the oscillation-frequency along with its change with V_{DD}. An additional purpose is the

characterization of phase-noise performance of the device and circuit by observing the behavior of the low-frequency skirts in the output-power spectrum. The MVSG model is used in simulations to estimate the power spectrum levels together with the slope of the transition of the spectrum from the peak-power point to the noise-floor. The slope of the low-frequency skirts is known to be dependent on the charge-trapping effects responsible for device flicker-noise [72]. The low-frequency flicker-noise of the device is up-converted to the oscillation-frequency which makes it easy to calibrate against the MVSG model. These circuit-level measurements are compared against model-simulations in the next section.

7.7 Circuit simulation vs. measurements

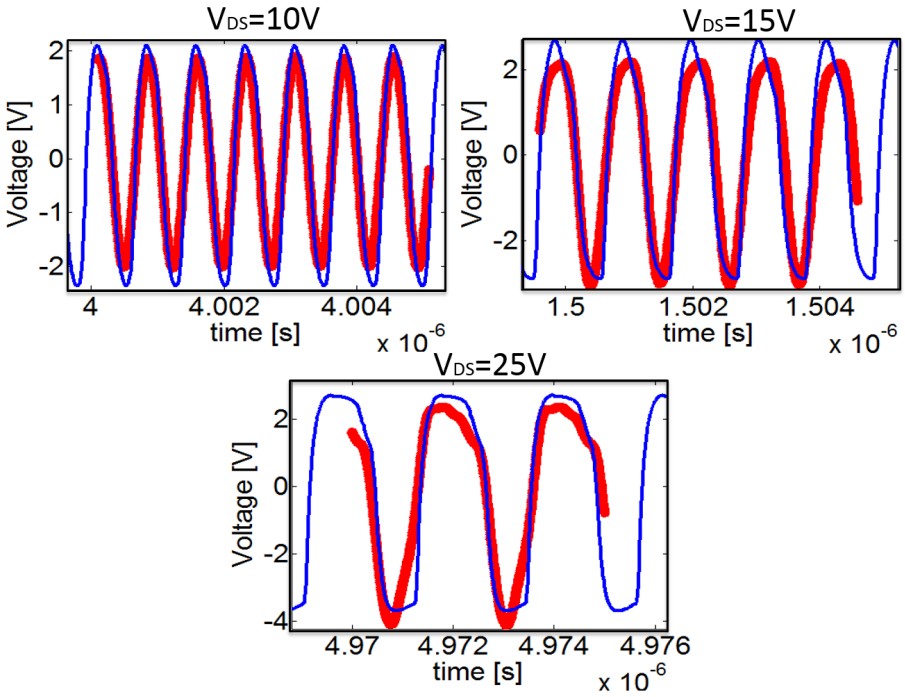


Figure 7-14: The time-domain waveforms of the output-voltage of the RO at different supply voltages are shown. The model captures the non-linear large-signal waveforms of the circuit along with changes in the voltage-level and frequency of oscillation with supply voltages (V_{DD}) from 10 V to 25 V.

The time-domain waveforms of the RO-output are shown in Fig.7-14 with different supply voltages V_{DD}. The shape- and frequency-change of the output-waveforms with

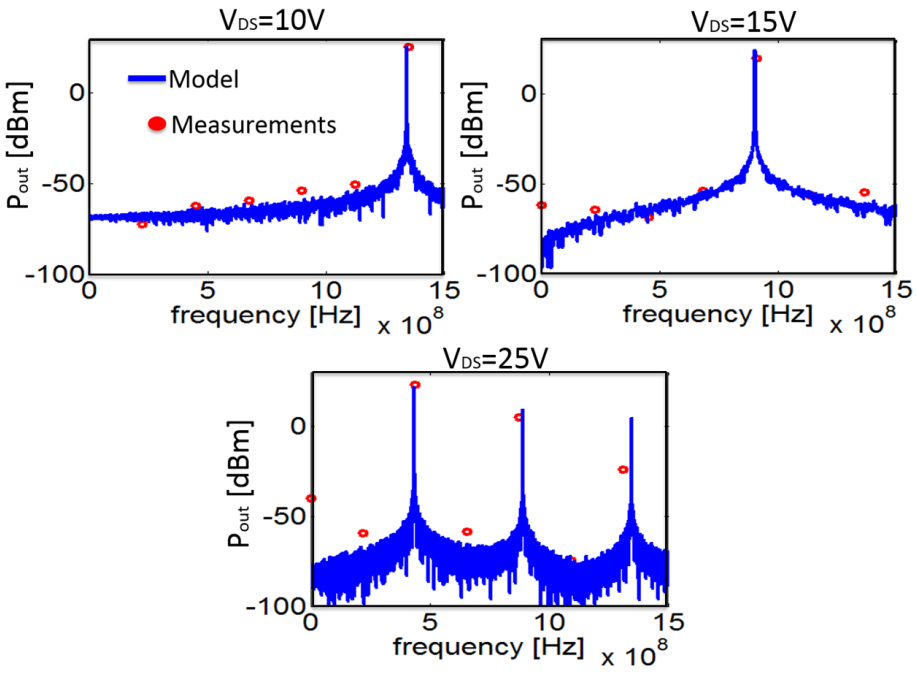


Figure 7-15: The output-power spectrum plots of the RO show that the f_{fund} of oscillation drifts to a lower frequency as V_{DD} increases, which is captured by the model. The RO generates around 20 dBm RF-output power at fundamental frequency in the range of $0.4 \approx 1.4$ GHz (L-band), highlighting the ability of GaN-HEMTs to deliver high-power densities at high frequencies. Accurate description of the power-spectrum by the MVSG model is the starting point for benchmarking the phase-noise model.

V_{DD} is captured reasonably well by the circuit-level transient simulations in ADS using the MVSG model for the HEMTs. Harmonic Balance, HB-simulations of the circuit using the MVSG model are compared against the output-power levels shown in Fig.7-15 at different supply voltages. The shift of the fundamental frequency (f_{fund}) from 1.3 GHz at $V_{DD} = 10$ V to 0.4 GHz at $V_{DD} = 25$ V with the output-power levels at 22 dBm is correctly captured by the MVSG model. The reduction in f_{fund} with V_{DD} is expected because the device-capacitances increase as the V_{DD} is reduced, pushing the device closer to linear-regime. The MVSG model is able to model the change in f_{fund} because it captures well the bias-dependent capacitances using the charge-formulation discussed in chapter 4.

The final set of circuit measurements that follow after the accurate estimation of switching-waveforms, is the characterization of the MVSG model's phase-noise formulation. The model is adopted from the Leeson-model [27] as given in chapter 4 with

the model parameters listed in Table 5.6. The measured phase-noise characteristics at the output of the RO using a signal-analyzer are compared against noise-activated HB-simulations of the circuit and are given Fig.7-16. The slope and noise spectral-levels at different V_{DD} are matched well with the circuit simulations using the MVSG phase-noise model. It is evident that the phase-noise characteristics show a single slope (close to $1/f^3$), and not the $1/f^2$ noise tail due to the high noise-floor, which is consistent with other studies on noise in GaN-technology [27].

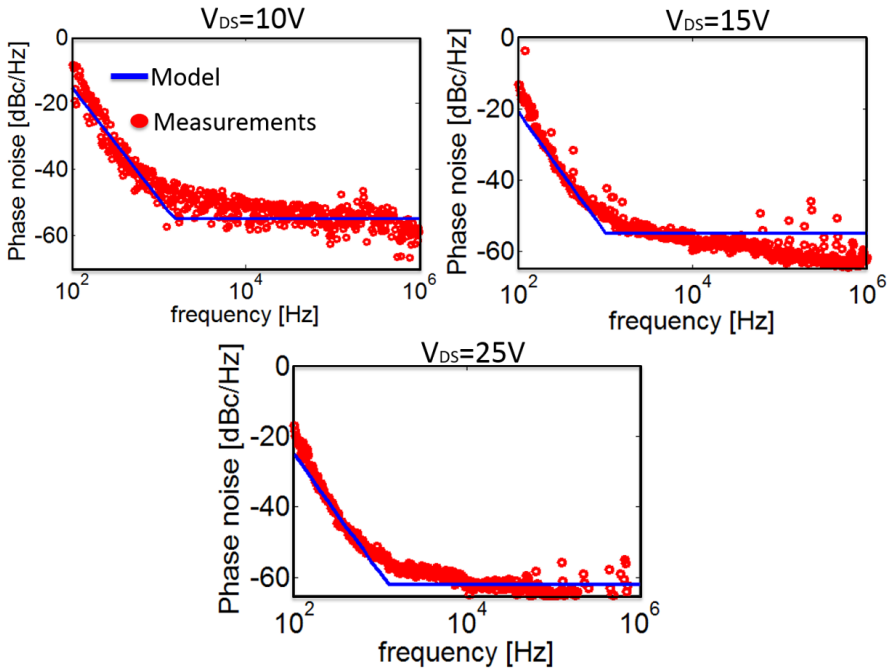


Figure 7-16: The low-frequency phase-noise spectrum measured using a signal-analyzer is compared against the Agilent-ADS simulation using the MVSG model for supply voltages from 10 V to 25 V. The up-converted white-noise regime ($1/f^2$) is absent as reported in other works on phase noise in GaN-MMICs [27]. The flicker-noise model described in chapter 4 is able to capture the phase-noise ($1/f^3$) spectral-levels and the corner-frequencies accurately along with the shift of these metrics with V_{DD}. The shift is mainly due to changes in I_D in the model-formulation and the impulse-sensitivity-function (ISF) (which in turn depends on output voltage waveforms of Fig.7-14).

From the seminal work by Hajimiri et.al on the phase-noise of oscillators particularly in ROs, impulse-sensitivity-function (ISF: $\Gamma(t)$) is defined as a metric to quantify the frequency-domain phase-noise or time-domain jitter in oscillators [72]. Since the oscillation waveforms in ROs are amplitude limited, only noise related to

phase-fluctuations are dominant in ROs and the total phase-noise computed using the periodic ISF as a response to the superposition of impulse noise-currents given in [72] as

$$L(f) = \frac{\Gamma_{rms}^2}{8\pi^2 f^2} \frac{i_n^2/\Delta f}{q_{max}^2} \tag{7.4}$$

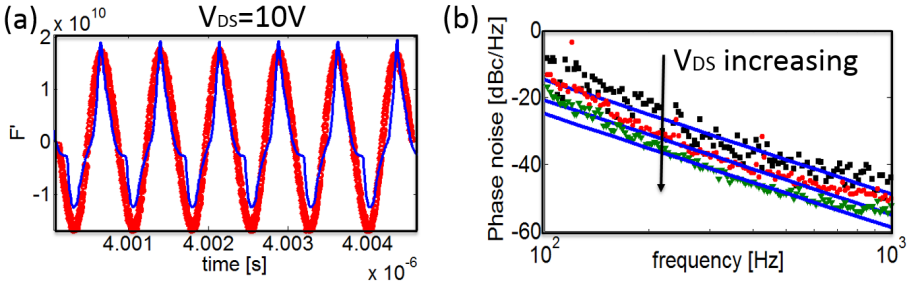
where Γ_{rms} is the rms-value of the ISF and $\frac{i_n^2/\Delta f}{q_{max}^2}$ is the single side-band noise power spectral density of injected noise-source. The key take-away from the above equation is that the phase-noise power-spectrum density of the unconverted-$1/f^3$-noise is proportional to Γ_{rms}. Furthermore, the corner-frequency f_{1/f^3} in ROs between $1/f^3$ and $1/f^2$ are related as given in [72] by:

$$f_{1/f^3} = f_{1/f} \frac{\Gamma_{DC}^2}{\Gamma_{rms}^2} \tag{7.5}$$

where Γ_{DC}^2 is the DC-value of the ISF. Hence the corner-frequency in the GaN-HEMT ROs in which we just observe the $1/f^3$-region, and the noise power spectral-density level are both proportional to Γ_{DC}^2. Hajimiri et al., calculate the ISF of ROs in terms of the transition-slopes of the time-domain output switching waveforms of the RO in [72] as:

$$\Gamma_{DC} = \frac{2\pi}{\eta^2 N^2} \frac{1-A}{1+A} \qquad A = \frac{f'_{rise}}{f'_{fall}} \tag{7.6}$$

where N is the number of stages, and f'_{rise} and f'_{fall} are slopes of the time-domain output-waveforms of the RO. Thus, by computing the A from the time-domain-waveforms we can verify the relationship between the phase-noise and Γ_{DC}^2 for different V_{DD}. It is observed that the reduction of noise spectral-level with the V_{DD}-increase seen in Fig.7-16 and Fig.7-17(b), can be explained by the reduction of the DC-component of ISF, Γ_{DC}^2, at the output-node. The derivative of output waveform (f') is shown for $V_{DD} = 10\ V$ in Fig.7-17 which matches with the model simulations. The DC-component of ISF can be calculated from the derivative values of the output-waveforms of Fig.7-14 at both rising- and falling-edges as given above and are tabulated in the figure. The plot of Γ_{DC}^2 vs. the noise-spectral value at 500 MHz-offset from f_{fund} shows a linear-relationship consistent with the phase-noise-theory



V_{DS} [V]	F'rise 10^{10}	F'fall 10^{10}	A= F'rise/ F'fall	Γ_{DC} (1-A)/(1+A) 10^{10}	1/f noise at 500Hz
8	1.7	2.1	0.84	8.9	-40
15	1.8	1.6	1.10	4.9	-43.7
25	1.6	1.7	0.98	0.9	-46.9

Figure 7-17: In accordance with the analysis of phase-noise by Hajimiri et.al. in [73], the $(1/f^3)$ phase-noise is found to be proportional to the DC-component of ISF (Γ^2_{DC}). (a) The ISF which depends on the derivative of the output-node waveforms (i.e. the rising- and falling-edge slopes) as shown, varies with V_{DD} and can be captured by the model. (b) The $1/f^3$ noise-levels decreases with V_{DD} as from (c) the table and it can be seen that the Γ^2_{DC} calculated from the ISF also decreases with V_{DD}. (d) The linear relationship between $1/f^3$ noise-level at 500 Hz offset-frequency and Γ^2_{DC} can be verified from the model. This is possible because the MVSG model is able to capture large-signal switching behavior in the RO and hence the ISF (and Γ^2_{DC}) as a function of V_{DD}.

in [72]. Since the MVSG model can accurately estimate the large-signal switching characteristics along with the bias-dependence of phase-noise (via I_D), the model can be used as a tool to test the established phase-noise theory, as was carried out in this section. In the next section, model-validation against an RF-converter is illustrated along with the analysis of the impact of charge-trapping effects on circuit performance.

7.8 RF-application regime: RF-step-up converters

The GaN-based RF front-end circuit presented earlier in this chapter to deliver high output-power for vehicular-communications can be integrated with the CMOS back-end signal-processing circuitry for the full system design. In addition to the challenges

associated with the heterogeneous integration of these two material-systems at the wafer-level, another concern is that the required supply voltage for the operation of GaN-circuits (28 V to 37 V) is much higher than the voltage available from a car battery (typically 12 V). Therefore an associated DC boost-converter is still needed to supply GaN-devices with high voltage. The converters for this purpose can be built on the GaN-platform alongside the front-end described earlier to achieve small form-factor. The design-validation of this converter using the MVSG model for the GaN-HEMT switches used in the circuit is described in this section.

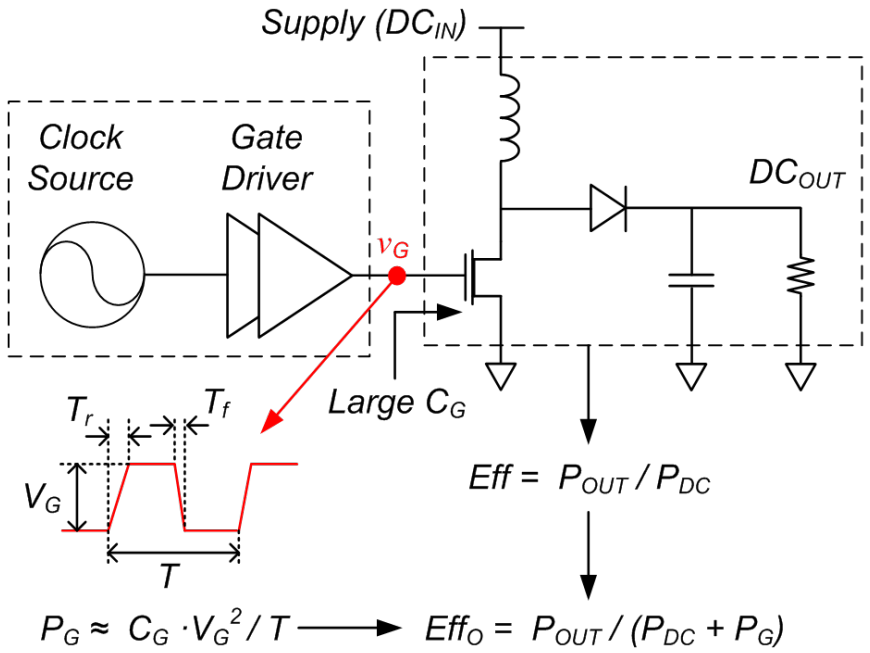


Figure 7-18: Conventional inductor-based DC boost-converter showing the gate-driver circuitry which shows the impact of gate-drivers on the overall efficiency of the converter.

Conventional DC-converters such as the one shown in Fig.7-18 inherently require a clock source and additional power consuming gate-drivers, which decrease the overall efficiency (E_{ffO}) of the converter. The switching-frequency has to be increased in order to scale down the size of the inductor since the converter must be fabricated on-chip for compact design. Higher frequency in turn results in greater switching-losses associated with the gate-driver circuit (P_G) for a given C_G that is determined by C_{iss} of the GaN-HEMT. The boost-converter topology adopted in [74] tries to eliminate the gate-driver by integrating an oscillator with the converter instead of

the gate-driver.

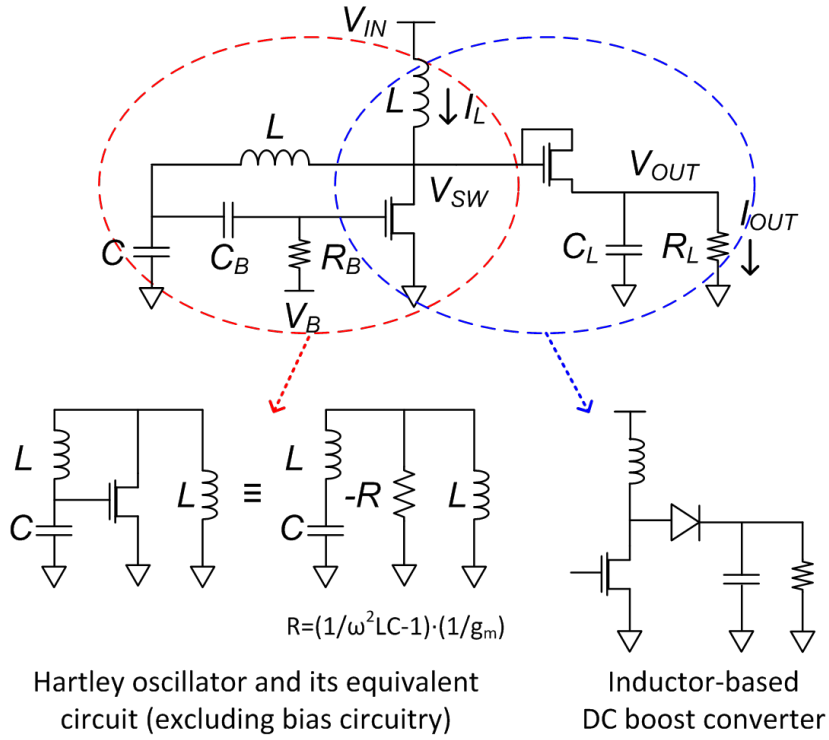


Figure 7-19: Inductor-based DC boost-converter merged with Hartley-oscillator to eliminate gate-driver circuitry and external clock-signals. Diode-connected FET is used at the output of the converter due to the unavailability of diode in the process. Circuit-design courtesy: Pilsoon Choi, MIT.

In the Fig.7-19, the integrated step-up converter that uses a Hartley-LC-oscillator instead of the gate-driver to the switching-FET is shown. The GaN-HEMT that acts as the gain-element of the oscillator also acts the switching-FET of the converter as shown in the figure and for this design a 14×500 μm-GaN-FET is chosen as the switching and oscillating-device. The LC-elements are chosen to minimize the circuit-area with the bias-inductance also forming part of the tank-circuit and the LC-combination yields oscillation-frequency of 680 MHz. The diode at the output in the converter is unavailable in the Wolfspeed-process and a diode-connected FET is used in its place as shown.

The circuit is fabricated using commercial Wolfspeed process technology and the die-micrograph is shown in Fig.7-20. The chip occupies an area of 3 $mm \times 3$ mm with GSG-pads provided for on-wafer-probing of the circuit in order to apply the input-supply voltage (V_{IN}) and gate-bias (V_B). The output-boosted voltage (V_{OUT})

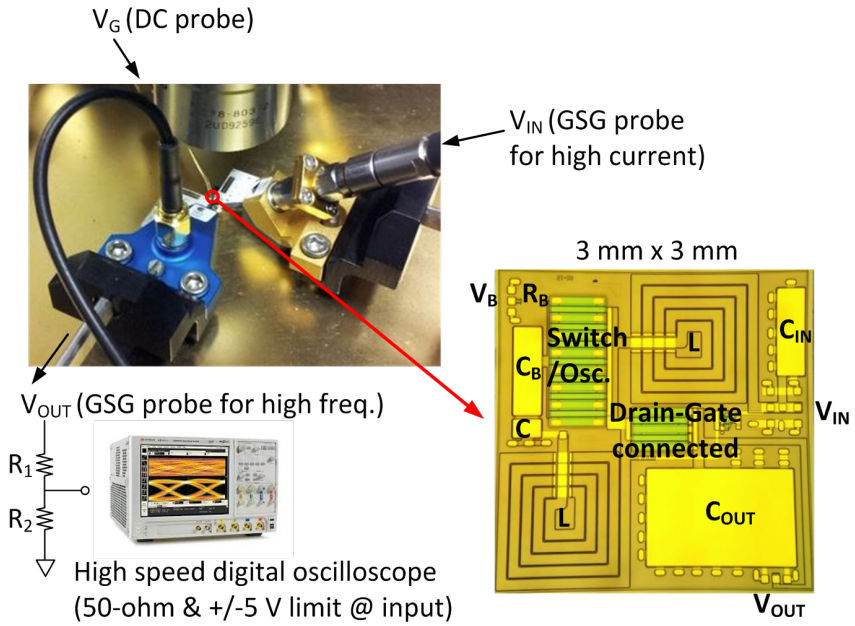


Figure 7-20: The chip-micrograph and the on-wafer measurement configurations are shown where the V_{IN}, V_B are applied through GSG-probes while the output V_{OUT} is extracted using a GSG-probe and connected through a resistive-divider (since the oscilloscope has 5 V-limit) to the 50 Ω port of the high-speed oscilloscope.

is measured using a GSG-probe that is connected to 50 Ω-port of the high-speed oscilloscope as shown. The boosted output voltage along with the ripple are measured and compared against the MVSG model simulations described next.

7.9 Impact of current-collapse on the boost-ratio

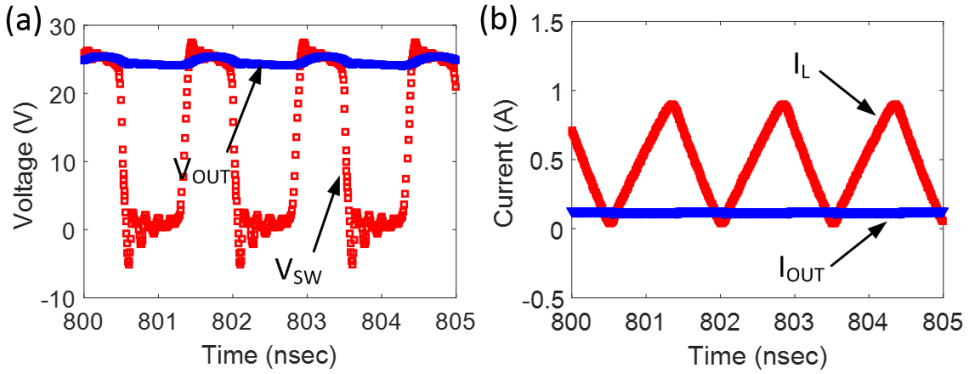


Figure 7-21: Simulated waveforms of the RF-DC boost-converter using an ideal-diode: (a) voltage waveforms before (V_{SW}) and after filtering (V_{OUT}) are shown where V_{SW} switched between $0-28\,V$ and $V_{OUT} = 24\,V$, (b) Inductor current shows the triangular waveform along with I_{OUT} dependent on the load resistance.

The simulated voltage- and current-waveforms with $200-\Omega$ load at 12 V supply

(car battery) using an ideal diode are shown in Fig.7-21, assuming a scenario where a high-current diode is available in the process. The GaN-device is self-switching without an external clock, with the figure showing V_{SW} switching between 0 V and 24 V along with the currents through the inductor and load. The simulated overall output voltage is 24 V with 120 mA load-current. The simulated output voltage with the drain-gate connected FET-configuration simulated using the calibrated MVSG model, instead of an ideal-diode causes a further reduced voltage output, due to the non-zero reverse currents of the drain-gate connected GaN-HEMT in the converter.

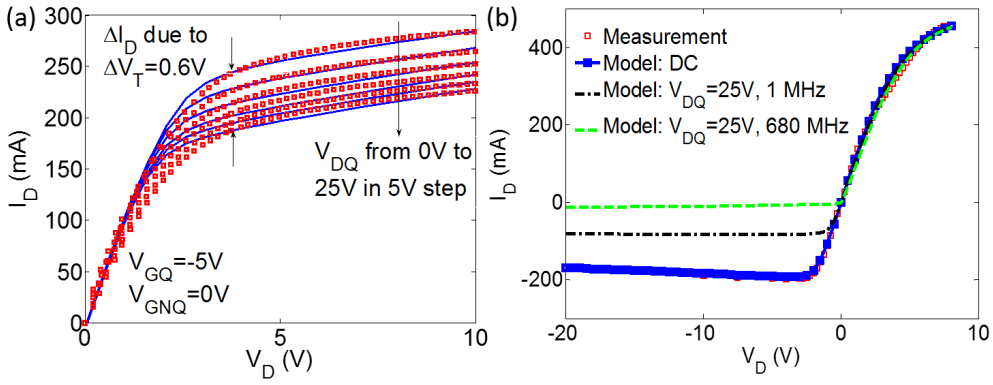


Figure 7-22: (a) Pulsed I-V characteristics of the 3-terminal GaN-HEMT compared against the MVSG model showing the current-collapse effect due to V_T shifts. (b) The DC- and simulated pulsed I-V characteristics of the 2-terminal gate-drain diode-connected GaN HEMTs shows that the current-collapse effect that causes the V_T shift is actually beneficial to the converter. The reverse-current is reduced due to the dynamic increase of V_T at the switching-frequency causing reduced discharge of output-capacitance. The behavior of the diode-connected FET with current-collapse is closer to that of an ideal-diode thus preserving the boost-ratio.

Realizing a diode functioning properly at 680 MHz is an obstacle to implement the GaN boost-converter since a high-current diode is not provided in the GaN-process used for this design. A simple drain-gate connected configuration of a 4×500 μm GaN-FET is used instead. In Fig.7-22(a), the pulsed forward-mode I-V measurement of a three-terminal GaN-HEMT from off-state quiescent-gate-voltage ($V_{GQ} = -5\ V < V_T$) with different quiescent-drain voltage stress (V_{DQ} changed from 0 V to 25 V in steps of 5 V) to the on-state non-quiescent gate-voltage ($V_{GNQ} = 0\ V$) at 1 MHz switching-frequency is shown. The figure reveals significant current-collapse effect with 20% saturation current reduction at $V_{DQ} = 25\ V$ which is a typical stress-voltage across

the diode in the converter. This effect is captured in the MVSG model by making the threshold-voltage (V_T) a function of V_{DQ} (V_T shift, $\Delta V_T = 0.6\ V$ for $V_{DQ} = 25\ V$) using the second approach to capture this effect as described in chapter 4. The impact of the current-collapse effect on the forward- and reverse-mode diode-connected FET characteristics is then studied using the model. The V_T shifted for pulsed I-V simulations is used to simulate the diode-connected FET I-V curves under switching conditions as shown in Fig.7-22(b) along with DC benchmarking against measurement. In both forward- and reverse-modes, the DC I-V does not resemble the ideal-diode characteristic. While the forward-mode current is sufficient to charge the output-capacitor of the converter during the 'charging' cycle (i.e. the switching FET is off), the non-zero reverse-current would discharge the output-capacitor during the 'preserving' cycle (i.e. the switching FET is on). However, as shown in Fig.7-22(b) the V_T-shift during switching reduces the reverse-current more significantly than the current in the forward-mode at 1 MHz. Since charge de-trapping becomes less efficient causing increased collapse at higher switching-frequencies, the drain-gate connected GaN-FET operating at 680 MHz exhibits significant collapse while switching and behaves closer to an ideal-diode. The very low-reverse current as seen from Fig.7-22(b) (dashed-curve) due to charge-trapping avoids the issue of the output-capacitor getting discharged when the switching-FET is on. Nevertheless, the converter has a degraded boosting-ratio and efficiency because the reverse-current is not exactly zero, as discussed in the next section. This investigation gives an understanding of the well-known current collapse-effect in GaN-devices on circuit-level performance.

7.10 Circuit simulation vs. measurements

The measured output waveforms at 225 Ω external load resistor with 200 pF on-chip output-capacitor are depicted in Fig.7-23. The output-capacitor restricted by the given die-area is not large enough to eliminate the ripple at output and the average DC output-voltage at V_B of $-3.0\ V$ is 20 V. It varies with different gate-biases (V_B) at the switching-device since the actual duty-cycle of the switching waveforms

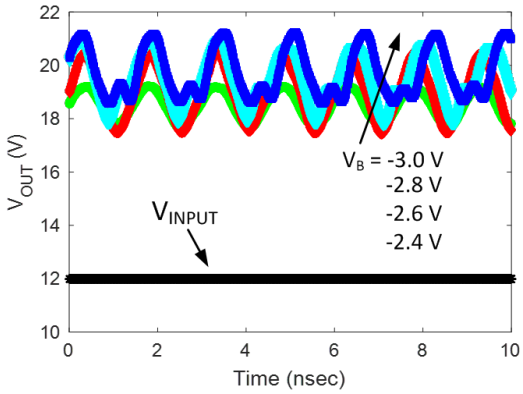


Figure 7-23: Measured output waveforms with different bias conditions.

slightly changes with V_B along with the corresponding magnitude of the waveforms. Fig.7-24 shows the measured output voltages with different load conditions and input voltages, where the simulation with the calibrated MVSG model including the current-collapse effect in the diode-connected FET shows a good match with the measurement data. The boost-ratio is about 1.66 and the overall efficiency is about 34% including the power consumption of the switching circuity and the converter itself. Fig.7-24(a) demonstrates that the non-ideal diode-characteristic of the gate-drain connected configuration described in the previous section causes a performance degradation of the converter. The issue is not an inherent problem in GaN-technology or the proposed circuit-topology and thus can be resolved if a high-current diode is provided in a GaN-process.

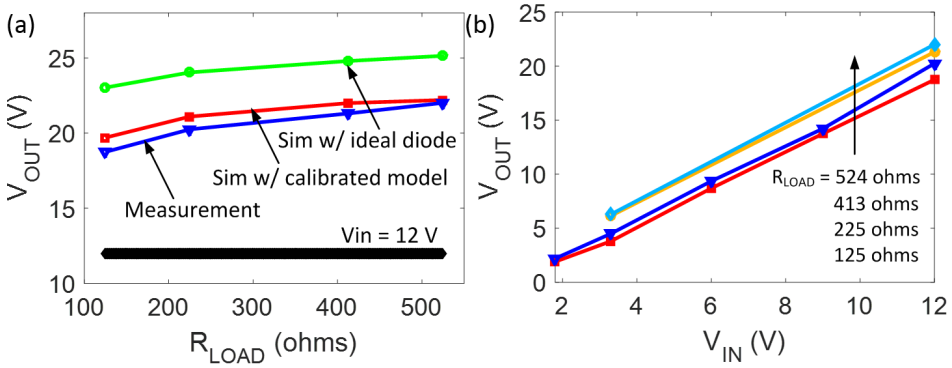


Figure 7-24: Measured output-voltages: (a) vs. load, (b) vs. V_{in} compared against model-simulations showing good-agreement. The boost-ratio is lesser than the upper-limit in the scenario of ideal-diode at the output and changes slightly with V_{IN} due to changing duty-cycle and oscillation-waveform with V_{IN}.

The circuit-level validation of MVSG-model for a wide-range of circuits spanning both HV- and RF-regimes done in this chapter completes the full-chain of compact-model development flow from solving device-physics equations to running dedicated circuit simulations. Through the various device- and circuit-level validation it is possible to claim that the MVSG model developed in this thesis is able to serve the end use of GaN-HEMT based circuit design.

Chapter 8

Conclusions and Future Work

The purpose of developing the MVSG model in this thesis along with the lessons learnt and the trade-offs made during the model development are highlighted in this concluding chapter of the thesis.

MIT-Virtual Source GaNFET (MSVG) model is an extension of the core MVS-model developed for scaled Si-FETs that is extended to a variety of field-effect-transistors built in material systems such as Si-FETs [41], GaAs-HEMTs [75], Graphene-FETs [76], and MOS_2-FETs [77]. The primary purpose of the family of models is to evaluate the potential strengths of the devices built in each technology and to accurately capture the transport and charge behavior of these devices using simple equations with minimum number of parameters that are grounded in physics. The models have served well as evaluation tools for studying carrier-transport and extract injection-velocities in the FETs.

The MVSG model developed in this thesis was originally formulated with a similar purpose and hence retained simplicity along with minimum parameter dependence (about 10) but over the course of this thesis development, the model was extended to meet the requirements of an industry-standard compact model as stipulated by the compact model coalition (CMC). The requirements of CMC were listed in chapter 2 and are evidently more stringent in comparison to the requirement of simplicity met by the above models. An industry standard compact model is required to capture a number of second order effects present in GaN-HEMTs, which results in an increased

set of model equations with larger number of parameters as discussed in the thesis. The goal during this model development has been to remain as close to physics as possible without having to resort to a large number of empirical equations but at the same time to retain accuracies that are sufficient for meaningful circuit design.

8.1 Lessons learnt from compact-model development

This section highlights several lessons learnt during the course of developing the compact model during this doctoral work. Industry collaboration also helped in the incorporation of some of the best model development practices that are prevalent in established semiconductor design houses and are elucidated here.

8.1.1 Verilog-A coding practices

The sub-circuit approach followed in the MVSG model to capture carrier-transport in different regions of the device results in series-connected transistor elements as described in chapter 4.5. Since the core-transistor equations adopted to model currents and charges are identical for all transistor elements, it is useful to write the model formulation for channel- current as a function-block in the Verilog-A code as given in Appendix A. The parameter sets and equations that are different for transistor elements can be passed in the function-call to the model formulation block. The exception is the gate-overdrive formulation (for implicit-gate transistors) and associated parameter set.

The importance of modularity of the code-formulation for different physical effects in the device is another lesson learnt over the course of this work. For example, the module for gate-leakage is only relevant for Schottky-gated RF-devices and separating the equations governing this effect in a separate module is particularly useful since it allows function-calls to this module only in scenarios where gate-leakage is required. This approach makes a single Verilog-A code translatable among different technologies with the function-calls that can be activated by flags in the parameter-set depending on the technology. The MVSG model employs flags such as **igmod**, **noise-**

mod, **trapselect** to activate gate-leakage, noise-model and charge-trapping model as necessary. In addition, the model can capture up to four field-plates (FPs) in which each FP can be of either gate-connected or source-connected type. The type of the FP-connection is determined by flags: **flagfp1**, **flagfp2**, **flagfp3** and **flagfp4** which makes the FP GFP-type if the flag-values are set to 1 or SFP-type if they are set to 0. The implicit-gate transistor formulation for access-regions may be simplified to simple resistive-formulations in scenarios also using a flag; **flagres**. This is useful where convergence is of high priority compared to accuracy, and/or in scenarios where the access-region non-linearities are less relevant. Details of these parameters can be obtained from the model-code in Appendix A.

The convergence robustness of the model code can be improved by using convergence aids within the code. One such tool is to connect high resistance (low value g_{min}) to ground at each internal node of the code using the parameter **rmin**. Similarly the minimum capacitance can be set within the model-code using **cmin** parameter. These are generally set in the simulator to aid circuit convergence in involved simulations but in circuits that have both Si-CMOS and GaN-HEMTs, the currents and capacitances of GaN-HEMTs have widely different values compared to CMOS devices and the required tolerance parameters (including *gmin* and *cmin*) could be different for the two technologies. The internal model definitions allow for setting the convergence tolerances for GaN-HEMTs independently in such scenarios. A second convergence-robust Verilog-A coding practice is to define all model equations based on branch-currents and branch-voltages as is done in the MVSG model given in Appendix A. Detailed modeling techniques can be read from [78] while nuances associated with the determination of model-parameter sets are described next.

8.1.2 Parameter extraction

A model is only as accurate as the parameters it employs and the MVSG model is not an exception. This becomes all the more important in cases of physics-based compact models since the model formulations are heavily weighted towards the accuracy of each of the physical parameter it employs. Therefore it is critical to have full information on

the geometry and technology parameters for accurate model extraction. The MVSG model is made technology-agnostic with respect to the gate-stack information, since it is usually unique to the fabrication technology and hence detailed information is restricted as propriety. However lateral geometry parameters (such as L_g, L_{gs}, L_{gd} and L_{fp} and so on) are critical for the model and must be provided by foundries for model extraction. Typically model (and process) characterization structures are fabricated by foundries to extract μ_0, R_{sh}, R_{cs}, R_{cd} etc. since the values for these parameters are also required for model fits to ensure maximum accuracy. In the absence of such data, parameters can also be used as fitting parameters but the accuracy of the fits are generally compromised and cannot be attributed to the deficiencies of the model.

The extraction procedure of the model parameters is highlighted in Appendix B and requires a combination of technology information, DC-IV, CV- and S-parameter measurements to extract them. The model formulation is such that, important parameters can be extracted from DC-IV measurements spanning linear-to-saturation and off-to-on-state with the knowledge of physical parameters from foundry. Once extracted, these parameters can be fixed during the remaining parameter extraction steps. Furthermore, the model accuracy is contingent on the availability of device-level capacitance information that requires CV-measurement data, especially for devices with FPs. Absence of this data impacts the model accuracy significantly since most of the physical parameters will then have to be used as fitting parameters. Most of the core-parameters can be extracted from IV- and CV-measurement data as explained in Appendix B. The remaining parameters associated with RF-parasitics, noise and charge-trapping require dedicated measurements as explained in chapter 5.

The parameters in the MVSG model are amenable to 'orthogonal' extractions in the sense that a few parameters are dominant in certain bias-regimes and can be extracted independent of other parameters in such regions. The industry-compliant MVSG model also employs certain number of empirical parameters since model accuracy is critical to capture effects such as electron trapping whose physics is not fully understood. In the next section, trade-offs that exist between accuracy vs. convergence robustness are discussed.

8.2 Trade-offs in compact models: Accuracy vs. robustness

The need for convergence robustness of compact models was described in chapter 4 in the context of the need for source/drain symmetry. In order to satisfy these symmetry requirements, compact models cannot use functions that are non-differentiable and hence have to compromise the model-accuracy since accurate formulations often employ functions that are not allowed from a robustness point of view. The MVSG model employs differentiable functions at the cost of some model accuracy, that enables it to pass the symmetry tests in both currents and charges as demonstrated in chapter 5.

Convergence robustness also places restrictions on the number of internal nodes that can be employed in the model and hence accuracy, particularly in the thermal module. It is widely reported that the thermal transients often have more than one dominant time-constant that are to be accounted for, with an equivalent number of nodes for accurate estimation of the effect. The model does not include geometry-dependent self-heating effects associated with multiple fingers since these are heavily layout- and technology-dependent, and thus they change the equivalent circuit-topology substantially. The same argument holds true for capturing trapping effects, which require modeling more than one time-constant (and hence multiple nodes) for both trapping and de-trapping effects. Modeling distributed effects in the channel and gate-line that are relevant at HF-regimes also require multiple internal nodes and are not included in the MVSG model due to convergence constraints. Increased accuracy of the MVSG model at frequencies beyond W-band ($> 110\ GHz$) therefore would require accounting for these distributed effects at the expense of computational robustness.

Finally another physical phenomenon in GaN-HEMTs that directly impacts the accuracy vs. robustness trade-off is the memory-effect associated with the initial condition that the device is subjected to. In addition to standard aging effects, that occur over long term device usage, it is often observed that short term reversible

changes occur on devices depending on waveform pattern as observed during various measurements done over the course of this thesis. It is difficult to estimate the exact initial condition that every device in a circuit operates from, every time the circuit turns-on. Even if it is possible to estimate the initial condition, modeling it requires the use of 'initial condition' statements in Verilog-A simulations that are not allowed. Since the MVSG-model does not include memory effects in the emergent GaN-devices, its manifestations such as V_T drifts and initial-condition dependence on V_T are not captured.

8.3 Further work

8.3.1 Modeling GaN HEMTs

The thesis work aims to tie-down all aspects of modeling of GaN-HEMTs linking technology and circuit-design by capturing most of the physical phenomena in the device that are of significance for circuit-design. However there is scope to include several second-order effects which may not contribute to significant increase of the model accuracy or robustness but are interesting physical problems to tackle. Some such remaining topics of research are listed below:

- Scalability of the model to include full ballistic transport in a seamless fashion with parameters (such as mean-free-paths, ballistic-velocity, apparent-mobility and so on) that are fully-physical.

  The step in this direction is the MVS-2 model-extension to the MVS-model where the channel surface-potential at both source and drain-end are computed to account for the V_T shift with V_G, and to express the linear-to-saturation function F_{sat} in terms of physical parameters (instead of β). This could be the approach to integrate the full ballistic regime in GaN HEMTs to the MVSG model.

- Making the electrostatic parameters such as DIBL, CLM, SS etc. scalable with gate-length without having to fit them from post-measurement data.

While expressing electrostatic parameters in terms of heterostructure, geometry and process parameters does not result in any reduction in parameter-count, the approach does enable computation of several electrostatic effects in a physical manner and captures their scalability. For example, if a full-physical approach is adopted to model the threshold voltage instead of using a single parameter V_{TO}, it results in the use of parameters such as t_{AlGaN}:heterostructure thickness, ΔE_c: conduction band offset, σ_p: polarization charges. The parameter count in this approach is increased without them being easily amenable to extraction, but the V_T would be computed from first principles.

- Physical modeling of thermal-model, cross-coupled charges, and charge-trapping.

  Thermal modeling is critical for realistic circuit simulations and both the R_{th} and C_{th} used in the model vary with geometry and power-dissipation levels and can be computed from device heterostructure and substrate information. The boundary layers that offer significant R_{th} and the heat-spreading problem in GaN-HEMTs described in chapter 3 can be accounted for in the R_{th} formulation either by using bias-dependent thermal network and/or via multiple time constants [24]. The cross-coupled charges in the device that result in CV-transitions at each FP-V_T can be modeled through physical-approach if the effective dielectric-thickness of the fringing fields between adjacent FP-transistors is computed. Charge-trapping effects are heavily technology dependent and the framework developed in this thesis can be extended to a full-physical formulation by expressing the source function $f(V_{GD})$ in terms of the physical mechanism that causes the dynamic-effect. The formulation of $f(V_{GD})$ that is currently adopted resembles the diode-current formulation which gives us some insight into the mechanism responsible for charge-trapping (which could be either thermal or tunneling currents charging trap-states). Further work in this direction involves detailed thermal, switching and spectroscopy techniques to identify the location and energy-levels of traps.

- Inclusion of multiple trapping- and heating-time constants in the models at the

expense of computational robustness and simulation-time.

Extending the point made earlier, the thermal and charge-trapping effects can be modeled more accurately if multiple time-constants (and hence nodes) associated with the phenomena are included. This approach is more useful for specific device-level simulations to study the impact of these dynamic effects on the device-performance.

- Incorporation of variation in device-V_T along the width-direction and the resulting width-dependent variation in terminal characteristics.

  Thermo reflectance thermography measurements indicate non-uniform heat distribution in the device along the gate-width direction which suggests varying power dissipation and therefore current density along the gate width. This may be due to non-uniformity of the gate-line length and/or changes in the device-heterostructure parameters along the width-direction. The resulting variation in V_T along the width-direction causes the device-currents to not scale properly with the width. The V_T variation also causes the 'smearing-out' of the transition from above-threshold and below-threshold regimes and can be captured by modeling the device as a parallel network of several transistors with smaller widths and varying values of V_T.

- HF-dynamic non-quasi-static effects that require distributed channel modeling at the expense of convergence robustness.

  Very high-frequency applications require modeling non-quasi-static effects in the channel within each transistor element used in the MVSG-sub-circuit. The non-quasi-static effects imply that the carrier transport through the gated-region has multiple time-constants (in addition to the dominant time constant captured via f_T) and needs distributed current modeling along the channel-direction. In addition, the linear Ward-Dutton charge partitioning function adopted in the MVSG-model may not be sufficient to capture the charge distribution at high frequencies and higher order partitioning (with super-linear charge partitioning

functions may have to be used). This formalism of course requires additional nodes and impacts the convergence robustness.

- Modeling technology non-idealities such as charges in gate-oxide and passivation-layers that cause V_T shifts.

  The lack of a highly mature GaN-process as contrasted with Si, manifests itself in V_T and mobility variations on account of the non-idealities in the heterostructure. In an industrial setting, the PVT-corner simulations using Monte-Carlo approach to add distributions to the key transport and electrostatic parameters (such as μ, V_T, n_s, C_g and so on) are sufficient to capture all the corner cases and study the distribution of device-performance resulting out of these variations. The physical meaning of the device-model parameters enable such studies. However in an academic setting, the model with inclusion of proper formulation for charges in the gate-oxide and passivation-layers can enable to identification of possible location and nature of these charges to help eliminate the effect through technology innovations.

- Increased complexity of RF-parasitic network compared to the standard Kondoh-topology used currently in the MVSG-model.

  The parasitic network used in the MVSG-model formulation to include device-level parasitics seems to capture the RF-device behavior reasonably well until the W-band frequency range (up to $\approx$ 100 GHz). For applications beyond these frequencies, such lumped circuit-approach may not be sufficient and the parasitic-network may have to be extended to multiple elements with parallel transistor needed for multiple fingers and each gate-line, along with distributed model for the contact leads and via-inductances. The only impediment to the implementation of such a distributed model is the increased node-count and increase in simulation times using this approach.

- Inclusion of bias-dependent substrate-loss and substrate-current in the MVSG model.

The substrate-loss due to the finite resistance of the buffer layer is included using an RC network between the source- and drain-terminals. The conductivity of the channel-layer formed in the substrate is currently captured as a bias-independent resistor extracted from S-parameter measurements in the MVSG-model. However the high V_{DS} in the off-state causes significant band-bending towards the drain-side of the device and depletes the charges in the buffer in this region. Bias-dependence of the substrate conductance is therefore critical for high-frequency RF applications with significant substrate-loss (particularly for GaN-on-Si). Capturing the substrate-channel as a secondary gated FET element (but with contact capacitances instead of source-drain contact resistances) could be the way to capture this effect.

- More circuit-level validation and benchmarking using circuits with increased complexity in terms of number of transistors and /or simulation complexity.

  The circuit-level validation presented in this thesis involves highly involved simulations for both RF and HV-circuits but still has limited number of transistors in the circuit. High density of GaN-FETs is unrealistic in both these application regimes but simulating the full system including the CMOS signal-processing and driver circuits can give better insight into the convergence robustness and simulation times yielded by the MVSG-model. The circuits used in this thesis also do not use very-wide devices especially for RF-applications and the distributed effects associated with wide-widths is not tested at the circuit-level. High-power RF circuits can be used to test the impact of these effects on the circuit-performance.

  The subsection described so far illustrates some of the possible research topics in modeling GaN-HEMTs that can be extensions to this thesis work. However as highlighted in the thesis, the developed MVSG-modeling framework is more generic and is capable of capturing any field-effect-transistor relevant for both RF- and HV-application domains. The model can therefore be used to study the performance of other recent emerging technologies for such application areas

and the methodology is briefly explained in the next subsection.

8.3.2 Extension of the MVSG model for emerging FET technologies

The MVSG-modeling framework developed in this thesis is not restricted by material technology used or the exact device geometry of the device and can capture the behavior of any semiconductor field-effect device. In addition, the second-order effects discussed and modeled in the MVSG-approach in this thesis are prevalent in most HV- and RF-technologies and the model formalisms for these effects can be adopted to such applications.

The MVSG-model can be easily extended to various wide-bandgap transistors proposed for HV-applications. While GaN-HEMTs are suitable for 600 V-power conversion applications, they are supposed to be less attractive for very HV-regimes particularly for $> 1000\ V$ applications. For such HV-applications, wide-bandgap (WBG) materials such as SiC, AlN, Ga_2O_3 [79], [80], [81] are considered to be promising alternatives but there is no formal proof for the improved figures of merit with these new wide-bandgap technologies. In this context, the MVSG-model developed in this thesis can be used as a tool to provide comparisons of the figure-of-merits (FoMs) among technologies. In particular, the switching FoM $BV^2/R_{on}C_g$ shown in this thesis for GaN-HEMTs can be evaluated for other technologies as a starting point to compare them and it requires accurate estimation of the transport parameters, electrostatic parameters for these technologies. The second important determinant of the performance of different technologies is the power dissipation and associated heating issue and can be estimated through accurate estimation of R_{th} associated with different channel- and buffer-layers from either first-principle calculations or from spectroscopy techniques [24]. Along with the thermal behavior of these materials, the MVSG-model calibrated against electrical data can be used to compute the power-density levels and temperature-rise in the device under operating conditions to demonstrate the thermal robustness of any of the emergent technology. In

addition to lateral FETs, the MVSG-model can also be applied to vertical HV-FETs where the model can be used for the lateral gated-region and the vertical transport and charge-depletion in the buffer layer can be captured as an additional transistor element. The vertical transistor model for FETs built on WBG-material platform is relevant for $> 1000\ V$-applications and so the MVSG-model can be used to serve the full operating regime in the power-conversion circuit application.

On the RF-side, the model can be adopted to describe conventional III-V HEMTs used in applications such as power amplification for communication (base-stations and radars), low-noise amplification and other HF-applications. The carrier transport in GaAs HEMTs, Si-LDMOS transistors can be captured using the model with suitable modifications to include behavioral nuances in these material systems and devices. The impact of various non-linear sources at the device-level on linear performance of the devices in RF-circuits, impact of self-heating on RF-device performance and so on can be studied using the model in such technologies. The model can be used to make relative comparisons of the power-density from each technology at various frequencies which enable to choose a material system for a particular application targeting a certain frequency band. This requires accurate estimation of the carrier transport in each material system that manifests as maximum current-drive and the estimation of the capacitances in each technology. Furthermore, realistic circuit-level simulations in each technology targeting specific applications can be performed using the model to translate the material benefits to the application-domain.

The flow of this thesis and its organizational structure is aimed to reflect the sequence of steps that are involved in developing a physics-based compact device model and translate the device-physics to circuit-design usable functionality. This involves understanding the principle of operation of the device and translating the relevant transport equations to simple model formulations by making reasonable assumptions that do not affect the accuracy of the model. It also involves verifying the accuracy against various device-level measurements and finally using the model in circuit-simulations to verify its usability. The methodology adopted in the thesis can be used for evaluating any new technology, learn about its usability and the tasks in-

volved in commercializing the technology to the end-use circuit products. The work could potentially be used as a reference framework for developing compact device models of use to the semiconductor technology community.

Appendix A

Verilog-A code

```
////////////////////////////////////////////////////////////////////////////////////////////////////

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////////////////////////////////////////////////////////////////////////////////////////////////////
```

```
// Model details:  U. Radhakrishna, et al, IEDM 2012, 2013, 2014, 2015.
// Implemented on 5/09/2016, 2015 by U. Radhakrishna

`include "disciplines.vams"
`include "constants.vams"

// Mathematical Constants
`define M_MAXEXP       (34.0)

module mvsg (d, g, s, b);

inout d, g, s, b;
electrical d, g, s, b;
electrical di, gi, si, fp1, fp2, fp3, fp4, drc, src, tr, tr1;
thermal dt;

// Instance parameters               Default value   Range
   Units         Desc
   parameter real    w               = 3.0e-3        from(0.0:inf];        // m
                  Width per Finger
   parameter real    l               = 1.0e-6        from(0.0:inf];        // m
                  Length
   parameter real    ngf             = 1.0           from(0.0:inf];        //
                  Number of Fingers

// Model parameters                  Default value   Range
   Units         Desc
   parameter real    version         = 1.10          from[0.0:inf];        //
                  Version
   parameter real    tnom            = 27.0          from[-273.15:inf];    //
                    tnom for temperature model
   parameter integer type            = 1             from[-1:1] exclude 0; //
                  nFET=1 pFET=-1
   parameter real    cg              = 1.70e-03      from(0.0:inf];        // F/m
      ^2         Gate Cap/Area
   parameter real    cifm            = 0             from[0.0:inf);        // F/m
                Inner fringing cap on each side (not used)
   parameter real    cofsm           = 1.6e-9        from[0.0:inf];        // F/m
                Gate - Source Outer Fringing Cap/Width
   parameter real    cofdm           = 1.0e-19       from[0.0:inf];        // F/m
                Gate - Drain Outer Fringing Cap/Width
   parameter real    cofdsm          = 8.0e-10       from[0.0:inf];        // F/m
                Source - Drain Outer Fringing Cap/Width
   parameter real    cofdsubm        = 0.0e-14       from[0.0:inf];        // F/m
                Sub - Drain Outer Fringing Cap/Width
   parameter real    cofssubm        = 0.0e-14       from[0.0:inf];        // F/m
                Sub - Source Outer Fringing Cap/Width
   parameter real    cofgsubm        = 3e-10         from[0.0:inf];        // F/m
                Sub - Gate Outer Fringing Cap/Width
   parameter real    rsh             = 100.0         from[-inf:inf];       // Ohms
      /Sq        2-DEG Sheet Resistance
   parameter real    rcs             = 0.21e-2       from[-inf:inf];       // Ohms
      *m         Source contact resistance * Width
```

```
  parameter real    rcd             = 0.21e-2       from[-inf:inf];       // Ohms
     *m        Drain contact resistance * Width
  parameter real    vx0             = 1.2e5         from(0.0:inf];        // m/s
               Source injection velocity
  parameter real    mu0             = 0.100         from(0.0:inf];        // m^2/
     Vs        Low-field Mobility
  parameter real    beta            = 1.16          from(0.0:inf];        // m/s
               Linear to Saturation Parameter
  parameter real    vto             = -3.9          from[-inf:inf];       // V
                 Threshold Voltage
  parameter real    ss              = 0.10          from(0.0:inf];        // V/
     dec          Sub-threshold Slope
  parameter real    delta1          = 0.005         from[0.0:inf];        //
                   DIBL Coefficient
  parameter real    delta2          = 0.00          from[0.0:inf];        //
                   DIBL Coefficient
  parameter real    dibsat          = 10.0          from[0.0:inf];        // V
                 DIBL Saturation Voltage
  parameter real    nd              = 0.0           from[0.0:inf];        //
                   Punchthrough factor for Subth Slope
  parameter real    alpha           = 3.5           from[0.0:inf];        //
                   Weak to Strong Inversion Transition Factor
  parameter real    lambda          = 0.0           from[0.0:inf];        // 1/V
               CLM Parameter
  parameter real    vtheta          = 0.0           from[0.0:inf];        //
                   Scattering: velocity reduction parameter with Vg
  parameter real    mtheta          = 0.0           from[0.0:inf];        //
                   Scattering: mobility reduction parameter with Vg
  parameter real    vzeta           = 4e-3          from[-inf:inf];       //
                   VXO dependence on temperature
  parameter real    vtzeta          = -1e-3         from[-inf:inf];       //
                   vto dependence on temperature
  parameter real    epsilon         = 3.0           from[0.0:inf];        //
                   Mobility dependence on temperature
  parameter real    rct1            = 0.0           from[-inf:inf);       //
                   Rsh and Rc temperature coefficient
  parameter real    rct2            = 0.0           from[-inf:inf);       //
                   Rsh and Rc temperature coefficient

  parameter integer flagres         = 0             from[0:1];            //
                   Flag parameter for resistor: resistor is chosen if flagres=1
     or implicit transitor is chosen if flagres=0

//Source access region parameter
  parameter real    lgs             = 2.0e-6        from[0.0:inf];        // m
                 Source access region distance
  parameter real    vtors           = -650          from[-inf:inf];       // V
                 SAR Threshold Voltage
  parameter real    cgrs            = 80e-5         from[0:inf];          // F/m
     ^2         SAR to Drain Cap/Area
  parameter real    vx0rs           = 1.0e5         from(0.0:inf];        // m/s
               SAR Source injection velocity
  parameter real    mu0rs           = 0.100         from(0.0:inf];        // m^2/
     Vs        SAR Low-field Mobility
```

```
   parameter real    betars          = 1.1           from(0.0:inf];        //
                    Linear to Saturation Parameter
   parameter real    delta1rs        = 4e-4          from[0.0:inf];        //
                    SAR DIBL Coefficient
   parameter real    srs             = 0.065         from(0.0:inf];        // V/
      dec          SAR Sub-threshold Slope
   parameter real    ndrs            = 0.0           from[0.0:inf];        //
                    SAR Punchthrough factor for Subth Slope
   parameter real    vthetars        = 0.0           from[0.0:inf];        //
                    SAR Scattering: velocity reduction parameter with Vg
   parameter real    mthetars        = 0.0           from[0.0:inf];        //
                    SAR Scattering: mobility reduction parameter with Vg
   parameter real    alphars         = 3.5           from[0.0:inf];        //
                    SAR Weak to Strong Inversion Transition Factor

//Drain access region parameter
   parameter real    lgd             = 7.0e-6        from[0.0:inf];        // m
                  Drain access region distance
   parameter real    vtord           = -650.0        from[-inf:inf];       // V
                  DAR Threshold Voltage
   parameter real    cgrd            = 70e-5         from[0:inf];          // F/m
      ^2          DAR to Drain Cap/Area
   parameter real    vx0rd           = 1.0e5         from(0.0:inf];        // m/s
                DAR Source injection velocity
   parameter real    mu0rd           = 0.100         from(0.0:inf];        // m^2/
      Vs         DAR Low-field Mobility
   parameter real    betard          = 1.1           from(0.0:inf];        //
                    Linear to Saturation Parameter
   parameter real    delta1rd        = 4e-4          from[0.0:inf];        //
                    DAR DIBL Coefficient
   parameter real    srd             = 0.08          from(0.0:inf];        // V/
      dec          DAR Sub-threshold Slope
   parameter real    ndrd            = 0.0           from[0.0:inf];        //
                    DAR Punchthrough factor for Subth Slope
   parameter real    vthetard        = 0.0           from[0.0:inf];        //
                    DAR Scattering: velocity reduction parameter with Vg
   parameter real    mthetard        = 0.0           from[0.0:inf];        //
                    DAR Scattering: mobility reduction parameter with Vg
   parameter real    alphard         = 3.5           from[0.0:inf];        //
                    DAR Weak to Strong Inversion Transition Factor

//Field-Plate 1 parameters
   parameter integer flagfp1         = 1             from[0:1];            //
                    Flag parameter: GFP=1 or SFP=0
   parameter real    lgfp1           = 0             from[0.0:inf];        // m
                  FP Length
   parameter real    vtofp1          = -44.5         from[-inf:inf];       // V
                  FP Threshold Voltage
   parameter real    cgfp1           = 2.0e-4        from[0:inf];          // F/m
      ^2          FP to Drain Cap/Area
   parameter integer flagfp1s        = 1             from[0:1];            //
                    Flag parameter: cfp1s select=1 or cfp1s not select=0
   parameter real    cfp1s           = 1e-19         from[0:inf];          // F/m
                FP (source-side) to Source Cap/Width
```

```
   parameter real    ccfp1           = 0.9e-10       from[0:inf];          // F/m
                Source or Gate to Drain (under FP) Cap/Width
   parameter real    cbfp1           = 0.0           from[0:inf];          // F/m
                Body to Drain (under FP) Cap/Width
   parameter real    vx0fp1          = 1.2e5         from(0.0:inf];        // m/s
                FP Source injection velocity
   parameter real    mu0fp1          = 0.2           from(0.0:inf];        // m^2/
      Vs        FP Low-field Mobility
   parameter real    betafp1         = 1.16          from(0.0:inf];        //
                    Linear to Saturation Parameter
   parameter real    delta1fp1       = 0.00          from[0.0:inf];        //
                    FP DIBL Coefficient
   parameter real    sfp1            = 3.2           from(0.0:inf];        // V/
      dec         FP Sub-threshold Slope
   parameter real    ndfp1           = 0.0           from[0.0:inf];        //
                    FP Punchthrough factor for Subth Slope
   parameter real    vthetafp1       = 0.0           from[0.0:inf];        //
                    FP Scattering: velocity reduction parameter with Vg
   parameter real    mthetafp1       = 0.0           from[0.0:inf];        //
                    FP Scattering: mobility reduction parameter with Vg
   parameter real    alphafp1        = 1e-2          from[0.0:inf];        //
                    FP Weak to Strong Inversion Transition Factor

//Field-Plate 2 parameters
   parameter integer flagfp2         = 0             from[0:1];            //
                    Flag parameter: GFP=1 or SFP=0
   parameter real    lgfp2           = 0             from[0.0:inf];        // m
                  FP Length
   parameter real    vtofp2          = -60.0         from[-inf:inf];       // V
                  FP Threshold Voltage
   parameter real    cgfp2           = 9.0e-5        from[0:inf];          // F/m
      ^2          FP to Drain Cap/Area
   parameter integer flagfp2s        = 0             from[0:1];            //
                    Flag parameter: cfp2s select=1 or cfp2s not select=0
   parameter real    cfp2s           = 0.0           from[0:inf];          // F/m
                FP (source-side) to Source Cap/Width
   parameter real    ccfp2           = 0.65e-10      from[0:inf];          // F/m
                Source or Gate to Drain (under FP) Cap/Width
   parameter real    cbfp2           = 0.0           from[0:inf];          // F/m
                Body to Drain (under FP) Cap/Width
   parameter real    vx0fp2          = 1.9e5         from(0.0:inf];        // m/s
                FP Source injection velocity
   parameter real    mu0fp2          = 0.29          from(0.0:inf];        // m^2/
      Vs        FP Low-field Mobility
   parameter real    betafp2         = 1.16          from(0.0:inf];        //
                    Linear to Saturation Parameter
   parameter real    delta1fp2       = 0.00          from[0.0:inf];        //
                    FP DIBL Coefficient
   parameter real    sfp2            = 4.1           from(0.0:inf];        // V/
      dec         FP Sub-threshold Slope
   parameter real    ndfp2           = 0.0           from[0.0:inf];        //
                    FP Punchthrough factor for Subth Slope
   parameter real    vthetafp2       = 0.0           from[0.0:inf];        //
                    FP Scattering: velocity reduction parameter with Vg
```

```
   parameter real    mthetafp2       = 0.0           from[0.0:inf];        //
                    FP Scattering: mobility reduction parameter with Vg
   parameter real    alphafp2        = 1.3e3         from[0.0:inf];        //
                    FP Weak to Strong Inversion Transition Factor

//Field-Plate 3 parameters
   parameter integer flagfp3         = 1             from[0:1];            //
                    Flag parameter: GFP=1 or SFP=0
   parameter real    lgfp3           = 0.0           from[0.0:inf];        // m
                  FP Length
   parameter real    vtofp3          = -120.0        from[-inf:inf];       // V
                  FP Threshold Voltage
   parameter real    cgfp3           = 1.0e-3        from[0:inf];          // F/m
      ^2         FP to Drain Cap/Area
   parameter integer flagfp3s        = 0             from[0:1];            //
                    Flag parameter: cfp3s select=1 or cfp3s not select=0
   parameter real    cfp3s           = 0.0           from[0:inf];          // F/m
                FP (source-side) to Source Cap/Width
   parameter real    ccfp3           = 0.0           from[0:inf];          // F/m
                Source or Gate to Drain (under FP) Cap/Width
   parameter real    cbfp3           = 0.0           from[0:inf];          // F/m
                Body to Drain (under FP) Cap/Width
   parameter real    vx0fp3          = 1.0e5         from(0.0:inf];        // m/s
                FP Source injection velocity
   parameter real    mu0fp3          = 0.17          from(0.0:inf];        // m^2/
      Vs         FP Low-field Mobility
   parameter real    betafp3         = 1.0           from(0.0:inf];        //
                    Linear to Saturation Parameter
   parameter real    delta1fp3       = 0.01          from[0.0:inf];        //
                    FP DIBL Coefficient
   parameter real    sfp3            = 0.1           from(0.0:inf];        // V/
      dec          FP Sub-threshold Slope
   parameter real    ndfp3           = 0.0           from[0.0:inf];        //
                    FP Punchthrough factor for Subth Slope
   parameter real    vthetafp3       = 0.0           from[0.0:inf];        //
                    FP Scattering: velocity reduction parameter with Vg
   parameter real    mthetafp3       = 0.0           from[0.0:inf];        //
                    FP Scattering: mobility reduction parameter with Vg
   parameter real    alphafp3        = 3.5           from[0.0:inf];        //
                    FP Weak to Strong Inversion Transition Factor

//Field-Plate 4 parameters
   parameter integer flagfp4         = 1             from[0:1];            //
                    Flag parameter: GFP=1 or SFP=0
   parameter real    lgfp4           = 0.0           from[0.0:inf];        // m
                  FP Length
   parameter real    vtofp4          = -220.0        from[-inf:inf];       // V
                  FP Threshold Voltage
   parameter real    cgfp4           = 1.0e-3        from[0:inf];          // F/m
      ^2         FP to Drain Cap/Area
   parameter integer flagfp4s        = 0             from[0:1];            //
                    Flag parameter: cfp4s select=1 or cfp4s not select=0
   parameter real    cfp4s           = 0.0           from[0:inf];          // F/m
                FP (source-side) to Source Cap/Width
```

```
  parameter real    ccfp4           = 0.0           from[0:inf];          // F/m
              Source or Gate to Drain (under FP) Cap/Width
  parameter real    cbfp4           = 0.0           from[0:inf];          // F/m
              Body to Drain (under FP) Cap/Width
  parameter real    vx0fp4          = 1.0e5         from(0.0:inf];        // m/s
              FP Source injection velocity
  parameter real    mu0fp4          = 0.17          from(0.0:inf];        // m^2/
     Vs       FP Low-field Mobility
  parameter real    betafp4         = 1.0           from(0.0:inf];        //
                   Linear to Saturation Parameter
  parameter real    delta1fp4       = 0.01          from[0.0:inf];        //
                   FP DIBL Coefficient
  parameter real    sfp4            = 0.1           from(0.0:inf];        // V/
     dec          FP Sub-threshold Slope
  parameter real    ndfp4           = 0.0           from[0.0:inf];        //
                   FP Punchthrough factor for Subth Slope
  parameter real    vthetafp4       = 0.0           from[0.0:inf];        //
                   FP Scattering: velocity reduction parameter with Vg
  parameter real    mthetafp4       = 0.0           from[0.0:inf];        //
                   FP Scattering: mobility reduction parameter with Vg
  parameter real    alphafp4        = 3.5           from[0.0:inf];        //
                   FP Weak to Strong Inversion Transition Factor
  parameter real    rgsp            = 0.0           from[0.0:inf];        // Ohms
     *m         Gate resistance * Width

// Gate leakage
  parameter integer igmod           = 0             from[0: 1];           //
                   Choice of gate leakage model set to 0
  parameter real    vjg             = 1             from(0.0:inf);        // V
                 Gate diode cut in voltage [V]
  parameter real    pg_param1       = 0.45          from[0.0:inf);        // 1/V
              Something like 1/eta

  parameter real    pg_params       = 0.3           from[0.0:inf);        // 1/V
              G-S something like 1/eta*Vt
  parameter real    ijs             = 0.00e3        from[0.0:inf);        // A/m
              G-S reverse leakage current normalized to width [A/cm]
  parameter real    vgsats          = 3             from[0.0:inf);        // V
                G-S high injection effect
  parameter real    fracs           = 1             from[0.0:inf);        //
                   G-S fractional change in ideality factor due to high
     injection
  parameter real    alphags         = 10            from[0.0:inf);        //
                   G-S high injection smoothing parameter
  parameter real    pg_paramd       = 0.38          from[0.0:inf);        // 1/V
              G-D something like 1/eta*Vt [1/V]
  parameter real    ijd             = 0.00e3        from[0.0:inf);        // A/m
              G-D reverse leakage current normalized to width [A/cm]
  parameter real    vgsatd          = 3             from[0.0:inf);        // V
                G-D high injection effect
  parameter real    fracd           = 1             from[0.0:inf);        //
                   G-D fractional change in ideality factor due to high
     injection
  parameter real    alphagd         = 10            from[0.0:inf);        //
```

```
                G-D high injection smoothing parameter

parameter real    pgsrecs         = 0.8           from[0.0:inf);        //
                G-S something like 1/eta
parameter real    irecs           = 000e-12       from[0.0:inf);        // A/m
            G-S reverse leakage current normalized to width [A/cm]
parameter real    vgsatqs         = 3.4           from[0.0:inf);        // V
              G-S mimics depletion saturation
parameter real    vbdgs           = 600           from[0.0:inf);        // V
              G-S soft breakdown voltage of GD diode
parameter real    pbdgs           = 4             from[0.0:inf);        //
                G-S fitting parameter
parameter real    kbdgates        = 0.0           from[0.0:inf);        //
                G-S fitting parameter
parameter real    betarecs        = 0.35          from[0.0:inf);        //
                G-S fitting parameter
parameter real    pgsrecd         = 0.957         from[0.0:inf);        //
                G-D something like 1/eta
parameter real    irecd           = 0e-18         from[0.0:inf);        // A/m
            G-D reverse leakage current normalized to width [A/cm]
parameter real    vgsatqd         = 0.55          from[0.0:inf);        // V
              G-D mimics depletion saturation
parameter real    vbdgd           = 600           from[0.0:inf);        // V
              G-D soft breakdown voltage of GS diode
parameter real    pbdgd           = 4             from[0.0:inf);        //
                G-D fitting parameter
parameter real    kbdgated        = 0.0           from[0.0:inf);        //
                G-D fitting parameter
parameter real    betarecd        = 0.734         from[0.0:inf);        //
                G-D fitting parameter

parameter real    rth             = 0             from [0:inf);         // K/W
              Thermal resistance
parameter real    cth             = 1e-4          from [0:inf);         // s.W/
   K          Thermal capacitance


parameter integer trapselect      = 0             from [0: 1];          //
                Select knob for charge trapping
parameter real    vttrap          = 280           from [0:inf);         // V
              Trapping stress time constant
parameter real    taut            = 3.0e-4        from [0:inf);         // s
              Trap time constant
parameter real    ctrap           = 1e-3          from [0:inf);         // F
              DC-block capacitor
parameter real    alphat1         = 1e-4          from [0:inf);         //
                Trap coefficient on bias stress
parameter real    alphat2         = 21            from [0:inf);         //
                Trap coefficient on bias stress
parameter real    tempt           = 0e-4          from [0:inf);         //
                Temperature coefficient for trapping

parameter integer noisemod        = 0             from [0: 1];          //
                Choice of noise model
```

```
parameter real    shs             = 2.0           from [0:inf);         //
                 G-S shot noise parameter
parameter real    shd             = 2.0           from [0:inf);         //
                 G-D shot noise parameter
parameter real    kf              = 0.0           from [0:inf];         //
                 Flicker noise coeff
parameter real    af              = 1.0           from (0:inf];         //
                 Flicker noise exponent
parameter real    ffe             = 1.0           from (0:inf];         //
                 Flicker noise parameter

parameter real    minr            = 1.0e-3        from[0.0:inf];        // Ohms
             Minimum resistance
parameter real    minl            = 1.0e-9        from[0.0:inf];        // m
               Minimum length
parameter real    minc            = 1.0e-15       from[0.0:inf];        // F
               Minimum capacitance

analog function real absfunc;
   input x;
   real x;
   begin
      absfunc=sqrt( x * x + 4.0 * 1e-5  );
   end
endfunction

analog function real mmax;
   input x,y;
   real x,y;
   begin
      mmax=0.5*( x + y + sqrt( ( x - y ) * ( x - y ) + 4.0 * 1e-5 ));
   end
endfunction

analog function real sd_dir;
   inout vgsout,vdsout;
   input type,vgsin,vgdin,vdsin;
   real  vgsout,vdsout,type,vgsin,vgdin,vdsin;
   real  vgsType, vgdType, vdsType;
   begin
      vgsType      = vgsin * type;
      vgdType      = vgdin * type;
      vdsType      = vdsin * type;
      vgsout       = vgsType;
      vdsout       = vdsType;
      sd_dir       = 1.0;
   end
endfunction // sd_dir

analog function real calc_iq;
   output idsout,qgsout,qgdout,qcout,qbout,qsout;
   input vgsin,vdsin,qcbflag,vcin,vbin,qgsflag,dirin,tambin,tnomin,phitin,w,lin
      ,cgin,cs,cc,cb,vto,ss;
   input delta1,delta2,nd,alpha,vel0,mu0,beta,mtheta,vtheta;
```

```
input vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type;

// IO
real  idsout,qgsout,qgdout,qcout,qbout,qsout,vgsin,vdsin,qcbflag,vcin,vbin,
   qgsflag,dirin;
real  tambin,tnomin,phitin,w,lin,cgin,cs,cc,cb,vto,ss,delta1,delta2,nd,alpha
   ,vel0,mu0,beta,mtheta,vtheta;
real  vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type;

// Local
real  alpha_phit, delta, n, vtof, vsatdibl, ffs, two_n_phit, qref, etas,
   qinvs, muf, vx, vxf;
real  alpha_phit0, n0, ffs0, two_n_phit0, qref0, etas0, qinvs0, muf0, vx0,
   vxf0;
real  ff, eta, qinvv;
real  ff0, eta0, qinvv0;
real  vdsats, vdsats1, vdsat, vdsat1, fsd, vdx, fds, vsx, ffd, etad, qinvd,
   vdsc, fsat, vel;
real  vdsats0, vdsats10, vdsat0, vdsat10, fsd0, vdx0, fds0, vsx0, ffd0,
   etad0, qinvd0;
real  qs2, qs3, qd2, qd3, qsqd, qinvdd, qd1, qs, qd, etac, etab, etags;
real  exparg, myarg, absvdsin, vgdin;
real  exparg0, myarg0;

begin
   absvdsin     = absfunc( vdsin );
   vgdin        = vgsin - vdsin;
   alpha_phit   = alpha * phitin;
   n            = ss / ( `M_LN10 * phitin ) + nd * absvdsin;
   vtof         = vto + vtzeta * ( tambin - tnomin );
   if (beta != 0 && dibsat != 0) vsatdibl = absvdsin / ( pow(( 1.0 + pow(
      absvdsin / dibsat, beta)),( 1.0/beta )));
   else  vsatdibl = 0;
   delta        = ( delta1 - vsatdibl * delta2 ) * absvdsin;
   two_n_phit   = 2.0 * n * phitin;
   qref         = cgin * two_n_phit;
   // Qinvv
   myarg        = vtof - delta - alpha_phit / 2.0;
   exparg       = (( mmax( vgsin,vgdin ) - myarg ) / ( alpha_phit ));
   if (exparg > `M_MAXEXP) ff = 0.0;
   else if (exparg < -`M_MAXEXP) ff =1.0;
   else ff      = 1.0 / ( 1.0 + exp( exparg ));
   eta          = ( mmax( vgsin,vgdin ) - ( vtof - delta - 0.1 * alpha_phit
      * ff )) / two_n_phit;
   if (eta > `M_MAXEXP) qinvv = qref * eta;
   else if (eta < -`M_MAXEXP) qinvv = 0;
   else qinvv   = qref * ln( 1.0 + exp( eta ));
   // velocity
   muf          = mu0 / (( pow(( tambin / tnomin ), epsilon )) * ( 1.0 +
      mtheta * qinvv /cgin ));
   vx           = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin
      )) * ( 1.0 + lambda * absvdsin /lin) / ( 1.0 + vtheta * qinvv/ cgin )
      ;
   vxf          = 2.0 * ff * phitin * muf / lin + ( 1.0 - ff ) * vx;
```

```
vdsats        = vx * lin / muf;
vdsats1       = vdsats * sqrt( 1.0 + 2.0 * qinvv / cgin / vdsats ) -
   vdsats;
vdsat         = vdsats * ( 1.0 - ff ) + two_n_phit * ff;
vdsat1        = vdsats1 * ( 1.0 - ff ) + two_n_phit * ff;
fsd           = 1.0 / pow( 1.0 + pow( mmax( 0,( vdsin / vdsat1 )),beta )
   ,1.0 / beta);
vdx           = vdsin * fsd;
fds           = 1.0 / pow( 1.0 + pow( mmax( 0,( -vdsin / vdsat1 )),beta)
   ,1.0 / beta);
vsx           = -vdsin * fds;
// Qinvs
exparg        = ( vgsin - myarg ) / ( alpha_phit );
if (exparg > `M_MAXEXP) ffs = 0.0;
else if (exparg < -`M_MAXEXP) ffs = 1.0;
else ffs      = 1.0  /( 1.0 +  exp( exparg ));
etas          = ( vgdin - vsx - ( vtof - delta - 0.1 * alpha_phit * ffs ))
    / two_n_phit;
if (etas > `M_MAXEXP) qinvs = qref * etas;
else if (etas < -`M_MAXEXP) qinvs = 0;
else qinvs    = qref * ln( 1.0 + exp( etas ));
// Qinvd
exparg        = ( vgdin - myarg ) / ( alpha_phit );
if (exparg > `M_MAXEXP) ffd = 0.0;
else if (exparg < -`M_MAXEXP) ffd = 1.0;
else ffd      = 1.0 / ( 1.0 + exp( exparg ));
etad          = ( vgsin - vdx - ( vtof - delta - 0.1 * alpha_phit * ffd ))
    / two_n_phit;
if (etad > `M_MAXEXP) qinvd = qref * etad;
else if (etad < -`M_MAXEXP) qinvd = 0;
else qinvd    = qref * ln( 1.0 + exp( etad ));
// Current
vdsc          = ( qinvs - qinvd ) / cgin;
myarg         = vdsc / vdsat;
fsat          = myarg / ( pow( 1.0 + pow( absfunc( myarg ),beta), 1.0 /
   beta));
vel           = vxf * fsat;
idsout        = dirin * type * w * ngf * 0.5 * ( qinvs + qinvd ) * vel;

// charge calc
n0            = ss / ( `M_LN10 * phitin );
two_n_phit0   = 2.0 * n0 * phitin;
qref0         = cgin * two_n_phit0;
// Qinvv0
myarg0        = vtof - alpha_phit / 2.0;
exparg0       = (( mmax( vgsin,vgdin ) - myarg0 )/( alpha_phit ));
if (exparg0 > `M_MAXEXP) ff0 = 0.0;
else if (exparg0 < -`M_MAXEXP) ff0 = 1.0;
else ff0      = 1.0 / ( 1.0 + exp( exparg0 ));
eta0          = ( mmax( vgsin,vgdin ) - ( vtof - 0.1 * alpha_phit * ff0 ))
    / two_n_phit0;
if (eta0 > `M_MAXEXP) qinvv0 = qref0 * eta0;
else if (eta0 < -`M_MAXEXP) qinvv0 = 0;
else qinvv0   = qref0 * ln( 1.0 + exp( eta0 ));
```

```
// velocity0
muf0          = mu0 / (( pow(( tambin / tnomin ),epsilon )));
vx0           = vel0 * (( 1.0 + vzeta * tnomin ) / ( 1.0 + vzeta * tambin
   ));
vxf0          = 2.0 * ff0 * phitin * muf0 / lin + ( 1.0 - ff0 ) * vx0;
vdsats0       = vx0 * lin / muf0;
vdsats10      = vdsats0 * sqrt( 1.0 + 2.0 * qinvv0 / cgin / vdsats0 ) -
   vdsats0;
vdsat0        = vdsats0 * ( 1.0 - ff0 ) + two_n_phit0 * ff0;
vdsat10       = vdsats10 * ( 1.0 - ff0 ) + two_n_phit0 * ff0;
fsd0          = 1.0 / pow( 1.0 + pow( mmax(0,( vdsin / vdsat10 )),beta )
   ,1.0 / beta);
vdx0          = vdsin * fsd0;
fds0          = 1.0 / pow( 1.0 + pow( mmax(0,( -vdsin / vdsat10 )),beta )
   ,1.0 / beta);
vsx0          = -vdsin * fds0;
exparg0       = ( vgsin - myarg0 ) / ( alpha_phit );
if (exparg0 > `M_MAXEXP) ffs0 = 0.0;
else if (exparg0 < -`M_MAXEXP) ffs0 = 1.0;
else ffs0     = 1.0 / ( 1.0 + exp( exparg0 ));
etas0         = ( vgdin - vsx0 - ( vtof - 0.1 * alpha_phit * ffs0 )) /
   two_n_phit0;
if (etas0 > `M_MAXEXP) qinvs0 = qref0 * etas0;
else if (etas0 < -`M_MAXEXP) qinvs0 = 0;
else qinvs0   = qref0 * ln( 1.0 + exp( etas0 ));
exparg0       = ( vgdin - myarg0 ) / ( alpha_phit );
if (exparg0 > `M_MAXEXP) ffd0 = 0.0;
else if (exparg0 < -`M_MAXEXP) ffd0 = 1.0;
else ffd0     = 1.0 / ( 1.0 + exp( exparg0 ));
etad0         = ( vgsin - vdx0 - ( vtof - 0.1 * alpha_phit * ffd0 )) /
   two_n_phit0;
if (etad0 > `M_MAXEXP) qinvd0 = qref0 * etad0;
else if (etad0 < -`M_MAXEXP) qinvd0 = 0;
else qinvd0   = qref0 * ln( 1.0 + exp( etad0 ));

qs2           = qinvs0 * qinvs0 + 1e-38;
qs3           = qs2 * qinvs0 + 1e-57;
qd2           = qinvd0 * qinvd0 + 1e-38;
qd3           = qd2 * qinvd0 + 1e-57;
qsqd          = qinvs0 * qinvd0 + 1e-38;
qinvdd        = 2.0 / 3.0 * ( qs2 + qd2 + qsqd ) / ( qinvs0 + qinvd0 + 2e
   -19 );
qd1           = 2.0 * ( 2.0 * qs3 + 3.0 * qd3 + 4.0 * qs2 * qinvd0 + 6.0 *
    qd2 * qinvs0 ) / ( 15.0 * ( qs2+ qd2 + 2.0 * qsqd ));
qs            = qinvdd - qd1;
qd            = qd1;
qgsout        = w * ngf * lin * type * qs;
qgdout        = w * ngf * lin * type * qd;
if (qcbflag==1) begin
   etac       = ( vcin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
   if (etac > `M_MAXEXP) exparg = etac;
   else if (etac < -`M_MAXEXP) exparg = 0;
   else exparg = ln( 1.0 + exp( etac ));
   qcout      = w * ngf * type * cc * two_n_phit0 * exparg;
```

```
      etab      = ( vbin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
      if (etab > `M_MAXEXP) exparg = etab;
      else if (etab < -`M_MAXEXP) exparg = 0;
      else exparg = ln( 1.0 + exp( etab ));
      qbout     = w * ngf * type * cb * two_n_phit0 * exparg;
   end else begin
      qcout     = 0;
      qbout     = 0;
   end
   if (qgsflag==1) begin
      etags     = ( vgsin - ( vtof - 0.5 * alpha_phit )) / two_n_phit0;
      if (etags > `M_MAXEXP) exparg = etags;
      else if (etags < -`M_MAXEXP) exparg = 0;
      else exparg = ln( 1.0 + exp( etags  ));
      qsout     = w * ngf * type * cs * two_n_phit0 * exparg;
   end else begin
      qsout     = 0;
   end
   calc_iq      = idsout;
end
endfunction


analog function real calc_ig;
   output igout, isdiodeout, isrecout;
   input vgin, phitin;
   input vgsatin, alphagin, fracin, pg_paramin, pbdgin, vbdgin, tambin, tnomin;
   input w, ngf,ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin,
      pg_param1, vjg;
   //IO
   real igout, isdiodeout, isrecout;
   real vgin, phitin;
   real vgsatin, alphagin, fracin, pg_paramin, pbdgin, vbdgin, tambin, tnomin;
   real w, ngf,ijin, kbdgatein, vgsatqin, betarecin, irecin, pgsrecin,
      pg_param1, vjg;
   // Local
   real  alpha_phit, t0, ffvgin, pgin, iginbd, tfacdiode, igindiode;
   real  frecgin, iginrec;

   begin
      alpha_phit   = alphagin * phitin;
      t0           = exp( pg_param1 / phitin *  - vjg );
      ffvgin       = 1.0 / ( 1.0 + exp(( vgin - ( vgsatin - alphagin *
         alpha_phit / 2.0))/( alphagin * alpha_phit )));
      pgin         = ( fracin * pg_paramin + ( 1.0 - fracin) * pg_paramin *
         ffvgin );
      iginbd       = ( exp( pbdgin * ( -vgin  - vbdgin ) ) - exp( -pbdgin *
         vbdgin ) );
      tfacdiode    = pow( ( tambin / tnomin ) , 3.0 );
      isdiodeout   = w * ngf * ijin * tfacdiode * t0;
      igindiode    = isdiodeout * ( exp( pgin / phitin * vgin ) - ( kbdgatein *
          iginbd ) - 1.0 );

      frecgin      = -vgin / pow(( 1.0 + pow( absfunc( vgin  / vgsatqin ),
```

```
            betarecin )), 1.0 / betarecin );
         isrecout     = -w * ngf * irecin * tfacdiode * 1.0;
         iginrec      = isrecout * ( exp( pgsrecin / phitin * frecgin ) - 1.0 );

         igout        = igindiode + iginrec;
         calc_ig      = igout;
      end
   endfunction

// Local variables
   real mygmin, mycmin;
   real rd, rs, rg;
   real dir, dirrs, dirrd, dirfp1, dirfp2, dirfp3, dirfp4;
   real vdsi, vgsi, vigs, vigd, vgsrs, vdsrs, vgsrd, vdsrd, vgsfp1, vdsfp1, vcfp1,
       vbfp1;
   real vgsfp2, vdsfp2, vcfp2, vbfp2, vgsfp3, vdsfp3, vcfp3, vbfp3;
   real vgsfp4, vdsfp4, vcfp4, vbfp4;
   real tambk, tnomk, tsh, tdut, phit, pdiss;
   real ids, qgs, qgd, qc, qb, qs, igs, igd, igssdio, igdsdio, igsrec, igdrec;
   real idsrs,  qgsrs, qgdrs, qcrs, qbrs, qsrs;
   real idsrd,  qgsrd, qgdrd, qcrd, qbrd, qsrd;
   real idsfp1, qgsfp1, qgdfp1, qcfp1, qbfp1, qsfp1;
   real idsfp2, qgsfp2, qgdfp2, qcfp2, qbfp2, qsfp2;
   real idsfp3, qgsfp3, qgdfp3, qcfp3, qbfp3, qsfp3;
   real idsfp4, qgsfp4, qgdfp4, qcfp4, qbfp4, qsfp4;
   real qofs, qofd, qofds, qofdsub, qofssub, qofgsub;
   real drsht, vtcollapse, vtcollapse0, ttrapfac;
   real gm, svc;

   (* desc="gate-source voltage", units="V" *) real vgsext;
   (* desc="gate-drain voltage", units="V" *) real vgdext;
   (* desc="drain-source voltage", units="V" *) real vdsext;
   (* desc="source-body voltage", units="V" *) real vsbext;
   (* desc="drain-body voltage", units="V" *) real vdbext;
   (* desc="drain current", units="A" *) real idext;
   (* desc="gate current", units="A" *) real igext;
   (* desc="source current", units="A" *) real isext;
   (* desc="body current", units="A" *) real ibext;

analog begin

   // Temperature dependence of voltage independent terms
   mygmin             = $simparam("gmin",1e-12);
   mygmin             = $simparam("gdev",mygmin);
   mycmin             = $simparam("cmin",0);
   tnomk              = tnom + `P_CELSIUS0;
   tambk              = $temperature;
   tsh                = Temp(dt);
   tdut               = tambk + tsh;
   rs                 = 0;
   rd                 = 0;
   if (flagres==0) begin
      rd              = ( rcd / w ) *  ( 1.0 + rct1 *  ( tdut-tnomk ) + rct2 *  (
         tdut - tnomk ) *  ( tdut -tnomk )) / ngf;
```

```
   rs              = ( rcs / w ) *  ( 1.0 + rct1 *  ( tdut-tnomk ) + rct2 *  (
      tdut - tnomk ) *  ( tdut -tnomk )) / ngf;
end else begin
   rd              = ( rcd / w + rsh * lgd / w ) *  ( 1.0 + rct1 *  ( tdut-
      tnomk ) + rct2 *  ( tdut - tnomk ) *  ( tdut -tnomk )) / ngf;
   rs              = ( rcs / w + rsh * lgs / w ) *  ( 1.0 + rct1 *  ( tdut-
      tnomk ) + rct2 *  ( tdut - tnomk ) *  ( tdut -tnomk )) / ngf;
end
rg                 = ( rgsp / w / ngf);
phit               = 'P_K * tdut / 'P_Q;
ttrapfac           = 1.0 + tempt * ( tdut-tnomk );

vdsi               = 0;
vgsi               = 0;
// Determines source for intrinsic transistor
dir                = sd_dir(vgsi,vdsi,type,V(gi,si),V(gi,di),V(di,si));

// Determines source for SAR transistor
vigs               = vtors + 1.0 / (rsh * cgrs * mu0);
vdsrs              = 0;
vgsrs              = 0;
dirrs              = sd_dir(vgsrs,vdsrs,type,(vigs - V(src,s)),(vigs - V(si,s))
   ,V(si,src));

// Trap time constant
if ( trapselect    != 0) begin
   vtcollapse0     = alphat1 * abs(V(d) - V(g)) + limexp( (V(d) - V(g) - vttrap
      ) / alphat2 );
   I(tr1)          <+ -vtcollapse0;
   I(tr1,tr)       <+ ddt(ctrap * V(tr1, tr));
   I(tr)           <+ ddt(taut * V(tr));
   I(tr)           <+ V(tr);
   vtcollapse      = V(tr);
   drsht           = 1.0 + (vtcollapse) * ttrapfac;
end else begin
   vtcollapse0     = 0;
   vtcollapse      = 0;
   V(tr1)          <+ 0;
   V(tr)           <+ 0;
   drsht           = 1.0;
end
// Determines source for DAR transistor
vigd               = vtord + 1.0 / (drsht * rsh * cgrd * mu0);
vdsrd              = 0;
vgsrd              = 0;
dirrd              = sd_dir(vgsrd,vdsrd,type,(vigd - V(fp4,s)),(vigd - V(drc,s)
   ),V(drc,fp4));

// Determines source for fp transistors
vdsfp1             = 0;
vgsfp1             = 0;
vdsfp2             = 0;
vgsfp2             = 0;
vdsfp3             = 0;
```

```
vgsfp3              = 0;
vdsfp4              = 0;
vgsfp4              = 0;
if (flagfp1 == 1) begin
   dirfp1           = sd_dir(vgsfp1,vdsfp1,type,V(gi,di),V(gi,fp1),V(fp1,di));
   vcfp1            = type * V(s,di);
end else begin
   dirfp1           = sd_dir(vgsfp1,vdsfp1,type,V(s,di),V(s,fp1),V(fp1,di));
   vcfp1            = type * V(gi,di);
end
vbfp1               = type * V(b,di);
if (flagfp2 == 1) begin
   dirfp2           = sd_dir(vgsfp2,vdsfp2,type,V(gi,fp1),V(gi,fp2),V(fp2,fp1));
   vcfp2            = type * V(s,fp1);
end else begin
   dirfp2           = sd_dir(vgsfp2,vdsfp2,type,V(s,fp1),V(s,fp2),V(fp2,fp1));
   vcfp2            = type * V(gi,fp1);
end
vbfp2               = type * V(b,fp1);
if (flagfp3 == 1) begin
   dirfp3           = sd_dir(vgsfp3,vdsfp3,type,V(gi,fp2),V(gi,fp3),V(fp3,fp2));
   vcfp3            = type * V(s,fp2);
end else begin
   dirfp3           = sd_dir(vgsfp3,vdsfp3,type,V(s,fp2),V(s,fp3),V(fp3,fp2));
   vcfp3            = type * V(gi,fp2);
end
vbfp3               = type * V(b,fp2);
if (flagfp4 == 1) begin
   dirfp4           = sd_dir(vgsfp4,vdsfp4,type,V(gi,fp3),V(gi,fp4),V(fp4,fp3));
   vcfp4            = type * V(s,fp3);
end else begin
   dirfp4           = sd_dir(vgsfp4,vdsfp4,type,V(s,fp3),V(s,fp4),V(fp4,fp3));
   vcfp4            = type * V(gi,fp3);
end
vbfp4               = type * V(b,fp3);

// current and charge calculations

idsfp4              = 0;
qgsfp4              = 0;
qgdfp4              = 0;
qcfp4               = 0;
qbfp4               = 0;
qsfp4               = 0;
if (lgfp4>=(minl)) begin
   idsfp4           = calc_iq(idsfp4,qgsfp4,qgdfp4,qcfp4,qbfp4,qsfp4,vgsfp4,
      vdsfp4,1,vcfp4,vbfp4,flagfp4s,dirfp4,tdut,tnomk,phit,w,lgfp4,cgfp4,cfp4s
      ,ccfp4,cbfp4,vtofp4,sfp4,delta1fp4,0.0,ndfp4,alphafp4,vx0fp4,mu0fp4,
      betafp4,mthetafp4,vthetafp4,vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type)
      ;
   I(fp4,fp3)       <+ idsfp4 + mygmin * V(fp4,fp3);
end else begin
   V(fp4,fp3)       <+ 0;
end
```

```
if (flagfp4==1) begin
   I(gi,fp3)        <+ ddt(qgsfp4) + ddt(minc * V(gi,fp3));
   I(gi,fp4)        <+ ddt(qgdfp4) + ddt(minc * V(gi,fp4));
   I(s,fp3)         <+ ddt(qcfp4) + ddt(minc * V(s,fp3));
   I(s,fp4)         <+ 0;
   I(gi,si)         <+ ddt(qsfp4) + ddt(minc * V(gi,si));
end else begin
   I(s,fp3)         <+ ddt(qgsfp4) + ddt(minc * V(s,fp3));
   I(s,fp4)         <+ ddt(qgdfp4) + ddt(minc * V(s,fp4));
   I(gi,fp3)        <+ ddt(qcfp4) + ddt(minc * V(gi,fp3));
   I(gi,fp4)        <+ 0;
   I(gi,si)         <+ 0;
end
I(b,fp3)            <+ ddt(qbfp4) + ddt(minc * V(b,fp3));

idsfp3              = 0;
qgsfp3              = 0;
qgdfp3              = 0;
qcfp3               = 0;
qbfp3               = 0;
qsfp3               = 0;
if (lgfp3>=(minl)) begin
   idsfp3           = calc_iq(idsfp3,qgsfp3,qgdfp3,qcfp3,qbfp3,qsfp3,vgsfp3,
      vdsfp3,1,vcfp3,vbfp3,flagfp3s,dirfp3,tdut,tnomk,phit,w,lgfp3,cgfp3,cfp3s
      ,ccfp3,cbfp3,vtofp3,sfp3,delta1fp3,0.0,ndfp3,alphafp3,vx0fp3,mu0fp3,
      betafp3,mthetafp3,vthetafp3,vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type)
      ;
   I(fp3,fp2)       <+ idsfp3 + mygmin * V(fp3,fp2);
end else begin
   V(fp3,fp2)       <+ 0;
end
if (flagfp3==1) begin
   I(gi,fp2)        <+ ddt(qgsfp3) + ddt(minc * V(gi,fp2));
   I(gi,fp3)        <+  ddt(qgdfp3) + ddt(minc * V(gi,fp3));
   I(s,fp2)         <+ ddt(qcfp3) + ddt(minc * V(s,fp2));
   I(s,fp3)         <+ 0;
   I(gi,si)         <+ ddt(qsfp3) + ddt(minc * V(gi,si));
end else begin
   I(s,fp2)         <+ ddt(qgsfp3) + ddt(minc * V(s,fp2));
   I(s,fp3)         <+  ddt(qgdfp3) + ddt(minc * V(s,fp3));
   I(gi,fp2)        <+ ddt(qcfp3) + ddt(minc * V(gi,fp2));
   I(gi,fp3)        <+ 0;
   I(gi,si)         <+ 0;
end
I(b,fp2)            <+ ddt(qbfp3) + ddt(minc * V(b,fp2));

idsfp2              = 0;
qgsfp2              = 0;
qgdfp2              = 0;
qcfp2               = 0;
qbfp2               = 0;
qsfp2               = 0;
if (lgfp2>=(minl)) begin
   idsfp2           = calc_iq(idsfp2,qgsfp2,qgdfp2,qcfp2,qbfp2,qsfp2,vgsfp2,
```

```
      vdsfp2,1,vcfp2,vbfp2,flagfp2s,dirfp2,tdut,tnomk,phit,w,lgfp2,cgfp2,cfp2s
      ,ccfp2,cbfp2,vtofp2,sfp2,delta1fp2,0.0,ndfp2,alphafp2,vx0fp2,mu0fp2,
      betafp2,mthetafp2,vthetafp2,vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type)
      ;
   I(fp2,fp1)       <+ idsfp2 + mygmin * V(fp2,fp1);
end else begin
   V(fp2,fp1)       <+ 0;
end
if (flagfp2==1) begin
   I(gi,fp1)        <+ ddt(qgsfp2) + ddt(minc * V(gi,fp1));
   I(gi,fp2)        <+ ddt(qgdfp2) + ddt(minc * V(gi,fp2));
   I(s,fp1)         <+ ddt(qcfp2) + ddt(minc * V(s,fp1));
   I(s,fp2)         <+ 0;
   I(gi,si)         <+ ddt(qsfp2) + ddt(minc * V(gi,si));
end else begin
   I(s,fp1)         <+ ddt(qgsfp2) + ddt(minc * V(s,fp1));
   I(s,fp2)         <+ ddt(qgdfp2) + ddt(minc * V(s,fp2));
   I(gi,fp1)        <+  ddt(qcfp2) + ddt(minc * V(gi,fp1));
   I(gi,fp2)        <+ 0;
   I(gi,si)         <+ 0;
end
I(b,fp1)            <+ ddt(qbfp2) + ddt(minc * V(b,fp1));


idsfp1              = 0;
qgsfp1              = 0;
qgdfp1              = 0;
qcfp1               = 0;
qbfp1               = 0;
qsfp1               = 0;
if (lgfp1>=(minl)) begin
   idsfp1           = calc_iq(idsfp1,qgsfp1,qgdfp1,qcfp1,qbfp1,qsfp1,vgsfp1,
      vdsfp1,1,vcfp1,vbfp1,flagfp1s,dirfp1,tdut,tnomk,phit,w,lgfp1,cgfp1,cfp1s
      ,ccfp1,cbfp1,vtofp1,sfp1,delta1fp1,0.0,ndfp1,alphafp1,vx0fp1,mu0fp1,
      betafp1,mthetafp1,vthetafp1,vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type)
      ;

   I(fp1,di)        <+ idsfp1 + mygmin * V(fp1,di);
end else begin
   V(fp1,di)        <+ 0;
end
if (flagfp1==1) begin
   I(gi,di)         <+ ddt(qgsfp1) + ddt(minc * V(gi,di));
   I(gi,fp1)        <+ ddt(qgdfp1) + ddt(minc * V(gi,fp1));
   I(s,di)          <+ ddt(qcfp1) + ddt(minc * V(s,di));
   I(s,fp1)         <+ 0;
   I(gi,si)         <+ ddt(qsfp1) + ddt(minc * V(gi,si));
end else begin
   I(s,di)          <+ ddt(qgsfp1) + ddt(minc * V(s,di));
   I(s,fp1)         <+ ddt(qgdfp1) + ddt(minc * V(s,fp1));
   I(gi,di)         <+ ddt(qcfp1) + ddt(minc * V(gi,di));
   I(gi,fp1)        <+ 0;
   I(gi,si)         <+ 0;
end
```

```
I(b,di)             <+ ddt(qbfp1) + ddt(minc * V(b,di));

idsrs               = 0;
if (flagres==0 && lgs>=(minl)) begin
idsrs               = calc_iq(idsrs,qgsrs,qgdrs,qcrs,qbrs,qsrs,vgsrs,vdsrs
   ,0,0,0,0,dirrs,tdut,tnomk,phit,w,lgs,cgrs,0,0,0,vtors,srs,delta1rs,0.0,ndrs
   ,alphars,vx0rs,mu0rs,betars,mthetars,vthetars,vtzeta,dibsat,epsilon,vzeta,
   lambda,ngf,type);
   I(si,src)        <+ idsrs + mygmin * V(si,src);
end else begin
   V(si,src)        <+ 0;
end

idsrd               = 0;
if (flagres==0 && lgd>=(minl)) begin
   idsrd               = calc_iq(idsrd,qgsrd,qgdrd,qcrd,qbrd,qsrd,vgsrd,vdsrd
      ,0,0,0,0,dirrd,tdut,tnomk,phit,w,lgd,cgrd,0,0,0,vtord,srd,delta1rd,0.0,
      ndrd,alphard,vx0rd,mu0rd,betard,mthetard,vthetard,vtzeta,dibsat,epsilon,
      vzeta,lambda,ngf,type);
   I(drc,fp4)       <+ idsrd + mygmin * V(drc,fp4);
end else begin
   V(drc,fp4)       <+ 0;
end

ids                 = calc_iq(ids,qgs,qgd,qc,qb,qs,vgsi,vdsi,0,0,0,0,dir,tdut,
   tnomk,phit,w,l,cg,0,0,0,vto,ss,delta1,delta2,nd,alpha,vx0,mu0,beta,mtheta,
   vtheta,vtzeta,dibsat,epsilon,vzeta,lambda,ngf,type);
I(di,si)            <+ ids + mygmin * V(di,si);
I(gi,si)            <+ ddt(qgs) + ddt(minc * V(gi,si));
I(gi,di)            <+ ddt(qgd) + ddt(minc * V(gi,di));

igs                 = 0;
igd                 = 0;
if (igmod == 1) begin
   igs              = calc_ig(igs,igssdio,igsrec,vgsi,phit,vgsats,alphags,fracs,
      pg_params,pbdgs,vbdgs,tdut,tnomk,w,ngf,ijs,kbdgates,vgsatqs,betarecs,
      irecs,pgsrecs,pg_param1,vjg);
   igd              = calc_ig(igd,igdsdio,igdrec,vgsi-vdsi,phit,vgsatd,alphagd,
      fracd,pg_paramd,pbdgd,vbdgd,tdut,tnomk,w,ngf,ijd,kbdgated,vgsatqd,
      betarecd,irecd,pgsrecd,pg_param1,vjg);
   I(gi,si)         <+ igs + mygmin * V(gi,si);
   I(gi,di)         <+ igd + mygmin * V(gi,di);
end

// resistors
if (rd < minr) begin
   V(d,drc)         <+ 0;
end else begin
  I(d,drc)          <+ V(d,drc) / rd;
end
if (rs < minr) begin
   V(src,s)         <+ 0;
end else begin
  I(src,s)          <+ V(src,s) / rs;
```

```
end
if (rg < minr) begin
  V(g,gi)           <+ 0;
end else begin
  I(g,gi)           <+  V(g,gi) / rg;
end

qofs                = w * ngf * cofsm * V(g,s);
I(g,s)              <+ ddt(qofs);

qofd                = w * ngf * cofdm * V(g,d);
I(g,d)              <+ ddt(qofd);

qofds               = w * ngf * cofdsm * V(d,s);
I(d,s)              <+ ddt(qofds);

qofdsub             = w * ngf * cofdsubm * V(d,b);
I(d,b)              <+ ddt(qofdsub);

qofssub             = w * ngf * cofssubm * V(s,b);
I(s,b)              <+ ddt(qofssub);

qofgsub             = w * ngf * cofgsubm * V(g,b);
I(g,b)              <+ ddt(qofgsub);

gm                  = 0;
svc                 = 0;
if (noisemod == 1) begin
  I(gi,si)          <+ white_noise(shs * `P_Q * abs(igs + 2.0 * (igssdio +
     igsrec)), "shot");
  I(gi,di)          <+ white_noise(shd * `P_Q * abs(igd + 2.0 * (igdsdio +
     igdrec)), "shot");

  I(di,si)          <+ flicker_noise(kf * ( w * ngf / l ) * pow( (ids / ( w *
     ngf )), af), ffe, "flicker");

  gm                =  ddx(ids , V(gi));
  svc               =  4.0 * `P_K * tdut * gm * ( qgs + qgd ) / ( w * ngf * l *
     type * cg );
  I(di,si)          <+ white_noise(svc, "channel thermal noise");

  if (lgfp1>=(minl)) begin
    I(fp1,di)       <+ white_noise(4.0 * `P_K * tdut / (rsh * lgfp1 / ( w * ngf
       )), "Rfp1");
  end
  if (lgfp2>=(minl)) begin
    I(fp2,fp1)      <+ white_noise(4.0 * `P_K * tdut / (rsh * lgfp2 / ( w * ngf
       )), "Rfp2");
  end
  if (lgfp3>=(minl)) begin
    I(fp3,fp2)      <+ white_noise(4.0 * `P_K * tdut / (rsh * lgfp3 / ( w * ngf
       )), "Rfp3");
  end
  if (lgfp4>=(minl)) begin
```

```
      I(fp4,fp3)      <+ white_noise(4.0 * `P_K * tdut / (rsh * lgfp4 / ( w * ngf
         )), "Rfp4");
    end
    if (rs >= minr) begin
      I(src,s)        <+ white_noise(4.0 * `P_K * tdut / rs, "Rcs");
    end
    if (rd >= minr) begin
      I(d,drc)        <+ white_noise(4.0 * `P_K * tdut / rd, "Rcd");
    end
  end

  // Self-heating
  if (rth >0) begin
     pdiss            = -( ids * V(di,si) + idsrd * V(drc,fp4) + idsrs * V(si,src)
         +  idsfp1 * V(fp1,di) + idsfp2 * V(fp2,fp1) + idsfp3 * V(fp3,fp2) +
        idsfp4 * V(fp4,fp3) + V(src,s) * V(src,s) / rs + V(drc,d) * V(drc,d) /
        rd);
     Pwr(dt)          <+ ddt( (cth + mycmin) * Temp(dt));
     Pwr(dt)          <+ pdiss;
     Pwr(dt)          <+ Temp(dt) / rth;
  end
  else
     Pwr(dt)          <+ Temp(dt) * 1e9;
  //else
  // Temp(dt)         <+  0.0;

  vgsext              = V(g,s);
  vgdext              = V(g,d);
  vdsext              = V(d,s);
  vsbext              = V(s,b);
  vdbext              = V(d,b);
  idext               = ids - igd;
  igext               = igs + igd;
  isext               = -ids - igs;
  ibext               = 0;

end

endmodule
```

Appendix B

Model parameter extraction

The extraction procedure of key model parameters of the MVSG-model is described in this appendix. The procedure pertains to the key transport parameters which impact the device-current characteristics along with the electrostatic parameters that are linked to the intrinsic-transistor and FP-regions. The flow of the basic parameter extraction procedure is described in Fig.B-1. As can be seen from the figure, the geometry parameters are often obtained from foundry data or obtained from SEM measurements of the devices to observe its cross-section geometry parameters. This is not the exhaustive list of parameters but the most significant ones. Most of the other parameters are either fitting parameters or constants for GaN-HEMTs. All parameters will be discussed in subsequent sections.

B.1 Device geometry and process parameters

Geometry and structural information are best provided by foundry. For the model, geometry parameters needed are: gate-length (L_g), source-access region (L_{gs}), drain-access region length (L_{gd}), device-width (W). In addition, parameters related to field plates such as field plate length, inter-layer dielectric thickness etc. might be necessary for future physical modeling. Other additional useful parameters required by the model are: low field mobility (μ_0), contact resistance (R_c) and sheet resistance (R_{sh}), and 2DEG density. If these are not provided, additional measurements might be

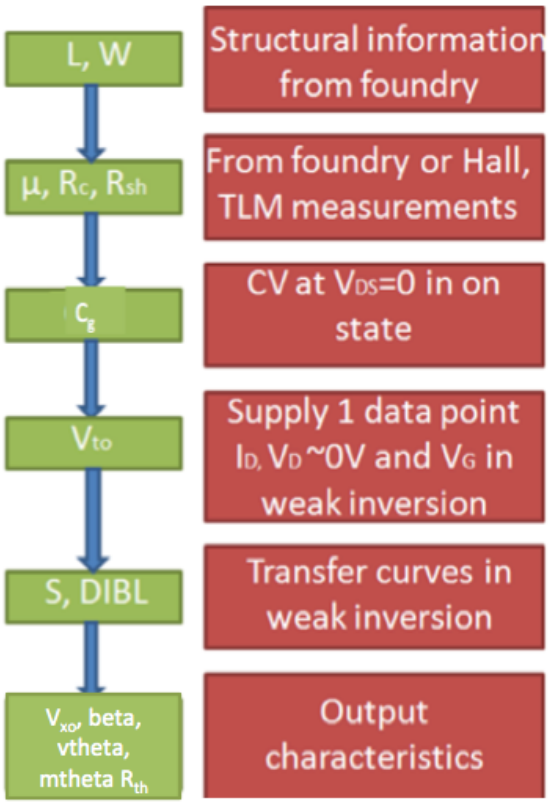

Figure B-1: Flowchart showing extraction flow of key parameters in the MVSG-model.

needed to extract them. μ_0 and R_{sh} extraction would require Hall measurements and special Hall-structures. R_c is extracted by measuring resistances of TLM structures of different lengths and extracting the offset at $L_g = 0$. Correct extraction of these parameters are also be verified from R_{on}-match in the output characteristics.

B.2 Extraction of C_g

C_g is an important model parameter in the MVSG-model and its accurate extraction is essential for correct device-modeling. C_g is extracted from CV measurements rather than from analytical calculation. Accurate analytical calculations if done must also include quantum correction as charge centroid in 2DEG is shifted away from the interface. This needs dedicated calculations/simulations, which from a compact modeling perspective might not be critical as long as we directly measure the capacitance. To get C_g, two terminal CV (with $V_{DS} = 0$) of devices with different gate-lengths but

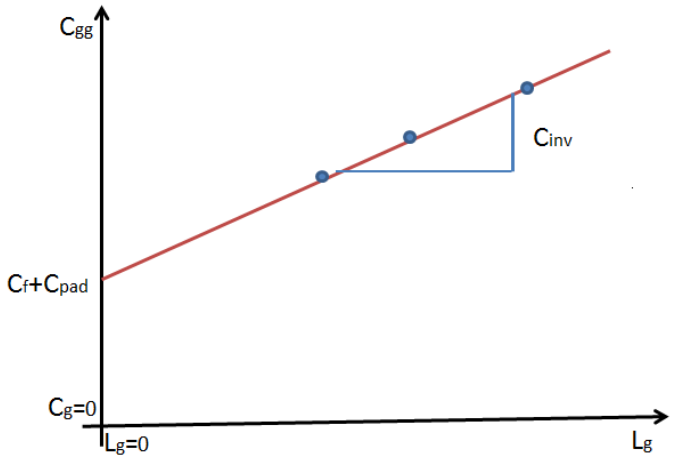

Figure B-2: Extraction of areal-gate capacitance from CV-measurements of different length devices. Off-state fringing capacitances are obtained from these measurements along with the C_g.

identical widths and access-region lengths are measured. The gate-to-channel capacitance in strong accumulation scales as a function of L_g. From the slope we get the value of C_g (areal gate capacitance) and the intercept gives the parasitic capacitance. Parasitic capacitance includes outer fringing capacitance (C_{of}) and pad parasitics. To remove the pad-parasitic, we need CVs of open test structures.

B.3 Extraction of other capacitance parameters

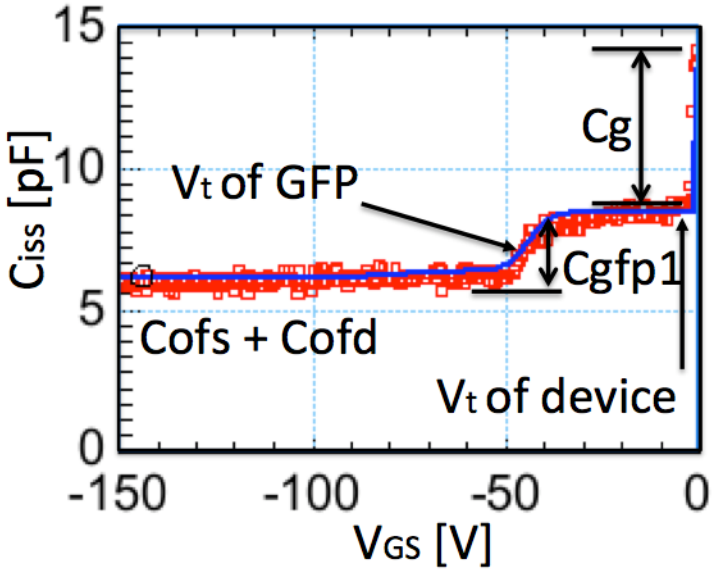

Figure B-3: Illustration of the extraction of gate-field plate parameters of devices from C_{iss} vs. V_G measurements.

Gate-capacitance measurements vs. V_G at $V_{DS} = 0\ V$ yields the areal-gate capacitances and $V_T s$ of all gate-connected field plates. This is shown in Fig.B-3 where the step in the CV-curve that is seen at $V_G = V_{to}$ of the FET is normalized to the width and gate-length (which are known) gives **cg** the areal gate-capacitance. Similarly the transition at $V_G = -50\ V$ in the figure is due to the depletion of the GFP-transistor occurring at its V_T (v_{tofp1}) and the areal gate-capacitance (c_{gfp1}) is the step in the CV-curve at that V_G. In addition, the electrostatic parameters such as sub-threshold slope **sfp1** are obtained from the slope of the transition. The off-state capacitance obtained from calibrated CV- measurements yields the total metal capacitances associated with the gate terminal (**cofsm**+**cofdm**). Individual components are then obtained from C_{gs} and C_{gd} measurements using bias-Ts to apply the DC bias.

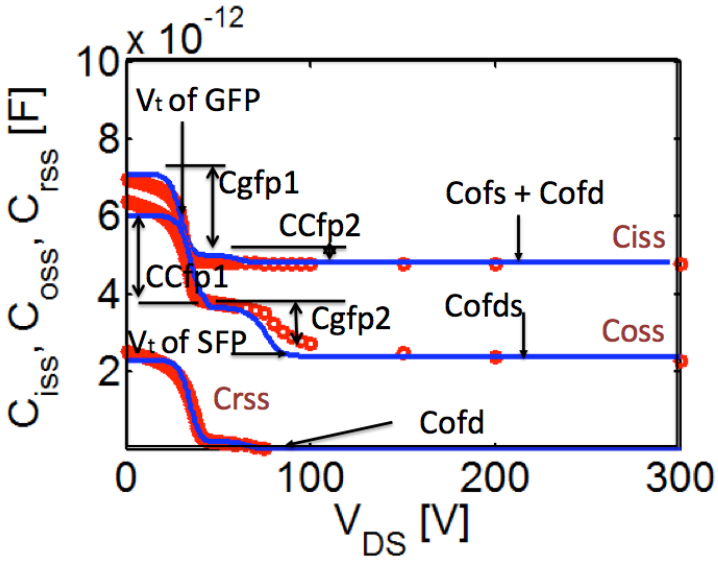

Figure B-4: Illustration of the extraction of field-plate parameters of devices from capacitances vs. drain voltage measurements.

Input, output and reverse transfer capacitance measurements vs. V_D in the off-state yields the areal-gate capacitances, cross-coupled capacitances and $V_T s$ of all field-plate transistors. Fig.B-4 shows representative C_{iss}, C_{oss} and C_{rss} plots which shows transitions at $V_D = V_T s$ of different field-plates which are due to depletion of these transistors. From C_{iss} (or C_{rss}) the areal-gate capacitances of GFP transistors (**cgfp1**) (can be cross-checked from the previous plot) and cross-coupled capacitances of SFP transistors (**ccfp2**) are obtained. Metal-to-metal fringing capacitances be-

tween gate- and other terminals (**cofs, cofd, cofgsub**) of the device are extracted as well. From C_{oss} plot, the capacitances associated with the source terminal are obtained, which includes the areal-gate capacitances of SFP transistors (**cgfp2**) and cross-coupled capacitances of GFP transistors (**ccfp1**) along with the metal capacitances associated with source-drain terminals (**cofds**).

B.4 Extraction of V_{to}, SS and DIBL

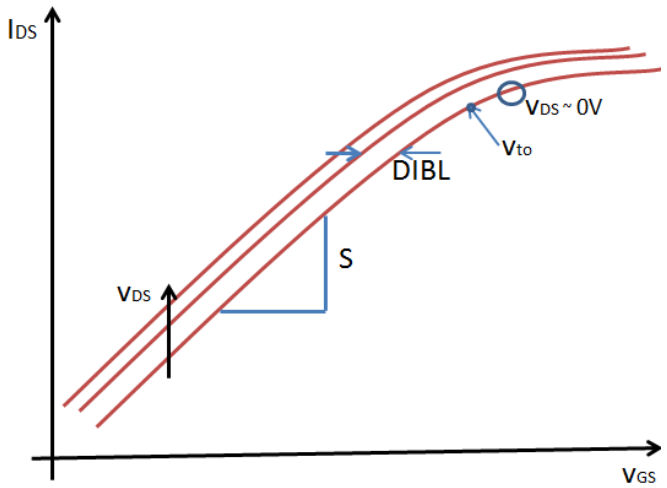

Figure B-5: Illustration of the extraction of v_{to}, SS and $DIBL$ from transfer curves.

Threshold voltage (v_{t0}) computation requires knowledge of the piezoelectric charges at the interface, heterostructure composition and thickness. Again the model is simplistic in the sense that v_{t0} needed for the model are extracted from the device data. The requirement is one data point (V_G, I_D, V_D) in weak accumulation (just beyond strong-to-weak accumulation transition) at low V_D ($\approx 0\ V$ where DIBL has negligible impact). Alternately v_{to} can be approximated as V_G at the same (V_G, I_D, V_D) point on the transfer curve. Sub threshold slope (SS) is obtained from the slope of the transfer curve on log scale in weak accumulation regime. Low V_D is preferred to avoid shift of SS due to modest punchthrough in the device. The parameter extracted must make sense for the L_g of the device. DIBL is extracted from the lateral shift of I_D (due to shift of V_t) as V_D is increased in the transfer curves in weak-accumulation. DIBL is multiplied by intrinsic drain voltage (V_{Di}) in the expression for the threshold

voltage in the model. It is extracted from the weak accumulation regime as shown in Fig.B-5.

B.5 Extraction of $v_{sat,0}$, β and θ_v, θ_μ and R_{th}

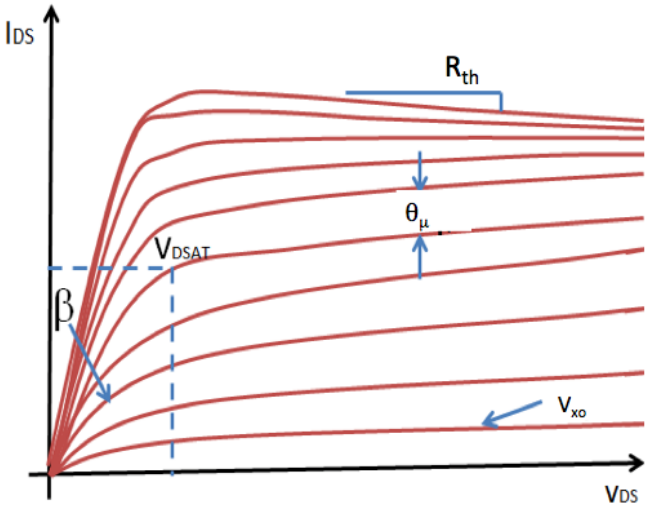

Figure B-6: Illustration of extraction $v_{sat,0}$, β and θ_v, θ_μ, R_{th} and η_v from the output curves.

$v_{sat,0}$, β and θ_v, θ_μ and R_{th} are extracted from the output characteristics. $v_{sat,0}$ are fitted to get accurate match with the saturation-current level. $v_{sat,0}$ extracted must lie between the bracket of peak electron velocity (2.5×10^7 cm/s) and saturation velocity (1.3×10^7 cm/s) depending on the gate-length. The transition from linear-to-saturation current in the output characteristics is governed by F_{sat} which has a parameter β. β should ideally lie between 1.5-3 for these type of HEMTs depending on saturation. η_v is the thermal coefficient affecting velocity. The parameter is extracted from the slope of the output curves in saturation at large V_G where self-heating is dominant. η_v together with the thermal resistance (R_{th}) are directly responsible for the negative slope of the output curves and are extracted from fitting. θ_v, and θ_μ are also fitting parameters which affect V_{DSAT}. They are extracted from V_{DSAT} at lower V_{GS} when self-heating has not yet kicked in. Thus by fitting to get correct linear-to-saturation transition voltages at larger V_{GS} we get values of θ_v and θ_μ. R_{th} of the thermal network is also obtained in the high bias-region where self-heating is

predominant. The R_{th} characterization through TCAD and evaluation of thermal coefficients through multi-temperature measurements can also be done.

B.6 Extraction of gate-leakage parameters

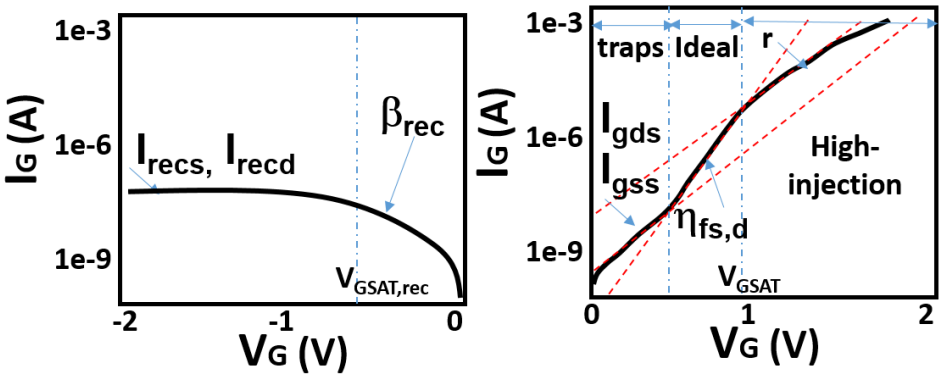

Figure B-7: Illustration of extraction forward- and reverse-mode Schottky-gate current

The gate-current parameter sets can be extracted from the gate-current data as shown in Fig. B-7 where the reverse-mode characteristics ($V_G < 0$) give the parameters: I_{recs}, I_{recd}, $V_{GSAT,rec}$ and β_{rec} and the forward-mode characteristics give the forward-mode parameters: I_{gss}, I_{gds}, V_{GSAT} and r. The saturation parameters for the reverse-leakage current such as β_{rec} and $V_{GSAT,rec}$ have similar extraction-procedure as the F_{sat} function-parameters in the MVS-model. The high-injection parameters r and V_{GSAT} can be extracted from the high-V_G regime in the forward-mode characteristics as shown. These are the key parameters for the gate-current model relevant for room-temperature measurement fits. The temperature coefficients such as ϕ_B and ϵ_G are extracted from saturation-current measurements at different temperatures.

B.7 Extraction of RF-parasitic-network elements

The extraction of RF-parasitic elements of the device can be done in a methodical open-short de-embedding method or can be extracted as a fitting approach to S-

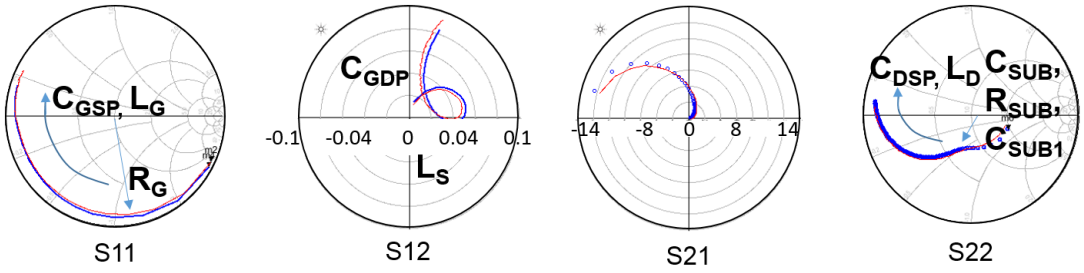

Figure B-8: Illustration of extraction forward- and reverse-mode Schottky-gate current

parameter data as explained in Fig.B-8. The S11 plot can be used to get the values of R_G, L_G and C_{GSP} while the reverse-gain determined primarily by C_{GDP}, L_S can be extracted from S12. The substrate-loss network-elements can be obtained from S22 as shown at high-frequencies. The parameters can be fine-tuned over a few bias-points to increase the model accuracy over a span of bias-conditions. Since the bias-dependent device-quantities are already modeled and benchmarked against device IVs and CVs, the constant RF-parasitics extracted against a few bias-points is sufficient to capture teh device small- and large-signal behavior over the entire bias and frequency-range with reasonable accuracy.

The parameter extraction procedure highlighted in this appendix is relevant for RF- and HV-applications and covers most of the important device-behavioral nuances. The model parameter extraction for a few secondary effects such as charge-trapping and phase-noise effects are highlighted in the main body of the thesis and are not repeated here. Moreover the charge-trapping mechanisms responsible for both the above two effects are technology dependent and it is difficult to express universal physical models for explaining the phenomena and the empirical model parameters are to be extracted from post-measurement data fits. The extraction of the model parameters is also provided in the model-manual in Nanohub NEEDS website [82] [83].

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