Development and Analysis of High-Frequency, High-Density PFC Power Conversion

by

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Abstract

This thesis explores the design of power converters that deliver isolated low-voltage dc output (~24V) and operate from "universal" ac input voltage (85 – 264 Vac RMS).

It is important that these converters have good overall efficiency (~90-95%), and good ac line power factor (>0.9, and ideally >0.95) to better utilize the available energy. This thesis looks into achieving high efficiency, high power factor, low voltage stresses, and smaller component sizes by utilizing high frequency operation. The research focuses on component and subsystem evaluation, development and testing as a part of many-person research in this space.

The thesis presents a literature based study on current PFC circuit designs and tradeoffs. It also introduces a specific PFC architecture, which provides a low dc output voltage drawing energy from a wide range ac input voltage while maintaining a high power factor. The architecture includes two stages:

The first is a "Power Factor Correction" (PFC) which functions as an input stage drawing energy from a wide-range input current. It uses a resonant transition inverted (RTI) buck converter topology to step down the voltage from line voltage (85 – 264 Vac RMS) to around 72V. Furthermore, the inductor for the RTI buck is analyzed.

The middle stage is an energy buffer to provide the required energy level for twice line frequency energy buffering and $20ms$ of energy hold up. The capacitor requirements, analysis, and selection are explored and developed.

The second stage is a transformation and regulation stage which also provides electrical isolation between the ac input and dc output. The thesis also explores the use of available conventional high-density telecom "brick" converters as a second stage.

In conclusion, the project explores the possibility of using a buck configuration for the PFC, sacrificing the ability to use high energy density 400V capacitors while gaining the advantage of using the high-density telecom brick converters and different output voltage options.

Thesis Supervisor: David J. Perreault
Professor of Electrical Engineering

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I would not have been able to accomplish this without the unlimited support of my family and friends. It is to them that this thesis is dedicated. The unconditional love and encouragement of my parents Saeed AlShehab and Zahra AlJuffairi, and my sisters Ghadeer AlShehab and Mariam AlShehab have always been a driving force for me. My brother Mohamed AlShehab has always been my best friend and source of comfort and guidance. And to my friends at MIT that made this a great and fun place to be to you all, I am truly grateful and "Thank you!"

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Chapter 1

Introduction

1.1. Background and Motivations

We are interested in power supplies which supply low dc voltage loads by drawing energy from the single-phase ac grid. These supplies have converters that deliver isolated low-voltage dc output (~12V or ~24V) and operate from "universal" ac input voltage (85 – 264 Vac RMS).

Furthermore, it is important that these converters have good overall efficiency (~90-95%), and good ac line power factor (>0.9, and ideally >0.95) to better utilize the available energy. This proposal is concerned with achieving high efficiency, high power factor, low voltage stresses, and smaller component sizes by utilizing high frequency operation. The research focuses on component and subsystem evaluation, development and testing as a part of many-person research in this space.

Such converters usually operate at relatively low switching frequencies – around 200kHz or below- and have low power densities – around 10 $\frac{W}{inch^3}$ or below. The relatively low frequency operation results in designs which require physically large magnetic components. The size issue could be addressed by increasing the switching frequency which would allow for smaller and cheaper magnetic components. Evidently, high frequency circuit architectures coupled with advances in semiconductor devices could have a big impact on the size and cost of grid-interfaced conversion from high-to-low voltage supplies.

Hence, there is an evident need for new power electronics technologies that can meet the requirements of practical applications at far lower size and cost than is presently achievable.

When operating at high frequency one of the main concerns is switching losses. Low loss circuit designs and control methods made it possible to achieve high switching frequencies in the range of 3 to 30 MHz with good efficiency ([11], Fig. 1.2).

1.2. Thesis Objectives and Contributions

This thesis will contribute to the design of a full PFC system of the type in Fig 1.1, shown below. It will focus on aspects of the high-frequency PFC portion, and will also explore selection and testing of commercial telecom converters for use in the power combining / isolation / transformation stage. In this effort, the design and testing of the high-frequency buck power stage will be the central focus, including design of miniaturized inductors for the converter and optimized selection of electrolytic capacitors to provide twice-line-frequency energy buffering and holdup energy. It will also include an experimental study of available high-density high efficiency telecom brick converters and how suitable they are to be used as the second stage converters.

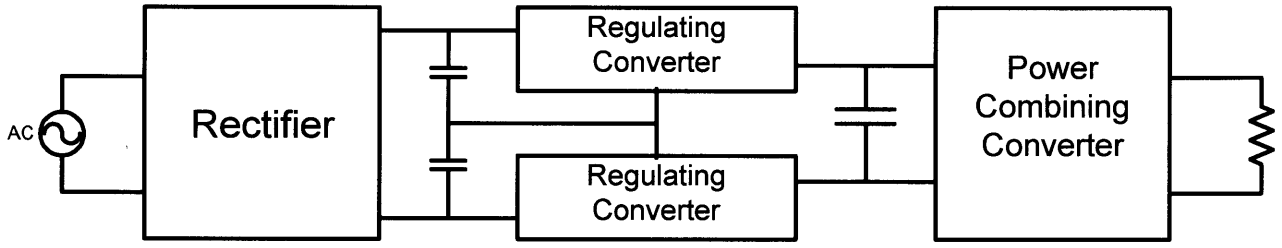

Fig 1.1: The full PFC grid interface power conversion system architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining

The thesis has three primary objectives in the design of a prototype high-frequency PFC system. The first objective of this thesis is to figure out the smallest capacitor that could be used for twice line frequency energy buffering as well as figure out the optimal operating point for utilizing this capacitor. The operating point includes choosing the voltage at which energy is stored, the capacitance value and the allowable ripple. The second objective is to realize the smallest inductor that could be used for the resonant transition buck converter in the high-frequency PFC stage. The third objective is to realize the possibility of using high-density and

high efficiency telecom brick DC/DC for the second isolation/transformation/configuration stage.

The thesis makes several contributions. The first contribution is a study, comparison and experimental evaluation of capacitors for twice-line frequency energy buffering and holdup in our proposed PFC system. Such capacitors are important because they represent a substantial fraction of converter volume. A second contribution is a study, comparison and experimental evaluation of inductors for the resonant-transition inverted buck PFC stage. This will include evaluation of various magnetic materials and inductor designs and their comparison in high-frequency power stages. This is important because miniaturization of the magnetics is a key goal. Moreover, the thesis includes development of a test stand for evaluating designs of the high-frequency PFC stage (resonant-transition inverted buck design), including design of a high-power 600 W load to absorb energy from the converter during testing and development of appropriate instrumentation. The test stand is used for testing and refinement of resonant-transition inverted buck converter designs for the high-frequency PFC stage. These contributions are valuable towards the development of a full PFC converter system based on the proposed architecture.

1.3. Thesis Organization

The thesis is divided in to six chapters, including this introductory chapter. Chapter 2 introduces the concepts and definitions of power factor correction. It further presents an overview of current PFC designs and tradeoffs and introduces the architecture of interest to this project.

Chapter 3 presents the requirements and design analysis for choosing a capacitor for twice line frequency energy buffering and holdup (e.g., for operation during line interruptions). The first part of the chapter analyzes the capacitors energy storing capability and the energy buffering capability. It looks at the energy density of the capacitor when constrained by the ripple allowed on the second stage, the RMS current capability, and the holdup energy requirement. The chapter concludes with capacitor selection and testing.

Chapter 4 presents the inductor design for a resonant transition buck converter. The first part of the chapter analysis the inductance requirement and the inductor realization in gapped E

and planar geometries. It inspects the magnetic flux density capabilities of some select ferrite materials and develops a method to calculate inductor loss, including both core and winding loss, and temperature rise. The chapter also shows the experimental results of some inductors that could be used for our application and architecture of interest.

Chapter 5 investigates the possibility of using high-density, high-efficiency telecom brick converters for the second isolation/transformation/combination stage in the topology of interest. The chapter looks through the operation of available converters then presents experimental results of select converters that could be used in the architecture of interest

Chapter 6 presents some of the test bench circuits built to test aspects of the proposed design. The first test bench is a 600W zener bank load used to test the resonant transition buck converter. The second test bench is used to test the holdup time capability of the buffer capacitor.

Chapter 2

Power Factor Correction Study

2.1 Introduction

This section introduces the concepts and definitions concerned with power factor correction circuits. It synthesizes a summary of IEC 1000-3-2 (and the European EN61000-3-2) standards and US Federal recommendations and ENERGY STAR product specifications. It further presents the results of a literature based study of current PFC circuit designs and tradeoffs. After looking at the concepts and study results, the chapter introduces the design approach explored in this thesis.

2.2 Background

2.2.1 PFC: Concepts and definitions

a. Power Factor (k_p) and Total Harmonic Distortion (THD) Review:

An elementary definition of power factor correction is the ratio between real power (expressed in Watts) and apparent power (expressed in VA) [19].

$$Power\ Factor = \frac{Real\ Power\ (Watts)}{Apparent\ Power\ (Volt.Amp)} \quad (2.1)$$

Real power is the average of the instantaneous product of current and voltage over one cycle. In contrast, apparent power is the product of the rms values of current and voltage.

According to the definition, for purely sinusoidal waveforms, when the voltage and current waveforms are in phase, the power factor is unity. A unity power factor indicates that the load behaves resistively. When the sinusoidal waveforms are out of phase, the power factor is the

cosine of the phase angle. Depending on the sign of the phase shift, the load is said to behave inductively or capacitively. This can be derived by calculating real power (P) through the following:

Using a general form of a sinusoidal input:

$$v_s(t) = V_s \sin(\omega t) \quad (2.2) \qquad i_s(t) = I_s \sin(\omega t + \theta) \quad (2.3)$$

Where θ is the phase shift in the current waveform. And we can find the average power through:

$$P = < p(t) > = \frac{1}{2\pi}\int_0^{2\pi} v_s i_s d(wt) = \frac{V_s I_s}{2} cos\theta = V_{srms} I_{srms} cos\theta \quad (2.4)$$

Where, the angle θ is called the power factor angle. A leading power factor with $\theta > 0$ (current leading voltage) indicates a capacitive load, and a lagging power factor with $\theta < 0$ indicates an inductive load.

The previous expression is only correct when both current and voltage are sinusoidal waveforms and doesn't take into consideration distortions of the waveforms and could lead to incorrect conclusions about the power factor. For instance, when we have a sinusoidal voltage waveform in phase with a distorted current waveform, the above definition would give a power factor of 1. Since only the fundamental component produces real power and the other harmonics contribute to the apparent power, the actual power factor in this case would be less than 1.

A more complete derivation takes into consideration the distortion of waveforms. Power factor $\boldsymbol{k_p}$ can be expressed as a product of two terms, one represents the displacement effect (k_θ) and the other represents the distortion effect (k_d):

$$k_p = \frac{< p >}{V_{srms} I_{srms}} = k_\theta k_d \quad (2.5)$$

We define V_{srms} is the root mean square of the sinusoidal voltage waveform, I_{srms} is the root mean square of the current waveform, and I_{1rms} is the root mean square of the fundamental component of the current waveform. In this case the current is the distorted waveform. And

therefore $k_\theta = cos\theta, and\ k_d = \frac{I_{1rms}}{I_{srms}}$, where k_d and k_θ are both factors having a magnitude less than or equal to one, and both must be close to one for high power factor.

From the previous discussion, it is clear that for sinusoidal voltages (the case considered here), low harmonic content is necessary for high power factor. This brings to the surface the concept of total harmonic distortion (THD). THD is defined as the quadratic sum of the unwanted high order harmonics over the fundamental ([19], chapter 3). It can be calculated as follows:

$$THD = \sqrt{\frac{I^2{}_{srms} - I^2{}_{1rms}}{I^2{}_{1rms}}} \quad (2.6)$$

Furthermore, we can derive a relation between the distortion factor and THD ([19], chapter 3):

$$k_d = \sqrt{\frac{1}{1 + THD^2}} \quad (2.7)$$

More importantly, power factor measures how well electrical energy is transferred from a source -in terms of not introducing excessive joule heating in the source- and is expressed as a number between 0 and 1. THD needs to be zero for the power factor to be 1. A high power factor requires BOTH a distortion factor k_d near one (or a low THD) and a displacement factor k_θ near one (or low phase shift between voltage and fundamental current). High power factor in turn means that electrical power is being used effectively, whereas low power factor indicates poor utilization of power.

b. Summary of standards and recommendations:

1) IEC 1000-3-2 (and EN61000-3-2) standards:

The IEC 1000-3-2 (and the European EN61000-3-2) standards define ac power source requirements and limits of harmonic emissions [14]. Compliance to these standards ensures that

the equipment will not generate (line frequency) harmonic currents which cause unacceptable degradation to the grid and other nearby equipment.

First the equipment must be categorized in one of four defined classes. Class A includes balanced three-phase equipment, Class B includes hand-held portable electric tools, Class C includes lighting equipment including dimming devices, and Class D includes equipment which has an input current with a special wave shape and an active input power $\leq 600\ W$(e.g. SMPS: switch-mode power supplies, an electronic power supply which has a switching regulator for efficient electrical power conversion).

Each class has a different set of requirements in terms of harmonic limits. Tables 2.1 and 2.2 below list the maximum permissible harmonic currents. The limits are broken down separately into requirements on odd line frequency harmonics and even line frequency harmonics.

Harmonic order (n)	Class A (A)	Class B (A)	Class D (A)	Class C (% of fundamental frequency input current)
3	2.30	3.45	2.30	30 *circuit power factor
5	1.14	1.71	1.14	10
7	0.77	1.155	0.77	7
9	0.40	0.60	0.40	5
11	0.33	0.495	0.33	3
13	0.21	0.315	0.21	3
15<=n<=39	2.25/n	3.375/n	2.25/n	3

Table 2.1: Odd harmonic requirements for different classes

Harmonic order (n)	Class A (A)	Class B (A)	Class C (% of fundamental frequency input current)
2	1.08	1.62	2
4	0.43	0.645	-
6	0.30	0.45	-
8<=n<=40	1.84/n	2.76/n	-

Table 2.2: Even harmonic requirements for different classes

Generally, harmonic currents less than 0.6% of the input current are disregarded during testing. Also, if the harmonics 20 through 40 decrease monotonically, only harmonic 2 through 19 need to be inspected. For details about the test setup, please refer to appendix B.

2) ENERGY STAR product specifications:

ENERGY STAR is an international standard for energy efficient consumer products. It was originally initiated in the United States back in 1992 by the Department of Energy and the Environmental Protection Agency. Its standards are adopted by many countries including the European Union. Products carrying the ENERGY STAR label are more efficient and use 20-30% less energy than required by federal standards.

To be eligible for ENERGY STAR qualification, certain specifications must be met within the criteria of Active Mode, No-load Mode, and power factor. Tables 2.3 and 2.4 below outline minimum average efficiency criteria for ac-ac and ac-dc external power supplies for Active Mode and No-Load Mode which varies which varies based on the model's nameplate output power P_{no}, also known as the rated or nominal output power ([15], Table 2.1).

Nameplate output power (P_{no}) in Watts	Minimum average efficiency (expressed as a decimal)
0 to ≤1 watt	≥ 0.48*P_{no} + 0.14
> 1 to ≤ 49 watts	≥ [0.626*ln(P_{no})] + 0.622
> 49 watts	≥ 0.87

Table 2.3: Energy Efficiency Criteria for Active Mode

Nameplate output power (P_{no}) in Watts	Maximum Power in No-Load	
	Ac-Ac EPS	Ac-Dc EPS
0 to < 50 watts	≤ 0.5 watts	≤ 0.3 watts
≥ 50 to ≤ 250 watts	≤ 0.5 watts	≤ 0.5 watts

Table 2.4: Energy Efficiency Criteria for No-Load

Furthermore, beyond the Active Mode efficiency requirements, power supplies with greater than or equal to 100 watts input power must have a true power factor of 0.9 or greater at 100% of rated load when tested at 115 V @ 60Hz. Recently, several stake holders highlighted that with half the current, the conduction losses would drop to one quarter of their value. Hence, they argue that power factor losses are less important at 230 V compared to 115 V. However, this argument may be viewed as specious, as equipment impedance will typically be correspondingly higher in higher-voltage systems.

And, since a two-stage PFC is more resource intensive design and may reduce the efficiency in the Active Mode, this less strict requirement could eliminate the single PFC architecture reducing cost and allowing for better efficiency. For these reasons, *the EPA revised the power factor requirement to apply only at 115V and not at 230 V.*

Furthermore, ENERGY STAR has different specifications for different products. For instance, the requirements for LED lighting includes: output consistency over time, color quality, flicker, power consumption in the off state, etc. Products must not draw any power in the off state. Power factor must be at least 0.7 and 0.9 for residential and commercial respectively. The light output and efficacy requirement is listed in table 2.5 below [16].

Light Output	150 lumens	50 lumens	100 lumens	300 lumens
Efficacy	24 lm/W	20 lm/W	25 lm/W	35 lm/W

Table 2.5: Light output and efficacy requirements

2.2.2. PFC: A literature based study

Harmonics introduced by power converters cause problems like: heating, noise, current and voltage distortions, reduction in efficiency, etc. These harmonics can be harmful to both the grid and the utility. These faults and the new and stricter mandatory standards in the US and many EU countries (by IEC 1000-3-2 and EN61000-3-2) brought power factor under examination.

For these reasons, the notion of power factor correction has been deemed very important in recent years. While unity power factor is the Holy Grail, it is neither a requirement nor a necessity for most applications. This allows for numerous topologies, control modes, and

technological advances to be proposed that provide acceptable performance and good but not unity power factor. This study introduces some designs cost and quality tradeoffs then explores some of the known power factor correction circuits and focuses on high frequency applications.

1) Overview: Cost vs. Quality:

Generally, based on cost and quality of current waveform, we can consider 3 types of solutions. First, a high cost solution which generates a high quality sinusoidal waveform. Good examples of this class of solutions are the multi-level converters ([7], Fig. 2.1). Second, intermediate cost solutions which have non-unity power factor but still satisfies the regulation. Solutions of this type include so-called single stage converters in which there is not a separate power conversion step for achieving high power factor. Third, non-regulated solutions which are low cost and simple. These could comprise a diode bridge and a capacitor filter for an input stage ([7], Fig. 1.2).

2) Classical PFC circuit and some improvements:

The traditional power factor correction circuit architecture can be seen in Fig. 2.1. It comprises a line-frequency rectifier as an ac input stage (can be implemented with a diode bridge), a power factor correction pre-regulator (PFCP) – a high-frequency dc-dc converter which draws a shaped current waveform for high power factor and stores twice-line-frequency energy on its output capacitor, and a dc/dc converter. It also includes several control loops within the second and third stages.

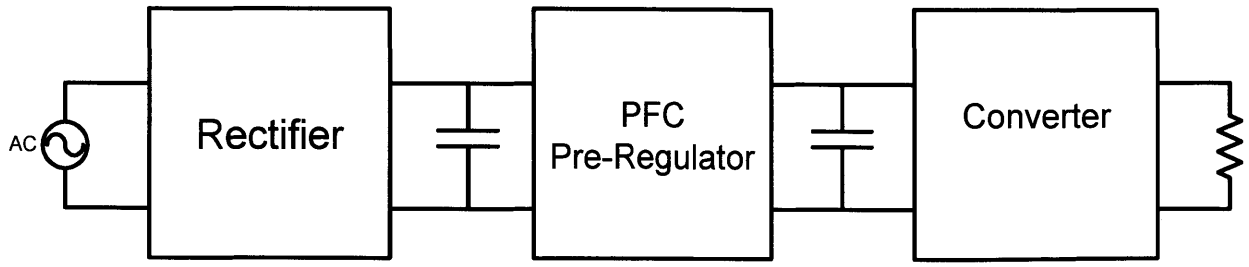

Fig 2.1: Illustrates the classical two stage PFC circuit topology

The following is a list of some solutions which deviate from the traditional two stage scheme for shaping and therefore increasing the quality of line current.

One common strategy is to utilize a single-stage converter via a topology that maintains quasi-sinusoidal line current such as through working in discontinuous conduction mode (DCM). Converters such as: buck-boost, Cuk, SEPIC, flyback, and Zeta, operated in DCM behave in a voltage follower manner and allow for the elimination of inner current loops [2]-[4]. This can be a good approach for medium and low power applications (< 1 kW), but due to high RMS currents in DCM causing high conduction losses, the average losses tend to make this less attractive for very high power converters. It can also be an attractive approach because of the absence of losses due to the reverse recovery of the boost diode.

Power processing can be used as an indicator of the expected efficiency of the topology; processing less energy (or processing the energy fewer times) generally results in higher system efficiency. In the traditional two-stage approach, the entire output power is being processed twice. Less processed energy can be achieved by using a bi-directional shunt connection at the PFC output, as illustrated in Fig. 2.2. While this still requires two high frequency stages, the output power is processed less (due to less number of stages in the path to the output). The shunt connection at the PFC output absorbs the excess power –twice line-frequency energy- and stores it and later releases it to the load [6].

Furthermore, using parallel processing decreases the number of times, as illustrated in Fig. 2.3, the output power is processed [7]. In this solution there are two paths for the power, one of which leads directly to the load. The issue in this scheme is that it complicates the power stage. Moreover, one can reposition the power blocks, as illustrated in Fig. 2.4, to allow for the processing of only half the waveform while delivering the other half to the load. This result in the output power being processed only 1.50 times, since 0.5 of the output power is processed only once [8]. However, this scheme restricts the connection of the converter limiting its application use.

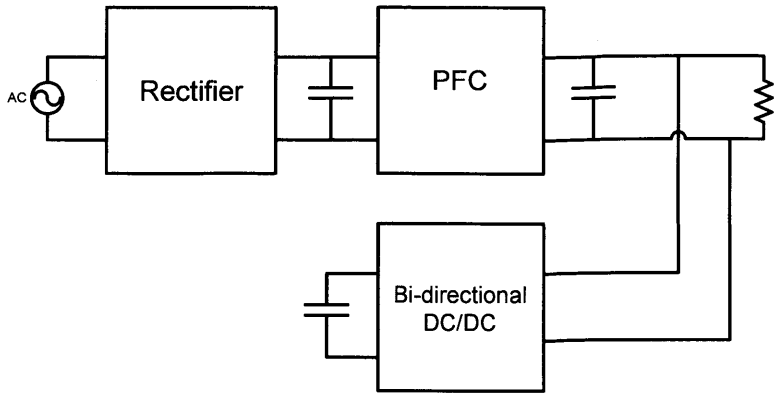

Fig 2.2: Bi-directional shunt connection at the PFP output

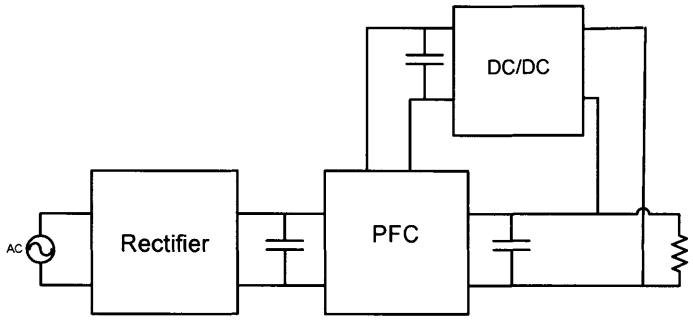

Fig 2.3: Parallel power processing topology

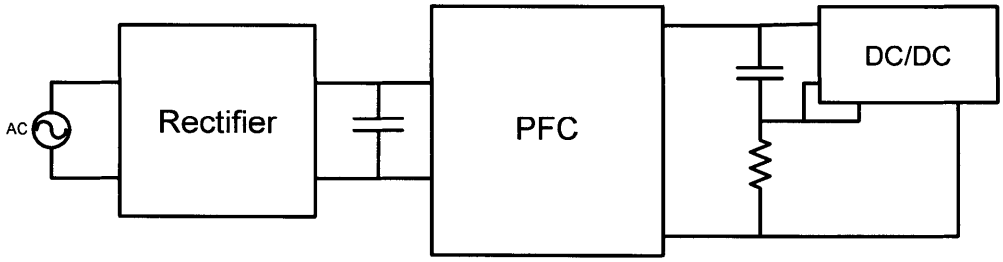

Fig 2.4: Block repositioning topology

Efficiency of power processing is as important as limiting power processing in improving the overall efficiency. Efficiency of power processing can be achieved a number of ways. Soft switching, such as realized using auxiliary networks, shown in Fig 2.5, can be used to decrease switching losses, which increases efficiency. For instance, a boost converter has high output voltage and high losses due to the diodes reverse recovery [9]. A good solution would be to use the auxiliary circuits in a zero-voltage transition converter (e.g., a "baby boost" converter applied in conjunction with a main boost power stage to provide ZVT operation). The down side is the

complexity increase and size increase of the control stage. Second, resonant converters have soft switching capability which also reduces switching losses through zero voltage switching (ZVS) [10].

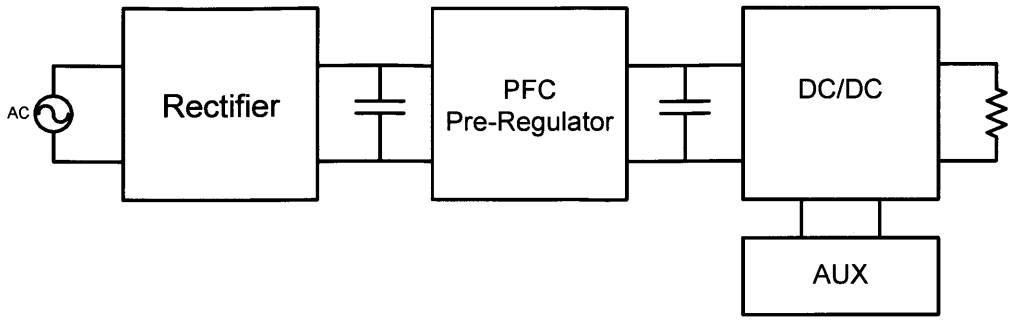

Fig 2.5: Using auxiliary networks to decrease switching losses

Furthermore, we can use passive filters to obtain nearly sinusoidal current. This solution does not involve using two converters (PFC and dc-dc). Although reactive elements are large and heavy, it is possible to use only reactive elements without PFCs to produce a nearly sinusoidal current without introducing electromagnetic Interference (EMI), and lowering reliability [5]. While this approach can't be used for universal input voltages (85-264 Vac), it still allows for lowering the number of stages.

Ultimately, the traditional two stage option is often the most straightforward scheme to obtain high power factor line current for universal line voltage operation. And, passive alterations are usually adequate enough for low power applications. Although better energy management (less or efficient energy processing) results in more efficiency, it usually adds more complexity and cost. Hence, it is only recommended in applications where high efficiency is important. To gain a worthwhile improvement and overcome the disadvantages of the 2 stage traditional PFC converter, new domains need to be explored.

3) High frequency Architecture:

One major disadvantage in ac-dc converters which use the grid ac input voltage (85-264 Vac RMS) to supply a low-voltage dc output (e.g., 24 V) is the size of its magnetic components, and consequent system cost. The reason is that such converters operate at low frequencies (up to

a few hundred kHz), and therefore require large magnetic components for energy storage and filtering. This has fueled the need for new power electronic systems which could achieve the required functionality at lower cost and size. The solution can be found in high frequency operation. The rest of the study describes major concepts on how high frequency operation can be achieved and gets into some details about a specific design.

Reference [11] describes a new power conversion scheme which realizes miniature ac-dc converters operating at high frequencies (above 3 MHz) which provides high efficiency, high power density, and high power factor for ac-dc applications. As depicted in Fig 2.6 the design includes a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter.

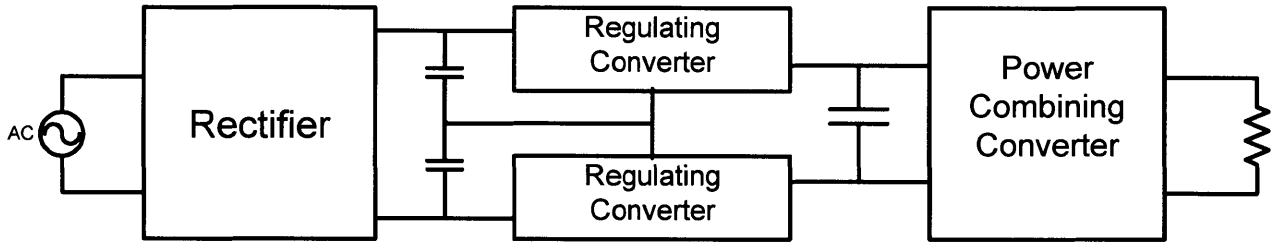

Fig 2.6: The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter

The line-frequency rectifier is controlled by the regulating converter. It interfaces with the grid and draws current during a portion of the cycle. The stack of capacitors (which are chosen to be relatively small) provides a wide range of capacitor voltages to accommodate and follow the variability in line voltage. It also buffers and shapes the waveforms eliminating most of the twice-line frequency energy. This increases the power factor and reduces the need for buffering at the output.

The regulating converters operate at a much lower voltage than the line voltage which allows for higher frequency switching than the line voltage. Many converter topologies can be used to implement the regulating converters. A good topology which allows high frequency operation, low device voltage stress, small component size, and good control capability is the resonant-transition discontinuous-mode inverted buck converter [12].

The power-combining converter draws energy from the regulating converters and delivers the combined energy to the output. Furthermore it can provide isolation, voltage

transformation, and buffering if needed. This converter works from low, narrow range input and doesn't need regulation. Hence it can be small and simple. One possibility could be to design it using switch capacitor techniques [11]. The authors of [11] managed to build a LED driver with 93.3% efficiency and a power factor of 0.89 for a 35V dc 30 W load while achieving 50 $^{W}/_{in^3}$.

This architecture can achieve high efficiency, high power factor, low voltage stresses, and smaller component sizes by utilizing high frequency operation. Moreover, the scheme can be designed with different converter topologies to satisfy a large range applications and power levels.

Ultimately, by employing ideas similar to the ones explored in this study, like functional stage separation and ZVS soft switching, numerous architectures could be designed to utilize high frequency operation. Even in high power systems (100-1000 W).

2.3. Architecture of interest

The following section introduces our PFC architecture of interest. We are interested in a converter which provides a low dc output voltage drawing energy from a wide range ac input voltage while maintaining a high power factor.

We start with the standard two-stage PFC architecture, shown in Fig 2.8, and add several components to it to build our high frequency design, shown in Fig 2.9. We also analyze a specific subsystem in the PFC stage topology, the inverted resonant- discontinuous-conduction-mode buck converter [11], illustrated in Fig. 2.10.

Looking at the standard two-stage architecture, we notice that it provides three functions:

First, the "Power Factor Correction" (PFC) functions as an input stage drawing energy from a wide-range input current.

Second, an energy buffer to provide the required energy for twice-line-frequency ripple and holdup. The capacitor sizes should be able to provide enough twice line-frequency energy storage (i.e, to allow the output to be continuously supplied with constant dc power while drawing pulsating input power from the line). Moreover, the capacitor should be large enough to provide sufficient "hold up" energy. That is, the capacitor should provide enough energy storage that the converter output can be supplied at rated power even if the line voltage drops out for a

given period of time (e.g., a half line cycle or full line cycle). In our application, the specified duration is a full time cycle.

Third, an isolation, transformation and regulation stage which provides electrical isolation between the ac input and dc output. It also transforms the voltage used to store twice-line-frequency energy to the desired output voltage. Finally, it regulates the output voltage against any load variations.

Our architecture is a variant of the two-stage standard PFC architecture that can more effectively handle the wide universal input range voltage while maintaining high-frequency and high efficiency. It has a reconfigurable input-stage, a high frequency power processing stage, and power combining, isolation and regulation stage. The approach is particularly suitable for utilizing conventional, high-efficiency high-density telecom "brick" converters as the isolation and transformation stage. In our work we principally focus on the PFC stage (with two outputs), and but do evaluate commercial telecom converters for use as the second stage.

Shown in Fig 2.9, our architecture of interest is closely related to the 2-stage PFC architecture. The input stage is comprised of a diode bridge rectifier and a low-frequency, low-loss switch. When the input voltage is low, the configuration switch turns on and the input stage functions like a full bridge rectifier. And, when the input voltage is high (>200V), the configuration switch turns off and the input stage functions like a voltage doubler. This allows the second stage to be designed for smaller current and voltage operating ranges which in turn help us achieve switching frequency in the HF power stage.

The second stage "soft-switched high frequency power stage" comprises two inverted discontinuous-conduction-mode resonant buck converters, as shown in Fig 2.10. When the configuration switch is open, the two converters draw the same input current and deliver the same output current. And, when the switch is closed, each converter runs over half the line cycle only. The upper converter runs when the input voltage is positive, and the lower converter runs when the input voltage is negative. Consequently, the buck converters are rated for half the peak input current.

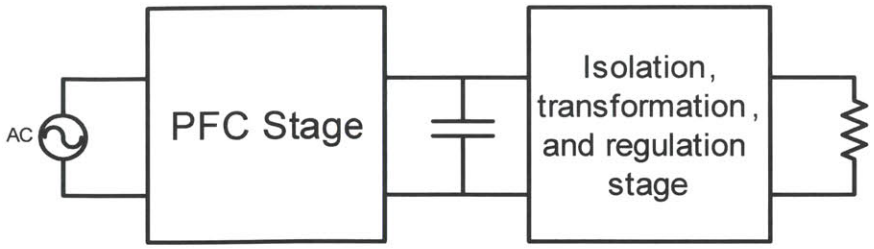

Fig 2.8: Two-stage grid interface power converter with a first power-factor correction (PFC) stage, an intermediate energy buffer, and a second isolation/transformation and regulation stage.

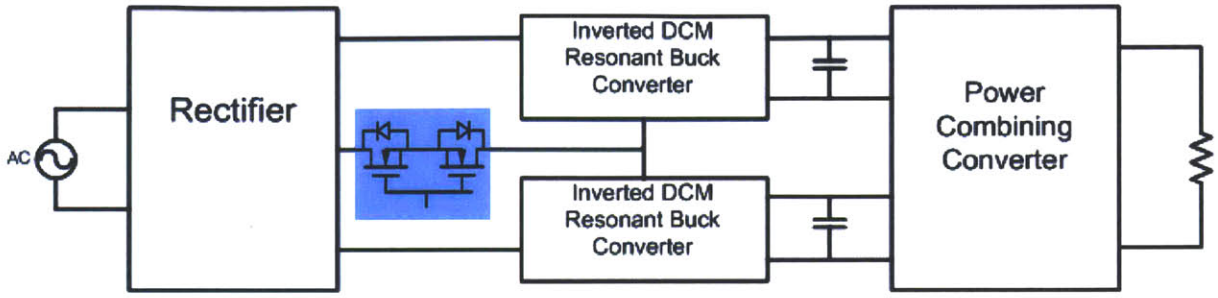

Fig 2.9: represents the topology of our high-frequency PFC system. The first stage is comprised of a full bridge rectifier and a configuration switch. When the input voltage is low, the switch allows the input stage to act as a voltage doubler. The two parallel buck converters function as a soft-switched HF power stage. The power combining stage combines the output energy from the two buck converters.

This first part of the thesis is concerned with optimizing the performance of the inverted discontinuous-conduction-mode buck converter shown in Fig. 2.9. The converter operates from a (80-186 V) input voltage range and outputs an average voltage of 72V with a current output up to 8 Amps. And, the converter's output capacitors are required to buffer energies between 0.3 and 1 Joules. Table 2.6 below lists a summary of the current, voltage, and power requirements.

Note: The inverted resonant-transition buck converter operates in the same way as its non-inverted counterpart. The design chooses the inverted converter is because its active switch is referenced to a slowly moving node, while the non-inverted converter has its active switch is referenced to a "flying node" which restricts the maximum achievable frequency (and can degrade efficiency owing to the difficulty of driving the switch). However, using the inverted converters requires and extra stage to combine the two separate output energy.

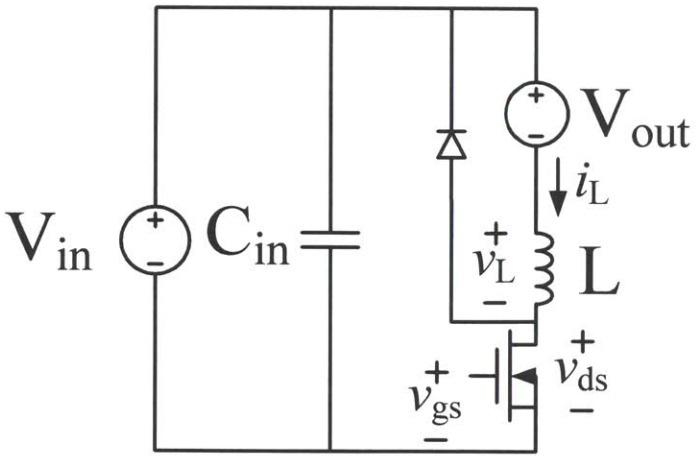

Fig. 2.10a illustrates the topology and components of an inverted resonant transition buck converter. This circuit works as a high-frequency dc-dc conversion block in the two stage converter design with 81-

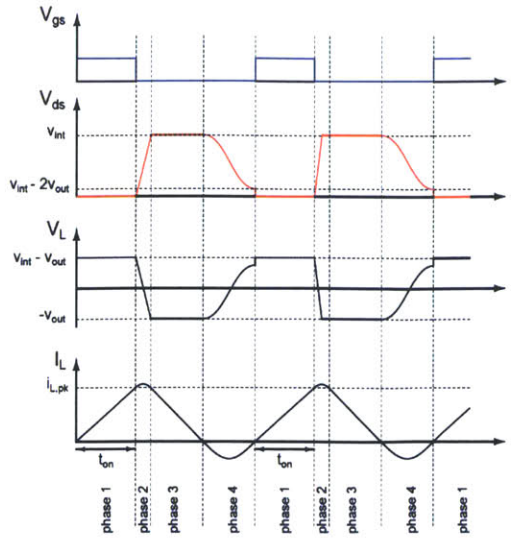

Fig. 2.10b Voltage and current waveforms of the resonant transition buck converter

Illustrated in Fig 2.10b, the bottom curve represents the inductor current ripple, the blue curve represents the switch gate drive and the red curve represents the voltage across the switch. The buck converter operates with high current ripple in the inductor; the design achieves a high switching frequency by minimizing the transistor voltage stress and achieving zero-voltage switching. Although the topology only operates with "ideal" ZVS soft switching over a 2:1 input voltage range (0.5 Vin < Vout < Vin), it still maintains high efficiency with a low ZVS over approximately a 3:1 input voltage range (~0.35 Vin < Vout < Vin). Moreover, the non-inverted resonant-conduction-mode buck converter has similar current and voltage characteristics, but does not have a ground-referenced switch.

Table 2.6 below shows a summary of the system and the single buck converter stage ratings we want to build:

	Entire System	Single buck converter
Input Voltage Range	85-265 Vrms	80-186 Vdc
Average Output Voltage	24 Vdc	72 Vdc
Average Output Power	240 Watts	573 Watts

Table 2.6: Entire system and single buck current, voltage, and power ratings.

Chapter 3

Twice Line Frequency Energy Buffering

This chapter covers a general study of the energy storage elements (capacitors and inductors), and the considerations taken into account when choosing the best devices – highest energy density -- to use for twice line frequency energy buffering. It also inspects the selection of the energy storage elements of a specific two stage PFC grid interface power converter.

3.1 Background and Motivation

Capacitors and Inductors are vital passive components in power electronic applications. Inductors are mainly used as magnetic energy storage elements while capacitors are used as electric energy storage elements. Other important uses include filtering, voltage and current stabilizing, and energy buffering. The topic of energy buffering is one that this document explores.

Often in power electronics, the size of a converter is dominated by passive components, namely the energy storage elements i.e. capacitors and inductors. There is an increasing demand for smaller, high efficiency, and high performance solutions for converters and power supplies. Since, energy storage requirements vary inversely with frequency. One way to decrease the size of needed passive components while still maintaining high performance is to operate at higher frequency.

That is why more and more power applications are utilizing higher frequencies to achieve, amongst others, higher energy density designs. We are interested in the energy buffering capabilities of capacitors, namely high energy density capacitors. This section is mainly

concerned with line frequency energy buffering. Energy buffering is independent of the converters operating frequency and depends only on line frequency.

In such applications and others, which require large capacitance values, electrolytic capacitors are mainly used. Electrolytic capacitors have bigger energy density than ceramic and film capacitors. They are often used as dc-link capacitors to reduce the ripple at dc output.

The goal is to find the capacitor with the smallest volume that satisfies our energy buffering and energy storage requirements to achieve a smaller overall system volume.

3.2 Architecture of interest

In many power electronics applications, especially multiple stage converters, there is a need for energy buffering. Our design of interest is a miniaturized two stage universal-input single-phase power-factor correction (PFC) converter which operates at high frequency. The first stage is a PFC stage and the second is a dc/dc isolation/transformation and regulation stage.

The two stages are connected by an intermediate energy buffering capacitor stage. High energy-density electrolytic capacitors can be used as buffering capacitors for interfacing between a single-phase ac source and a dc output load. Such applications our application of interest illustrated in Fig 3.1 below.

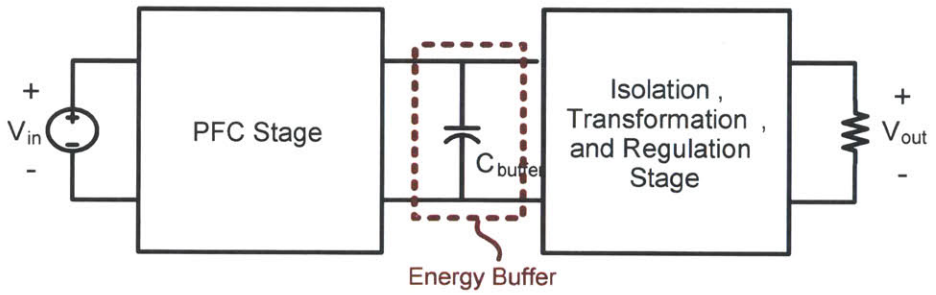

Fig 3.1 Two-stage grid interface power converter with a first power-factor correction (PFC) stage, an intermediate energy buffer, and a second is a dc/dc isolation/transformation and regulation stage.

The converter shown in Figure 3.1 above operates from a universal-input single-phase ac (85-265 Vrms and 50-60 Hz) to an isolated low-voltage dc output. While there are various architectures to achieve such conversion, the two stage approach provides very small PFC stage size and enables the use of telecom "brick" converters as the second stage.

3.3 Capacitor Energy

To figure out the best capacitor, first we analyze the capacitors energy buffering capabilities and to do so first we look at the energy stored by the capacitor. From physics perspective, to figure out the amount of energy stored on a capacitor, we can look at a parallel plate capacitor. We calculate the work it would take to put charge on the two plates of the capacitor. Or, how much work it would take to move a charge element (ΔQ) from the negative plate to the positive plate. Knowing that voltage is equal to energy per unit charge the amount of work it takes to move (ΔQ) from one plate to the other is:

$$\Delta W = Fd = \Delta QEd = V\Delta Q \quad (3.1)$$

Where F is the force needed to move ΔQ, d is the distance between the two plates, E is the electric field, and V is the capacitor voltage. Now we add up the work done to charge up the capacitor to Q.

$$Energy\ (E) = \int dW = \int_0^Q VdQ = \int_0^Q \frac{Q}{C_{buffer}} dQ = \frac{Q^2}{2C_{buffer}} \quad (3.2)$$

If we use the fact that ($dQ = CdV$) in the above equation, we get that the amount of energy stored on a capacitor in terms of voltage and capacitance:

$$Energy\ (E) = \frac{C_{buffer}V^2}{2} \quad (3.3)$$

It is often the case in applications that we charge and discharge only a fraction of the energy stored on the capacitor. For simplicity, we look at a sinusoidal capacitor voltage waveform. The energy we need to buffer in that case depends on the maximum voltage (V_{max}) and minimum voltage (V_{min}) on the capacitor.

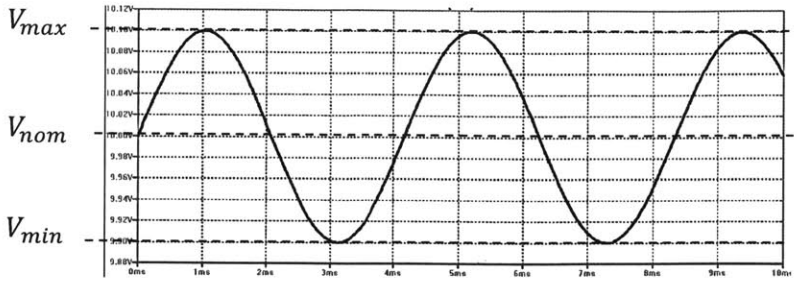

Fig 3.2 Capacitor voltage sinusoidal waveform

The equation for the buffered energy then becomes:

$$E_{buffer} = \frac{1}{2}C_{buffer}{V_{max}}^2 - \frac{1}{2}C_{buffer}{V_{min}}^2 = \frac{1}{2}C_{buffer}\left({V_{max}}^2 - {V_{min}}^2\right) \quad (3.4)$$

3.4 Capacitor Energy Buffering

In Fig 3.1, repeated below, the capacitor C_{buffer} provides twice-line-frequency energy buffering and energy for "holdup" to support the second stage operation over a temporary input line-voltage outage.

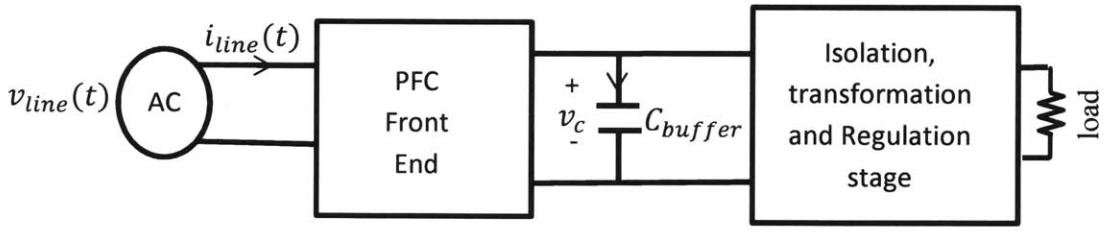

Fig 3.4 Two-stage grid interface power converter. The first stage is a power-factor correction (PFC) circuit, followed by an intermediate energy buffer. The second stage is a dc/dc converter that provides isolation/transformation and regulation stage.

Since we are considering electrolytic capacitors to achieve a high energy density design, we analyze three possible constraints to achieve minimum capacitor size:

1- Energy density constrained by design allowed ripple.
2- Energy density constrained by capacitor RMS limit.
3- Energy density constrained by holdup energy.

3.4.1 Energy Density Constrained by Allowed Ripple

The amount of energy and capacitance needed to limit the voltage ripple in v_c to within an acceptable range. The range is constrained by the operation of the PFC first stage and/or the second stage. The allowable ripple value is chosen by the designer.

The characteristics and shape of the capacitor voltage ripple is depends upon the PFC and second stage. However, if we make the simplifying assumption that the mean voltage of the waveform is half way between the peaks (as for sinusoidal or triangular ripple). We can use the "ripple ratio" R_c to characterize the waveform:

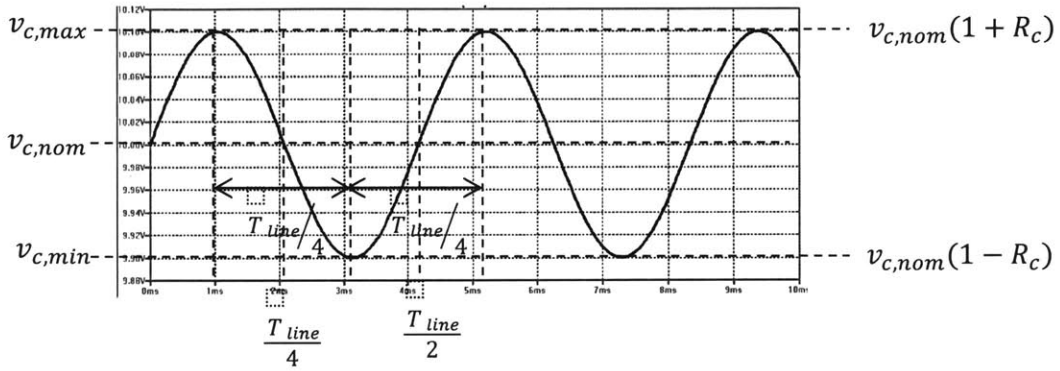

Fig 3.5 Capacitor sinusoidal voltage ripple

Where,

$$R_c = \frac{v_{c,max} - v_{c,min}}{2v_{c,nom}} = \frac{v_{c,max}}{v_{c,nom}} - 1 \qquad (3.5)$$

If we state that there is an allowed limit on ripple ratio (for converter design and operation purposes) we can express the energy buffered in a cycle as:

$$\begin{aligned} E_{buffer} &= \frac{1}{2} C_{buffer}\left(v_{c,max}{}^2 - v_{c,min}{}^2\right) \\ &= \frac{1}{2} C_{buffer} v_{c,nom}{}^2((1+R_c)^2 - (1-R_c)^2) \\ &= \frac{1}{2} C_{buffer} v_{c,nom}{}^2((1+R_c)^2 - (1-R_c)^2) \end{aligned}$$

$$= 2R_c C_{buffer} {v_{c,nom}}^2$$

$$E_{buffer} = \frac{1}{2} C_{buffer} {v_{c,max}}^2 \frac{4R_c}{(1+R_c)^2} \qquad (3.6)$$

If $v_{c,max}$ is the capacitors rated voltage, the peak energy storage capability of the capacitor is:

$$E_{c,pk} = \frac{1}{2} C_{buffer} {v_{c,max}}^2 = \frac{1}{2} C_{buffer} {v_{rated}}^2 \qquad (3.7)$$

Hence, by substituting (3.7) into (3.6) we can write the capacitor buffered energy as:

$$E_{buffer} = E_{c,pk} \frac{4R_c}{(1+R_c)^2} \qquad (3.8)$$

We can also find the usable energy density as:

$$\frac{E_{buffer}}{Volume} = \frac{E_{c,pk}}{Volume} \frac{4R_c}{(1+R_c)^2} \qquad (3.9)$$

Where $\frac{4R_c}{(1+R_c)^2}$ is the fraction of peak energy storage we can access at ripple ratio R_c. So if we know the peak energy density of a capacitor, we can find the usable energy density as constrained by ripple ratio.

The plot below shows the usable energy density for 5 different ripple ratio values against the rated voltage of all electrolytic capacitors listed on digikey.com (the website for the electronics supplier DigiKey). The data was downloaded on Feb 2015.

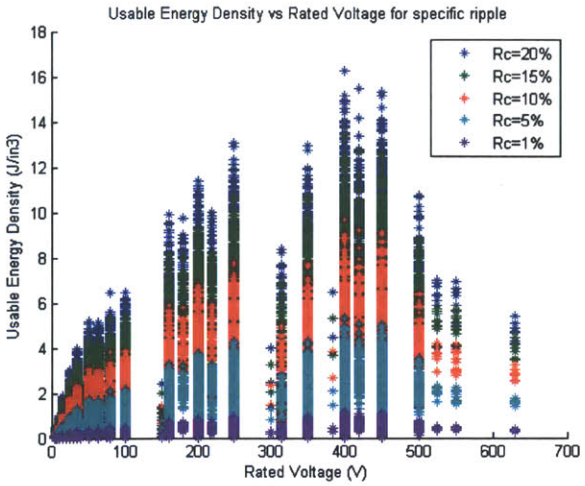

Fig 3.6 Usable energy density vs. rated voltage for available electrolytic capacitors for several ripple ratio values

We notice from Fig 3.6 that the higher ripple ratio gives us higher accessible energy (and hence higher energy density). We also notice that the highest energy density capacitors are the 400 V capacitors. (This may in part be because 400 V is an extremely common storage voltage for twice-line-frequency energy in grid-interface power supplies, and hence highly-optimized capacitors are available at that voltage rating.)

Furthermore, Fig 3.7 applies equation (3.10) to show the usable energy normalized by peak capacitor energy for different ripple ratio values:

$$\frac{E_{buffer}}{E_{c,pk}} = \frac{4R_c}{(1+R_c)^2} \qquad (3.10)$$

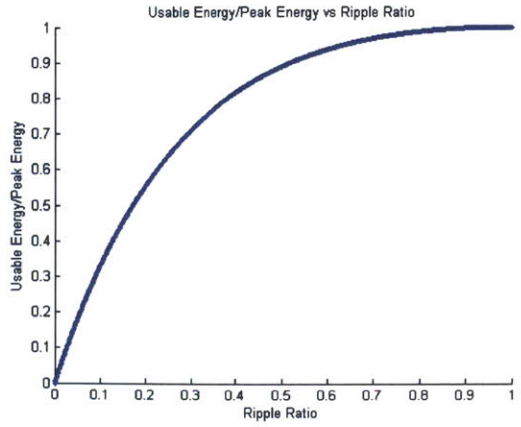

Fig 3.7 Usable energy normalized by peak capacitor energy for different ripple ratio value

3.4.2 Energy Density Constrained by RMS Current Limits

A second factor that may constrain the usable energy density of the capacitor is RMS current limits (which are ultimately governed by the thermal constraints of the capacitor). Before analyzing the RMS current constraint and what it means to a capacitors energy buffering capabilities. First we need to understand the meaning of the RMS ratings and why they are important.

The average current which flows in and the average voltage across AC circuit elements with sinusoidal excitation is zero, as shown below.

$$I_{avg} = \frac{1}{T}\int_0^T I_{peak}\sin(\omega t)\,dt = \frac{1}{T}I_{peak}\left[-\frac{\cos(\omega t)}{\omega}\right]_0^T = -\frac{1}{T}\frac{I_{peak}}{\omega}[\cos(2\pi) - \cos(0)] = 0$$

However, for joule heating of the capacitor (e.g., owing to parasitic resistance) we are concerned with average power dissipation in the parasitic resistance. This average power dissipation is related to the average of the square of the current times the parasitic resistance. Thus, despite the fact that the average current is zero, what we care about as regards parasitic heating is the square-root of the mean-square current. (The rms or root-mean-square current is the dc current that would generate the same dissipation in the same parasitic resistance as the original current.) That is why we use the RMS values of current and voltage when dealing with AC circuits. Furthermore, multi-meters output RMS values for current and voltage rather than peak values. The RMS value is the square root of the arithmetic mean of the squares of the values or waveform that define a function.

When currents is defined by a set of n values $\{I_1,\ I_2,\ I_3, \ldots, I_n\}$ then

$$I_{RMS} = \sqrt{\frac{{I_1}^2 + {I_2}^2 + {I_3}^2 + \cdots + {I_n}^2}{n}} \qquad (3.11)$$

And when current is defined by a continuous waveform, then

$$I_{RMS} = \sqrt{\frac{1}{T_2 - T_1}\int_{T_1}^{T_2} I(t)^2 dt} \qquad (3.12)$$

I_{RMS} is an important concept which is usually overlooked when using capacitors. If not considered properly, excess current may cause the capacitor to overheat and fail. Hence, I_{RMS} constrains the amount of energy a capacitor can buffer.

For our architecture, the RMS current limit constraint depends upon the current waveforms from the PFC stage and the current drawn by the second stage (e.g. for constant power to output). The current from the PFC stage likewise depends on the power factor and line voltage, as does the energy buffering requirement.

The simplest case to calculate, which also represents the best case, is to assume that the energy buffering capacitor charges and discharges at a constant current (charging for ¼ of the line cycle and discharging for ¼ of the line cycle). This represents the maximum usable energy from a capacitor within a given RMS current limit; all other situations will be worse (having a lower Δv_c for a given RMS value). Fig 3.8 shows the waveforms of this scenario.

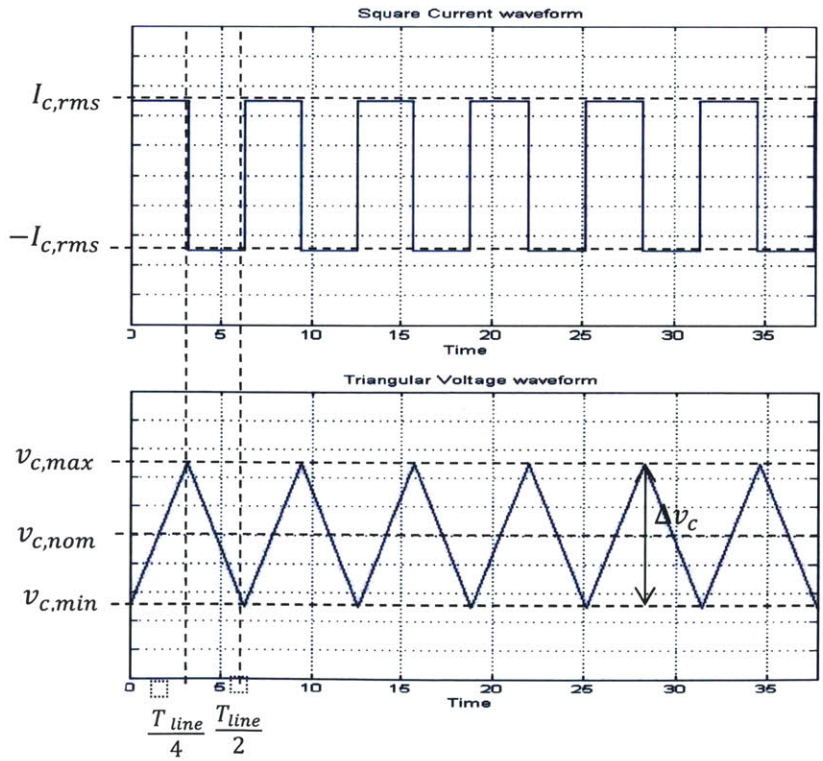

Fig 3.8 Square wave capacitor current waveform and triangular capacitor voltage waveform

Note that for the square wave the instantaneous charge and discharge current is the RMS current. Also, the plotted capacitor voltage ripple neglects the effects of ESR on the voltage ripple waveform.

If we assume that the capacitor charges and discharges at its RMS current limit:

$$\Delta v_c = \frac{I_{c,rms} T_{line}}{4 C_{buffer}} \qquad (3.13)$$

$$\begin{aligned} E_{buffer} &= \frac{1}{2} C_{buffer} {v_{c,max}}^2 - \frac{1}{2} C_{buffer} \left(v_{c,max} - \Delta v_c\right)^2 \\ &= C_{buffer} v_{c,max} \Delta v_c - \frac{1}{2} C_{buffer} {\Delta v_c}^2 \\ &= C_{buffer} \Delta v_c \left(v_{c,max} - \frac{\Delta v_c}{2}\right) \qquad (3.15) \end{aligned}$$

Hence,

$$E_{buffer} = C_{buffer} v_{c,nom} \Delta v_c = \frac{v_{c,nom} I_{c,rms} T_{line}}{4} \qquad (3.16)$$

From Fig 3.8 if we set $v_{c,max} = v_{c,rated}$ and substitute in for (3.13), we get:

$$v_{c,nom} = v_{c,rated} - \frac{\Delta v_c}{2} = v_{c,rated} - \frac{I_{c,rms} T_{line}}{4 C_{buffer}} \qquad (3.17)$$

Now we can calculate the capacitors buffered energy:

$$E_{buffer} = \frac{I_{c,rms} T_{line}}{4} \left(v_{c,rated} - \frac{I_{c,rms} T_{line}}{8 C_{buffer}} \right) \qquad (3.18)$$

Note that we can do related calculations for different charge and discharge waveforms to relate $I_{c,rms}$ to Δv_c.

For our application, we would like to identify the best capacitor in terms of usable energy and usable energy density. Fig 3.9 below uses equation (3.16) to show the energy density vs.

rated voltage constrained by RMS current capability of the available electrolytic capacitors in the market.

The output power is 120W and the frequency is 100 Hz. The capacitor data was downloaded from digikey.com on Feb 2015. Note, the plots show the best 522 capacitors. The plots below use the rated voltage instead of the nominal. Similar trends are noticed when using nominal voltage.

The highest energy density capacitors constrained by their RMS current limit are again the 400V capacitors. One can use capacitors even down to 80 V, paying for a penalty of less than a factor of two in energy density. Tables 3.1 and 3.2 below list the highest energy capacitors constrained by RMS current limit.

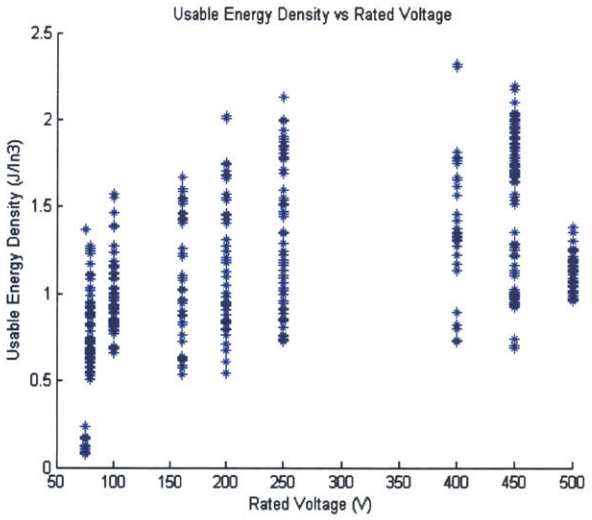

Fig 3.9 Usable energy density taking into consideration RMS current limits and triangular voltage waveforms

Manufacturer Part Number	Height (In)	Diameter (In)	RMS Current (A)	Voltage Rating (V)	Capacitance (uF)	Usable Energy (J)	Usable Energy Density (J/In3)
UCY2H150MHD1TO	1.043	0.492	0.22	500	15	0.275	1.386846
UCY2H150MHD	1.043	0.492	0.22	500	15	0.275	1.386846
380LX470M500H012	0.984	0.866	0.63	500	47	0.7875	1.358719
450QXW47MEFC10X45	1.85	0.394	0.44	450	47	0.495	2.194579
450QXW39MEFC10X40	1.654	0.394	0.39	450	39	0.43875	2.175701
UCP2W270MPD	1.319	0.394	0.3	450	27	0.3375	2.098682
UCY2G680MHD	1.634	0.492	0.72	400	68	0.72	2.317717
UCS2G220MHD1TO	0.866	0.492	0.38	400	22	0.38	2.308052
UCS2G820MHD1TN	1.063	0.709	0.7625	400	82	0.7625	1.816872

Table 3.1 lists the highest energy density capacitors constrained by RMS current limit available at 400V to 500V. The RMS current is calculated at 100 Hz (twice-line frequency)

Manufacturer Part Number	Height (In)	Diameter (In)	RMS Current (A)	Voltage Rating (V)	Capacitance (uF)	Usable Energy (J)	Usable Energy Density (J/In3)
UCS2D680MHD1TO	0.846	0.492	0.65	200	68	0.325	2.020658
UCY2D680MHD3TO	0.846	0.492	0.65	200	68	0.325	2.020658
UCY2D820MHD9TO	0.846	0.492	0.645	200	82	0.3225	2.005115
UCY2C820MHD3TO	0.846	0.492	0.64	160	82	0.256	1.591657
UCY2C820MHD3TO	0.846	0.492	0.64	160	82	0.256	1.591657
EEU-EE2C470	0.787	0.394	0.37275	160	47	0.1491	1.553891
EKZN101ELL560MH20D	0.846	0.315	0.416	100	56	0.104	1.577437
EKZN101ELL180MF11D	0.492	0.248	0.148	100	18	0.037	1.556838
EKZN101ELL330MHB5D	0.512	0.315	0.248	100	33	0.062	1.553856
EKZN800ELL221MJ25S	1.043	0.394	0.81	80	220	0.162	1.273938
EKZN800ELL820MH20D	0.846	0.315	0.416	80	82	0.0832	1.261949
EKZN800ELL270MF11D	0.492	0.248	0.148	80	27	0.0296	1.24547
DCMC223U075AF2B	5.687	1.375	10.8	75	22000	2.025	0.239799
E36D750MLN183TC79M	3.125	2	9.4	75	18000	1.7625	0.179527
DCMC303U075BC2B	4.125	2	12.1	75	30000	2.26875	0.17507

Table 3.2 lists the highest energy density capacitors constrained by RMS current limit available at 75V to 200V. The RMS current is calculated at 100 Hz (twice-line frequency)

3.4.3 Hold up time requirement

Moreover, when designing systems for applications such as DC/DC converters in telecom and Off-line power supplies, designers are faced with the topic of hold-up requirement. In such applications, the design must be able to continue operating for a set time (T_{holdup}) after the input energy source turns off at a specified converter load (e.g., one line cycle at full load). During this time the energy is taken from the buffering capacitor of the converter.

Hence, a third factor that might constrain capacitor size is the holdup time requirement. It is assumed for this case that the AC line voltage goes away for some duration T_{holdup} and that converter is required to support an output power $P_{o,holdup}$ during this time. Moreover it is assumed that the buffer capacitor may discharge down to $v_{c,holdmin}$during this time. The waveforms are illustrated in Fig 3.10 below.

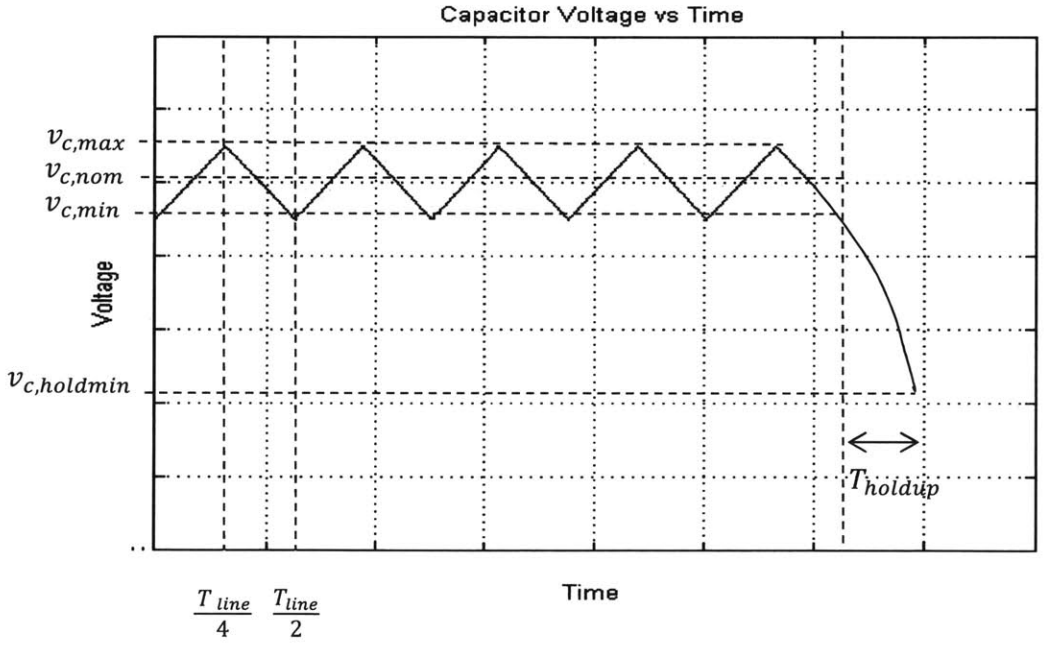

Fig 3.10 illustrates the capacitor voltage vs time under holdup requirement

Fig 3.10 above illustrates the capacitor voltage under normal operation where the voltage ripples around the nominal voltage and under holdup operation where the voltage drops down to the minimum operating voltage of the second stage.

The details of the calculation may vary based on when we assume the line voltage may go away, etc. but we can treat as follows:

$$i_c = C_{holdup}\frac{dv_c}{dt} = \frac{-P_{o,holdup}}{v_c}$$

$$v_c dv_c = \frac{-P_{o,holdup}}{C_{holdup}}dt$$

$$\int_{v_{c,holdmin}}^{v_{c,min}} C_{holdup} v_c dv_c = \int_0^{T_{holdup}} P_{o,holdup} dt$$

$$E_{holdup} = \frac{1}{2}C_{holdup}\left({v_{c,min}}^2 - {v_{c,holdmin}}^2\right) = P_{o,holdup}T_{holdup} \quad (3.19)$$

For our application, we would like to know the amount of required hold up capacitance needed to supply constant output power for a set duration of time, without dropping our capacitor voltage below a minimum discharge voltage. Fig 3.11 below uses equation (3.19) to show the amount of capacitance we need to supply 120W of constant output power for 20ms (or 30ms) without dropping below a minimum discharge voltage starting from 72V.

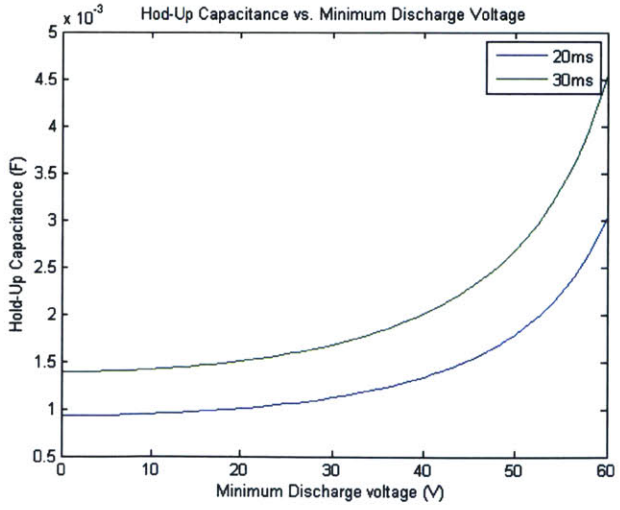

Fig 3.11 Hold up capacitance vs minimum discharge voltage. This is for a discharge from 72 V on the capacitor to a specified minimum voltage assuming a constant 120 W load.

Consider an example where we store holdup energy on a capacitor at a 72 V nominal voltage. From Fig 3.11 we can calculate the minimum holdup capacitance required with a 20ms (and 30ms) holdup time for different minimum discharge voltages. The commercial second stage converters of interest (e.g., as described in Chapter 5) can have a minimum discharge voltage of 18V or 36V. Looking at the 20ms holdup time, for a minimum discharge of 18V, the holdup capacitance is 0.9877 mF and for 36V, the holdup capacitance is 1.235mF.

Tables 3.3 and 3.4 below illustrate the minimum box volume for 80V capacitors with a capacitance of at least 0.9877mF and 1.235mF respectively. The tables also list the capacitor ripple current constraint at 100Hz:

Manufacturer Part Number	Height (In)	Diameter (In)	Voltage Rating (V)	Capacitance (mF)	RMS Current (A)	No. of Caps (0.9877mF)	Box Volume (0.9877mF)
EGPD800ELL112MM30H	1.24	0.709	80	1.1	1.932	1	0.623324
EKZN800ELL122ML40S	1.634	0.63	80	1.2	2.106	1	0.648535
EKYB800ELL122ML40S	1.634	0.63	80	1.2	1.74	1	0.648535
EKZN800ELL122MMN3S	1.299	0.709	80	1.2	1.716	1	0.652983
EKZN800ELL561MK35S	1.437	0.492	80	0.56	1.3	2	0.695692

Table 3.3 lists the smallest 80Vcapacitor box volume for 0.9877mF minimum (2:1 discharge). The RMS current is calculated at 100 Hz (twice-line frequency)

Manufacturer Part Number	Height (In)	Diameter (In)	Voltage Rating (V)	Capacitance mF	RMS Current A	No. of Caps (1.235mF)	Box Volume (1.235mF)
EKZN800ELL152MMP1S	1.457	0.709	80	1.5	2.106	1	0.732406
EKYB800ELL152MMP1S	1.457	0.709	80	1.5	1.83	1	0.732406
EKYB800ELL681MK40S	1.634	0.492	80	0.68	1.47	2	0.791065
EKZN800ELL182MM40S	1.634	0.709	80	1.8	2.316	1	0.821381
EGPD800ELL162MM40H	1.634	0.709	80	1.6	2.292	1	0.821381

Table 3.4 lists the smallest 80V capacitor box volume for 1.235mF minimum (4:1 discharge). The RMS current is calculated at 100 Hz (twice-line frequency)

In our application of interest, we have a total allocated volume of 4.8 $in^3$for the whole converter. From the tables above we can calculate the percentage of this target volume for the volume required by the holdup capacitors. With a minimum discharge voltage of 18V, the holdup capacitors take up 25.9% of total volume. And with a minimum discharge voltage of 36V, the holdup capacitors take up 30% of total volume. The volume is even larger when we use 100V capacitors at 72V as shown in table 3.5 and 3.6 below:

Manufacturer Part Number	Height (In)	Diameter (In)	Voltage Rating (V)	Capacitance (mF)	RMS Current (A)	No. of Caps for 0.9877 mF	Box Volume for 0.9877 mF
UVR2A331MHD	0.984	0.492	100	0.33	0.76	3	0.714573
UVZ2A331MHD	0.984	0.492	100	0.33	0.54	3	0.714573
ECA-2AM102	1.476	0.709	100	1	1.3	1	0.741957
ECA-2AHG102	1.476	0.709	100	1	0.985	1	0.741957

Table 3.5 lists the smallest 100V capacitor box volume for 0.98775mF at least (2:1 discharge). The RMS current is calculated at 100 Hz (twice-line frequency)

Manufacturer Part Number	Height (In)	Diameter (In)	Voltage Rating (V)	Capacitance (mF)	RMS Current (A)	No. of Caps for 1.235 mF	Box Volume 1.235 mF
UVR2A331MHD	0.984	0.492	100	0.33	0.76	4	0.952764
UVZ2A331MHD	0.984	0.492	100	0.33	0.54	4	0.952764
ESMG101ELL331MK25S	1.043	0.492	100	0.33	0.76	4	1.009891
100PX330MEFC12.5X25	1.043	0.492	100	0.33	0.69	4	1.009891
UVR2A331MHD1TO	1.063	0.492	100	0.33	0.76	4	1.029256

Table 3.6 lists the smallest 100V capacitor box volume for 1.235mF at least (4:1 discharge). The RMS current is calculated at 100 Hz (twice-line frequency)

Furthermore, we can express our hold up energy equation in terms of ripple ratio:

$$E_{holdup} = P_{o,holdup}T_{holdup} = \frac{1}{2}C_{holdup}\left((v_{c,nom}(1-R_c))^2 - {v_{c,holdmin}}^2\right) \quad (3.20)$$

Fig 3.12 below uses equation (3.20) to shows the different capacitor values we would need to supply 120W of constant output power for 20ms (or 30ms) without dropping below 36V (or 18V) for different ripple values with 72V nominal capacitive storage voltage.

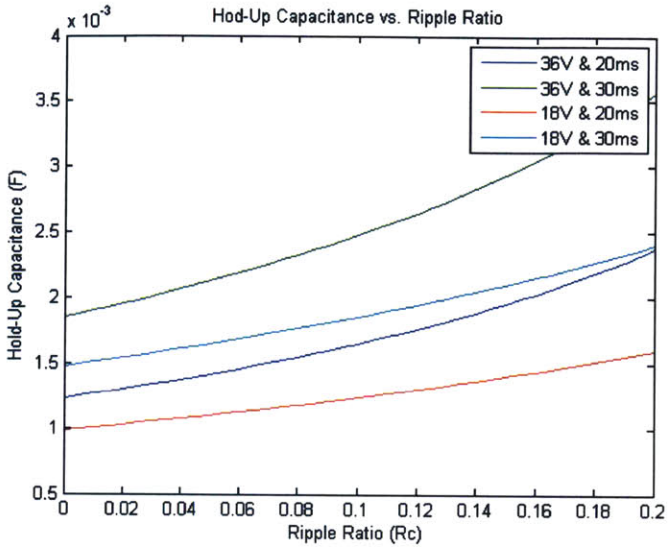

Fig 3.12 hold up capacitance vs ripple ratio

Fig 3.13 below illustrates the maximum energy density for available capacitors, this data was downloaded from digikey.com during Feb, 2015) One can use this figure to get a first order approximation for capacitor sizing under holdup constraint.

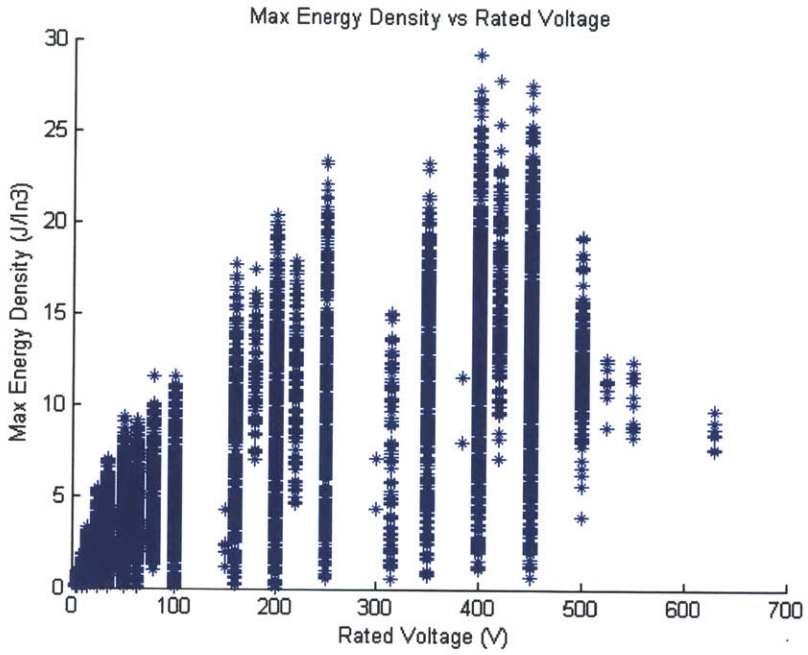

Fig 3.13 illustrates the max energy density for available capacitors.

Ultimately, what ripple ratio exists during (non-holdup) operation depends upon the capacitor size requirement (e.g. during holdup). Hence, we can first find the minimum capacitance that meets the ripple ratio requirement in the topology. Then select a large enough capacitance that meets the ripple ratio constraint and the RMS current constraint. This gives an approximate voltage minimum value. After that, select a large enough capacitance that would also meet the holdup requirement from that voltage minimum value. This will give a conservatively sized capacitor that meets all of ripple ratio, rms current and holdup time constraints. If the capacitance value increases due to the holdup requirement, the minimum voltage will also increase.

3.5 Design Application

This section applies the capacitor constraints, explained in previous chapters, and provides specific capacitor recommendations. It evaluates and compares different capacitors, namely 80V, 160V and 400V capacitors, at an average power of 120W for different discharge ratios, namely 2:1 and 4:1, for our specific design. It also identifies choices for second stage dc/dc converters that fit our design specifications.

3.5.1 Topology of Interest

The diagram below, repeated from previous chapter, illustrates the developed topology of interest.

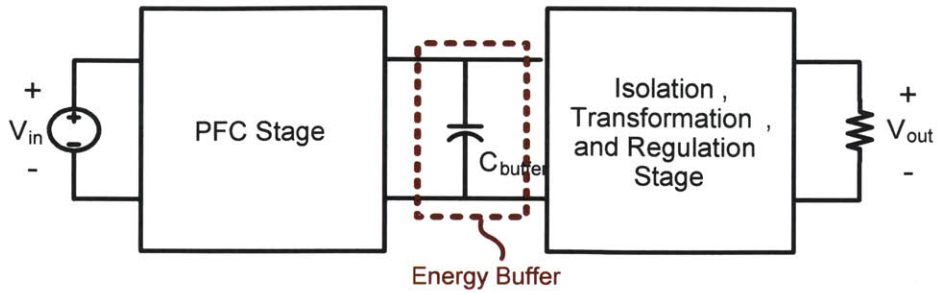

Fig 3.14 Two-stage grid interface power converter with a first power-factor correction (PFC) stage, an intermediate energy buffer, and a second is a dc/dc isolation/transformation and regulation stage.

We would like to minimize the volume of the energy buffering capacitors and the second stage dc/dc converter to achieve the highest energy density possible while still maintaining high efficiency. In order to do so we need to figure out the amount of capacitance needed, the nominal voltage to store our energy at, and the RMS current limitation. The section below presents a detailed analysis for 80V capacitors and the results for 160V and 400V capacitors for our topology of interest.

3.5.2 Capacitor Selection and Conclusion

In order to compare design options (and conventional solutions) we assume we can choose to buffer our energy using 80V, 160V or 400V capacitors at a nominal voltage near the rated voltage. We assume the following ratings: Power 120 W, Line Frequency 50 Hz, Rated holdup: 1 line cycle at 120 W. Fig 3.13 shows that 400V capacitors have the highest energy density. While this may seem like a reasonable choice for the capacitors, we get penalized in efficiency and volume of the second stage converters when we step down from 160V and 400V to our desired output. Furthermore, we would like our choice of capacitors to meet both ripple and hold-up specifications. The analysis below examines the tradeoffs in using the capacitors at different voltages.

First we do the analysis 80V capacitors. Again, we need to calculate the optimal buffer and holdup capacitance, the nominal operating voltage, and the RMS current limit. To calculate the capacitance and nominal operating voltage, we substitute equations (3.5) into (3.19), and plot (3.6) and (3.19) as a function of $v_{c,nom}$. We can choose the second stage converter to have an input voltage range of 18-75 V (e.g. Synqor's IQ36240QTx05) for a 4:1 discharge, which translates to a $v_{c,max}$ of 75 V and $v_{c,holdmin}$ of 18 V. Or, an input voltage range of 36-75 V (e.g. Synqor's SQ60120ETA20) for a 2:1 discharge. Since the size of the capacitors is inversely proportional to the minimum discharge voltage, for minimum capacitor volume we use 4:1 discharge, this plot is shown in Fig 3.14 below. From Fig 3.14, the minimum value of capacitance is the interception of both graphs; in this case the minimum capacitance is 1.189 mF stored at $v_{c,nom}$ = 71.65 V. Similar analysis for a 2:1 discharge gives us a minimum capacitance of 1.454 mF and a $v_{c,nom}$ = 72.3 V.

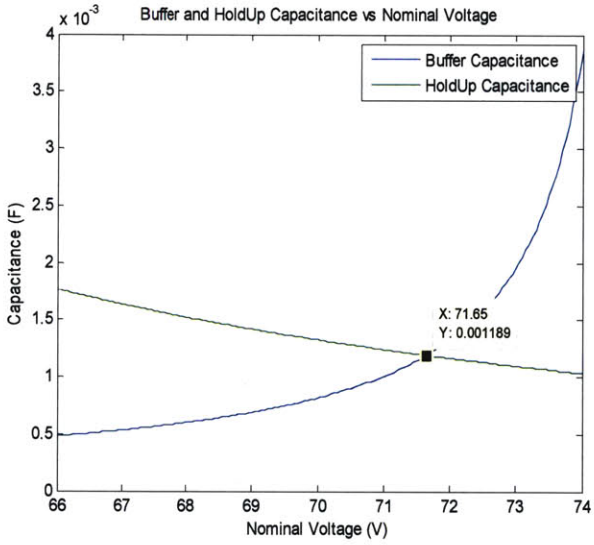

Fig 3.14 shows a plot of buffer and holdup capacitance requirements as a function of nominal voltage. This plot tells us the minimum capacitance that meets both buffer and hold-up capacitance specs for 80V capacitors with 4:1 discharge. The intersection point in the plot and shows C= 1.189 mF and nominal voltage = 71.65V.

Now we find the RMS current rating for the capacitor current. Fig 3.15 below illustrates the current model for our topology of interest, shown in Fig 3.13. We assume that the second stage converter draws constant dc current (in our case it is the average of the current supplied by the PFC) and the entire current ripple goes through the capacitor. We can relate the current out of

the PFC stage, the current drawn by the second stage, and the current into the capacitor as follows:

$$I_C = I_{PFC} - I_{DC} \quad (3.21)$$

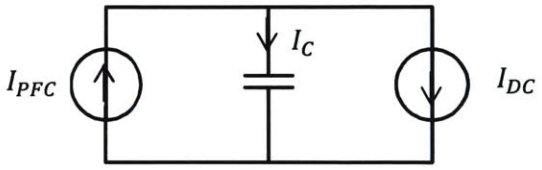

Fig 3.15 shows the current model for our topology of interest

For our topology of interest I_{PFC} is defined as follows:

$$I_{PFC} = \begin{cases} I_{pk}sin^2(\omega t) & , \ 43° < \omega t < 137° \ and \quad 223° < \omega t < 317° \\ 0 & , \ otherwise \end{cases}$$

Where, $I_{pk} = \frac{Peak\ Power\ (W)}{Nominal\ Voltage\ (V)}$ and the peak power for our topology of interest is 300W. Fig 3.16 below shows the waveforms for I_{PFC} and I_C for a nominal voltage of 71.65V.

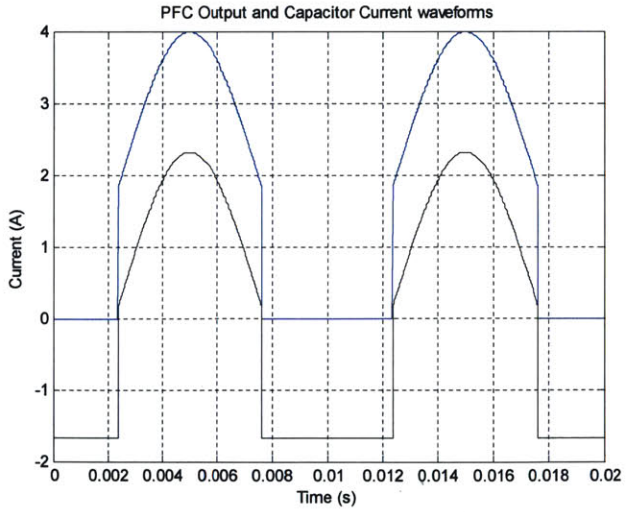

Fig 3.16 shows the PFC stage output current waveform (Blue), and the capacitor current waveform (Black)

From Fig 3.16 we can see that the average current $I_{DC} = 1.6761\ A$ and $I_{pk} = 3.9916\ A$. We also find the RMS current (explained in section 3.4.2) to be 1.6723 A. Now we can find the smallest capacitor or combination of capacitors rated for 80 V with an RMS current rating greater than

1.6723 A at 100 Hz and an equivalent capacitance greater than 1.189 mF. Shown in Table 3.3, the smallest energy buffering capacitor that satisfies the capacitance and RMS current constraints chosen as the best candidate is the EKZN800ELL122ML40S (rated for 80 V, capacitance of 1.2 mF and RMS current capacity of 2.106 A). The percentage of total volume taken by this capacitor is 13.51 % of the target volume for the PFC system. Doing the same calculation for a 2:1 discharge, we find that the RMS current is now 1.6573 A.

Similar analysis can be done for 160V and 400V capacitors. We found that the optimal capacitor nominal voltage to store energy is around 144V for 160V capacitors and around 365 for 400V capacitors. Tables 3.7 and 3.8 below list a summary of 80V, 160V, and 400V capacitors and their corresponding capacitance and RMS current requirements for a 2:1 and 4:1 discharge. The tables also show the percentage of total volume (4.8 in^3) each constraint requires.

Rated Voltage	Box Volume (in3)	Percentage of total volume (4.8in3)	Requirement
80 V	0.64853	13.5%	C > 1.189mF Ic_RMS > 1.6761A
160 V	0.498	10.3%	C > 0.2976 mF Ic_RMS > 0.8361A
400 V	0.25676	5.35%	C > 46.4 uF Ic_RMS > 0.33A

Table 3.7 provides a summary of the smallest capacitor box volume percentage taking into account the buffer and holdup capacitance, and RMS current constraints. The holdup constraint is calculated for a 4:1 discharge.

Rated Voltage	Box Volume (in3) Single	Percentage of total volume (4.8in3)	Requirement
80 V	0.7324	15.26%	C > 1.454mF Ic_RMS > 1.6573A
160 V	0.548	11.42%	C > 0.3636 mF Ic_RMS > 0.8286 A
400 V	0.3527	7.35%	C > 56.3 uF Ic_RMS > 0.3273A

Table 3.8 provides a summary of the smallest capacitor box volume percentage taking into account the buffer and holdup capacitance, and RMS current constraints. The holdup constraint is calculated for a 2:1 discharge.

Tables 3.9 – 3.14 below list the smallest capacitors at 80V, 160V and 400V for both 2:1 and 4:1 discharge.

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
EKZN800ELL122ML40S	1.634	0.63	80	1.2	2.106	0.648535
EKYB800ELL122ML40S	1.634	0.63	80	1.2	1.74	0.648535
EKZN800ELL122MMN3S	1.299	0.709	80	1.2	1.716	0.652983

Table 3.9 lists the smallest 80V capacitors for 4:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
EKZN800ELL152MMP1S	1.457	0.709	80	1.5	2.106	0.732406
EKYB800ELL152MMP1S	1.457	0.709	80	1.5	1.83	0.732406
EKZN800ELL182MM40S	1.634	0.709	80	1.8	2.316	0.821381

Table 3.10 lists the smallest 80V capacitors for 2:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
160TXW100MEFC8X40	1.673	0.315	160	0.1	0.49	0.49801
160TXW330MEFC12.5X50	2.067	0.492	160	0.33	1.2	0.500346
UCY2C151MHD9TO	1.043	0.492	160	0.15	0.76	0.504946

Table 3.11 lists the smallest 160V capacitors for 4:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
160TXW390MEFC12.5X55	2.264	0.492	160	0.39	1.35	0.548033
UCY2C391MHD9	1.457	0.63	160	0.39	1.51	0.578283
160TXW390MEFC16X35	1.476	0.63	160	0.39	1.34	0.585824

Table 3.12 lists the smallest 160V capacitors for 2:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
400BXW47MEFC10X40	1.654	0.394	400	0.047	0.44	0.25676
UPZ2G470MND9	1.654	0.394	400	0.047	0.435	0.25676
EKXJ401ELL560MJ50S	2.028	0.394	400	0.056	0.44	0.314819

Table 3.13 lists the smallest 400V capacitors for 4:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

Manufacturer Part Number	Height (Inches)	Diameter (Inches)	Voltage Rating (V)	Capacitance (mF)	RMS Current at 100 Hz (A)	Box Volume (In3)
400BXW68MEFC12.5X35	1.457	0.492	400	0.068	0.57	0.352687
UCP2G680MHD	1.476	0.492	400	0.068	0.54	0.357286
400BXW33MEFC10X30	1.26	0.394	400	0.033	0.34	0.391195

Table 3.14 lists the smallest 400V capacitors for 2:1 discharge. The current ripple is calculated at 100 Hz (Twice line frequency)

To conclude, we get smaller volume for 2:1 discharge as opposed to 4:1 discharge. Commercial dc-dc converters tend to be more efficient when operating at 2:1 discharge. We explore that more in chapter 5. Hence, one should choose 2:1 discharge if efficiency is the priority and 4:1 discharge if volume is the priority. Ultimately, one can use this analysis to compare different capacitors (across different voltage ratings) and figure out the best nominal voltage and capacitor to achieve the smallest volume needed to process a specific output power. From tables 3.7 and 3.8 we can see that if we want to process 120W we can achieve the smallest volume by using 400V capacitors. Our volume increases by more than twice if we were to use 80V capacitors.

Chapter 4

Inductor design for Resonant Transition Buck Converter

This chapter covers the considerations taken when designing the inductor for a resonant transition buck converter. The goal is to design an inductor with small losses, including both core and winding losses, to achieve high efficiency. Moreover we would like to find the smallest inductor to achieve a high energy density and high efficiency design.

4.1 Background and Motivation

The current trend in power electronics is to move to miniaturized designs. Inherently, the size of power electronics circuits is dominated by passive components. Since the energy storage requirements of inductors in a power converter are inversely proportional to the frequency of operation; there is an opportunity to move to smaller sizes through increases in frequency [18]. However, in practice, physical component sizes do NOT reduce proportional to frequency (or even monotonically with frequency in many cases). Moreover, operating at higher frequencies enforces other design constraints and requires appropriate methods to handle losses, thermals, etc.

Even though increasing the operational frequency allows us to (in some cases) decrease the size of the required magnetic component, we cannot increase the frequency indefinitely hoping to get even smaller designs. The core loss and copper loss increase with frequency and our design will suffer from a decrease in efficiency and an increase in temperature rise [21] [22]. This tells us that there is a "sweet spot" optimal frequency at which we can achieve the smallest design with acceptable losses and temperature rise. This sweet spot depends upon available magnetic core materials, conductor structures (e.g., litz wire, copper thickness, etc.)

The design of magnetic components depends on many factors. Those include: Desired inductance, applied voltage, core material flux density saturation, core loss, ac and dc resistance, winding loss, and temperature rise. The different circuit topologies in which magnetic components are used enforce limitations and constrains on inductor designs. An inductor can be limited by one or more of the factors depending on the inductor's functionality. These limitations must be respected to ensure reliable and proper circuit operation.

Currently, there isn't a simple and general way to design inductors. This is due to the many factors that can limit the inductor design, all of which need to be considered. This chapter explores one of the ways that can be used to design an a planar inductor for a resonant transition buck converter (to be used in the proposed grid interface converter). It goes though the inductor calculation for a specific design, illustrated in Fig 4.1 below.

4.2 Inductance Requirement

In order to figure out the inductance value needed for the inductor, we need to inspect the waveform of the current going through the inductor. And to get the inductor current waveform we need to look at our circuit topology and operation. The inductor we are trying to design is for a resonant transition inverted buck converter circuit at the edge of discontinuous conduction mode.

Fig 4.1 below illustrates the topology and components of a resonant transition inverted buck converter (RTI). This topology has been successfully used at high frequencies and voltages in recent works, including [12]. The circuit works at the edge of discontinuous conduction mode (DCM) and operates near zero voltage switching (ZVS) to minimize the switching losses since the design is operating at high frequency switching, between 1 to 4 MHz. Also, the low voltage stress allows operation with large device capacitance and enables the use of small valued and small size inductors to help with the resonant transition of the buck.

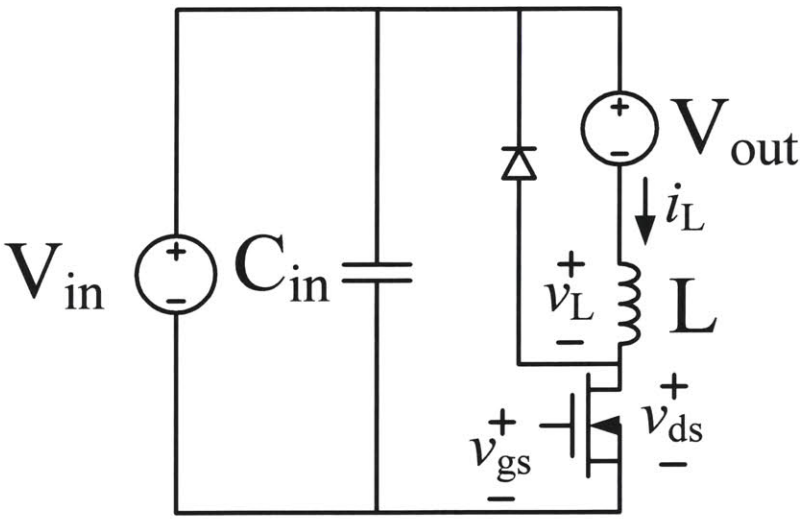

Fig 4.1 illustrates the topology and components of an inverted resonant transition buck converter. This circuit works as a high-frequency dc-dc conversion block in the two stage converter design with 81-186V input voltage to 72V output voltage.

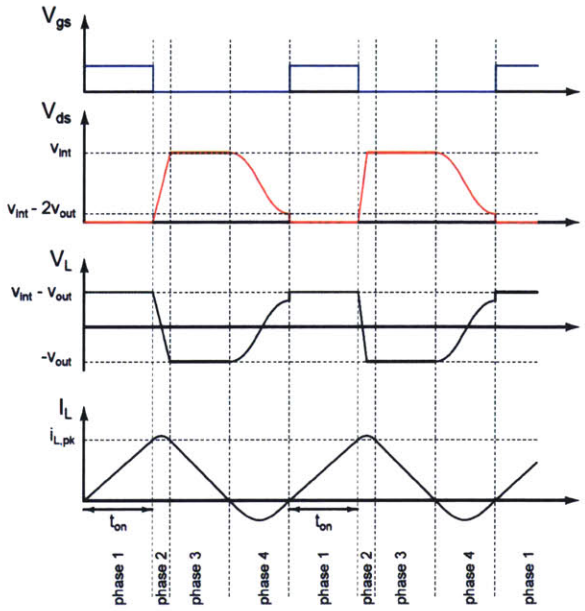

Fig 4.2 Voltage and current waveforms of the resonant transition buck converter

Now that we have our inductor current waveform, illustrated above in Fig 4.2, we can calculate the required inductance value for the inductor. From Fig 4.2 above we notice in phase 1 how the inductance value is limited by the transistor switch on-time. We will consider an RTI Buck converter design based on the following specifications: Input voltage between 81-186V, output voltage of 72V, and output power of 300W.

Hence,

$$v_L = \int L \frac{di_L}{dt}$$

$$L = t_{on} * \frac{(V_{in} - V_o)}{i_{L,PK}} \quad (4.1)$$

From (4.1) we see that the inductance value needed depends on the input voltage, output voltage, peak inductor current and transistor switch on time. Again, the resonant transition buck converter is required to process 300W at maximum input voltage with the input ranges between 186V down to 81V while the output is constant at 72V. For less than maximum input voltage, the power backs off approximately as the square of input voltage, in keeping with its application in a PFC converter.

To size the inductor, we assume a minimum transistor on-time that can be effectively utilized (e.g., owing to control limitations), leading to a minimum value of inductance to limit current to a desired value during that on-time. In this case, the operating point which sets the inductance is when we are operating at high input voltage and low current. At that point, the input voltage is 186V, the peak inductor current is 0.85A and the resonant transition buck converter is processing 10% of rated power. We assume that for below 10% of rated power that other techniques, such as burst-mode control, can be used to control power. Furthermore, given a minimum driver and transistor on-time of 20ns:

$$L = t_{on} * \frac{(V_{in} - V_o)}{i_{L,PK}} = 20ns * \frac{(186V - 72V)}{0.85A} \approx 3\mu H$$

The frequency at which the converter operates depends on the on-time of the FET, which depends on the amount of power we draw from the input, and inductance value of the inductor, and the capacitance value of the FET and diode. While and expression can be derived for ideal conditions (like eliminating the non-linearity of the capacitance), the dependency on power makes it hard to do so. The frequency was measured experimentally and ranged between 1 to 4 MHz.

After calculating the inductance value needed, we design the inductor to have the smallest achievable volume with acceptable losses and temperature rise. To do so we need to pick out the best performance core materials at our operating frequency of interest. We also need to pick a suitable inductor geometry, copper winding thickness, and number of layers.

The sections below do the analysis on E cores and planar inductors. Similar analysis can be done on others (e.g. rods, toroids, etc). E cores are good because they contain the magnetic field inside the core, as opposed to rod cores for example which require shielding. We will consider a conventional E core inductor structure with a gapped center post, Illustrated in Fig 4.3 below.

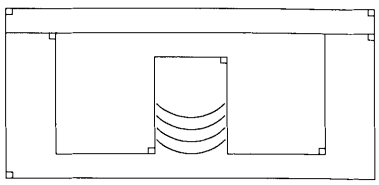

Fig 4.3 illustrates an E core inductor with the winding on a gapped center post

4.2.1 Inductor Gap

To determine the size of the inductor gap we can use the magnetic circuit model, illustrated in Fig 4.4 below. The E core inductor material has a permeability of μ_c. The inductor has a coil of N turns that carries current around the center post. The mean length of the of the magnetic core is l_c and the cross sectional area is A_c.

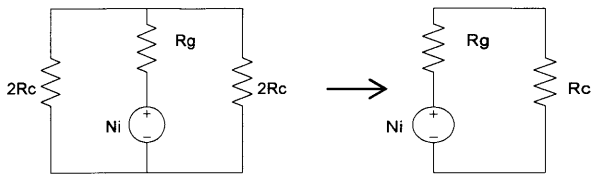

Fig 4.4 illustrates the magnetic circuit model of the E core in Fig 4.3

Assuming that permeability of the core material is high and the displacement current in Maxwell's Equations is negligible due to the size of the inductor and the operating frequency, we can conclude that the magnetic flux will be contained within the core. Now we can use Ampere's law to relate the magnetic field strength H_c to the current through the windings. Moreover, we note that the source of the magneto motive force (MMF) in the core is the current in the winding. In other words,

$$MMF\ (magneto\ motive\ force) = Ni \quad (4.2)$$

Also since,

$$\oint_{Closed\ path} H \cdot dl = \int_{Interior\ path} J \cdot da$$

We get

$$H_c(t) l_c = Ni(t) \quad (4.3)$$

The flux density B is related to the total magnetic flux φ_c passing through the inductor's effective cross sectional area A_c. Assuming a uniform flux distribution, we get

$$\varphi_c = \int_{surface\ A_c} B \cdot dA = B_c(t) A_c \quad (4.4)$$

The permeability of core materials is often characterized by the relation between the flux density and strength of the magnetic field. This relation in magnetic core materials is highly nonlinear with hysteresis and saturation. It can be characterized by a piecewise-linear model as the following

$$B_c = \begin{cases} B_{sat} & for\ H_c \geq B_{sat}/\mu_c \\ \mu_c H_c & for\ |H_c| < B_{sat}/\mu_c \\ -B_{sat} & for\ H_c \leq -B_{sat}/\mu_c \end{cases} \quad (4.5)$$

Where, a typical B_{sat} for ferrite cores is between 0.3 and 0.5 Tesla. In our designs, however, peak flux will be limited far below this value by core loss considerations.

From (4.2), (4.3), (4.4) and (4.5) we can get that

$$\varphi_c = \frac{Ni}{l_c/\mu_c A_c} = \frac{Ni}{R_c} \quad (4.6)$$

Where, $R_c = l_c/\mu_c A_c$ is the magnetic reluctance.

Similarly, the reluctance of the gap in Fig 4.4 is $R_g = l_g/\mu_0 A_g$. Where, l_g is the length of the gap and μ_0 is the permeability of free space, which equals$4\pi * 10^{-7}\ {}^{H}/_{m}$. We also assume that the cross sectional area of the gap A_g is equal to the cross sectional area of the core A_c, even though the magnetic flux lines bend outwards (fringing) increasing the effective cross sectional area of the gap. And by taking into account the gap in our E core we can re-write (4.6) as:

$$\varphi_c = \frac{Ni}{l_c/\mu_c A_c + l_g/\mu_0 A_g} = \frac{Ni}{l_c/\mu_c A_c + l_g/\mu_0 A_c} = \frac{Ni}{R_c + R_g} \quad (4.7)$$

The magnetic circuit model illustrated in Fig 4.4 is analogous to an electric circuit model. Where the magnetic flux φ_c is the current, the magneto motive force is the emf of a voltage source, and the magnetic reluctance R_c is the resistance. Hence, we can derive ohm's law for the magnetic circuit in Fig. 4.4:

$$V = IR \quad \leftrightarrow \quad Ni = \varphi_c(R_g + R_c)$$

We can use the relationships above along with Faraday's law to figure what gap length we need to achieve the inductance value we want. Faraday's law tells us that we can induce voltage in a in the inductor windings by changing the total flux φ_c which passes through the core cross sectional area.

$$v(t) = \frac{d\varphi_c(t)}{dt}$$

Substituting in (4.6), (4.3), and (4.5) and including the effect of multiple turns we get:

$$v_{inductor}(t) = NA_c\frac{dB_c(t)}{dt} = N\mu_c A_c\frac{dH_c(t)}{dt} = N\mu_c A_c\frac{dH_c(t)}{dt} = \frac{N^2\mu_c A_c}{l_c}\frac{di(t)}{dt} \qquad (4.8)$$

And since the inductance of an inductor relates the voltage across the windings of the inductor to the change in the current through the winding we conclude that

$$L = \frac{N^2\mu_c A_c}{l_c} = \frac{N^2}{l_c/\mu_c A_c} = \frac{N^2}{R_c} \qquad (4.9)$$

Including the effect of the gap and the relative permeability μ_r into (4.9) to get

$$L = \frac{N^2}{R_c + R_g} = \frac{N^2}{l_c/\mu_r\mu_0 A_c + l_g/\mu_0 A_c} \qquad (4.10)$$

Rearranging (4.10) and solving for l_g in terms of L, we get

$$l_g = \frac{N^2\mu_0 A_c}{L} - \frac{l_c}{\mu_r} \qquad (4.11)$$

4.3 Magnetic Flux Density

Before we can calculate the peak magnetic field through the core of the inductor --since we are analyzing a gapped inductor-- we need to include the effect of the gap in the value of the

core permeability. In other words, we need to find the effective permeability. To find the effective permeability we need to understand the effect of air gap on the inductor.

The magnetic permeability of the material is related to the slope of the B-H cure, expressed in (4.5). Increasing the air gap decreases the inductance, increases the saturation current, reduces the slope of the B-H curve, reduces the dependence of inductance on core material, and reduces the changes due to variations in flux density, temperature, bias, etc.

We can derive the effective permeability by using the magnetic reluctance concept and assuming a constant cross sectional area, a gap length that is much smaller than the effective core length, a core permeability that is larger than the permeability of the gap, and a negligible fringing effect [23].

$$\mu_e = \frac{\mu_r}{1 + \frac{\mu_r l_g}{l_c}} \qquad (4.12)$$

The effective permeability can be calculated for non-uniform and multi-path magnetic circuits as well [23]. We can now use (4.4) and (4.6) to calculate the peak magnetic flux density in the inductor.

$$B_{pk} = \frac{\mu_e \mu_o N I_{pk}}{l_c} \qquad (4.13)$$

Where, I_{pk} is the peak inductor current and B_{pk} is the peak flux density in the core.

4.4 Inductor Losses

At low frequency, the magnetic devices have two loss mechanisms: DC copper loss and core loss. At high frequency magnetic devices have extra losses because of the eddy currents in the windings. This section examines the losses at high frequency for an E core inductor with planar or Litz windings. Similar analysis can be used for other inductor designs.

4.4.1 Core Losses

Since, it is hard to obtain a theoretical model for core loss; the most effective way to obtain core losses is through measurements or through use of data (such as "Steinmetz parameters" or core loss curves as provided by the core manufacturer). Gradzki in [21]

summarizes measurement methods and develops core loss models that can be adopted to characterize core losses.

Core loss curves are often provided by the manufacturer in the form of a curve of the power loss density in kW/m^3or mW/cm^3vs. the magnetic flux density in milli Tesla or Gauss. The plot includes curves at different frequencies. Usually within the frequencies which the material performs best. Fig 4.5 below illustrates the core loss curves of 3F4 – one that we are considering for our design-- material from Ferroxcube. The plot shows typical data values, the maximum core losses maybe larger.

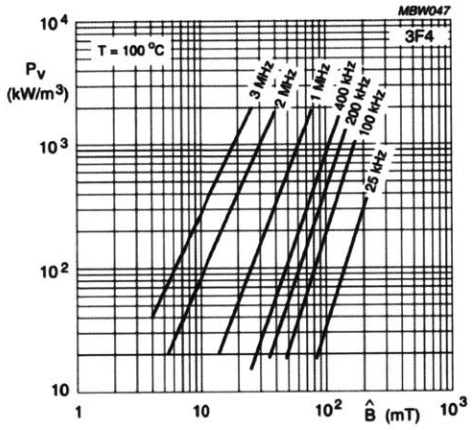

Fig 4.5 Specific power loss as a function of peak flux density with frequency as a parameter [24]

Different materials have different losses at different frequencies. And when the manufacturer doesn't provide data about the material losses, the materials need to be measured to obtain a good model for the materials losses. Hanson and Belk [25] characterized losses on magnetic cores driven between 2-20 MHz under high flux density conditions. The results could be applied to estimate the achievable performance of cored magnetics across frequency.

The "Performance Factor", examined below in Fig 4.6 is an approximate measure of the ability of a core material to process power vs. frequency. Due to winding area and winding loss we can imagine that for a fixed core size there is a limit on $N \cdot I$ (Ampere-turns) that can be applied, so we can treat $N \cdot I$ as fixed. We know that the voltage amplitude is $N \cdot B \cdot f \cdot A_c$, where B is the core flux density and f is the operating frequency. And since the reactive power handled is proportional $|Voltage| \cdot |Current|$, $N \cdot I$ is proportional to $B \cdot f$ (for a fixed $N \cdot I$). While the performance factor is only a rough measurement it is useful for comparing core materials.

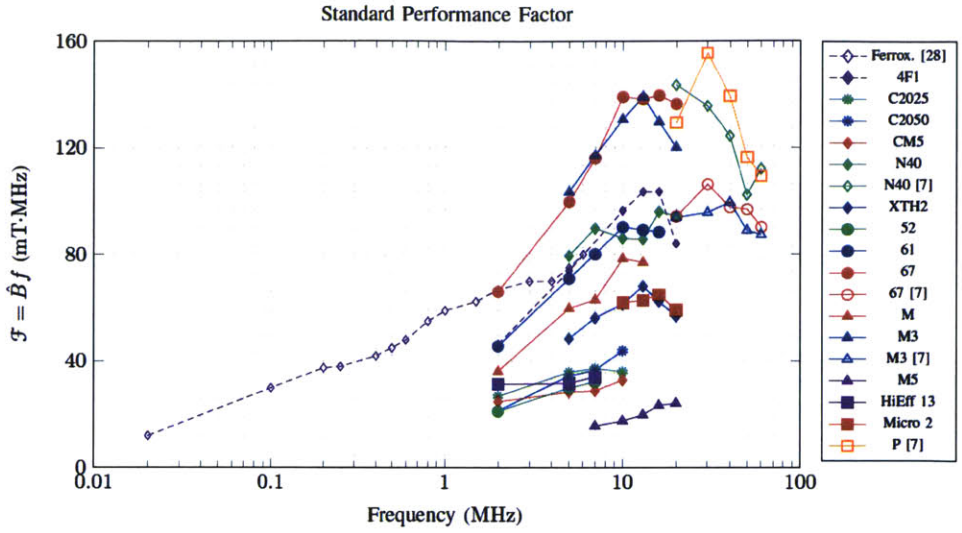

Fig 4.6 illustrates the performance factor for many materials at 500 mW/cm^3[25]

Fig 4.6 above from [25] illustrates the performance factor for many materials at a given allowed loss level to understand the relative performance. We could use Fig 4.6 to figure out the best performing materials at set frequencies. For instance, the best performing materials between 2 to10 MHz are F67 and M3.

We can write an equation for core loss density using the curves in Fig 4.5; this is known as the "Steinmetz Equation", after Charles Proteus Steinmetz who developed this model. (Some versions also include frequency to a power, but we simply adopt K as a frequency-dependent constant):

$$P_{core} = KB_{pk}{}^{y}V_c \quad (4.14)$$

Where,

- **K:** a constant from a curve fitting. Value dependent on frequency and come material. Units: W/(T*m^3) (watts per tesla per unit volume in meters cubed)
- $\boldsymbol{V_c}$: Effective volume of the magnetic core in m^3 (meters cubed)
- $\boldsymbol{y}$: a constant from a curve fitting. Value dependent on frequency and come material. (unitless)

Equation (4.14) above is a fit to empirical data, from material data sheets and also shown in [25]. Note that different materials have different K and y values at different operating frequencies. The data for K

and y can be obtained from Fig 4.5 above. Then a mathematical expression can be obtained by curve fitting. This representation doesn't include the effects of ambient temperature on core loss density.

4.4.2 Winding Losses

When operating at high-frequencies, losses due to eddy currents in the windings should not be ignored. Those losses can be attributed to the skin effect and proximity effect.

When we have a sinusoidal current, the current density (the cross sectional area which current passes through) exponentially decays as a function of distance through the conductor. This is known as the skin effect. In other words, the current in the conductor is distributed such that the current density is largest on the surface of the conductor and decreases as we get close to the center. This results in higher resistance in the conductor at high frequencies and higher losses as well.

We can calculate the skin effect factor $\Delta(n)$ at every harmonic frequency in the wave form, shown in (4.15). The skin effect factor is the ratio between the thickness of the conductor to the skin depth of the material at a specific frequency.

$$\Delta(n) = copper\ thickness * \sqrt{\frac{n\omega_o\mu_o}{2\rho}} \qquad (4.15)$$

Where,

- ***copper thickness:*** The thickness of the conductor in m (meters).
- $\boldsymbol{\omega_o}$: The operating frequency in radians. Equal to 2πf, with f in hertz.
- $\boldsymbol{\rho}$: Copper resistivity equals $2.5 * 10^{-8}\ \Omega m$ (ohms times meters) at 125 °C.

Moreover, Ac currents in conductors induce eddy currents in nearby conductors due to the proximity effect. In inductors, the proximity effect results in higher winding losses which cannot be ignored. Dowell in [26] developed a one-dimensional model that takes account of both the skin and proximity effects based on the skin effect factor and the number of winding layers. This model is also utilized and verified by Hurley in [28].

To calculate the total winding loss, we calculate the DC losses using the average current and dc resistance, and the AC losses using the ac resistance at each frequency and losses over all harmonic components:

$$P_{wind} = {I_{avg}}^2 R_{dc} + \frac{1}{2}\sum_{n=1}^{\infty} {I_n}^2 R_{dc} \frac{R_{ac}(n)}{R_{dc}} \quad (4.16)$$

Where,

$\boldsymbol{I_{avg}}$: average inductor current in A. (amperes)

$\boldsymbol{R_{dc}}$: dc resistance of the copper winding in Ω (ohms).

n: The harmonic number

$\boldsymbol{I_n}$: The amplitude of the nth harmonic in A (amperes).

To calculate the ratio of Rac to Rdc, we utilize Dowell's equation as described in equation (4.17). Dowell's equation accounts for skin effect (left side term of (4.17)) and proximity effect (right side term of (4.17)), where M is the number of winding layers:

$$\frac{R_{ac}(n)}{R_{dc}} = \Delta(n)\left[\frac{\sinh(2\Delta(n)) + \sin(2\Delta(n))}{\cosh(2\Delta(n)) - \cos(2\Delta(n))} + \frac{2}{3}(\mathrm{M}^2 - 1)\frac{\sinh(\Delta(n)) - \sin(\Delta(n))}{\cosh(\Delta(n)) + \cos(\Delta(n))}\right] \quad (4.17)$$

The dc resistance, Rdc, in a planar inductor is calculated per layer and summed as series connected resistors for all layers connected in series.

$$R_{dc} = \sum_{i=layer}^{\#\ layers} \rho \frac{4{N_{l_i}}^2 (OD + W_{core})}{(OD - ID) * copper\ thickness} \quad (4.18)$$

Where,

$\boldsymbol{N_{l_i}}$***:*** Number of turns on the ith layer

***OD*:** Outer diameter of the magnetic core (m)

ID: Inner diameter of the magnetic core (m)

$\boldsymbol{W_{core}}$**:** Width of the core posts (m)

Fig 4.7 below shows the core dimensions OD, ID and Wcore used to calculate Rdc.

Instead of using rectangular planar winding we can use litz wire to try and decrease the winding losses. Dowell's model was developed for rectangular conductors. When using litz wire, Dowell's model should be modified [22]. The equation of Rac to Rdc becomes:

$$\frac{R_{ac}(n)}{R_{dc}} = \Delta(n)\left[\frac{\sinh(2\Delta(n)) + \sin(2\Delta(n))}{\cosh(2\Delta(n)) - \cos(2\Delta(n))} + \frac{2}{3}(M_L{}^2 N_s - 1)\frac{\sinh(\Delta(n)) - \sin(\Delta(n))}{\cosh(\Delta(n)) + \cos(\Delta(n))}\right] \quad (4.19)$$

Where,

- M_L is the number of litz wire layers in one partition
- N_s is the number of strands in the litz wire.

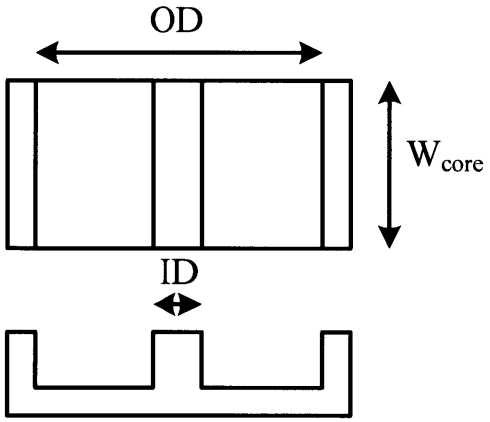

Fig 4.7. Planar core geometry and relevant dimensions for calculating Rdc.

4.4.3 Temperature Rise

The temperature rise in the inductor is roughly proportional to the total power loss and roughly inversely proportional to the surface area of the core. One can use the thermal resistance of the core provided by the manufacturer to calculate the temperature rise. Alternatively, more empirical models can be used to approximate temperature rise. For example, for our calculation we use equation (4.20) below which is adopted from Micrometals [27].

$$T_{rise}(°C) = \left[\frac{Power\ Dissipation(milliwatts)}{Surface\ Area\ (cm^2)}\right]^{0.833} \qquad (4.20)$$

4.5 Application Design

Now that we explored the important parameters that we need to consider when designing an inductor. We can use an algorithm to help us run through all possible designs and identify the successful ones. We can eliminate a design if it violates any of the limitation we choose. Fig 4.8 below illustrates a flow chart of the inductor design algorithms. Furthermore, this section also goes through all the calculations for our specific design of interest. The code utilized for calculations in this thesis is provided in Appendix A.

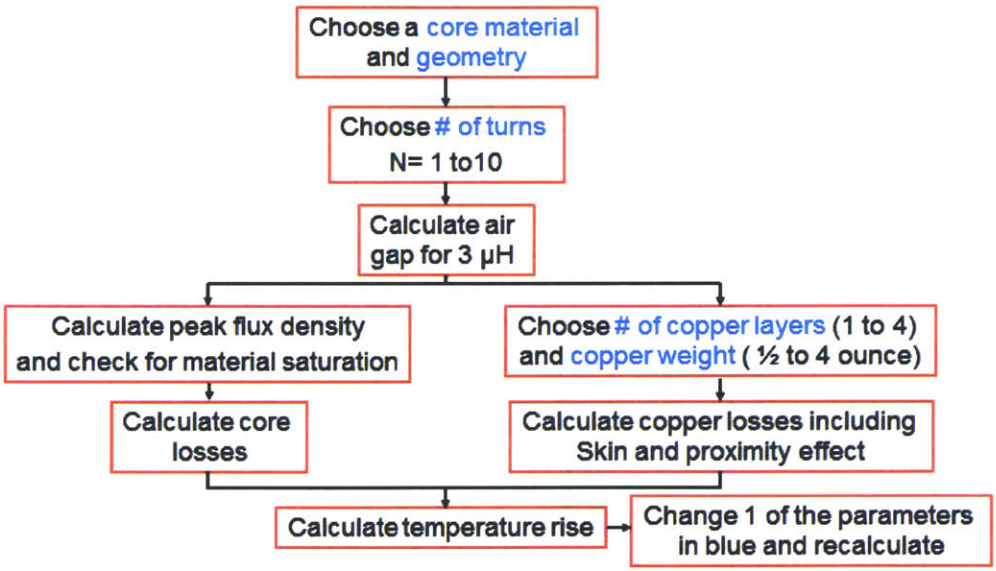

Fig 4.8 illustrates a flow chart of the developed code that calculates total inductor losses and temperature rise for different core materials, geometries, gaps and turn configurations

The algorithm first chooses a specific core material and geometry. It then iterates through possible number of turns, for our design we choose 10 as the maximum number of turns. The algorithm then calculates the size of the air gap needed to get $3\mu H$. It then calculates the peak flux and the core losses. The code also chooses the optimal number of layers (maximum number of layers is 4) and copper thickness that would give us the smallest winding losses including the skin and proximity effects. After calculating the losses the code calculates the temperature rise.

The code eliminates:

- Designs that have an air gap larger than half the height of the center post.
- Designs that have a B-field larger than $B_{max} = 0.3\ T$.
- Designs that have a temperature rise larger than $T_{max} = 60\ °C$.

For our design of interest we considered the following:

- **Core Material:** 3F4, F-67, 3F45, 4F1.

  These materials had a "high performance factor (B*f)" at our frequencies of interest 1-5 MHz [24][25].
- **Inductor Geometries:** EILP Cores, EQ cores, Planar E Cores.
- **Copper Thickness:** 0.5 ounce to 4 ounce copper.

Table 4.1 below shows the results we got by running the code using the limitations and considerations listed above.

Material	Copper Thickness	Core Geometry	Turns	Layers	Core Loss	Winding Loss	Total Loss	Temperature rise
	ounce		turn	Layer	W	W	W	deg C
F67	2	EILP22/6/16	8	4	1.98	2.55	4.53	58
F67	2	EILP32/6/20	7	4	1.7799	1.8352	3.6151	33.22
F67	2	E22	8	4	1.91	2.62	4.53	57.75
F67	2	E32	10	4	3.0198	3.7569	6.7767	56.34
3F4	2	EILP22/6/16	7	4	1.1952	2.0752	3.2704	47.986
3F4	2	EILP32/6/20	5	4	1.6811	0.98817	2.6698	27.676
3F4	2	EQ25	7	4	1.2483	1.8144	3.06	36.62
3F4	2	EQ30	7	4	1.2133	1.49	2.71	28.03
3F45	1	EILP22/6/16	7	4	0.59432	2.669	3.2633	47.985
3F45	1	EILP32/6/20	5	4	0.85209	1.2709	2.123	23.772
3F45	2	EILP22/6/16	7	4	0.59432	2.0752	2.67	36.6163
3F45	2	EILP32/6/20	5	4	0.85209	0.988	1.84	22.983
3F45	2	EQ25	7	4	0.63809	1.8144	2.45	30.43515
3F45	2	EQ30	6	4	0.94	1.15	2.08	22.55
4F1	2	E38	6	4	4.9428	1.4561	6.3989	32.0066825

Table 4.1 illustrates the results we got when trying to design a 3 μH using the algorithm illustrated in Fig 4.8. The analysis uses the limitations and considerations listed above. The table lists the smallest cores that passed.

Furthermore, table 4.2 below lists the dimensions of all EQ, EILP, and PlanarE cores that were considered in the calculation. It also lists the inductors box volume with and without traces and how much percentage it takes of 4.8 in^3 (Our converter design target volume).

Core Name	height	width	length	inner diameter	outer diameter	box volume	Percentage of 4.8 in3 Without trace	Box volume (with tracks)	Percentage of 4.8 in3 With trace
	mm	mm	mm	mm	mm	mm^3	%	mm^3	%
EILP									
EILP14/3.5/5	5	5	14	3	11	350	0.444726811	910	1.156289708
EILP18/4/10	6	10	18	4	14	1080	1.372299873	2160	2.744599746
EILP22/6/16	8.2	15.8	21.8	5	16.8	2824.408	3.588828463	4933.776	6.269092757
EILP32/6/20	9.5	20.35	31.75	6.35	25.4	6138.06875	7.799324968	11884.025	15.10041296
EILP38/8/25	12.05	25.4	38.1	7.6	30.8	11661.267	14.81736595	22312.503	28.35133799
EILP43/10/28	13.6	27.9	43.2	8.1	35.4	16391.808	20.82821855	32431.104	41.20851842
Planar E									
E14	5	5	14	3	11	350	0.444726811	910	1.156289708
E18	6	10	18	4	14	1080	1.372299873	2160	2.744599746
E22	8.2	15.8	21.8	5	16.8	2824.408	3.588828463	4933.776	6.269092757
E32	21.6	9.5	32	9.5	22.7	6566.4	8.343583227	15690.24	19.93677255
E38	12.07	25.4	38.1	7.6	30.23	11680.6218	14.84195909	22087.41201	28.06532657
E43	13.6	27.9	43.2	8.1	34.7	16391.808	20.82821855	32019.84	40.68594663
E58	14.6	38.1	58.4	8.1	50	32485.584	41.27774333	68211.2	86.67242694
E64	15.28	50.8	64	10.2	53.8	49678.336	63.1236798	92315.648	117.3006963
EQ									
EQ13	3.95	8.7	12.8	5	11.2	439.872	0.55892249	566.272	0.719532402
EQ20	8.6	14	20	8.8	18	2408	3.059720457	3096	3.933926302
EQ25	10.85	18	25	11	22	4882.5	6.203939009	5967.5	7.582592122
EQ30	10.7	20	30	11	26	6420	8.157560356	8346	10.60482846
EQ38	10.7	25.4	38.1	14	33.1	10354.818	13.1573291	13493.877	17.14596823

Table 4. 2 shows the dimensions of all cores considered for our calculation. The information was extracted from the manufacturer's data sheets. Also listed in [24]

Next we go through an example calculation. We use the geometry EILP22/6/16 with 3F4 material:

1- Calculate the center post gap length:

$$l_g = \frac{N^2 \mu_o A_e}{L} - \frac{l_e}{\mu_r} = \frac{7^2 * 4\pi * 10^{-7} * 78.5 * 10^{-6}}{3 * 10^{-6}} - \frac{26.1 * 10^{-3}}{770} = 0.0015773\ m$$

2- Calculate the effective permeability:

$$\mu_e = \frac{\mu_r}{1 + \frac{\mu_r l_g}{l_e}} = \frac{770}{1 + \frac{770 * 0.0015773}{26.1 * 10^{-3}}} = 16.199\ H/m$$

3- Calculate the peak magnetic field:

$$B_{pk} = \frac{\mu_e \mu_o N I_{pk}}{l_e} = \frac{16.199 * 4\pi * 10^{-7} * 7 * 9.08}{26.1 * 10^{-3}} = 0.049572\ Tesla$$

4- Calculate the core loss:

$$P_{core} = K {B_{pk}}^y V_c = 0.0138 * 49.72^{2.7287} * 2050 * 10^{-3} = 1.1952\ Watts$$

5- Calculate winding/copper loss:

a. Calculate the skin effect factor:

$$\Delta(n) = copper\ thickness * \sqrt{\frac{n\omega_o \mu_o}{2\rho}}$$

$$= 0.07 * 10^{-3} * \sqrt{\frac{2\pi * 1.3 * 10^6 * 4\pi * 10^{-7}}{2 * 2.5 * 10^{-8}}} * [\sqrt{1}, \sqrt{2}, \ldots, \sqrt{9}, \sqrt{10}]$$

$$= [1.003, 1.418, 1.737, 2.0059, 2.2427, 2.4567, 2.6536, 2.837, 3.0089, 3.1716]$$

b. Calculate the dc resistance:

$$R_{dc} = \sum_{i=layer}^{\#\ layers} \rho \frac{4{N_{l_i}}^2 (OD + W_{core})}{(OD - ID) * copper\ thickness}$$

$$= 3 * \left[2.5 * 10^{-8} \frac{4 * 2^2 * (16.8 * 10^{-3} + 15 * 10^{-3})}{(15 * 10^{-3} - 5 * 10^{-3}) * 0.07 * 10^{-3}}\right] + 2.5 * 10^{-8} \frac{4 * 1^2 * (16.8 * 10^{-3} + 15 * 10^{-3})}{(15 * 10^{-3} - 5 * 10^{-3}) * 0.07 * 10^{-3}}$$

$$= 0.0591\ \Omega \text{ (Note: Turns per layer: 2,2,2,1)}$$

c. Calculate the ratio of Rac to Rdc,:

$$\frac{R_{ac}(n)}{R_{dc}} = \Delta(n)\left[\frac{\sinh(2\Delta(n)) + \sin(2\Delta(n))}{\cosh(2\Delta(n)) - \cos(2\Delta(n))} + \frac{2}{3}(\mathrm{M}^2 - 1)\frac{\sinh(\Delta(n)) - \sin(\Delta(n))}{\cosh(\Delta(n)) + \cos(\Delta(n))}\right]$$

$$= [1.003 * \left(\frac{\sinh(2 * 1.003) + \sin(2 * 1.003)}{\cosh(2 * 1.003) - \cos(2 * 1.003)} + \frac{2}{3}(4^2 - 1)\frac{\sinh(1.003) - \sin(1.003)}{\cosh(1.003) + \cos(1.003)}\right), \ldots,$$

$$3.1716 * \left(\frac{\sinh(2 * 3.1716) + \sin(2 * 3.1716)}{\cosh(2 * 3.1716) - \cos(2 * 3.1716)} + \frac{2}{3}(4^2 - 1)\frac{\sinh(3.1716) - \sin(3.1716)}{\cosh(3.1716) + \cos(3.1716)}\right)]$$

$$= [2.707, 7.1045, 12.7073, 18.2655, 23.166, 27.2657, 30.642, 33.4324, 35.7657, 37.7662]$$

d. Calculate the winding loss:

$I_n = [\,3.9064;\ 0.6779;\ 0.2203;\ 0.2458;\ 0.0288;\ 0.093;\ 0.0527;\ 0.0373;\ 0.0669;\ 0.0291]$

$R_{dc}\frac{R_{ac}(n)}{R_{dc}} = [0.16, 0.4199, 0.7510, 1.0795, 1.0795, 1.3691, 1.6114, 1.8109, 1.9759, 2.1138, 2.2320]$

$$P_{wind} = 4.246^2 * 0.0591 + \frac{1}{2}\sum_{n=1}^{\infty} {I_n}^2 R_{dc}\frac{R_{ac}(n)}{R_{dc}} = 2.075\ Watts$$

6- Calculate temperature rise:

$$T_{rise} = \left[\frac{0.55 * (P_{core} + P_{wind})}{Surface\ Area}\right]^{0.833} = \left[\frac{0.55 * 3.2704 * 10^3}{17.28}\right]^{0.833} = 47.986°C$$

4.5.1 Experimental Results

Table 4.3 below shows the results of testing an E32/6/20 core in 3F4 material with 5 turns using 40 AWG litz wire with 100 strands. The legs of the inductor all have a gap of 1.4 mm. The measured inductance of the inductor at 1.3 MHz is $3.145\mu H$ and the measured resistance is 0.88 *ohms*. The first 3 rows show the converters operation points over a line cycle. Those can be used to calculate the average losses. The rests are for different operating points at 186 V and 150V input.

Input Current	Input Voltage	Output Current	Output Voltage	Input Power	Output Power	Power loss	Efficiency	Temperature Rise	Frequency
A	V	A	V	W	W	W	%	°C	MHz
1.114	126.54	2.028	67.949	140.96556	137.80	3.16	97.754	11	1.6
1.248	142.63	2.549	68.138	178.00224	173.68	4.32	97.573	44	1.535
1.569	179.39	3.969	68.583	281.46291	272.21	9.26	96.711	54	1.237
1.65	185.99	4.33	68.769	306.8835	297.77	9.11	97.030	56	1.23
0.89	186.21	2.338	68.096	165.7269	159.21	6.52	96.066	48	1.875
2.079	149.5	4.416	68.79	310.8105	303.78	7.03	97.736	48.5	1.074
1.399	149.73	2.996	68.243	209.47227	204.46	5.02	97.605	44	1.422
0.699	149.92	1.489	67.669	104.79408	100.76	4.03	96.149	20	2.173

Table 4.3 shows the results of testing an E32/6/20 core 3F4 material with 5 turns and 40/100 litz wire

From table 4.3 above we notice an efficiency value between 96% and 97.75%. The converter tends to be less efficient at low power operating points. The efficiency at full power (300W) is around 97.03%, with 7 watts of total loss. The operating frequency also ranged between 2.173 MHz at low power and 1.23MHz at high power. Moreover, the measured peak inductor temperature rise at 300W was 56°C. while our model expected to get a 27.1°C temperature rise, 1 W winding loss, and 1.7 W core loss, and 2.7 W total power loss, results shown in table 4.1. We notice a difference of 6 W between our predicted value and our measured value of 9 W at 300 W. And we notice a 29°C difference between the predicted and measured value.

To further understand the losses in the inductor, a similar inductor was built using 200 strands of 40 AWG litz wire. The measured inductance value of the inductor at 1.3 MHz was $3.109\mu H$and the measured resistance was 0.78 *ohms*. Table 4.4 below shows the results of the experiment.

We notice in table 4.4 below that the efficiency improved at most operating points. The efficiency ranged between 97.97% and 96%. The converter had an efficiency of 97.06% at full power (300 W). The operating frequencies showed similar values as listed in table 4.3 above. The thermal response was also slightly better, showing up to around a couple degrees less temperature rise.

Furthermore, table 4.4 below allows us to understand how accurate is our developed model and calculation of inductor losses. Table 4.1 tells us that for E32/20/6 core with 3F4 material has a winding loss of 0.98817 W. We suspect that if we were to double the number of strands in the inductor winding we would decrease the winding loss by 0.49W. And from tables 4.3 and 4.4 we found that at full power (300W) our losses dropped by 0.42W. Even though, the calculation was meant for planar windings, the losses were close. This also leads us to suspect that the source of the difference between the predicted losses and the measured losses is the core loss.

Input Voltage	Output Current	Output Voltage	Input Power	Output Power	Power loss	Efficiency	Temperature Rise
V	A	V	W	W	W	%	°C
126.54	2.02	67.999	140.20632	137.35798	2.84834	97.96846533	11
146.62	2.617	68.237	183.12838	178.576229	4.552151	97.51422963	40
179.85	3.961	68.616	280.2063	271.787976	8.418324	96.99566926	56
185.58	4.305	68.788	305.09352	296.13234	8.96118	97.06280881	57
185.9	2.367	68.083	167.8677	161.152461	6.715239	95.99968368	48
149.69	4.304	68.821	302.82287	296.205584	6.617286	97.81479979	46
149.86	2.986	68.289	208.90484	203.910954	4.993886	97.60949244	44
149.88	1.486	67.711	104.61624	100.618546	3.997694	96.1787061	20

Table 4.4 shows the results of testing an E32/6/20 core 3F4 material with 5 turns and 40/200 litz wire

Chapter 5

High Density High Efficiency Telecom Converters

5.1 Background and Motivations

This chapter presents a study on high density high efficiency telecom brick converters for use as elements of the second stage in a proposed power factor corrected power supply architecture (e.g., as illustrated in Fig. 5.1, repeated from chapter 2). The proposed architecture has the PFC stage with output(s) at a nominal value of 72 V, within the voltage range of typical telecom "brick" converters. These converters can also operate down to lower voltages (e.g., 18 or 36 V) providing plenty of headroom for discharging the energy buffer capacitor for holdup thereby reducing capacitor size. Those will be used for the second stage in our architecture of interest, repeated below.

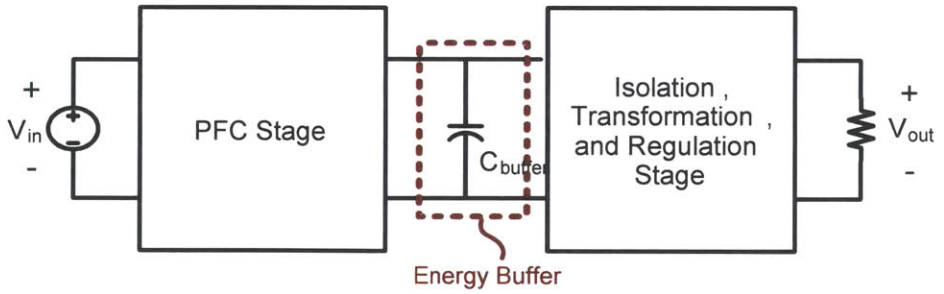

Fig 5.1a Two-stage grid interface power converter with a first power-factor correction (PFC) stage, an intermediate energy buffer, and a second is a dc/dc isolation/transformation and regulation stage.

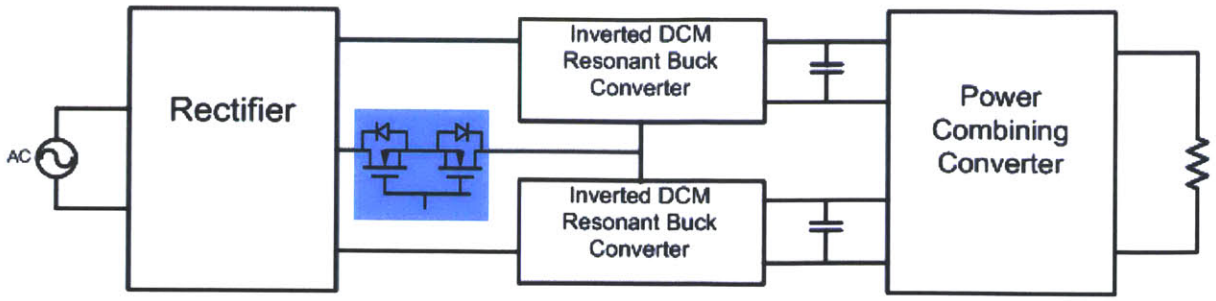

Fig 5.1b represents the topology of our high-frequency PFC system. The first stage is comprised of a full bridge rectifier and a configuration switch. When the input voltage is low, the switch allows the input stage to act as a voltage doubler. The two parallel buck converters function as a soft-switched HF power stage. The power combining stage combines the output energy from the two buck converters.

While Fig 5.1b shows two parallel buck converters acting as the soft-switched HF power stage and using 80V capacitors for energy buffering. The buck converters can be re arranged in series to for stacked output that uses 160V capacitor as an energy buffer at the input of the second stage.

Our discussion in previous chapters explored the possibility of using a buck PFC configuration to step down the line voltage in the first stage, and using either 80V or 160V capacitors to buffer and store energy (at 72V and 143V respectively).

The advantage of using the architecture shown above in Fig 5.1 is that we can use the high efficiency and high energy density brick converters to realize the second stage (for voltage transformation, isolation, and post regulation. One can easily change the output voltage for a given PFC architecture by selecting different second stage converters. Moreover, the 2:1 or 4:1 input range typically available with telecom brick converters enables substantial discharge of the energy buffer capacitor during holdup events, helping to minimize the energy buffer capacitor size.

5.2 Converter Selection

For the proposed architecture the second stage converter, the isolation, transformation and regulation stage from Fig 5.1, can be realized using a pair of conventional high-density telecom "brick" converters. One can use two 24V output converters connected in parallel or two 12V output converters connected in series. Tables 5.1 and 5.2 list the best of such converters from different manufacturers, sampled from those on the market as evaluated by the author during 2015. Converters are rated for input voltage ranges of either 18-75 V or 36-75 V. The

tables would allow us to get a sense of volume and efficiency tradeoffs. Converters that have a 4:1 discharge ratio are less efficient than converters that have a 2:1 discharge ratio.

The tables below also list the efficiency of the converters at a target rated power of 120W. Appendix B lists more high efficiency converters.

Manufacturer	Part Number	Rated Power (W)	Volume (in3)	Power Density (W/in3)	Efficiency at 75 V and 120W Power	Output DC Voltage
SynQor	IQ36240QTx05	120	1.8324	65.49	89%	24
Ericsson	PKB 5113W PI	120	0.8073	148.64	90%	12
Power-One	UIE48T10120	120	0.9068	132.34	91%	12
Delta Electronics	Q36SR12017	204	1.6675	122.34	91%	12
General Electric	EHHD010A0B	120	0.7245	165.63	90%	12
Murata	UNE-12/10-Q48-C	120	0.8073	148.64	90%	12

Table 5.1 High-Power Density Standard Telecom Converters with input voltage of 75-18 V.

Manufacturer	Part Number	Max Power (W)	Volume (in3)	Max Power Density (W/in3)	Power Density @ 120 W (W/in3)	Usable Power at 60C (W)	Efficiency at 75 V and 120W	Output DC Voltage
SynQor	SQ60120ETA20	240	1.03086	232.815	116.4	156	93.5%	12
General Electric	EBVW020A0B	240	0.91	263.74	131.86	180	93.7%	12
Murata	RBE-12/20-D48NB-C	240	0.828	289.855	144.93	204	92.5%	12
Delta Electronics	E48SH12010	120	0.7659	156.678	156.67	111	92.5%	12

Table 5.2 lists highest efficiency and highest energy density 72-36V input range and 12V output. Two of these will be stacked with inputs stacked in series across the 160V capacitor (with active voltage balancing provided at the converter inputs by a balancer circuit). These have been chosen from the more comprehensive table 13 below to match our project specification. Note that the usable power is calculated at 100 LFM (0.5 m/s) except for Ericsson which is calculated at 200 LFM (1 m/s).

The next section shows the experimental results for two converters.

5.3 Experimental Results

This section tests the top two converters listed in table 5.2 above. Namely SynQor's SQ60120ETA and General Electric's EBVW020A0B The efficiency and temperature rise is measured at different operating points for the two converters. The Figures below show the results.

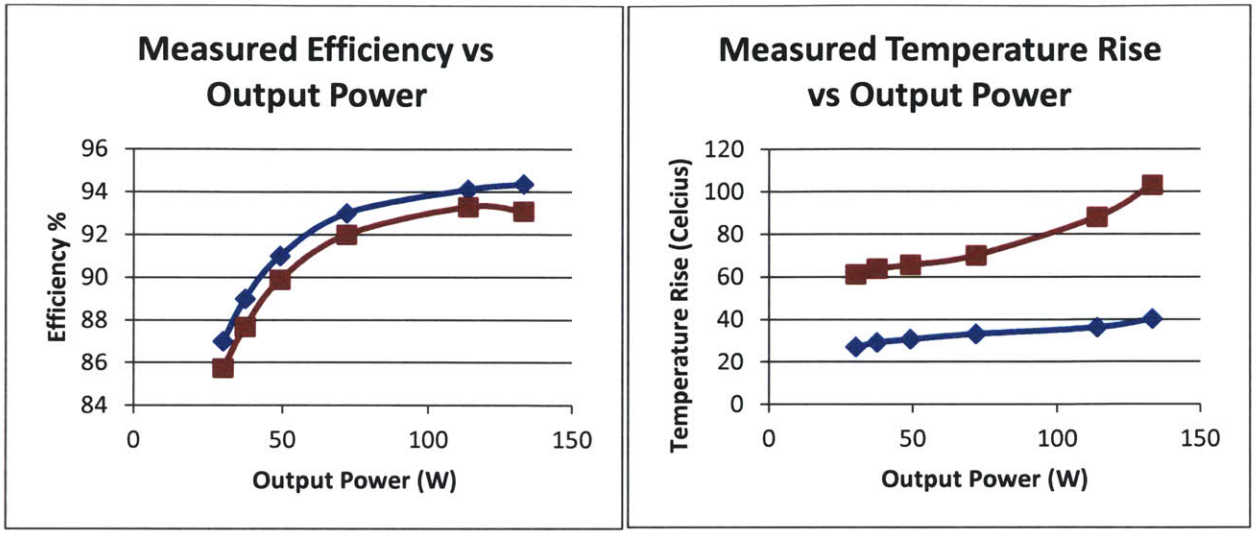

Fig 5.2 shows the experimental results for efficiency and temperature rise for the SynQor SQ60120ETA Converter. The red line shows the results of operation under 0 LFM. And the blue line shows the results of operation under 200 LFM

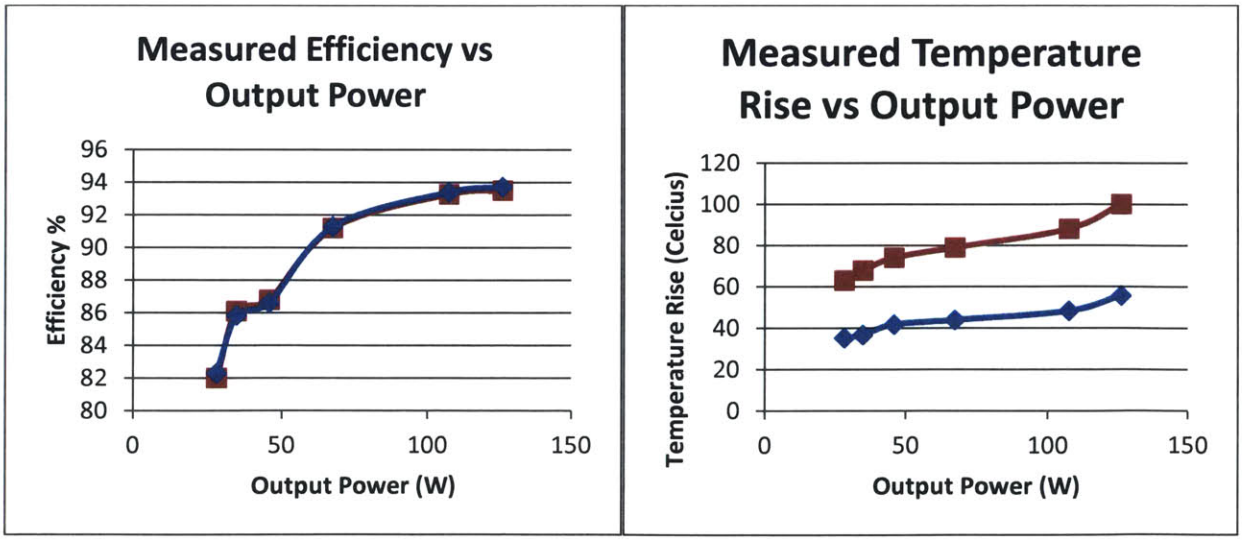

Fig 5.3 shows the experimental results for efficiency and temperature rise for the GE EBVW020A0B Converter. The red line shows the results of operation under 0 LFM. And the blue line shows the results of operation under 200 LFM

In conclusion, both converters showed high efficiency ~93.5% at 120W output power. The efficiency of the SynQor converter dropped by ~1.5% when the converter was tested with no air flow in comparison to 200 LFM. The GE converter had almost the same efficiency when tested with no air flow and when tested under 200 LFM. Both converters reached a maximum of 100 degrees while running at 120W output with no airflow. But overall, the SynQor converter had a better overall thermal response.

Chapter 6

System Testing

6.1 Zener Bank Load

This section describes the design and implementation of a zener bank load that can handle up to 600 Watts, 9 Amps at a nominal voltage of 72V. This load will be used as a test bench to test the output of the resonant transition buck converter. Fig 6.1 below illustrates the circuit topology of the design.

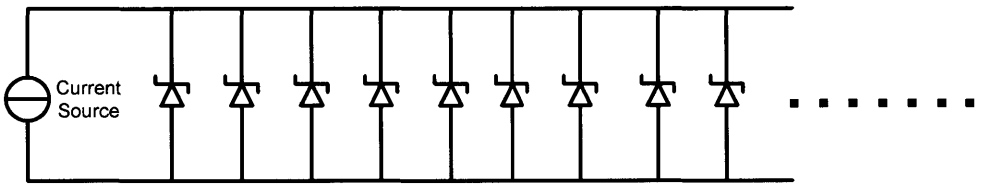

Fig 6.1 illustrates the circuit topology of the zener bank load

6.1.1 Modeling and Analysis

In LT Spice the zener diode was modeled using a voltage source and a resistor in series. The voltage source had a value of 68V at 0.18 A and the value of the resistance was 8 ohms at 0.18A. The model took into consideration the effects of temperature and voltage tolerance on the zener voltage. The voltage tolerance for the devices used is +/-5% and the temperature coefficient is 0.09%/°C.

The model used assumes that temperature and tolerance affect only the zener knee voltage and not the device impedance. In other words, the slope of the device's iv-curve does not change due to temperature and tolerance. The temperature affect is calculated via:

$$V_z = \frac{\propto V_{z_0}(\Delta T)}{100} + V_{z_0} \quad (6.1)$$

Where V_{Z_0} is the voltage calculated at zero current (knee voltage) using the zener voltage and impedance given at 0.18A. And ΔT is the temperature difference from T_A = 30 C. Now that we have a model for the load we need to figure out the number (if any) of zeners that we need use in parallel such that we can insure that the power dissipated by each zener is under the maximum rated power for the zeners (~50W) when including the effects of temperature and voltage tolerance.

For example, if we were to use 24 zeners in parallel, half of which have -5% variation from nominal and the other half have +5% variation from nominal with the temperature rising from 35C to 75C, the design will succeed up to 8A of input current. We would need 26 devices to handle up to 9 A.

Also, more devices in parallel decreases the amount of power each device is required to handle. With 40 devices the maximum power to be handled by one device (taking into consideration temperature and tolerance effects) is less than 30 W.

6.1.2 Heat Sink

Analyzing the load's thermal model is important for choosing the proper heat sink. The load is modeled as a single current source which dissipates 600W – the maximum power the load will be required to handle is ~575W- in series with the parallel combination of the devices thermal resistance.

$$T_j - T_A = P_{dissipated}\left(R_{\theta js} + R_{\theta sa}\right) \quad (6.2)$$

Choosing the values $T_j = 175\,°C$, $T_A = 30°C$, $P_{dissipated} = 600\,W$, and a single device's thermal resistance is 2 $°C/W$ which simplifies to:

$$R_{\theta sa} = \frac{145}{600} - \frac{1}{\left(\frac{n}{2}\right)} \quad (6.3)$$

Where n is the number of devices.

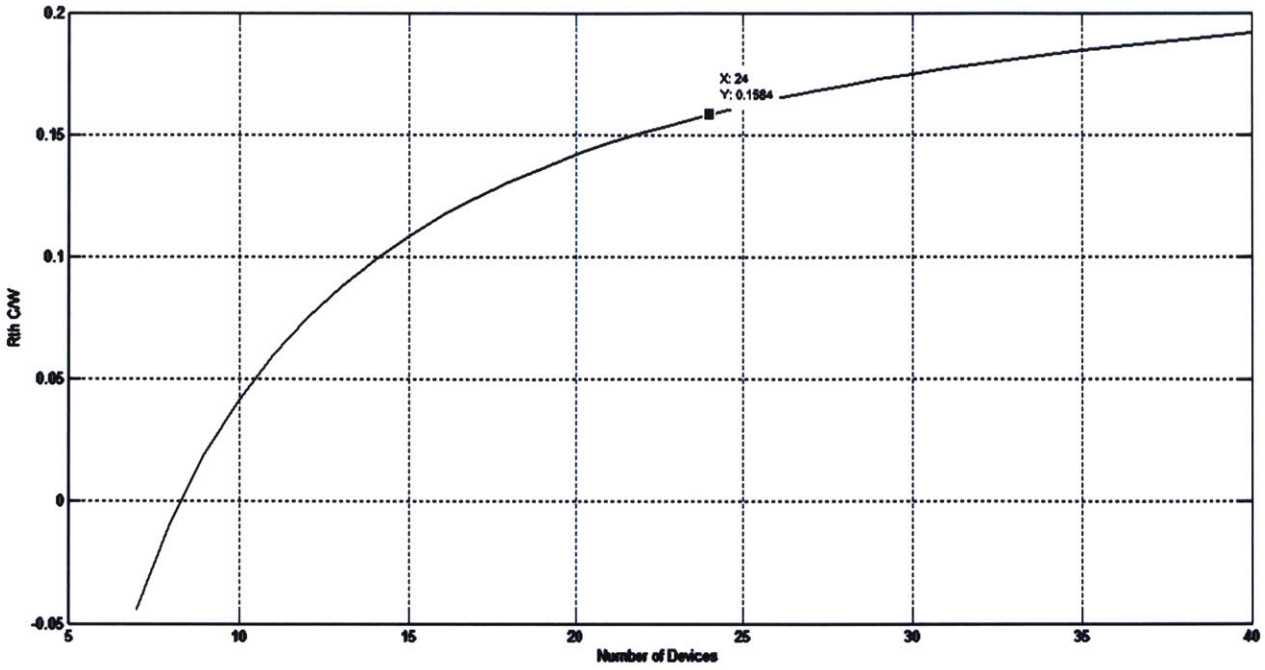

Fig 6.2 illustrates the heat sink's thermal resistance vs. the number of devices used in parallel.

6.1.3 Recommendations and Experimental Results

The recommended load design is composed of 25 zener diodes in parallel. To succeed at 9A input current, the devices should have between -2 and +2% voltage tolerance. Devices could be tested to ensure voltage tolerance lies within the range.

The plots below illustrate the experimental performance of the zener load

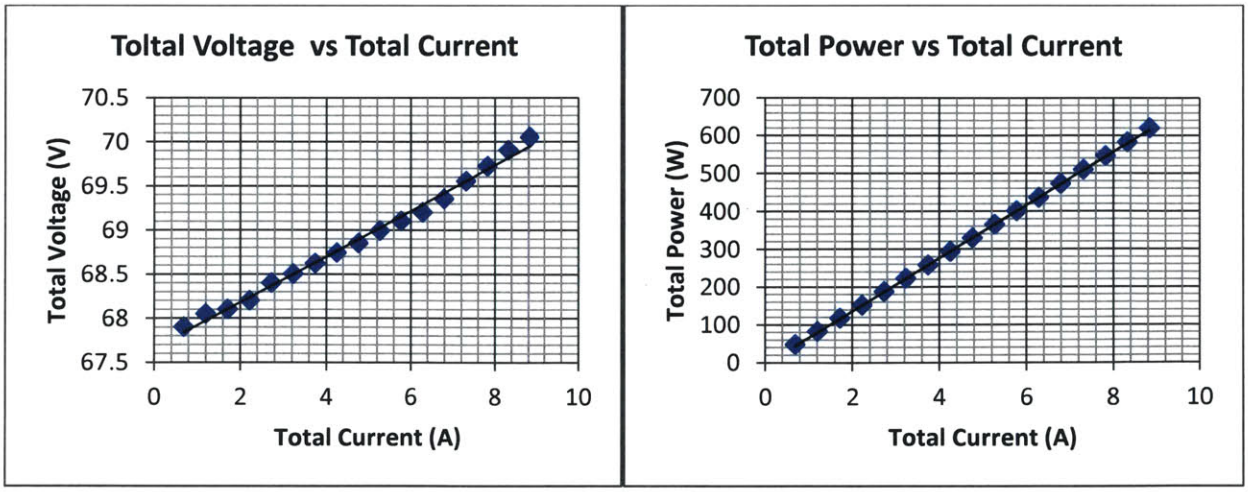

Fig 6.3 illustrates the total voltage and power as the input current is swept between 0 and 9A.

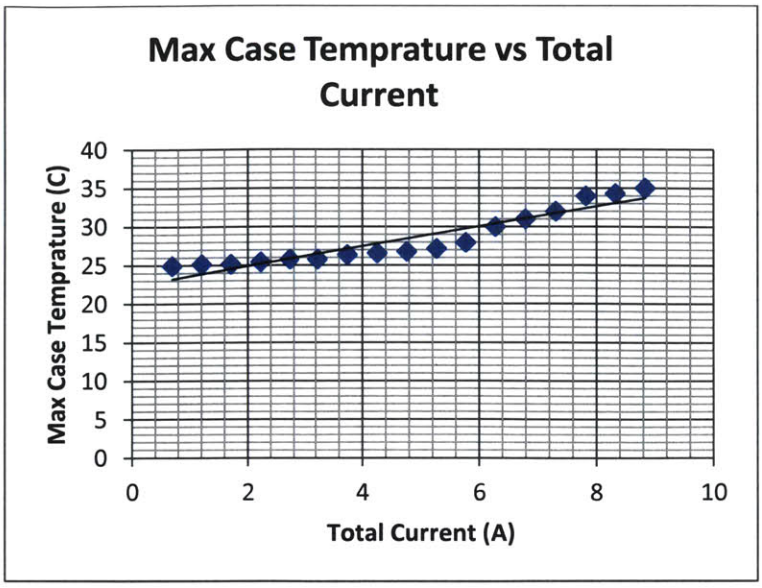

Fig 6.3 illustrates the maximum case temperature as the input current is swept between 0 and 9A.

6.2 Holdup time test

As discussed in chapter three, our design of interest has a hold up requirement of 20ms. This section shows that our selected capacitors pass the holdup requirement. Fig 6.4 below illustrates the topology of the test bench.

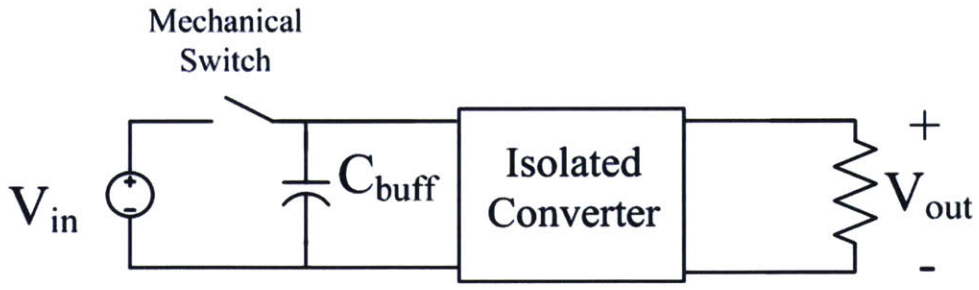

Fig 6.4 illustrates the circuit topology for the hold-up test bench

Using the setup shown in Fig 6.4 above, the capacitor is charged up to 72V from an input voltage source by closing the mechanical switch. After the capacitor is charged up, the switch is opened. During that time the converter is running off the energy stored in the capacitor.

Fig 6.5 below illustrates the results of the hold-up time test. The test used the Synqor SQ60120ETA20 converter and two EKYB800ELL681MK40S 80V capacitors. The capacitors

were initially charged to 72.1V, and then the mechanical switch is opened. Since the converter draws constant power, the waveform seen is similar to the expected waveform shown in Fig 3.10 and discussed in section 3.4.3. As seen in the figure, the capacitor

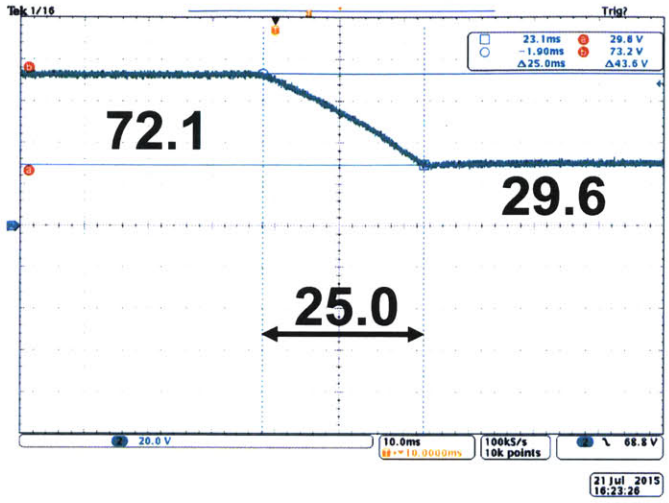

Fig 6.5 illustrates the voltage across the capacitor in the hold-up time test

Fig 6.5 above shows that the selected capacitor succeeds in supplying the energy required to keep the converter running for more than the required hold up time (20 ms).

In conclusion, this chapter covered the design, analysis and experimentation of a 600W zener load that was used to test the output of the resonant transition buck converter, and a hold up time test bench that was used to test the 20ms hold up time requirement. The zener load was successfully used to test the resonant buck converter circuit components, shown in Fig 4.1 (switches, diodes, and inductors). The holdup time test bench validated that the chosen capacitor passed the holdup time requirement.

Chapter 7

Summary and Conclusion

7.1 Thesis Summary and Conclusion

This thesis explored achieving high efficiency, high power factor, low voltage stresses, and smaller component sizes by utilizing high frequency operation, and contributed to the design of a full PFC system shown in Fig 1.1. The thesis focused on the design and test of the high-frequency buck power stage. It included the optimization of electrolytic capacitors to provide twice-line-frequency energy buffering and hold up energy, and the design of miniaturized inductors for the converter. Furthermore, the thesis verified that high-efficiency and high-density telecom "brick" DC/DC converters can be used as an isolation/transformation/configuration stage. Finally, it included the development, analysis and experimentation of a zener load, which was used to test the output of the resonant transition buck converter, and the development, analysis, and experimentation of a holdup test bench which was used to test the holdup energy requirement for a specific topology of interest.

The thesis showed that the buck topology can be used as a PFC stage (instead of a boost topology). The advantage we gain from using a buck PFC is lower voltage rating which allows for the use of high-density and high-efficiency telecom "brick" converters as isolation/transformation/configuration stage. Furthermore, this scheme allows for an easy way to get a different output by simply using a different converter for second stage.

Chapter 2 introduced the concepts and definitions of power factor correction. It further presents an overview of current PFC designs and tradeoffs and introduces the architecture of interest to this project.

Chapter 3 presented the requirements and design analysis for choosing a capacitor for twice line frequency energy buffering and holdup (e.g., for operation during line interruptions). The first part of the chapter analyzes the capacitors energy storing capability and the energy buffering capability. It looks at the energy density of the capacitor when constrained by the ripple allowed on the second stage, the RMS current capability, and the holdup energy requirement. The chapter concludes with capacitor selection and testing.

Chapter 4 presented the inductor design for a resonant transition buck converter. The first part of the chapter analysis the inductance requirement and the inductor realization in gapped E and planar geometries. It inspects the magnetic flux density capabilities of some select ferrite materials and develops a method to calculate inductor loss, including both core and winding loss, and temperature rise. The chapter also shows the experimental results of some inductors that could be used for our application and architecture of interest.

Chapter 5 investigated the possibility of using high-density, high-efficiency telecom brick converters for the second isolation/transformation/combination stage in the topology of interest. The chapter looks through the operation of available converters then presents experimental results of select converters that could be used in the architecture of interest

Chapter 6 presented some of the test bench circuits built to test aspects of the proposed design. The first test bench is a 600W zener bank load used to test the resonant transition buck converter. The second test bench is used to test the holdup time capability of the buffer capacitor.

7.2 Recommendations for Future Work

There are several directions in which the continued development of high-frequency and high-efficiency PFC development should proceed. The thesis includes the design of the PFC stage and utilizes high-density and high-efficiency telecom brick converters as a second stage. Lower cost and higher efficiency of the overall system can be achieved by integrating the design of both stages into a full architecture.

Further development of a loss model to characterize inductor losses, namely core loss, and inductor temperature rise is also worthwhile. The current models are somewhat limiting and are application specific. It would be beneficial to have a model that generalizes well and more measurement data on core performance.

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Appendix A

This appendix contains the Matlab code used for the analysis and design of the resonant transition buck converter.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The script calculates the Core loss, winding loss and temperature rise
% for all feasable planar inductor designs with DCM triangular current
waveforms
% Based on David Perreault's PhD optimization files
%
% Author: Ali S. AlShehab
% Review: Juan A. Santiago
% Date: July 2015
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc
clear all
close all

%% To run this code:
% Make sure the core data file is in the same directory as this file. And,
% 1- Choose the core geometry and core type.
% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
% 3- Specify the copper_thickness
% 4- Specify the K, y and relative permiability values for the material
%    at frequency of interest
% Steps explained below:

% 1- Choose and load the core geometry and core type. (Comment/Uncomment)
% EQCoredat;           % EQ Cores have a rectangular center post
% PlanarECoredat;      % PlanarE Cores have a circular center post
EILPCoredat;           % EILP Cores have a rectangular center post
Coretype = 1;          % Coretype 1 has a rectangular center post
% Coretype = 2;        % Coretype 2 has a circular center

% 2- Specify the operating frequency, currents (Irms, Ipk, Iavg)
f = 1.3e6;              %Specify operating frequency (Hz)
f_str = '1.3 MHz';      %For plotting purpose
Ipk= 9.08;              %Specify peak current (A)
Irms= 5.1245;           %Choose current RMS (A)
Iavg= 4.246;            %Choose average current  (A)

% 3- Specify the copper_thickness.
copper_thickness = [0.018*1e-3 ; 0.03556*1e-3 ; 0.07*1e-3 ; 0.105*1e-3 ;
0.14*1e-3];% 1/2, 1, 2, 3, 4 ounce copper in m
copper_thickness_ounce ={'1/2 ounce', '1 ounce', '2 ounce', '3 ounce', '4
ounce'};
thickness_index =3;  % Choose the copper thickness from the list above
thickness = copper_thickness(thickness_index);


% 4- Specify the K, y and relative permiability values for the material at
frequency of interest:
K1 = 0.7661; y1 = 2.0457;  % Coefficients of power for 4F1 @ 1MHz
```

```
K2 = 1.7385; y2 = 2.0665;  % Coefficients of power for 4F1 @ 5MHz

K3 = 0.0138; y3 = 2.7287;  % Coefficients of power for 3F4 @ 1 MHz
K4 = 7.0863; y4 = 2.0517;  % Coefficients of power for 3F4 @ 4 MHz

K5 = 0.0107; y5 = 2.6149;  % Coefficients of power for 3F45 @ 1 MHz
K6 = 8.248; y6 = 2.2057;   % Coefficients of power for 3F45 @ 4 MHz

K7 = 0.0973; y7 = 2.441;   % Coefficients of power for 67 @ 1.3 MHz
K8 = 0.6863; y8 = 2.2016;  % Coefficients of power for 67 @ 5 MHz

K = K3; % Choose K value
y = y3; % Choose y value
ur = ur_3F4; % Choose relative permiability of core material: ur_3F4, ur_F67,
ur_3F45, ur_4F1

% Other parameters and specifications:

I_n =[0.4302; 0.0747; 0.0243; 0.0271; 0.0032; 0.0103; 0.0058; 0.0041; 0.0074;
0.0032] .* Ipk; % Fourier Coeffs of waveform

% Applies for DCM triangular current waveform
Bmax = 0.3;                                % Maximum flux density in T
Tmax = 60;                                 % Maximum temperature rise in
deg Celcius
L = 3e-6;                                  % Inductance in H
mu=4*pi*10^-7;                             % Permeability of free space
(H/m)
p = 2.5e-8;                                % Resistivity of copper (Ohm-m)
@ 125 deg C
N = 10;                                    % Max number of turns in an
inductor

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% End User Input
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

No_of_layers = 4;                          % Max number of layers
d = sqrt(2./(4*pi*10^-7*2*pi.*f*10^8/2.5)); % Skin depth in m

%% save core data
lg = zeros(numcores,N); %Gap length
ue = zeros(numcores,N); %Effective permiability
Bpk = zeros(numcores,N); %Peak magnetic field
Pcore = zeros(numcores,N); %Core loss
Ptot = zeros(numcores, N); %Lowest total loss
Ptot1 = zeros(numcores, N); %Total Losses using 1 layer
Ptot2 = zeros(numcores, N); %Total Losses using 2 layers
Ptot3 = zeros(numcores, N); %Total Losses using 3 layers
Ptot4 = zeros(numcores, N); %Total Losses using 3 layers
Pwind = zeros(numcores, N); %Lowest Winding Loss
Pwind1 = zeros(numcores, N); %Winding Losses using 1 layer
Pwind2 = zeros(numcores, N); %Winding Losses using 2 layers
```

```
Pwind3 = zeros(numcores, N); %Winding Losses using 3 layers
Pwind4 = zeros(numcores, N); %Winding Losses using 4 layers
No_layers = zeros(numcores,N); %Number of layers
deltaT = zeros(numcores,N); %Temperature rise
designok = zeros(numcores,N); %Design check

%% Loop through available cores and synthesize inductor designs

%Calc Delta(harmonic)
for harmonic = 1:length(I_n)
    Delta_n(harmonic) =thickness*sqrt(harmonic*2*pi*1.3e6*pi*4e-7*(1/p)/2);
end


%Loop over all cores
for core =1:numcores

    %Calculate surface area for each core
    if Coretype == 1;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)- h(core)*(OD(core)-
ID(core)))+4*h(core)*w_core(core)+ 2*(OD(core)-ID(core))*w_core(core));
    elseif Coretype ==2;
        SA(core)= 10000*(2*(h_core(core)*w_core(core)+
l_core(core)*w_core(core)+l_core(core)*h_core(core)-
h(core)*OD(core))+2*pi*h(core)*(ID(core)/2)+ 2*(OD(core)*w_core(core)-
pi*(ID(core)/2)^2));
    end

    %Loop over different number of turns
    for n= 1:N

        designok(core, n) = 1; % assume this core design works

        %Calc gap
        %lg(core,n) = mu*Ae(core)*(1/Al(core,n) -
le(core)/(Ae(core)*mu*ur(core)));
        lg(core,n) = ((n^2*mu*Ae(core))/L)-(le(core)/ur(core));
        if lg(core,n) < 0
            designok(core, n) = 0;      % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: lg =
',num2str(lg(core,n))]);
        end

        if lg(core,n) > 0.5*h(core)
            designok(core, n) = 0;      % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: lg  =
',num2str(lg(core,n)), ' (larger than 0.5*core height)']);
        end

        % Calc the effective permeability (coefficient)
        ue(core,n) = ur(core)/(1+ur(core)*lg(core,n)/le(core));
        if ue(core,n) < 0
            designok(core, n) = 0;      % design is not ok
```

```
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: ue =
',num2str(Bpk(core,n))]);
        end

        % Calc the peak magnetic field Bpk in Tesla
        Bpk(core,n) = ue(core,n)*mu*n*Ipk/le(core);
        if Bpk(core,n) > Bmax
            designok(core, n) = 0;      % design is not ok
            disp([corename{core,:},' @ ',num2str(n),' turns rejected: Bpk =
',num2str(Bpk(core,n)),' tesla']);
        end


        %Calc Core Loss
        Pcore(core, n)=(Vc(core)*K*(Bpk(core,n)*1000)^y)/1000;

        %Initialize Factors = Rac(n)/Rdc
        Factors = zeros(length(I_n), 1);

        %Calc turns per layer, dc resistance, and Winding Loss
        for number_of_layers=1:No_of_layers
            turn_layer = zeros(1,No_of_layers); % This array will contain
the number of turns in each layer
            layer_dc_resistance = zeros(1,No_of_layers); % Array to store
the dc resistance for each layer
            %Calc number of turns in each layer
            if n > number_of_layers % calculate the number of turns in each
layer
                turn_layer(1:number_of_layers) =
turn_layer(1:number_of_layers) + floor(n/number_of_layers); %divide divisable
turns
                remaining_turns = mod(n, number_of_layers); %divide up
remaining turns
                turn_layer(1:remaining_turns) =
turn_layer(1:remaining_turns)+1;
                true_number_of_layers = number_of_layers;
            elseif n <= number_of_layers
                turn_layer(1:n) = 1;
                true_number_of_layers = n;
            end
            %Calc dc resistance for each layer
            for layer=1:number_of_layers
                ni = turn_layer(layer);
                if Coretype == 1;
                    layer_dc_resistance(layer)=
(ni^2)*4*p*(W(core)+OD(core))/(thickness*(OD(core)-ID(core)));
                elseif Coretype == 2;
                    layer_dc_resistance(layer) =
((ni)^2)*p*pi*(OD(core)+ID(core))/(thickness*(OD(core)-ID(core)));
                end
            end
            dc_resistance = sum(layer_dc_resistance); % total dc resistance

            for harmonic=1:length(I_n) %Factors= Rdc*Rac(n)/Rdc
```

```
                Factors(harmonic) =
dc_resistance*Delta_n(harmonic)*(((sinh(2*Delta_n(harmonic))+sin(2*Delta_n(ha
rmonic)))/(cosh(2*Delta_n(harmonic))-cos(2*Delta_n(harmonic))))+ ...
                            (2/3)*(((true_number_of_layers)^2)-
1)*((sinh(Delta_n(harmonic))-
sin(Delta_n(harmonic)))/(cosh(Delta_n(harmonic))+cos(Delta_n(harmonic)))));
            end

            %Calc Winding loss for different number of layers
            if number_of_layers == 1
                Pwind1(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
            elseif number_of_layers == 2
                Pwind2(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
            elseif number_of_layers == 3
                Pwind3(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
            elseif number_of_layers == 4
                Pwind4(core, n)= Iavg^2*dc_resistance +
0.5*sum((I_n.^2).*Factors);
            end

        end

        %Calc Total Loss for different number of layers
        Ptot1(core, n)=Pwind1(core,n)+Pcore(core,n);
        Ptot2(core, n)=Pwind2(core,n)+Pcore(core,n);
        Ptot3(core, n)=Pwind3(core,n)+Pcore(core,n);
        Ptot4(core, n)=Pwind4(core,n)+Pcore(core,n);

        %Find the best number of layers and the corresponding total power
        %loss
        [Ptot(core, n), No_layers(core,n)] = min([Ptot1(core, n), Ptot2(core,
n), Ptot3(core, n), Ptot4(core, n)]);
        if No_layers(core,n) == 1
            Pwind(core,n)= Pwind1(core, n);
        elseif No_layers(core,n) ==2
            Pwind(core,n)= Pwind2(core, n);
        elseif No_layers(core,n) ==3
            Pwind(core,n)= Pwind3(core, n);
        elseif No_layers(core,n) ==4
            Pwind(core,n)= Pwind4(core, n);
        end
        %Calc Total temperature rise
        deltaT(core, n) = (0.55*Ptot(core, n)*1E3/SA(core)).^0.833;
        if deltaT(core, n) > Tmax
           designok(core, n) =0;
           disp([corename{core,:},' @ ',num2str(n),' turns rejected: delta T
= ',...
                    num2str(deltaT(core, n)),' deg C']);
        end

        % Write out the data for the best design and plot Losses for all
        %designs that worked
        if designok(core, n) == 1
```

```
            %Display best designs stats
            disp('              ');
            disp([corename{core,:},' : Works!']);
            disp(['f = ',num2str(f), ' Hz']);
            disp(['L = ',num2str(L), ' H']);
            disp(['lg = ',num2str(lg(core, n)), ' m']);
            disp(['N = ',num2str(n)]);
            disp(['No of layers = ',num2str(No_layers(core, n))]);
            disp(['Bpk = ',num2str(Bpk(core,n))]);
            disp(['Pcore = ',num2str(Pcore(core,n)),' Watts']);
            disp(['Pwind = ',num2str(Pwind(core,n)),' Watts']);
            disp(['Ptot = ',num2str(Ptot(core,n)),' Watts']);
            disp(['delta T = ',num2str(deltaT(core, n)),' deg C']);
            disp('              ');

            corenamevalid{core,n} = corename{core,:};
            lgvalid(core,n) = lg(core, n);
            Bpkvalid(core,n) = Bpk(core,n);
            Pcorevalid(core,n) = Pcore(core,n);
            Pwindvalid(core,n) = Pwind(core,n);
            Ptotvalid(core,n) = Ptot(core,n);
            deltaTvalid(core,n) = deltaT(core,n);
            Nvalid(core, n) = n;
        else
            corenamevalid{core,n} = [corename{core,:}, '(Failed)'];
            lgvalid(core,n) = NaN;
            Bpkvalid(core,n) = NaN;
            Pcorevalid(core,n) = NaN;
            Pwindvalid(core,n) = NaN;
            Ptotvalid(core,n) = NaN;
            deltaTvalid(core,n) = NaN;
            Nvalid(core, n) = NaN;

        end
    end

    if sum(designok(core,:))==0
        disp([corename{core,:},' Doesnt work for any n']);
    else
    % Plots:
        figure;
        plot(Nvalid(core,:), Pcorevalid(core, :), '*',Nvalid(core,:),
Pwindvalid(core, :), '*',Nvalid(core,:), Ptotvalid(core,:), '*');
        title([corename{core,:},' : Power Loss vs number of turns (',
copper_thickness_ounce{thickness_index}, ' cu)']);
        xlabel('number of turns (turn)')
        set(gca, 'XTick', [1 2 3 4 5 6 7 8 9 10 ])
        xlim([min(Nvalid(core,:))-1 max(Nvalid(core, :))+1]);
        ylabel(' Power Loss (W)')
        legend('Core Loss', 'Winding Loss', 'Total Loss')
    end
end

for core= 1:numcores
    [Best_Ptot(core), Best_N(core)] = min(Ptotvalid(core,:));
    Best_corename{core}= corenamevalid{core, Best_N(core)};
```

```
    Best_Pwind(core)= Pwindvalid(core, Best_N(core));
    Best_Pcore(core)= Pcorevalid(core, Best_N(core));
end

figure;
subplot(2,1,1)
plot(1:length(Best_corename),Best_Pcore, 'color', 'b')
hold on
plot(1:length(Best_corename),Best_Pwind, '-.', 'color', 'r')
hold on
title(['Core Loss & Winding Loss vs Core @ ',f_str, ' with
(',copper_thickness_ounce{thickness_index}, ' cu)']);
hold all
legend('Core Loss', 'Winding Loss')
set(gca, 'xtick', 1:length(Best_corename))
set(gca, 'xticklabel', Best_corename)

subplot(2,1,2)
plot(1:length(Best_corename),Best_Ptot, 'color', 'r')
title(['Total Loss vs Core @ ',f_str, ' with
(',copper_thickness_ounce{thickness_index}, ' cu)']);
hold all
legend('Total Loss')
set(gca, 'xtick', 1:length(Best_corename))
set(gca, 'xticklabel', Best_corename)
```

Appendix B

This appendix shows the highest efficiency telecom DC/DC converter available. Data was taken in March 2015.

Manufacturer	Part Number	Max Power (W)	Volume (in3)	Max Power Density (W/in3)	Rated Power Density (W/in3)	Usable Power at 60C (W)	Efficiency at 75 V and 120W	Output DC Voltage
SynQor	SQ60120EPB25	300	1.243104	241.33	96.532	210	93%	12
SynQor	SQ60120QZB40	480	1.6675	287.856	71.964	NA	NA	12
SynQor	PQ60120HZx50	600	2.36256	253.96	50.8	360	90%	12
SynQor	PQ60120QEB20	240	1.45406	165.055	82.5	228	92%	12
SynQor	PQ60120QZB33	400	1.65416	241.81	72.5	300	93%	12
SynQor	SQ60120ETA20	240	1.03086	232.815	116.4	156	93.5%	12
SynQor	PQ60240HZx25	600	2.36256	253.962	50.8	312	93.5%	24
SynQor	SQ60120ETA17	204	1.03086	197.89	116.4	156	93.5%	12
SynQor	SQ60120QPA28	336	1.45406	209.895	82.5	264	92%	12
SynQor	SQ60120QPB33	396	1.65416	237.481	72.5	250	91%	12
SynQor	CF48120QTx12	150	1.83	81.96	65.6	149	92%	12
SynQor	CF48240QTx06	150	1.83	81.96	65.6	139	91%	24
SynQor	IQ48240HPx10	255	3.04	83.88	39.47	168	92%	24
SynQor	IQ48120HTx16	200	3.04	65.79	39.47	180	92%	12
SynQor	IQ48240HTx08	200	3.04	65.79	39.47	187	92%	24
SynQor	IQ48120HZx50	602	3.04	198.03	39.47	300	90%	12
SynQor	IQ48240HZx25	602	3.04	198.03	39.47	288	89%	24
SynQor	MCOTS-C-48-24-HP	252	3.04	82.89	39.47	252	92%	24
SynQor	PQ60240QGA05	120	1.43	83.68	93.68	115	92%	24
SynQor	PQ60120HZx50	600	2.36256	253.96	50.8	360	90%	12
SynQor	PQ60120QEB20	240	1.45406	165.055	82.5	228	92%	12
SynQor	PQ60120QZB33	400	1.65416	241.81	72.5	300	93%	12
SynQor	PQ60240HZx25	600	2.36256	253.962	50.8	312	93.5%	24
SynQor	SQ60120ETA17	204	1.03086	197.89	116.4	156	93.5%	12

SynQor	SQ60120QPA28	336	1.45406	209.895	82.5	264	92%	12
SynQor	SQ60120QPB33	396	1.65416	237.481	72.5	250	91%	12
General Electric	EBVW012A7B	152	1.1003	138.508	109.09	NA	95% (152W)	12
General Electric	ESTW010A0B	120	0.72	165.63	165.63	108	91%	12
General Electric	EBVW020A0B	240	0.91	263.74	131.86	180	93%	12
General Electric	EBVW025A0B	300	0.91	329.67	131.86	198	93%	12
Murata	UEE-12/12.5-D48P-C	150	0.8694	172.53	172.61	138.09	88%	12
Murata	MYBEA01212AZT	144	0.683	210.83	175.69	NA	92.5% (144W)	12
Murata	RBQ-12/33-D48xB-C	386	1.67	231.48	71.96	282	92%	12
Murata	RBE-12/20-D48NBH-C	240	1.035	231.88	115.94	210	92%	12
Murata	HPQ-12/25-D48PBX-C	300	1.67	179.64	71.86	264	91%	12
Murata	UVQ-12/10-D48PB-C	120	1.67	71.86	71.86	120	86%	12
Murata	RBE-12/20-D48NB-C	240	0.828	289.855	144.93	204	92.5%	12
Delta Electronics	E48SC12020	240	0.89	269.66	134.83	180	89%	12
Delta Electronics	E48SP12020	240	0.89	269.66	134.83	215	92.5%	12
Delta Electronics	E48SC12025	300	0.89	337.08	134.83	132	92.5%	12
Delta Electronics	Q48SQ12018	216	1.57	137.58	76.43	216	92%	12
Delta Electronics	E48SH12010	120	0.7659	156.678	156.67	111	93%	12
Power-One	SQE48T10120	120	0.7707	155.695	155.69	82	91.5%	12
Power-One	HBC25ZH	300	3.36	89.286	35.71	144	90.5%	12
Power-One	QM48S14120	168	0.945	177.778	126.98	114	91.5%	12
Ericsson	BMR453 0000/001	396	1.5207	260.396	78.91	276	92.5%	12
Ericsson	BMR453 0007/013	376	1.5207	247.255	78.91	256	92.5%	12
Ericsson	BMR456 0004/001	420	1.47117	285.487	81.58	336	94%	12
Ericsson	BMR456 0007/013	400	1.47117	271.892	81.58	312	94%	12
Ericsson	BMR457 0004/001	264	0.8188	322.423	146.56	192	92.5%	12
Ericsson	BMR457 0007/013	251	0.8188	306.546	146.56	204	92.5%	12
Ericsson	PKB4113C PI	144	0.700672	205.517	171.26	108	92%	12
Ericsson	PKM4213C PINBSP	204	1.2166	167.679	98.68	156	93.5%	12