Radiation Management, Avionics Development, and Integrated Testing of a Class-D Space-Based Asteroid X-ray Spectrometer

by

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Abstract

The Regolith X-ray Imaging Spectrometer (REXIS) is a student designed and built payload instrument aboard NASA's OSIRIS-REx asteroid sample return mission. The interplanetary target for this mission is a primitive asteroid known as Bennu that is believed to be relatively unchanged since the formation of the Solar System over 4.5 billion years ago. The primary goal of REXIS is to provide data to determine the elemental abundance composition of Bennu's surface through the measurement of X-ray fluorescence from Bennu's regolith. Achieving this goal requires the REXIS instrument to have an avionics system designed to operate the x-ray detectors, perform some preliminary processing of the x-ray events detected, and transfer this information to the main spacecraft computer for transmission to Earth. REXIS avionics accomplish these tasks using a mixture of commercial and spaceflight-grade hardware, reconfigurable Xilinx and Actel FPGAs, and a softcore MicroBlaze processor. Although the REXIS instrument is classified as a high-risk Class-D project by NASA, it must safely interface (in the manner of "do no harm") with the low-risk Class-B OSIRIS-REx spacecraft. Furthermore, REXIS must operate in the interplanetary space radiation environment of the OSIRIS-REx mission. This thesis details the REXIS avionics system and its novel features for collecting scientific x- ray data, interfacing safely with the OSIRIS-REx main spacecraft in spite of differing Class B/D risk postures, and robust operation in the interplanetary space radiation environment. Emphasis is placed on how the REXIS avionics design and radiation hazard mitigation features were implemented with significant budget and time constraints.

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I would like to thank Dr. Rebecca Masterson and Professor Richard Binzel for starting the REXIS project, guiding me through the project development, giving me encouragement, and helping me write this thesis. I am also thankful for Dr. Alvar Saenz-Otero and his advice and guidance that was essential for this thesis.

I enjoyed working with my REXIS team-mates and greatly appreciate their support, both throughout the project and for writing this document. I would not have been able to get started without the mentoring of Shuyi Chen and Mike Jones. I appreciate the practical advice and encouragement from Mark Chodas throughout the REXIS project. Finally, Conor McMenamin, Laura Bayley, and David Carte always made our office a fun and productive place to work.

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Contents

List of Figures

List of Tables

Acronym List

ADC – Analog to Digital Converter
C&DH – Command and Data Handling
CCD – Charge Coupled Device
CDR – Critical Design Review
CMOS – Complementary Metal Oxide Semiconductor
Co-ax – Coaxial Cable
COTS – Commercial Off The Shelf
CXEL – Candidate X-ray Events List
DAC – Digital to Analog Converter
DAM – Detector Assembly Mount
DC – Direct Current
DE – Detector Electronics
DSN – Deep Space Network
E-box – Electronics Box
ECC – Error Correcting Codes
EDAC – Error Detection and Correction
EM – Engineering Model
EMC – Electromagnetic Compatibility
EMI – Electromagnetic Interference
ET – Event Threshold
FM – Flight Model
FOV – Field of View
FPGA – Field Programmable Gate Array
FSW – Flight Software
GaAs – Gallium Arsenide
GCR – Galactic Cosmic Ray
GNC – Guidance Navigation and Control
GPIO – General Purpose Input/Output
GSFC – Goddard Space Flight Center
GUI – Graphical User Interface
HDL – Hardware Description Language
JTAG - Joint Test Action Group
LDO – Low Dropout
LEO – Low Earth Orbit
LET – Linear Energy Transfer
MEB – Main Electronics Board
MicroMAS – Micro-sized Microwave Atmospheric Satellite
MIT – Massachusetts Institute of Technology

MPMC – Multi Port Memory Controller
MRO – Mars Reconnaissance Orbiter
NICER- Neutron star Interior Composition Explorer
NOR Flash – Not OR Flash
Op Amp – Operational Amplifier
PCB – Printed Circuit Board
PDR – Preliminary Design Review
PRT – Platinum Resistance Thermometer
Rad – Radiation Absorbed Dose
Rad Cover – Radiation Cover
Rad-hard – Radiation Hardened
RC – Resistor-Capacitor
REXIS – REgolith Imaging X-Ray Spectrometer
OSIRIS-REx – Origins, Spectral Interpretation, Resource Identification, Security Regolith Explorer
PWM – Pulse Width Modulation
TAGSAM – Touch and Go Sample Acquisition Mechanism
TESS – Transiting Exoplanet Survey Satellite
TID – Total Ionizing Dose
TNID – Total Non-Ionizing Dose
TVac – Thermal Vacuum
SBB – SXM Backpack Board
SDD – Silicon Drift Detector
SDRAM – Synchronous Dynamic Random Access Memory
SEB – SXM Electronics Board
SEL – Single Event Latch-up
SET – Single Event Transient
SEU – Single Event Upset
Si – Silicon
SPE – Solar Particle Event
SPI – Serial Peripheral Interface
SRAM – Static Random Access Memory
SRC – Sample Return Capsule
SSL – Space Systems Laboratory
ST – Split Threshold
STL – Spacecraft Test Laboratory
SXM – Solar X-ray Monitor
TID – Total Ionizing Dose
TIL – Thermal Isolation Layer
TVAC – Thermal Vacuum
ULD – Upper Limit Discriminator
VDC – Volts, Direct Current
XRF - X-Ray Fluorescence

Chapter 1 - Introduction

The REgolith X-ray Imaging Spectrometer (REXIS) is one of the remote sensing instruments aboard the spacecraft of the NASA Origins, Spectral Interpretation, Resource Identification, Security, Regolith Explorer (OSIRIS-REx) mission. The OSIRIS-REx mission is designed to allow scientists to remotely study the asteroid Bennu, and return a sample from the asteroid's topsoil, or regolith, to laboratories on Earth. The goal of REXIS is to remotely acquire scientific data in the form of elemental composition of Bennu's regolith for the OSIRIS-REx mission.

REXIS is a high-risk and low-cost component of the OSIRIS-REx system. The most important requirements of the REXIS project are educating student engineers through practical spaceflight development experience and not damaging the OSIRIS-REx spacecraft. The low-cost nature of REXIS has caused the development and testing of the REXIS avionics system to be more time and budget constrained than a typical spaceflight project. These time/budget constraints and the REXIS's two high-level requirements take priority over the secondary requirement of acquiring scientific data from Bennu, thus allowing for higher risks to be taken with this data acquisition. Overall, this outlook can be summarized by the fact that REXIS-spacecraft interface is class-B (low-risk) but has other subsystems which are class-D (high-risk), like the science data collection, that are outside of the spacecraft-interface. Class B and Class D are further explained in section 1.1.

The REXIS avionics is the combination of electrical and software subsystems that enable the REXIS instrument to process commands, operate instrument subsystems, and generate both scientific and engineering telemetry. The high-risk and radiation-tolerant nature of the REXIS avionics system is presented as guide and example for the design and testing of similar resource-constrained high-risk space systems. This thesis presents the design of the electrical and software systems of the REXIS instrument, how these systems operate in spite of the space radiation hazard, and the development and testing of these

systems. Rationale behind design decisions and lessons learned from the REXIS avionics system are also detailed in order to guide future space system development.

The remainder of this chapter begins with the background and motivation for this thesis. Afterward, an overview of the OSIRIS-REx system and its scientific goals is presented. Next the REXIS instrument is presented as a scientific payload that contributes to the scientific return of the OSIRIS-REx mission. Finally, a thesis roadmap that details the layout and content of this entire document is presented.

1.1 Background and Motivation

Humanity has realized many practical benefits through operating spacecraft both within and beyond Earth's orbit. Without these spacecraft, modern society's reliance on state-of-the-art space exploration, remote sensing, surface imaging, global tracking/positioning, and communications technology would be impossible. To continue realizing the benefits of these space-based technologies, there must be ongoing progress in the research, development and testing of new spacecraft.

A new spacecraft system requires the development, integration, and testing of the electronic subsystems. These electronics that are designed to operate in outer space are known as avionics, and they are provide electrical power, process commands from Earth, generate and send telemetry to Earth, and control the spacecraft and its mechanisms. Avionics have certain specially designed features that allow them to operate reliably without complications in outer space for long durations. When compared to the electronics on Earth, avionics require extra development and testing resources.

Spacecraft in general, and avionics in particular, are very expensive to develop in terms of time and money. Compared to operating conditions on Earth, avionics in space must endure an extreme temperature range, harsh vibrations from a rocket launch, constant radiation bombardment, and a hard vacuum. To operate in these extreme conditions, avionics require expensive components, and implementation of costly design, testing and optimization that increase the overall cost and development time. Testing an avionics design to determine if it works in these environments requires expensive array of equipment like thermal-vacuum chambers, vibration tables, radiation chambers, and particle

accelerators. Finally, because spacecraft typically cannot be repaired in space, there is a push to have these spacecraft operate for as many years as possible without servicing. Spacecraft longevity is accomplished through spending more resources to increase spacecraft reliability and fault tolerance. These factors combine together to make both spacecraft and their avionics extremely expensive to design, build, integrate, and test.

In recent years, there is a push for developing low-cost spacecraft and avionics. Entities with smaller budgets like small companies, universities, and technology demonstration projects are enabled by lower rocket-launch costs, new research and development goals, and state-of-the-art technology to develop spacecraft. The projects of these entities are typically allocated smaller budgets than the usual spacecraft programs from large companies and governments. An example of such spacecraft are CubeSats which are miniature satellites designed to utilize surplus payload capability aboard rockets. These spacecraft have limited capability and their stakeholders are more failure tolerant than traditional large-budget space systems.

Another low-cost and experimental project is the REXIS instrument. REXIS is classified as a Class D mission by NASA in contrast to the Class B designation of the whole OSIRIS-REx mission. Class D missions "have a lifecycle cost of less than $250 million. They generally are less complex, have a streamlined reliability approach, and may have a shorter design life" [1]. Class B missions are the traditional high-cost space missions since they are "high priority" in terms of advancing NASA's scientific mission, have "high complexity", and have "high national significance" [2]. On the other hand, REXIS's Class D nature means that REXIS mission success provides valuable science data to enhance the OSIRIS-REx mission, but a failure of REXIS to provide this scientific data does not put the OSIRIS-REx's mission success, or NASA's overall space science mission, in jeopardy. Because of this directive, REXIS can take higher risks in the development and testing of its avionics system.

There is a lack of published literature and guidance for the successful development, testing and operation of such high-risk spaceflight missions [3]. There is no guide to designing, building, integrating, and operating a Class D subsystem that properly interfaces with a Class B system. For example, the

REXIS development team had very few guidelines or standards to follow when designing a robust avionics system that would not damage the OSIRIS-REx spacecraft and its asteroid sample recovery program, but operate within the allocated time and budget.

The design, development, and testing of the REXIS avionics system is presented as an example of low-cost high-risk design that interfaces with a high-cost low-risk spacecraft system. Successes and failures that occurred during the REXIS avionics project are presented and can be used as a learning guide for future missions.

1.2 OSIRIS-REx Spacecraft Overview

The OSIRIS-REx is NASA's asteroid sample return mission. OSIRIS-REx's main component is a spacecraft that is scheduled to launch in September 2016 and will return a pristine sample from the asteroid Bennu's surface in 2023 [4] [5]. The OSIRIS-REx spacecraft is designed to launch from Earth, cruise to Bennu, remotely study this asteroid, acquire an asteroid regolith sample, and deliver this sample to Earth.

The OSIRIS-REx mission motto of "Exploring Our Past, Securing Our Future Through Pioneering Asteroid Science" summarizes the objective and purpose of the OSIRIS-REx scientific mission [6]. The acronym OSIRIS-REx is derived from the mission's scientific objectives and is further explained below:

- **Origins** - Bennu is a carbonaceous asteroid that is believed to contain material left over from the formation of the solar system [4]. The asteroid topsoil, known as regolith, that OSIRIS-REx is designed to sample and return will allow scientists to understand the organic chemistry and geochemistry of Bennu, and consequently the early solar system as a whole [4].
- **Spectral Interpretation** – The OSIRIS-REx spacecraft carries a suite of spectrometers that generate spectra of the photons emitted from Bennu. These spectra span a variety of wavelengths ranging from infrared, visible light, and x-ray, and they are used to determine the physical, mineralogical, chemical, and elemental composition of Bennu.

- **Resource Identification** – The spectral information will also be acquired for specific areas on Bennu's surface. The preliminary data will be used to understand the geology and composition of Bennu, and ultimately help in finding the sampling site on Bennu's surface.
- **Security** – Bennu is an asteroid 500 meters in diameter and has a 0.037% chance of impacting the Earth between the years of 2175 to 2196 [7]. OSIRIS-REx is designed to provide data for understanding the momentum change caused by the absorption and emitting of the sun's thermal energy on Bennu. Precise understanding of this orbital disturbance, known as the Yarkovsky Effect, further refines the current estimate of a 0.037% chance that Bennu and Earth will collide [8].
- **Regolith Explorer** – OSIRIS-REx's remote sensing instruments and sample return mission will currently focus on the topsoil, or regolith of Bennu.

The OSIRIS-REx spacecraft consists of the following subsystems to meet the previously described scientific objectives:

- A spacecraft bus that meets the structural, navigational, optical, thermal, electrical, and communications requirements imposed by the mission's remote-sensing instruments and sample-acquisition hardware
- A mechanism to acquire and deliver an asteroid regolith sample to Earth
- Remote Sensing instruments to fully characterize the asteroid Bennu in relation to other asteroids

The following sections provide an overview of each of these OSIRIS-REx spacecraft subsystems.

1.2.1 OSIRIS-REx Spacecraft Bus

The spacecraft bus is both physically and functionally in the center of the OSIRIS-REx system. This central subsystem interacts with all the subsystems of the OSIRIS-REx system. The spacecraft bus consists of a chassis derived from the Mars Reconnaissance Orbiter (MRO) spacecraft that has mounting points for all the other spacecraft components. All spacecraft functionality such as power, propulsion,

avionics, communication, navigation, and scientific data acquisition are implemented with components that are mounted on the spacecraft bus. An Atlas-5 rocket is the launch vehicle for OSIRIS-REx since it places the spacecraft on an interplanetary trajectory to the asteroid Bennu [4].

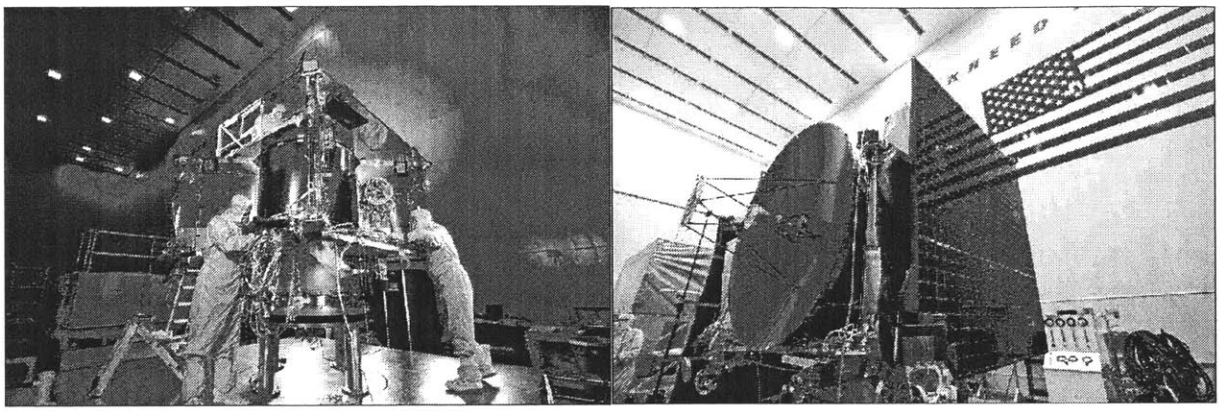

Figure 1-1: Pictures of the OSIRIS-REx Spacecraft[1]

The left side of Figure 1-1 shows technicians building the spacecraft chassis and gives an idea of spacecraft size. The black cylinder in the middle of this left image is a structural member that contains the main OSIRIS-REx propellant tank. Four gussets protrude radially from this structural cylinder and serve as the mounting surface for many spacecraft subassemblies. The four gussets and structural cylinder are capped with decks on both ends which provide mounting for remote sensing instruments, the sample return capsule (SRC), and main propulsion system. The left side of Figure 1-1 is the same spacecraft chassis with the addition of the mounted circular high-gain antenna and rectangular solar panels.

1.2.2 Regolith Sample Acquisition and Delivery

The spacecraft bus provides the mounting for two key assemblies required for sample return from Bennu. These assemblies are the Touch and Go Sample Acquisition Mechanism (TAGSAM) and the Sample Return Capsule (SRC). TAGSAM is a robotic arm that allows OSIRIS-REx to acquire the asteroid sample, and SRC is a container that contains and protects the asteroid sample during its journey through Earth's atmosphere. Through commands from the ground, the spacecraft extends the TAGSAM

[1] Taken from the blog of OSIRIS-REx Principle Investigator Dante Lauretta on 6/26/2016. URL: https://dslauretta.com/2015/11/13/osiris-rex-progressing-through-environmental-testing/

arm and positions it near the asteroid. A puff of pure nitrogen gas is used to push Bennu's regolith dust into the TAGSAM head.

After the asteroid regolith sample is acquired, it needs to be measured and returned to Earth. Immediately after sample acquisition, the spacecraft is commanded to do the following to verify the sample has been properly acquired [4]:

1. Take images of the sample-site on Bennu with remote sensing instruments
2. Determine the sample mass by measuring the change in the spacecraft's moment of inertia. By using small rocket thrusters to spin the spacecraft, and measuring the spin-rate with the spacecraft's Guidance Navigation and Control (GNC) sensors, the change in the spacecraft's moment of inertia due to the asteroid sample can be determined for estimating sample mass.

Once these steps are completed, the asteroid sample is ready to be stored.

After sample acquisition, The TAGSAM robotic arm is actuated to store the asteroid sample in an open SRC. Afterward, the SRC closes and is ready for its journey through Earth's atmosphere. OSIRIS-REx then leaves Bennu and takes a 2 year journey to Earth. Once this journey is complete, the spacecraft is commanded to release the SRC into Earth's atmosphere [5].

1.2.3 OSIRIS-REx Payload Instruments

Prior to acquiring a sample of Bennu's regolith, an appropriate sampling site must be chosen. A sampling site is selected by analyzing data from the remote sensing instruments aboard OSIRIS-REx. These instruments are used to understand Bennu's physical, elemental, visual, and infrared composition. This holistic understanding of Bennu's surface provided by remote sensing instruments is essential for picking a sample site that is scientifically interesting and not hazardous for operating the TAGSAM mechanism.

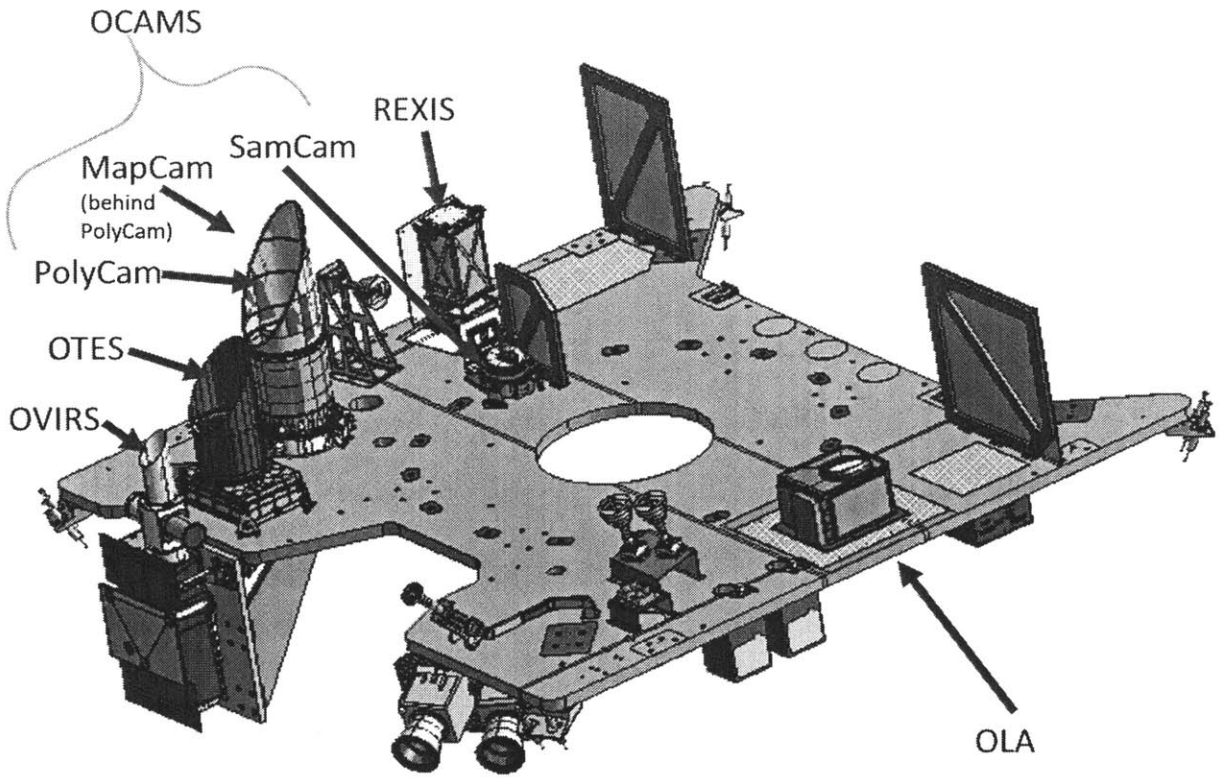

Figure 1-2: OSIRIS-REx Remote Sensing Instruments[2]

OSIRIS-REx has an instrument deck (Figure 1-2) which has a variety of scientific payload instruments and the SRC mounted to it. In order to collect scientific data, the spacecraft orients itself so that the instrument deck faces the asteroid. This maneuver is important because it allows all the scientific payload instruments to simultaneously collect data from the asteroid.

The scientific payload aboard OSIRIS-REx are the following remote sensing instruments (Table 1.1) used to determine the shape and composition of Bennu in terms of particles sizes, chemicals, minerals, and elements. The OSIRIS-REx Camera Suite (OCAMS) consists of three cameras that use the same imaging sensor to sense visible light at various ranges. PolyCam serves as both a telescope and microscope designed to acquire Bennu from long ranges and provide high resolution images of Bennu's regolith. MapCam is designed to image the entire surface of Bennu. SamCam is designed to take close-up images of the sample site and the TAGSAM mechanism. Next to OCAMS is the OSIRIS-REx Visible

[2] Taken from the blog of OSIRIS-REx Principle Investigator Dante Lauretta on 6/26/2016. URL: https://dslauretta.com/2014/06/04/spacecraft-structure-the-bones-of-osiris-rex/

and Infrared Spectrometer (OVIRS), which is sensitive to light wavelengths of 0.4-4.3 micrometers and used to determine local and global concentrations of organic volatile compounds on Bennu's surface. Longer infrared wavelengths from 4-50 micrometers are sensed by the OSIRIS-REx Thermal Imaging Spectrometer (OTES) that provides thermal data about Bennu's surface. The instrument deck also hosts the OSIRIS-REx Laser Altimeter (OLA) that provides data used to create topographical maps of Bennu. The final instrument is the Regolith X-ray Imaging Spectrometer (REXIS) is designed to sense x-rays within the energy range of 0.5-7 keV emitted by Bennu. The x-ray spectra derived from REXIS data is used to determine the global and local elemental makeup of Bennu's regolith. The information produced by all of these instruments is used to determine the sample selection site [9].

Table 1.1: Scientific Payload Instruments aboard OSIRIS-REx [9]

Instrument Name	**Abbreviation**	**Purpose**
OSIRIS-REx Camera Suite	OCAMS	Detect the asteroid visually, photograph the asteroid, detect satellites/outgassing around the asteroid, and observe the asteroid sampling process
OSIRIS-REx Laser Altimeter	OLA	Create a topographical map of the asteroid
OSIRIS-REx Visible and Infrared (IR) Spectrometer	OVIRS	Create visible/IR spectra for areas on the asteroid to determine chemical composition of these areas
OSIRIS-REx Thermal Emission Spectrometer	OTES	Create a thermal IR spectrum for areas on the asteroid to determine mineral composition and particle size within these areas
Regolith X-ray Imaging Spectrometer	REXIS	Create an x-ray spectrum for areas on the asteroid to determine elemental composition of these areas

1.3 REXIS Instrument Overview

The Regolith Imaging X-ray Spectrometer (REXIS) is a remote sensing payload instrument that flies aboard OSIRIS-REx and is used to determine the elemental composition of Bennu's regolith. Knowledge of the composition of Bennu's regolith aids in classifying Bennu amongst the different types of asteroids and determining an appropriate site for sampling Bennu's regolith. REXIS determines the composition of Bennu's regolith by sensing the x-rays emitted by Bennu's surface.

1.3.1 REXIS Science Process and Data

The REXIS instrument is designed to sense x-ray fluorescence (XRF) from Bennu's regolith. A schematic of this process is shown in Figure 1-3 where the Sun emits x-ray energy that excites the regolith of Bennu. The excitation caused by solar x-ray energy causes the regolith to emit its own x-rays – this is the XRF process. The energy of these x-rays depend on the regolith's elemental composition. REXIS uses Charged Coupled Device (CCD) sensors to sense these x-rays originating from Bennu. Using data from the CCDs, the REXIS instrument produces scientific telemetry from Bennu that consists of x-ray energy, the position where x-rays intersect REXIS's sensor, and how the x-rays energize clusters of pixels within this sensor. In order to properly interpret x-ray energies and correctly derive elemental abundances in Bennu's regolith from the XRF, the solar x-ray spectrum at Bennu must be acquired at the same time as the XRF reading. REXIS has an auxiliary detector known as the Solar X-ray Monitor (SXM) that detects the solar x-rays while the CCD sensors are operating as shown in Figure 1-3 [10]. While the main CCD x-ray sensors provide data for x-ray spectra that correspond to local elemental abundances on Bennu, the SXM only provides the x-ray spectrum of the Sun as a whole.

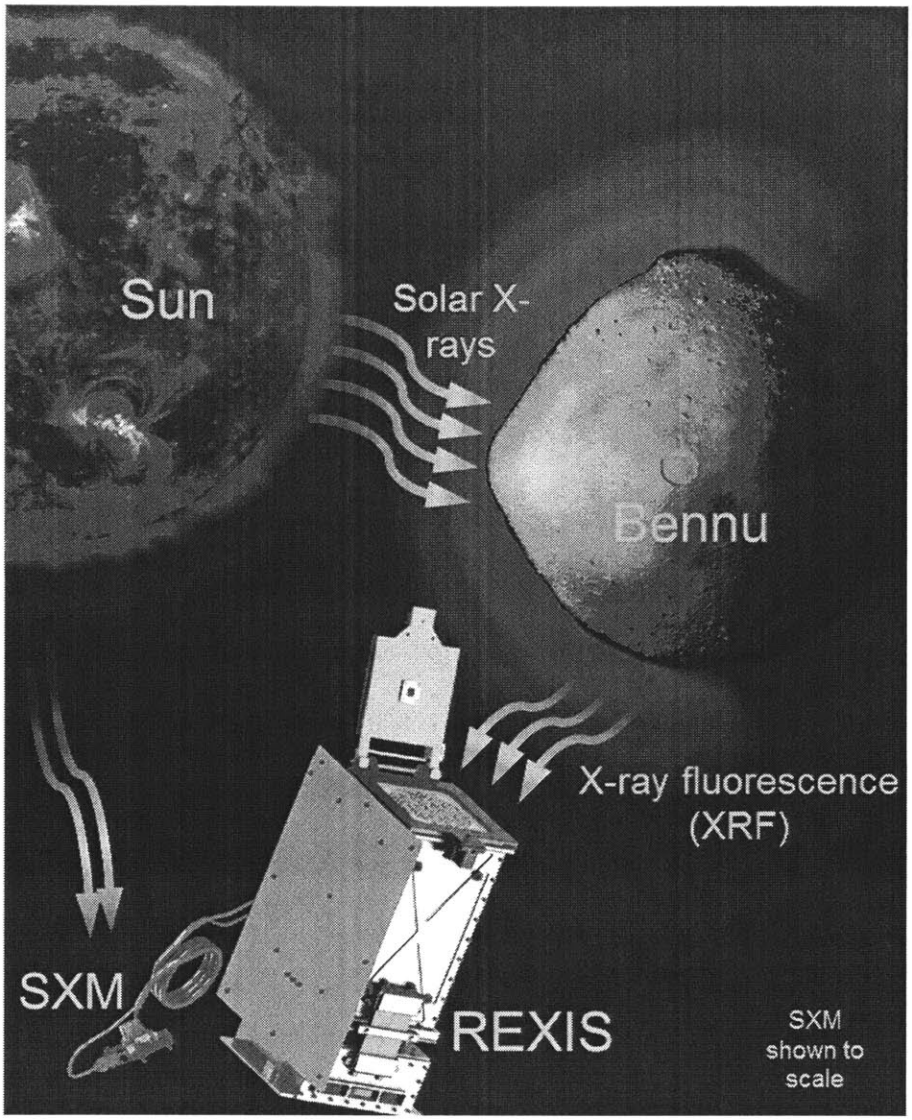

Figure 1-3: REXIS X-ray Data Acquisition (Credit: Branden Allen and Niraj Inamdar)

REXIS uses a coded aperture x-ray imaging process to sense where on Bennu's surface an x-ray originated from. This process consists of encoding x-ray light from the asteroid with a coded aperture mask. A coded aperture mask is a metal sheet coded with a pattern that is opaque to x-rays at random points as shown in Figure 1-4 below. This pattern is randomly generated during REXIS design and used by scientists to transform REXIS scientific x-ray telemetry into elemental abundance maps of Bennu.

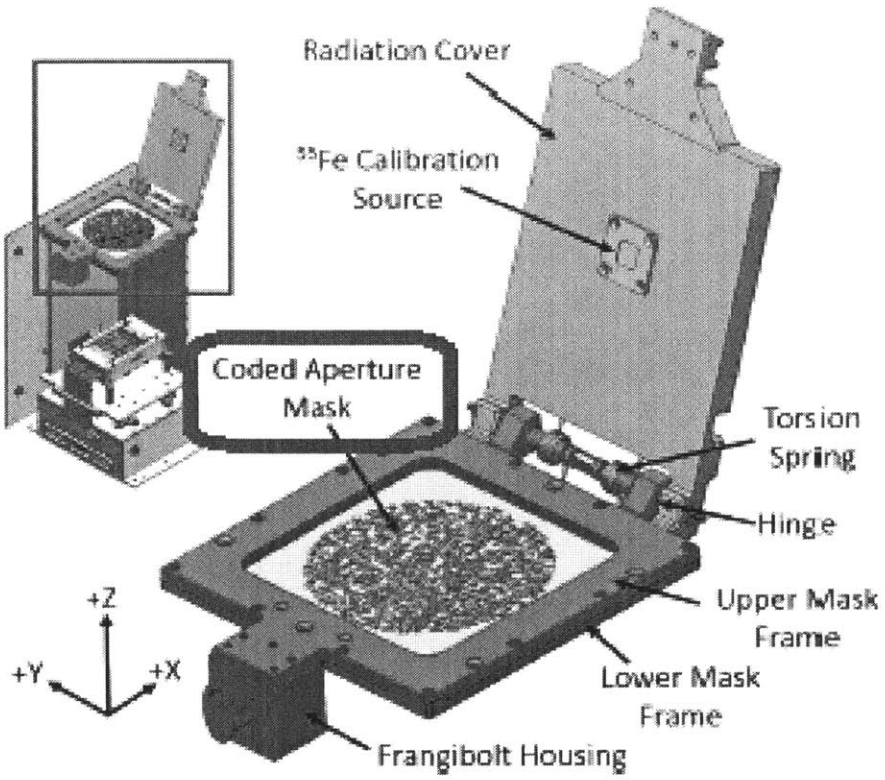

Figure 1-4: REXIS Coded Aperture Mask [3]

Consider a point source of x-ray light on Bennu's surface within the REXIS spectrometer's field of view. The x-ray light from this point source will create a particular shadow of Figure 1-4's coded aperture mask on the CCD detectors. This particular shadow depends on the position of the point source in the REXIS spectrometer's field of view. The pattern of photons that are not blocked by the coded aperture mask are sensed by the REXIS CCDs. The 2-dimensional image of these unblocked x-ray photons forms x-ray image telemetry that is transmitted to Earth. Scientists on Earth can perform a two-dimensional mathematical de-convolution of the coded mask pattern and CCD-derived x-ray image to recover the position of the x-ray point-source. Since all of the x-ray light from the asteroid can be broken down into a superposition of x-ray point-sources, this convolution technique can used to recreate an x-ray image of the asteroid [11].

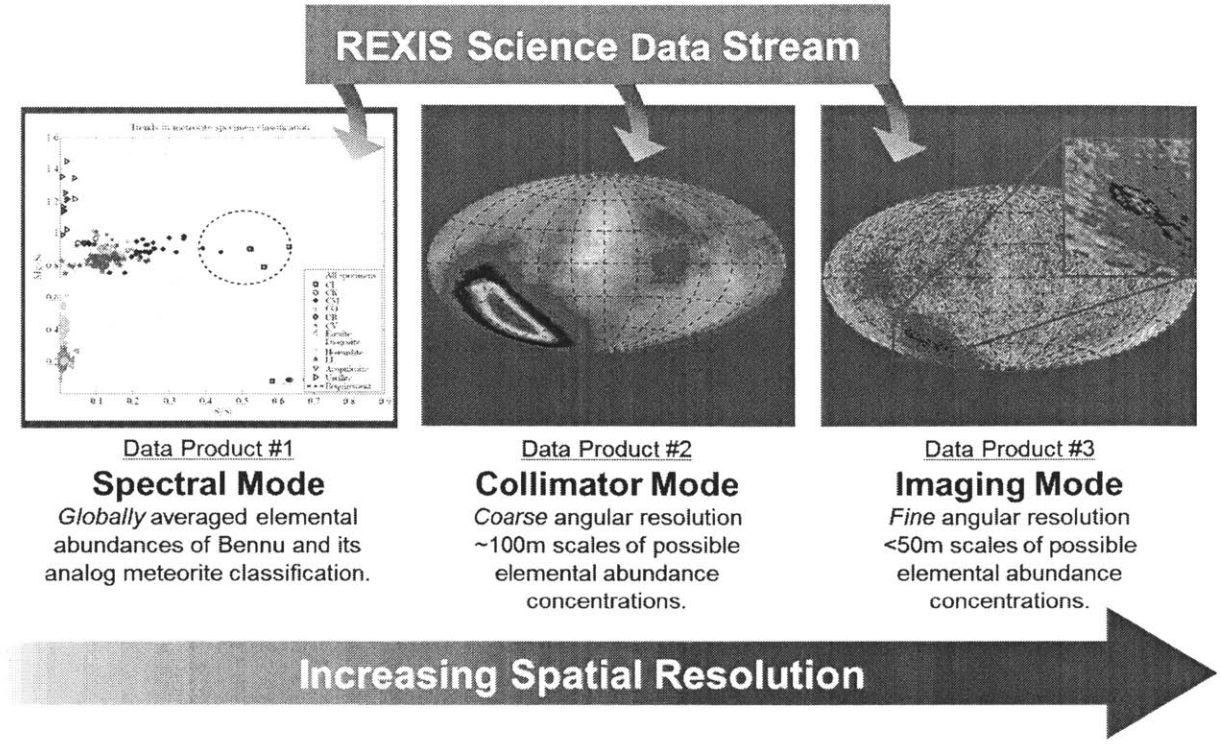

Figure 1-5: REXIS Scientific Data Products [10]

Three different scientific products are produced from REXIS telemetry that indicate the composition of Bennu's regolith with varying spatial resolutions of Bennu's surface, as shown in Figure 1-5. As the spatial resolution of REXIS scientific products increases, the resolution of elemental concentrations decreases. This resolution decrease occurs because there are fewer photons for smaller areas of Bennu to make detailed spectral histograms. The Spectral Mode data in Figure 1-5 is generated by creating an x-ray energy histogram that includes all of the photons emitted by Bennu's regolith. This large quantity of photons from all of Bennu ensures a high resolution of elemental concentration values for the entire asteroid surface. Collimator mode data is produced by taking REXIS's 200 meter wide field of view (FOV) on the asteroid's surface into account. Photons from the same 200-m wide FOV footprints on Bennu are grouped into an image of Bennu's elemental abundances with a 200-m spatial resolution. However, collimator mode images have less elemental abundance resolution when compared to Spectral Mode data. Similarly, Imaging Mode uses coded aperture imaging to resolve areas within the 200 meter FOV footprints and determines elemental concentrations at finer spatial resolutions. High resolution elemental abundance data in Spectral Mode is used to classify Bennu among other asteroids in the Solar

System while high resolution spatial data from imaging mode may be used to help select a regolith sample site. Furthermore, high accuracy instruments on Earth will determine the elemental composition of the asteroid sample. This composition data will be compared to REXIS Imaging Mode science data to determine the effectiveness of XRF and coded aperture imaging at an asteroid [10].

1.3.2 REXIS System Description

REXIS senses x-rays emitted by Bennu and the Sun with two separate mechanical assemblies known as the main spectrometer and the SXM. Figure 1-6 shows the placement of these REXIS components aboard the OSIRIS-REx spacecraft. The main spectrometer is aimed towards Bennu along with the other remote sensing instruments mounted on the instrument deck. The SXM is mounted so that it monitors the Sun whereas the main REXIS spectrometer monitors Bennu. These two assemblies are connected with wiring harnesses. The REXIS instrument uses another set of wiring harnesses to interface with the OSIRIS-REx spacecraft. These harnesses provide electrical power and conductors used for digital communication. This digital communication consists of sending commands to and receiving telemetry from the REXIS instrument.

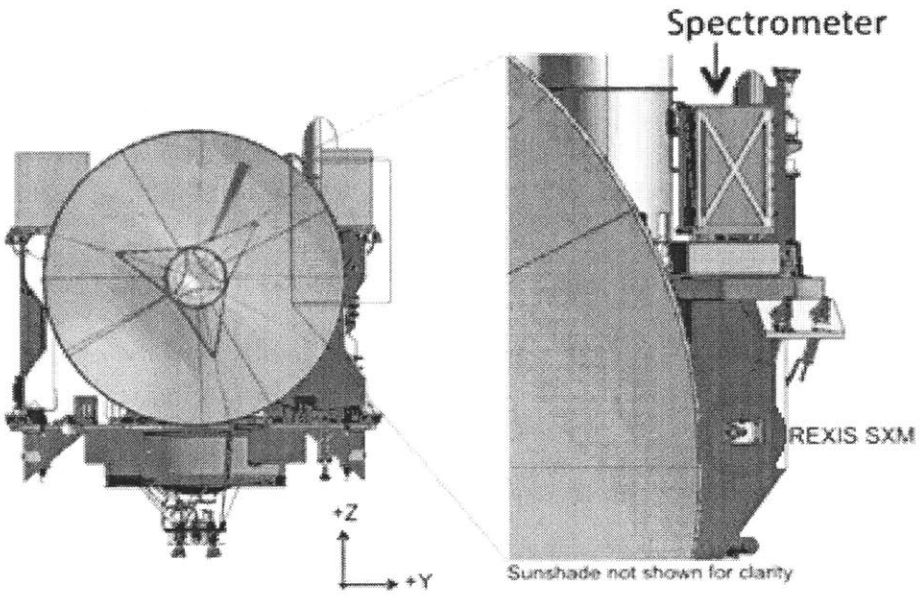

Figure 1-6: REXIS Main Spectrometer and SXM Aboard OSIRIS-REx (Credit: Lockheed Martin)

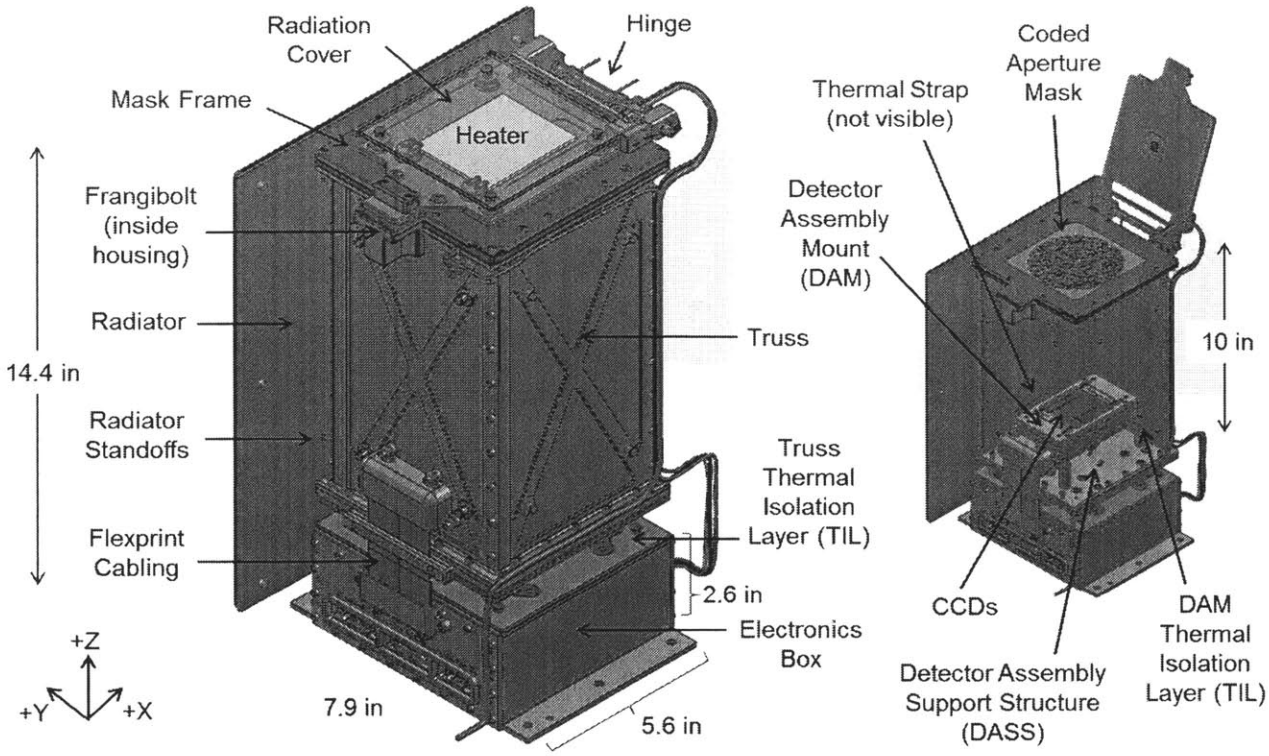

Figure 1-7: REXIS Spectrometer Physical Overview [3]

Figure 1-7 details the physical components that form the REXIS main spectrometer assembly. At the center of the instrument (seen within the cutaway model on the left of Figure 1-7) are the four Charge Coupled Device (CCD) sensors arranged in a 2x2 array. These CCDs are CCID-41 sensors that are an array of x-ray sensitive pixels. These pixels convert the energy of an x-ray photon into electrical current. The CCDs are sensitive to the soft x-ray range of 0.3 keV - 7.5 keV [12]. The REXIS system supports the CCDs with the following subsystems in order to produce quality scientific data:

1. **Radiation Cover and Shielding** – Because the CCDs degrade with exposure to radiation, the aluminum mass of the REXIS truss and radiation cover are designed to reduce the total radiation dose the CCDs receive while flying through space. Once REXIS is arrives to image the asteroid Bennu, the radiation cover opens through the actuation of a TiNi Aerospace FD04 Frangibolt mechanism. When electrical current is applied to the Frangibolt by the avionics system, it is designed to fracture a bolt that holds the radiation cover closed. Once the bolt is fractured, torsion springs open the radiation cover and permanently hold it open [3].

2. **Thermal Isolation and Passive Cooling** - The CCDs are mounted in a Detector Assembly Module (DAM) that is thermally isolated and radiatively cooled to reduce temperature-dependent noise in the CCD output signal. This thermal management system consists of two thermal isolation layers that prevent the avionics heat energy from flowing to the DAM and a passively operating radiator that dissipates the CCD sensor's heat energy into outer space through radiative heat transfer [13] [14].
3. **Coded Aperture Mask** – The coded aperture mask is shown in Figure 1-4 and consists of a stainless steel sheet with a circular pattern of randomly placed holes. In total, these create a 50% open-fraction and there is a 0.15mm wide support grid that runs between each hole and opaque portion of the mask [10].
4. **Electrical CCD Drive and Readout** - Electronics within the electronics box power the CCDs and read data from them. The REXIS electronics transmits CCD drive voltages and receive CCD pixel data through flexible printed circuit boards known as flexprints. This CCD-derived data is used to create the REXIS science telemetry.

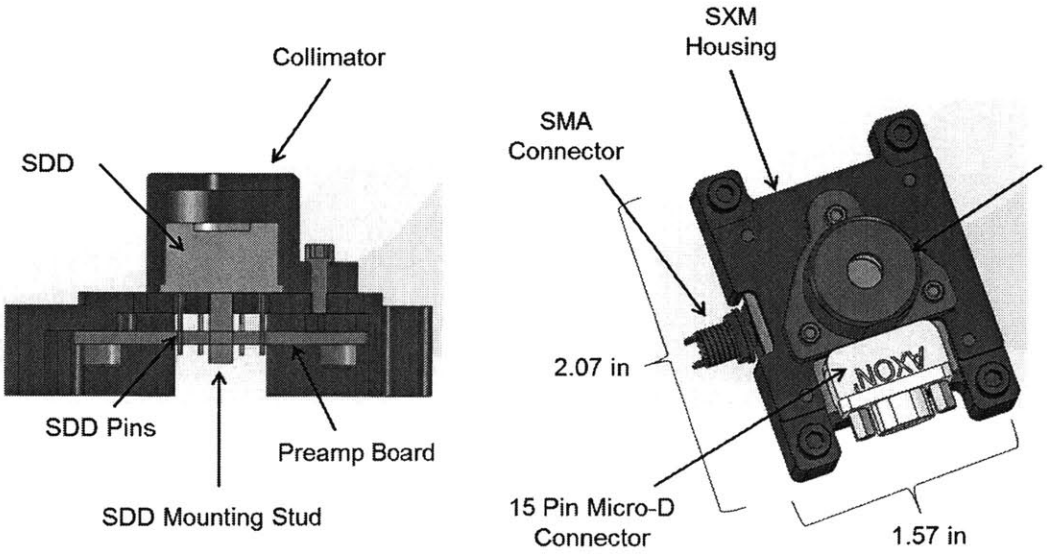

Figure 1-8: REXIS SXM Physical Overview [8]

The other component of the REXIS is the SXM. Similar to how the main spectrometer is built around the CCD sensors, the SXM is built around the Silicon Drift Detector (SDD) x-ray sensor as shown in Figure 1-8. The electronics that operate the SDD sensor are split between the main spectrometer's electronics-box and SXM assembly (Figure 1-8). The spectrometer electronics provide a high voltage bias voltage for the SDD, power for the SDD's preamplifier, and power for the SDD's built-in thermo-electric cooler (TEC). Unlike the CCD's passive cooling system, the TEC uses electrical power to keep the SDD at its operating temperature. The SDD converts x-rays that travel through the collimator (used to restrict the SDD's FOV) into electrical pulses. These pulses are amplified by the SXM's preamplifier circuit on an SXM Electronics Board (SEB), sent over a coaxial cable wiring harness, and counted/measured by the electronics within the REXIS electronics box. A coaxial cable is used to transmit the analog SDD pulses amplified by the SEB for its superior noise-rejection compared to normal wiring. The other electrical signals required to operate the SXM such as the high voltage bias, power, and ground, are provided through a separate wiring harness between the SXM and the main spectrometer.

1.4 Thesis Roadmap

This chapter presents the background and motivation behind this thesis, an overview of the OSIRIS-REx system, and an overview of the REXIS system within OSIRIS-REx. The REXIS system has been introduced within the context of the larger OSIRIS-REx project and the need to share the experience and lessons learned from high-risk low-cost avionics design. The rest of this thesis will delve deeper into these ideas with the following chapters.

- Chapter 2 introduces the space radiation hazard and how it affects avionics in general. Emphasis is given to the adverse effects of space radiation and how avionics are typically designed to avoid or mitigate these effects.

- Chapter 3 details the REXIS avionics system that is the main subject of this thesis. The functionality, hardware, software, and FPGA[3] design are explained in this chapter.
- Chapter 4 describes how the REXIS avionics system is designed to function as it is bombarded with space radiation. REXIS's cost-saving designs for mitigating the radiation hazard are highlighted.
- Chapter 5 concludes this thesis with lessons learned from designing, testing, and operating the REXIS avionics system. These lessons can also be generalized to other avionics systems.

In short, this thesis presents the design, development, and testing of the REXIS avionics system. Successes and failures that occurred during the REXIS avionics project are presented and can be used as a learning guide for future missions.

[3] Field Programmable Gate Array – A microchip that contains an array of digital logic and computation hardware. This hardware and its interconnections can be reconfigured to implement digital computing functionality

Chapter 2 - Interaction of Space Radiation and Electronics

The OSIRIS-REx mission imposes a 3-year operational lifetime on the REXIS instrument in the interplanetary space radiation environment because of the spacecraft's 2.5 year cruise to Bennu. Without proper precautions, radiation has a damaging and degrading effect on system performance. This chapter discusses the effects of space radiation on the operation of avionics. First, the space radiation environment is presented and compared to radiation sources found on Earth. Then, transient and permanent radiation-caused avionics malfunctions are discussed. Finally, techniques to mitigate this damage and prevent system malfunction are presented.

2.1 Space Radiation Environment

Space radiation consists of highly energized subatomic particles and atomic nuclei. Radiation in outer space originates from a variety of sources ranging from normal stars to exploding supernovae. Radiation particles can also accumulate in planetary magnetic fields and become hazards for avionics operating within these areas. For Earth, such areas where radiation is trapped by the Earth's magnetic field are known as the Van Allen belts [15].

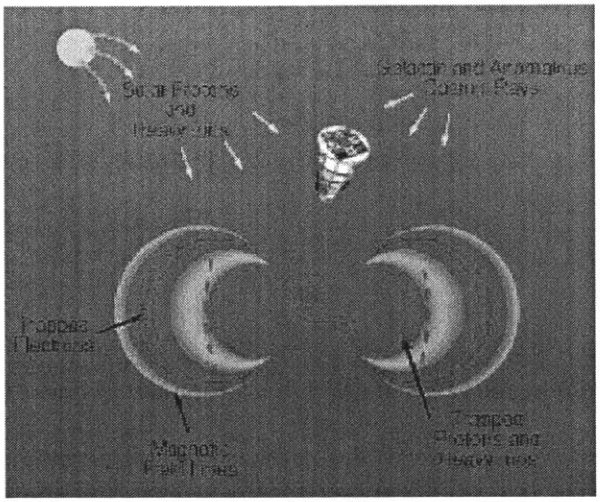

Figure 2-1: Origins of Space Radiation (Credit: NASA Space Environments and Effects Office[4])

Radiation damages electronics by putting too much energy and charge into sensitive places within the electronics' physical micro-architecture. Space electronics designers must account for radiation coming from three different hazards shown in Figure 2-1. Two of these hazards that create space radiation are Solar Particle Events (SPEs) from our Sun, and Galactic Cosmic Rays (GCRs) from extra-solar sources such as supernova [16]. The third radiation hazard for spacecraft are planetary magnetic fields which trap and accumulate energetic charged subatomic particles originating from the previous two sources around planetary bodies. The radiation dose caused by these particles is measured in the unit of rad which is defined as one erg (10^{-7} Joules) of energy absorbed by one gram of material. One rad may appear as a small amount of energy, but when such energy continuously accumulates within microchip circuits measured in atom-widths during the many years of a spaceflight mission, it can negatively affect operation and functionality.

Spaceflight missions usually have low radiation dose rates and high accumulated radiation doses compared to conditions found in Earth's laboratories. While Earth orbits outside the Van Allen belts can be characterized with low dose rates ranging from 10^{-4} to 10^{-2} rad/second, years of operation in these orbits can result in a high accumulated dose in the order of 10^{5} rad [17]. The space radiation environment

[4] Taken from URL: http://holbert.faculty.asu.edu/eee560/tiondose.html

is difficult to replicate on Earth due to constraints from time and available equipment. More specifically, it is impractical to test a newly developed spaceflight components at all possible orientations continuously for years on end.

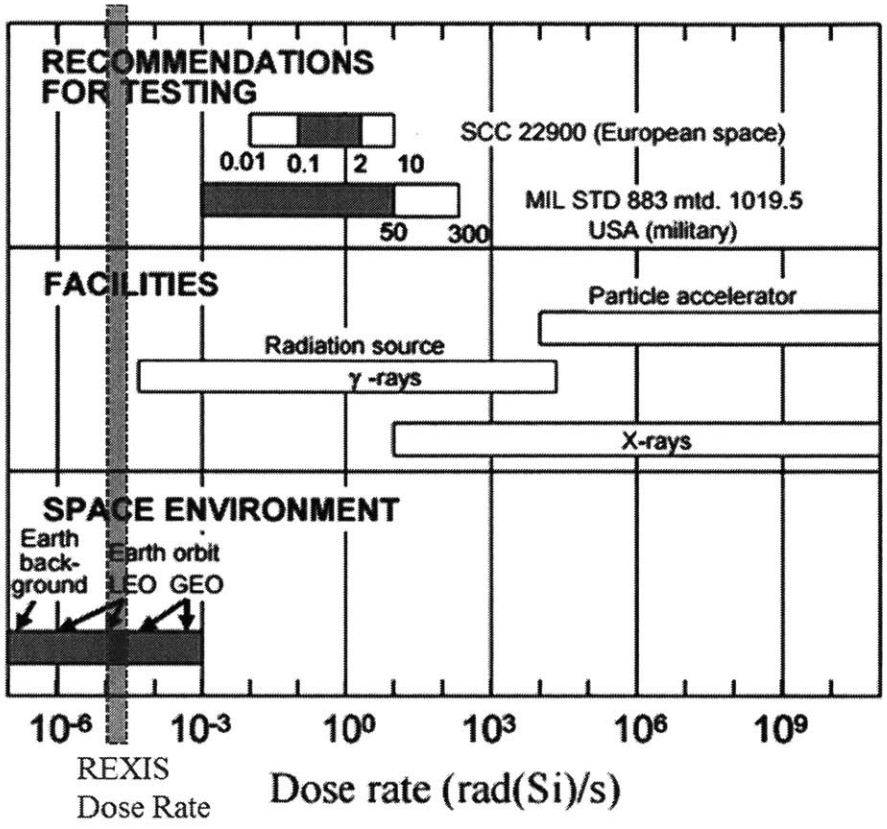

Figure 2-2: Dose-rate Comparison of Earth-based Radiation Sources and Space Radiation [18]

The difference in dose rates on Earth and space is shown in Figure 2-2 where the bottom third of the figure shows the low dose rate in space and the middle third shows the dose rates that are practically available through various testing facilities such as X-ray sources, gamma-ray sources, and particle accelerators. These facilities create dose rates notably higher than the space dose rates but have the benefit of allowing radiation testing to be completed in a reasonable timeframe of hours/days instead of years for a given component at a particular dose. However, high dose-rates are not representative of space so typically parts are over-designed and over-tested to ensure they continue to work reliably in the space environment [17].

Furthermore, radiation in space bombards components from all directions. This effect is usually simulated by rotating parts within radiation sources. Each new orientation requires a new part and this quickly adds time and cost to testing. New parts are needed for testing each orientation since allowing radiation dose to accumulate within a single continuously rotated part simultaneously tests the independent variables of dosage accumulation and sensitive to radiation angle-of-incidence. Thus, component degradation observed from testing cannot be conclusively attributed to dosage accumulation or radiation angle-of-incidence.

The time-wise and location-wise variation of the space radiation environment requires that a system or component be designed, optimized, and vetted to operate in specific conditions. Location-wise, the three radiation hazards have different energy distributions, fluxes, and are dominant in different areas of outer space. Time-wise, the 11-year period of the solar activity cycle causes the GCR flux and SPE flux to vary inversely. An example of the location-oriented radiation dose variation is within the various Earth orbits that intersect the trapped radiation regions of Earth's magnetic fields at varying levels. Lower energy radiation hazards such as SPEs and trapped ions are simulated with radioactive x-ray or gamma-ray sources while the testing high energy hazards like GCRs requires the use of particle accelerators. The following paragraphs describe these three sources of space radiation in detail.

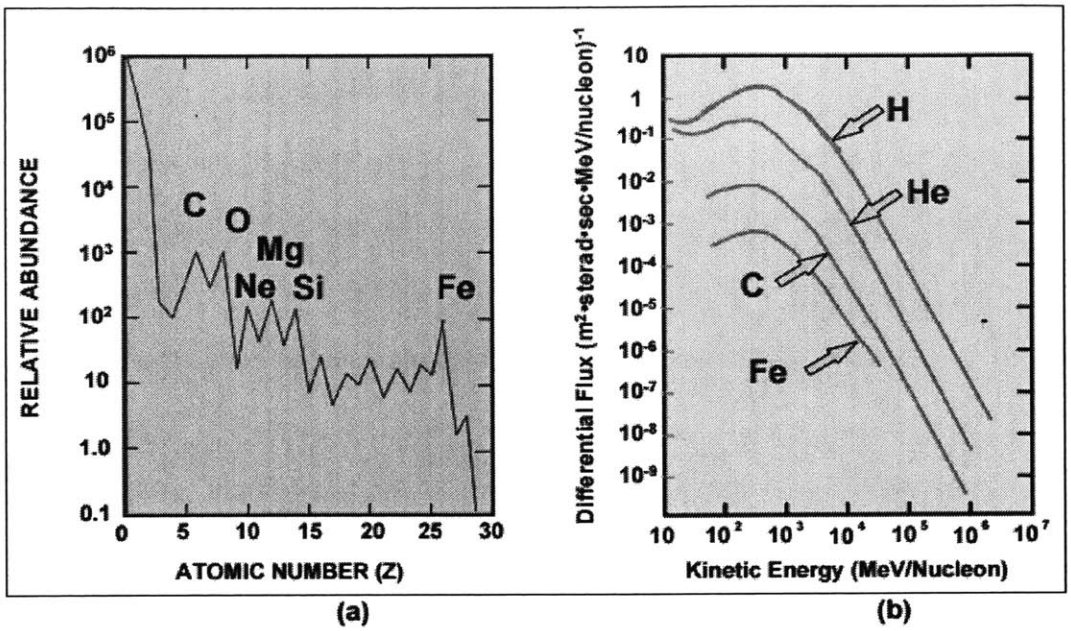

Figure 2-3: Abundances (a) and Energy Spectra (b) of Galactic Cosmic Radiation (GCR) [19]

Galactic Cosmic Rays - Spacecraft must contend with energetic charged particles that originate from sources beyond the solar system. These charged particles are known as the Galactic Cosmic Rays (GCRs) and consist of a variety of nuclei ranging from hydrogen to iron that originate from various supernovae. Figure 2-3 shows the distribution of atomic nuclei that form GCRs and the various energy distributions that these nuclei have [19]. GCRs are unique since they sometimes consist of very heavy atomic nuclei like Iron or Carbon while the vast majority of space radiation consists of energetic much lighter electrons and protons. Heavy nuclei from GCRs can only be simulated by particle accelerators on Earth and are particularly damaging to electronic semiconductors [17]. The high mass of GCR particles contributes to the overall high energy levels of GCRs when compared to SPEs. This excessively high energy makes it practically impossible to shield components from GCRs [20].

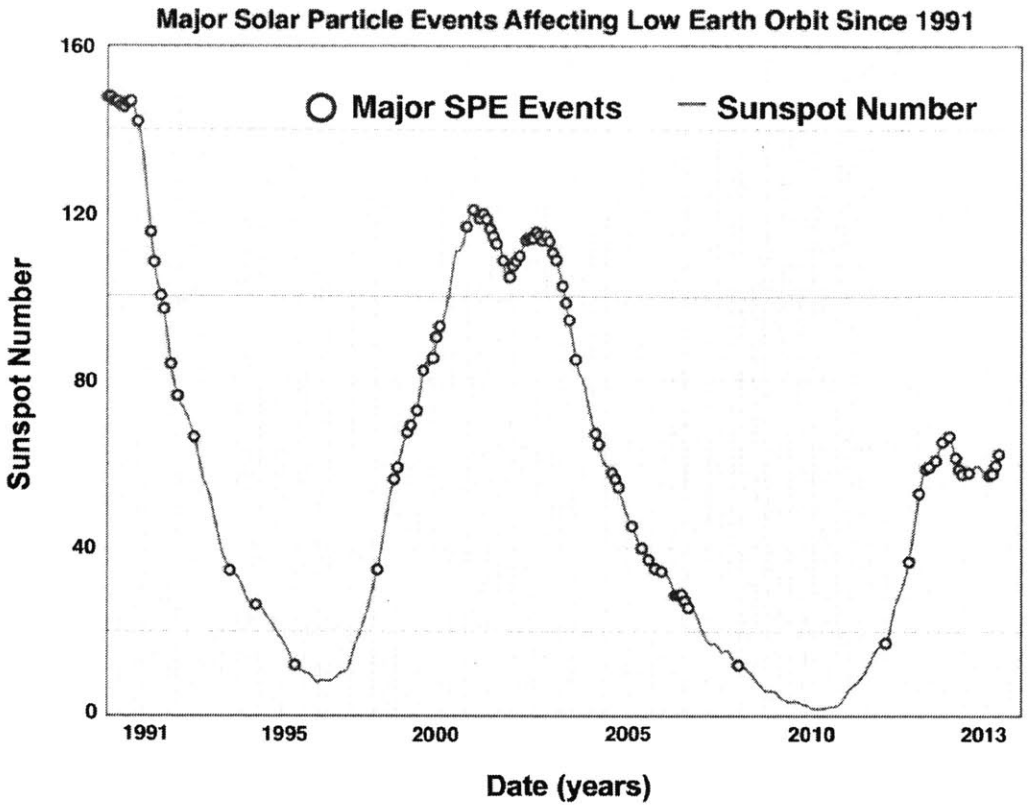

Figure 2-4: Sunspot Count vs. SPE Occurrences with 100MeV Protons [15]

The intensity of GCRs within the solar system is dependent on the 11-year solar cycle. The solar magnetic field also varies with the 11-year solar cycle and when the solar-cycle peaks, the solar magnetic field blocks GCRs. During periods of solar maximum, the flux, or number of ions per unit area, decreases by a factor of two [20].

Solar Particle Events - Solar Particle Events (SPE) are primarily emissions of protons and a few heavy ions from the sun. These energetic charged particles are emitted from solar flares during periods of high solar activity. Solar activity has lulls and peaks that follow an 11 year cycle [15]. Figure 2-4 shows solar activity for 22 years as a subset of the solar sunspot cycle with the number of visible sunspots plotted on the y-axis vs time on the x-axis. Major SPEs containing highly energetic protons (>100MeV) are marked with red circles. The greatest concentrations of the major SPEs align with periods of high solar activity or high sunspot counts. Typically SPEs have much lower energies than GCRs but their flux is much greater within the Solar System.

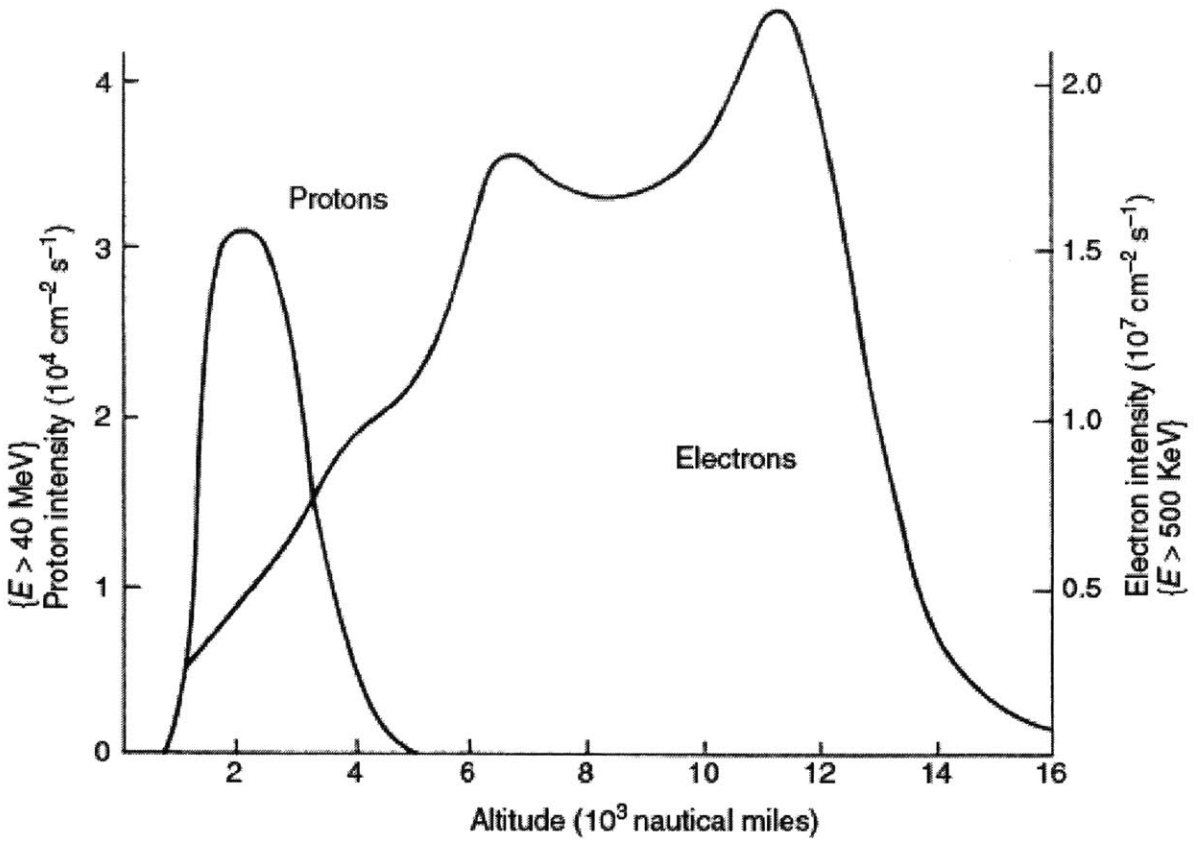

Figure 2-5: Structure of the Van Allen Belts (Idealized) [21]

Planetary Magnetic Fields - Energetic charged particles originating from the Sun such as protons, electrons, and other ions can be trapped by magnetic fields in the solar system. For example, the magnetic fields that surround the Earth and Jupiter trap these energetic particles and become radiation hazards for spacecraft. The Earth's magnetic field is of interest since the vast majority of spacecraft operate within it whereas Jupiter's magnetic field is notable because it traps many more solar charged particles than Earth's field. Since Jupiter has the strongest planetary magnetic field, it is a significant hazard to Jovian spacecraft [22].

The particle concentration of Earth's magnetic field is shown in Figure 2-5 while the location of these particles around Earth is shown in Figure 2-1. At altitudes within the upper end of Low Earth Orbit (LEO) beyond the 215 nautical mile altitude orbit of the International Space Station, the radiation environment is primarily trapped solar protons. As orbit altitude increases, trapped solar electrons become

the dominant radiation hazard. However, most satellites operate either in LEO or geostationary orbit which is much higher than the Van Allen belts in Figure 2-1 to avoid this radiation hazard.

2.2 Radiation-caused Electrical Malfunctions

Space radiation negatively affects the operation of space electronics by depositing charge and energy within the micro-architecture of integrated-circuit microchips. This transfer of energy causes malfunction through one of the following mechanisms [17]:

1. Permanently changing the composition and structure of the semiconductors that comprise electronic circuits
2. Causing transient voltage or current spikes within electronic circuitry
3. Creating unwanted state changes in computer memory elements

Depending on the semiconductor architecture and the magnitude/direction of the disruption, the electronics may recover from a temporary failure or become permanently damaged/degraded [17].

Radiation can either cause temporary or permanent malfunctions in radiation-tolerant electronics. The persistence of a radiation-caused malfunction depends on the electronic/radiation interaction and electronic design. A permanent malfunction is characterized by an irreversible change in the electronic device's physical makeup that affects functionality. A transient malfunction will go away after waiting for a certain time period, power cycling, or invoking any other features that returns the device to its normal state. Examples of these features are automatic processor resetting after a fault occurs, correcting data corrupted by radiation, retaking radiation corrupted measurements, or switching to a back-up while the radiation-affected system recovers.

Transient effects that do not cause permanent damage to an appropriately designed avionics system are presented first in this subsection. These are collectively known as Single Event Effects (SEE) and only occur within electronics that are already powered and operational. The SEE category can be divided into Single Event Upsets (SEUs), Single Effect Transients (SETs), and Single Event Latch-up (SEL).

SEEs only affect electronics that are powered on. The final three topics are Single Event Gate Rupture (SEGR), Total Ionizing Dose (TID) and Total Non-Ionizing Dose (TNID) that permanently affect the operation of electronics that are both on or off.

2.2.1 Single Event Upset

Single Event Upsets (SEUs) occur when an energetic radiation particle is absorbed by a transistor and causes the transistor to change its state in a digital circuit. Transistors are either on or off in digital circuitry, and a SEU will undesirably toggle the transistor's state. The amount of energy a transistor must absorb for an SEU to occur depends on the transistor size, composition, angle of radiation incidence, and energy of the radiation particle. Digital circuitry in general is vulnerable to SEU-caused malfunctions since their transistors seldom operate between the on and off transistor states. For example, digital computer memories, which consist of transistors, are typically affected by SEUs. A SEU can persist in memory if the avionics system is not built to handle it. However, the SEU hazard can be resolved with appropriate algorithms to mitigate the malfunction.

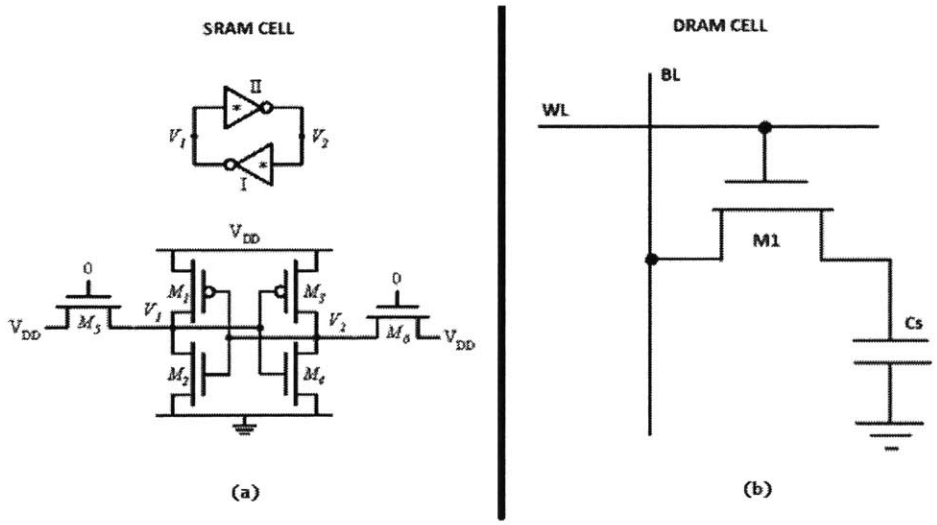

Figure 2-6: SRAM[5] (a) and DRAM[6] (b) Memory Cells

[5] Diagram taken from "Ultra Low Power SRAM Design" by Huifang Qin and Jan M. Rabaey at the UC Berkeley Wireless Research Center. URL: https://buffy.eecs.berkeley.edu/PHP/resabs/resabs.php?f_year=2006&f_submit=chapgrp&f_chapter=5

[6] Diagram taken from "DRAM – An Intro". URL: https://allthingsvlsi.wordpress.com/tag/dram-cell/

The two types of radiation susceptible memory common in avionics systems are Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). These computer memories are composed of many memory cells and the circuitry for reading/writing data to/from these cells. SRAM and DRAM memory cells both utilize transistors as shown in Figure 2-6. SRAM on the left can be thought of two interconnected inverter circuits that can take on two states – either V_1 is high and V_2 is low or vice versa. These two states correspond to one bit of digital data and can be read/written to with external circuitry. The bottom left of Figure 2-6 shows the transistor-based implementation of an SRAM cell. The right side of Figure 2-6 shows a DRAM cell stores the value of one digital bit in a capacitor, with transistor M1 reading/controlling the value of this bit.

If any of the transistors in these memory cells are disrupted by radiation, then the data stored in the memory cell can be corrupted. This failure is known as a SEU and could cascade into an avionics system malfunction depending on which memory cell is affected and the ability of the system to handle these failures. Energetic protons or heavy ions can deposit dangerously high levels of energy inside the transistors of an electronic memory circuits shown in Figure 2-6. This excess energy is dangerous because it corrupts data stored in digital memory by unwantedly causing the transistors in a digital memory cell to conduct electricity. This unwanted conduction of electricity causes the memory cell to change state and corrupts the digital data in the memory cell [12] [17]. Improperly designed space electronics that cannot detect and correct corrupt data can result in SEUs causing permanent issues.

SEUs can also corrupt the SRAM memory that is frequently used by microchips to store their internal configuration necessary to implement avionics functionality. This type of malfunction is known as Single Event Fault Interrupt (SEFI) and can prevent these microchips from operating correctly. An uncorrected SEFI will propagate through the operation of the microchip and could cause the wrong instructions to be executed by a microprocessor or corrupt reconfigurable digital logic circuitry within a Field Programmable Gate Array (FPGA) microchip [12].

2.2.2 Single Event Transient

The passage of a charged particle near an electrical circuit node can cause transient currents in that node. By interacting with other circuit components, these currents cause transient voltages [3]. This process is known as a Single Event Transient (SET). SET-caused voltage spikes can show up as noise within instruments and analog circuitry [17]. In the case of REXIS and other space-based instruments with analog electronics, SETs decrease the resolution of scientific telemetry due to the spurious signals it causes.

If a SET-caused voltage spike is clocked into digital circuitry without triggering a fault, the error can propagate through the system and cause permanent damage [17]. Higher clock speeds make a digital system more vulnerable to SET but design that detects and resolves radiation-caused faults ensures that SET cause transient malfunctions [23]. SETs cause transient voltages that can be erroneously interpreted by digital circuitry [17]. Higher clock speeds mean more of these interpretations and calculations per second, and thus increase the chances of SET errors [17].

2.2.3 Single Event Latch-up

Single Event Latch-up (SEL) occurs when radiation causes unwanted conduction and high currents in Complementary Metal Oxide Semiconductor (CMOS) transistors. The (CMOS) transistors used in space electronics have alternating layers of P-type and N-type silicon that form a parasitic thyristor[7]. SEL occurs when charge deposited from space radiation creates small but abnormal currents in the CMOS base layer. This current provides the initial energy to cause the MOSFET's parasitic thyristor to start conducting electricity though a positive feedback loop. Left unchecked, this SEL causes a damaging over-current event that overheats and destroys the small and sensitive electronics within microchips [23].

[7] A thyristor is an electrical semiconductor component that allows small voltages at one terminal to control large currents at other terminals. The small voltage causes a positive feedback loop within the thyristor that facilitates the conduction of large currents.

Without built-in protection, SELs can cause permanent damage in circuitry. If the circuit undergoing SEL has no current limiting or the circuit is not shut off in time, then the high current caused by the latch up will cause permanent damage through overheating. Circuits with current limiters or over-current detectors will stop the heat build-up from SEL by limiting power to the SEL affected circuit. There will be a temporary lapse in functionality, but the circuit will not have permanent damage. For low-power circuitry, a current limiter could be a simple resistor on the supply line. Higher power circuitry requires more complex electronics that actively detect and cut power to remove the overcurrent fault.

2.2.4 Single Event Gate Rupture

Single Event Gate Rupture (SEGR) is caused by ionizing space radiation that deposits enough charge within certain transistors to permanently damage the control terminal of a transistor, known as the gate. Transistors affected by SEGR are the Metal Oxide Semiconductor Field Effect Transistors (MOSFET) that are used in modern digital electronics, where the gate is electrically isolated from the rest of a transistor with a non-conductive dielectric layer. Ionizing radiation can deposit enough charge on the dielectric layer to break it down. This breakdown causes a brief but damaging current flow that damages the MOSFET by electrically connecting the gate to the rest of the transistor. The damage mechanism is similar to charge building up in clouds, causing lightning but on the microscopic scale of a transistor. Using MOSFETs well below the voltage limits that it is rated for greatly reduces the chance of SEGR [17].

2.2.5 Total Ionizing Dose

Total Ionizing Dose (TID) is a measure of radiation dose accumulation caused by prolonged exposure to radiation in space that can cause permanent damage to electronics. While an electronic component is in outer space, ionizing radiation deposits charge that accumulates within semiconductors that form the component's circuitry [23]. This additional charge changes the composition of circuit components that in turn affects operation speed, threshold voltages, and overall functionality [17] [23].

This composition of circuit components is formally known as doping, and is defined as the concentration of charge within a volume of semiconductor. Modern integrated circuits consist of differently doped regions of a semiconductor like silicon or gallium arsenide that form interconnected transistors. As TID increases, the semiconductor doping changes and leads to poorly operating transistors.

Low radiation dose rates cause more damage to electronics than the high dose rates that electronics are typically tested with on Earth. This susceptibility to low dose rates is known as Enhanced Low Dose Rate Sensitivity (ELDRS) and space-grade electronics are designed to be less susceptible to ELDRS. On a typical geostationary orbit space mission of several years, the TID accumulates to around 10^5 rad [17]. Typically devices are tested to levels of 10^6 rad with a higher dose rate on Earth than that experienced in outer space. This margin of an order of magnitude radiation dosage difference is needed because of the ELDRS vulnerability and impracticality of testing a component continuously for years. The underlying cause for the ELDRS vulnerability is unknown and an area of active research.

TID also has serious long term effects on analog electronics. Within analog circuitry, voltage thresholds, characteristic response, and current-voltage curves change from radiation exposure. Changing these parameters usually has negative effects on the power consumption, noise, accuracy, precision, and overall operation of analog electronics [17] [24]. These TID-caused circuitry changes are permanent so avionics designers must account for this gradual degradation over the circuitry's operational lifetime.

Unlike analog circuitry, once the TID radiation dose goes beyond a certain level, digital circuitry abruptly stops working [25]. Digital electronics quickly change status from operational to defective because their internal components are supposed to exist in distinct "on" or "off" states, and TID interferes with this neat categorization. The transition between these states is dictated by a voltage threshold. TID causes this threshold to drift over time. If the threshold changes slightly, the electronics would still function normally, but there could be increased current drawn since the circuit is slightly deviating from the operating point that it was designed for. However, once these TID-caused threshold changes become severe enough to violate the definitions of digital logic – the voltages defining the "on" and "off states – the digital electronic component will abruptly stop working. Degradation in digital electronics is different

from analog electronics since TID degradation in analog electronics is immediately evident because analog circuitry has a continuous range of operating voltages.

2.2.6 Total Non-Ionizing Dose

Another source of long-term radiation-caused damage similar to TID are high-energy neutrally-charged particles measured in terms of Total Non-Ionizing Dose (TNID). Exposure to non-ionizing radiation causes the crystalline structure of electronic semiconductors to become riddled with irregularities in contrast to TID that changes the charge of electronic semiconductors. These radiation-caused defects are known as displacement damage and they degrade the performance of CCDs, solar cells, and linear regulators [17]. Displacement damage will damage semiconductor crystal structures and permanently degrade the charge transfer efficiency [17]. This degradation negatively affects the pixel readout of CCDs, voltage output from voltage references, and power output from solar panels. Like damage from TID, displacement damage is always accumulating, even if the space electronics in question are turned off.

2.3 Techniques for Radiation Risk Mitigation

Avionics designers implement a variety of techniques to prevent radiation-caused malfunctions and gracefully recover the avionics system when these malfunctions occur. Collectively these techniques are known as avionics design for radiation (DFR). More specifically, design decisions that address and mitigate radiation-caused malfunctions fall within the category of DFR.

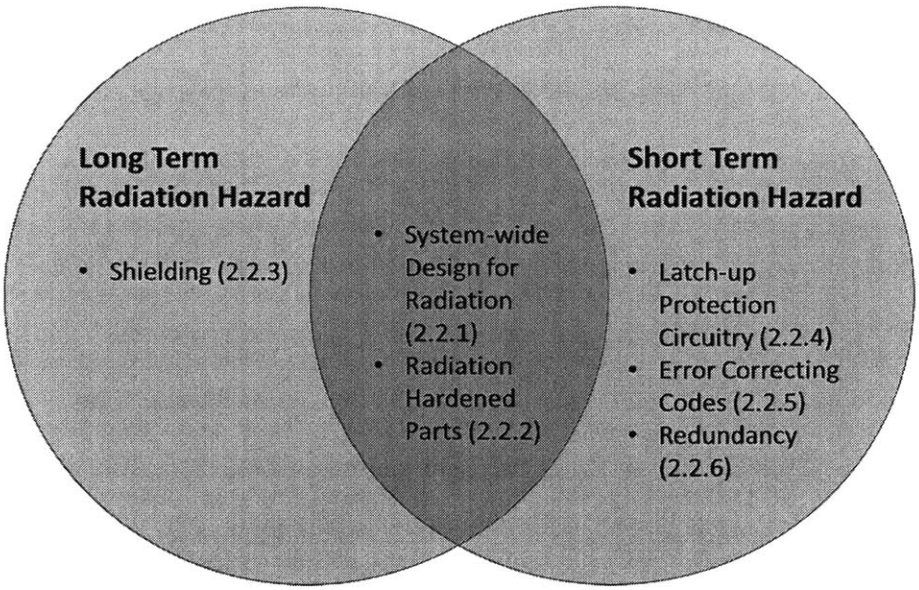

Figure 2-7: Radiation Hazard Mitigation Techniques

DFR techniques protect against both the long term effects of radiation like TID and displacement damage and short term transient effects created by SEEs. DFR methods add complexity to space system avionics but ensure that these circuits can function and allow the space system to meet its requirements. DFR techniques can be grouped using two criteria: the radiation hazard the technique addresses and the avionics complexity required to implement the technique. Mitigating and recovering from SEE-caused malfunctions and long term radiation-caused degradation require the implementation of different approaches in the electronics design as shown in Figure 2-7. Some of these approaches are effective against both long and short term radiation exposure. Furthermore, the implementation of radiation hazard mitigation techniques range from simple to complex. An example of a simple technique is using a current limiting resistor on a power supply line to prevent damaging currents from Single Event Latch-up (SEL) hazards. On the other hand, a complex technique is triplicating critical functionality to compare the three results for consistency and correctness [17].

It is important to realize that these groupings are convenient, but they are mainly superficial. A single technique cannot fall squarely in the simple or complex categories. For example, the implementation of current limiting resistors requires an electrical power system that can continuously

support the significantly increased current draw of a latched-up component until the component is shut down. For certain low-power electrical systems, accommodating this extra current on top of nominal power consumption can add further complexity. On the other hand, using triple modular redundancy to redundantly compute and compare values could be simple to implement in an FPGA-based design if there are enough digital logic resources available on the FPGA and the FPGA manufacturer provides a standardized way to triplicate functionality [17] [23].

2.3.1 System-wide Design for Radiation

The design of a radiation tolerant avionics system must first take the whole space system and operational environment into account. In other words, it is important to adjust other non-avionics aspects of the system like orbit design, enclosure thickness, or functionality uptime requirements to establish reasonable radiation tolerant derived requirements for the avionics system. Failing to do so can cause unnecessarily burdensome radiation tolerance requirements on the avionics system when there could be a potentially straightforward system-wide design decision when taken early-on in the project lifecycle, provides the same radiation tolerance. Two examples of system-wide parameters affecting avionics radiation tolerance are orbit/trajectory designs and the operation of subsystems/components in a conservative manner. A proper radiation-conscious orbit design will avoid radiation hazards instead of imposing difficult radiation tolerance requirements on the avionics system. Meanwhile, designing an avionics system to operate with parts that are conservatively accommodated or can tolerate intermittent functionality loss can lead to a more feasible design that doesn't rely as much on costly component-wise radiation tolerance techniques.

Concepts of Operation (Con-ops), mechanical design, and orbit trajectories can sometimes be adjusted to reduce radiation dosage while still delivering the same science returns. A simple example of this is a CCD imaging sensor that would output an unacceptable level of noise due to exposure to TID and displacement damage due to the current orbit design. This problem can be avoided by designing the spacecraft trajectory to collect the most desired scientific data early-on in the mission with undamaged

sensors or upgrading the CCD's cooling system to reduce thermal noise and still stay within the noise requirement [17] [22]. For example, in the case of REXIS, the CCDs are enclosed in opaque aluminum shielding and a radiation cover opens to expose the CCDs to the asteroid they are supposed to image. Another example is placing space telescope exclusively in Low Earth Orbit (LEO) to minimize TID since the Earth's magnetic field limits radiation exposure [26].

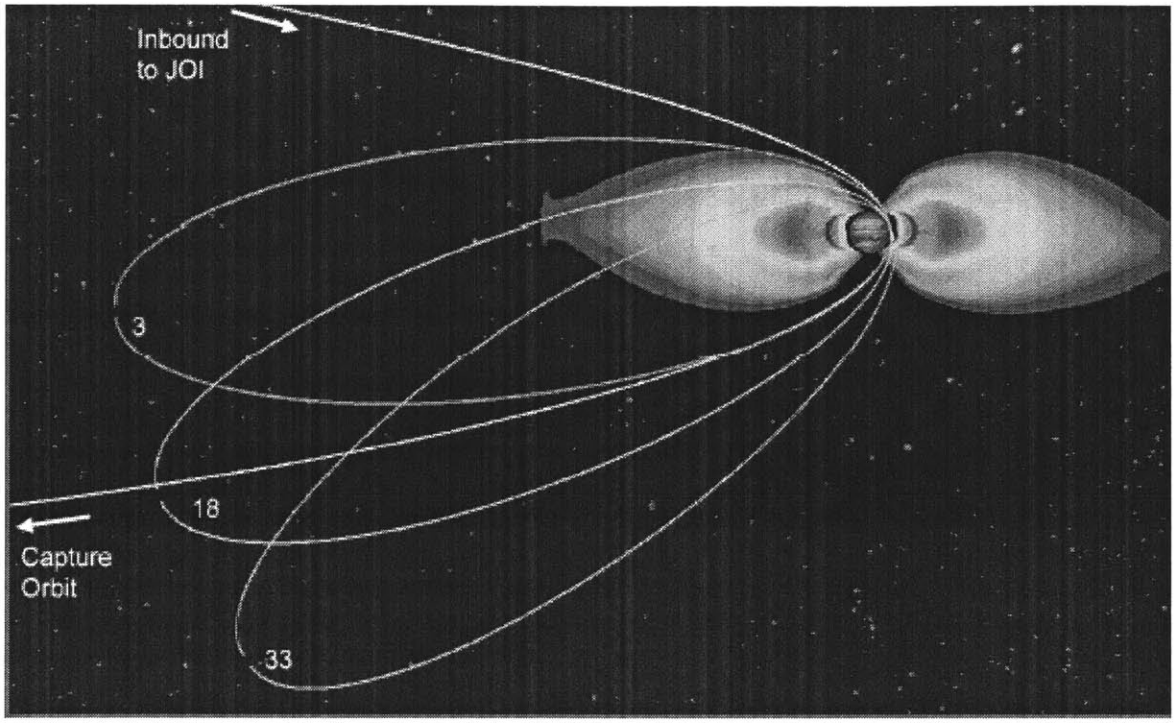

Figure 2-8: Perijove Passage through Jupiter's Radiation Environment [22]

A specific example of designing orbits to avoid radiation exposure is shown in Figure 2-8 that describes how the Juno spacecraft's orbital trajectory was designed to postpone flying though the radiation belts of Jupiter. The top of Figure 2-8 shows the beginning of the Juno mission with Jupiter Orbit Insertion (JOI) and the progression of the Juno spacecraft's orbits that slowly dip into the Jupiter radiation belts. All of the initial orbits around Jupiter (example: orbit 3 in Figure 2-8) have a benign radiation environment and Juno receives most of the Jovian TID in its last few orbits [22]. More specifically, orbit 3 of Juno in Figure 2-8 completely misses the colored radiation belts while the later orbits like 18 and 33 are within the belt. This orbit design is used so Juno can collect as much science data as possible early-on with instruments undamaged by radiation.

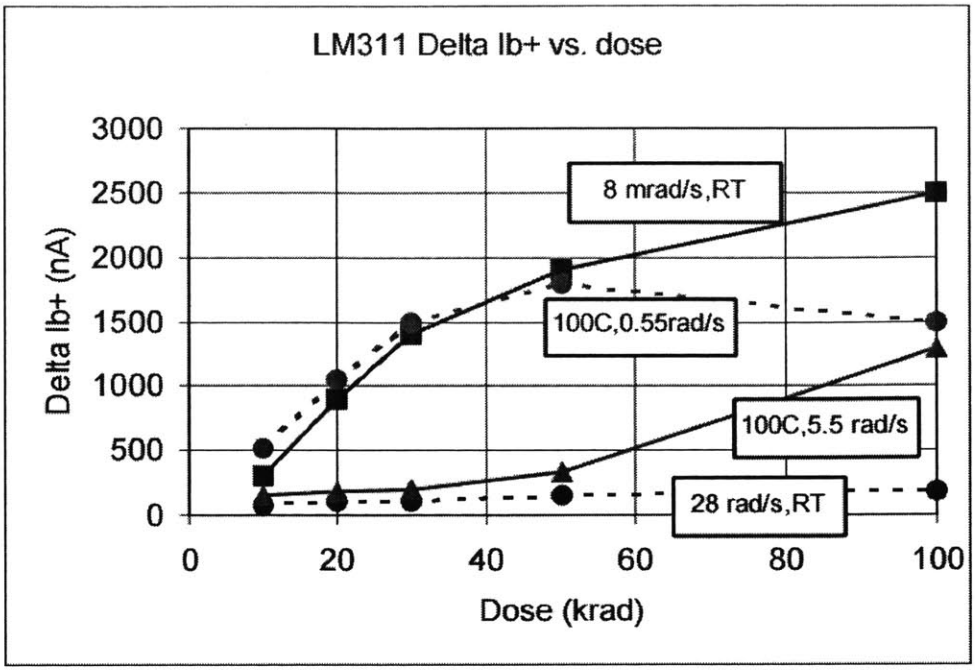

Figure 2-9: Degradation of the Input Bias Current vs TID Imparted to the LM311 Voltage Comparator for Various Dose Rates and Temperatures [26]

Another way to prevent radiation-cause damage from compromising the space mission is parts derating which is applying technical specifications less rigorous than the original manufacturer's specification. Designing avionics system with derated components gives the system extra margin that accounts for radiation-caused degradation but has consequences on the space system the avionics operate in as a whole. For example, avionics system could use the LM311 comparator in Figure 2-9 and be designed to handle the two order or magnitude increase in input bias current due to TID effects on the LM311. Such a design modification has a ripple-effect on the rest of the avionics system. For example, allowing higher leakage currents requires power supplies that can supply more current. More robust power supplies need bigger PCB traces. Bigger PCB traces mean the avionics circuit boards require more mass/volume, larger enclosures, and so on.

An avionics system can be designed to meet data-quality requirements even with SET caused noise through derating. For example, a sensor that outputs very low noise can be used so that there is sufficient margin between the sensor performance requirement and actual sensor performance. Any performance degradation due to SET-caused noise is accommodated by this margin.

This ripple effect on system requirements is also seen with another example of derating. Consider discrete MOSFET transistors designed to handle more than a few volts of milliamps. These devices are used to regulate power within electrical power supplies. Using a 60-volt rated MOSFET instead of a 6-volt rated one for a 3.3 volt power supply significantly reduces the chance of SEGR failures. This derating will also have a similar system ripple effect since these transistors are many times larger, require more PCB space, require a bigger enclosures, and so on. Thus, the decision to derate components must be taken early on in the design process to lay out appropriate derived requirements for the other subsystems affected by derated components.

For the avionics of noncritical spacecraft subsystems, it is essential to determine the acceptability of an occasional SEE-caused interruption of functionality. If such a lapse in functionality can be tolerated, then radiation tolerance requirements can be less stringent. An example of such a subsystem is the REXIS instrument with respect to the OSIRIS-REx system, but this approach can be generalized to any other non-critical system as well. The worst case scenario is that an SEU or SEFI causes the system microprocessor to crash and freeze. Other hardware like a watchdog timer or an externally commanded power-cycle will clear this issue. Since every single packet of the non-critical system's telemetry is not continuously needed, it is acceptable to have an interruption of functionality. A more benign example of this is an SEE caused corruption of downlinked telemetry. Checksums embedded in telemetry will not match the checksums calculated from the telemetry on the ground and the data will be invalid. In many cases, it is not harmful to miss one packet of telemetry out of many for slowly changing signals like voltages, temperatures, etc.

Before deciding which of the following DFR techniques to implement, a multi-disciplinary trade study needs to be conducted on the system design. Questions about whether radiation-benign orbits are feasible, a conservative derated avionics design is possible, and whether an avionics subsystem must function continuously must be asked early on. Based on the derived requirements from these discussions, the following costly avionics DFR techniques could be partially avoided.

2.3.2 Radiation Hardened Parts

Radiation hardened (rad-hard) electronics that are specially designed to operate in the space-radiation environment by withstanding SEEs and cumulative radiation damage. These characteristics are achieved usually at the expense of other microcircuit metrics like power consumption, accuracy, size, and processing speed. Rad-hard microchips are also very costly since they have high prices, long lead times, and have significantly reduced capability compared to the latest Commercial Off The Shelf (COTS) parts. For functionality that is absolutely essential to mission success, rad-hard parts may be appropriate since they are inherently less vulnerable to space radiation and are comprehensively tested to verify this robustness.

Rad-hard components are highly modified or clean-sheet redesigns of their COTS counterparts. The modifications are to the internal semiconductors and external composition that allow these rad-hard parts to withstand space radiation and the high vacuum of the space environment. The physical makeup of the part consists of high quality materials that are suited for the space environment like a non-outgassing ceramic instead of plastic for a microchip enclosure. Furthermore, the pins of these rad-hard space-grade microchips are coated with leaded solder which prevents the growth of short-circuit causing tin-whiskers. Finally, rad-hard components have redesigned circuitry that does not degrade from the excess energy and charge deposited by space radiation.

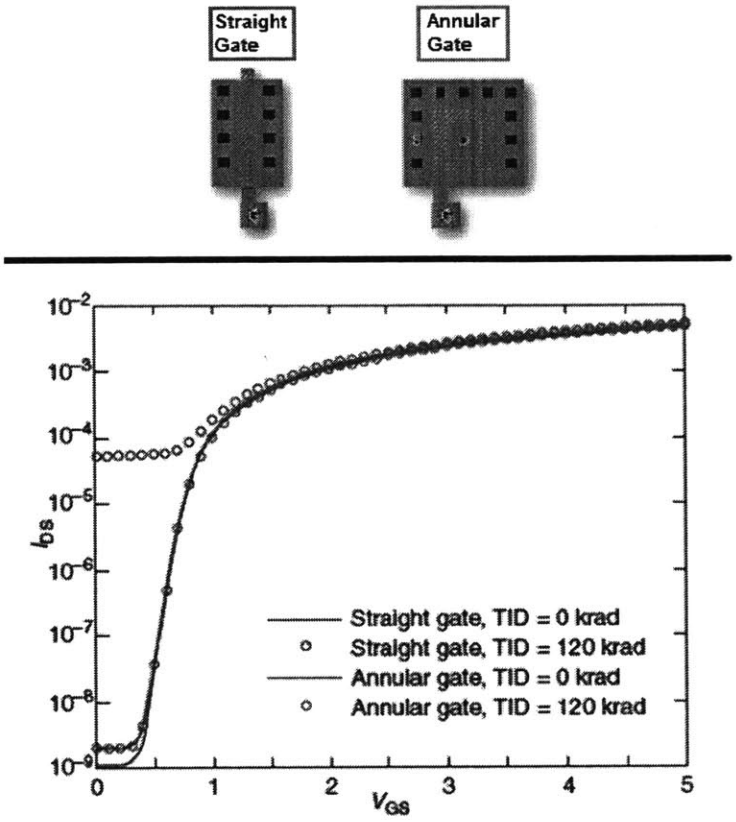

Figure 2-10: Transistor Current vs. Control Voltage for a Radiation-tolerant Device [17]

An instance of redesigning electronic hardware to withstand radiation is depicted in the bottom half of Figure 2-10, which shows transistor current as a function of gate voltage. Normally, a low gate voltage below a transistor's turn-on threshold causes the transistor to conduct a negligibly small current from its drain to source terminals. A high gate voltage above the turn-on threshold does the opposite. The transistors in Figure 2-10 have a turn-on threshold of approximately 0.5 volts where increasing the voltage beyond this point results in significant transistor current. This turn-on behavior is shown by the undamaged typical straight-gate transistor shown with the blue line in Figure 2-10. After a 120 krad(Si) dose, the typical transistor has a high leakage current shown by the dotted blue line at low gate voltages. This high leakage current is highly undesirable because it makes the transistor less effective at regulating current and further increases power consumption. The rad-hard transistor, shown with red lines and dots, has no such degradation after the 120 krad(Si) dose. Resilience to TID is created by the annular design of the rad-hard transistor's gate. The annular gate layout at the top of Figure 2-10 is more radiation tolerant

than a traditional straight gate since there are fewer sharp points for a dangerously high electric field to exist. This reduction of electric field strength makes MOSFET transistors less susceptible to current leakage and radiation damage [17].

Rad-hard parts are also typically designed to accommodate transient SEE radiation hazards as well. There are specific microchip design techniques that make circuits less susceptible to short-term radiation hazards. These techniques range from implementing redundancy on a circuit level within the microchip to modifying circuits so that SEUs and latch-ups do not propagate. These SEE-tolerant rad-hard components also incur similar costs in terms of budget, processing speed, power consumption, and mass/volume. For example, the low clock speeds of rad-hard components, compared to their COTS counterparts, provides SET tolerance. In most cases, rad-hard parts are both SEE-tolerant and TID/TNID tolerant.

In addition to providing avionics designers with a ready-made, highly tested, and low-risk option for mitigating the space radiation hazard, rad-hard parts have other benefits too. Each production lot of rad hard parts has extensive testing data that allows designers to more easily trace faults and find failure causes. Rad-hard parts also have lots of heritage from other spaceflight missions that allow avionics designers to be confident in using them. For example, the RAD750 microprocessor has been used successfully on 28 spaceflight missions[8] ranging from the Deep Impact probe to the Mars Curiosity Rover.

There are many drawbacks to using rad-hard parts that an avionics designer must consider. In general, rad-hard parts are expensive since manufacturers must invest extra design, testing, and manufacturing resources to bring rad-hard parts to the market. Specific examples of these disadvantages for the radiation-tolerant annular gate transistor in Figure 2-10 are listed below and these disadvantages are easily generalized to all rad-hard parts.

[8] BAE Systems RAD750 microprocessor datasheet accessed 6/2/2016

1. A separate manufacturing process needs to be set up to accommodate the annual transistor in a microchip design. This process cannot take advantage of mass-manufacturing techniques for COTS electronics due to the comparatively low demand for rad-hard electronics.
2. The transistor itself takes up more space within the microchip. This decreases the total amount of transistors that can fit within a microchip and thus reduces capability and increases the cost.
3. This annular design is more difficult to model with microchip design tools and methods.

The testing of rad-hard components is another reason why these components are so expensive. Prototypes and samples from production runs of rad-hard electronics are tested in radiation chambers and particle accelerators to verify that they can function while being bombarded by high and low energy radiation for extended durations. This testing allows the manufacturer to publish the part's resilience to TID and SEUs. In addition to the additional design work for rad-hard parts, this rigorous radiation testing increases the cost of rad-hard parts beyond the costs of COTS electronics.

The low production volumes of rad-hard parts create other issues for avionics engineers. These issues are long lead times of many weeks and large minimum order quantities that make it difficult for low-cost space missions to easily acquire, prototype, and test with the rad-hard parts that are needed.

2.3.3 Shielding

The harmful effects of TID and TNID can be reduced through shielding. Shielding material surrounds sensitive electronics and absorbs the energy from space radiation that would otherwise damage unshielded sensitive electronics. Shielding can be applied around individual electronic components or around entire electronics assemblies like PCB stacks. The former is known as spot shielding while the latter is assembly-wise shielding. Assembly-wise shielding is effective since there are other requirements to have enclosures around subassemblies. For example, mechanical requirements could impose a rigid enclosure of a certain thickness to meet stiffness targets for vibration testing. This thickness also provides radiation shielding and it could be more cost effective to add more shielding if necessary instead of designing a new spot-shielding system. Particularly radiation vulnerable parts can have spot shielding

added as necessary. This approach was used for developing the Galileo spacecraft for the Jovian environment [27].

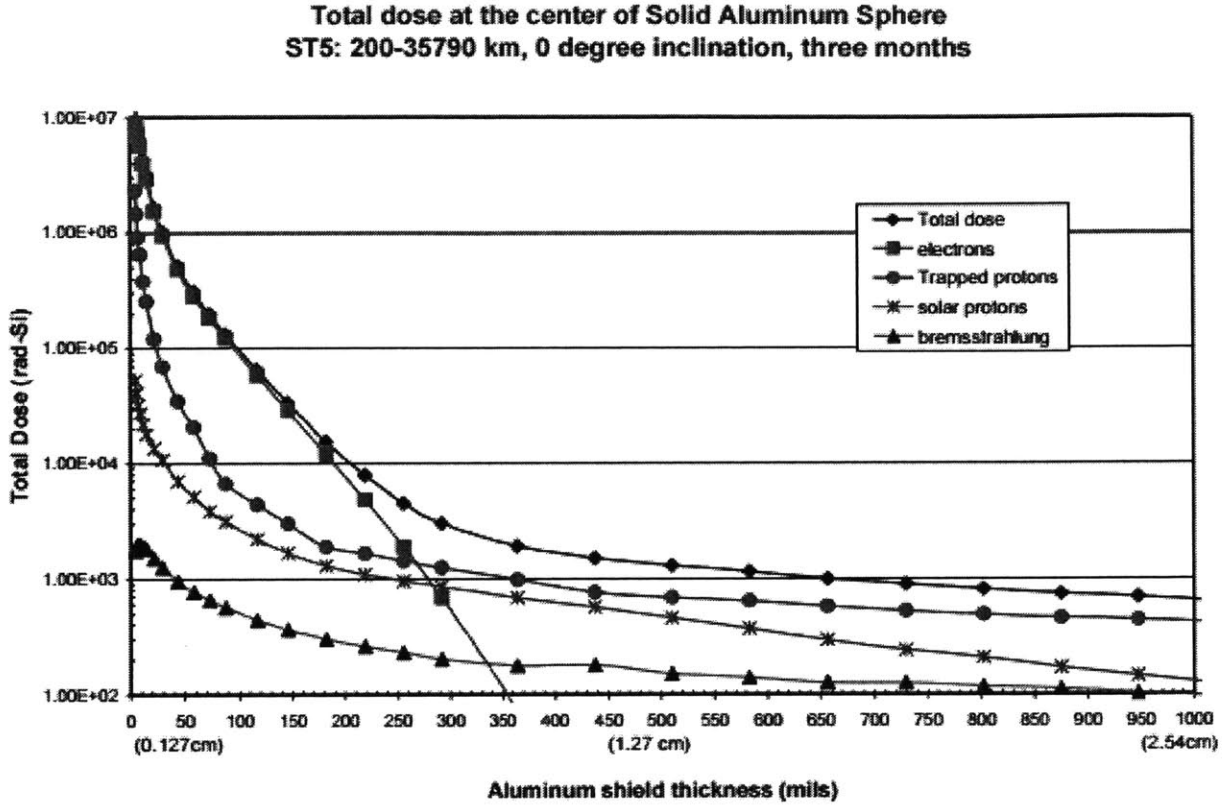

Figure 2-11: Radiation Dose vs. Aluminum Shielding Thickness [26]

For a given shielding composition, the shielding effectiveness depends on the thickness. Figure 2-11 shows the effectiveness of reducing TID levels versus increasing aluminum shielding thickness aboard the ST5 spacecraft in a highly elliptical Earth orbit for 3 months. As shielding thickness surrounding a component increases, the radiation TID decreases by a nonlinear amount. More specifically, 0.5 inches of aluminum between the electronics and outer space reduces the TID by four orders of magnitude by another 0.5 inches of shielding does little to reduce the TID. In short, adding more shielding beyond a certain thickness leads to diminishing returns in the effectiveness of shielding. The proper thickness of radiation shielding enclosure is determined by looking at other design factors like structural and thermal requirements in addition to TID [22]. For example, it would be unwise to design an avionics enclosure

with the minimum thickness for sufficient radiation shielding if this design cannot pass launch vibration tests or effectively conduct heat away from the electronics.

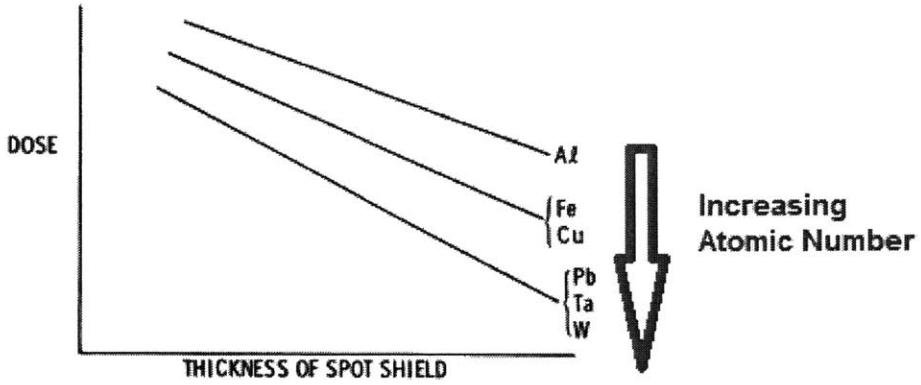

Figure 2-12: Shielding Effectiveness of Various Elements [27]

The effectiveness of shielding also depends on shielding composition. For a given thickness, compounds comprised of elements with high atomic numbers reduce TID more effectively, as seen in Figure 2-12. This effectiveness is seen in the titanium avionics enclosure on the Juno spacecraft and the tantalum spot shielding aboard the Galileo spacecraft where both shielding element choices provided maximum protection using minimum mass [22] [27]. Shielding that is too thick can cause an increase of secondary radiation through the interaction of energetic GCRs and shielding atoms. An increase of secondary radiation increases SEU and SEE rates in electronics [17]. Designers can mitigate this secondary radiation hazard with additional shielding layer with lower atomic numbers like aluminum that is better suited to absorbing low-energy secondary radiation [17].

2.3.4 Latch-up protection circuitry

Avionics design that prevents malfunction from single event latch-up (SEL) events can be grouped into two categories. First, SEL-caused damage can be prevented by using specific rad-hard components that do not latch-up [23] [17]. Rad-hard components typically have their electronic micro-architecture designed so that the probability of a SEL occurring are many orders of magnitude lower than COTS parts. This increase in reliability is accomplished by redesigning the CMOS circuitry from the ground-up so the

parasitic PNPN thyristor structures are less susceptible to becoming energized through space radiation and causing dangerously high current conditions [17]. The alternate to using SEL-hardened components is preventing long periods of destructively high levels of electrical current from occurring in the first place [17].

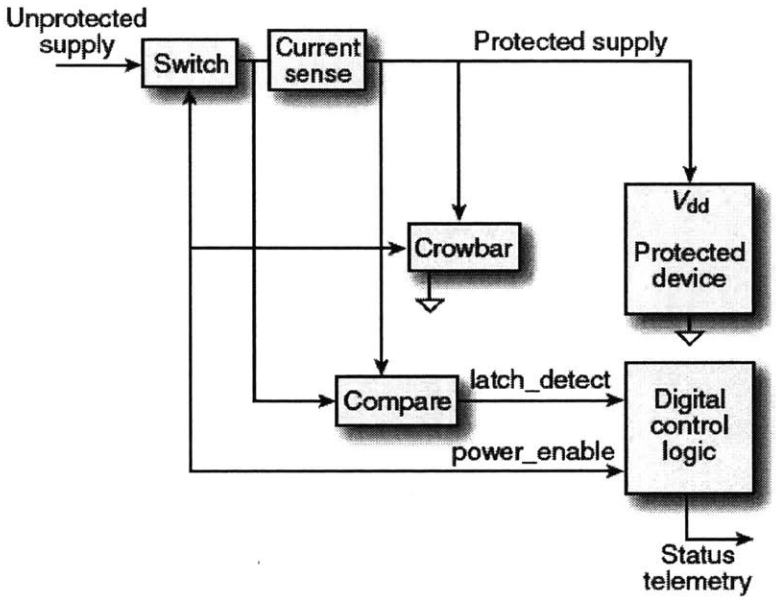

Figure 2-13: Active SEL-protection Circuitry [17]

Alternatively, the SEL hazard can be mitigated with special circuit design by implementing current limiting functionality. The simplest method of limiting current is placing a current limiting resistor in series with the power-supply input of a microchip. This resistor limits the current flowing through the microchip to a safe level but this technique is only suitable for low-current devices. Typically, high current devices have an unacceptable voltage drop or power loss across a current limiting resistor. For these high-current devices, sophisticated circuitry shown in Figure 2-13 is needed. This circuitry actively monitors the SEL-sensitive components, detects SEL, shuts off power before permanent damage occurs, and bleeds off excess charge to ground as needed [17].

Depending on the functionality that certain SEL-vulnerable circuitry implements, SEL can be avoided through clever operation of the circuitry. For example, an ADC that acquires data once per second can be turned on briefly every second to acquire the measurements. Typically, a modern ADC is

capable of acquiring several thousand samples per second so the on-time required to sample a few sensors is a few milliseconds. Leaving the ADC on for a few milliseconds reduces the SEL duration to a few milliseconds as well since turning off a device makes it immune to SEL. When coupled with current limiting resistors, this SEL duration is very benign for most ADCs [17].

2.3.5 Error correction codes

Error Detection and Correction (EDAC) algorithms are used to detect and correct errors in critical data stored in computer memory. EDAC consists of:

1. Extra verification data that is generated from a segment of critical data. Verification data is stored next to the critical data
2. A mechanism to check and correct the critical data based on the verification data.

Error Detection and Correction (EDAC) algorithms can be used to ensure the integrity of data that is stored. This capability is very useful for computer memories in space that are susceptible to corruption caused by SEUs, SETs, and SEFIs. EDAC algorithms are used to scan computer data to detect and correct errors. If an EDAC algorithm detects critical data that does not match with the corresponding verification code using the verification code generation procedure, the data is marked as corrupt. Some EDAC algorithms are sophisticated enough to correct a portion of the corrupted critical data.

SEUs can corrupt downlinked scientific data or place the avionics system in an undesired state by corrupting a microprocessor's control registers. A SEU can cause one bit of memory to flip. EDAC algorithms can fix this corruption by calculating and rewriting the correct value to the memory bit [17]. Some DRAM memories have built in EDAC as part of their refresh schemes that periodically keep the capacitors in DRAM memory cells topped up with voltage; empirically these memories can handle SEUs as well since DRAM memory capacitor voltage leakage also similarly corrupts data [24].

If EDAC algorithms are not implemented or fail to correct an error, a SEU can cause malfunctions by directly changing the state of digital electronics [17]. More specifically, SEUs and SETs can corrupt values in computer memory or registers, resulting in the processor executing incorrect software, incorrect

results of computations, or corrupted telemetry [17]. Depending on the EDAC implemented within the spacecraft, these failures can cascade and cause more serious system failures [24].

The extra resources needed to implement EDAC are the key drawback of this technique. More computing power is required to generate the data verification codes. Storing these codes with the critical data requires more computer memory as well. Furthermore, carrying out these EDAC computations and correcting errors when necessary requires time and thus slows the avionics system [17].

2.3.6 Redundancy

Components or functionalities can be implemented multiple times within a system to prevent a certain functionality from getting corrupted from the transient radiation-caused malfunctions. This technique is known as redundancy. Redundancy is applied to functions in terms of duplicate hardware components or executing the functionality repeatedly over time. Instead of using one computer or memory unit, three can be used concurrently and their outputs can be compared with voting circuitry to determine the correct outcome of a computation or memory read/write. It is highly unlikely that more than one copy of the hardware will be affected by radiation. SEEs occur randomly and thus, they typically only affect one hardware component at a time. Normally, the correct output is always computed and incorrect outputs are discarded by the voting circuitry. Similarly, a computation or memory read can be carried out three times in series to produce three results. These results can be compared and if they do not equal each other, there was a radiation caused error and the erroneous result is not allowed to propagate through the system.

Using redundancy to recover from radiation-caused errors imposes costs on the avionics system. These costs can be increased processing time, more hardware components, and overall, more system complexity. For example, implementing three redundant Microblaze processors and extra voting circuitry within an FPGA microchip utilizes many times more digital logic resources than a single MicroBlaze processor. However, if this processor is computing critical data for critical operations such as Entry, Descent, and Landing (EDL), TAGSAM, or orbital insertion, this extra utilization is acceptable [17].

2.4 Summary of Radiation Effects and Mitigation Techniques

This chapter has presented the space radiation environment, how this environment interrupts the operation of avionics, and avionics design features that prevent these interruptions from occurring. Avionics design features to guard against specific radiation-caused interruptions are summarized in Table 2.1. Usually, all of these techniques do not need to be used on a particular avionics system since each technique incurs its own costs on the system design, project time/budget, and testing phases. Designers must evaluate what the spacecraft needs to accomplish as a whole, design a spacecraft trajectory to minimize radiation exposure while accomplishing mission objectives, and then choose the most effective techniques in Table 2.1 to resolve radiation tolerance issues in their system.

Table 2.1: Radiation Hazard and Mitigation Technique Summary

			Radiation Hazards					
			SEU	**SET**	**SEL**	**SEGR**	**TID**	**TNID**
			2.2.1	2.2.2	2.2.3	2.2.4	2.2.5	2.2.6
Design for Radiation Techniques	**System-wide Design**	2.3.1	X	X	X	X	X	X
	Rad-hard Parts	2.3.2	X	X	X	X	X	X
	Shielding	2.3.3					X	X
	Latch-up Protection	2.3.4			X			
	Error Correcting Codes	2.3.5	X	X				
	Redundancy	2.3.6	X	X	X	X		

LEGEND
Long Term
Long and Short Term
Short Term
Section Number

"X" indicates mitigation of a particular radiation hazard

Chapter 3 - REXIS Avionics

Overview

The REXIS instrument has an avionics system that generates scientific telemetry that describes the elemental composition of Bennu's regolith. The OSIRIS-REx spacecraft downlinks this telemetry to scientists on Earth for further processing to determine the elemental composition of Bennu's regolith. This chapter documents the REXIS avionics system starting with an introduction of terminology and concepts that are required to understand the details, design decisions, components and operation of the REXIS avionics system. Next, the avionics system is presented with a high level functional overview that connects the functions implemented by the avionics system to the overall REXIS objective of generating scientific telemetry that can be used to characterize the asteroid Bennu. Following this, all the avionics subsystems and components that implement the previously stated functionality are described with increasing detail.

3.1 Introduction to REXIS Avionics

This subsection describes the REXIS avionics system with sufficient detail necessary to understand the next subsections that delve deeper into the following avionics components.

1. **Hardware**: physical electronic components distributed and wired across several printed circuit boards (PCBs). One particularly important hardware component is the Field Programmable Gate Array (FPGA), a large microchip containing reconfigurable digital computation resources.
2. **FPGA Firmware**: the configuration of the digital logic resources within a FPGA. Alternatively, FPGA firmware consists of various digital logic cores that provide certain functionality and the data connections between these digital logic cores. One of the most essential digital logic cores is

the MicroBlaze – a 32-bit microprocessor created purely with digital logic/computation resources within an FPGA.

3. **Flight Software (FSW)**: a series of instructions for the Microblaze processor to execute that are grouped into interconnected software functions. FSW also implements functionality required of the REXIS system.

The FSW and FPGA firmware are discussed first since they directly implement the functional requirements of the REXIS avionics system. The hardware is discussed afterward because it supports the FPGA firmware and FSW.

The REXIS avionics hardware, FPGA firmware, and FSW are designed to operate the x-ray detectors of REXIS (the CCDs and SDD), read the detector responses, and transfer this scientific data to the OSIRIS-REx Command and Telemetry Handling (C&DH) system. The OSIRIS-REx C&DH system is an electronic system that downlinks REXIS data to scientists on Earth to enable them to create the elemental abundance maps of Bennu - the primary science product of REXIS. This science process is further described in section 1.3.1. This predominant objective of generating scientific data creates several derived requirements. Some examples of these requirements are summarized below:

1. **Command Processing** – REXIS avionics interpret digital data transmitted to it as commands to activate certain functionality. These commands are used to initiate data acquisition and configure REXIS.
2. **Engineering Telemetry** – REXIS avionics must send engineering telemetry that indicates overall instrument health and status. Some of these data are periodically transmitted and other data packets are sent as response to a command. Engineering telemetry is essential to understanding the overall instrument health, troubleshooting issues, and relaying the current status of science data acquisition hardware.

3. **Power Regulation** – REXIS avionics must convert unregulated power supplied from the OSIRIS-REx spacecraft into regulated power suitable for REXIS avionics components and x-ray sensors.
4. **Radiation Cover Actuation** – The CCD sensors are surrounded by aluminum shielding in order to limit damage caused by radiation. Part of this aluminum shielding is removable through the radiation cover mechanism. The REXIS avionics system opens the radiation cover upon command. Although this actuation exposes the CCDs to radiation, it also allows x-rays from Bennu to be sensed by the CCDs.

The REXIS avionics system has many more requirements that are derived from the top-level requirement of downlinking x-ray spectrometry data. Together, these requirements describe the functionality that the REXIS avionics system must to provide to OSIRIS-REx spacecraft/mission and REXIS instrument system. This functionality is described further in the next section.

3.1.1 Avionics Functional Overview

The REXIS avionics system functionality is shown in Figure 3-1 as a collection of subsystem functions that exchange data. Collectively, these subsystem functions are implemented across combinations of hardware, FPGA firmware, software/memory, and detectors/actuators to meet the top level requirement to downlink scientific x-ray telemetry. Figure 3-1 has boxes for each function with the colored box corners indicating which avionics components are used to implement the function. White corners indicate that either sensors or actuators are used to provide the functionality. Blue corners indicate the presence of hardware. Red indicates FPGAs while yellow indicates FSW. Figure 3-1 also shows the OSIRIS-REx spacecraft that has a Command and Data Handling (C&DH) system and solar panels. The C&DH system relays commands from Earth to REXIS and telemetry from REXIS to Earth while the solar panels supply the REXIS avionics system with electrical power.

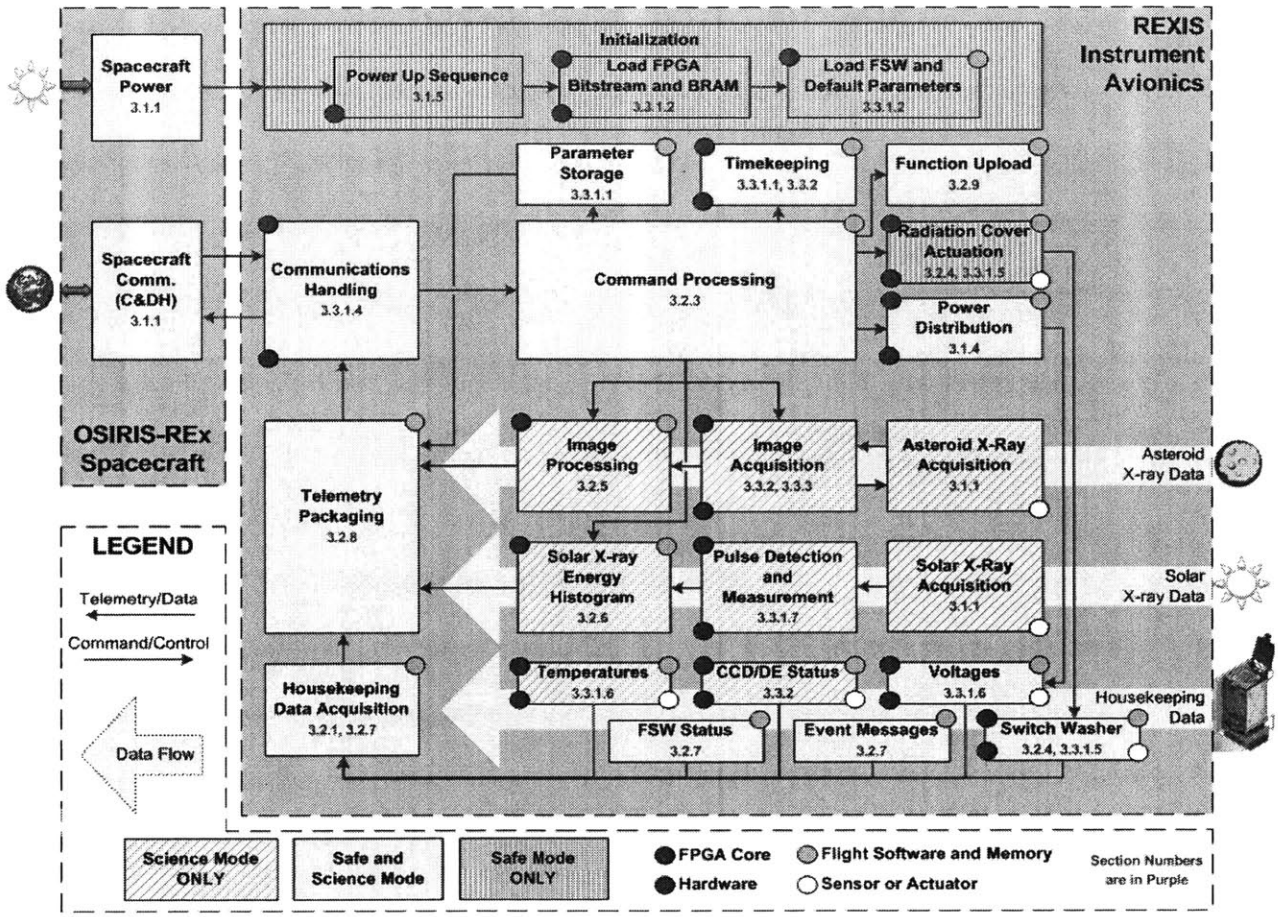

Figure 3-1: Functional Block Diagram of REXIS Avionics System

REXIS scientific and engineering telemetry requirements are implemented with three main data-flows that are downlinked to Earth through the OSIRIS-REx spacecraft. These three data flows are the light-green right-to-left arrows shown in the background of Figure 3-1 that are labeled "Asteroid X-ray Data", "Solar X-ray Data", and "Housekeeping Data". The Asteroid x-ray data-flow is the primary science telemetry product while the solar x-ray data-flow helps scientists on Earth to properly interpret the asteroid x-ray data and derive the elemental compositions of the asteroid regolith. REXIS scientific data processing is described in more detail in Section 1.3.1. The third data flow is the housekeeping and engineering data flow that is used primarily for tracking the instrument's health and status. Both in physical and functional terms, the rest of the avionics system supports these three data flows. For example, without the command processing function, it would be impossible to enable and configure the downlink of the crucial REXIS science telemetry.

In addition to generating telemetry, REXIS must process commands or digital data transmitted from Earth to OSIRIS-Rex. These commands activate instrument functionality that ultimately control the telemetry data flows. OSIRIS-REx relays the REXIS specific commands to the REXIS instrument that interprets command data and takes the appropriate action. For example, the Radiation Cover Actuation and Timing function in Figure 3-1 is controlled through frangibolt-specific commands. If the frangibolt system is armed, the frangibolt fire command will cause REXIS to send electrical current through the frangibolt actuator that causes it to heat up and expand. The radiation cover opens when the frangibolt actuator's expansion fractures the bolt that holds the radiation cover closed.

The avionics system operates in two modes – safe mode and science mode. Safe mode is the default operating state of REXIS and has minimal functionality and power draw. Scientific data acquisition occurs in science mode. The avionics functionality in Figure 3-1 is available in safe mode (dark blue), science mode (striped blue), or both modes (plain blue). When REXIS is powered on, the avionics are in the safe mode state where electrical power consumption is low since all the scientific data hardware is off. REXIS operators send a command to transition REXIS into science mode. In science mode, the CCDs and SXM are active, REXIS processes data from these components and downlinks scientific asteroid and solar x-ray telemetry.

The rest of the REXIS avionics system implements miscellaneous functionality like initialization, power distribution and data storage. These capabilities provide the necessary electrical/software infrastructure required for command processing and telemetry generation. For example, the initialization system puts REXIS in a state where all the avionics are powered up, operating in safe mode, and the FPGA/FSW are configured to implement the remaining functions in the functional block diagram (Figure 3-1). Similarly, the power distribution functionality regulates electrical power from OSIRIS-REx into various voltage rails that are used for powering the electrical hardware aboard REXIS. A third example is the computer memory available to the FSW that allow it to store a variety of data ranging from x-ray images, telemetry, or FSW instructions. These hardware components are further detailed in the next section.

3.1.2 Avionics Hardware Overview

When REXIS is performing science data collection, x-rays are sensed by the four CCID-41 CCDs (Figure 3-2) and a SXM sensor which convert x-ray photons into electrical voltages. For the CCDs, these voltages are sensed by the Detector Electronics (DE). The DE consists of two Printed Circuit Boards (PCBs) that generate CCD drive voltages, sense CCD output voltages, and interface with the CCDs through flexible circuit boards called flexprints. The DE converts the analog CCD voltages into digital numbers that are transmitted to the Main Electronics Board (MEB) over CameraLink image data transfer protocol. Similarly, the SXM transmits its x-ray voltage pulses to the MEB over a coaxial cable harness. The MEB performs scientific data processing on both these signals, packages the results into telemetry packets, and sends this telemetry to Earth through the OSIRIS-REx communication system.

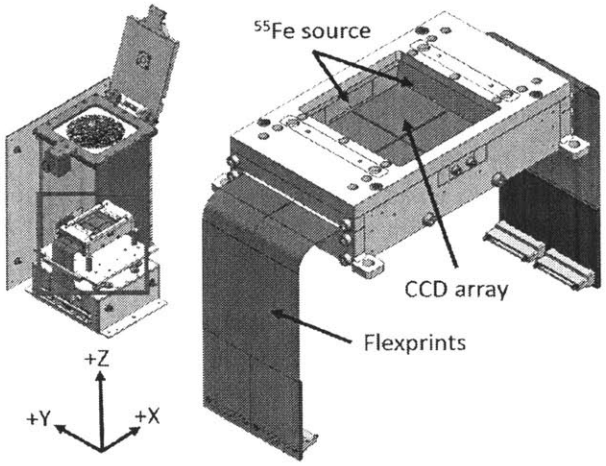

Figure 3-2: REXIS CCD Sensors in the Detector Assembly Module (DAM) [3]

Numerous REXIS functions are implemented aboard the MEB using various interconnected analog and digital microchips. The most vital microchip the MEB has is a Xilinx Virtex5 FPGA that is used to implement digital logic cores described by the REXIS FPGA firmware. The most important FPGA core is the Microblaze processor that executes the REXIS flight software (FSW). With all these components, the MEB plays a crucial role in implementing a majority of functionality in the REXIS Avionics functional diagram (Figure 3-1).

The DE is responsible for the x-ray "Image Acquisition" functionality denoted in Figure 3-1 and executes this functionality with two PCBs known as the Video Board and Interface Board. The DE is an intermediary between the analog CCDs and the digital data processing hardware on the MEB. The REXIS CCDs consist of sixteen nodes which are 256x1024 pixels controlled by drive and read-out circuitry on the Video Board. The DE video PCB's readout circuitry amplifies data from each of the sixteen CCD pixel clusters and converts this amplified signal to digital data with analog to digital converter (ADC) microchips. These sixteen streams of digital data are read in parallel by an another Actel FPGA aboard the Interface Board that sends this pixel data to the MEB FPGA using a CameraLink digital data transfer protocol.

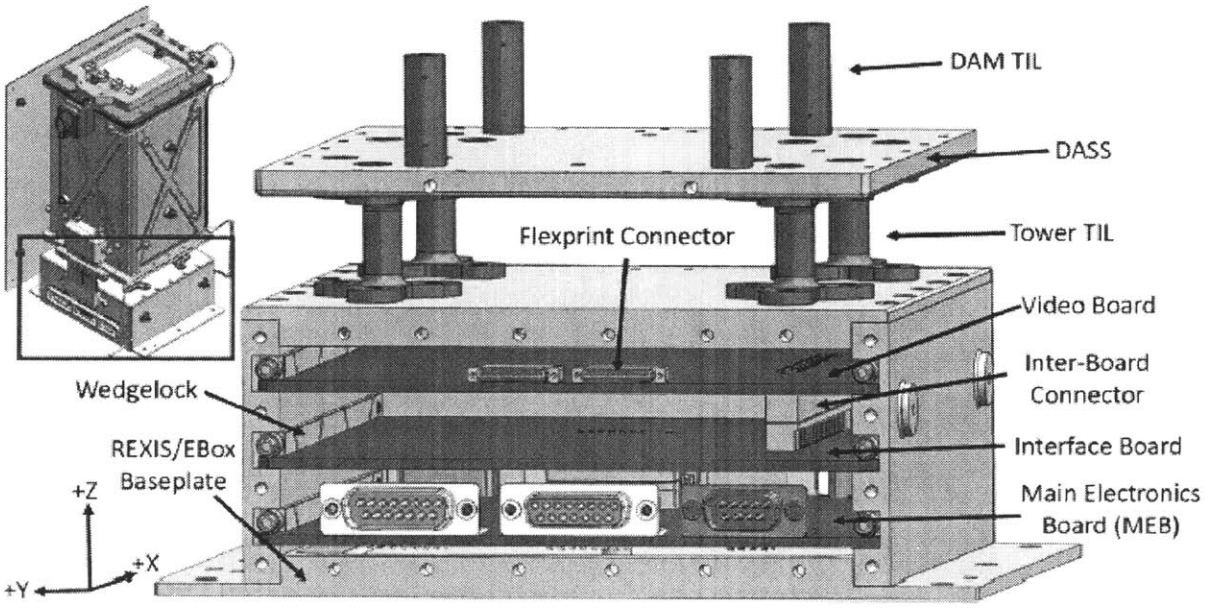

Figure 3-3: REXIS Electronics Box Assembly [3]

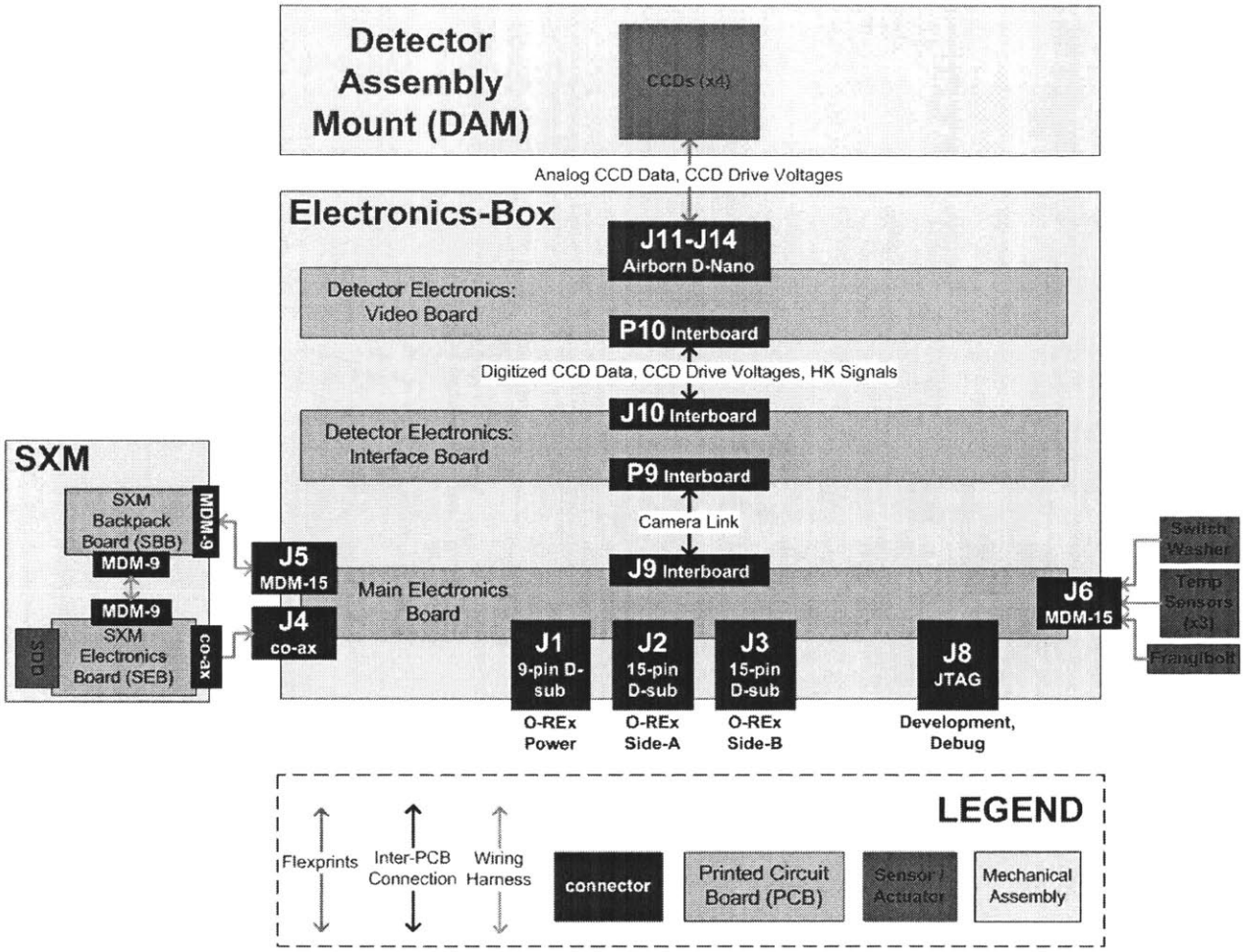

Figure 3-4: REXIS Electrical Connector Layout

The MEB and DE PCBs are located inside the electronics box as shown in Figure 3-3 and schematically in Figure 3-4. In Figure 3-3, the electronics box's front panel that contains cut-outs to for the spacecraft-to-REXIS wiring to pass through, is removed. The MEB is on the bottom of the PCB stack in these figures and contains connectors to interface with the spacecraft, frangibolt, and SXM. The DE Interface Board is immediately above the MEB and the x-ray image data travels between these boards over a pair of 30-pin inter-board connectors J9 and P9 as shown in Figure 3-4. J9 and P9 implement the CameraLink protocol is used to transfer image data between electronics. Another set of connected 100-pin inter-board connectors J10 and P10 are between the DE Interface Board and DE Video Board shown at the top of the Figure 3-3 avionics stack. J10 and P10 enable the Interface Board's circuitry to send CCD-drive voltages to the Video Board and the Interface Board's FPGA to control/read the sixteen ADCs

aboard the Video Board. The Video Board interfaces with the CCDs through four flexprint connectors signified with an orange arrow in Figure 3-4.

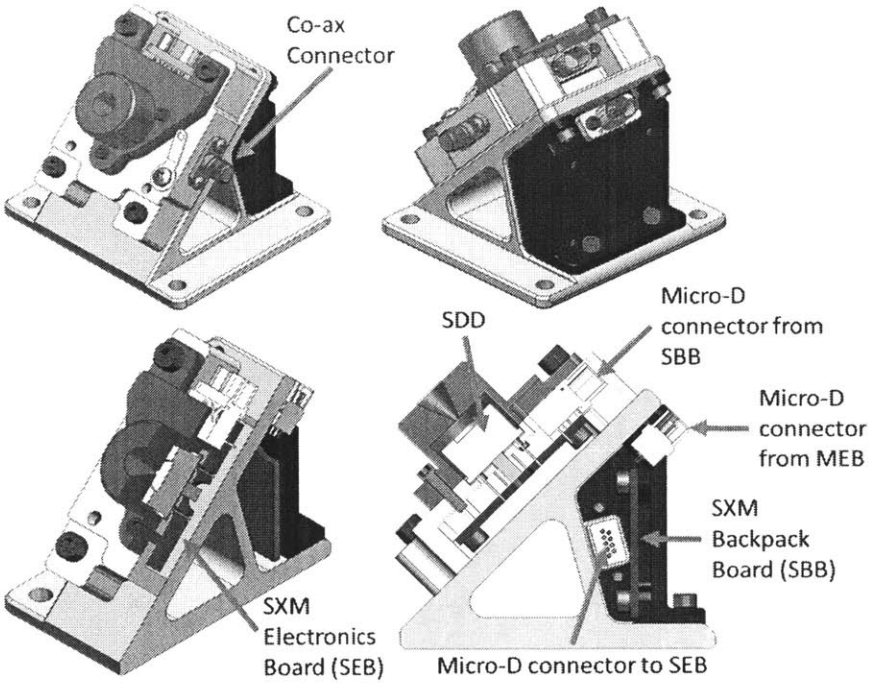

Figure 3-5: Renderings of the FM Solar X-ray Monitor

The electronics box in Figure 3-3 only holds three out of the five REXIS PCBs – the other two PCBs are within the SXM shown in physically Figure 3-5 and schematically in the left of Figure 3-4. The SXM uses an Amptek XR-100SDD Silicon Drift Detector (SDD) x-ray sensor that is supported by these PCBs. Circuitry within the SXM and MEB reads the x-ray voltage pulses from the SDD, provides the SDD with a high voltage bias, and energizes the SDD's built-in thermo-electric cooler (TEC) that keeps the SDD sensor cold enough to obtain low-noise data. The two PCBs within the SXM in Figure 3-5 are the SXM electronics board (SEB) and SXM Backpack Board (SBB). The SEB contains a preamplifier circuit which amplifies the x-ray voltage pulses from the SDD so they can be sent to the MEB through the co-ax connector/wiring harness in Figure 3-4 and Figure 3-5. Electrical power for the TEC, preamplifier, and high voltage bias come from the MEB through the SBB. The SBB has a switching DC/DC converter circuit that steps down the TEC power from the MEB to a voltage suitable for the TEC. This low voltage TEC power, and the other SXM signals are passed to the SEB with a wiring harness.

3.1.3 Avionics Software and FPGA Core Overview

Along with the previously described hardware, REXIS also uses software and digital FPGA logic cores. The REXIS FSW plays a role in implementing most of the REXIS avionics functionality depicted with yellow circles in Figure 3-1. The FSW consists of a series of instructions for the Microblaze processor on the MEB FPGA to execute. The FSW directs the Microblaze processor to interact with data structures stored on digital computer memory or the FPGA cores. Meanwhile, the FPGA cores are interconnected configurations of the MEB FPGA's digital logic/computation circuitry set up for specific tasks like RS422 data transmission, computer memory control, or FSW execution that are carried out by the Microblaze processor implemented as an FPGA core.

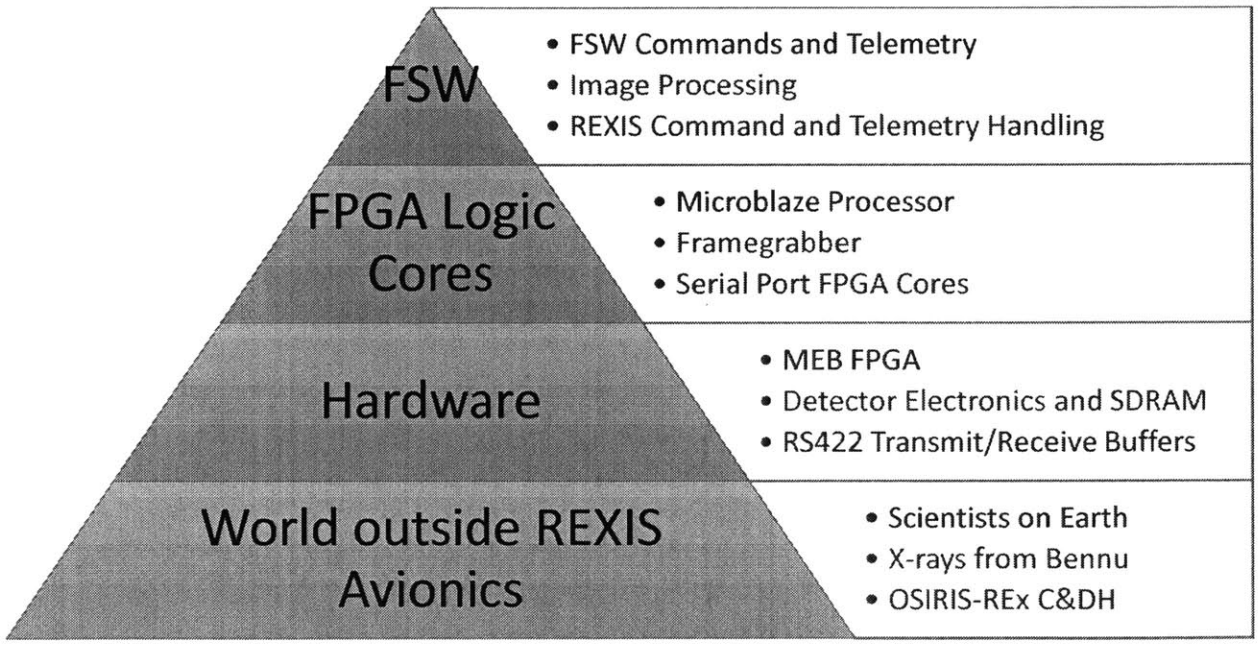

Figure 3-6: FSW Support Structure

The avionics hardware and FPGA logic cores allow the flight software operate as demonstrated in Figure 3-6. The key takeaway from Figure 3-6 is that the FSW interacts with the outside world by commanding FPGA cores that are physically connected to avionics hardware through the MEB FPGA microchip's pins. The following examples shown with red, green and blue text in Figure 3-6 illustrate the hierarchy of hardware, FPGA core, and FSW:

- Red - In order to process commands from and send telemetry to scientists on Earth, the FSW must operate on the Microblaze processor FPGA core. In turn, the Microblaze processor relies on the MEB FPGA microchip hardware to interact with the physical world.
- Green – Sensing the fluoresced x-rays from Bennu requires the FSW to interact with the framegrabber core. The framegrabber stores and processes x-ray image data from the DE inside the SDRAM memory. After the framegrabber completes this data transfer and processing, the FSW can generate scientific x-ray telemetry.
- Blue – The FSW must interact with the OSIRIS-REx spacecraft's C&DH system in order to process REXIS-specific commands and send REXIS telemetry to Earth. The serial port FPGA cores and RS422 buffer microchips make this interaction possible. The serial port FPGA cores take data to/from the FSW and generate the appropriate voltages to drive the RS422 buffer microchips which are physically connected to the OSIRIS-REx C&DH system.

The simplest component that allows the FSW and FPGA cores to interface with the physical world is the General Purpose Input/Output (GPIO) pin aboard the FPGA. A GPIO pin is a physical pin on the FPGA that is connected to external circuitry. Thus, a GPIO pin is a bridge between the internal digital logic hardware of an FPGA and external circuitry. Digital logic circuitry within the FPGA can either sense or control a voltage on the GPIO pin. Since the FPGA is a digital system, these voltages can only be zero or 3.3 volts. FPGA cores can be directly wired to GPIO pins in order to interface with external circuitry. One of these FPGA cores is the GPIO core that acts as a bridge between the FSW and the physical GPIO pin. The FSW can interface with external components by calling a function that utilizes a GPIO core to sense or command a digital voltage on a physical GPIO pin.

The FSW interfaces with REXIS's Synchronous Dynamic Random Access Memory (SDRAM) chip with GPIO pins. The SDRAM memory is used for:

1. Holding all the uncompressed intermediate data used for scientific data processing
2. Maintaining buffers for REXIS commands and telemetry

3. Storing unprocessed CCD frames from the DE for downlink

Additionally FSW has also access to another type of memory known as Block Random Access Memory (BRAM) that is built into FPGAs. While SDRAM stores large amounts of data the BRAM contains the FSW instructions the Microblaze executes and the variables, values, and data structures the FSW needs to operate upon.

3.1.4 Avionics Power Overview

The previously described FSW, FPGA cores, and hardware all require electrical power to operate. This subsection describes the REXIS electrical power system that converts unregulated electrical energy originating from the OSIRIS-REx solar panels to regulated voltage rails suitable for powering the variety of electronics with REXIS.

The electrical power that REXIS requires to operate varies depending on its state as shown in Table 3.1. The power draw in safe mode is lower than science mode because the CCDs and DE are off. During science mode, the DE acquires an x-ray image from the CCDs every four seconds, causing REXIS power draw to spike up to 12.8 Watts every four seconds. Frangibolt firing requires about 20 watts of electrical power that significantly increases the safe mode power draw.

Table 3.1: REXIS Electrical Power Draw from OSIRIS-REx

REXIS state	**Power Draw (Watts)**
Safe Mode	9
Science Mode	11.2
Science Mode during CCD Data Readout	12.8
Safe Mode during Frangibolt Firing	30

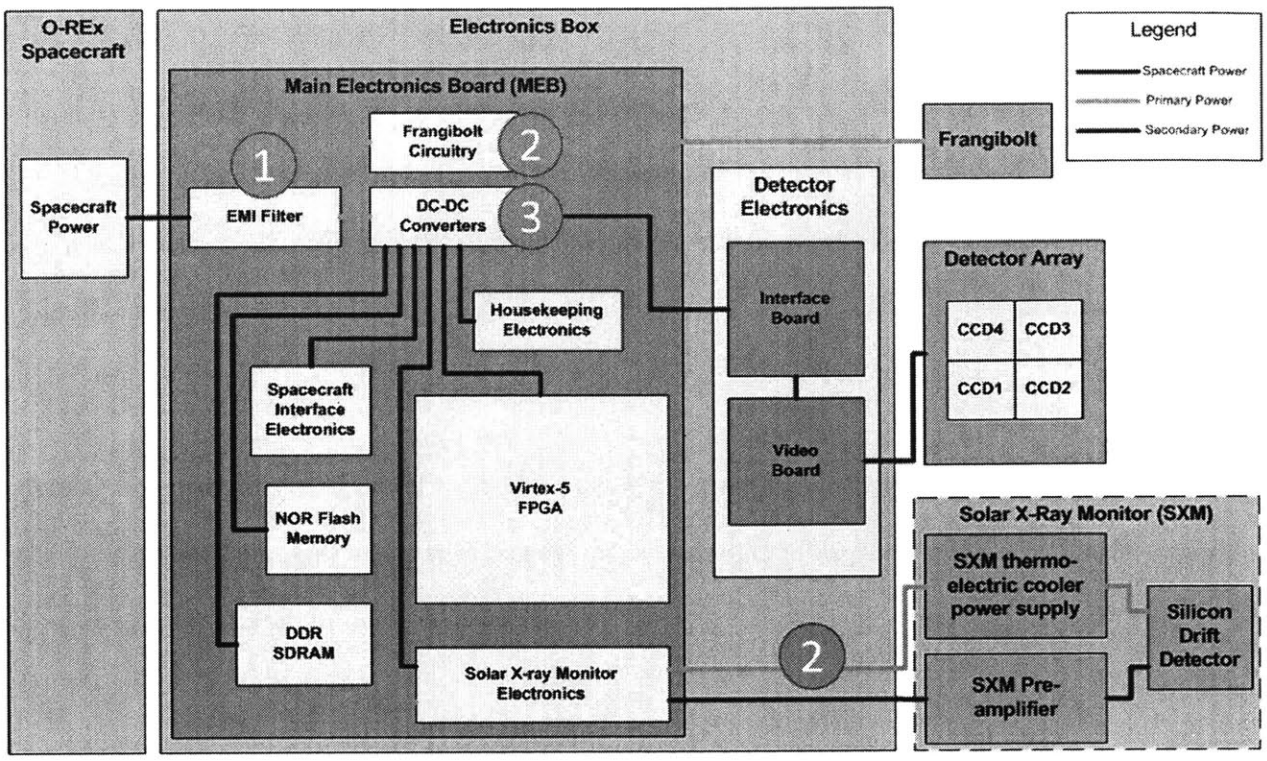

Figure 3-7: REXIS MEB Power Distribution

The MEB provides electrical power to the REXIS system by using switching DC/DC converters to convert unregulated 26-34 volt power supplied from OSIRIS-REx into suitable lower voltages for REXIS's electronic components. First, spacecraft electrical power is filtered with a SFMC28-461/00 EMI filter that ensures REXIS is electromagnetically compatible with OSIRIS-REx (shown as (1) in Figure 3-7). Some of this filtered power is used directly by high current components like the frangibolt circuitry and SXM TEC as shown with the orange lines and (2) in Figure 3-7. The remainder of REXIS electrical power is secondary power that is available on further regulated voltage rails and shown in red and (3) in Figure 3-7. The secondary power rails are electrically isolated from the spacecraft power and REXIS primary power since the secondary rail's DC/DC converters electrically isolate their input and output voltages.

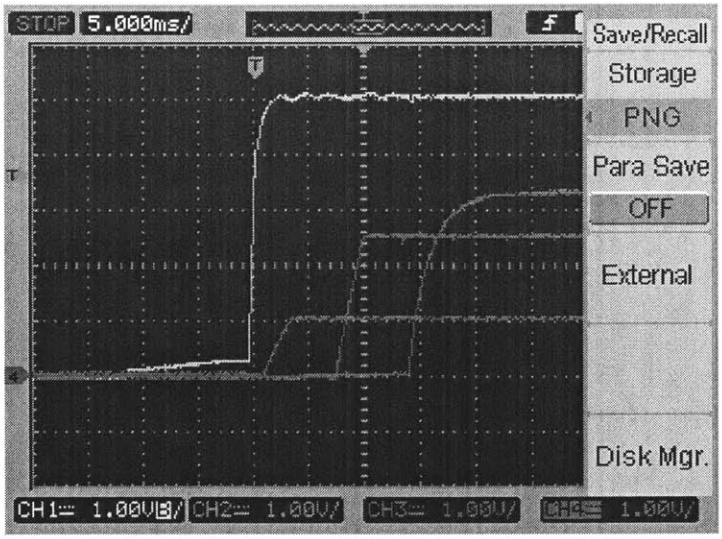

Figure 3-8: REXIS Power Rail Ramp-up during System Power-up

REXIS uses a series of rad-hard voltage converters to generate the secondary voltage levels shown with red lines in Figure 3-7. During power up, the REXIS system defaults to safe mode where the 1.0V, 2.5V, 3.3V, and 5V rails become active. These secondary voltage rails are powered on in a specific order shown in Figure 3-8 to satisfy the power supply bring-up timing requirements of the MEB FPGA. This power supply sequencing is accomplished by having each voltage regulator activate the next voltage regulator when its voltage output is stable.

When REXIS transitions to science mode, the -12V, -5V, 12V, and 24V rails are turned on. The voltage regulators responsible for providing these voltage rails have enable-pins connected to GPIO pins on the MEB FPGA. When REXIS transitions to science mode, the FSW calls functions to activate MEB FPGA's GPIO pins that turn on these science mode voltage rails.

Table 3.2 below has details about which components each voltage rail powers.

Table 3.2: Overview of the Secondary Power Voltage Rails

Voltage of Power Rail	Hardware used for power rail generation	What the Power Rail is used to power
-12.0	A Crane-Interpoint SLH2812D/KR Switching DC/DC converter generates both the ±12V rails from the primary +28V rail	• Generation of the -5V rail • Negative drive voltages for the CCDs
-5.0	A Linear Technology RH137H linear voltage regulator steps down the -12V rail to -5V	• Negative voltage supply for the SXM pre-amplifier board
1.0	An Intersil ISL70001SRHQF switching DC/DC converter steps down the 5.0V rail to 1.0V	• MEB FPGA
2.5	An Intersil ISL70001SRHQF switching DC/DC converter steps down the 5.0V rail to 2.5V	• MEB FPGA • SDRAM
3.3	An Intersil ISL75051SRHQF linear voltage regulator steps down the 5.0V rail to 3.3V	• ADCs • RS422 receiver and transmitters • Opto-couplers • Op amps • NOR flash • DACs • SXM Circuitry • PRT Temperature Sensors • MEB FPGA • Crystal Oscillator • Detector Electronics PCBs
5.0	A Crane-Interpoint SMHF2805S/KR Switching DC/DC converter generates -5V rail from the primary +28V rail	• AD590 Temperature Sensors • Generation of 1.0V, 2.5V, and 3.3V power rails • Powering the SXM circuitry through high side switches that are closed when the SXM is turned on in science mode • Detector Electronics PCBs
12.0	A Crane-Interpoint SLH2812D/KR Switching DC/DC converter generates both the ±12V rails from the primary +28V rail	• CCD drive voltages generated on the DE
24.0	A Crane-Interpoint SLH2812D/KR Switching DC/DC converter generates the +24V rail from the primary +28V rail. The 24V output is achieved by wiring the two ±12V outputs in series as recommended by the datasheet.	• CCD drive voltages generated on the DE • SXM SDD high voltage bias

3.1.5 Interface between REXIS Avionics and OSIRIS-REx

In addition to processing commands and creating scientific and engineering telemetry, the REXIS avionics system is designed to interface with the OSIRIS-REx spacecraft. The spacecraft relays commands and telemetry between REXIS and the Earth as shown in the functional diagram in Figure 3-1. The spacecraft also provides electrical power to REXIS through an unregulated electrical power line and switches this power on when REXIS functionality is needed during the OSIRIS-REx mission.

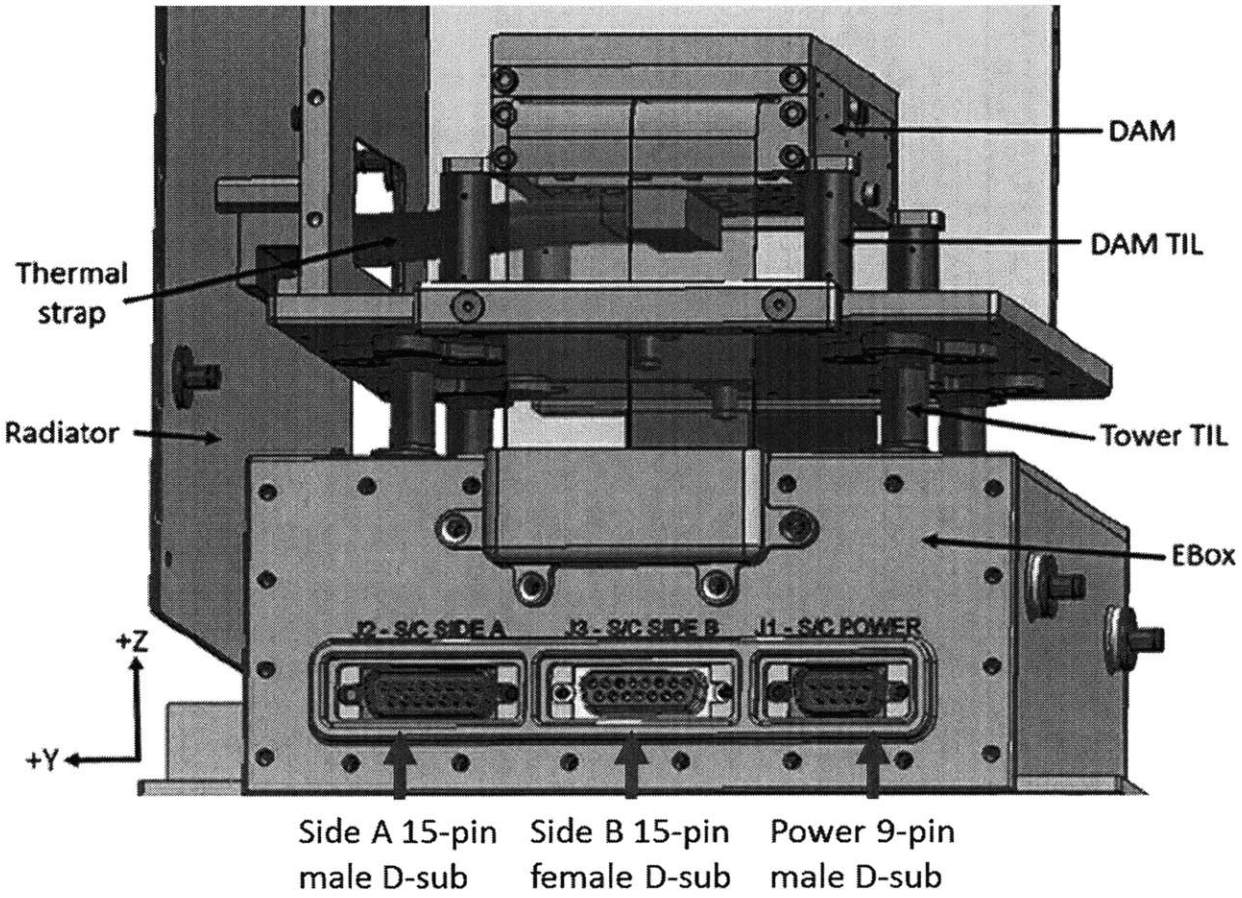

Figure 3-9: REXIS/Spacecraft Interface Connectors [3]

Figure 3-9 shows the physical interface that REXIS uses to interface with the OSIRIS-REx spacecraft. Wiring harnesses from the spacecraft's C&DH and power systems connect to the D-subminiature (D-sub) connectors marked with red arrows in Figure 3-9. The spacecraft has two redundant C&DH systems known as "Side A" and "Side B". REXIS can communicate with the spacecraft using

either side A or side B connectors. Because these connectors have the same number of pins, they are opposing genders in order to prevent incorrect connections. If the avionics system senses a high voltage level on the Side Select Voltage line (purple in Figure 3-10), then the side A connector is used. Otherwise, the side B connector is used.

The third connector in Figure 3-9 is the 9-pin D-sub connector that allows the spacecraft's electrical power system to power the REXIS instrument. The power connector has two pairs of electrical supply and return lines that allow REXIS to use either one of the spacecraft's two redundant power systems. These two power lines are wired together into one power line on the MEB. Physically, all of these connectors are soldered and bolted to the MEB.

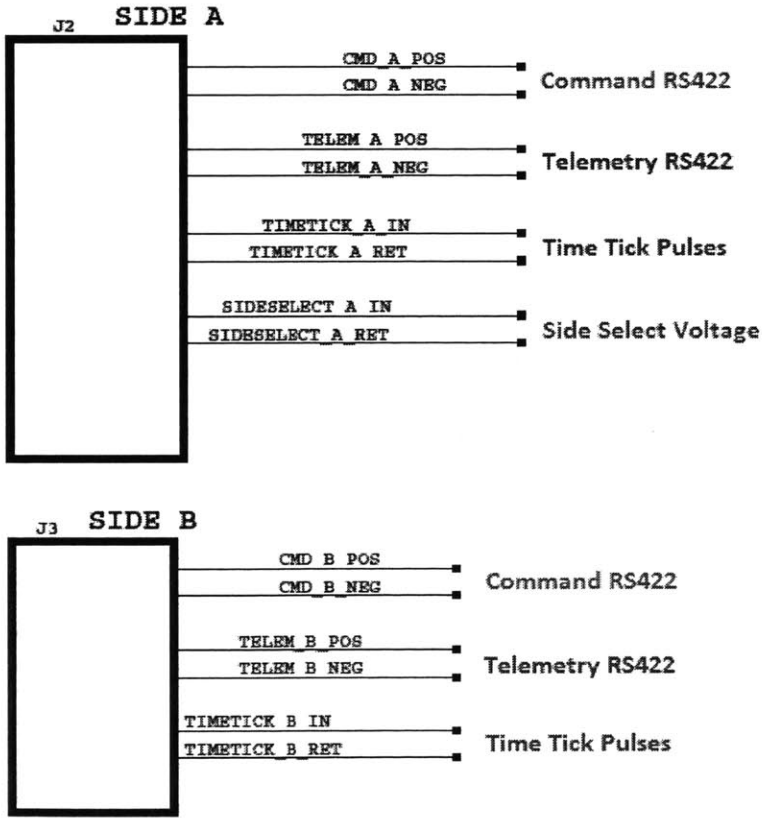

Figure 3-10: REXIS/Spacecraft Interface Connector Schematics for Commands and Telemetry

The Side A and Side B connectors provide physical connections for the RS422, Time Tick, and Side Select digital communication interfaces between REXIS and OSIRIS-REx. The electrical schematics of the Side A and Side B connectors in Figure 3-9 are shown in Figure 3-10. Depending on the voltage

REXIS senses across the purple Side-Select lines during its power-up, it chooses to communicate over a certain spacecraft side thus uses only one of the 15-pin connectors (J2 or J3) in Figure 3-10 at a time.

REXIS uses an RS422 digital serial communication interface with OSIRIS-REx. Since REXIS selects a spacecraft side to communicate with upon startup, it only uses one of the two RS422 interfaces in Figure 3-10. The RS422 digital data is transmitted to/from the FSW through buffer microchips aboard the REXIS MEB and serial port cores aboard the MEB's FPGA. All of the REXIS commands, scientific telemetry, and engineering telemetry are sent through these RS422 ports.

The third interface that the connectors in Figure 3-10 show are the time-tick voltage pulse lines in blue. The OSIRIS-REx C&DH system sends voltage pulses across the time-tick lines every second to keep all of the OSIRIS-REx payload instruments synchronized. REXIS uses this pulse for time-keeping but has its own internal clock to pace execution as well.

This overview of the REXIS Avionics and its role in processing commands, creating scientific and engineering telemetry gives a preliminary insight to the REXIS avionics design and its interface with the OSIRIS-REx spacecraft. The next two sections, 3.2 and 3.3, describe the design and operation of the avionics subsystems and components (software, FPGA cores, and hardware) used to achieve the ultimate goal of gathering relevant data to characterize the asteroid Bennu.

3.2 Description of Software and FPGA Cores

This section explains the digital logic cores instantiated within the MEB FPGA and the FSW that runs on the Microblaze processor. These two components implement the vast majority of REXIS avionics functionality shown in Figure 3-1 since FSW and FPGA cores are highly reconfigurable and can be easily debugged with tools such as step-through debuggers or ChipScope. These tools allow the developer to track the internal status of the FPGA cores and FSW during execution. This development ease and flexibility of FPGA cores and FSW made them well suited to the time-constrained nature of REXIS project development.

As detailed in section 3.1.3, The FPGA cores support the FSW by

1. Executing the FSW with the Microblaze microprocessor FPGA core
2. Enabling the FSW to interact with other physical avionics components
3. Supporting the FSW by performing time-consuming computations.

The simplest example of this support is the FSW reading the side-select voltage generated by the spacecraft in on the purple lines of Figure 3-10. The FSW interfaces with an FPGA GPIO core that has the appropriate digital logic configuration to read the side select voltage on a physical pin on the MEB FPGA. In general, the FSW uses multiple copies of the FPGA GPIO core to read and write voltages in the physical world. More complex examples of FPGA cores supporting the FSW are the framegrabber and Microblaze FPGA cores. The framegrabber allows the FSW to interface with the DE since it takes the digital x-ray image data from the DE, performs the repetitive initial processing on the image, and stores the image in SDRAM in preparation for the FSW's processing.

The FSW is a single-threaded embedded software written specifically for the Microblaze processor. Xilinx supplies the Microblaze processor as an off-the-shelf FPGA core. The FSW is written in the C programming language and uses Xilinx-supplied code libraries that allows the REXIS-specific FSW to interface with the FPGA cores. The FSW also has a series of Interrupt Service Routines (ISRs) that are short blocks of code that run periodically or in response to external events. The ISRs enable the FSW to respond to events such as spacecraft time tick, the availability of new serial port data, or external sensor actuation. The FSW is organized into a series of functions and data structures. Functions are blocks of ordered instructions that the Microblaze executes to either manipulate data structures or invoke other functions.

The following subsections describe the functionality that the FSW and FPGA cores implement. First the foundation of the FSW is presented – the main execution loop and the timekeeping functions as shown in section 3.2.1 and 3.2.2. The remaining functionality is presented in the order sections 3.2.3 through 3.2.9 that it is invoked to downlink REXIS science data to Earth. Each subsection title has the same circle icons from Figure 3-1 indicating which avionics component the functionality is implemented

on or interacts with significantly. White circles signify sensors/detectors, blue circles signify hardware, red circles signify FPGA cores, and yellow circles signify software.

3.2.1 FSW Main Loop and Interrupt Service Routines

The Main Loop is a collection of ordered function calls in the FSW that continuously runs after REXIS is powered up and initialized. This code is responsible for invoking other FSW functionality like command processing, science mode data processing, and telemetry downlink as shown in Figure 3-11. The main loop is supported by several Interrupt Service Routines (ISRs) that complete periodic tasks and respond to events external to the FSW.

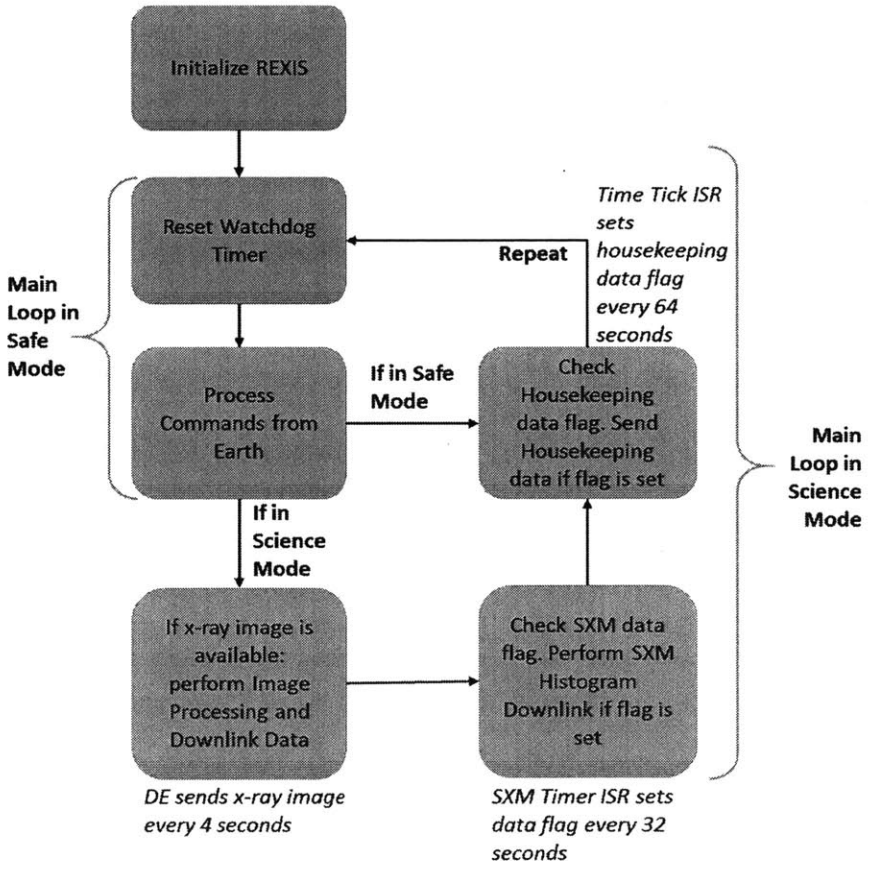

Figure 3-11: REXIS FSW Main Loop

Figure 3-11 is a flowchart diagram that shows the Main Loop's sequence of FSW function calls. In safe mode, the Main Loop initially consists of the FSW resetting the watchdog timer and processing commands. The watchdog timer is an FPGA core used for resetting and re-initializing the FSW in the

event FSW crashes and fails to reset the watchdog timer. During normal FSW operation, the watchdog timer is constantly reset and never causes a system reboot. After resetting the watchdog timer, the FSW processes any commands in the FSW's command buffer. This buffer is a memory location in SDRAM that contains data from Earth, relayed to REXIS by the OSIRIS-REx C&DH system.

In science mode, the FSW's Main Loop performs scientific data processing functions in addition to the safe mode tasks of resetting the watchdog timer and processing commands. Scientific data processing consists of acquiring, processing, and downlinking asteroid x-ray data and solar x-ray data. The DE sends a new x-ray image to the FSW through the framegrabber every four seconds. This 4-second cadence requires the main loop to execute its cycles quickly enough to catch the next frame in order to continuously perform x-ray image processing and downlink the results. The SXM timer ISR in Table 3.3 sets a flag every 32 seconds to indicate that the SXM data acquisition and processing core is ready with another SXM data sample. If the Main Loop detects an active SXM data flag, this telemetry is also downlinked.

The FSW handles housekeeping data acquisition in both safe and science modes. After scientific data processing is completed, the Main Loop checks a housekeeping flag. If the flag is active, the Main Loop acquires and downlinks housekeeping data. This data is comprised of voltages, temperatures, FSW state, and other values that indicate the health and status of the REXIS instrument. Once housekeeping data is downlinked, the Main Loop begins another iteration by resetting the watchdog timer again.

A periodic telemetry function called by the external and internal time tick ISRs (Table 3.3) independently of the main loop is used for controlling the downlink of certain periodic telemetry. This function asserts the housekeeping flag every 64 seconds and sends aliveness telemetry. The housekeeping flag signals the main loop to downlink housekeeping. The aliveness telemetry consists of REXIS no-operation (NOOP) data sent every four seconds independently of the main loop. This NOOP telemetry serves as periodic pings that let the OSRIS-REx spacecraft sense that REXIS is functioning nominally. If the science telemetry stream is enabled, then the NOOP telemetry is not sent because science telemetry also satisfies this spacecraft-imposed aliveness requirement.

Table 3.3: FSW Interrupt Service Routines

ISR Name	ISR Attributes		Condition to Activate ISR	Purpose of ISR	State Variables Changed
Switch Washer 3.2.4	GPIO	Continuous	Change in switch washer sensor voltage	Track switch washer state and shut off frangibolt if switch washer sensor transitions from closed to open	switch washer open/closed state
External Time Tick 3.2.2	GPIO	Side A/B	Falling edge of the time tick signal from spacecraft	Perform periodic FSW timekeeping and telemetry tasks. Resets the Time Tick Timer so its ISR does not unnecessarily execute	seconds elapsed, subseconds elapsed, housekeeping flag
Internal Time Tick 3.2.2	Timer	Continuous	Expiration of timer with 1.01 second period	Performs the same tasks as the Time Tick GPIO ISR in case the spacecraft time tick does not arrive. Missed time ticks are also noted	Seconds/subseconds elapsed, housekeeping flag, missed time-tick count
Sub-second Timer 3.2.2	Timer	Continuous	Expiration of timer with 0.001 second period	Updates the FSW's subseconds timing value every millisecond	subseconds elapsed
Frangi-bolt Timer 3.2.4	Timer	Frangibolt	Expiration of timer with 1 second period	Handles frangibolt timing tasks such as the arm and fire timeout.	Frangibolt off/armed/firing state
SXM Timer 3.2.6	Timer	Science	Expiration of timer with 1 second period	Handles the FSW's SXM management tasks and state transitions every second.	SXM timer value, SXM data flag, SXM data acquisition state
Space-craft Serial Port 3.2.3	Serial	Side A/B	Data is available from the OSIRIS-REx spacecraft	Transfer spacecraft command data from the small buffer in the serial port FPGA core to a large buffer the FSW uses.	Command data Buffer
DE serial Port 3.2.5	Serial	Science	Data is available from the DE over the CameraLink serial port	Transfer DE data from the small buffer in the serial port FPGA core to a large buffer the FSW uses.	DE data buffer

Explanation for ISR Attributes

GPIO	ISR is activated through a voltage change on a GPIO pin
Timer	ISR is activated periodically through the expiration of a timer implemented as an FPGA core
Serial	ISR is activated when data is available on a serial port
Continuous	ISR is always enabled after initialization
Side A/B	Two identical ISRs exist for side A or B. One of them is enabled on start-up based on the side-select voltage
Frangibolt	ISR is enabled only while the frangibolt is armed or is firing
Science	ISR is enabled only during science mode

The periodic telemetry function is called either by one of two sources – either the external time tick ISR or the internal time tick ISR in Table 3.3. The external time tick ISR is activated by the spacecraft 1Hz time tick voltage pulses while the internal time tick ISR is activated by an FPGA timer core every 1.01 seconds. Normally, the 1Hz rate of the spacecraft time ticks triggers the periodic telemetry function before the internal time tick ISR. However, if the spacecraft fails to send a time tick, the FPGA timer core activates every 1.01 seconds and triggers the internal time tick ISR. This occurrence is known as a missed time tick and is logged by the FSW. The number of missed time ticks is downlinked in housekeeping since this information could indicate a fault with the REXIS or OSIRIS-REx systems. When the spacecraft does send a time tick to REXIS, the FPGA timer core that activates the internal time tick ISR is reset so it does not unnecessarily activate the periodic telemetry function.

3.2.2 Timekeeping

The REXIS system needs to keep track of time to acquire scientific data at the correct intervals, correctly pace FSW execution, and allow REXIS operators on Earth to correlate scientific and engineering telemetry with timestamps from the rest of the spacecraft system's telemetry and state. REXIS follows the timekeeping convention of the entire OSIRIS-REx system of measuring the number of seconds elapsed since a particular date. This count of seconds is broken into seconds and subseconds values – the former is the whole number of seconds elapsed and the latter is the fractional component.

REXIS has two methods of keeping track of time: spacecraft supplied timing data and internal timing mechanisms. If the REXIS FSW receives no time update telemetry or time-tick pulses from the spacecraft, the FSW uses two timers implemented as FPGA cores to keep track of the number of seconds and subseconds elapsed since power-up. These FPGA timer cores trigger the internal time tick ISR and subseconds timer ISR every second and millisecond respectively to update the FSW counters that correspond to these time values.

The time update command data and time tick pulses from the spacecraft are used for keeping REXIS's second and subsecond counters in synchronization with the spacecraft. The OSIRIS-REx

spacecraft is designed to send time update voltage pulses to REXIS every second which in turn are used by REXIS to synchronize its timekeeping with the spacecraft. Therefore, time tick pulses take precedence over REXIS's internal FPGA core timekeeping hardware with regards to updating the FSW's second and subsecond counters. The OSIRIS-REx spacecraft also sends REXIS time-update commands that contain the mission elapsed time at the moment of the next time-tick voltage pulse. REXIS overwrites the second and subsecond counter values with the latest data available from the time update command data. These commands are useful immediately after REXIS powers up since the OSIRIS-REx time is not stored in the volatile REXIS avionics memory.

3.2.3 Command Processing

The REXIS FSW processes data relayed by the OSIRIS-REx spacecraft to REXIS from Earth. After command data passes through the REXIS/OSIRIS-REx interface further detailed in section 3.1.5, the data is available to the FSW through a serial port FPGA core. This Xilinx-supplied FPGA core triggers the spacecraft serial port ISR that transfers command data from the FPGA serial port core and places it in the FSW's command buffer. The command buffer is an area of the SDRAM set aside for command data.

The Main Loop periodically checks for command data in the command buffer and processes any available command data. The FSW uses a state machine to validate the digital data of the command such as the headers, parameters, and checksums. Invalid commands are rejected or dropped while the FSW calls the appropriate function to start the processing of a valid command. The FSW keeps track of the number of commands dropped, rejected, and processed and downlinks this telemetry in the housekeeping packet. Once a valid command is detected, the FSW uses the op-code data, or a particular number, in the command to invoke the appropriate functionality shown in

Table 3.4. In general, commands either activate particular REXIS functionality like downlinking certain data or firing a frangibolt, or change the instrument behavior/state.

Table 3.4: REXIS Commands, Actions, and State Changes

Command	Opcode	Action/Functionality	State Change
Enter Safe Mode	0x8001	Disables Scientific Data Acquisition Functions	Mode Flag to Safe Mode
Enter Science Mode	0x8002	Enables Scientific Data Acquisition Functions	Mode Flag to Science Mode
Enable Science Telemetry	0x8004	Starts Downlink of Scientific Telemetry	Science Telemetry Flag to Enabled
Disable Science Telemetry	0x8007	Stops Downlink of Scientific Telemetry	Science Telemetry Flag to Disabled
Arm Frangibolt	0x8008	Allows FSW to accept Frangibolt Fire Command	Frangibolt State to Armed
Fire Frangibolt	0x8010	Applies Power to Frangibolt Actuator	Frangibolt State to Firing
Shutdown Frangibolt Power	0x8020	Removes Power from Frangibolt Actuator	Frangibolt State to Off
Request Raw CCD Frame	0x8040	Downlinks CCD Pixels without Image Processing	Interrupts Image Processing
Request Bias Map	0x8100	Downlinks Bias Map Pixels	
Regenerate Bias Map	0x C0C4	Forces Bias Map Regeneration	Interrupts Image Processing
Request Hot Pixel Mask	0x8200	Downlinks Hot Pixel Mask Data	
Request Parameter Settings	0x8803	Downlinks REXIS Operating Parameters	
Memory Load	0x9000	Uplinks Values in Computer Memory	
Memory Dump	0xA000	Downlinks Segment of Computer Memory	
Function Upload	0xC000	Uplinks Code for New FSW functions	
REXIS NOOP	0xC003	Does nothing other than increment command counter like other commands	
Send Safe-Me Message	0x0000	Sends Message to Spacecraft Requesting that REXIS Power is Shut Off	REXIS is shut off by Spacecraft
Parameter Adjustment Threshold	0x8806	Adjusts Image Processing Thresholds	
Parameter Adjust Level Limit	0x880C	Adjusts Image Processing Thresholds	
Parameter Adjust One-Byte	0x8818	Adjust Value of 1-byte Parameters	
Parameter Adjust Two-Bytes	0x8830	Adjust Value of 2-byte Parameter	
Parameter Adjust Hot Pixel	0x88C0	Adjusts the Hot Pixel Mask for Image Processing	

3.2.4 Radiation Cover Actuation ●●●○

In order to collect asteroid X-ray data from the CCDs, the radiation cover needs to be opened. The radiation cover is a deployable metal cover on a spring-loaded hinge that is held closed with a frangibolt during the OSIRIS-REx spacecraft cruise to Bennu. Opening the radiation cover by applying current to the frangibolt exposes the CCDs to space so they can sense x-rays from Bennu. While closed, the radiation cover protects the REXIS CCDs from radiation during OSIRIS-REx's interplanetary cruise. Upon processing a certain set of commands, the REXIS avionics actuates a frangibolt device that fractures the bolt holding the radiation cover closed while a set of springs forces the radiation cover open. A switch washer sensor relays to the FSW that the frangibolt has broken the bolt and the radiation cover is open. The avionics component of the radiation cover system consists of two parts:

1. Hardware such as circuitry that provides power to the frangibolt actuator, the switch washer sensor, and associated harnessing that allows components within the electronics box to interface with the frangibolt actuator and switch washer at the top of the REXIS instrument.
2. FPGA cores and FSW that control the hardware in order to fire the frangibolt and generate switch washer telemetry. The FPGA contains timing and GPIO cores that support the FSW. The FSW contains frangibolt command processing functions and ISRs that manage the frangibolt related timing and switch washer sensor data.

The key interface between the frangibolt hardware and frangibolt-associated FPGA cores and FSW are the MEB FPGA's GPIO pins. When the FSW is ready to actuate the frangibolt, it commands FPGA GPIO cores to apply voltage on these pins that in turn activates the frangibolt hardware. Another GPIO pin is used to sense the output of the switch washer sensor and activate the Switch Washer ISR that updates the FSW switch washer state variable. This section discusses the FPGA cores and FSW within the radiation cover system while section 3.3.1.1 discusses the hardware component in more detail.

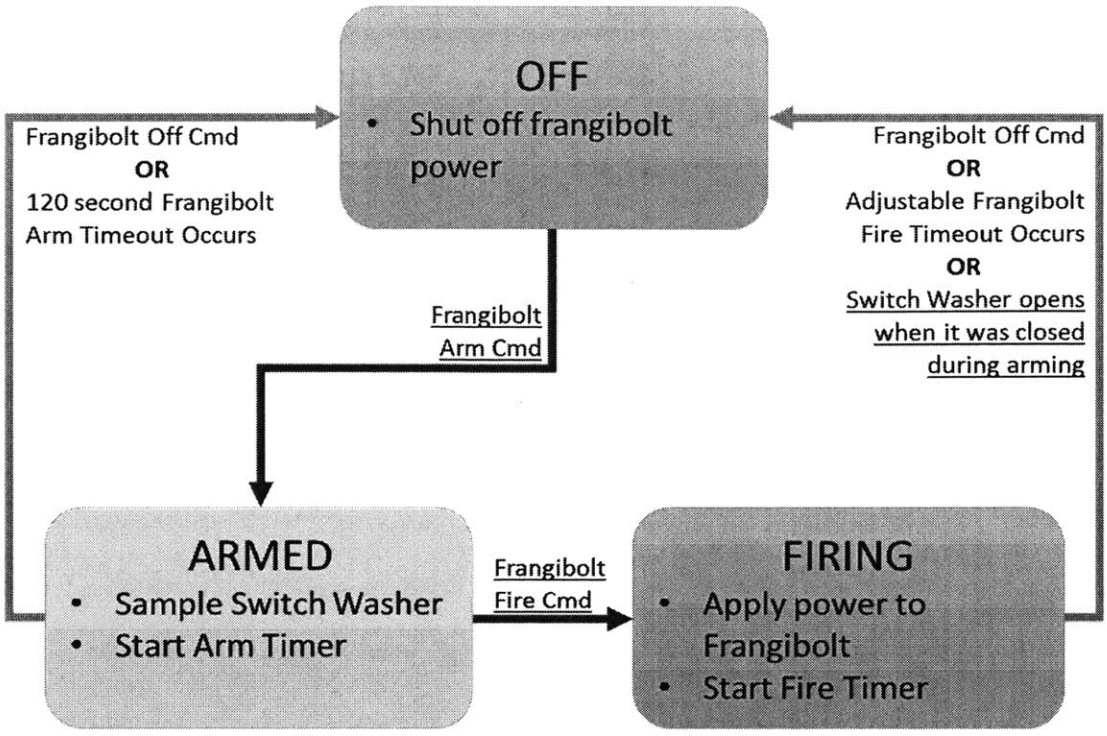

Figure 3-12: Frangibolt Actuation State Diagram

To open the radiation cover, the nominal sequence is shown with underlined text in Figure 3-12 where:

1. The frangibolt-arm command is sent. This command advances the FSW to the frangibolt-armed state and enables the FSW to accept the frangibolt-fire command within a 120 second window
2. The frangibolt-fire command is sent within 120 seconds after the frangibolt-arm command. This command puts the FSW in the frangibolt-fire state by activating the frangibolt DC/DC converter through an FPGA GPIO core and GPIO pin. These components are further detailed in the frangibolt hardware section 3.3.1.1.
3. After successful processing of the frangibolt-fire command, the frangibolt actuator heats up due to current from the active frangibolt DC/DC converter. The heating causes the frangibolt actuator to expand and axially stress the bolt holding the radiation cover closed.
4. The stress imparted by the frangibolt actuator onto the radiation cover bolt eventually fractures the bolt, causing the radiation cover to open.

5. The FSW continuously senses the switch washer through a GPIO pin. When the radiation cover opens, the FSW sees a transition in the output of the radiation cover's switch washer sensor. The change in the switch washer's output causes the FSW to shut off the frangibolt DC/DC converter and cease the heating of the frangibolt actuator. Nominally, this transition in the switch washer value should happen before a frangibolt-firing timeout value that is set in the FSW. Now the FSW is in the frangibolt-off state.

There are many safety mechanisms in the radiation cover opening system to prevent unwanted actuation of the frangibolt actuator. The following safety mechanisms are used to prevent this contamination from happening:

1. The arm/fire command sequence prevents an errant frangibolt-fire command from being immediately accepted
2. The frangibolt firing timeout has a default value of zero. If this parameter isn't adjusted correctly through a parameter-adjust command before frangibolt firing, then the frangibolt DC/DC converter is shut off immediately after it is turned on and prevents any unwanted frangibolt actuation.
3. Actuating the frangibolt requires substantially more electrical power (as shown in Table 3.1) from OSIRIS-REx than REXIS is normally allowed to use. If the frangibolt DC/DC converter is activated without removing the OSIRIS-REx REXIS-specific power limit, REXIS would be shut off due to a power overload seen on the spacecraft's fault protection system.
4. The frangibolt fire timeout protects against a faulty switch washer. First, if the switch washer is working properly, then it indicates a closed radiation cover while arming. Secondly, the switch washer senses an open radiation cover during frangibolt firing, the FSW takes the appropriate action to shut off the frangibolt. If either of these two actions do not occur, the FSW will not apply power to the frangibolt beyond an experimentally determined fire timeout duration in order to prevent frangibolt overheating.

If current is applied to the frangibolt actuator for too long the actuator will outgas due its increased temperature. This outgassing is very undesirable during the OSIRIS-REx mission since outgassing could contaminate the SRC and TAGSAM mechanisms that are located near REXIS aboard the spacecraft. The outgassing problem is initially caused by the frangibolt arm and fire commands that are marked with red arrows in in Figure 3-12 to highlight this hazard.

3.2.5 Image Processing

Every four seconds, the image processing functionality aboard REXIS creates an x-ray events list a few hundred bytes long from an uncompressed 8MB x-ray image stored in SDRAM. Image processing is necessary the OSIRIS-REx telemetry budget cannot accommodate REXIS downlinking uncompressed x-ray images. An x-ray events list contains the position, shape, and energy of scientifically interesting x-ray events on the CCD detector plane. These x-ray events are created by x-ray photons striking one or more adjacent pixels on the CCDs. Scientifically interesting x-ray events are created by x-ray photons between certain intervals of x-ray energies. The x-ray events list is the primary REXIS science telemetry product.

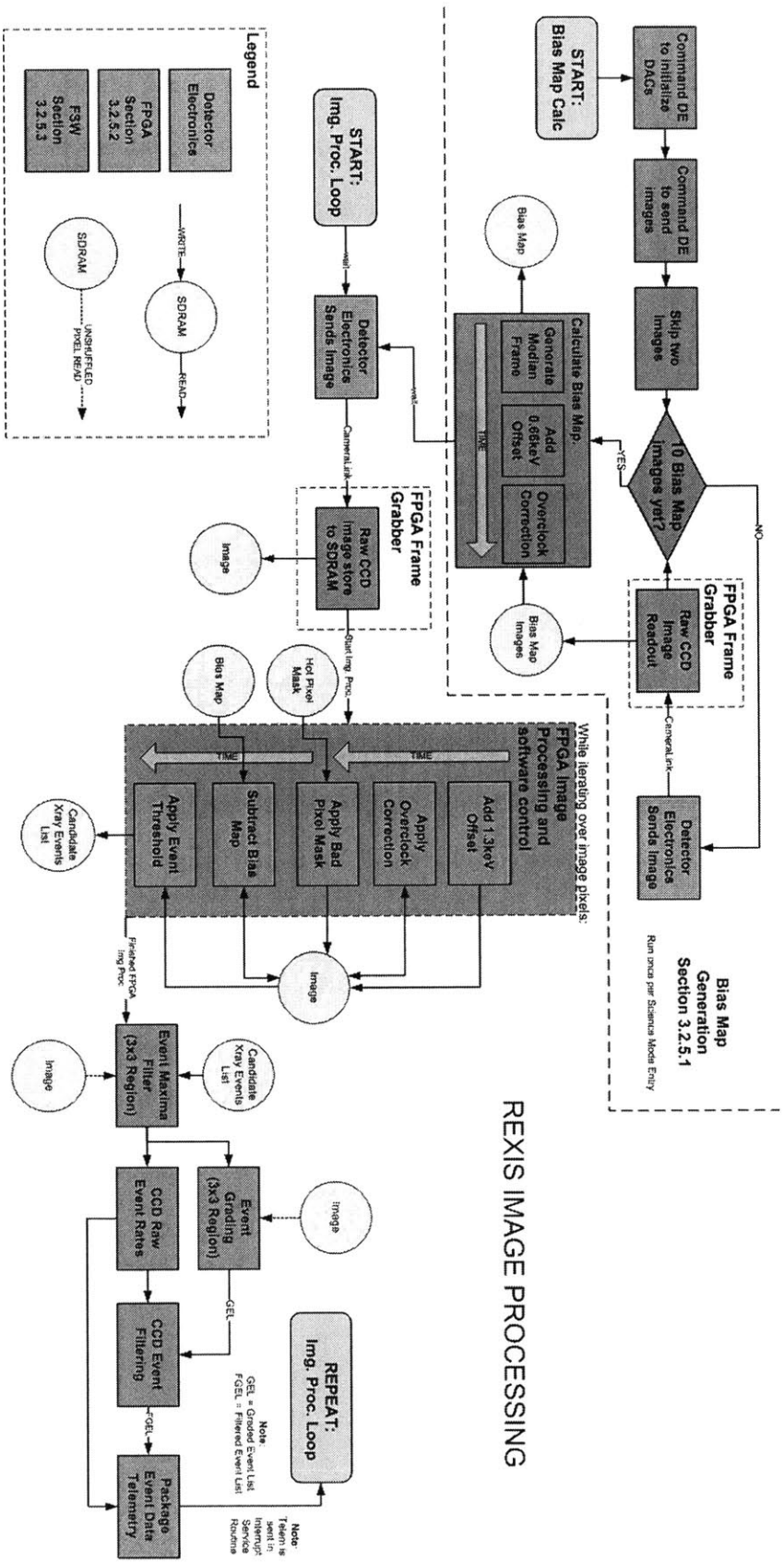

Figure 3-13: Image Processing Block Diagram

Figure 3-13 shows how the x-ray events list is generated from an x-ray image supplied by the DE. The process is initiated when a FSW-generated bias map, which is a composite image of the baseline response of each CCD pixel, is available. The bias map is subtracted from an x-ray image on a pixel-by-pixel basis to remove any background CCD detector response from an uncompressed image, allowing x-ray events to be found. Once the bias map is available, the FPGA's framegrabber core acquires x-ray images from the DE and performs the initial repetitive pixel-by-pixel image processing calculations such as bias-map subtraction. The framegrabber generates a Candidate X-ray Events List (CXEL) that is a list of potential scientifically interesting x-ray events within the x-ray image. Next, the FSW uses the CXEL in conjunction with the framegrabber-processed image in SDRAM to generate the x-ray events list. Finally, the FSW packages the x-ray events list into a telemetry packet suitable for downlink to Earth. The following subsections go over the various steps in the image processing algorithm in Figure 3-13 in detail.

Image processing requires the FSW to interact with the DE to obtain x-ray image data through the CameraLink interface, as shown with the connectors J9 and P9 in Figure 3-4. The FSW commands the DE by sending DE scripts through a serial port built into the CameraLink interface between the MEB and DE. The DE scripts are ordered DE-specific lists of instructions and parameters for appropriately driving the CCDs, reading out pixel data, and initializing DE hardware. DE scripts are stored in the FSW's memory and relayed to the DE as necessary. The DE sends a ready signal over the CameraLink serial port to let the FSW know it is ready to receive DE script data. The FSW receives this notification through the DE Serial Port ISR. The other component of the CameraLink interface are a series of differential voltage pairs used to transmit x-ray image pixel data sensed by the framegrabber FPGA core.

3.2.5.1 Bias Map Generation

The first step taken by the REXIS FSW to generate x-ray events lists is creating a bias map. A bias map is a measure of CCD background noise and is continuously used in image processing for noise reduction. To generate a bias map, REXIS first acquires and stores ten unprocessed x-ray images in the

SDRAM for bias map calculation using the framegrabber. Then FSW calculates the bias map on a pixel-by-pixel basis. Each bias map pixel is the median of the same pixel across the 10 x-ray images stored in SDRAM. Before finding x-ray events, this bias map must be subtracted out on a pixel-by-pixel basis from every CCD image to remove this nonzero background CCD response

CCD noise embedded in the bias map is reduced by first adding an offset of 0.6 keV to each pixel value and then performing the overclock correction process. The addition of 0.6 keV to each pixel ensures that pixel values remain positive after subtraction since pixel values are represented as unsigned integers. The overclock correction process, which is applied to both bias maps and uncompressed x-ray images, consists of subtracting off the inherent noise in the pixel readout circuitry from each pixel. This readout noise can be measured within non-physical overclock pixels that result from reading pixel data beyond the physical borders of the CCD. Once the median values for the bias map are calculated, offsets added, and overclock correction is performed, the bias map is stored in SDRAM and ready to be used continuously for image processing.

3.2.5.2 FPGA-based image processing ●

Once the bias map is stored in SDRAM, the FSW starts the image processing loop that constantly processes x-ray images using the bias map until REXIS leaves science mode. The FSW directs the MEB FPGA's framegrabber core (denoted by the large dashed box in the middle of Figure 3-13) to perform the first image processing steps on incoming x-ray images. The framegrabber initially adds a 1.3keV offset to each pixel to prevent unsigned integer underflows from upcoming subtraction operations. The framegrabber then performs two subtractions on each image pixel:

1. **Bias map subtraction** – For each image pixel, the value of the same pixel in the bias map is subtracted from the value of the image pixel. This subtraction removes the default response of the CCD.

2. **Overclock correction** – Like the bias map pixels, each x-ray image pixel value has its overclock value subtracted from it. The framegrabber computes these average overclock values prior to applying the overclock correction.

The framegrabber also discards any pixels that the FSW marks as defective in the hot pixel mask stored in SDRAM. More specifically, these hot pixels will not appear in the final x-ray events list since the hot pixel mask data structure tells the framegrabber which pixels to ignore. Once these processing steps are completed, the framegrabber checks if each pixel value exceeds the event threshold (ET) value. If a pixel value is greater than the ET after the bias map and overclock subtractions, then it could be a potential x-ray event of scientific interest. A candidate x-ray events list (CXEL) is a list of these potentially scientifically interesting x-ray events. It consists of a series of pointers that point to x-ray image pixels that exceed the ET. Both the CXEL and the framegrabber-processed x-ray image are stored in SDRAM. Along with performing pixel-wise image processing, the CXEL is the primary data product of the framegrabber core.

3.2.5.3 FSW-based Image Processing

Once the CXEL and framegrabber-processed image is in SDRAM, the FSW takes over the image processing cycle. On a high level, the FSW removes x-ray events from the CXEL until an appropriate amount of scientifically interesting x-ray events remain based on the data in the framegrabber-processed image. This CXEL subset is known as the x-ray events list and is the primary REXIS science telemetry product. Furthermore, the FSW also performs event grading and event energy summation on each x-ray event, in order to better characterize the scientifically interesting x-ray events. The results of these calculations are also downlinked as part of the x-ray events list. However, if the x-ray events list is too large for the REXIS mission telemetry allocation, the FSW randomly removes events from the x-ray events list. Thus, the FSW generates an x-ray events list with the framegrabber's output that consists of a list of x-ray events' position on the CCDs, event grade, and event energy.

X-ray events consist of an x-ray photon's energy distributed over one or more adjacent CCD pixels. Therefore, multiple pixels that form a single x-ray event could appear in the CXEL if they exceed the ET. The FSW selects one pixel that corresponds to the x-ray event from these multiple pixels through the Event Maxima Filter function in the image processing block diagram (Figure 3-13). This filter consists of the FSW iterating through the CXEL and removing any entry with a pixel value that is not the local maximum in a 3x3 grid of surrounding pixels' values on the CCD detector plane. After the Event Maxima Filter process is complete, the CXEL consists of pixels that correspond to unique x-ray events.

The FSW also removes CXEL entries if their pixel value is greater than the CCD upper limit discriminator (ULD) parameter in order to filter out x-rays and cosmic rays with unsuitable high x-ray energies. This process is similar to the framegrabber screening pixels with the ET, except in this case, the scientifically interesting pixels are less than the ULD screening parameter.

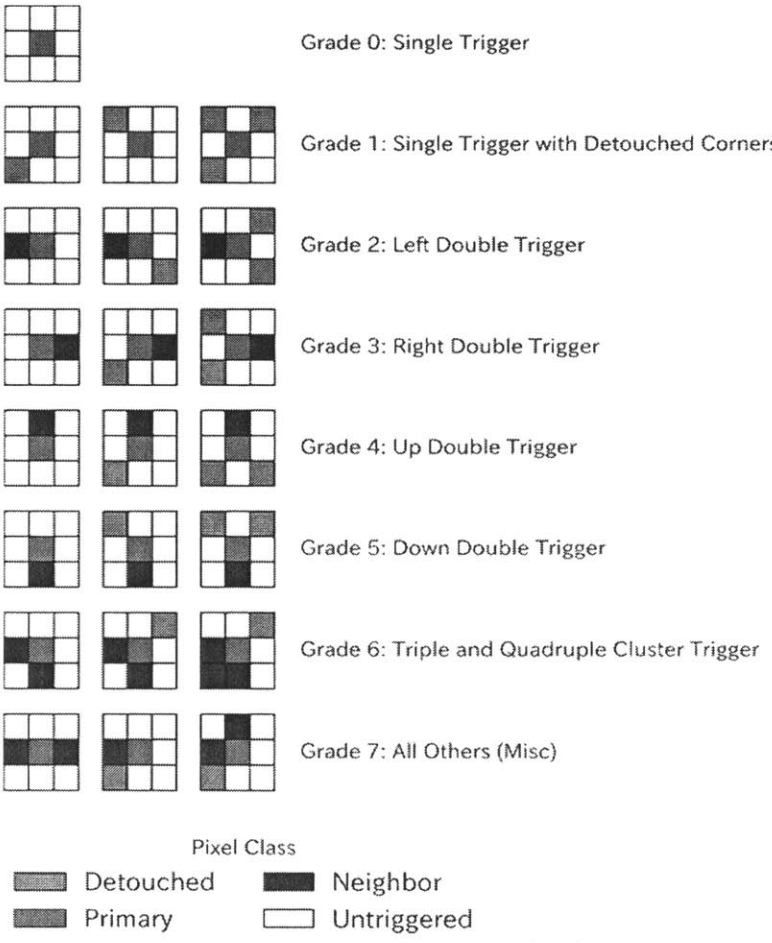

Figure 3-14: X-ray Event Grades [11]

The remaining pixels in the CXEL each correspond to a unique x-ray event since they are the local maximum amongst their surrounding pixels on the CCD detector plane. The FSW iterates once more over these remaining entries to assign them a grade and calculate their x-ray event energy. Both of these operations take the value of the physically adjacent pixels into account. The x-ray event grade information characterizes the shape of the x-ray event and is based on the adjacent pixels' value exceeding a split threshold (ST). The possible grades are shown in Figure 3-14 where the colored pixels denote adjacent pixels greater than the ST value. X-ray event energy is the sum of the center pixel's value and horizontally/vertically adjacent pixels' values that exceed the ST. If the diagonally adjacent pixels' values are greater than the ST, they are included in the event energy summation provided the horizontally/vertically adjacent pixels next to them are also above the ST as well [11].

If there are too many x-ray events after event grading, a process called event rate filtering is used to discard randomly selected events. Excess x-ray events can be caused by high solar x-ray emissions. To implement event rate filtering, the FSW essentially flips a biased coin for each event where the bias fraction is the desired number of events divided by the total number of events. On average, the number of events remaining after this process is the desired number of x-ray events. By default, REXIS is limited to sending down 800 events per frame based on the OSIRIS-REx telemetry budget allocation to REXIS. This 800 events per frame value is adjustable through a command and is known as the event rate limit. After event rate filtering is completed, the CXEL is the primary REXIS science data product containing information about the position, energy and grade of each scientifically interesting x-ray event. This final product is now ready for telemetry packaging and downlink to Earth by the FSW.

3.2.6 SXM Control and Data Processing ●●●○

The SXM data processing subsystem is required to detect, measure, and count x-ray event pulses within the signal sent from the SXM detector to the MEB. The SXM data processing functionality is split across four components – the SXM sensor (Figure 3-5), physical MEB hardware, FPGA cores, and flight software. This section primarily focuses on the processing of SXM generated signals within FPGA cores

and FSW. SXM hardware is discussed with more detail in section 3.3.1.7. The SXM hardware on the MEB is designed to filter out noise from the SXM sensor signal and detect signal peaks that correspond to solar x-ray events. The MEB also contains an analog to digital converter (ADC) that samples the SXM signal peaks [8]. Meanwhile, the combination of the SXM FPGA core and FSW create SXM histogram that serves as solar x-ray spectrum telemetry. This telemetry is generated by counting the number of solar x-ray events for a series of histogram bins this correspond to x-ray event energy ranges.

The MEB FPGA has a custom-built SXM core that generates the SXM histogram. The SXM core uses a GPIO pin to sense when the MEB circuitry detects a solar x-ray event peak. When a peak is detected, the SXM core uses other GPIO pins to command the SXM ADC to sample the peak's voltage. The SXM core uses the SPI protocol[9] to read the solar x-ray event peak magnitude from the ADC. It also creates a 512 bin histogram of the peak values read from the ADC over 32 second intervals. This process of sampling the ADC and updating the histogram is controlled by a state machine within the SXM core [8].

The FSW interfaces with the SXM core to periodically downlink the SXM histogram and reset histogram bin counts to zero. This SXM period for downlinking and clearing the histogram is normally 32 seconds but can be adjusted through command. The values in the 512-bin SXM histogram appear to the FSW as values at preset memory addresses through the design of the SXM core. No special FSW interface is needed to access the histogram. Once the FSW reads the 512 bin histogram, this data is assembled into a telemetry packet and sent to the spacecraft at the end of the SXM period for downlink to Earth later [8].

The FSW also has control over the supporting voltages that are sent from the MEB to the SXM sensor. These voltages are the +5V power line, SDD high voltage (HV) bias, and TEC power. The FSW also controls the voltage for the SXM trigger threshold that is used by MEB hardware to detect valid solar x-ray events over the background noise. For the +5V power, TEC power, and SXM HV bias power lines,

[9] SPI – Serial Peripheral Interface – A serial digital communication protocol used for communication between microchips on PCBs

the FSW uses an FPGA GPIO core to actuate the circuitry on the MEB that provides this functionality. For the analog SDD HV bias and SXM trigger threshold voltages, the FSW sends values to the SXM core that interfaces using SPI with two digital to analog converters (DACs). These DACs on the MEB provide the reference voltages that other MEB circuitry use to generate the trigger threshold voltage and SXM HV bias.

3.2.7 Housekeeping Data Acquisition ●●●○

REXIS housekeeping data consists of voltages and temperatures sampled across the REXIS instrument and information about the FSW and image processing state like the number of commands processed, science telemetry downlink state, science/safe mode state, number of x-ray images processed, and FSW version. Housekeeping telemetry is collected and downlinked every 64 seconds by default but the housekeeping period is adjustable through a command from Earth.

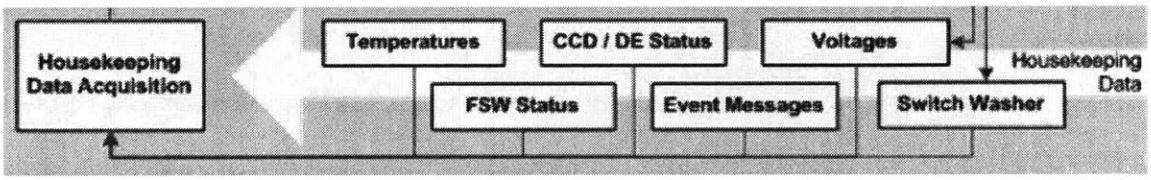

Figure 3-15: Housekeeping Data Flow

The components of a housekeeping packet are shown in Figure 3-15 that is a subset of the housekeeping data flow within the diagram in Figure 3-1. The bulk of housekeeping data consists of temperature and voltage readings. The FSW acquires these readings through FPGA cores that interface with ADCs. These ADCs convert the analog voltages from temperature sensors and power rail monitoring circuits into digital values for the FSW. However, there are two exceptions to this sensor sampling setup:

1. **DE/CCD housekeeping** – In science mode when the DE and CCDs are turned on, the FSW uses the serial port built into the MEB/DE CameraLink interface to request housekeeping data from the DE FPGA. The DE FPGA then samples all the voltage and temperature sensors aboard the DE PCBs and CCDs using a DE-specific set of ADCs. The DE FPGA then sends this housekeeping data to the MEB FPGA for packing into the housekeeping packet. In safe mode,

dummy data generated by the FSW is used since the DE and CCDs are off. The DE Serial Port ISR notifies the FSW when the DE is transmitting housekeeping data.

2. **Platinum Resistance Thermometer (PRT) sensors** – REXIS uses PRT sensors to measure the frangibolt housing temperature, CCD DAM temperature, and radiation cover temperature. These sensors are wired into the ADC controlled by the SXM core. When the SXM core is in active science mode, these PRT voltages are sampled by the SXM core and supplied to the FSW. The FSW also performs low-pass filtering on these temperature values to remove noise.

The FSW also keeps samples of a variety of other parameters for downlink in the housekeeping packet such as

1. Switch washer state by using a GPIO core to sample the GPIO pin connected to the frangibolt's switch washer sensor.
2. FSW status such as the current FSW version number (useful for debugging), on/off state of science telemetry, and if REXIS is functioning in safe or science mode.
3. Timing related parameters such as the number of missed time ticks and missed time updates.
4. Number of commands processed, dropped, and rejected.
5. CCD image processing parameters such as event rates and number of frames processed since startup.

The final component of the housekeeping packet is the event log. The event log is used to keep track of notable events during REXIS operation. Examples of notable events are REXIS initialization status, the radiation cover opening, or the completion of bias map generation. The FSW implements the event log as a queue of event messages that consist of an ID indicating the type of event, an event value describing what the event was, and a timestamp indicating when the event message was written to the event log queue. Events are written to the event log queue as soon as they occur. During housekeeping packet assembly, the FSW will empty the event log queue and transfer all the events the housekeeping packet for downlink to Earth.

3.2.8 Telemetry Packaging

Once telemetry data is collected, the FSW packs this telemetry by adding padding to meet 4-byte alignment requirements and IP/UDP/CIP/IDP headers.

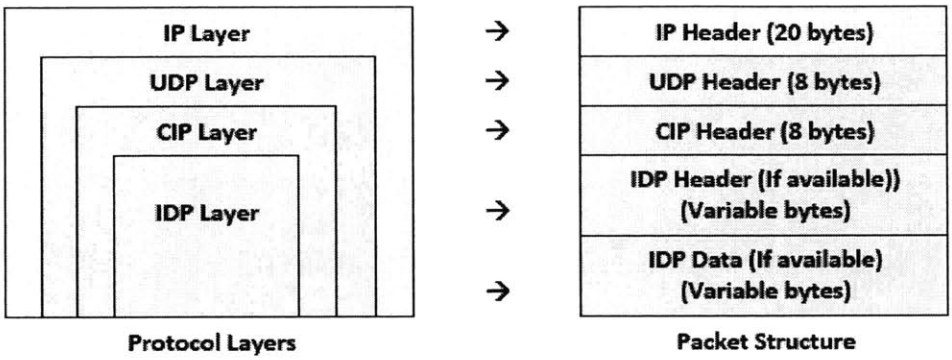

Figure 3-16: REXIS Telemetry Protocol and Packet Structure

This extra data is added to telemetry packets in order to maintain compatibility with the spacecraft FSW data interface shown in Figure 3-16. The IP and UDP headers identify REXIS telemetry to the OSIRIS-REx spacecraft. The CIP header identifies what kind of REXIS telemetry is being sent and the IDP header contains details about telemetry data like how many packets in the series and marker words to detect the telemetry. Once these telemetry packaging actions are completed, the FSW puts the packet in the telemetry buffer and the FPGA serial port core sends the data to the spacecraft.

3.2.9 Function Upload

New FSW code can be uploaded to REXIS through function upload commands. This capability of Function Upload is applicable only to a specific set of FSW functions. For example, a new CCD drive algorithm that produces x-ray image data with less noise could be developed after REXIS launches. This new CCD drive algorithm could be uploaded to REXIS through a function upload command that contains new code for the DE CCD Sequencer function. Thus the avionics system has the capability to accommodate some modification to its functionality even after its integration with the OSIRIS-REx spacecraft and launch.

Table 3.5 is a list of the functions that can be modified while REXIS is in space. These functions are primarily for scientific data processing and can be implemented/upgraded in future cycles of research and development. Some of these functions implement the absolute minimum functionality required for REXIS mission success. Achieving minimum requirements allowed for more FSW testing time and facilitated an on-time delivery of REXIS to OSIRIS-REx. Examples of such functions are - more sophisticated event rate filtering, detection of defective columns in the CCD, or better event grading schemes. These algorithms can still be developed, tested with spare REXIS hardware on Earth, and uploaded to the REXIS instrument in space.

Table 3.5: Uploadable Functions within REXIS FSW

ID	Function Name	Type	Default Implementation in FSW
0	X-ray image processing	Image Processing	Functionality for processing x-ray images from the framegrabber core as outlined in section 3.2.5.3
1	Grade Event	Image Processing	Functionality for processing x-ray events in the CXEL as outlined in section 3.2.5.3
2	Filter Events	Image Processing	Random removal of events from the x-ray events list if there are too many as outlined in 3.2.5.3
3	process SXM data	SXM	Processes SXM histogram after the SXM core generates it
4	hot column detect	Image Processing	Not implemented. Serves as a platform for an algorithm developed in the future that removes bad lines of CCD pixels from the x-ray events list.
5	start SXM	SXM	Turns on the SXM and starts data processing
6	stop SXM	SXM	Stops SXM data processing and shuts off the SXM
7	DE dac-init	DE Script	Initializes the DE DACs in preparation to drive the CCDs
8	DE CCD sequencer	DE Script	Programs the DE to drive the CCDs and read data from the CCDs
9	no-op handler	debug/test	This is currently a do-nothing function. Only returns zero but can be used in the future to implement other functionality.
10	set bias map	new DE sim script	Not implemented. Serves as a platform for image processing testing.
11	set sim image	new DE sim script	Not implemented. Serves as a platform for image processing testing.
12	temp sensor LPF	PRT filtering	Averages PRT sensor samples whenever they are available from the SXM core over a 60-second window.
13	calculate bias map	Image Processing	bias map is median of 10 frames on a pixel-by-pixel basis

Regardless, some uploadable functions like the Platinum Resistance Thermometer (PRT) temperature sensor low-pass filter and No-op command handler (IDs 12 and 9 in Table 3.5) are engineering-oriented. The PRT data filter was a late addition to REXIS. Although it is tested, if a better, more sophisticated filter is developed in the future, it can be added post-launch to the FSW. The no-op function is called to process the REXIS no-op command that is accepted at any time. While developing the function upload capability, various no-op functions were uploaded and tested to verify the function upload capability. A newly uploaded no-op function can be used to implement any miscellaneous functionality in the REXIS system post-launch that needs to be invoked through NOOP command.

To transmit the function upload data to REXIS a series of commands are used – each containing part of the new function's code in the form of assembly code instructions. The REXIS FSW has a built in error and checksum checking mechanism that ensures the chunks are valid and transmitted in the right order. Validated new FSW function data is put into the MEB FPGA's BRAM to be executed when needed. The FSW can accommodate four new versions of each of the functions in

Table 3.2 in addition to the default function in the FSW. The Microblaze development C-compiler desktop software determines where a new function should be placed in memory and this memory location parameter a part of the function upload command.

Commands are used to select and delete new or old variants of a function for use. This function selection ability is useful as it permits testing of multiple solutions to a problem on-orbit without tedious and time-intensive uploading and reloading of code. Uploaded functions are deleted when REXIS is turned off since the new function code is stored in volatile memory which loses data upon power-down. Thus, previously uploaded functions that are required for nominal operation must be newly uploaded every time REXIS is switched on.

3.3 Hardware Description

The electronic hardware aboard REXIS allows the FSW and FPGA cores to interface with the OSIRIS-REx spacecraft, collect engineering/diagnostic data, collect scientific data and in general, execute system functionality. Without hardware, FSW and FPGA cores would be confined to computer screens as untested designs. The bulk of the avionics hardware is located on the three boards in the REXIS electronics box. Some electrical components used for signal conditioning can also be found in the CCD and SXM sensor.

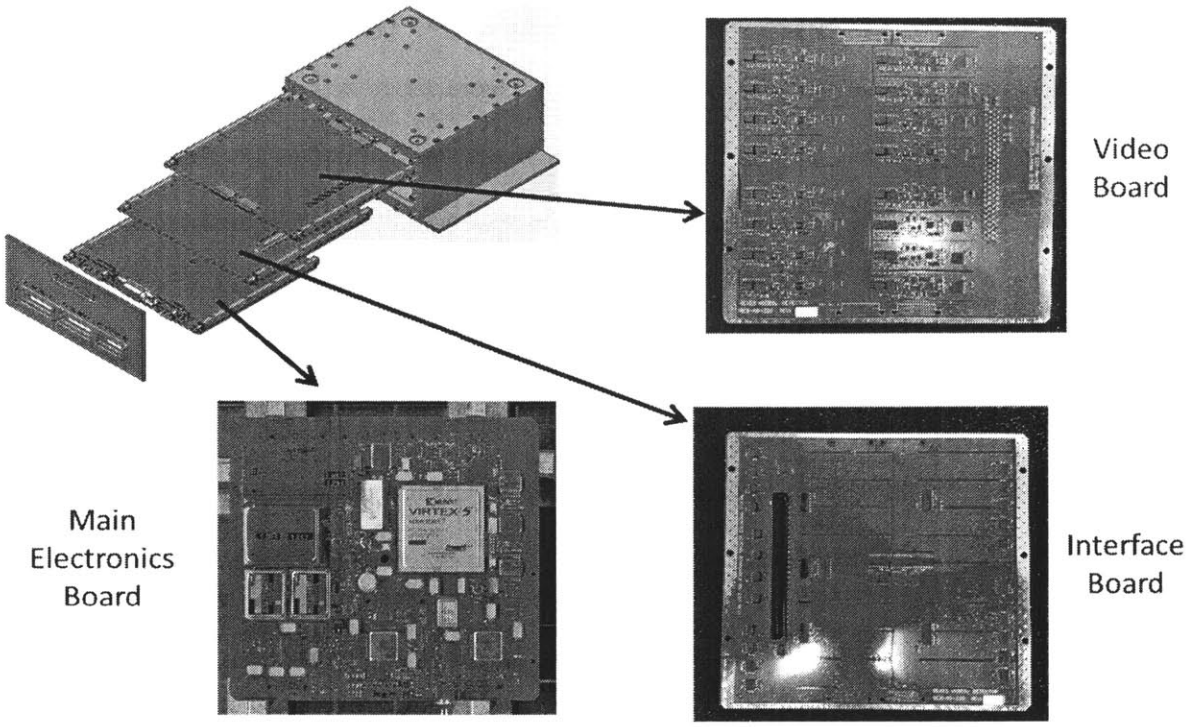

Figure 3-17: Main REXIS PCBs

Figure 3-17 shows the three main printed circuit boards (PCBs) of the REXIS system within the electronics box. The PCBs are held firmly in place within the electronics-box with wedge-lock fasteners. The PCBs exchange power and data through two sets of inter-board connectors (J9, P9, J10, and P10 in Figure 3-4) as well. The following subsections provide details about each PCBs, their components, and the interaction of these components. Each subsection title has the same circle icons from Figure 3-1 indicating which avionics component the functionality is implemented on or interacts with significantly.

3.3.1 Main Electronics Board (MEB) ○●●

The Main Electronics Board (MEB) PCB is the backbone of the REXIS avionics system and is indispensable for implementing a majority of REXIS's functional requirements. For any REXIS avionics function, either the MEB plays a role in implementing that function or the function is implemented on the MEB itself. The MEB has many electrical hardware components to provide this functionality and the following subsections will give an overview of these electrical components.

3.3.1.1 Xilinx Virtex5 FPGA

The MEB FPGA is a critical part of the MEB and the whole REXIS system. The MEB FPGA is necessary for delivering all the functionalities that the MEB provides. The REXIS MEB uses a Xilinx XC5VFX130T-1FF1738I industrial grade FPGA mounted close to the center of the MEB. This device has spaceflight heritage in a low-criticality class-D application aboard the International Space Station that is similar to REXIS in terms of criticality. This suitability is further discussed in section 4.3.1.

The reconfigurable digital logic circuitry inside the MEB FPGA allows the REXIS designer to implement custom digital logic cores, use ready-made Xilinx-supplied digital logic cores, and have options for FSW execution. The combination of FPGA cores and the compiled FSW form the REXIS FPGA bitstream. REXIS has a NOR[10] flash memory microchip which stores this bitstream. The FPGA uses a volatile memory known as Static Random Access Memory (SRAM) to store the bitstream data. SRAM is used since each of its memory cells is wired to configure part of the FPGA's digital logic resources. When REXIS is powered on, the MEB FPGA automatically loads this bitstream from the NOR flash into the FPGA's SRAM.

Digital logic cores are configurations of a FPGA's internal hardware that are used for providing certain functionalities like microcontrollers, GPIO control, clock generation, memory controller, etc. Similar to how FSW is implemented with programming language like C or Python, digital logic cores are implemented with Hardware Description Languages (HDLs). Compilers will synthesize multiple HDL files into the non-FSW component of a bitstream. REXIS uses the following two custom-designed digital logic cores for acquiring and processing science data:

1. **SXM Core** – The SXM core provides the interface between the FSW and SXM hardware by controlling the SXM hardware through FSW-based command and reporting the results back to the FSW. The SXM core also controls the SXM ADC and DACs. Therefore the SXM core

[10] NOR ("not OR") refers to a certain type of digital logic gate circuitry that forms the memory cells of the NOR flash memory microchip

reports the SXM housekeeping data and the readings of temperature sensors connected to the SXM ADC. The SXM core also commands the DACs for setting the HV level and SXM trigger threshold based on values set by the FSW. These DACs and ADCs are further described in section 3.3.1.7.

2. **Framegrabber** – the framegrabber core is used to acquire x-ray image data from the DE over a CameraLink interface and store this data in SDRAM. For computing bias maps or downlinking raw x-ray image data, this raw image acquisition functionality is sufficient. The framegrabber is also commanded by the FSW to perform the initial steps of REXIS image processing that are computationally intensive and do not require much knowledge of adjacent pixels. More specifically, the framegrabber performs the bias map subtraction, hot pixels correction, overclock correction, and event thresholding to generate a Candidate X-ray Events List (CXEL) that is also stored in the SDRAM. The FSW continues image processing by operating on the CXEL and the processed x-ray image stored in SDRAM. This process is detailed in section 3.2.5.2.

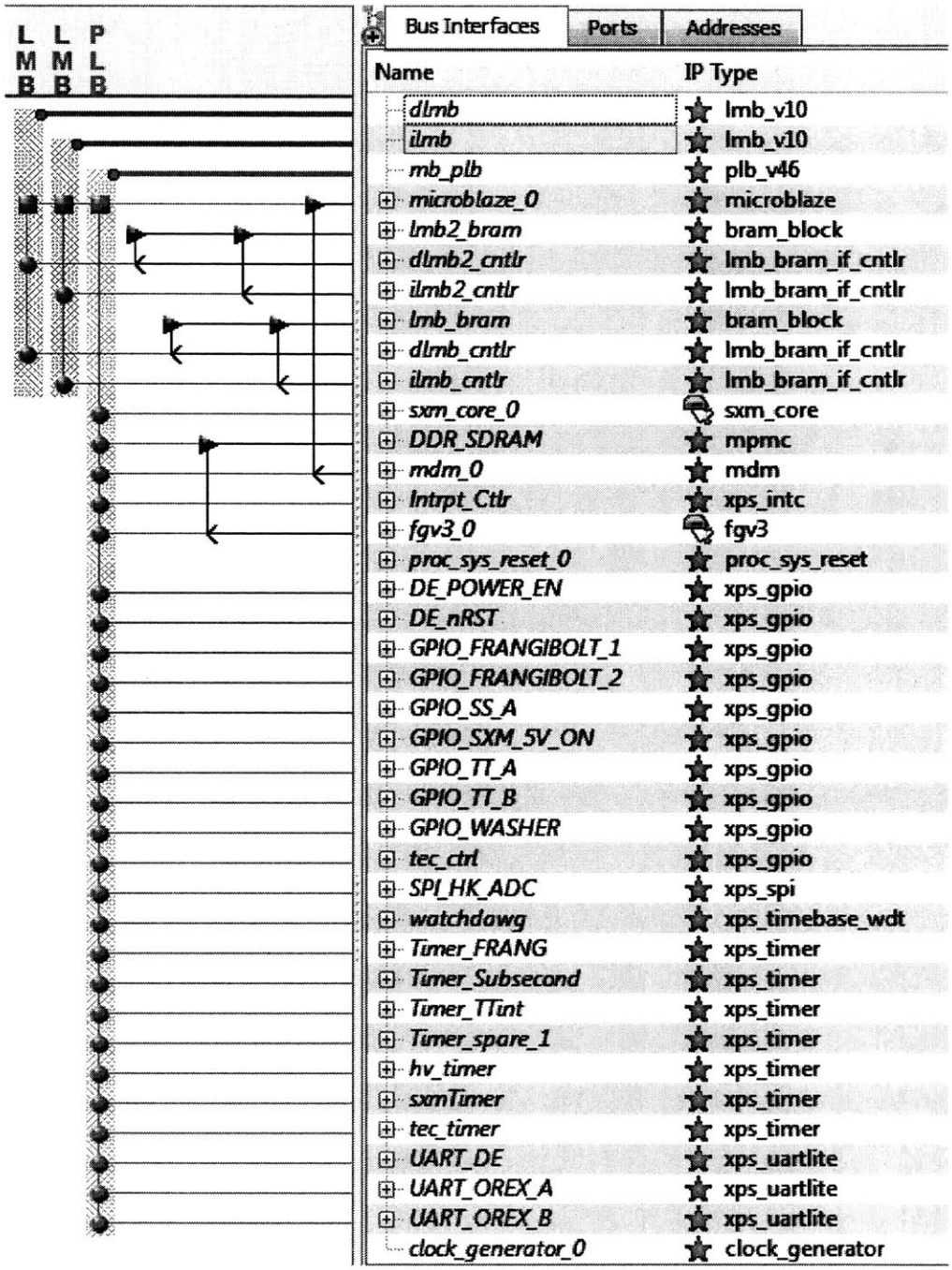

Figure 3-18: FPGA cores that are implemented on the MEB FPGA

These two custom FPGA cores are shown amongst all the Xilinx-supplied FPGA cores in Figure 3-18. The custom FPGA cores are the *sxm_core_0* and *fgv3_0* (framegrabber) that are marked with the non-green star in the "IP Type" column.

In addition to the two custom IP cores REXIS uses, there are a multitude of other FPGA cores that form the REXIS digital logic subsystem. These non-custom cores are designed, tested and supplied by

Xilinx. After configuring these cores for their particular application, they are ready to be integrated into the MEB FPGA. The left side of Figure 3-18 shows how all the custom and the COTS digital logic cores interact with each other. This interaction is made possible with the digital logic circuitry within the MEB FPGA configured as electronics designed to let FPGA cores share information with each other. These electronics are called busses.

The MEB has three busses. The two Local Memory Busses (LMB) connect the FPGA's internal BRAM memory to the MicroBlaze Processor. The LMBs are shown with two short blue columns on the left side of Figure 3-18 that depict the BRAM memory controller getting connected to the BRAM memory itself. The third bus is the general-purpose Processor Local Bus (PLB) which connects the Microblaze processor with all the FPGA cores. The yellow column on the left side of Figure 3-18 shows how the PLB enables data flow between all the FPGA cores and the Microblaze Processor (*microblaze_0*).

The most important digital logic core is the Microblaze processor since it controls all the MEB FPGA cores through the PLB and executes the REXIS FSW. The FSW calls special functions that command the Microblaze to appropriately use the other digital logic cores by sending digital signals through the PLB. The Microblaze is very similar to other microprocessors since it executes software code and performs computations. The key difference that sets the MicroBlaze apart is that it is completely implemented in the MEB FPGA with reconfigurable digital logic.

The MEB FPGA also has a Joint Test Action Group (JTAG) debugging port that can be physically seen as a small 14-pin connector on the edge of the MEB (connector J8 in Figure 3-4). This port enables new bitstreams and FSW to be loaded onto the MEB FPGA, FSW execution to be run line-by-line for debugging, and FPGA cores to be debugging through the ChipScope program. Thus the JTAG port was essential for REXIS MEB and FSW development.

The execution pacing of the FSW and the REXIS system timing is controlled with a rad-hard Vectron 1116R36M00000BF 36MHz crystal oscillator. The periodic signal from the crystal oscillator is

fed to the clock generator digital logic core that generates the 100MHz system clock, and the other specialized clocks used for the SDRAM.

3.3.1.2 NOR Flash ●

The SDRAM, MEB FPGA's BRAM, and the MEB FPGA's configuration SRAM memories are volatile. Since the FSW initializes the SDRAM and BRAM with fresh data upon power up, the volatility of these memories are acceptable. The bitstream data normally stored in the MEB FPGA's SRAM must be loaded each time during REXIS boot-up. This task is accomplished with the non-volatile UT8QNF8M8-60XEC NOR flash memory chip on the MEB. This rad-hard microchip maintains its internal bitstream data through power cycles and is rated for 10,000 write operations. The NOR Flash chip on the REXIS instrument has only been reprogrammed 19 times, giving the REXIS team confidence that this critical part will operate during spaceflight.

3.3.1.3 SDRAM ○●●

REXIS uses a 1-gigabit rad-hard 3D 1D1G16TS1267 MS Synchronous Dynamic Random Access Memory (SDRAM) microchip to hold large amounts of data. This large data capacity is required for scientific data processing and command/telemetry buffers.

The MEB FPGA has a SDRAM memory controller digital logic core supplied by Xilinx that controls the MEB's SDRAM chip. In addition to the standard connection of the SDRAM to the Microblaze-PLB, the framegrabber core has a direct connection to the SDRAM through the SDRAM memory controller. This is seen in Figure 3-18 with the purple arrow originating at the fgv3_0 framegrabber core and ending at the DDR_SDRAM multi-port memory controller (MPMC) core. MPMC means that the core is able to deliver data to and accept data from multiple sources. In the case of the MEB FPGA, these sources are the Microblaze Processor running the FSW and the framegrabber that stores images and performs image processing.

3.3.1.4 Spacecraft Interface Hardware ●●

The REXIS avionics system uses rad-hard RS422 microchips in order to receive commands from the spacecraft and send telemetry to the spacecraft. The HS9-26CLV32RH-Q receiver chip relays commands from the spacecraft to the MEB. More specifically, the HS9-26CLV32RH-Q receiver chip converts the double-ended RS422 signal from the spacecraft into a single ended signal that is sensed by a MEB FPGA GPIO pin. Meanwhile, the HS9-26CLV31RH-Q microchip does the opposite task of converting single ended telemetry signals from a MEB FPGA GPIO pin to a double ended signal suitable for the RS422 protocol the spacecraft uses. These transmit and receive microchips are essential for keeping the REXIS avionics system compatible with the RS422 specification for a seamless interface with the spacecraft.

Opto-couplers are used on the MEB to meet electrical isolation requirements imposed by the spacecraft. For example, an Intersil HCPL-6751 opto-coupler is used to electrically isolate REXIS electronics from OSIRIS-REx electronics for the time-tick and side select interfaces. Similarly, REXIS uses an SFMC28-461/00 EMI filter to interface with the spacecraft power bus. This EMI filter produces a ground designated as EMI_common derived from the spacecraft power system. The REXIS digital computation system maintains isolation with respect to this spacecraft-derived ground because of a spacecraft-imposed requirement for electrical isolation.

The MEB also has two 66171-300 optocoupler chips which maintain isolation between the FPGA's GPIO pins and the EMI_common side of the power supply circuitry, frangibolt circuitry, and SXM TEC circuitry. In summary, the 66171-300 opto-couplers enable the MEB FPGA to control circuitry that references REXIS primary power from the spacecraft and still maintain isolation between primary power and secondary FPGA power.

3.3.1.5 Frangibolt Circuitry ●●●○

The frangibolt circuitry on the MEB applies power to a frangibolt actuator and sense whether or not the frangibolt has actuated through the signal from a switch washer. This sensor/actuator pair is seen in detail on the right side of Figure 3-19 while their mechanical integration is shown on the left side. The

frangibolt housing, shown in green in Figure 3-19 houses this pair and is also shown in green Figure 1-7 as part of the entire REXIS instrument. When the FSW successfully processes the command to fire the frangibolt, it activates two general purpose IO (GPIO) pins on the FPGA which in turn, activate the two opto-couplers circled at the top of Figure 3-20. These opto-couplers are necessary to isolate the frangibolt circuitry that is powered from with respect to the EMI_common ground that needs to be kept isolated from the secondary power rails that the FPGA uses.

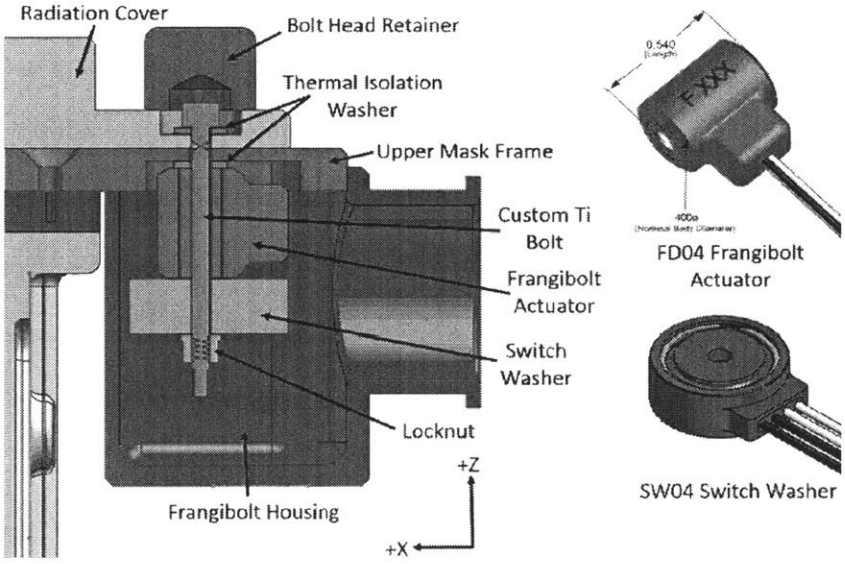

Figure 3-19: Frangibolt Actuator and Switch Washer Sensor [3]

The 66171-300 opto-couplers circled in red at the top of the Figure 3-20 are a redundant pair that relay the frangibolt firing signal from the FPGA GPIO pins to the DC/DC converter that actuates the frangibolt. The double opto-coupler setup gives the FSW two independent mechanisms of activating the frangibolt and increases the reliability of this system if there is a malfunction between the FSW and the frangibolt DC/DC converter while opening the radiation cover.

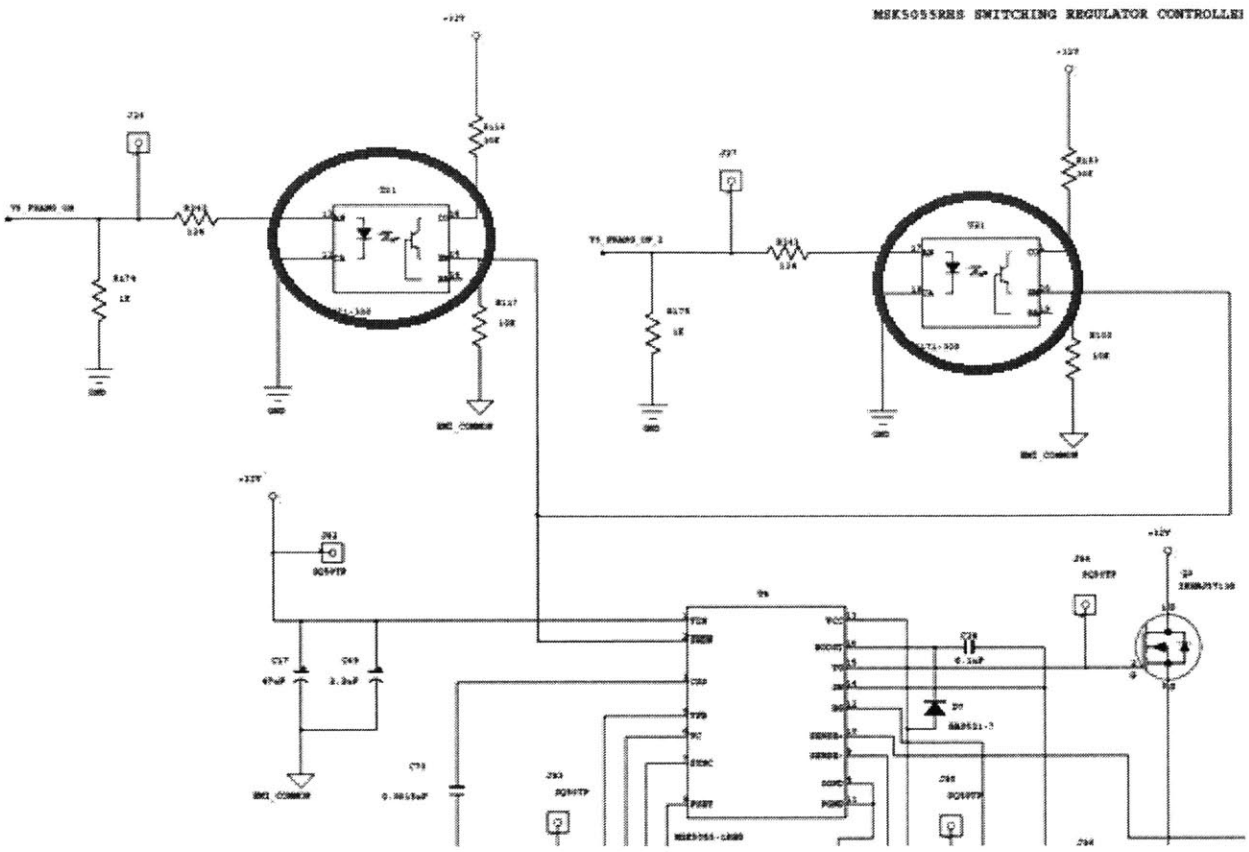

Figure 3-20: Opto-coupler Based Circuitry to enable the Frangibolt DC/DC Converter

Once the MSK5055-1RHG DC/DC converter is activated by one or both of the opto-couplers, it sends 20 watts of power to the frangibolt actuator. The MSK5055-1RHG DC/DC converter was chosen because it can convert the spacecraft-supplied 28V to the frangibolt-required 10V, it can handle the required current to actuate the frangibolt, and it is radiation hardened and suitable for the critical operation of opening the radiation cover. Rad-hard IRHNJ57130 transistors are wired to the frangibolt DC/DC converter in order to give it the capability to create and control the high current necessary for frangibolt actuation.

3.3.1.6 Analog to Digital Converters

The MEB uses two ADC128S102WGRQV rad-hard analog digital converters to sample housekeeping data and SXM pulses. This subsection will primarily discuss the housekeeping data acquisition ADC while the SXM data acquisition is performed by another ADC128S102WGRQV

described in detail in section 3.3.1.7. With the exception of the 2.5V line, all the voltage rails and an AD590 temperature sensor are buffered and measured by housekeeping data acquisition ADC.

Auxiliary circuitry is used to protect ADC128S102WGRQV ADCs from input voltages exceeding the device's capabilities and causing permanent damage. The ADCs are not rated for input voltages beyond their power supply and these ADCs measure voltages derived from higher voltage power rails that come up earlier than the 3.3V rail powering the ADCs. This power rail sequencing is shown in detail in Figure 3-8.

The ADCs have protection and buffer circuitry that prevent the ADC analog voltage input pins from seeing more than the operating limit of 3.3 volts. All analog input voltages are limited with diodes so they cannot exceed the 3.3V rail. Furthermore, LT2078IS8 op amps are used in circuits that buffer, reduce voltage, and invert the voltage avionics power supply rails. These rails, ranging from -12V to +24V, are converted into voltages between 0 and 3.3V so that they can be appropriately monitored by the ADC128S102WGRQV ADC without exceeding the ADC's operating limits.

3.3.1.7 SXM Circuitry ●●●○

The REXIS Solar X-ray Monitor (SXM) is supported on the MEB with circuitry that:

1. Provides sensor power
2. Biases the SXM Silicon Drift Detector (SDD) sensor
3. Sets the trigger threshold for x-ray event pulse detection
4. Performs signal conditioning on the SDD output voltage
5. Reads the SDD's x-ray event pulse voltages
6. Powers a thermo-electric cooler (TEC) built into the SDD

The design for the MEB's SXM circuitry is derived from the x-ray detector system from the Neutron star Interior Composition ExploreR (NICER) instrument. Because the SDD is a COTS sensor and the SXM is not the primary detector aboard REXIS, the bulk of the previously described SXM circuitry aboard the MEB is COTS as well [8].

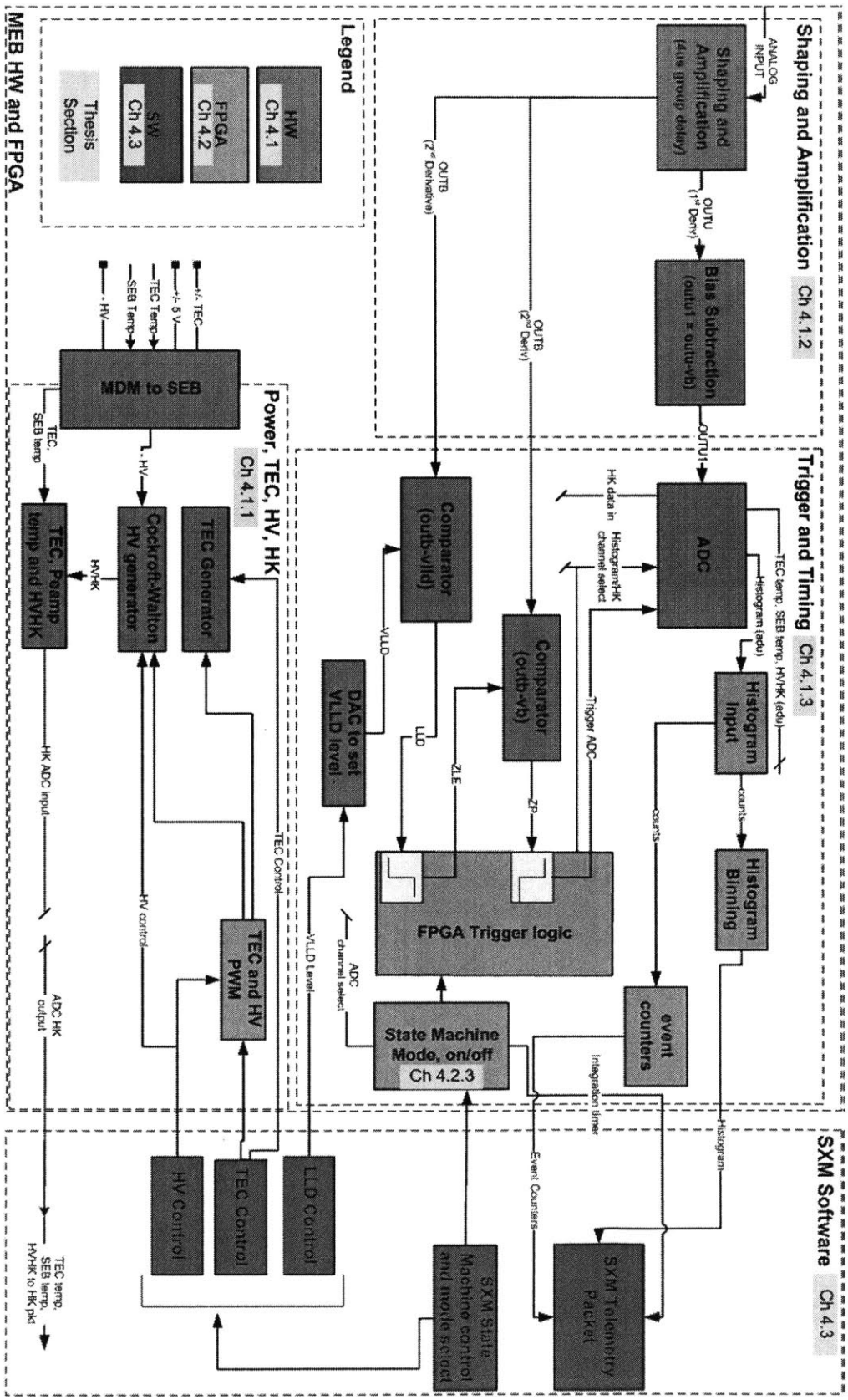

Figure 3-21: SXM Data Processing (Note: Chapter Numbers are for Mike Jones's Thesis [8])

Figure 3-21 above shows the entire SXM signal processing chain used to detect solar x-ray events. Part of this chain is implemented on the MEB with analog circuitry. First an analog low pass filter removes noise from the SXM signal. The MEB has a series of analog circuit components that are used to detect peaks which correspond to x-ray events in the filtered SXM signal. This peak is detected by finding the zero-voltage crossing of the second derivative of the SXM signal by using differentiation and comparator circuits. This zero-crossing corresponds to peak values in the SXM signal and its occurrence is fed to the FPGA through a GPIO pin. The FPGA samples the peak through an ADC128S102 ADC and thus measures the pulse height [8].

The SXM detector uses a variety of switched voltage rails for sensor biasing and powering. Micrel MIC94073YC6 high-side power switches are used to connect or disconnect the 5V rail to the MEB SXM circuitry. Two of these switches are wired in parallel on the 5V rail to provide redundant backup against radiation-caused failures. The SXM uses another voltage rail generated on the MEB that biases the SDD sensor with high voltage so that it is sensitive to x-rays. This high voltage rail is generated by the MEB's Cockroft-Walton voltage multiplier circuit that uses an FPGA-generated PWM signal to multiply the +24V rail to a maximum of -120V. The high voltage output used to bias the SDD is adjustable with an op-amp/transistor feedback circuit that reduces the voltage output. The set-point for this feedback circuit is created by one of the DAC121S101WGRLV Digital to Analog Converters (DACs) on the MEB.

The MEB has two DAC121S101WGRLV DACs that are both used for SXM operation. One DAC provides the set-point for regulating the high voltage rail while the other provides an adjustable trigger threshold used for the detection of voltage pulses caused by solar x-rays. This trigger threshold DAC is controlled through command. The functionality of these DACs was originally implemented with the COTS 2-channel AD5302ARMZ DAC on the EM. Rad-hard DAC121S101WGRLV DACs were used on the FM MEB since complex integrated circuits like DACs have smaller circuitry features compared to discrete electronic components, thus making them vulnerable to radiation [24].

In addition to the high voltage bias, the SXM's SDD needs to be cooled with a thermo-electric cooler (TEC). The MEB switches power to the SXM to power this TEC which cools the SDD to -30C [8]. The

SXM hardware has a separate PCB called the SXM Backpack Board (SBB). The SBB contains a switching DC/DC converter that converts 28V rail from the MEB into the 3.5V required for powering the TEC. The MEB simply switches the 28V rail on and off to the SBB. Originally the EM MEB had a TEC temperature feedback-controlled DC/DC converter that directly provided the correct voltage to the TEC for a given TEC temperature.

On the REXIS flight hardware, a 66171-300 opto-coupler was added between the FPGA GPIO pin that provided the switching component of this DC/DC converter. Like the frangibolt actuation system, this opto-coupler was added to meet the isolation requirements between primary and secondary power. The 66171-300 opto-coupler has a long response time which rendered the TEC DC/DC converter on the MEB inoperable. To fix this TEC power issue, the SBB was created with a COTS DC/DC converter that provided 3.5V to the TEC which keeps it cold enough for proper SXM operation [8].

The SXM subsystem aboard the MEB also uses ADCs for gathering TEC temperature telemetry and solar x-ray data. The TEC's temperature is monitored with a temperature-sensitive diode built into the SXM's SDD sensor. This diode is fed with a constant current from a MEB circuit while the temperature-dependent diode voltage is monitored by an ADC128S102WGRQV ADC that is discussed in detail in section 3.3.1.6. This 8-channel SXM ADC also converts the SDD's voltage pulses that are greater than the trigger threshold set by a DAC. The MEB FPGA monitors a comparator circuit that actives whenever the SDD voltage crosses the trigger threshold. When a crossing occurs, the MEB FPGA commands the SXM ADC to sample the peak of the SDD signal that corresponds to a solar x-ray event.

3.3.2 Interface Board

The interface board is in between the main electronics board (MEB) and video board in Figure 3-17 and connects these boards together electrically. The interface board uses the ±12V and +24V rails supplied from the MEB to generate CCD drive voltages. These voltages are relayed through the video board and flexprints to the CCDs. The video board is designed to convert analog CCD pixel data into

sixteen parallel streams of digital data for the Interface Board FPGA. The Interface Board FPGA is a radiation tolerant Actel A3P600-FG484 microchip and is used to accomplish the following:

1. Control the ADCs on the video board responsible for conversion of analog CCD data into a digital data-stream
2. Interpret a series of commands from the MEB used to specify CCD drive signal patterns. These commands are known as DE scripts and are sent over a RS232 serial port built into the CameraLink interface.
3. Using the information in DE scripts, the FPGA controls DACs on the interface board used to generate CCD drive signals. These DACs are not typical microchips but are instead implemented with a pulsed voltage that is converted to an analog voltage with a low-pass filter. More details about this approach are in section 4.4.1.
4. Send CCD pixel data to the MEB over the CameraLink interface
5. Upon command from the MEB over the CameraLink RS232 port, the FPGA will gather housekeeping voltages and temperatures and relay them to the MEB over CameraLink RS232 port. This housekeeping data collected by the Interface Board FPGA consists of various voltages and temperatures measured on the DE PCBs, flexprints, and CCDs. This DE housekeeping data is downlinked to Earth through the REXIS housekeeping telemetry.

Thus, the interface board enables the MEB to command the DE and receive pixel data from the DE in order to perform image processing. This command/data interface is only possible through the electrical connections between the three PCBs in the REXIS electronics-box. A set of 100-pin connectors (J10 and P10 in Figure 3-4) between the Interface Board and Video Board provides enough capacity to accommodate all the signals for CCD driving, ADC control, and CCD data for all 16 nodes. Meanwhile, a set of 30 pin connectors (J9 and P9 in Figure 3-4) between the MEB and Interface Board extends the MEB's voltage rails to the Interface Board and implements the physical connections for the CameraLink interface.

3.3.3 Video Board

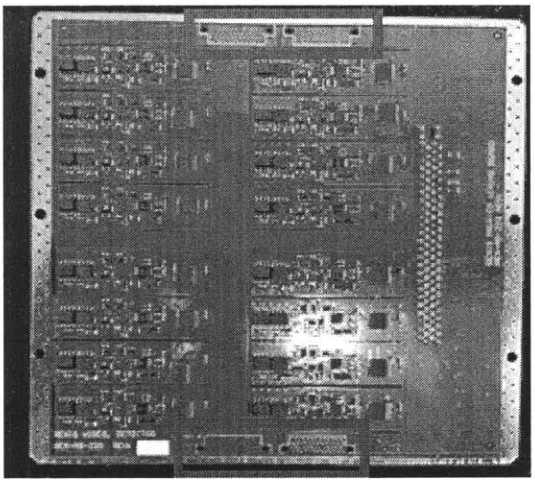

Figure 3-22: REXIS Video Board [28]

The video board is the top-most board in the electronics-box. The video board alone is shown in Figure 3-22 and it has the following functions:

1. Providing drive-voltages to the CCDs. High current drive signals are relayed from the Interface Board while low current drive signals are generated on-board the Video Board.
2. Buffering and amplifying analog CCD pixel data
3. Converting analog CCD pixel data into digital signals suitable for the interface board FPGA.

Since the four REXIS CCDs have a total of sixteen output signals, there are sixteen identical copies of CCD pixel processing circuitry that perform the functions listed above. These circuitry copies operate in parallel to send sixteen streams of digital data to the interface board below within the electronics-box. The video board has 4 100-pin Airborne connectors that are used to interface with the flexprints. These connectors are necessary to connect the video board to the CCDs through the flexprints and the pads for these connectors shown in red rectangles in Figure 3-22.

Chapter 4 - Radiation Tolerant Design of REXIS Avionics

The REXIS avionics system is designed to operate in the interplanetary OSIRIS-REx space-radiation environment. This chapter details the features of the REXIS avionics system that enable scientific data collection in this radiation environment. These design features are primarily hardware based since there was limited time and resources to develop and test the FSW and FPGA cores. This lack was partially caused by student-turnover and a small development staff that was imposed by the REXIS Class-D designation and overall REXIS objective to educate students with practical experience. These limitations prevented radiation hazard management techniques like triple modular redundancy (TMR), redundant FSW calculations, or autonomous FSW-based fault handling from being implemented.

First, this chapter describes the radiation environment that REXIS must operate in. Avionics design features that allow REXIS to operate in this environment are detailed next. Overall radiation-tolerance features are discussed first, and then features specific to each REXIS avionics hardware component. Table 4.1 gives an overview of the radiation tolerance features built into REXIS in the context of the radiation hazards and mitigation techniques described in Table 2.1. These radiation tolerance features are discussed in detail in the following sections.

Table 4.1: Summary of REXIS Radiation Tolerance Features

LEGEND

Long Term
Long and Short Term
Short Term
Section Number from Ch. 2

"X" indicates mitigation of a particular radiation hazard

		System-wide Design	Rad-hard Parts		Shielding	Latch-up Protection	EDAC	Redundancy
		2.3.1	2.3.2		2.3.3	2.3.4	2.3.5	2.3.6
SEU	2.2.1	X	X				X	X
SET	2.2.2	X	X				X	X
SEL	2.2.3	X	X			X		X
SEGR	2.2.4	X	X					X
TID	2.2.5	X	X		X			
TNID	2.2.6	X	X		X			
		4.2: REXIS Single String Setup	**4.2.2**: Rad-hard Components aboard REXIS	**4.3.5**: Frangibolt Drive circuitry	**4.2.1**: CCD, E-box and SXM shielding	**4.3.7**: SXM Current Limting Resistors		**4.3.5**: Redundant FSW Frangibolt Acutation
		4.3.1: Tolerance for SEE-caused FPGA interruption	**4.2.2**: Radiation Tolerant Passive Components	**4.3.6**: MEB ADCs				**4.3.7**: Redundant SXM 5V Power Switches
		4.4: Primary and Secondary Science Products	**4.3.1**: MEB FPGA and Crystal Oscillator	**4.3.7**: SXM DACs				**4.4**: Redundant nodes for asteroid characteriza-tion
			4.3.2: NOR Flash Memory Microchip	**4.3.8**: Power System Components				
			4.3.3: SDRAM Memory Microchip	**4.4.1**: DE FPGA, Crystal, and DACs				
			4.3.4: Spacecraft Interface Microchips	**4.4.1**: Video Board ADCs				

4.1 REXIS Radiation environment overview

OSIRIS-REx is designed to be launched onto an interplanetary trajectory to rendezvous with asteroid Bennu and return to Earth. Once in space, OSIRIS-REx will use its rocket thrusters and an Earth Gravity Assist (EGA) maneuver to fly to Bennu and away from the radiation hazards of Earth's Van Allen belts.

This trajectory, which is usually 93 million miles from the Sun and far away from Earth's Van Allen Belt radiation hazard, puts OSIRIS-REx in a relatively benign radiation environment when compared to other environments in the solar system like Jupiter orbits [17] [22]. Regardless, OSIRIS-REx does not have radiation protection from Earth's magnetic field, requiring REXIS to operate in a radiation environment more dangerous than Low Earth Orbit (LEO). If not properly designed for, the radiation hazard OSIRIS-REx faces can easily damage REXIS avionics components and interrupt REXIS operation.

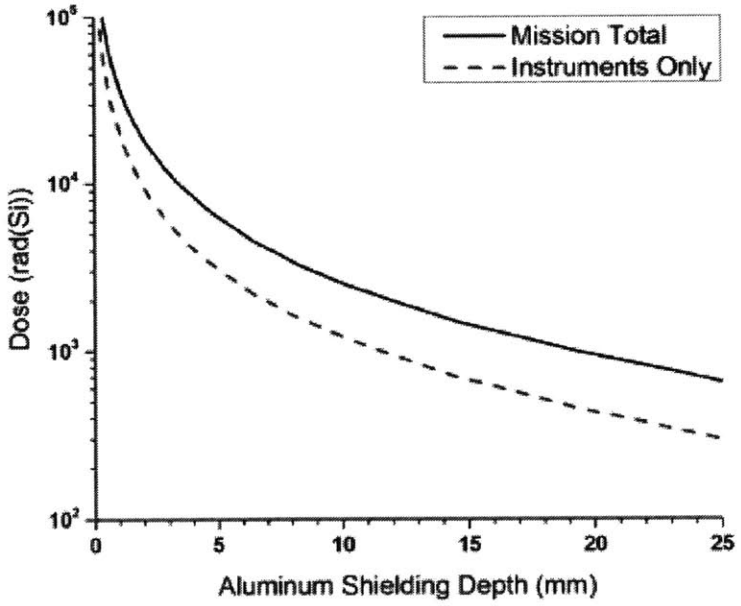

Figure 4-1: Aluminum dose-depth curve for the OSIRIS REx Mission. The dashed line is the instrument dose after 1,721 Days [11]

The initial conservative estimates for Total Ionizing Dose (TID) imparted to the instruments aboard OSIRIS-REx are shown in Figure 4-1. With 3mm wall thickness on the REXIS electronics box (electronics-box), the TID for the electronics within it is about 6 krad(Si). Space-grade rad-hard electronics are typically rated for 100 krad(Si) so the conservative estimate of a 6 krad(Si) dose for REXIS electronics is easily accommodated by these rad-hard electronics.

[11] OSIRIS-REx Project Radiation Hardness Assurance Plan by Ray Ladbury. Published in 2012 at GSFC in Greenbelt , MD

Table 4.2: REXIS Maximum TID [12]

Location	**Maximum Dose in krad(Si)**	**Duration for dosage accumulation**
SXM Sensor	2.8 – 6.16, depending on specific location on the SXM	Full Mission of 1730 days
SXM Electronics Board	1.85	Full Mission of 1730 days
Electronics-box PCBs	1.13	Full Mission of 1730 days
CCDs (Radiation Cover Closed)	1.39	1700 days
CCDs (Radiation Cover Open)	2.61	30 days

Furthermore, the results of a more detailed analysis of radiation doses experienced by REXIS components in Table 4.2 shows the maximum TID imparted to the REXIS electronics-box PCBs and SXM boards/sensors is about 1-2 krad(Si) [8]. The radiation doses in Figure 4-1 are derived from a numerical analysis program known as NOVICE. To calculate the radiation doses, the NOVICE program takes the following variables into account - spacecraft/instrument geometry, components' material composition, and the appropriate distributions of radiation fluxes and directions given OSIRIS-REx's position within the solar system. Considering that most COTS part can handle up to 5 krad (Si) of TID, the main radiation hazard for REXIS are single event effects (SEE) like SEUs, SELs, and SETs [24]. Quantifying this SEE hazard is difficult since SEE rate depends on the radiation environment, the geometry/composition of materials surrounding the device in question, and the material composition of the device itself [19]. Thus, determining the SEE occurrence rate requires expensive experimental testing in particle accelerators which is not feasible for the REXIS project [17]. Thus, REXIS is designed with the expectation that SEEs may occur in its avionics system.

[12] 3D-CAD RayTrace Results (without margin): OSIRIS-REx/REXIS2 Radiation Detector Doses by Craig Stauffer. Published in 2015 at GSFC in Greenbelt, MD

4.2 Design for Radiation Tolerance

The REXIS avionics system has specific design features that allow it to operate in the space radiation environment. These features can be grouped into two categories, first an overall shielding that protects the electronic components and second, an integration of radiation tolerant features into the avionics system on a part-by-part basis. It is also important to note that the REXIS avionics system has a single-string setup, meaning that at any given time there is only one copy available of all the avionics hardware, software and FPGA cores. Thus, in the absence of redundancy, it is critical that the avionics are protected from radiation damage with a robust design. The next sections describe different radiation protection mechanisms used on REXIS

4.2.1 Shielding

REXIS uses shielding to reduce TID-caused damage since TID continuously degrades and damages electronic components. REXIS has aluminum structures that shield the SXM electronics, CCDs, and electronics-box electronics. Figure 4-1 shows how TID experienced by OSIRIS-REx spacecraft components is reduced as aluminum shielding thickness is increased for the same OSIRIS-REx mission duration. The importance of shielding can be seen in Table 4.2 which shows increased radiation dose-rate (TID per day) when the REXIS radiation cover stops shielding the CCDs. More specifically, the CCDs receive only 1.39 krad(Si) of TID over 1700 days and once the cover opens, the TID on the now-exposed CCDs increases by another 2.61 krad(Si) in just 30 days. Too much shielding is less effective since there is an increase in the levels of secondary radiation created by the interaction between high energy space radiation and the shielding mass. [24]. This decrease in shielding effectiveness is depicted in Figure 4.1 as a lack of change in TID levels when shielding thickness is increased. Thus, the REXIS electronics-box is retained at 1/8" thickness to limit the TID experienced by PCBs within it to the 1.13 krad(Si) levels shown in Table 4.2 [10].

These shielding mechanisms primarily protect REXIS against long-term damage from radiation. However, rates of short term single event effects (SEEs) are not reduced since SEEs are caused predominantly by high-energy particles that are not absorbed by shielding. Thus, the REXIS avionics system must implement other precautions and design techniques to prevent SEEs from affecting the avionics system's ability to meet REXIS mission requirements. These techniques are detailed in the following section.

4.2.2 Avionics Component Selection and Design

A majority of critical functionality within the REXIS avionics system, is implemented with rad-hard electronics designed to withstand the OSIRIS-REx radiation environment - both short and long term hazards in the form of SEEs and TID/TNID respectively. An example of a critical REXIS functionality is the acquisition and downlinking of scientific x-ray data from the asteroid regolith. Using the straightforward approach would mean that all the electronics within REXIS would be rad-hard for critical functionality. However, using a 100% rad-hard design for REXIS is not feasible because rad-hard parts are expensive, have long lead times, and are sometimes difficult to integrate into a non rad-hard design consisting of the latest COTS parts.

To avoid these issues of a 100% rad-hard design, the REXIS avionics system uses COTS parts connected and configured in a radiation-tolerant manner as detailed in the rest of this chapter. Some of the key advantages of using COTS are it saves time and resources for testing component design and reduces risk of any malfunction by implementing an already-working design. However, this approach may not be always applicable because there may not exist a parallel/direct rad-hard replacement for a COTS parts. The COTS approach is applicable to REXIS since it was never conceived as a 100% rad-hard design – instead the primary objectives are to impart avionics design experience to students and utilize robust techniques, which may include rad-hard parts, that does not damage the spacecraft.

Typically the cost of rad-hard parts is in the order of 2-3 magnitude more than their COTS-equivalent parts. This is further clarified with the following example from the REXIS project. The

MSK5055-1RHG DC/DC converter cost $1569.00[13] while the functionally equivalent COTS part, the LT3845 costs only $5.00 from Arrow Electronics[14]. The relatively high cost of procuring rad-hard parts is attributed to the following:

1. Low production volume makes it difficult to amortize the fixed cost of production over several unit thus reducing the availability of large stocks of parts for immediate shipment.
2. Extra design, testing, and qualification is required for marketing rad-hard parts. Additionally they need certification to endure specific space radiation environment.
3. Rad-hard components need to be physically large to accommodate transistor-level design features which make electronics radiation resistant. However, this increase in size drives up the expense as costly production techniques are used to produce these bigger chips.

Similarly long lead time was another limiting factor for the project. For example the rad-hard version of DAC121S101 DAC has a lead time of 32 days[15] while the COTS version from DigiKey has a lead time of only one day[16]. These long lead times constrained the early design efforts of the REXIS development team and made it difficult to implement any modification to the avionics design late in the design process.

In conjunction with the high cost and long lead time, the reduced capability of rad-hard parts make them difficult to integrate into COTS-based avionics designs. This difficulty was frequently experienced in avionics development of the SXM and DE because these components started off as pure COTS designs. Starting off with proven COTS designs reduced the overall cost and cut down development and testing time. Furthermore the failure risk was lowered as these designs were already developed, tested, and given to the REXIS team as a working baseline that could be tweaked for REXIS-specific requirements instead of creating a new design from the ground-up. Furthermore, since REXIS is a Class-

[13] Quote for MSKennedy 5055RH HRH KRH supplied to REXIS project in 2013 from MSKennedy

[14] Arrow Electronics Webpage for LT3845IFE#PBF. Accessed March 15, 2016 at https://www.arrow.com/en/products/lt3845ifepbf/linear-technology

[15] Quote for DAC121S101WGRLV supplied to REXIS project in 2014 from Avnet

[16] Digikey Electronics Webpage for DAC121S101CIMK. Accessed March 15, 2016 at http://www.digikey.com/product-detail/en/texas-instruments/DAC121S101CIMK%2FNOPB/DAC121S101CIMK%2FNOPBCT-ND/953477

D mission with no directive to use a 100% rad-hard design, relying on COTS designs to provide student development experience was an acceptable approach.

For instance, a rad-hard op-amp could require more PCB space and have inferior operating parameters when compared to its COTS equivalent part. Thus, integrating this rad-hard part into an avionics design using COTS-equivalent part would be difficult as it would require a substantial change of PCB design and layout for the rad-hard part. To overcome this difficulty in the initial development phase, the REXIS avionics development team used prototype rad-hard components while designing circuitry from scratch. Prototype components are physically identical to their rad-hard counterparts but do not have the rigorous testing and quality control that certify them for spaceflight. Such parts are still suitable for Earth-based testing and development. Thus, the REXIS engineering model (EM) avionics utilizes prototype-grade hardware while the flight model (FM) avionics which is integrated onto OSIRIS-REx use rad-hard spaceflight-grade hardware.

Rad-hard electronic components are used for most critical functionality aboard REXIS to ensure that this functionality is executed even with the possibility of interruption from SEEs and hardware degradation caused by TID/TNID. The circuitry that implements this functionality have low part counts so the REXIS project could afford to use rad-hard parts. All the rad-hard components aboard REXIS as shown in Table 4.2 are active semiconductor electronics components such as MOSFET transistors and integrated circuit microchips which are collections of interconnected transistors. This hardware is most vulnerable to radiation-caused malfunctions [29].

Table 4.3: Rad-hard Parts aboard REXIS

Functionality	**Parts used**	**Section Discussed**
Regulating spacecraft power for use aboard REXIS	• SMHF2805S/KR – 5V output DC/DC converter • SLH2812D/KR – 12V output DC/DC converter • ISL70001SRH – 1.0 and 2.5V output DC/DC converter • ISL75051SRH – 3.3V output LDO linear regulator • RH137H – negative 5V output LDO linear regulator	4.3.8
Isolating the spacecraft and REXIS power systems	• 66171-300 space-grade opto-couplers	4.3.8
Driving the frangibolt with the appropriate voltage and current	• MSK5055-1RHG – 10V output DC/DC converter • IRHNJ7130 – Rad-hard transistor	4.3.5
Buffering, Transmitting and Receiving RS422 signal to/from the spacecraft	• HS9-26CLV31RH-Q – RS422 Driver • HS9-26CLV32RH-Q – RS422 Receiver	4.3.4
Electrical isolation between the spacecraft and REXIS power system	• HCPL-6751 4-channel opto-coupler	4.3.4
Engineering diagnostic telemetry and SXM data acquisition	• ADC128S102WGRQV Analog to Digital Converter	4.3.6
Setting trigger voltage thresholds and high voltage bias for the SXM	• DAC121S101WGRLV Digital to Analog Converter	4.3.7
Time-keeping	• 1116R36M00000BF 36MHz MEB crystal oscillator • 1116R24M00000BF 24MHz DE crystal oscillator	4.3.1, 4.4.1
Command, telemetry, and x-ray detector processing/control	• XQ5VFX130T-1EF1738I FPGA on MEB • RT3PE600L-1CG484B FPGA on DE	4.3.1, 4.4.1
Storage of MEB FPGA bitstream	• UT8QNF8M8-60XEC 64Mbit NOR flash	4.3.2
Storage of intermediate data	• 3D 1D1G16TS1267 MS 1Gigabit SDRAM	4.3.3
Filtering out electromagnetic transients to and from the spacecraft	• SFMC28-461/KH EMI filter	4.3.8

Certain functionality aboard the REXIS avionics system cannot be implemented with rad-hard components due to the previously discussed costs and issues with using rad-hard parts. For these

functionality, either other approaches are taken to ensure resistance to radiation or the REXIS system as a whole is designed to withstand the temporary losses of that functionality. Implementation details of functionality executed without rad-hard parts is detailed below.

An overall example of where COTS parts were used instead of space-grade parts are the passive electronic components of the REXIS avionics circuitry. The lead-times and total cost for these space-qualified parts were unacceptable and forced the REXIS development team to look at alternatives. The REXIS FM used automotive grade (AEC-Q200 specification) passive components like resistors and capacitors. These components have sufficient temperature rating and quality control suitable for the REXIS project. Since these components are not radiation-vulnerable semiconductors, it is safe to assume that they are radiation tolerant up to 30 krad(Si) [24]. AEC-Q200 parts are a subset of COTS parts since they are tested to more rigorous standards than typical COTS parts.

Spaceflight missions typically use space-qualified passive components that are certified at levels beyond the AEC-Q200 standard. It is important to realize that AEC-Q200 has "no requirements for periodic qualification verification" [30]. Put in other words, only the initial production of an AEC-Q200 grade part is tested to meet the AEC-Q200 standard and parts purchased later may not undergo such a stringent level of testing but will still have the same design and production method. However, AEC-Q200 electronics are much more reliable than their pure-COTS counterparts. In general, the radiation-caused failure of an active electronic device that requires power is much more likely than the failure of an AEC-Q200 passive component. Therefore, the general low risk of these automotive-grade passive electronics failure was mitigated for REXIS through derating components and realistic system level testing (vibration, thermal-vacuum, and continuous run-time) that would have revealed any defects.

The next subsections present the avionics hardware components of REXIS in the same order of section 3.3 but details the design features that are implemented to enable REXIS avionics to operate in the space radiation environment. The REXIS avionics design originally planned on having fault detection and recovery features but later these were omitted due to the limited development time. This thesis focuses on

the features of the MEB and DE that are used for radiation tolerance. Radiation tolerance for the SXM sensor is further detailed in the "Radiation Concerns" section 3.4 of Mike Jones's Thesis [8].

4.3 MEB Design for Radiation

4.3.1 Xilinx Virtex5 FPGA

The Xilinx XQR5VFX130 (Virtex-5QV) FPGA was selected for command and data handling [12]. FPGAs have reconfigurable digital computation hardware built into them that can be used for command, control, and telemetry functions of REXIS. This space-grade Xilinx FPGA can handle up to 1 Mrad(Si) of TID and has been used on NASA spacecraft like the Mars Exploration Rovers [31]. After further analysis and recommendation from NASA Goddard Space Flight Center (GSFC), a Xilinx XQ5VFX130T-1EF1738I industrial grade FPGA was selected for use aboard the REXIS FM and this decision saved the REXIS team about $100k over two units. This device has 100 krad(Si) of TID tolerance and GSFC testing showed that the device was immune to latch-up [32]. The specifications of the industrial grade FPGA are more than sufficient for the REXIS mission while the space-grade part was overkill. However, the industrial part is still vulnerable to SEUs and SETs. The effects of SEUs and SETs can vary from corrupt data in unused memory to a more severe system reboot. But these effects are usually transient and do not jeopardize the overall REXIS mission objectives. The industrial FPGA's 100krad(Si) of TID tolerance is identical to the tolerance level of other rad-hard parts used on REXIS and many times more than the projected radiation dose of the REXIS mission [33].

The MEB FPGA is connected to a Vectron 1116R36M00000BF 36MHz rad-hard crystal oscillator that is used for time keeping. This crystal oscillator provides the following critical timekeeping functionality:

1. Timestamping the telemetry generated by the FSW running in the FPGA
2. Properly pacing FSW execution and the transitions of the state machines in the FPGA cores.
3. Providing clock signals that are used to interpret digital data.

Changes from the EM to FM MEB design were required to accommodate this crystal. The MEB FPGA has a clock generator core that transforms the crystal oscillator's signal into several different clock signals for use aboard the MEB. The COTS MEB crystal oscillator in the EM design has a 125MHz output frequency. In the FM design, a rad-hard Vectron crystal with 100MHz frequency was used to accommodate the critical nature of the crystal's functionality. The MEB clock generator core had to be reconfigured to accommodate this new clock speed. The flexibility of the Xilinx clock generator in the MEB FPGA allowed the REXIS design to adapt to the new crystal oscillator without any issues. Furthermore, the crystal-specific PCB layout was changed since the rad-hard part is much bigger than the original COTS part.

The FPGA bitstream in the MEB also required debugging and modification to accommodate the new crystal. If the EM's COTS crystal oscillators were identified earlier as vulnerable to radiation, then the lead time, cost issues, and development/debugging encountered while procuring rad-hard Vectron crystal oscillators at the clock frequencies of the EM COTS parts could have been avoided. Instead, the REXIS team decided to use surplus Vectron rad-hard crystal oscillators available from GSFC electronics surplus on short-notice.

4.3.2 NOR Flash

The NOR flash memory chip aboard the REXIS MEB is used to store FPGA bitstream data. The MEB FPGA reads this bitstream data on startup to configure its internal digital logic components. Once this configuration is implemented, the FPGA cores, their interconnections, and FSW are ready to implement REXIS avionics functionality. The NOR flash operates at the start of this critical process that leads to a functioning avionics system. Furthermore, it is only one microchip so a rad-hard Aeroflex UT8QNF8M8-60XEC 64Mbit NOR flash memory chip is used.

Within the REXIS radiation environment, the NOR flash is extremely resilient to radiation. The NOR flash has a TID tolerance of 50 krad(Si) which is many times more than the conservative REXIS radiation dose estimates in Table 4.2. Even though the NOR flash is resistant to SEE malfunctions, it only

operates for a few seconds each time REXIS is turned on. Depending on the exact OSIRIS-REx mission plan, REXIS is switched on around 10-20 times during the entire mission. Since the NOR flash operates for a short duration compared to the entire REXIS mission, and SEEs only affect operational electronics, the NOR flash aboard REXIS is extremely resilient to SEEs.

4.3.3 SDRAM

REXIS has a Synchronous Dynamic Random Access Memory (SDRAM) microchip that is used by the FSW and framegrabber FPGA core to store intermediate data that results from command/telemetry processing, image processing, and SXM data processing. The storage of these intermediate data products is critical to successfully implementing REXIS functionality of acquiring and downlinking X-ray science data so this memory is a rad-hard 3Dplus 1D1G16TS1267MS 1Gigabit SDRAM chip.

4.3.4 Spacecraft Interface Hardware

The spacecraft interface hardware consists of transmitter/receiver microchips and opto-couplers. The transmitter/receiver microchips relay the differential voltage pulses between REXIS and the spacecraft in order to implement the RS422 digital serial communication protocol. Meanwhile the opto-couplers electrically isolate and buffer the spacecraft avionics' voltages for time tick and side select from the GPIO pins on the MEB FPGA. If any of these microchips fail, REXIS will not communicate properly with the spacecraft and the important scientific telemetry generated by REXIS will not be relayed to Earth through the spacecraft's communication system. These three microchips implement critical functionality and have low parts counts so rad-hard components are used. The RS422 serial port driver that relays telemetry from REXIS to the spacecraft is an Intersil HS9-26CLV31RH-Q microchip while the opposite command relaying functionality is an Intersil HS9-26CLV32RH-Q RS422 Receiver microchip. The REXIS/spacecraft GPIO isolation requirement is implemented with an Intersil HCPL-6751 4-channel opto-coupler.

These microchips have unused channels on them, meaning that there is unused capability aboard the MEB, that incurs unnecessary cost. However, rad-hard hardware with an appropriate number of channels is not available. The designer for a typical COTS non-spaceflight project has more options for microchips that can be used. Thus, a COTS design would usually have fewer unused ports and capabilities and are better designs from a pure electrical engineering point of view. Anywhere from a few cents to a few dollars could have been saved per part in the COTS world and depending on production volume, these savings can be significant. Since REXIS avionics consists entirely of one-off boards, it is not an issue.

4.3.5 Frangibolt Drive Circuitry

The REXIS radiation cover forms an important part of the radiation shielding for the CCD x-ray sensors detailed in section 4.2.1. Once REXIS is within the vicinity of Bennu, the avionics system opens the radiation cover by applying current to a frangibolt actuator. The avionics system has a DC/DC voltage converter that regulates spacecraft-supplied 28 volts to the 10 volts required to actuate the frangibolt. This DC/DC converter, and its associated components are rad-hard because they drive the critical frangibolt aboard REXIS. The frangibolt is critical since there would be serious consequences for improper actuation. If the frangibolt fails to actuate, then the radiation cover does not open, and the CCDs cannot collect scientific x-ray data. Furthermore, if current is applied to the frangibolt actuator for too long, then the actuator can outgas and contaminate the OSIRIS-REx sample return capsule, and cause a major problem for the OSIRIS-REx mission. However, by using rad-hard circuitry for the frangibolt system, this contamination hazard is prevented.

The frangibolt DC/DC converter is centered around the MSK5055-1RHG DC/DC buck converter. This microchip has no built-in capabilities to handle the high currents required to drive the frangibolt so two rad-hard IRHNJ7130 power transistors are connected to the MSK5055-1RHG to provide this high-current capability. Since a buck DC/DC converter circuit is used in the frangibolt drive system, an inductor is required for energy storage. Thus, Coilcraft ML558PTA222MLZ 2.2uH spaceflight-grade

inductors were used for this purpose since they were easily acquired from GSFC surplus or directly from the Coilcraft student-outreach program. If this typically expensive and long-lead-time part was not easily available from GSFC and Coilcraft, then an alternate automotive-grade part would be used. The remaining components of the frangibolt-drive circuitry are automotive-grade AEC-Q200 passive components that were previously detailed in Section 4.2.2.

The frangibolt system has design features to prevent SEE-caused failures for both hardware, FPGA, and software components. On the hardware side, these failures are prevented with the rad-hard components that form the frangibolt DC/DC converter. On the FSW and FPGA-core side, the following safeguards were implemented:

1. The default duration for firing the frangibolt is zero seconds. This number is adjusted through command prior to the actual firing.
2. There is a specific arm/fire command sequence required to actuate the frangibolt.
3. The spacecraft will shut down REXIS before it draws too much power to unwantedly actuate the frangibolt.

These safeguards are further detailed in Section 3.2.4 and they are responsible for preventing any SEE-induced corruption of the FSW execution or FPGA GPIO core from causing an unwanted frangibolt actuation.

4.3.6 Analog to Digital Converters

REXIS uses two 8-channel Analog to Digital Converters (ADCs) for gathering housekeeping temperature/voltage data and sampling the voltage of SXM x-ray pulses. This housekeeping and SXM data is supplied to the FSW and SXM FPGA core for further processing and is vital for monitoring REXIS and interpreting the asteroid x-ray data. By themselves, these capabilities are not necessary for acquiring scientific data from Bennu but given the fact that only two ADCs are needed to implement these capabilities and housekeeping data is critical to operating REXIS, rad-hard parts were used. The

MEB has two Texas Instruments rad-hard ADC128S102WGRQV ADCs that carry out these measurements.

4.3.7 SXM Circuitry

The Solar X-ray Monitor (SXM) is the auxiliary x-ray detector used to obtain solar x-ray spectra and is supported by circuitry aboard the MEB. The SXM transmits a time-varying signal consisting of x-ray voltage pulses. Circuitry on the MEB detects and measures these pulses through commands from the SXM core and FSW. The SXM is necessary for REXIS to produce the highest quality scientific data. However, if the SXM fails then a fraction of this scientific data can still be generated. Essentially, a fully functional SXM is critical for generating high quality scientific data but these science objectives are still achievable even if the SXM fails to operate. The difference would be in the overall quality of REXIS data. Thus, the functional requirements for SXM components are relaxed, which allowed the REXIS team to use COTS components and designs for the MEB SXM circuitry instead of rad-hard parts. However, the MEB SXM circuitry has upgrades that increases its tolerance to radiation. These upgrades were implemented whenever the REXIS budget and schedule allowed and are further discussed in this section.

The SXM uses an Amptek COTS SDD-based design borrowed from the Neutron star Interior Composition Explorer (NICER) project [8]. Since the SXM detector is a COTS part that is operated with a COTS circuit, the decision to use all COTS electronics that support the SXM on the MEB was made early in the REXIS project [8]. More specifically:

1. The SXM is not the primary sensor in the REXIS instrument. The initial REXIS designs did not feature any SXM at all. Project resources were spent on making the primary REXIS sensor, the CCDs, and other critical functionality robust to radiation.
2. The NICER circuit design already produces an x-ray spectrum with COTS parts. It features current limiting resistors that deal with radiation caused latch-up.
3. The NICER circuit design was already tested to 0.6 krad(Si) TID and still functioned with reduced resolution and no catastrophic damage [8]. The SXM design focused on reducing the

TID experienced by the sensors and electronics to one below this level through aluminum shielding [8].

The REXIS avionics switches 5-volt power onto the SXM while transitioning to science mode using two Micrel MIC94073YC6 high-side switches. Two of them are wired in parallel to ensure the SXM gets voltage in science mode. Each has a 1k ohm resistor that limits latch-up current to 5mA. This current level is an order of magnitude lower than the absolute maximum currents in the MIC94073YC6 datasheet. This switch design could be improved by putting this hardware through TID testing but since the REXIS mission has a low TID (see section 4.1 for more details), this testing was not a priority. TID testing would have either increased confidence in this redundant-switch design or signaled the need to redesign it. This redundancy ensures that power is switched on appropriately so even if one of these COTS devices fail from SEEs or TID accumulation, the SXM will still receive power.

The SXM requires two analog voltages that are controlled by FSW. These analog voltages are used by the MEB SXM circuitry to derive the high voltage bias for the SXM's SDD sensor and the threshold voltage that SXM pulses are compared against to detect solar x-ray events of scientific interest. The MEB design uses Digital to Analog Converter (DAC) microchips to generate these voltages. These SXM DACs are controlled by the FSW through the SXM FPGA core.

The EM avionics design uses a two channel COTS DAC to create these voltages. However, for the FM design, two single-channel rad-hard Texas Instruments DAC121S101WGRLV DACs were used since complex semiconductors like DACs are more radiation vulnerable [29]. These rad-hard DACs were used since they were available with sufficiently short lead-times to meet the FM PCB manufacturing schedule and the overall cost was affordable. However, the integration of these DACs was not completely seamless since there was an undesired expenditure of development time to make the SXM FPGA core compatible with these DACs.

Resistors are essential to prevent latch-up from damaging the microchips that form the MEB SXM circuitry. These resistors are used as current limiting resistors on the power supply pins of the integrated

circuits. The resistors limit the current draw through the integrated circuit to the maximum permissible current that prevents damage [17]. This technique is only effective on components that draw low current since high current components would either shut down from an unacceptable voltage drop over the resistor or waste significant power across the resistor. SXM hardware with low current draws are protected with current limiting resistor while the reminder of SXM hardware is rad-hard.

4.3.8 Power System

The REXIS power distribution system is designed to convert unregulated voltage from the OSIRIS-REx spacecraft into various voltage rails that all the REXIS avionics components use as their electrical power supply. The power distribution functionality is absolutely critical to the REXIS system so it consists entirely of rad-hard parts. A list of these rad-hard components, the voltage rails they generate, and the other REXIS avionics components that utilize these rails can be found in Table 3.2..

In addition to these rad-hard power converters, REXIS uses a rad-hard SFMC28-461/KH EMI filter to filter out electromagnetic transients between the spacecraft and REXIS's electrical power system. The EMI filter makes sure any transient signals or ripple from the REXIS avionics power system are not conducted into the spacecraft and vice versa. Because this component is in series with the entire REXIS avionics power system, it is also rad-hard. If this EMI filter fails due to radiation, then the spacecraft electrical system could have undesired transient voltages. This critical nature also requires the EMI filter to be rad-hard.

The voltages of the REXIS power system are referenced from the isolated ground created by the DC/DC converters of the REXIS power system. However, the MEB FPGA, which is also referenced to this isolated ground, needs to control components on the unregulated side of the power system that reference the ground provided by the spacecraft. These components are part of the SXM thermo-electric cooler, frangibolt systems, and enable pins for the power system's DC/DC converters. Since the majority of these systems are critical, and ground isolation is an OSIRIS-REx-imposed requirement, rad-hard 66171-300 opto-couplers are used in these interfaces. Not only are these opto-couplers electrical resilient

to radiation-caused damage, the optical medium within these devices does not degrade from radiation exposure.

4.4 DE Design for Radiation

The Interface Board and Video Board PCBs are known collectively as the Detector Electronics (DE). These PCBs are used to drive and collect data from the CCDs. The REXIS CCDs consist of sixteen nodes. The Video Board's readout circuitry amplifies data from each of these sixteen nodes and converts the amplified analog data to digital data with sixteen AD7984 ADCs (detailed in subsection 4.4.2). These sixteen streams of digital data from the AD7984s are read in parallel by the Interface Board's FPGA.

Nominally, with all sixteen nodes functioning, 72 hours of data from REXIS would be used to classify Bennu and meet the high level REXIS objectives described in section 1.3.1. However, REXIS is scheduled to observe Bennu for 480 hours (16 hours over 30 days). The difference between 480 and 72 is a 667% margin that enables the instrument to handle the failure of nodes, either due to radiation or other issues like mishandling, vibration, manufacturing defects, etc. In short, the nodes provide redundancy to the primary REXIS objective of generating scientific telemetry used for globally characterizing Bennu since each node can generate asteroid x-ray spectra. However, the loss of nodes restricts REXIS from acquiring data needed to produce collimator or imaging mode science products which indicate surface concentrations of elements on Bennu's surface (further detailed in section 1.3.1). However, these other imaging techniques are not necessary for REXIS primary mission success.

The following subsections describe the component-specific design features used to mitigate the radiation risk on the two PCBs that comprise the DE – the Video Board and the Interface board. These boards are detailed at a functional and physical level in sections 3.3.3 and 3.3.2 respectively.

4.4.1 Interface Board

The DE Interface Board's main component is the Actel RT3PE600L-1CG484B FPGA. This device controls CCD drive voltage generation, acquires DE housekeeping data, and sends the digital pixel data

from the Video Board's sixteen nodes to the MEB FPGA through a CameraLink connection. This Actel FPGA is resistant to up to 15 krad(Si) of TID but does not have any provisions to handle SEE transient effects. Like the MEB FPGA detailed in Section 4.3.1, the occurrence of SEE within the Interface Board's FPGA would at worst cause a small fraction of the downlinked data to become corrupted and a full REXIS avionics system reset in space. Or in short, no permanent damage to REXIS would occur and the avionics system requirements can continue to be met. On the other hand, based on the conservative estimates of TID in Table 4.2, 15 krad(Si) of TID tolerance of this Actel FPGA is sufficient to survive OSIRIS-REx's cruise to Bennu and collect x-ray data from this asteroid.

The finite state machines implemented within the FPGA cores of the Interface Board's FPGA need reliable timing signals for proper execution. This signal is provided by a Vectron 1116R24M00000BF 24MHz crystal oscillator. This Vectron part is rad-hard since it provides the critical signal that allows the Interface Board FPGA to operate correctly. Originally, this crystal oscillator was a COTS 25MHz part for the EM Interface board. The one MHz difference in clock speeds between the EM and FM designs caused the CameraLink serial port to operate slower and out of the CameraLink spec. As a result, time had to be spent debugging and isolating this problem and eventually the serial port FPGA core in the Interface Board FPGA had to be reconfigured to accommodate the new rad-hard crystal oscillator for the FM design.

If the EM's COTS crystal oscillators were identified earlier as vulnerable to radiation, then the lead time and cost issues surrounding procuring rad-hard Vectron crystal oscillators at the clock frequencies of the EM COTS parts could be avoided. Instead, the REXIS team decided to use surplus Vectron rad-hard crystal oscillators with different clock frequencies available from GSFC electronics surplus on short-notice. These rad-hard parts was the only suitable option available to the REXIS design team for meeting the rad-hard requirement for this critical timing functionality, since this vulnerability was not identified on the EM Interface Board.

The Interface Board provides drive voltages for the CCDs by taking advantage of the radiation tolerance of the Interface Board FPGA. In the EM design, digital to analog converters (DACs) were used

to provide these voltages. In the FM design, a series of voltage pulses of varying width, known as a pulse-width-modulation (PWM) signal, is run through a low-pass filter to provide the analog CCD drive signal. The PWM signal originates from a FPGA GPIO pin while the resistor/capacitor (RC) low-pass filter circuit converts the varying duty cycle of the FPGA's PWM signal to a time-varying voltage acceptable to the CCDs. The result of this process of converting digital pulses from the FPGA into analog voltages is shown in the green line in Figure 4-2.

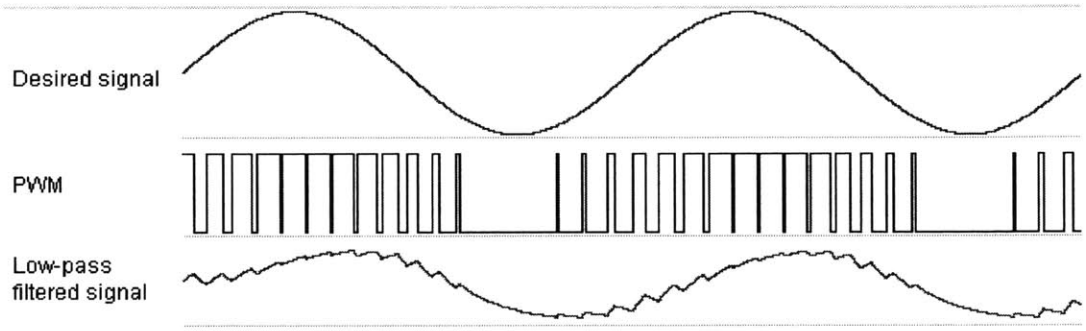

Figure 4-2: Analog Voltage Generation with PWM [17]

From a radiation tolerance perspective, the FM's combination of a PWM signal from a radiation tolerant FPGA's GPIO pin and an inherently radiation tolerant RC filter is much better than a COTS DAC microchip. Furthermore, this combination is replicable since the Interface Board FPGA had many unused GPIO pins and RC filters are made of small and cheap passive electronics. Since 32 of these analog voltage outputs were needed, the ability to copy these RC filters and the FPGA GPIO configuration was highly preferable to the other rad-hard alternative. This alternative is using an array of single or dual-channel rad-hard DACs that occupy at least 10-20 times the PCB space the COTS EM design does.

Originally, the REXIS design team looked for rad-hard DACs that could output at least 8 voltages at once like their COTS counterparts on the EM design. Such hardware could not be found and this was the motivation to adopt the combination of an FPGA-derived PWM signal run through a low-pass RC filter.

[17] Figure from webpage: *"Piano" with RTOS* by Victor Timofeev. Produced April 2009. Accessed March 16, 2016. URL: http://www.pic24.ru/doku.php/en/osa/articles/pk2_osa_piano

Regardless, the PCB pads from the EM design that the COTS DACs are soldered to are still retained on the FM design in case if testing revealed this new approach for the FM did not work. Although these pads have remained unpopulated on the FM boards, removing them would have incurred more PCB rework in the EM-to-FM process and leaving this backup in place did not have any drawbacks.

Instead of using discrete rad-hard digital encoder and decoder microchips, used for activating CCD drive-voltage generation circuitry, this functionality is implemented with digital logic hardware within the Interface Board FPGA. The cost of this method is extra FPGA development, increased digital logic resource utilization aboard the DE FPGA, and more GPIO pins used. However, the functionality of a 3-to-8 decoders and 8-to-3 decoders provide is extremely simple to implement in an FPGA and requires a minimal amount of digital logic resources. Furthermore, the Interface Board FPGA has a large surplus of GPIO pins. These digital encoder/decoder microchips were original COTS parts in the EM Interface Board design which borrows heavily from circuitry developed early on in the Transiting Exoplanet Survey Satellite (TESS) project. The TESS project did not have an FPGA available to implement the encoder/decoder functionality so discrete chips were used in the TESS design. This TESS design was optimized for integration into the Interface Board in the transition from EM to FM REXIS designs by implementing the encoder/decoder functionality in the Interface Board FPGA.

4.4.2 Video Board

The Video board consists of hardware from the 16 CCD nodes which provide digital pixel data from $1/16^{th}$ of the CCD sensor. Collectively, these nodes form a redundant mechanism that allows REXIS to meet its primary science objectives in spite of node failures further described in Section 4.4. Having this system-level protection from radiation-caused failures, component-level design of the Video Board takes degradation from space radiation into account. However, the resilience to radiation-caused damage that system-level redundancy provides through 16 identical nodes allows the Video Board to consist primarily of COTS components.

An example of using COTS parts in place of rad-hard parts can be found on the ADCs aboard the Video Board. In this case, these COTS parts are empirically proven to be suitable for the REXIS mission through testing. After the CCD pixel data goes through pre-amplification and buffer circuitry on the DE video board, the resulting voltages are read by sixteen ADCs. There is one ADC for each node. For the FM, these ADC128S102WGRQV ADCs were originally specified to do this conversion. They cost $2291.00 each[18] and were also used for housekeeping data acquisition (more details in Section 3.3.1.6). Using sixteen of these chips for each node would be too expensive for the REXIS project and the lead time on these parts was unacceptable for timely project completion. Radiation testing data from the TESS program showed us that the significantly cheaper $48.11 AD7984BRMZ[19] was qualified to work in their mission. Their mission duration and high Earth orbit has a similar dose to the REXIS mission so it was decided to use this part instead of the ADC128S102WGRQV. After testing the AD7984BRMZ aboard REXIS, it was found that this chip could not handle single ended voltage measurements that it was required to take. We ended up switching to the variant of this chip that could take single ended voltage measurements. The single ended variant used the same exact PCB footprint and interface as the previous microchip and the internal micro-circuit architecture was very similar. Thus, this was the best option given the double-ended microchips inability to accurately measure the CCD signals.

The FM Video Board was also supposed to use sixteen ISYE-1009RH-Q rad-hard microchips for each node. These chips supply a 2.5 volt reference signal for the CCD buffer, amplification, and readout circuitry. This microchip is significantly larger than the COTS-equivalent part the EM Video Board was designed with. Since there was not enough time to rework the component layout of the Video Board PCB to accommodate the ISYE-1009RH-Q part and meet the design completion deadline for the FM Video board, the COTS-equivalent REF43GSZ from the EM was used instead. The REF43GSZ is a voltage reference implemented with a precision diode which is much more radiation tolerant than complex

[18] Quote for ADC128S102WGRQV supplied to REXIS project in 2014 from Avnet

[19] Digikey Electronics Webpage for AD7984BRMZ. Accessed March 18, 2016 at http://www.digikey.com/product-detail/en/analog-devices-inc/AD7984BRMZ/AD7984BRMZ-ND/1762644

microchips like FPGAs, DACs, microprocessors, etc. This COTS voltage reference has no tiny semiconductor features which are much more vulnerable to radiation-caused malfunction, thus making this component a low-risk replacement [29].

4.5 Summary of REXIS Avionics Mitigation of Radiation Hazard

The REXIS instrument is designed to operate in the interplanetary radiation environment of the OSIRIS-REx mission. Since REXIS is a Class-D instrument operating in a relatively benign radiation environment, various non-traditional radiation hardening features were added to the Engineering Model (EM) design to form the Flight Model (FM) avionics hardware. These features balance the requirements to not harm the OSIRIS-REx spacecraft, educate students in space systems design, and produce scientific data from the asteroid Bennu. However, the REXIS avionics system uses traditional radiation hazard mitigation techniques as permitted by requirements, cost, and schedule.

Table 4.4 is a summary of the radiation hazard mitigation techniques implemented on REXIS. It also details the EM design in order to show which radiation-related upgrades were applied to the FM avionics system. Traditional radiation hazard mitigation techniques are shown with green, approaches unsuitable for spaceflight are shown in red, and novel techniques suitable for the REXIS mission are shown in yellow. Rationale is also provided for why the upgrades for a particular avionics system in the EM-to-FM transition were implemented.

Table 4.4: Summary of REXIS Avionics Radiation Hazard Mitigation

	EM	FM	Rationale	Section
Shielding	0.125" thick shielding and deployable radiation cover	0.125" thick shielding and deployable radiation cover	Shielding design met requirements from the EM design onward.	4.2.1
Passive Components	COTS	Automotive Grade	Automotive grade parts have sufficient quality and radiation tolerance for the REXIS mission.	4.2.2
MEB and DE FPGAs	COTS	Radiation tolerant industrial grade	FM FPGAs have significant margin on TID tolerance and since REXIS is class-D, occasional SEE-caused fault is acceptable. These FPGAs are drop-in replacements for their COTS-equivalent parts on the EM.	4.3.1, 4.4.1
MEB and DE Oscillators	COTS	Rad-hard	Failure of this part causes mission loss.	4.3.1, 4.4.1
NOR Flash	Prototype	Rad-hard	Failure of this part causes mission loss.	4.3.2
SDRAM	Prototype	Rad-hard	Failure of this part causes mission loss.	4.3.3
Spacecraft Interface Parts	Prototype	Rad-hard	Failure of this part causes mission loss.	4.3.4
Frangibolt Drive Circuitry	Prototype and COTS	Rad-hard	Failure of this part will cause mission loss and harm the OSIRIS-REx mission.	4.3.5
MEB ADCs	Prototype	Rad-hard	Low component count makes rad-hard parts affordable.	4.3.6
MEB SXM Circuitry	COTS	COTS, Rad-hard, Redundancy, SEL current limiting	COTS SXM circuitry passed testing at REXIS TID-levels. SXM is not primary REXIS sensor. For high radiation risks (complex microchips) with low parts count, using rad-hard parts was affordable.	4.3.7
Power System	Prototype	Rad-hard	Failure of these parts causes mission loss.	4.3.8
CCD Node Redundancy	COTS	COTS	Overall redundancy protects CCD image acquisition functionality.	4.4
Interface Board DACs, Encoder, and Decoder	COTS	Implemented in Interface Board FPGA	Rad-hard 8-channel DACs could not be found. Radiation tolerance Interface Board FPGA was leveraged.	4.4.1
Video Board ADCs	COTS	Experimentally proven radiation tolerant parts	Cost of fully rad-hard solution was too high and forced exploration and usage of experimentally proven parts.	4.4.2
Video Board Voltage References	COTS	COTS	Risk of radiation-caused failure of simpler electronics like voltage references is small. Effort necessary to change PCB design was too high.	4.4.2

Chapter 5 - Lessons Learned and Conclusion

This chapter presents some of the lessons learned from the REXIS avionics design. Recommendations are outlined for the improvement of the REXIS avionics system and successful avionics development in general. The content of this thesis is summarized at the end of this chapter.

5.1 Reconfigurability Facilitates Project Development

REXIS is an example to how flexibility is essential for the successful development of NASA Class-D missions. Flexibility is the ability to easily reconfigure system parameters and behaviors. Consider the GSFC Class-D Mission constitution that states "Given that these [Class-D] Projects allow for flexibility in risk mitigation to constrain cost or schedule overrun, and that all Projects will present unique challenges in that regard, mission assurance requirements may vary considerably from one Project to the next and will be dependent upon the individual Project's risk posture" [1]. It is expected that Class-D projects reconfigure systems during development to mitigate newly uncovered project risks. This redevelopment was undertaken while developing REXIS avionics. Thus, it is essential for Class-D missions to incorporate flexibility and reconfigurability early on and preserve these attributes through system development and operation as much as possible. These attributes increase the chances of a Class-D mission of satisfying mission requirements while staying within the strict Class-D schedule and budget constraints.

REXIS avionics development would not have been possible without the flexibility and radiation-tolerance of the FPGAs used in the project. REXIS used two FPGAs – a Xilinx Virtex5 XQ5VFX130T-1EF1738I chip on the Main Electronics Board (MEB) and an Atmel RT3PE600L-1CG484B chip on the

DE-interface board. Both chips are designed to function in the OSIRIS-REx's radiation environment, thus making them rad-hard umbrellas under which designers place required avionics functionality by implementing them as FPGA digital logic cores. This approach is much more preferable and quicker than procuring expensive rad-hard hardware and running through many cycles of expensive PCB design/fabrication/testing. The flexibility of these FPGAs allowed the REXIS development team to affordably and rapidly iterate design/fabrication/test cycle to add features and fix issues.

Furthermore, REXIS uses a Microblaze processor to execute the FSW. This processor is created with the logic resources aboard the Xilinx FPGA so it is effectively radiation hardened like the FPGA cores implemented with FPGA logic resources. The FSW is also highly reconfigurable since the functions and commands that it consists of can easily be created or rearranged in the FSW Integrated Development Environment (IDE). The radiation tolerance and reconfigurability of the FPGAs and FSW significantly contributed to the REXIS avionics system being functional at the time of REXIS integration with the spacecraft.

5.1.1 FPGA Digital Logic Cores

Configurable Xilinx-supplied FPGA cores that were pre-built and tested were extremely convenient for REXIS development. Figure 3-18 shows the majority of FPGA cores in the MEB FPGA are developed by Xilinx. Because these FPGA cores are tested and designed to integrate easily with each other, the REXIS development team could focus on the novel functionality in the REXIS FPGA like the image and SXM data processing.

Some examples of the flexibility and ease of use of the REXIS FPGAs that simplified the REXIS avionics development are listed below.

1. **Clock Generators** – The MEB FPGA has a clock generator core that transforms the signal from a crystal oscillator into the variety of clock lines necessary to operate the FPGA and SDRAM. The clock generator core was already designed and tested by Xilinx and had the capability to accommodate the 100MHz crystal from the EM hardware and the 36MHz crystal in the REXIS

flight hardware. This flexibility was essential since the REXIS team did not have to purchase new hardware to accommodate the rad-hard crystal oscillators that were added during the EM to FM transition.

2. **Analog Voltage Output for CCD Drive Signals** – The DE interface board was required to provide time-varying voltages to appropriately power the CCDs. Instead of using a rad-hard DAC to supply these voltages on the FM, the flexibility of the DE interface board's FPGA allowed a different approach to be used. The digital logic resources aboard the DE FPGA made a PWM signal readily available for low-pass filtering. This approach created the appropriate time-varying FPGA-controlled voltage. Instead of using the FPGA to command a DAC, it is commanding an internal PWM core that generates the same CCD drive voltage. This approach is further detailed in 4.4.1.
3. **RS422 Baud Rate Changes** – While testing the REXIS flight software and x-ray image acquisition hardware, uncompressed full-resolution x-ray images needed to be acquired from the REXIS system. Normally, this would take 25 minutes with the RS422 port set to the OSIRIS-REx imposed baud rate. However, the baud rate of REXIS's RS422 ports could easily be changed by reconfiguring the RS422 FPGA core. Increasing the baud rate to 460800 baud reduced the time to download an x-ray image to a much more reasonable 5 minutes and greatly sped up REXIS development. However, high-baud rate bitstreams are not representative of conditions aboard OSIRIS-REx so the slower baud rates specified by the OSIRIS-REx mission were used for final testing.
4. **DE Simulator** – The correctness of the REXIS image processing algorithms was verified with the DE simulator. The DE simulator is physically identical to the DE-interface board but different functionally. More specifically, the interface board's FPGA is designed to operate the DE while the DE simulator's FPGA tests the image processing. Instead of outputting an x-ray image acquired from CCDs to the MEB, the DE simulator supplies the MEB with imaging test patterns. The DE simulator is extremely convenient since it uses the same exact CameraLink

interface to the MEB that the interface board uses and allows for realistic testing of the image processing algorithms. The reconfigurability of the DE FPGA was essential for developing this convenient test platform.

In all these cases, the REXIS development team easily reconfigured the FPGA cores in the Xilinx graphical user interface (GUI) instead of buying, testing, and integrating expensive new physical hardware.

5.1.2 Microblaze Processor

One particular FPGA core that works well in the REXIS system is the Microblaze processor. It is very straightforward to generate FSW for this processor, configure it for the REXIS requirements, and integrate it with the rest of the REXIS system since the Microblaze is frequently used and easily reconfigured in other COTS applications. The Microblaze was designed by Xilinx to integrate easily with other FPGA cores through the Processor Local Bus (PLB) so the integration of both custom and COTS FPGA cores within REXIS was not difficult.

Furthermore, the Microblaze could be configured to better meet REXIS's needs. For example, the image processing algorithm did not use any floating-point computation so the resource-intensive floating point computation hardware within the Microblaze design was not instantiated on the FPGA. On the other hand, the REXIS FSW frequently multiplied integers together and there was surplus digital logic hardware available within the FPGA. So the integer-multiplication hardware within the Microblaze was instantiated and used instead of using time consuming general machine-code based assembly instructions to implement multiplication.

Most of the computation architecture of the Microblaze processor could be configured in this straightforward GUI-based manner in Figure 5-1. The top-left red box in Figure 5-1 shows how the REXIS Microblaze processor was configured with additional hardware such as a barrel shifter that quickly computes multiplication and division by powers of two, integer multiplier/divider circuitry that quickly computes these operations instead of using repeated additions/subtractions, and other similar

computation functionalities implemented with FPGA digital logic resources. The red box at the bottom of Figure 5-1 shows how the processing speed (Frequency), FPGA digital logic resource utilization (Area), and Microblaze computation capability (Performance) change as the processor is configured with the GUI in the other red box. For example, enabling the floating point computation unit doubles the FPGA digital logic resource utilization and increases the performance of the processor as well.

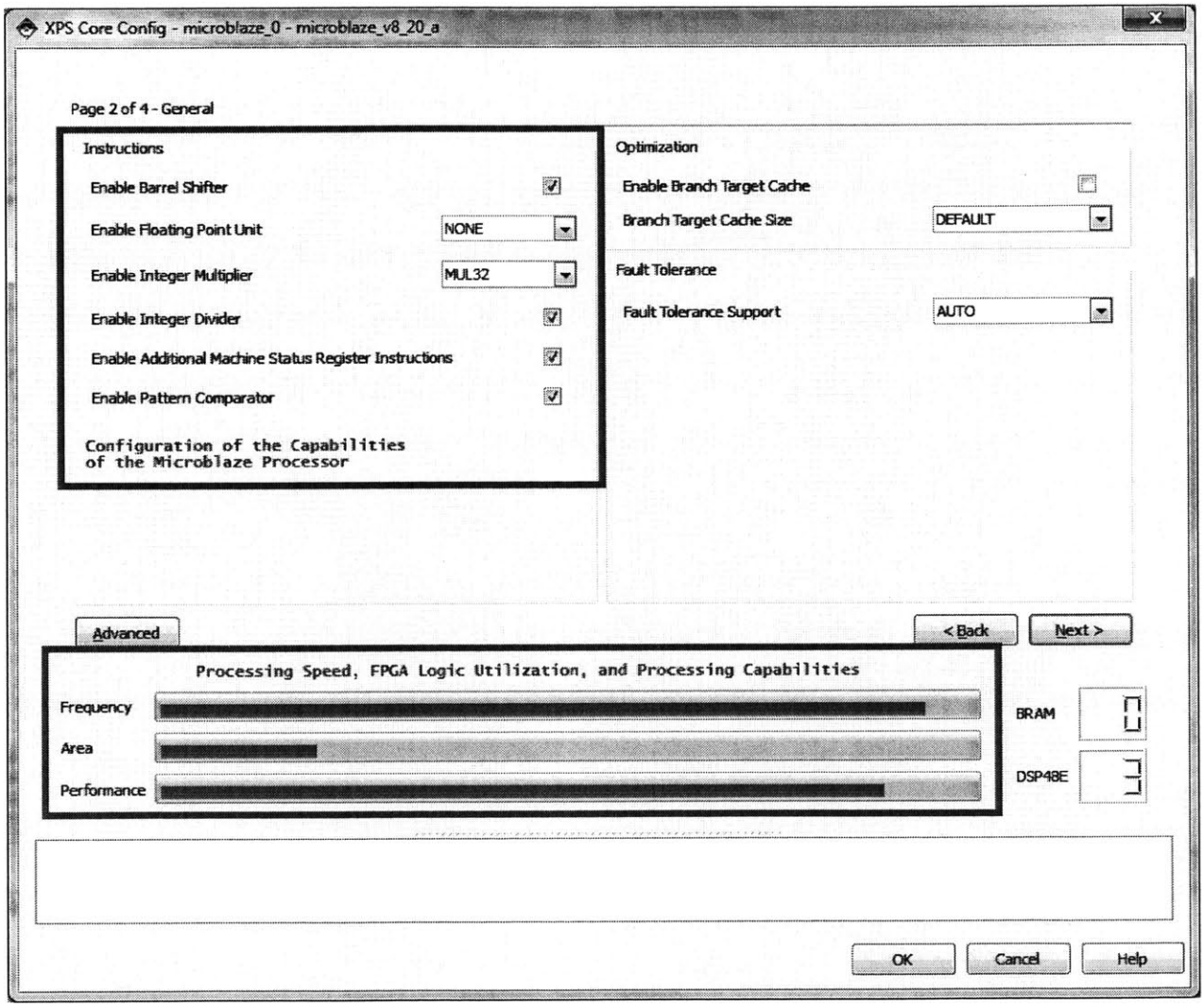

Figure 5-1: Microblaze Configuration GUI for REXIS

5.1.3 Image Processing

The image processing FSW and FPGA cores were originally developed with the assumption that the CCD data is transmitted to the MEB in row-major order. Row major order is defined as the values of each

contiguous row of CCD pixels stored in contiguous sections of computer memory. The REXIS development team found out very late in the project development cycle that the CCD pixel data was not stored in row-major order. Instead the pixels were stored in a shuffled manner due to the CCD/DE design. Each group of 16 pixels in adjacent memory locations corresponds to pixels from each of the 16 CCD nodes. To further complicate this readout pattern, nodes 1 and 2 on each CCD are output in a left-to-right order while nodes 3 and 4 are read out from right-to-left. The overclock and underclock pixels are always read out left to right.

The main method of fixing this surprise CCD pixel readout issue is adding FSW functions that translate between these two coordinate systems: image coordinates and CCD coordinates. CCD coordinates correspond to the shuffled arrangement of pixels that is actually output by the DE. Image coordinates correspond to the physical arrangement of pixels that is useful for determining the location, energy, and grades of x-ray events. The assumption that the original FSW was built on was x-ray images would be stored with the image coordinate system in SDRAM. Various FSW functions implement algorithms that transform between these two coordinate systems. These algorithms were initially tested in MATLAB since MATLAB's large amount of built-in tools and data visualization capabilities made this testing process easier. Once the algorithms were vetted, they were implemented in the FSW as functions. These FSW coordinate transform function were called any time the pixel data in SDRAM memory was accessed. So the image processing code that was originally written to operate over images stored with the image coordinates order was now compatible with the data stored in CCD coordinate order.

The framegrabber FPGA core also had to be modified to handle this switch from image coordinates to CCD coordinates. Since the FPGA primarily did pixel-by-pixel processing, the only change had to be applied to the overclock correction and ET-thresholding performed by the FPGA. The overclock correction and ET-thresholding components of the framegrabber was modified so that the FPGA core would sample the pixels in the correct area of the memory required for CCD pixel readout.

Reconfigurability eases project development since it allows designers to react quickly and effectively to issues. Since the FSW was reconfigurable, the REXIS development team could redesign the image

processing functionality to handle the differently stored pixels. This highly reconfigurable computing is vital to projects like REXIS and state-of-the-art spaceflight computers like NASA's SpaceCube. SpaceCube uses three reconfigurable FPGAs to implement large computing systems with many FPGA cores and soft-core processors to meet space-computing requirements [32].

5.1.4 Importance of Avionics Reconfigurability

Based on the previous example of the reconfigurability of FSW and FPGA cores, reconfigurability should be a priority for resource constrained missions since it increases the chances of success. New concepts can quickly be tried and tested with a reconfigurable system so system properties can be determined early on and unforeseen problems can be easily dealt with. The ability to easily load new FSW and FPGA cores into REXIS greatly contributes to the ease of development since this reconfigurability allows:

1. The fixing of unexpected problems
2. System changes to meet requirements
3. Easy transition from EM to FM designs

Because there is more design freedom early on in the project, new concepts can quickly be tried and tested with a reconfigurable system [3]. Rapidly experimenting to determine the best system configuration allows properties can be determined early-on and unforeseen problems can be easily dealt with.

The usefulness of a reconfigurable avionics system can also be extended to the time the system is operational in outer space. The ability to reconfigure an avionics system during spaceflight will allow the users to deal with unforeseen problems and add new capabilities as necessary. The design of the REXIS avionics system has already taken a step in this direction by implementing Function Upload. Function Upload is a FSW capability to accept and run new FSW functions through command data sent from Earth. This functionality allows the REXIS team to add new FSW code to handle unforeseen problems during flight and is further detailed in Section 3.2.9.

The key question to ask is if the same reconfigurability capabilities that REXIS had on the ground during development should be available during space flight. Such capability is possible in the SpaceCube spaceflight scientific computing system which uses an auxiliary FPGA to verify and relay configuration data to two Xilinx Virtex5 primary computation FPGAs [32]. Implementing this complete spaceflight avionics reconfiguration capability has its own set of benefits and drawbacks that need to be explored and evaluated.

The complete spaceflight avionics reconfiguration capability has three key benefits. The first benefit is the increased ability of the REXIS operations team to fix unforeseen problems during operations, beyond the existing function upload capability by uploading new FSW or FPGA cores. Secondly, new functionality can be added through new FSW and FPGA cores. Finally, schedule-based pressure on development process is eased since the avionics can be integrated and launched without meeting all the requirements, assuming that the uploading of new FSW or FPGA cores is scheduled to meet requirements during spaceflight.

For REXIS, the capability of full FSW/FPGA reconfiguration through RS422 ports would have been very useful. This capability would have given the REXIS development team extra time to improve and test the FSW and FPGA cores. Once the REXIS instrument was bolted onto and integrated with OSIRIS-REx, uploading new bitstream data through the JTAG (connector J8 in Figure 3-4) was not allowed since this upload process required connecting an unknown computer to the OSIRIS-REx system. If new bitstream data could be sent to REXIS over the RS422 ports which are integrated into the OSIRIS-REx C&DH system, then this restriction could be avoided altogether. However, adding extra FSW/FPGA development time leaves less time for crucial documentation and ground-side data processing tools.

In general, the full avionics reconfigurability adds complexity and risk since resources need to be expended to develop and test this capability. For REXIS, there are several drawbacks to complete spaceflight avionics reconfigurability which are:

1. The REXIS bitstream requires 16 megabytes of space. Uploading 16 megabytes of data to the OSIRIS-REx spacecraft for relaying to REXIS requires a lot of time and OSIRIS-REx communications budget.
2. There must be enough non-volatile memory to store two bitstreams. One of the bitstreams will be the original one with minimal functionality that is verified as working. The other bitstream will be the newly uploaded one. The storage of two bitstreams is necessary in order to have a working copy to always revert back to in case a problem occurs. It may also be necessary to have two separate memory chips storing these bitstreams. Either way, the current REXIS bitstream storage system needs to be reworked.
3. No matter how many times a new bitstream with new FSW and FPGA cores is uploaded, the physical hardware will not change. This permanence limits the possibilities for fixes and new functionality to be implemented through bitstream upload.

These drawbacks must be carefully weighed against the benefits and post-launch development time provided by full avionics system reconfigurability.

5.2 Importance of keeping FSW simple

5.2.1 Software Development with C Programming Language

The REXIS development team created the REXIS FSW with the C programming language. The C programming language is highly suitable for Microblaze FSW development since it gives developers direct access to the Microblaze hardware, has no overhead in terms of background processes, and is a well-understood and commonly used language amongst programmers. Furthermore, REXIS had no need for dynamic memory allocation, memory management, and advanced data structures of other more complicated programming languages like Python.

However, the REXIS development team could have utilized the object oriented features of the C++ programming language. It would have been a better tool to keep track of the complexity associated with

image processing and telemetry generation. The C-based FSW uses nested data structures to allow programmers to interact with complex constructs with multiple attributes like the CXEL, telemetry queue, and FSW state machines. C++ is still a simple programming language like C but has extra object oriented syntax and features that are better suited to complex data structures. These features do not require any overhead like the more complex programming languages.

5.2.2 Minimizing the Number of Interrupt Service Routines

The REXIS FSW used too many interrupt service routines (ISRs), or small snippets of code that perform auxiliary tasks such as responding to a voltage change on a GPIO pin, managing newly available data from serial ports, or periodically performing timekeeping tasks. The execution of ISRs are triggered by the interrupt controller FPGA core that senses external events such as changes in specific GPIO pin voltage levels, serial port activity, and the expiration of FPGA timer cores. An ISR is executed by pausing the main FSW execution, running the appropriate ISR, and then resuming execution of the main FSW at the point prior to shifting to the ISR.

The REXIS FSW had too many ISRs (

Table 5.1) which made FSW development and debugging difficult. Because the Microblaze processor allows the use of many ISRs, it very tempting to implement functionality inside ISRs and keep the code for the main FSW thread very simple. However, there are many drawbacks to using many ISRs. It was a major inconvenience to debug code with lots of interrupts since the programmer has to jump between multiple functions without a clear written connection between them. The programmer must keep all the relevant ISRs in mind and think about the interactions they can have instead of having one clear FSW execution path to follow.

Table 5.1: Redesign Recommendations for ISRs

ISR Name	ISR Attributes		Condition to Activate ISR	Purpose of ISR	Future Redesign Recommendation
Switch Washer 3.2.4	GPIO	Continuous	Change in switch washer sensor voltage	Track switch washer state and shut off frangibolt if switch washer sensor transitions from closed to open	Remove and replace with FSW polling mechanism
External Time Tick 3.2.2	GPIO	Side A/B	Falling edge of the time tick signal from spacecraft	Perform periodic FSW timekeeping and telemetry tasks. Resets the Time Tick Timer so its ISR does not unnecessarily execute	Keep because time tick pulses are not deterministic in the REXIS system since they originate from the spacecraft
Internal Time Tick 3.2.2	Timer	Continuous	Expiration of timer with 1.01 second period	Performs the same tasks as the Time Tick GPIO ISR in case the spacecraft time tick does not arrive. Missed time ticks are also noted	Combine into one ISR that operates at the rate of the Subsecond Timer ISR. This approach of combing the timer ISRs puts all the timing code in one place instead of split across concurrently running ISRs which are hard to debug.
Sub-second Timer 3.2.2	Timer	Continuous	Expiration of timer with 0.001 second period	Updates the FSW's subseconds timing value every millisecond	
Frangi-bolt Timer 3.2.4	Timer	Frangibolt	Expiration of timer with 1 second period	Handles frangibolt timing tasks such as the arm and fire timeout.	
SXM Timer 3.2.6	Timer	Science	Expiration of timer with 1 second period	Handles the FSW's SXM management tasks and state transitions every second.	
Space-craft Serial Port 3.2.3	Serial	Side A/B	Data is available from the OSIRIS-REx spacecraft	Transfer spacecraft command data from the small buffer in the serial port FPGA core to a large buffer the FSW uses.	Keep because the serial port data can arrive at any time.
DE serial Port 3.2.5	Serial	Science	Data is available from the DE over the CameraLink serial port	Transfer DE data from the small buffer in the serial port FPGA core to a large buffer the FSW uses.	Keep because the serial port data can arrive at any time.

Table 5.1 contains recommendations for making the FSW ISR system simpler and easier to debug.

Table 5.1 follows the same format as Table 3.1 which introduces all the ISRs, but contains a different column on the right with redesign recommendations that are underlined. For example, the four timer-based ISRs should be combined into one consolidated timer ISR that operates in response to just one FPGA timer core with a 1 millisecond period. This consolidated timer ISR keeps track of the second and subsecond counts and modifies all the flags that original four ISRs did. For example, if the frangibolt-arm command is processed, then the frangibolt-arm timeout counter is incremented by the consolidated timer ISR. Similarly, if REXIS is in science mode, the consolidated timer ISR operates the SXM histogram core. This approach is much simpler, uses fewer digital logic resources within the FPGA, and fewer ISR ports in the FPGA ISR core.

Currently the frangibolt/radiation cover system sub-optimally uses two ISRs to handle timing and switch washer sensing as shown in

Table 5.1. The frangibolt timer ISR executes the fire and arm timeouts and the switch washer ISR monitors the switch washer sensor. Thus, the frangibolt system has three independent segments of code – the two ISRs and the main FSW code. Developing and debugging this system was difficult because the execution of these three pieces of code had to be managed. Instead of three independent FSW routines, a single routine should be used for the frangibolt that polls the timekeeping variables (from the consolidated timer ISR) and switch washer. This system is much easier to understand and debug since there is only one body of code that directly implements the frangibolt state machine that is further detailed in Figure 3-12. Polling the switch washer is acceptable since this sensor does not need to have an immediate reaction. The exception to this polling scheme is when the frangibolt is fired and the FSW must immediately cut power based on switch washer output. In this case, the FSW can sample the switch washer frequently enough to prevent the outgassing hazard during the frangibolt fire state.

5.3 Conclusion

This thesis describes the avionics system of the Regolith X-ray Imaging Spectrometer (REXIS) along with the radiation concerns this avionics system had to overcome. The first chapter details the OSIRIS-REx mission where REXIS is integrated as a remote-sensing payload instrument. The REXIS system and scientific objective of classifying the asteroid Bennu based on the elemental regolith composition also described in chapter 1. The second chapter introduces how radiation in space impacts the nominal operation of space electronics systems. The third chapter presents the REXIS avionics system and the subsystems it is comprised of. The fourth chapter presents how the REXIS avionics system is designed to meet its requirements in the presence of space radiation. The fifth chapter concludes with technical lessons learned from designing, testing, and operating the REXIS avionics system.

REXIS is an example of a successful interface between a low risk Class-B spacecraft and a high risk class-D payload that is useful for developing similar space systems. The REXIS avionics system has features and precautions that make this interface possible by preventing harm to the OSIRIS-REx spacecraft. These range from electrical isolation of power busses to the frangibolt system design that

prevents the contamination of the OSIRIS-REx asteroid sample. The radiation approach used aboard REXIS balances the low-cost nature of class-D projects with the hazards from the interplanetary space radiation environment usually reserved for class-B missions. These aspects of REXIS, along with the avionics design as a whole, should be used as an example for the development of future Class-D missions operating in challenging environments.

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