

Energy Management in Biomedical Applications: Wireless Power and Biosensing

by

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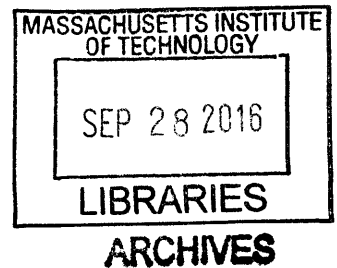
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Abstract

Wireless health and fitness devices as well as traditional medical devices such as cardiac and neurological implants, skin patch sensors, and automatic drug delivery pumps extend and improve life by providing therapy, monitoring, and diagnostics. They ensure health and safety while promoting prevention and wellness. These devices are found in chronic and acute settings that range from emergency and critical care to personalized health and telemedicine; they accelerate medical research and support data-driven medicine. The push towards the ubiquity of ever smaller devices with more functionality compels power-centric strategies in every aspect of design.

Long-term implantables such as neural implants for the treatment of Parkinson's disease and epilepsy traditionally rely on primary cell batteries, which occupy a large portion of the implant volume and when exhausted require a new surgery for replacement. The motivation of the thesis is to reduce the size (weight and volume) and increase the lifetime of neural implants through the use of a smaller rechargeable battery. The two strategies chosen in this thesis are: 1) using a new spread-spectrum wireless power transfer to recharge and ultimately, eliminate the battery through direct powering; 2) reducing power consumption through the use of closed-loop decision and parameterization of electrical stimulation using feedback from neural sensing.

The first part of this thesis is the development of spread-spectrum wireless power transfer to deliver power over many frequencies over a uniform single-sided magnetic field, which enables better design of systems with various physical dimensions, lower tissue loss, and less sensitivity to component tolerances, while remaining within the regulatory limits for electromagnetic interference. The investigation encompasses the design of a spread-spectrum transmitter and modulation method that resolves the ostensible paradox of "resonant, yet spread-spectrum", a passive power receiver, and power transfer using a uniform single-sided magnetic field.

The second part of this thesis involves the design of a system to amplify and extract the spectral power of neural electrical signals from the brain. From the spectral power, "biomarkers" are extracted to titrate deep brain electrical stimulation to im-

prove therapy and better utilize this functionality that dominates the implant power consumption.

Thesis Supervisor: Steven B. Leeb

Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

WIRELESS health and fitness devices as well as traditional medical devices such as cardiac and neurological implants, skin patch sensors, and automatic drug delivery pumps extend and improve life by providing therapy, monitoring, and diagnostics. They ensure health and safety while promoting prevention and wellness. These devices are found in chronic and acute settings that range from emergency and critical care to personalized health and telemedicine [9]; they accelerate medical research and support data-driven medicine. The push towards the ubiquity of ever smaller devices with more functionality compels power-centric strategies in every aspect of design.

Long-term implantables such as neural implants for the treatment of Parkinson's disease and epilepsy traditionally rely on primary cell batteries, which occupy a large portion of the implant volume and when exhausted requires a new surgery for replacement. The motivation of the thesis is to reduce the size (weight and volume) and increase the lifetime of neural implants through the use of a smaller rechargeable battery. The two strategies chosen in this thesis are: 1) using a new spread-spectrum wireless power transfer to recharge and ultimately, eliminate the battery through direct powering; 2) reducing power consumption through the use of closed-loop decision and parameterization of electrical stimulation using feedback from neural sensing.

1.1 Bilateral Strategy for Energy Management in Implants

The size of biomedical devices, especially implants, is largely determined by the battery. In these types of devices, the relevant factor for battery size is energy capacity, which fundamentally limits operational life. The traditional design for long-term im-

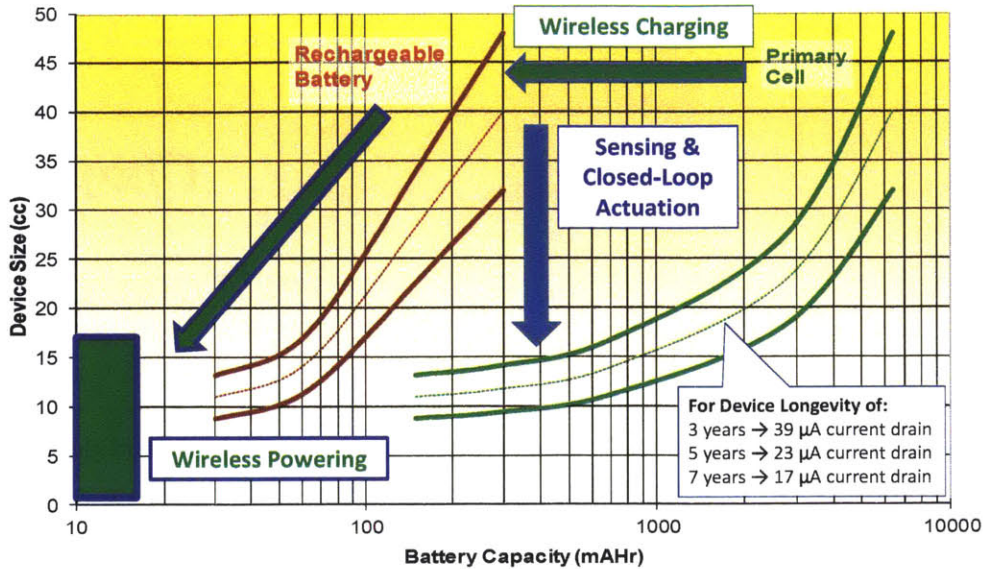


Figure 1-1: Bilateral Approach to Implant Power Management: Wireless Power Transfer and Sensing for Closed-Loop Actuation.

plantables uses a primary cell (i.e. non-rechargeable battery). Figure 1-1 illustrates the tradeoff between battery capacity and device size. It is notable that the device size asymptotically approaches less than 10 cc as the battery capacity reduces. Wireless power transfer enables the use of rechargeable batteries. Although rechargeable batteries have much less energy density than an equivalent primary cell, periodic recharging ultimately results in lower overall device size.

To put matters into perspective, a 1 mW device requires a weekly charge for approximately 10 minutes at 1 W. Even with an energy density of about half that of a 7-year primary cell, a rechargeable battery represents over a 175-fold decrease in required battery capacity. Of course, careful use-case analysis will dictate the required capacity margin.

For example, the Quallion QL0200I-A lithium-ion rechargeable battery, which is used for medical implants, has a capacity of 200 mAh with a nominal voltage of 3.6 V weighing 8 g and occupying 3.27 cc [80]. After 2,000 charge-discharge cycles, the battery only loses approximately 20% of its capacity retention [4]. If charge-discharge cycling were the primary consideration, this capacity retention can be extrapolated to 40 years.

To further reduce implant size, micropower sensing [11, 23] enables “closed-loop” therapies. Power consumption is reduced by only performing therapy (e.g. electrical

Table 1.1: Comparison of Wireless Powering Requirements

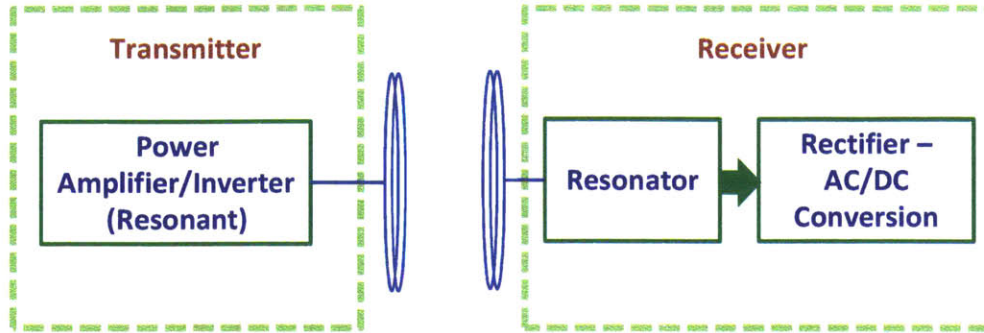
| Biomedical Devices | |
|-------------------------------------|------------------|
| M2510 Mote | 10 μ W |
| Cardiac Implant (Closed-Loop) | 1 μ W |
| Cardiac Implant (Open-Loop) | 2.5 μ W |
| Neural Implant (15 cc) | 100 μ W–1 mW |
| Insulin Pump | 3.5–10 mW |
| Endoscopy | 10 mW–30 mW |
| Wirelessly Powered Artificial Heart | 10–30 W |
| Charging Consumer Devices | |
| Phone/Tablet (3000 mA-hours) | 5 W |
| Laptop | 20–100 W |
| Cars | |

stimulation) when needed. As neuroscience and the understanding of neurological diseases progresses, fine-tuning of parameters in real-time such as stimulation amplitude among other pulse profiles using complex controllers in response to electronic neural sensing will ensure the most effective use of electrical power [6].

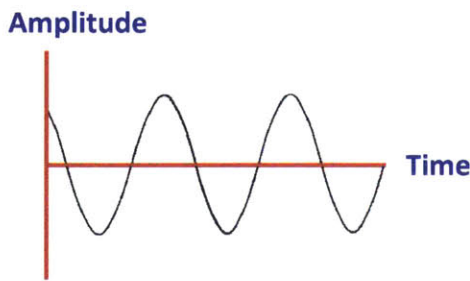
1.2 Wireless Power Transfer

Wireless power transfer (WPT) was pioneered by Nikolai Tesla in 1899 [35]. WPT can be characterized by the physical medium of energy transfer and by the transfer distance (d) relative to the wavelength (λ) of the energy in the medium. Examples of wireless power transfer can be found using pressure waves through the air and biological tissue using ultrasound [81] and acoustically through metal barriers [62]. In electromagnetic systems, energy transfer can be rendered through either electric or magnetic fields in the near-field (quasi-static) ($d \ll \lambda$) and transverse electromagnetic fields propagating in the far-field ($d \gg \lambda$) and weakly propagating in the mid-field ($d \approx \lambda$) [49].

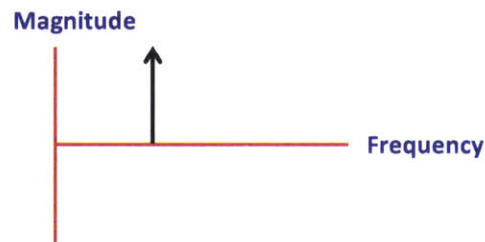
The work in this thesis is confined to contributions in near-field wireless power transfer, specifically magnetic coupling, but extendable to capacitive as well. Throughout this document, reference to WPT will specifically be restricted to power transfer by near-field magnetic coupling.



(a) Single-Frequency Wireless Power Transfer Architecture



(b) Time-Domain Sine Wave



(c) Frequency-Domain Impulse

Figure 1-2: Single-Frequency Wireless Power Transfer

1.2.1 Single-Frequency Wireless Power Transfer

Wireless power transfer is most conspicuously and usually borne through a single frequency. Figure 1-2 conceptually illustrates the schema. Alternating current is generated and transformed into a magnetic field as efficiently as possible and then received and transformed back into a current also as efficiently as possible. Both the efficiency and the power transferred are strongly dependent on the coupling coefficient (k), which is purely a factor of physical geometry and the material in between that describes the portion of total magnetic flux that is shared by the transmitter and receiver coils and hence semi-definitely positive and inclusively less than unity. A thorough discussion can be found in [13].

1.2.2 Regulatory Considerations

There are several considerations in the unfettered broadcast of wireless power: electromagnetic interference and safety unequivocally paramount and both governed by regulations. There are a specific set of frequencies, which are generally agreed throughout

Table 1.2: Single-Frequency Unrestricted Industrial, Scientific, and Medical Bands¹

| Center Frequency (f_c) | BW | $Q = f_c/BW$ |
|-------------------------------|---------|--------------|
| 6.78 MHz | 30 kHz | 226 |
| 13.56 MHz | 14 kHz | 969 |
| 27.12 MHz | 326 kHz | 83 |
| 40.66 MHz | 40 kHz | 1017 |

the world to be unrestricted vis-à-vis the power output, some of which are summarized in Table 1.2. What is notable is the lack of breadth about each of these frequencies, termed *Industrial, Scientific, and Medical (ISM)* bands. From 6.78 MHz to 40.66 MHz, which are in the range of frequencies of interest in this thesis, the Q or quality factor ranges from 83 to 1,017, corresponding to a bandwidth of 326 kHz at 27.12 MHz and 40 kHz at 40.66 MHz, respectively. There are some important consequences to this exactitude. Communications at these illustrated frequencies can only occur at a relatively low rate because modulation sidebands are required to remain within these spectral limits. Components for tuning such as inductors and capacitors must maintain tight tolerances over ensemble, temperature, and time. For example, a second-order circuit that is tuned to receive power at 27.12 MHz must have the inductor and capacitor each be precise to just over 1% because even accommodations in output frequency that might be made by the transmitter are limited by the allowed bandwidth. This necessarily drives cost and complexity to stave reductions in performance like efficiency and power.

Apart from these unrestricted ISM bands, limits to broadcast power are stringent. According to CISPR 11, the magnetic field limits decrease linearly with logarithm from 39 dB μ A/m at 150 kHz to 3 dB μ A/m at 30 MHz² [1, 2].

Safety as it pertains to wireless power transfer is encapsulated in the SAR (Specific Absorption Rate) metric, which quantifies the heating of a specific biological tissue due to electric, magnetic, or electromagnetic fields. Regulatory limits have been based on measurements and compilation of data originally by Gabriel et al. in the 1990's [32]. Recent standards including from IEEE [3] and ICNIRP guidelines [38] limit whole-body exposure conservatively to 0.08 W/kg between 100 kHz and 3 GHz.

¹FCC Part 18 Subpart C, Section 18.301 Operating Frequencies.

²The magnetic field limit is a quasi-peak measurement at 3 m with a resolution bandwidth (RBW) of 9 kHz for group 2, class B equipment

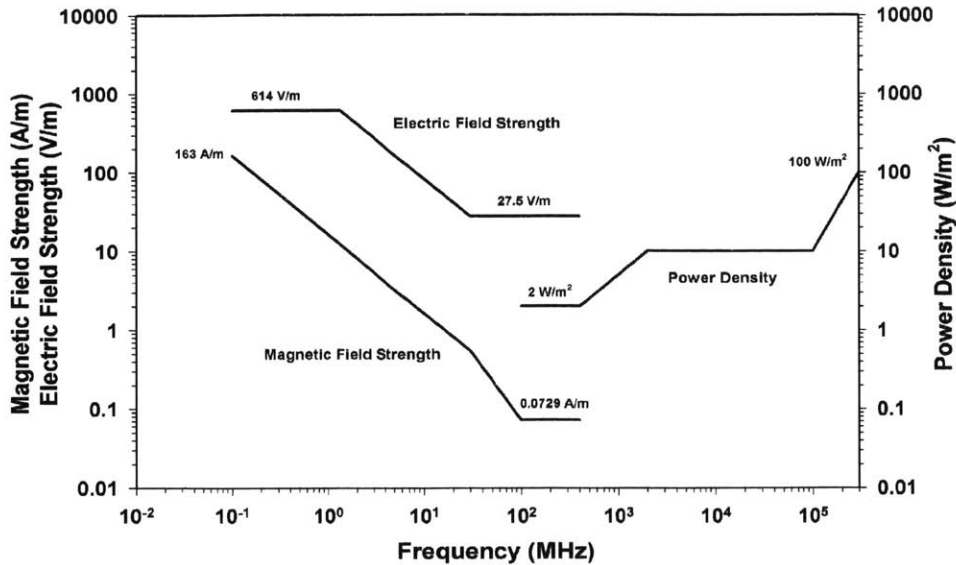


Figure 1-3: Maximum exposure to electric, magnetic, and electromagnetic fields from 100 kHz to 300 GHz reproduced from [3].

This corresponds to a 150 lb person limited to an average absorption of just under 5.5 W; the absorption depends on frequency and whether the field is electric, magnetic, or electromagnetic with the specific limits illustrated in Figure 1-3. The allowances are higher for localized exposure (up to 2 W/kg) when averaged over 10 g of tissue in the shape of a cube with a volume corresponding to approximately 10 cm³. Extremities distal to the elbows and knees limited to 4 W/kg.

1.2.3 Spread-Spectrum Wireless Power Transfer

The concept of spread-spectrum transfer of energy dates back to World War II, where it was invented by Hedy Lamarr and George Anthiel [69] for communications. This form of spread-spectrum consisted of transmitting power over different frequencies that change over time and is known as “frequency hopping”. By spreading the transmitted power over different frequencies, the receiver becomes more resistant to intentional or unintentional interference [29]. This concept has been extended to reduce the effect of electromagnetic interference by frequency-modulating digital clocks [44, 50].

An illustrative way to think about spread-spectrum power transfer is to consider white noise in Figure 1-4a. White noise is created by a random process with a

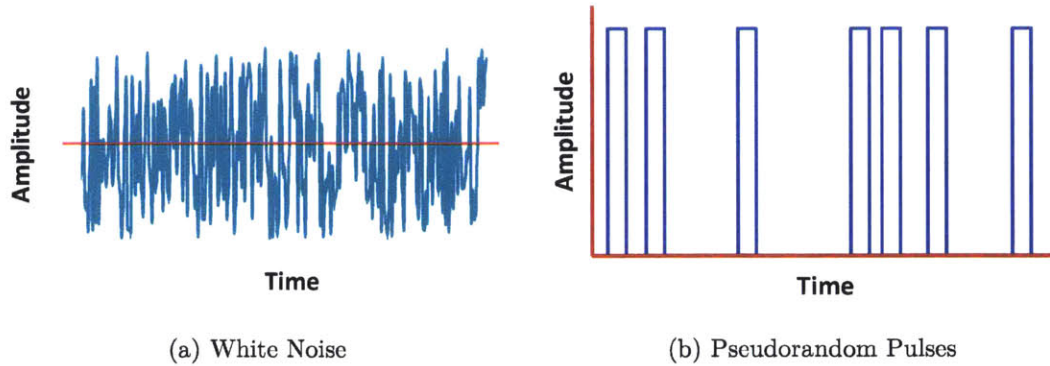


Figure 1-4: Examples of Spread Spectrum Waveforms.

flat power spectral density³. Another way to spread power over a wide spectrum is through *direct-sequence spread spectrum* (DSSS) [29]. An example of DSSS is the modulation in a pseudorandom pattern the time-position of pulses with fixed width and amplitude [115] as illustrated in Figure 1-4.

Towards spectrum-spreading, many types of constant-amplitude modulation are possible including frequency, phase, pulse-position, and duty-cycle; in many ways, these can be considered equivalent [34, 102]. To reduce electromagnetic interference in power electronic systems, random modulation methods have been employed [36, 106, 107]. Power electronic systems, being most often at the front of cascades of means-towards-ends in energy transformation, impact the efficiency of every pathway. Wireless power transfer is no different.

In Chapter 2 of this thesis, a means to wirelessly transfer power over a wide frequency band is delineated, resolving the ostensible paradox of resonant yet spread-spectrum. A major goal of the endeavor is to transfer power at any frequency while remaining innocuous to that which is sensitive to electromagnetic interference, which is mandated by regulations throughout the world. Figure 1-5 conceptually illustrates the structuring of the power transmission with a magnetic field over individual frequency bins, each below the stipulated limit.

1.2.4 Power Transfer Through Single-Sided Magnetic Fields

Single-sided fields allow the transfer of power in a particular direction. In principle, this doubles the magnetic field in the sought-after direction, eliminating loss and

³Power spectral density is one of the ways to depict the frequency spectrum of a random process.

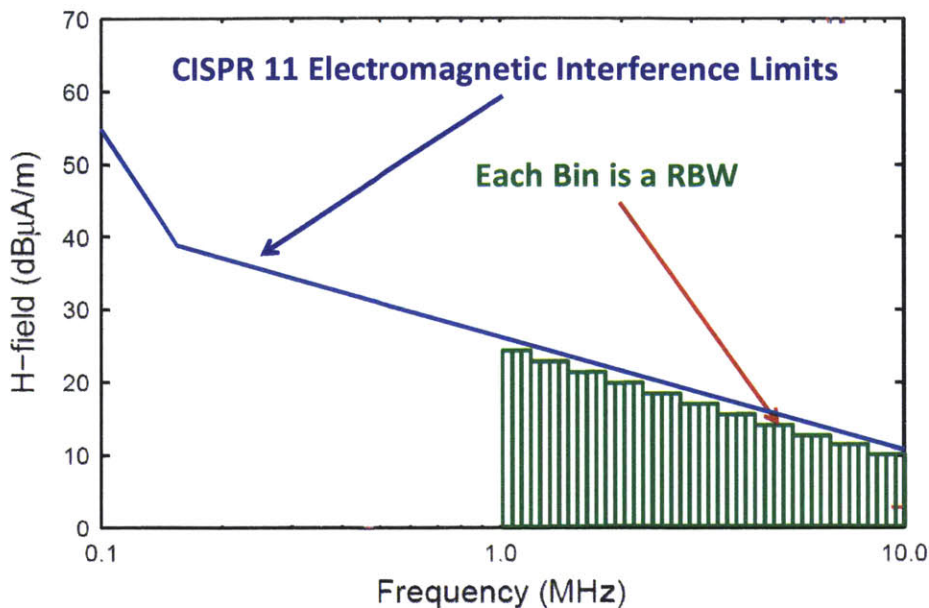


Figure 1-5: Spreading the magnetic field power into frequency bins sized at the resolution bandwidth (RBW) so the peaks fall below regulation mask.

subsequent heating, possibly due to unwanted coupling, in the reverse.

Permanent magnets or wound current-carrying conductors can be assembled to yield single-sided magnetic fields. Both Halbach [43] and Mallinson [67] independently posited configurations of magnetization that elicit these one-sided magnetic fluxes. Although originally meant to create static fields, these *Halbach* winding structures can be used to create ac magnetic fields. In chapter 4, the design of these windings is investigated and extended to create uniform fields using spatially-orthogonal windings. The design does not require magnetic material or conductor for shielding the unwanted direction with the uniform field allowing free-positioning of the power receiver. Both wireless power transfer and induction heating applications are prime beneficiaries; in the study, induction heating was used as surrogate to model and demonstrate the capabilities.

1.3 Neural Sensing

Neuromodulation or the actuation of the nervous system with electrical stimulation is a rapidly evolving field as a confluence between electrical engineering and neu-

rosience. Electrical stimulation dominates the power consumption in neurological implants. For example, a 3 V pulse with a peak current of 1 mA lasting for 400 μ s at a repetition rate of 100 Hz corresponds to 120 μ W of power. In comparison, neural sensing can be performed at 5 μ W per channel.

Many neurological conditions, such as epilepsy, are episodic and provide an increased opportunity to reduce power by providing therapy only prior to the onset. Neural sensing not only provides the tools for detecting onset, but also the important prerequisite of discovering potential biomarkers for prediction. Chapter 5 describes the design and application of a neural sensing amplifier that extracts the spectrum of the electrical signals from the brain.

1.4 Contributions and Organization of Thesis

The advancement in the quality of devices for biomedical applications through better power transfer and consumption is the essential contribution of this thesis. Spread-spectrum wireless power transfer because of its novelty required the conception of an entire system from end to end. Concepts, constraints, and goals for encoding the power along with its efficient transmission and reception had to be considered concurrently. The result is encoding by half-sine waves of almost arbitrary polarity using variable zero duration, ternary minimum-shift keying. The optimization and results of fixed-length sequences of this encoding are the subject of Chapter 2.

Sine waves are the seemingly natural choice for efficient, high-frequency power electronics, but are determinately single-frequency in preponderance. The design of high-frequency power electronics is enabled by the subjugation of device capacitance through *zero-voltage switching* (ZVS) and can be accomplished simply by a switched second-order system, which is exemplified by an inverse Class D (D^{-1}) amplifier⁴. The D^{-1} amplifier is capable of freezing its states by storing energy in its inductor, as a dual in the same vein as a voltage sample-and-hold analog circuit, hence permitting both ZVS and variable zero voltage duration. Arbitrary polarity required extra degrees of freedom that were enabled by two additional switches and a configuration of two transformers to properly structure the voltages, resulting in the *quad-switch push-pull amplifier* (QSPP). Along with the transmitter, a passive bandpass receiver was designed to capture energy from the spread spectrum. Both the transmitter and receiver are presented in Chapter 3.

⁴*Inverse* meaning the topological circuit dual and often referred to as current-mode in contrast to the usual voltage-mode.

Chapter 1 : Introduction

To better direct the energy, winding configurations for single-sided magnetic fields along with frequency orthogonal driving strategies were investigated and described in Chapter 4. These studies resulted in a more efficient two-layer winding structure with spatially-orthogonal windings for high uniformity fields with a drive that exploits frequency as opposed to phase-orthogonality to separate resonances and allow virtually independent control of power in each winding.

Chapter 5 presents the design and application of a spectral analysis integrated circuit. The concept of feedback demodulation results in micropower performance at low noise levels along with better interference rejection. This, along with further innovations allowed concurrent sensing and stimulation, resulting in the use and validation of closed-loop neuromodulation for epilepsy in a freely-moving sheep.

Chapter 2

Spread Spectrum Wireless Power Transfer

THERE is a growing concern for both electromagnetic interference (EMI) and human RF exposure in wireless power transfer applications. The conventional solution is to operate in one of the ISM bands such 13.56 MHz or 27.12 MHz [37, 73, 111] where transmitter power is largely unrestricted. However, in many applications like medical, portable, and wearable devices, where RF exposure of human beings is a greater concern, the ISM bands are often not the optimal frequency [75, 78, 109]. Outside of the ISM bands, the restrictions on radiated emissions and at lower frequencies, inadvertently conducted emissions, are particularly onerous [75, 118].

A large body of work in power electronics exists in the spectrum-spreading of interference using random modulation, which includes [36, 106, 107] and also in digital clocking [44, 50]. Spread spectrum wireless power transfer requires the power spectrum to be concentrated in the receiver passband with the smallest ratio of the spectral peak to integrated power in the passband. Precise spectral shaping using random methods can be difficult, especially with more complex spectral constraints, with only guarantees of average performance, but not reproducibility. Periodic modulation methods such as frequency sweeping can be precise in spectral shaping, but can introduce sizeable ripple with the same output energy storage because of amplitude modulation from the response of the resonant circuits and because the frequency of this secondary modulation is typically much slower than the base carrier frequency.

A motivation of this thesis is to develop methods to increase power delivery while decreasing the peak spectral amplitude of the magnetic field through the use of *direct-sequence spread spectrum* (DSSS) techniques. From a power electronics perspective, it is desirable to transmit power using a switched-mode as opposed to a linear transmitter and in particular at higher frequencies, a resonant topology with zero voltage

switching. We introduce a variant of minimum shift keying (MSK) where the voltage levels are ternary (three-level) with positive and negative half-sine pulses with variable zero durations generated by a variant of an inverse (or current mode) class D amplifier (D^{-1}). The application to a classic two-quadrant D^{-1} amplifier is demonstrated, along with a discussion of a new four-quadrant topology that enables a wider spectral spread. The tradeoff is that most of the spread spectrum power is delivered at lower frequencies than the switching frequency, but this is analogous for example to PWM sine wave inverters for motor drives where the design objectives outweigh the tradeoff. The other tradeoff is that during the zero voltage duration in the modulation, no real power is delivered, but current is carried, resulting in additional conduction losses in the transmitter. In applications, such as in biomedical and wearable devices, where receiver efficiency along with low electromagnetic interference is heavily weighted, a tradeoff in transmitter performance (size, complexity, efficiency, or cost) can be appropriate.

2.1 Spread-Sequence Optimization

There are different possible objectives for the optimization of spread-sequences. These include better correlation properties for decreased multiple access interference in communications [19, 29], among others. While better embedded communications may ultimately part of a multi-objective goal in wireless power transfer, the goal in this thesis is to maximize the amount of power that can be transferred for a given amount of electromagnetic interference.

2.1.1 Optimization Based on Standards for Electromagnetic Interference

The magnetic field is proportional within a geometric factor to the total ampere-turns of the wireless power transformer,

$$\oint H \cdot dl = NI = (N_p I_p + N_s I_s) (1 - k) \quad (2.1)$$

where I_p and I_s are the primary and secondary currents, respectively, and N and I are the effective turns ratio and current, respectively, if the coils were approximated as collocated. At perfect coupling, the coupling coefficient $k = 1$, the ampere-turns cancel, but in a near-field wireless charging system where typically $k = 0.01$ to 0.1 ,

most of the flux is uncoupled, representing a finite ampere-turns sum, which is considered spurious. Collocation is the equivalent of only considering the dipole term of the multipole expansion [52], which is a good approximation at more than several radii away, which is typically where EMI is measured (e.g. 3 m).

A useful figure of merit is the ratio of the output power P_{out} to the product of the maximum spectral interference,

$$\mathcal{Z} = \frac{k}{1-k} \frac{P_{out}}{(N_p I_{pf} + N_s I_{sf}) V_{pf}}, \quad (2.2)$$

where I_{pf} , I_{sf} , and V_{pf} are the peaks in the spectrum of primary and secondary currents and the primary voltage, respectively, at a specified resolution bandwidth (RBW) (e.g. 10 kHz for CISPR11 [75]). The assumption is that the primary and secondary coils are the same radius, but (2.2) can be modified with geometric factors to take differences in to account.

For example, many wireless power receivers use a parallel resonant circuit topology with a transmitter operating at the resonant frequency; for these single-frequency resonant systems, as $Q \rightarrow \infty$ for an optimistic bound, $\mathcal{Z} \rightarrow 1$. For the same wireless power transformer, a spread-spectrum system does much better, as we show below.

EMI standards typically specify interference limits based on a quasi-peak metric [16] for the spectrum, but the implementation and measurement process is involved and time-consuming. Even a simulated, or approximate version becomes computationally intensive. However, using peak spectral magnitudes in the optimization objective functions is a conservative estimate, which is the approach we employ.

In CISPR 11 described in §1.2.2, the magnetic field limits drop linearly over the 1 MHz–20 MHz, which is the frequency range of interest for the system in this thesis. From Maxwell's equations

$$\begin{aligned} \oint \mathbf{H} \cdot d\mathbf{l} &= NI && \text{(Amp-Turns)} \\ \mathbf{B} &= \mu_0 \mathbf{H} && \text{(Magnetic Field)} \\ \phi &= \int \mathbf{B} \cdot d\mathbf{A} && \text{(Magnetic Flux)} \\ V &= -\frac{d\phi}{dt} && \text{(Voltage),} \end{aligned}$$

the voltage is proportional to the derivative of the H-field. Hence, over this pertinent frequency range, a voltage spectrum with an appropriate constant magnitude will stay within regulatory limits.

2.1.2 Optimization Strategy

Several objective functions are possible because both electric field and magnetic field limits may be pertinent depending on EMI standards. This means that objective functions may involve both voltage and current on the primary and secondary WPT inductors. As implied previously, it is worthwhile to note that current is the integral of the voltage across the WPT inductors.

A path towards optimizing a system for wireless power transfer.

1. Find optimal input voltage spectrum and linear system approximation of band-pass rectifier by optimizing together.
2. Optimize t-MSK spread sequence so the spectrum resembles the results from Step 1.
3. Optimize bandpass rectifier so it matches (in the objective function sense) the spectrum from Step 2.

In our application, the possible voltage spectra is constrained in theory by the shape of the pulse (half-sinusoid) and in implementation by the constraints on the inverter. As a strategy, we chose in the sequence optimization to minimize to the peak-to-rms ratio of the primary voltage spectrum; in the design of the bandpass rectifier, to minimize the total amp-turns, which represents the total uncoupled and therefore spurious magnetic field. In general, to capture the most power from the transmitter, the bandpass spectrum of the rectifier should match the receiver. Several receiver architectures exist. For example, multiple narrower band receivers can spectrum slice the spread power from the transmitter; in the case of a passive bandpass rectifier, the optimization would be for a specified order¹ rectifier.

Other choices are possible for transmitter sequence objective, such as a linear weighting on the primary voltage spectrum to minimize the spectral of the current, or perhaps a more complicated function. The methods discussed still apply, with maybe higher computational cost.

Optimization was performed using a genetic algorithm followed by a pattern search on the Global Optimization Toolbox in MATLAB. These optimization tools can handle a wider variety of problems including mixed integer and complicated objective functions, which are in general non-convex, yet pertinent for our problem. Although there are no guarantees of finding the global maximum, these tools have been well used in both sequence design in communications [21] and resonant circuits [20, 112].

¹Analogous to bandpass filter order.

2.1.3 Sequence Optimization Structure

Genetic algorithms and often pattern searches typically require a large number of function evaluations, which also typically increase with the number of optimization variables along with the size of the search space.

While a ternary sequence with fixed zero durations might be optimized directly over $\{-1, 0, 1\}$ because of a smaller search space, it may be advantageous to choose a more efficient representation in optimizing variable zero duration sequences.

If we choose the following representation for an MSK sequence consisting of alternating non-zero $\{-1, 1\}$ and variable zero durations,

$$\{p_1, z_{1,1}, \dots, z_{1,l}, \dots, p_n, z_{n,1}, \dots, z_{n,k}\} \quad (2.3)$$

where p_i are indices to a dictionary of well-formed subsequences of length k and $z_{i,j}$ are the corresponding zero durations. The subsequences are well-formed in the sense that they satisfy the constraints, for example those imposed by the inverter implementation, or spectral by bounding the run-length of patterns or polarities.

2.1.4 Sequence Objective Functions

The objective function used for sequence optimization in this chapter, which minimizes the ratio of the spectral peak to rms power in the signal is derived from (2.2)

$$\underset{x_i, z_{i,j}}{\text{minimize}} \quad \max_k \frac{W(x_i[n], z_{i,j}[n])}{p(x_i, z_i)} \quad (2.4a)$$

subject to

$$x_i \in D, \quad (2.4b)$$

$$z_{i,j} \in Z_d, \quad (2.4c)$$

$$\sum_{i,j} z_{i,j} = z_t, \quad (2.4d)$$

where the objective function Z_s in 2.4a is given by

$$W[k] = \left| \mathcal{F}_k \left(\bigoplus_i (x_i[n] \Pi z_i[n]) \right) \right| \quad (2.5)$$

$$p(x_i, z_i) = \frac{n(x_i)}{n(x_i) + \sum_j z_{i,j}}. \quad (2.6)$$

Note that \mathcal{Z}_s behaves reciprocally to the original \mathcal{Z} in (2.2) so as to form a minimization problem. x_i are subsequences chosen from dictionary D and $z_{i,j}$ are the corresponding constrained zero durations from set Z_d ; $z_{i,j}$ are normalized to unity pulse duration. These zero duration constraints may impose minimum and maximum allowable durations, and in the examples discussed below, are integer multiples of a base duration, which is imposed by the digital controller implementation. For example, the inverter constraints might include volt-second limits, which constrains the possible pulse patterns.

The explicit constraint on $z_{i,j}$ that is expressed in (2.4d) fixes the *duty-cycle* of the sequence. Without this constraint, the duty-cycle can still be implicitly be bounded by bounding $z_{i,j}$. For example,

$$\begin{aligned} a < z_{i,j} < b \\ \Rightarrow \quad Na < z_i < Nb, \end{aligned}$$

where $a, b \in \mathbb{R}^+$ in principle, but in practical implementations such as a digital controller, $a, b \in \mathbb{Z}^+$.

$W[k]$ is the magnitude of the discrete Fourier transform \mathcal{F}_k of the sampled time signal formed by the concatenation \uplus of the time domain construction \mathbb{I} of the subsequences with their corresponding zero durations. $p(x_i, z_i)$ is the number of non-zero entries in $W[n]$ added to the sum of zero durations. This is proportional to the signal rms because each half-sine wave pulse has a fixed rms value, so calculating the total portion of time that the pulses occupy is all that is required.

It is important, however, that in the evaluation of the objective function, the peak spectral amplitude that is computed is pertinent. This means that the sampling frequency must satisfy the RBW of the germane EMI standard. For example, CISPR22 with a 10 kHz RBW and a half-sine wave pulse period of 100 ns, requires 10^3 samples per period; this sampling rate is purely for computation of the objective function and should not be confused with an actual implementation in a spectrum analyzer. Another key consideration is that the most efficient algorithm for the discrete Fourier transform is a Fast-Fourier Transform (FFT) on sample lengths which are a power of 2. The typical approach to non-aligned signals is to pad with zeros, but in comparing trial sequences of different lengths, this can bias the estimation and hence comparison of the peak spectral amplitude [77]. One can reduce this estimation bias by over-padding the longest possible sequence by several factors of two so that the ratio of the difference in padding between shortest and longest sequences to the average

zero padding is smaller.

For example, in a sequence consisting of 100 ns pulses with zero durations ranging from 15 ns to 100 ns in 5 ns steps, a sequence with 10^3 pulses results in a worst-case sequence period below the RBW of 10 kHz. A fixed sample length which is a power of 2 to accommodate the fastest FFT evaluation is chosen to have an overpadding factor of 4 for the worst-case sequence sample length.

A fortunate consequence of fixing z_t explicitly is that all trial sequences will have the same sample length. This means that padding to the nearest larger power of two is all that is necessary and overpadding to a possible worst case is no longer necessary.

Fortunately, genetic algorithms can be parallelized well. This feature is realized in the Global Optimization Toolbox in MATLAB. The optimizations were performed on a 16-core compute-optimized instance using cloud computing.

2.1.5 Genetic Algorithm

A genetic algorithm (GA) was chosen for sequence optimization for several reasons. GAs are suited for non-convex optimization, highly parallelizable, and easily customizable for a variety of nonlinear constraints. There are a number of examples of its successful use in sequence optimization including [19, 53, 71].

In essence, the algorithm amounts to the simultaneous optimization of two sequences: the sequence of polarities P and the sequence zero durations Z . $P = \{p_1 p_2 \dots p_L\}$ is a binary sequence where L is the length of the sequence and $p_n \in \{-1, 1\}$.

Specific Hardware Constraints and Dictionary Construction

Several constraints are imposed on P . For wireless power transfer with an output inductor, the relevant constraints are:

Zero Total Flux:

$$\sum_{n=1}^L p_n = 0. \quad (2.7)$$

Bounded Flux Excursion:

$$\left\| \sum_{n=k}^l p_n \right\| \leq \phi_1, \quad \forall k < l, l \leq L. \quad (2.8)$$

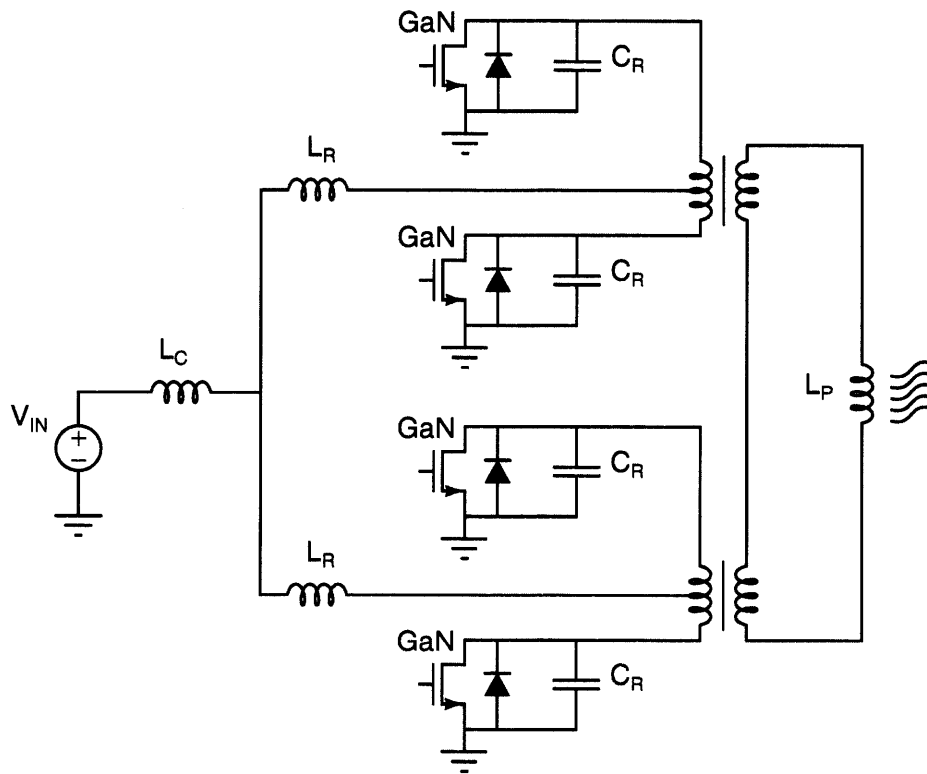


Figure 2-1: Quad-Switch Push-Pull Amplifier

Table 2.1: Switching Pattern.

| | | I_n | |
|-------|----|--------------|--------------|
| | | + | - |
| p_o | +1 | (0, 1, 1, 1) | (1, 0, 1, 1) |
| | 0 | (1, 1, 1, 1) | (1, 1, 1, 1) |
| | -1 | (0, 1, 0, 1) | (0, 1, 1, 0) |

Although the quad-switched push-pull (QSPP) topology is introduced in Chapter 3, we will have to examine it to understand the constraints its operation imposes on the spread pattern. If we scrutinize Figure 2-1, additional constraints are needed for the application of voltage to the transformers. The four switch states (S_1, S_2, S_3, S_4) depend on the desired output polarity $p_o \in \{-1, 0, 1\}$ and the inductor current polarity I_n as shown in Table 2.1, with $S_k = 1$ and $S_k = 0$ corresponding to ON and OFF, respectively.

Note that nonzero voltages with positive I_n current correspond to flux increment on top transformer T_1 and negative currents to bottom transformer T_2 . In §3.4.2, the QSPP amplifier operates so that the current alternates on every non-zero polarity and holds on every zero polarity (zero duration). If every sequence on every repetition is programmed to begin with positive I_n , then every *odd* n corresponds to transformer T_1 and every *even* n to transformer T_2 .

The logical next step is to also constrain the flux in the transformers similarly to that of the output inductor so that:

Zero Total Flux:

$$\sum_{n \text{ odd}} p_n = 0, \quad (2.9)$$

$$\sum_{n \text{ even}} p_n = 0. \quad (2.10)$$

Bounded Flux Excursion:

$$\left\| \sum_{n=k}^l p_n \right\| \leq \phi_2, \quad n, l, k \text{ odd}, \quad (2.11)$$

$$\left\| \sum_{n=k}^l p_n \right\| \leq \phi_2, \quad n, l, k \text{ even}. \quad (2.12)$$

These constraints impose the condition that the length L of any non-trivial se-

quence be a multiple of 4.

A difficult and computationally prohibitive approach is to perform an optimization directly on the full sequence with each member p_n as a degree of freedom and then imposing the constraints with perhaps a sieve. A more tractable alternative, albeit reduced search space, is to perform the optimization over a dictionary of subsequences which satisfy the constraints to construct the full subsequence.

So, let $P = \{p_1 p_2 \dots p_N\}$ be constructed from subsequences p_n of length L_p satisfying constraints (2.7, 2.8, 2.9, 2.10, 2.11, 2.12) . It is clear that L_p must also be a multiple of 4 and that if each p_n satisfies the constraints, then full sequence P must also satisfy these constraints.

The set of subsequences p_n that satisfies a particular set of constraints that extend to the construction of the full sequence constitutes a dictionary D and each subsequence is considered *well-formed*.

The portion of the *genotype* that corresponds to the nonzero polarities is encoded as an index n to an entry in D . Each nonzero polarity has a corresponding zero duration, which is encoded as an integer multiple of some base duration². Together the representation of the *phenotype* appears as:

$$g_k = \{p_1, z_{1,1}, \dots, z_{1,L_p}, \dots, p_N, z_{N,1}, \dots, z_{N,L_p}\}_k. \quad (2.13)$$

Sequence Objective Functions

Each phenotype is converted to the time domain representation $g_k \rightarrow g_k(t)$ of half-sine pulses. The spectral peak is obtained from the Fast Fourier Transform (FFT) of $g_k(t)$. Sampling is performed at the rate that is appropriate for the implemented pulse duration and required resolution bandwidth. It is well-known that the FFT performs the most efficiently at sample lengths that are powers of 2, hence a conservative and more computationally efficient approach is to zero pad to the next higher power of 2.

Although not proven here, the supposition that the spectrum spreading figure of merit Z_S steadily improves with a greater range of zero durations is assumed. To properly constrain the optimization, the sequence duty cycle D_s must be fixed. The sequence duty cycle is defined as portion of time occupied by the half-sine pulses in the sequence,

$$D_s = \frac{LT_p}{LT_p + \sum_{n,k} z_{n,k}}, \quad (2.14)$$

where T_p is the duration of the half-sine pulse.

²In practice is determined by the digital controller implementation.

A fortunate consequence of fixing D_s is that all the phenotypes (population members) will have the same number of samples in the calculation of the FFT, hence eliminating sample-size effects in the calculation of the figure of merit Z_s .

Examples in the following sections use a dictionary with subsequence lengths of 16 and with unit flux excursions constrained to be no larger than 2. This D_{16} dictionary was constructed by exhaustively testing the 2^{16} possible subsequences for constraint satisfaction.

2.1.6 Custom Genetic Algorithm Functions for Explicitly Fixed Duty-Cycle

Although the MATLAB Global Optimization Toolbox is used for the genetic algorithm (GA) implementation, several custom functions used by the GA were needed because of the constraints imposed by the zero duration sequence.

The constraints to the zero durations described in §2.1.4 for fixed duty-cycle are partly linear constraints

$$\begin{aligned} \mathbb{1}^\top \mathbf{x}_k &= s \\ \mathbb{1}a \preceq \mathbf{x}_k \preceq \mathbb{1}b \\ a, b, s &\in \mathbb{Z}^+. \end{aligned} \tag{2.15}$$

The additional difficulty occurs in that the elements of \mathbf{x}_k are required to be positive integers.

Population Creation Function

The initial population in a genetic is drawn from a random distribution. The creation of an initial population for the polarity sequence \mathbf{P} is relatively straightforward as the dictionary indices are drawn from a uniform integer distribution that spans the number of entries. The creation of a sequence of zero durations \mathbf{Z}_d is actually more involved.

Three parameters must be specified: the minimum and maximum of each zero duration and the total sum. For these parameters to be described all at once, the whole \mathbf{Z}_d sequence must be drawn from the distribution with the three parameters considered as the *support*. This is reminiscent of the Dirichlet distribution [57], but

with arbitrarily chosen support,

$$\begin{aligned}
 v &= v_1, v_2, \dots, v_n \\
 \text{where } v_k &\in [a, b], \\
 \sum_n v_k &= s, \\
 a, b, s &\in \mathbb{Z}^+
 \end{aligned}$$

The sequence generation with this distribution ‘randfixedsum()’ was reported and coded by Roger Stafford in MATLAB Central [105]. The generated vectors from ‘randfixedsum()’ are quantized using ‘round()’ and the resulting quantization error (i.e. integer remainder) is spread randomly over the sequence. The MATLAB function to create the initial population for zero durations is listed in Appendix D.2.

Crossover Functions

The crossover function used for the polarity sequence indices is the default MATLAB function ‘crossoversscattered()’ [70]. A random vector v , which is the same length as the parents. A ‘1’ entry selects genes from the first parent $p1$ and a ‘0’ selects from the second parent $p2$ to form a child $c1$. For example:

$$\begin{aligned}
 p1 &= [a \ b \ c \ d \ e \ f \ g \ h] \\
 p2 &= [1 \ 2 \ 3 \ 4 \ 5 \ 6 \ 7 \ 8] \\
 r &= [1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0] \\
 c1 &= [a \ b \ 3 \ 4 \ e \ 6 \ 7 \ 8].
 \end{aligned}$$

For the zero duration sequences, ‘crossoverintermediate()’ which is included with MATLAB is used. The average of two parents are used to create a new sequence. This results in non-integer elements in this new sequence. The elements are rounded using round() and the error in the sum (which is an integer) is spread randomly through the sequence to create a child that satisfies the constraints in (2.15) as well as positive.

The complete crossover function, which incorporates both the polarity sequence and zero duration crossovers is listed in Appendix D.3.

Mutation Functions

The mutation function for the polarity sequence is the included MATLAB function ‘mutationuniform()’ [70]. The algorithm first selects polarity sequence elements to be replaced at some mutation probability rate that is specified. Recall that the elements in the polarity sequence are indices from a dictionary of subsequences. The elements that are selected are replaced by a random number from a uniform distribution over the range of allowed indices.

The mutation function for the zero duration (ZD) sequence is similar to ‘mutationuniform()’. Elements of the ZD sequence are similarly chosen at random to create a deletion set. The important difference is that the replacement set is chosen to have the same sum as the deletion set; this preserves the sum of the ZD sequence. ‘randfixedsum()’ is also used to create the replacement set with the result similarly quantized and remainder spread over the sequence as in the population creation function.

The complete mutation function, which includes both the polarity sequence and zero duration is listed in Appendix D.4.

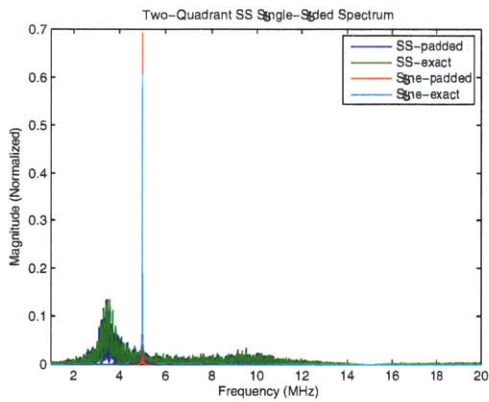
2.2 Results of Spread-Sequence Optimization

Several results are presented below, which are representative of different types of numerical trials. Results are shown for sequence optimization with implicitly bounded duty-cycle and for explicitly fixed duty-cycle.

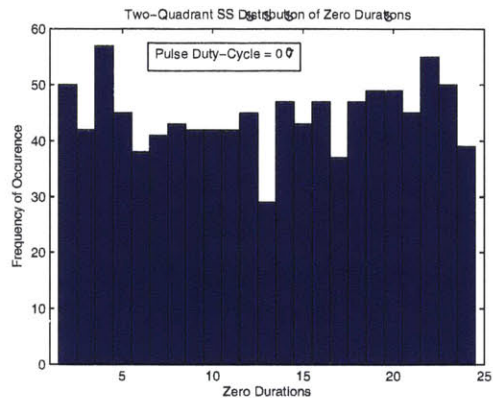
2.2.1 Implicitly Bounded Duty-Cycle

In Figures 2-2a and 2-2c the power spectrum of an equivalent single-frequency sine wave is spread over a two-quadrant (strictly alternating polarities) and four-quadrant (arbitrary polarities) sequence, respectively; the sequence length is 1024. One can observe that the four-quadrant sequence has better spreading than the two-quadrant and this is reflective of the additional degrees of freedom offered by the arbitrary polarity. Two-quadrant sequences can be implemented with a conventional D^{-1} amplifier and four-quadrant sequences with a quad-switched push-pull amplifier, both of which will be discussed in Chapter 3.

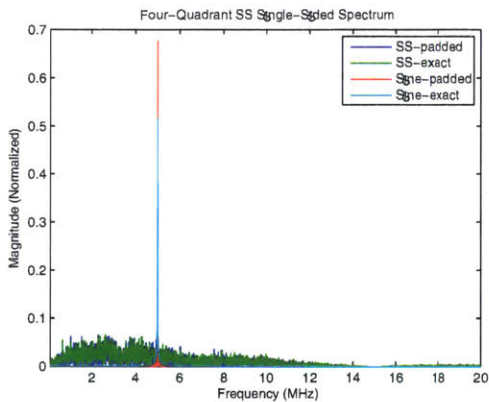
Figures 2-2b and 2-2d show the distributions of zero durations. Each zero duration is 1/30 of a single pulse duration. The zero duration distribution is representative of different optimization trials in that the zero durations distribute roughly uniformly over the bounded interval.



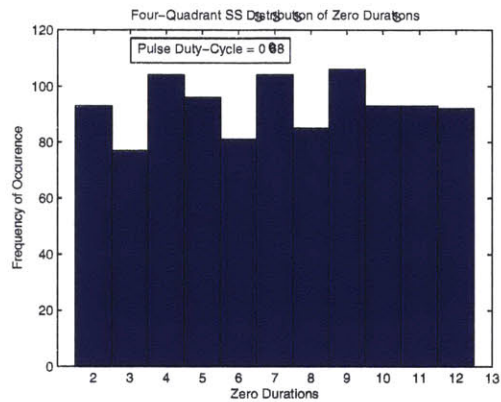
(a) Two-Quadrant Spectrum



(b) Two-Quadrant Zero Duration Distribution



(c) Four-Quadrant Spectrum



(d) Four-Quadrant Zero Duration Distribution

Figure 2-2: Spread-Spectrum Sequence Optimization Results

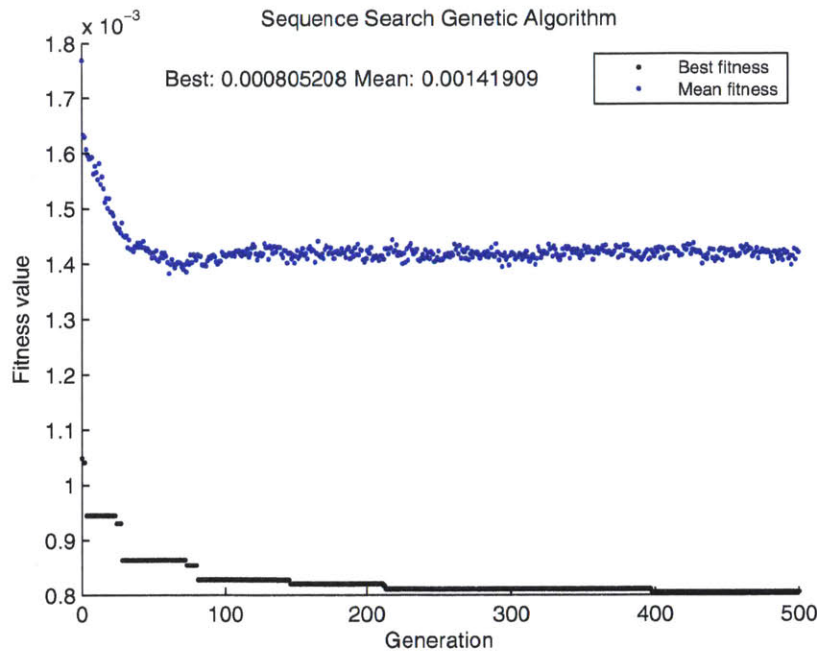


Figure 2-3: Genetic Algorithm Optimization

Figure 2-3 shows the progression of the GA optimization, which is typical; the salient feature of this plot highlights the advantage of a GA over a purely random sequence design because even the average population is over factor of two worse than the best GA result for any given generation.

2.2.2 Explicitly Fixed Duty-Cycle

The imposition of a fixed duty-cycle constraint along with the development of algorithms to do so was undertaken to both improve the accuracy and accelerate the sequence optimization. Accuracy is improved by comparing candidate sequences with the same base sample length and zero-padding, which meant a consistent calculation of the objective function. Sequence optimization was accelerated because of the reduced processing from the shorter sample length as over-padding for varying base sample length was no longer necessary. This improved computational efficiency allowed a longer sequence length to be optimized: 2048 from the previous 1024.

A result of this optimization, illustrated in Figure 2-4 shows that the ratio of the highest peak of the spread spectrum is over 16 times lower than that of a single-frequency sine wave with the same average power. The FFT spectrum was calculated with a 9 kHz RBW (resolution bandwidth), which is specified for CISPR22 between

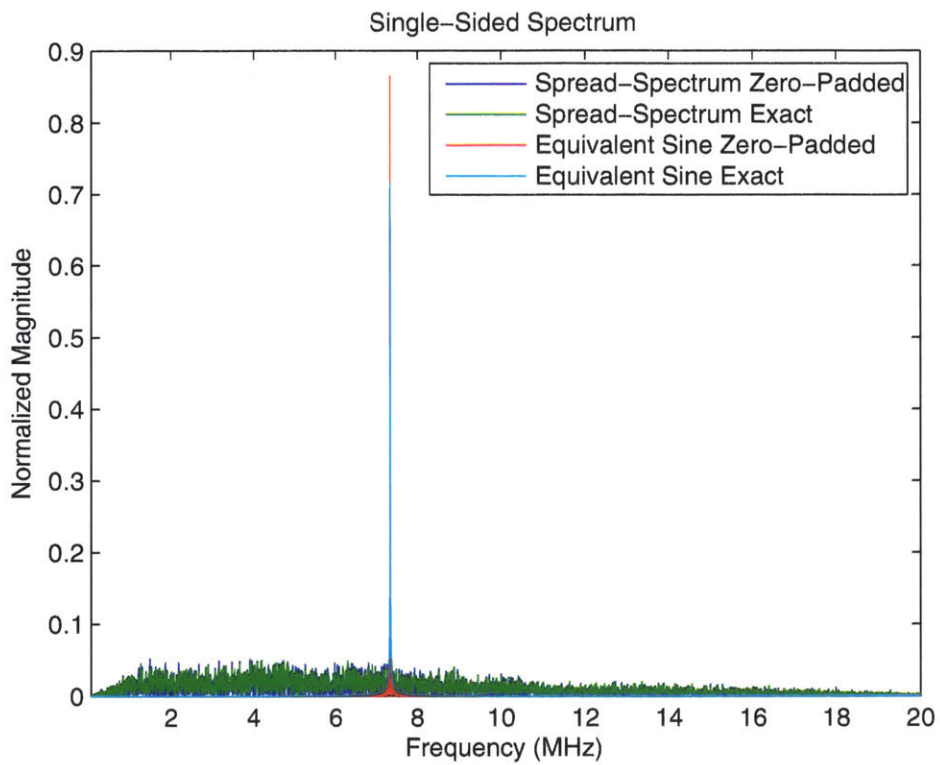


Figure 2-4: Exact FFT of spread-spectrum sequence (RBW = 9 kHz). Note that the sine wave frequency 7.35 MHz is not a multiple of 9 kHz. Magnitude is normalized to unit spread spectrum pulse amplitude. Spread spectrum pulse-duty of 0.75 is included in the calculation of the equivalent single-frequency sine wave.

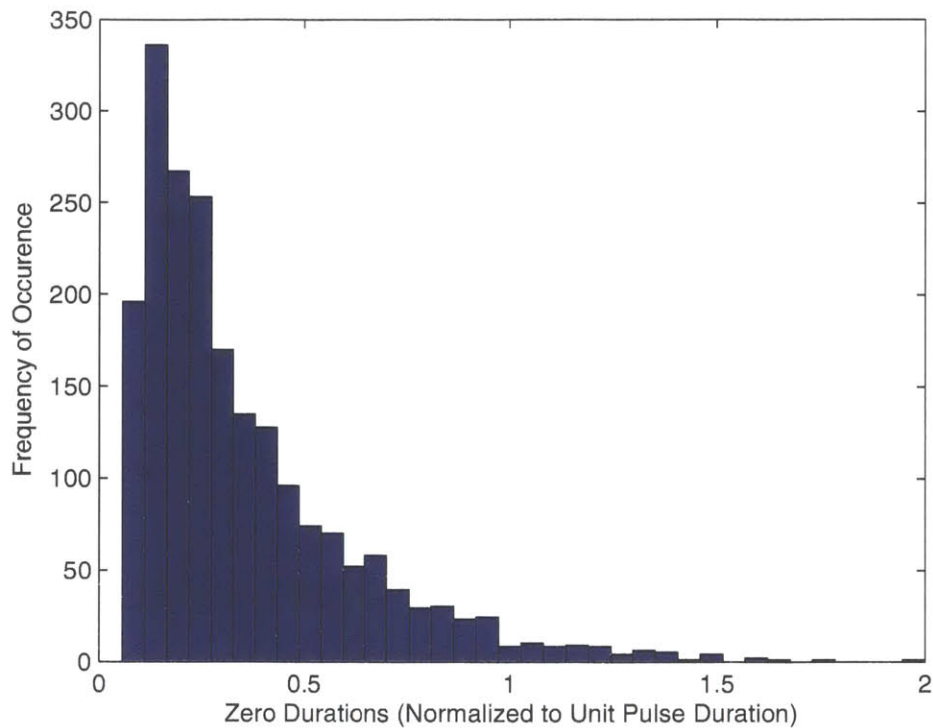


Figure 2-5: Histogram of the zero durations for unit pulse duration. The sequence optimization was constrained to a pulse duty-cycle of 0.75.

150 kHz and 30 MHz.

The pulse-duty of 0.75, among other optimized spread sequences, was a tradeoff between a higher spreading figure of merit (average power ratio to spectral peak) and lower conduction losses from current-carrying, zero-voltage durations. A histogram is shown in Figure 2-5 of the distribution of zero durations when the total zero duration is constrained in the optimization. The time resolution of 1/18 of a single-pulse duration is due to the practical constraints imposed by the FPGA implementation of the controller in Chapter 3.

A comparison of the EMI figure of merit is shown in Figure 2-6 for various optimization trials. Longer spread sequences along with lower sequence duty-cycles result in lower EMI. Lower duty-cycles trade off efficiency in the QSPF amplifier described in Chapter 3 because zero durations represent current conduction losses without an offsetting transfer of energy.

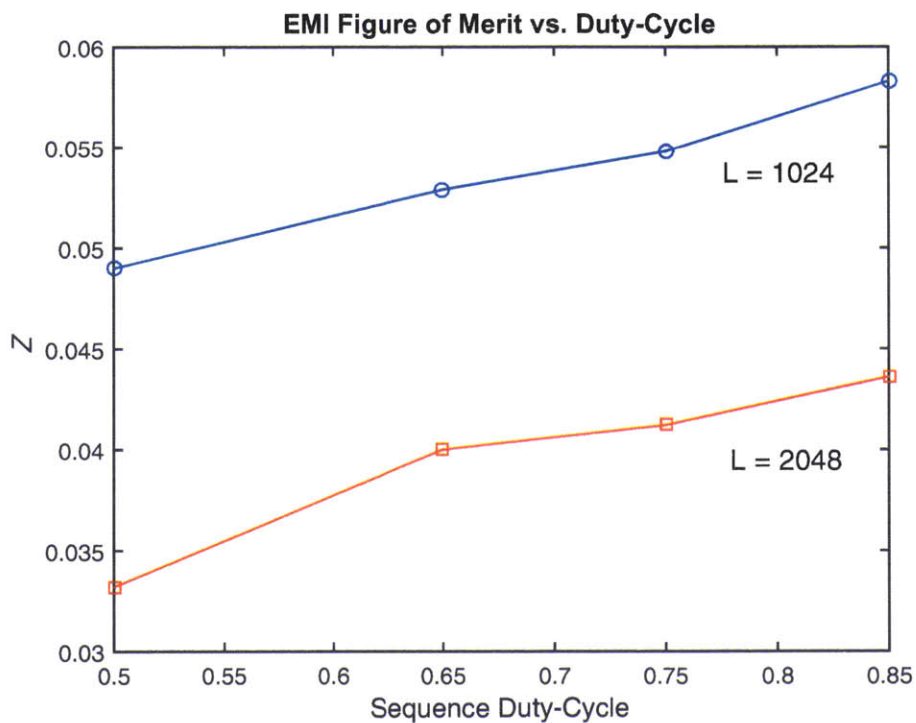


Figure 2-6: EMI Figure of Merit Z as a function of Sequence Duty-Cycle D and Sequence Length L .

2.3 Chapter Summary

A modulation method along with the construction and optimization of a sequence to spread energy for wireless power transfer over a wide frequency band. This modulation method along with the sequence construction is affiliated with the quad-switched push-pull amplifier (QSPP), discussed in the next chapter, to realize ‘resonant, yet spread-spectrum’.

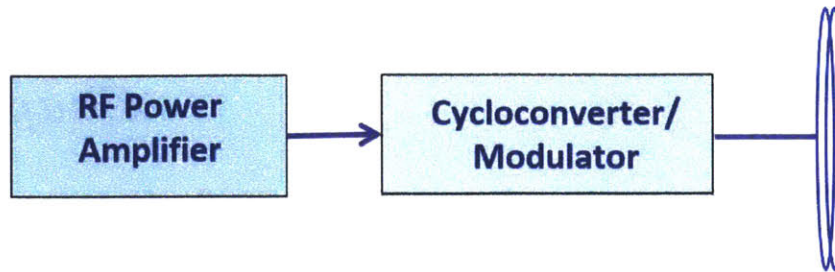
Chapter 3

Hardware for Spread Spectrum Wireless Power Transfer

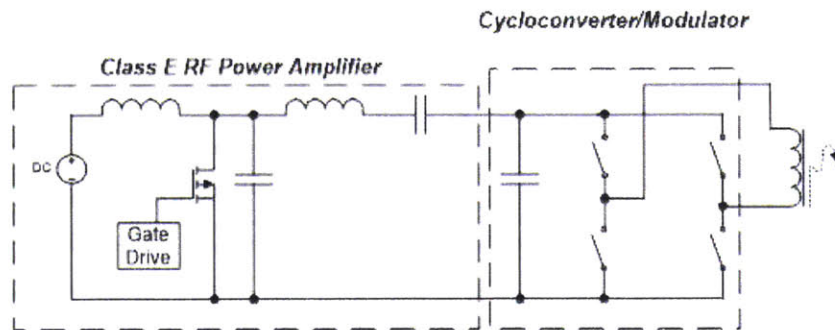
M IRED in the imperfections of corporeal electronic circuits, one must nevertheless excogitate a way to efficiently transform a constant voltage to spread spectrum energy only to as efficiently transform it back again. The greatest challenges for the transmitter lie in the semiconductor switches and the magnetics—in the receiver, in the extraction of as much power as possible from a source spread over a broad band using only passive components and asynchronous switches.

The crux of the transmitter problem lay in creating pulses of energy at arbitrary times without the entailing losses that are typically inherent in the function of a semiconductor switch. The dominating loss is from turning on because energy is stored across the voltage blocking terminals in an intrinsic capacitance. This *switching loss* can only be eliminated if the switch is activated when there is no voltage across its terminals—this can only happen if the terminal voltage varies in time even when the switch state does not change. There is an abundance of literature where this circumstance can be imposed by interposing the switch within a resonant circuit.

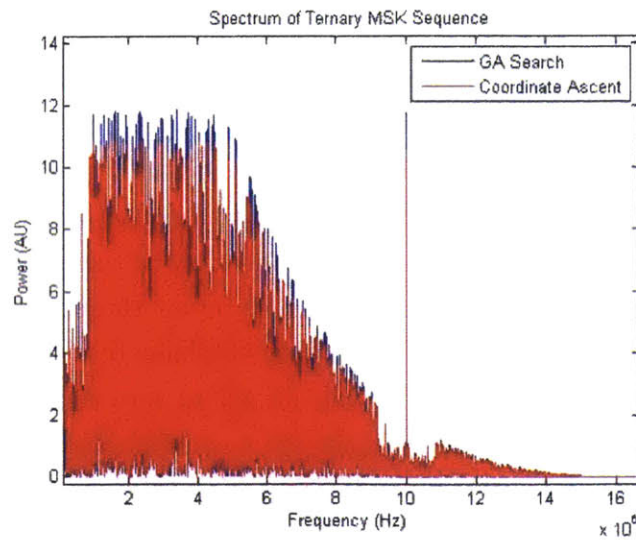
While it is clear that the wireless transfer of power through a magnetic field is accomplished by modulating a current, the small epiphany that this can be performed by pulses of voltage to yield a spread spectrum allows *zero voltage switching* (ZVS). The half-sine pulses in the previous chapter are a consequence of using the switched resonant circuits described in this chapter, hence the expression ‘spread-spectrum yet resonant’. Not only does the transmitter hardware dictate the shape of the voltage and current, but it also imposes constraints on the allowed patterns and timings of positive, negative, and zero polarities. The restrictions on patterns and timings are both architectural and topological. An example of an architecture that imposes a timing constraint is illustrated in Figure 3-1a. The figure shows a continuous sine



(a) Two-stage spread spectrum modulation based on traditional cycloconverter.



(b) Class E amplifier followed by a cycloconverter for arbitrary polarity output.



(c) GA-optimized spectrum, fixed zero duration.

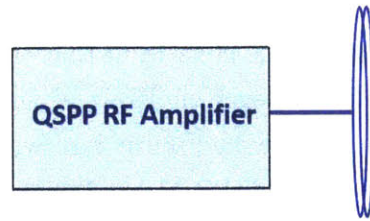
Figure 3-1: Fixed Zero-Duration Spread-Spectrum Transmitter

wave generator, possibly a class E amplifier, followed by cycloconverter, which in principle could be the full-bridge illustrated in Figure 3-1b. It is clear that continuity in the sine wave generator imposes the constraint that the zero durations (polarities) have a period that is a positive integer multiple of the sine wave half-period. A representative spectrum is illustrated in Figure 3-1c with a tone at the half-period frequency saliently observable. In addition to the limitations to spectrum spreading, a full bridge within a transmitter operating at high frequency (>1 MHz) at relatively high voltage (>100 V) is likely impractical because of the require floating gate drives.

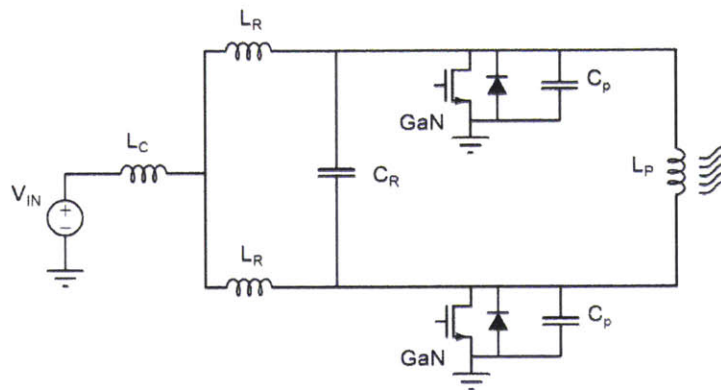
The onerous constraint of alternating positive and negative polarity is imposed by a conventional D^{-1} amplifier in Figure 3-2b. This amplifier, however, has the degree of freedom of arbitrary zero duration between the polarity bumps/pulses, hence providing an opportunity for spreading the spectrum. The spread bandwidth is proportional to the duty-cycle and if we assume the dominant mechanism for loss is resistance to conduction, then the tradeoff between efficiency and duty-cycle is affine. The D^{-1} amplifier has a number of favorable features. These include ZVS, ground-referenced switches and hence gate drives, and a peculiar ability to *freeze all the states*. The operation and analysis of the D^{-1} amplifier is discussed in the ensuing section, but in short, because switches change state at zero voltage, maintaining the overlap so that both switches are on at the same time results in the inductor holding its current value along with enforcing the voltage across all the capacitors to be zero. This architecture in Figure 3-2a is single-stage.

In §3.4 shown in Figure 3-2c, a spread-spectrum amplifier, which is spawned from the D^{-1} amplifier along with the need for arbitrary polarity, is developed and discussed. This *quad-switched push-pull* (QSPP) amplifier has the freedom of arbitrary zero duration and almost any polarity pattern—the constraints on polarity are now imposed by the flux one is willing to levy on the magnetics. We will see that even a small degree of this freedom (e.g. two pulse units of flux excursion in every piece of magnetics) is enough to allow a wide spread where almost all the energy is distributed nearly evenly over twice the center frequency.

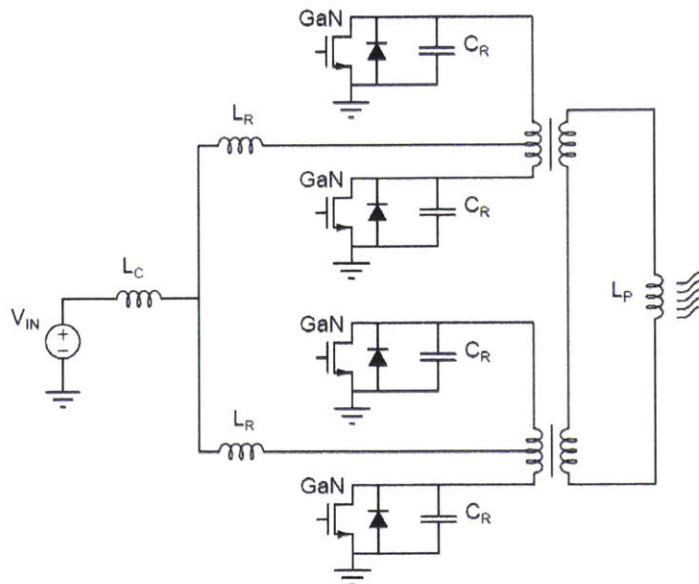
Although passive receivers were chosen to lead off the research, they ultimately exceeded the requirements for medical implants in collecting almost 2 W from a narrower band spread sequence, while remaining below regulatory limits for EMI. Another application of these narrower band, albeit higher order, passive circuits is in dividing the spectrum of a wide-spreading power transmission among multiple lower power receivers. A discussion of the analysis, modeling, optimization, and demonstration of these passive receiver circuits follows in the ensuing sections.



(a) Single-stage architecture not only combines power signal generation, but has additional degrees of freedom.



(b) Inverse/Current-Mode Class D Amplifier.



(c) Quad-Switch Push-Pull Amplifier (QSPP).

Figure 3-2: Variable Zero-Duration Transmitters

3.1 Power Amplifier Considerations

Wireless power transfer (WPT) has gained prominence in a wide range of applications that include medical, consumer, and transportation. These application spaces represent over seven orders of magnitude in power transferred, below milliwatts for some medical applications to tens of watts for consumer applications to over ten kilowatts for transportation. Frequencies span from tens of kHz to THz, and tens of kHz to GHz in medical applications.

Traditional approaches to driving wireless power transfer have used class D, class E, and class DE power amplifiers. At frequencies below 1 MHz and at lower voltages, class D amplifiers can be an attractive choice, but at higher frequencies with higher voltages suffer from prohibitive switching losses from repetitively discharging the active device capacitance because of non-ZVS (zero voltage switching) operation. Class E amplifiers as well as the class DE variant appear to be the most widely used because of zero voltage switching, which enables operating at high frequency.

High frequency operation is attractive not only because passive components are smaller, but also because power transfer inductors, which are air-core, improve monotonically in Q (quality factor) with increasing frequency [64]. It can be shown that inductor Q ultimately limits the power transfer and efficiency, especially at lower coupling levels [13].

Wireless power transfer involves the design of three elements: the transmitting inverter/power amplifier, WPT coupled inductors, and the receiver circuit. Typically the design process is involved because the performance of these three elements is highly coupled and becomes more difficult especially when operation over a range of magnetic coupling and loading is required.

We present the design and analysis of class D^{-1} (current-mode) amplifiers for wireless power transfer. D^{-1} amplifiers completely satisfy certain important requirements for wireless power transfer; class D, E, and DE amplifiers only partially satisfy these requirements:

1. Zero voltage switching for high frequency and/or high voltage operation;
2. Guaranteed zero voltage switching from full load to no load;
3. Tolerance to device removal, i.e. removal of the secondary—guaranteed ZVS; bounded currents and voltages.

Loss of ZVS at high frequencies and/or high voltages is catastrophic in most cases because device dissipation is directly proportional to the frequency and to the square

of the voltage at the switching instant. Even small deviations from ZVS can result in large power dissipation because dV/dt near the zero voltage crossing is proportional to the product of the frequency with the peak of a sinusoidal voltage. The D^{-1} amplifier is tolerant to the removal of the secondary because even in this unloaded condition, ZVS can be guaranteed and the current and voltage bounds can be designed.

Push-pull topologies help ease thermal management because dissipation is distributed over two devices instead of one, doubling power capability without increasing the effective device output capacitance or changing on-resistance. The disadvantage of double the gate drive power is often mitigated by modern devices, and in many cases a small fraction of the processed power.

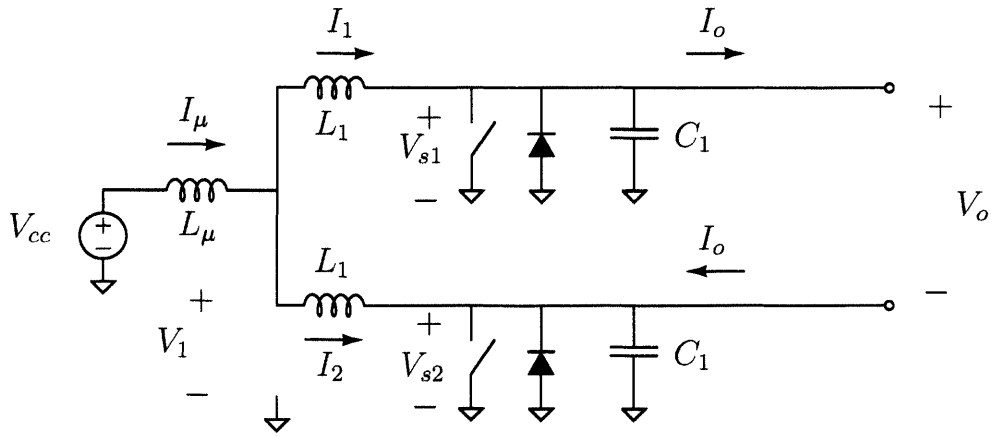
Several methods to the analysis of the D^{-1} amplifier (references) have been published based on harmonic analysis. Our approach differs in that the waveforms are derived in the time domain, which gives us a better analysis of the device stresses and component losses, leading to better device choice and/or maximizing device capability. Because the D^{-1} amplifier can be modeled at its terminals as a voltage source, the coupled inductors and the secondary resonant circuit comprise a second order system, which simplifies the analysis. A further simplification is possible for fixed frequency operation, for example within an ISM band because of regulatory restrictions for most practical transmitter power levels.

A goal of this chapter is to present an analysis of the D^{-1} amplifier with models for resonant WPT that leads to design procedures and equations in terms of physical design variables in intuitive forms, along with practical approximations for different cases. We will illustrate that the D^{-1} amplifier behaves largely as a voltage source at its output terminals if ZVS is guaranteed, which largely decouples the design of the amplifier from the rest of the system.

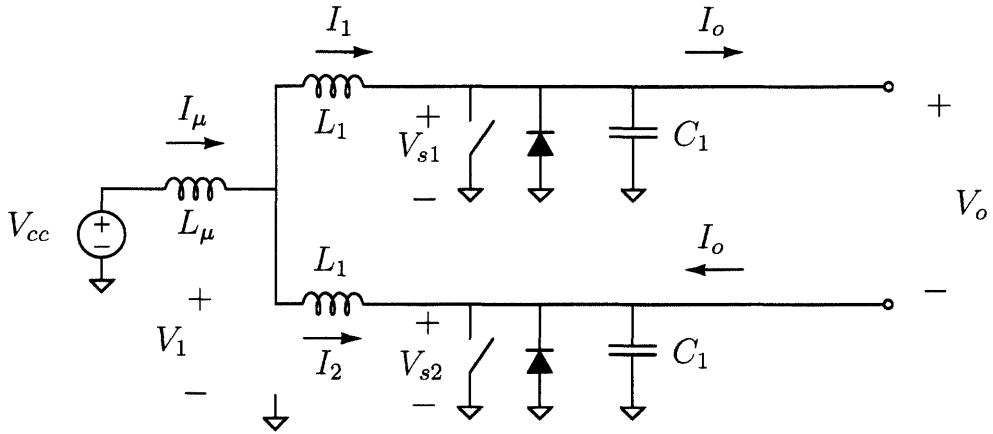
3.2 Analysis of the D^{-1} Amplifier

The typical intention for the operation of the D^{-1} amplifier is at fixed frequency with analyses in literature based on harmonic formulations [55, 92]. The calculations that follow are based on the time domain behavior of the circuit to detail the loss mechanisms and stresses. A D^{-1} amplifier with a load that consists of a series resistor and inductor is illustrated in Figure 3-4. There are several useful observations :

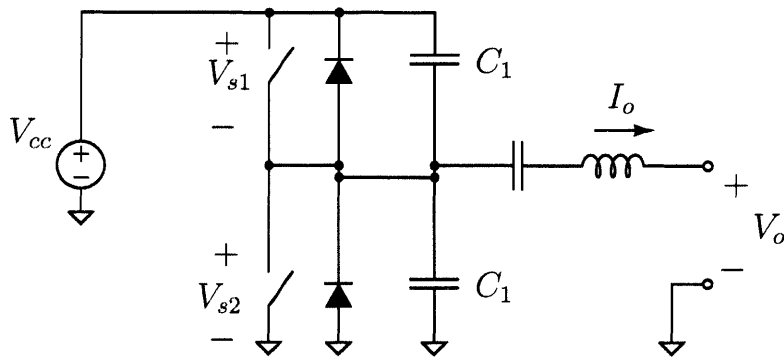
1. The average of $V_1 = V_{cc}$ because there can be no average voltage across inductor L_{μ} .



(a) Class D^{-1}



(b) Class E



(c) Class DE [56]

Figure 3-3: WPT Driver Amplifier Topologies

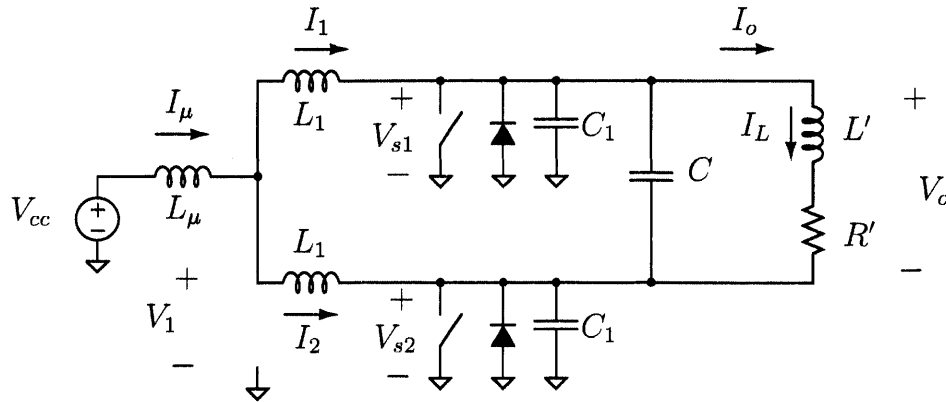


Figure 3-4: Inverse Class D with Series L/R Load.

2. $V_1 = (V_{s1} + V_{s2})/2$; V_{s1} and V_{s2} are always positive.
3. If V_o is a perfect sine wave, then $V_{o,peak}/V_{cc} = \pi$ exactly.

3.2.1 Active Device Capability

The analysis of device capability is useful from several points of view. As a manufacturer of WPT systems, one can then decide on particular capabilities and price points based on available devices. As a circuit designer, one will want to choose the appropriate devices for a specified WPT capability. For devices manufacturers, the product line for different device ratings can be tailored to target specific markets and applications spaces. These upper bounds can also be compared with other WPT driver topologies.

For WPT, the device specifications that most impact capability¹

- V_{max} —the maximum peak voltage that the device will stand off;
- $I_{rms,max}$ —the maximum rms current, which is usually a thermal limit;
- C_{sw} —the effective switch output capacitance, which is often approximated by C_{oss} .

The goal is to place upper bounds on maximum power delivery, which we will show is traded-off with operational frequency. In WPT, there are three typical modes of operation:

¹Efficiency only implicitly affects switch capability in that heating reduces a device's ability to carry rms current. Device rms current results in heating from conduction loss.

1. Fixed frequency operation at the secondary resonance ω_2 ;
2. Variable frequency tuned to the peak power point for frequency ω and load R_L ;
3. Secondary disconnected so there is no load, but the primary inductor is still connected.

The third mode can be designed to operate continuously, or momentarily until under automatic control, and in certain topologies limited by the device thermal characteristics. In the D^{-1} amplifier, the device current is usually small and corresponds to the required power to offset the losses so as to enforce that the voltage oscillation results in zero average voltage across the choke inductor.

3.2.2 Maximum Power Delivery to a Matched Resistive Load

The D^{-1} amplifier in Figure 3-4 can be modeled as a parallel resonant circuit as in Figure 3-5 under the above assumptions, where X are the reactances such that $X_L = \omega L$, $X_C = 1/\omega C$, and so forth. This transformation motivates our notion of both resonance and Q , so that

$$\omega_0^2 = \frac{1}{(L \parallel L'_p) C} \quad (3.1)$$

$$Q_0 = \omega R'_p C. \quad (3.2)$$

We assume that the secondary behaves extrinsically to obtain the peak power transfer, so that $X'_L = R'$. Under these conditions $X'_{Lp} = 2X'_L$ and $R'_p = 2R'$. In terms of D^{-1} circuit parameters,

$$\begin{aligned} L &= 2L_1 \\ C &= C + C_{sw} \\ L'_p &= 2L' \\ R'_p &= 2R' \\ Q_0 &= 2\omega_0 R' (C + C_{sw}) \end{aligned}$$

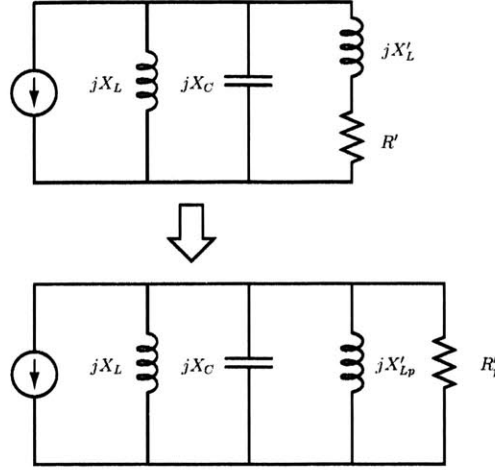


Figure 3-5: Series-to-Parallel Impedance Transformation

3.2.3 Effect of Switch Capacitance on Current Stress

Device capacitance C_{sw} increases switch stress because of the resulting current divided as illustrated in Figure 3-6a. A linear approximation the current in this region is given by,

$$i_{sw,a} = i_{\mu} + \Delta i_{sw,a} = i_{\mu} + \frac{C_{sw}}{C + C_{sw}} \frac{2}{\pi} Q_1 i_{\mu}, \quad (3.3)$$

and during switch overlap in Figure 3-6b,

$$i_{sw,b} = \frac{2}{\pi} Q_1 i_{\mu}. \quad (3.4)$$

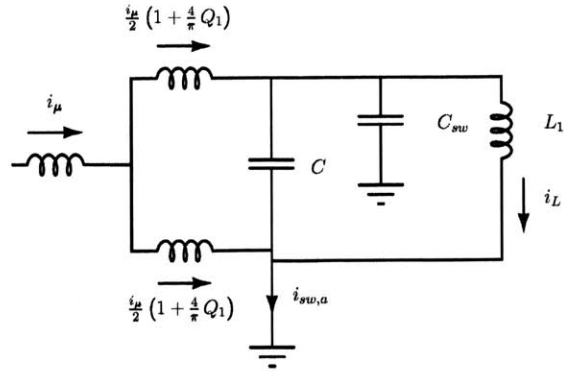
The switch rms current can be approximated piecewise linearly to be In the case of no overlap, the rms current through the switch is well approximated by

$$i_{sw,rms} = i_{\mu} \left(\frac{\gamma^2}{12} + 1 \right)^{1/2}, \quad (3.5)$$

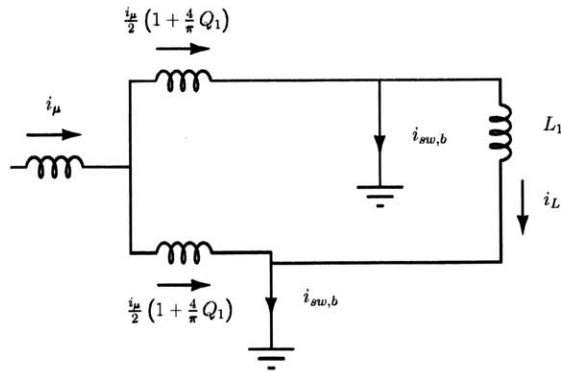
where

$$\gamma = \frac{4}{\pi} Q_1 \frac{C_{sw}}{C + C_{sw}}$$

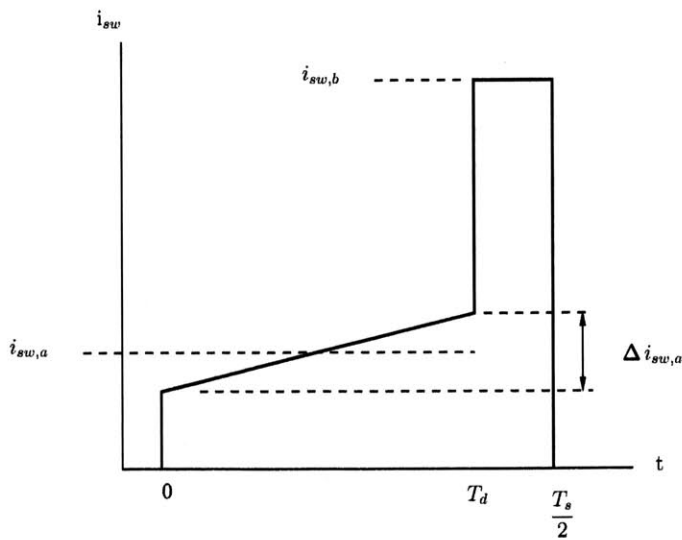
Section 3.2 : Analysis of the D^{-1} Amplifier



(a) With Device Capacitance

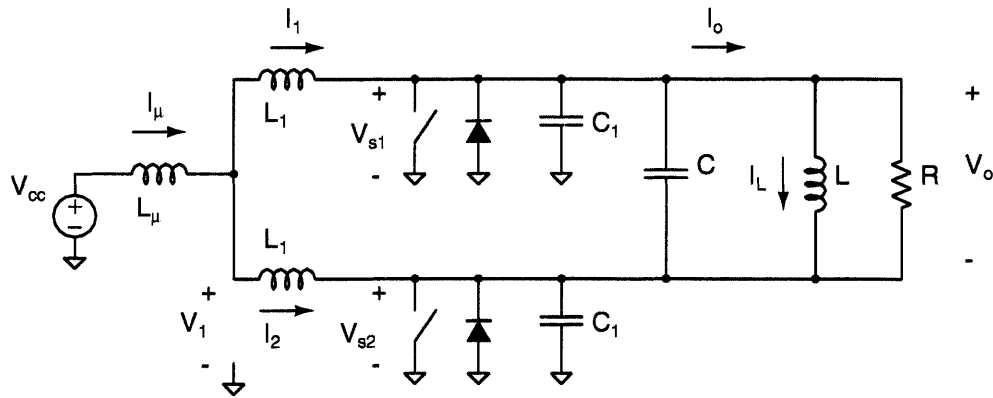


(b) Overlap

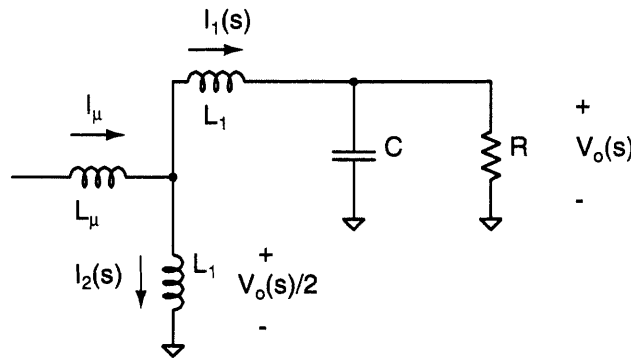


(c) Waveform

Figure 3-6: Switch Current Stress



(a) Shunt Capacitor and Parallel L/R Load.



(b) Half-Circuit

Figure 3-7: Inverse Class D Simplification

3.2.4 Derivation of Inverse Class D Equations

We assume the following in the derivation for the operation of the inverse class D amplifier illustrated in Figure 3-7a:

1. Switches and diodes are ideal with no resistance or voltage drop.
2. Switching is instantaneous with no overlap or deadtime between the two switches.
3. Zero voltage switching at the switch instance $V_0 = 0$; $V_{s1} = 0$ or $V_{s2} = 0$.
4. i_μ is constant.
5. Operation is in the periodic steady state and for this topology symmetric.

Let $V_{s2} = 0$ and V_{s1} be open. $V_1 = V_{s1}/2$ and $V_o = V_{s1}$. The output current consists of the superposition of the zero state response (ZSR) and zero input response

(ZIR); in the Laplace domain, where $i_L(t = 0)$ are periodic boundary conditions such that $i_L(t = 0) = i_L(nT_z)$; $n \in \{1, 2, \dots\}$ and T_z are the zero crossings given below. Similarly,

$$V_o(s) = \frac{I_1(s) - I_o(s)}{C_1 s} + \frac{v_o(t=0)}{s}, \quad \text{0 for ZVS} \quad (3.6)$$

$$I_1(s) = -\frac{V_o}{2L_1 s} + \frac{i_1(t=0)}{s}, \quad (3.7)$$

and

$$I_L(s) = -\frac{V_o}{L s} + \frac{i_L(t=0)}{s}. \quad (3.8)$$

Simplifying,

$$V_o(s) = \frac{\omega R/Q}{s^2 + \frac{\omega}{Q}s + \omega^2} \left[i_1(t=0) - i_L(t=0) \right], \quad (3.9)$$

where $Q = \omega RC_1$, $\omega^2 = \omega_1^2 + \omega_0^2$, $\omega_1^2 = 1/2L_1C_1$, and $\omega_0^2 = 1/LC_1$.

In the time domain for the underdamped case ($Q > 1/2$),

$$v_o(t) = \frac{\omega R}{\omega' Q} e^{-\omega t/2Q} \sin \omega' t \left[i_1(t=0) - i_L(t=0) \right], \quad (3.10)$$

where the underdamped frequency is

$$\omega' = \frac{\sqrt{4Q^2 - 1}}{2Q} \omega.$$

What is important to notice in (3.10) is that ZVS is guaranteed at $t = T_z = \pi/\omega'$ for any $Q > 1/2$, regardless of i_1 and i_L , which makes ZVS for the inverse class D robust to load.

A half-circuit as illustrated in Figure 3-7b can be used to simplify analysis. We assume the ripple in the choke inductor L_μ is infinitesimal so that I_μ can be considered constant. C_1 and shunt C can be lumped into the half-circuit $C = C_1 \parallel C_{\text{original}}$; L_1 and shunt L can be lumped into half-circuit $L_1 = L_{1,\text{original}} \parallel L$.

Using a similar analysis as (3.6)-(3.10),

$$V_o(s) = \frac{1}{C s} \left[I_1(s) - \frac{V_o(s)}{R} \right] + \frac{v_o(t=0)}{s}, \quad \text{0 for ZVS} \quad (3.11)$$

and

$$I_1(s) = -\frac{V_o}{2L_1 s} + \frac{i_1(t=0)}{s}. \quad (3.12)$$

We can label and define some parameters for better notation,

$$\omega_0 = \sqrt{\frac{1}{2LC}} \quad (3.13)$$

$$Q = \omega_0 RC \quad (3.14)$$

$$\xi \triangleq \sqrt{4Q^2 - 1} \quad (3.15)$$

$$\omega' \triangleq \frac{\xi}{(1 + \xi^2)^{1/2}} \omega_0 \quad (3.16)$$

$$\psi = \tan^{-1} \xi \quad (3.17)$$

$$\bar{\psi} = \tan^{-1} \frac{1}{\xi}. \quad (3.18)$$

The output voltage can be found from the Laplace domain

$$V_o(s) = \frac{1}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} i_1(t=0), \quad (3.19)$$

to the time domain,

$$v_o(t) = \frac{2Q}{\omega_0 C \xi} e^{-\omega_0 t / 2Q} i(t=0) \sin \omega' t, \quad (3.20)$$

and by taking derivatives, the peak voltage can be found to be

$$v_{o,\text{pk}} = \frac{1}{\omega_0 C} \exp\left(-\frac{1}{\xi} \tan^{-1} \xi\right) i(t=0), \quad (3.21)$$

hence the initial current can be found,

$$i(t=0) = V_{\text{LIM}} \omega_0 C \exp\left(\frac{1}{\xi} \tan^{-1} \xi\right). \quad (3.22)$$

The complete expression for output voltage is

$$v_o(t) = V_{\text{LIM}} \frac{(1 + \xi^2)^{1/2}}{\xi} \exp\left(\frac{1}{\xi} \tan^{-1} \xi\right) e^{-\omega_0 t / 2Q} \sin \omega' t, \quad (3.23)$$

where V_{LIM} is the maximum output voltage chosen, which is usually limited by the switch rating.

The inductor current can be found from Equation 3.12

$$i_1(t) = \frac{1}{2L} \int_0^t v_o(t') dt' + i(t=0) \quad (3.24)$$

$$= \frac{V_{ds,pk}}{2} \omega_0 C e^{\psi/\xi} \left[3 - \frac{(1 + \xi^2)^{1/2}}{\xi} e^{-\omega' t/\xi} \sin(\omega' t + \psi) \right]. \quad (3.25)$$

The rms output voltage can be found by integrating,

$$v_{o,rms}^2 = \frac{1}{\frac{\pi}{\omega'}} \int_0^{\pi/\omega'} v_o(t)^2 dt,$$

$$v_{o,rms}^2 = \frac{1}{4\pi} \xi V_{LIM}^2 (1 - e^{-2\pi/\xi}) \exp\left(\frac{2}{\xi} \tan^{-1} \xi\right). \quad (3.26)$$

The output power deliver to the load R can now be calculated,

$$P_o = \frac{v_{o,rms}^2}{R} = \frac{\omega_0 C}{2\pi} \frac{\xi}{(1 + \xi^2)^{1/2}} V_{LIM}^2 (1 - e^{-2\pi/\xi}) \exp\left(\frac{2}{\xi} \tan^{-1} \xi\right). \quad (3.27)$$

The required dc input voltage required to satisfy this output power can be calculated by integrating the average rectified output voltage, which is required to be equal to the input voltage so that the average voltage across the choke inductor L_p will be zero

$$V_{cc} = \frac{1}{2} \frac{1}{\frac{\pi}{\omega'}} \int_0^{\pi/\omega'} v_o(t) dt$$

$$= \frac{1}{2\pi} \frac{\xi}{(1 + \xi^2)^{1/2}} V_{LIM} (1 + e^{-\pi/\xi}) \exp\left(\frac{1}{\xi} \tan^{-1} \xi\right). \quad (3.28)$$

Figure 3-8 illustrates how the output power varies as the load, which is embedded in ξ is swept; the components (L's and C's) and the input voltage (V_{cc}) from Table 3.1 are fixed. As mentioned previously, the D^{-1} topology is impervious to unloading ($\xi \rightarrow \infty$). It is resistant to overload, but cannot handle a short-circuit ($\xi \rightarrow 0$) corresponds to $Q = 1/2$, which is the minimum Q for resonance. Note that in this case the switch current is not limited.

The switch current can be found by examining Figure 3-9,

$$i_{sw} = i_1 + i_2 - i_{csw}. \quad (3.29)$$

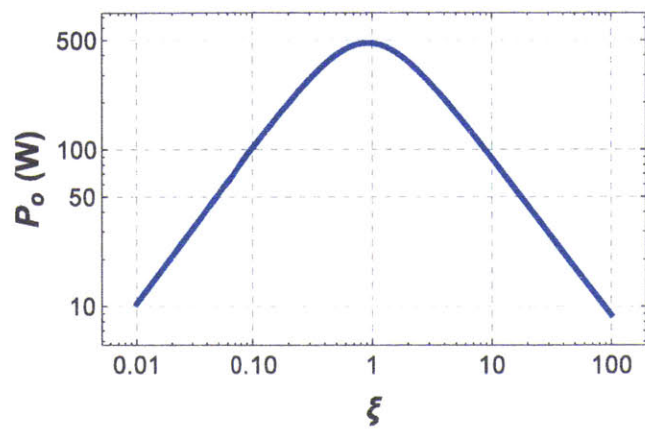


Figure 3-8: Output Power as Function of Load

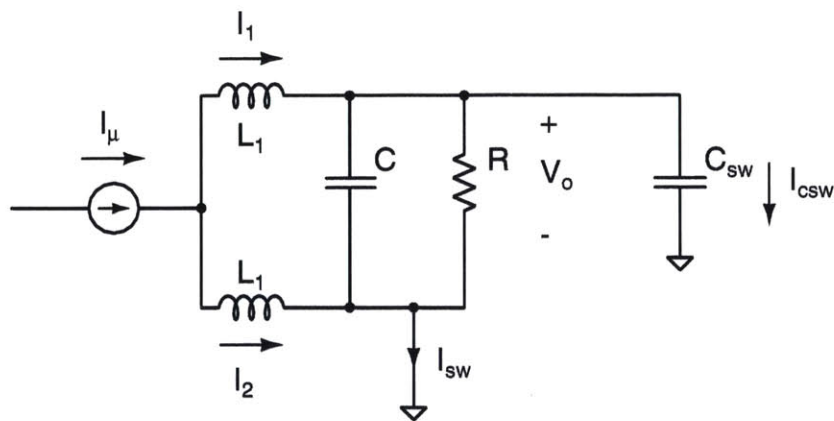


Figure 3-9: Half-Circuit Model Including Switch Parasitic Capacitance

Table 3.1: Example D^{-1} Transmitter

| Component | Value |
|--------------|-----------------|
| L_1 | 249 nH |
| C | 160 pF |
| C_{sw} | 100 pF |
| R | 87.5 Ω |
| f_s | 13.56 MHz |
| V_{cc} | 47 V |
| $V_{ds,pk}$ | 150 V |
| $I_{sw,rms}$ | 2.0 A |
| R_L | 1.15 k Ω |
| Q | 2 |
| P_o | 122 W |

The input current i_μ will be considered constant (i.e. infinitesimal ripple) so that

$$i_1 + i_2 = i_\mu \quad (3.30)$$

where i_μ can be found by power balance

$$P_{out} = V_{cc} i_\mu = \frac{V_{o,rms}^2}{R}. \quad (3.31)$$

Using Equations 3.14 and 3.26,

$$i_\mu = V_{ds,pk} \omega_0 C \left(\frac{1 - e^{-2\pi/\xi}}{1 + e^{-\pi/\xi}} \right) e^{\psi/\xi}. \quad (3.32)$$

I_μ represents the input current to the amplifier and is show in Figure 3-10 as a function of loading; the input current is proportional to the input power so the figure also illustrates that the input power goes to zero when the amplifier is unloaded.

The current through the switch parasitic capacitance can be found by using Equa-

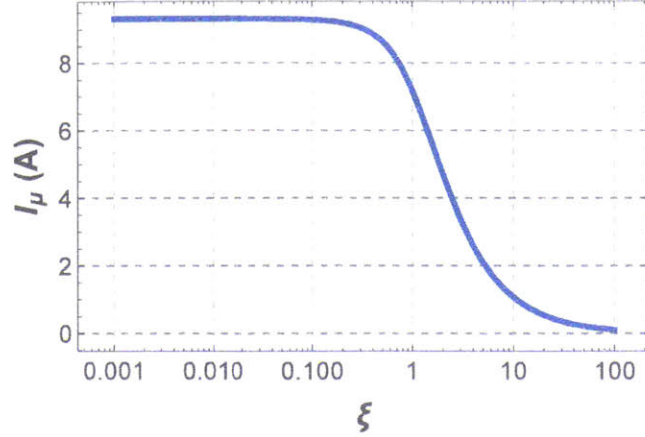


Figure 3-10: Input Current as a Function of Loading

tion 3.23,

$$i_{csw} = C_{sw} \frac{dv_o}{dt} \quad (3.33)$$

$$= V_{ds,pk} \frac{(1 + \xi^2)^{1/2}}{\xi} \omega_0 C_{sw} e^{-\omega't/\xi} \cos(\omega't + \bar{\psi}). \quad (3.34)$$

The switch current is then

$$i_{sw}(t) = i(0) \left[\frac{1 - e^{-2\pi/\xi}}{1 + e^{-\pi/\xi}} - \gamma \frac{(1 + \xi^2)^{1/2}}{\xi} e^{-\omega't/\xi} \cos(\omega't + \bar{\psi}) \right], \quad (3.35)$$

where $i(0)$ is the same as Equation 3.22 and

$$\gamma = \frac{C_{sw}}{C + C_{sw}}. \quad (3.36)$$

The rms switch can then be found by mean-squared integration,

$$i_{sw,rms} = \frac{\omega_0 C}{\sqrt{2}} V_{ds,pk} e^{\psi/\xi} \left(\frac{1 - e^{-2\pi/\xi}}{1 + e^{-\pi/\xi}} \right) \left[\frac{1}{\gamma^2} + \frac{1}{4\pi} \frac{1 + \xi^2}{\xi} \frac{(1 + e^{-\pi/\xi})^2}{1 - e^{-2\pi/\xi}} \left[1 + \frac{1}{(1 + \xi^2)^{1/2}} \cos(2\bar{\psi} + \psi) \right] \right]^{1/2}. \quad (3.37)$$

3.3 Device Capability in the D^{-1} Amplifier

It is worthwhile to examine some theoretical upper bounds on the device capability for D^{-1} amplifiers. A useful limiting case, that of a matched resistive load, leads to simple and intuitive analytical results. The results are based on the following assumptions:

1. Perfectly matched load for the maximum possible power output at the device limits.
2. No losses in the inductors and capacitors.
3. Zero voltage switching with no deadband in the output voltage.

In the previous section, we investigated amplifier behavior as designed for given passive components (L's and C's) and parameterized by load ξ . In this section, we take the alternative point of view and specify a device with a given characteristic C_{sw} and limits:

$$\begin{aligned} v_{ds,pk} &= V_{lim} \\ i_{sw,rms} &= I_{lim}. \end{aligned}$$

If we solve for γ in Equation 3.37

$$\frac{1}{\gamma} = \frac{I_{lim}}{V_{lim}} \frac{\sqrt{2}}{\omega_0 C_{sw}} e^{-\psi/\xi} \frac{1 + e^{-\pi/\xi}}{1 - e^{-2\pi/\xi}} \left[1 - \left(\frac{\omega'}{\omega_c} \right)^2 \right]^{1/2}, \quad (3.38)$$

where

$$\omega_c = \frac{\sqrt{8\pi}}{\frac{V_{lim}}{I_{lim}} C_{sw}} \frac{e^{-\psi/\xi}}{(1 - e^{-2\pi/\xi})^{1/2}} \frac{\xi^{3/2}}{1 + \xi^2} \left[1 + \frac{1}{(1 + \xi^2)^{1/2}} \cos(2\bar{\psi} + \psi) \right]^{-1/2}, \quad (3.39)$$

and substituting into the expression for output power

$$P_o = \frac{\omega_0 C_{sw}}{2\pi\gamma} \frac{\xi}{(1 + \xi^2)^{1/2}} V_{lim}^2 (1 - e^{-2\pi/\xi}) e^{2\psi/\xi}, \quad (3.40)$$

a new expression emerges that can help elucidate device performance in this topology

$$\boxed{P_o = \frac{\sqrt{2}}{2\pi} V_{lim} I_{lim} \frac{\xi}{(1 + \xi^2)^{1/2}} e^{\psi/\xi} (1 + e^{-\pi/\xi}) \left[1 - \left(\frac{\omega'}{\omega_c} \right)^2 \right]^{1/2}}. \quad (3.41)$$

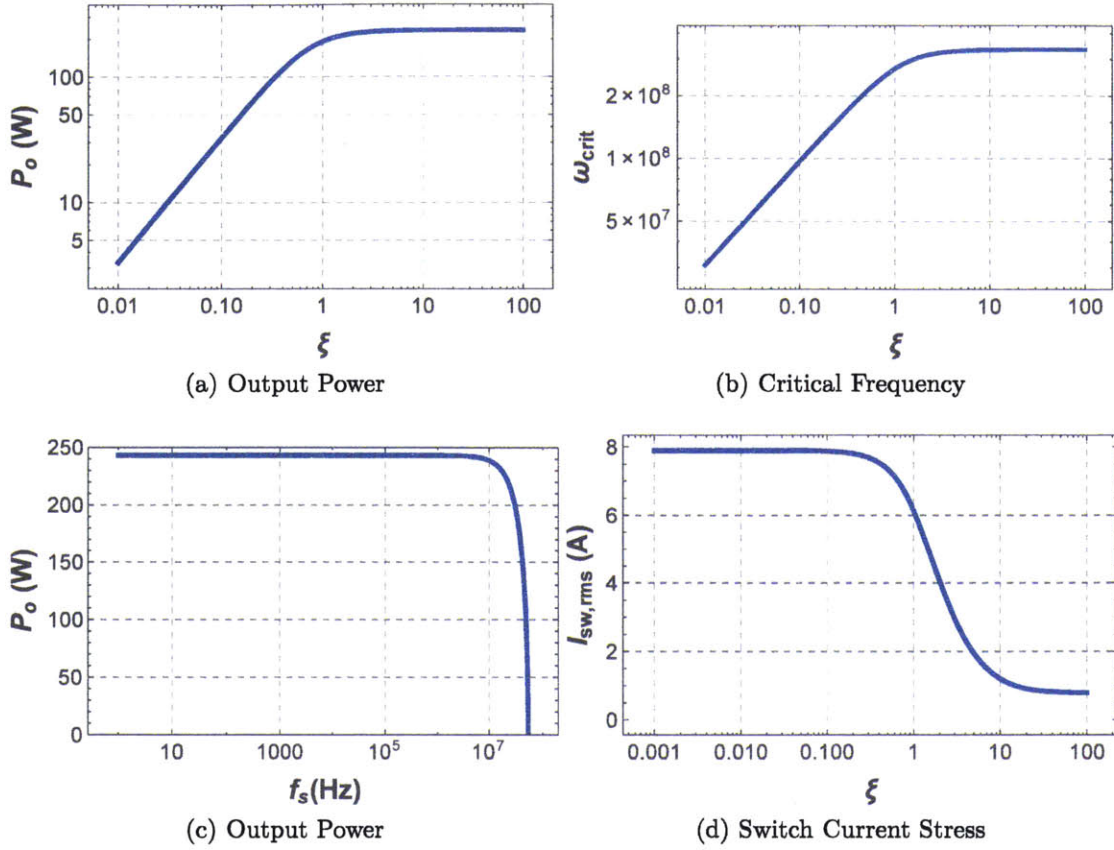


Figure 3-11: Optimal Design of D^{-1} amplifier is switching device dependent.

Figure 3-11 illustrates the performance for a representative device EPC 2019—200 V derated to 180 V with a worst-case $R_{ds,on} = 50 \text{ m}\Omega$ with 0.5 W free-air thermal limit, which corresponds to $i_{sw,rms} = 3 \text{ A}$. As noted before, the output power illustrated in Figure 3-11a has a different shape than that in Figure 3-8 because in the device-centric power expression the rms switch current is limited to I_{lim} with γ as the free parameter. It is apparent that both output power and critical frequency increase and then approach asymptotes with ξ . The low-frequency ($\omega' \rightarrow 0$ along with $\xi \rightarrow \infty$) limits can be written as

$$\lim_{\xi \rightarrow \infty} P_o = \frac{\sqrt{2}}{\pi} V_{lim} I_{lim} \quad (3.42)$$

$$\lim_{\xi \rightarrow \infty} \omega_c = \frac{2}{R_{lim} C_{sw}} \quad (3.43)$$

$$R_{lim} = \frac{V_{lim}}{I_{lim}}. \quad (3.44)$$

It is noteworthy to mention that it is apparent from Equation 3.23 operation at

a switching frequency that is equal to the damped natural frequency results in ZVS and no switch overlap

$$f_s = \frac{\omega'}{2\pi},$$

which is the circumstance in Figure 3-11c.

A figure of merit reminiscent of the gain-bandwidth product of linear amplifier at the ξ_∞ limit can be written

$$\xi_\infty: \omega_c P_o = \frac{2\sqrt{2}}{\pi} \frac{I_{lim}^2}{C_{sw}}, \quad (3.45)$$

which is nearly proportional to the area under the curve in Figure 3-11c. The $\sqrt{2}$ factor in Equation 3.42 is from the reduction in the rms switch current in push-pull, while $1/\pi$ is the topology dependent factor for the D^{-1} amplifier.

We can introduce some figures of merit with which to compare devices. We can define a limiting Q for the circuit as the switch Q_0 ,

$$Q_0 = \frac{1}{\omega_c C_{sw} R_{ds,on}} = \frac{1}{2} \frac{\frac{V_{lim}}{I_{lim}}}{R_{ds,on}}. \quad (3.46)$$

We can then derive a fundamental product that gives us a metric for the power handling capability and loss of is

$$\omega_c P_o Q_0 = \frac{\sqrt{2}}{\pi} \frac{V_{lim} I_{lim}}{C_{sw} R_{ds,on}}. \quad (3.47)$$

The figure of merit indicated in Equation 3.47 is a measure of the ability to provide power over a wide bandwidth at low loss. A map of a representative devices in Appendix A is shown in Figure 3-12. The oval is a datapoint for the EPC 2019 GaN device, which is used in the next section for the QSPP amplifier.

3.4 Quad-Switched Push-Pull Amplifier (QSPP)

We demonstrate a 23 W amplifier that spreads over 90% of the power from 1 MHz to 20 MHz with up to 80% efficiency. An advantage of spread-spectrum modulation with a resonant topology is that switching can be varied to match changes in resonance due to load or voltage-dependent components such as switch capacitance, which we show improves efficiency.

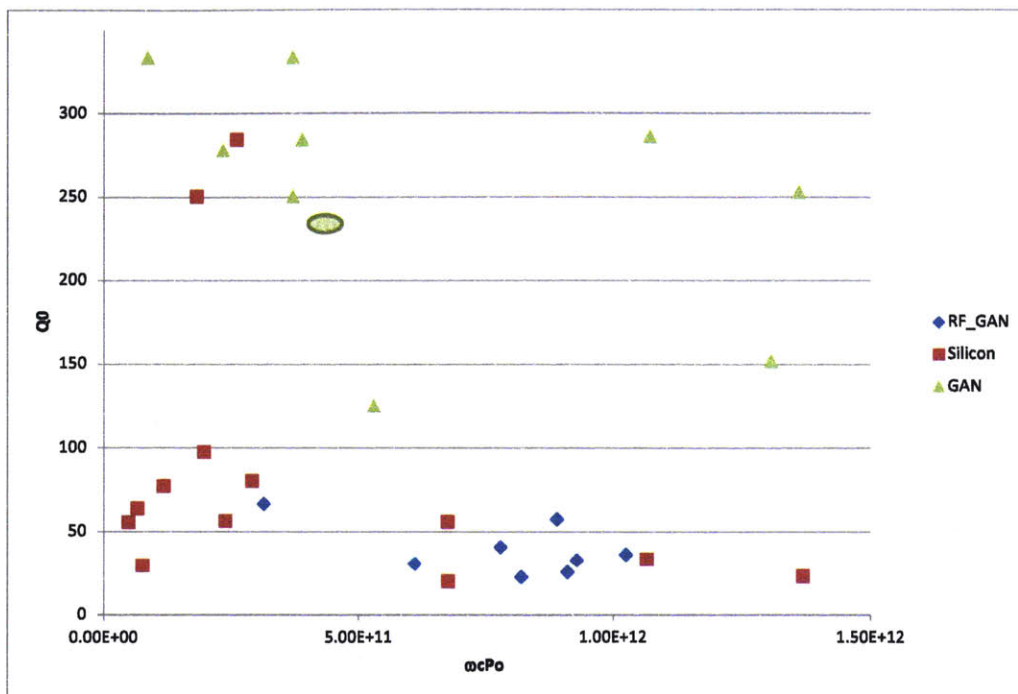


Figure 3-12: Figure of Merit Map for Various Devices

There are several improvements in this thesis to the sequence optimization described in [12]. First, the pulse duty-cycle is held constant for a given optimization; the pulse duty-cycle is defined as the ratio of the time the pulses occupy in a given sequence to the total duration of the sequence (duration at zero, or zero duration, plus duration of pulses). The number of pulses in the sequence was increased from 1024 to 2048, but with decreased time resolution of the zero durations from 1/30 of a single pulse duration to 1/18, due to FPGA timing constraints at the new operating frequency, which is almost 150% higher. Figure 3-13 shows that the ratio of the highest peak of the spread spectrum is over 16 times lower than that of a single-frequency sine wave with the same average power. The FFT spectrum was calculated with a 9 kHz RBW (resolution bandwidth), which is specified for CISPR22 between 150 kHz and 30 MHz.

The pulse-duty of 0.75, among other optimized spread sequences, was a tradeoff between a higher spreading figure of merit (average power ratio to spectral peak) and lower conduction losses from current-carrying, zero-voltage durations. A histogram is shown in Figure 3-14 of the distribution of zero durations when the total zero duration is constrained in the optimization. The results are different from that in [12] because of the zero duration constraints and the details of performing such an optimization

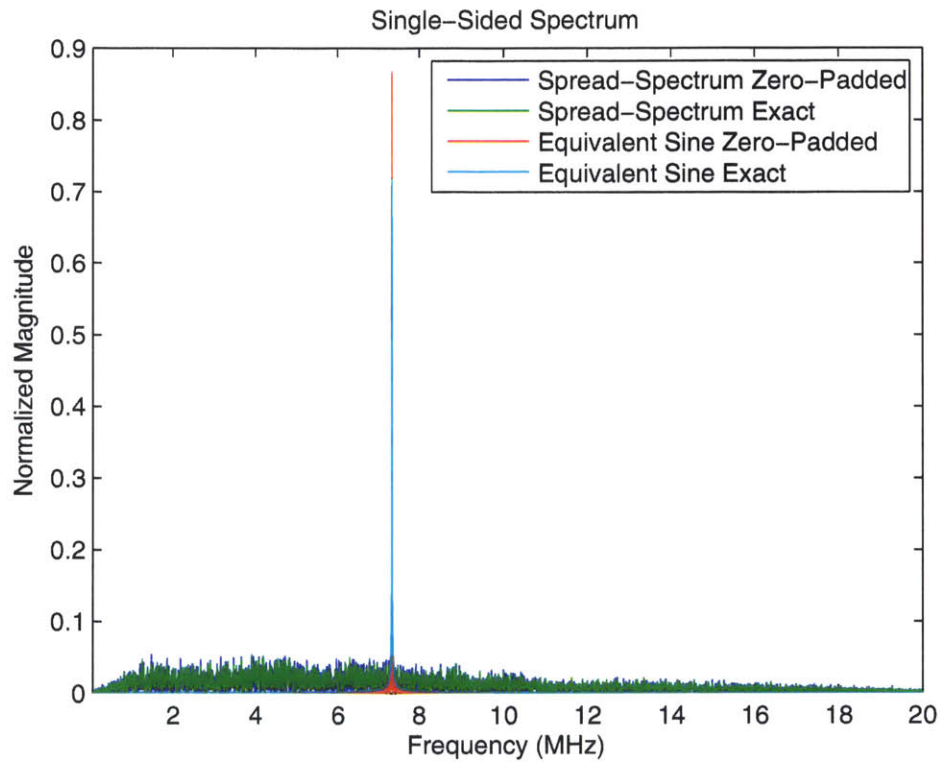


Figure 3-13: Exact FFT of spread-spectrum sequence (RBW = 9 kHz). Note that the sine wave frequency 7.35 MHz is not a multiple of 9 kHz. Magnitude is normalized to unit spread spectrum pulse amplitude. Spread spectrum pulse-duty of 0.75 is included in the calculation of the equivalent single-frequency sine wave.

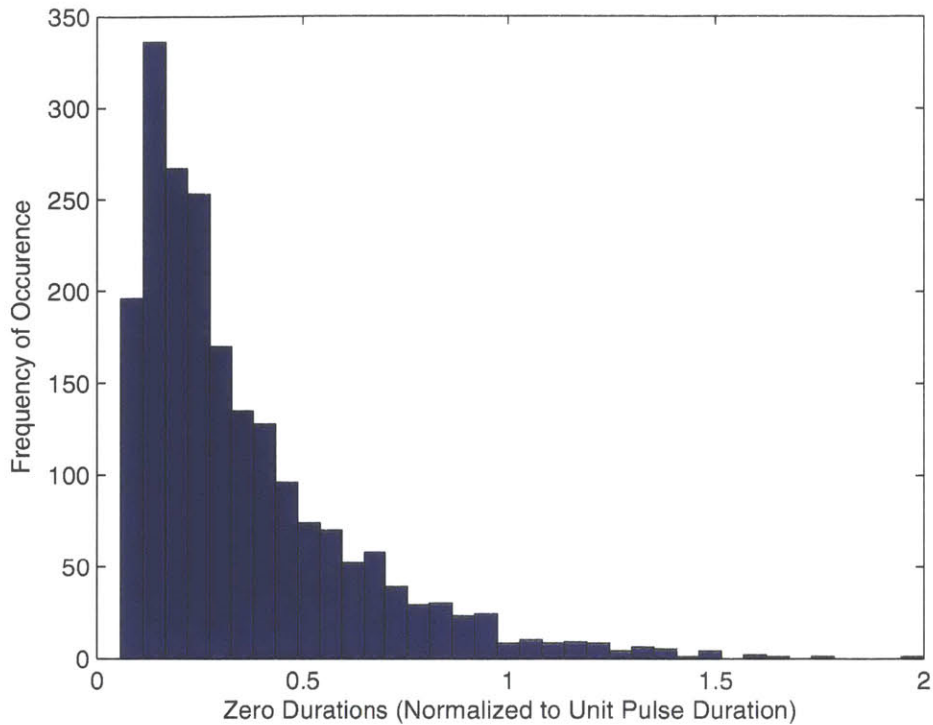


Figure 3-14: Histogram of the zero durations for unit pulse duration. The sequence optimization was constrained to a pulse duty-cycle of 0.75.

will be described in a future paper.

3.4.1 Comparison of D^{-1} -Derived Topologies to Other Amplifiers for Spread-Spectrum

Class E amplifiers are conventionally used in high frequency amplifiers including those for wireless power transfer because both zero voltage switching and zero voltage derivative switching can be guaranteed over a range of operating conditions [104], ensuring that the body diode of FET switches do not turn on with the resulting reverse recovery loss. In [117], a spread spectrum system using pseudorandom modulation based on a class D (voltage mode) amplifier is described. The disadvantage of this conventional class D amplifier implementation is that the switches do not operate with zero voltage switching and hence incur higher switching losses, which limits its applicability in applications that require high frequency and higher voltage.

With the advent of gallium nitride (GaN) FETs, there is no reverse recovery loss because the inherent parallel diode is majority carrier. Even though the voltage drop is higher (2V vs. 0.8V for an equivalent Si MOSFET) the current conducts in the

diode for only a short period of time, corresponding to a switch delay margin to ensure that the switch turns on at essentially zero voltage. This tolerance to switch timing means that the topology is relatively insensitive to mismatches in gate drive delay, device parasitics and parameters, and layout, among others. Several advantages of topologies derived from the D^{-1} amplifier include:

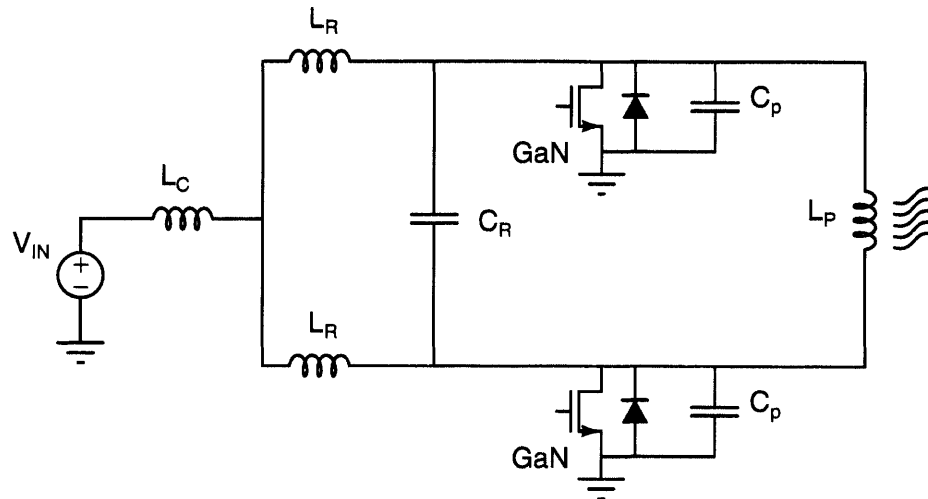
1. Guaranteed zero voltage switching for high frequency/high voltage operation,
2. Guaranteed zero voltage switching from full load to no load,
3. Tolerance to unloading/device removal; ZVS guaranteed with voltages and currents bounded. All that is needed are drain clamps that absorbs a fixed amount of energy,
4. In the ideal case (i.e. current source input and no parasitics), when the switches are all closed, the states are essentially frozen (inductor currents unchanged and capacitor voltages zero). This allows pulse position modulation that is not limited by a resonance, e.g. output resonance of a class E.
5. Piecewise 2nd order, unlike a Class E or other higher order amplifiers (F, EF, etc.), which means that much of the time domain behavior can be reliably predicted from linear analysis.

3.4.2 Principles of Operation

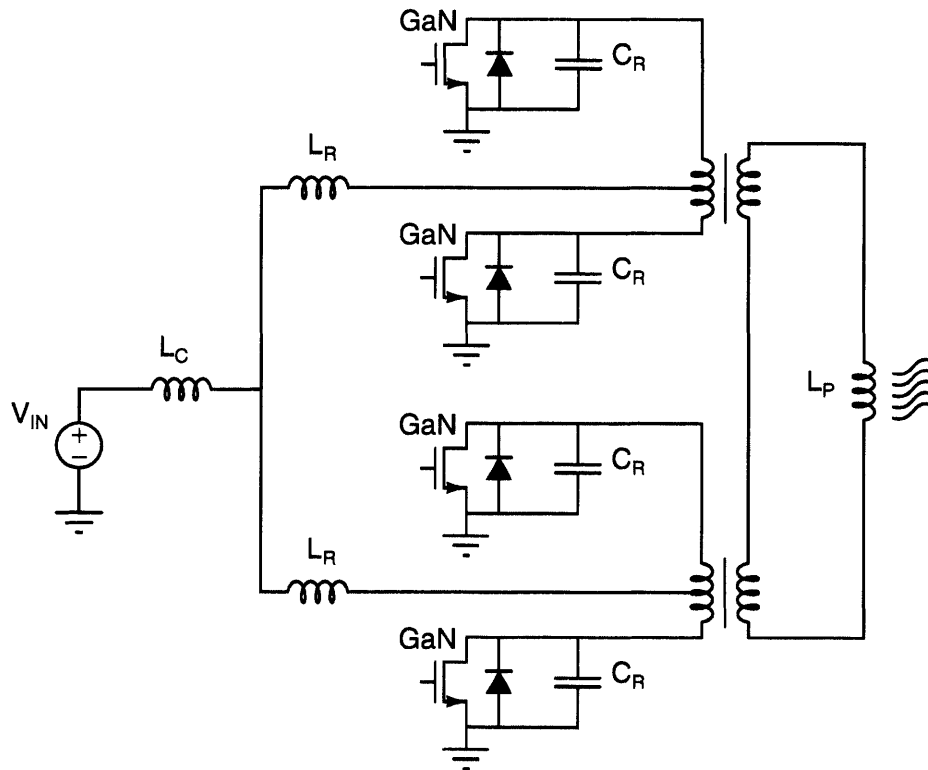
Quad-switch push-pull operation allows the independent and simultaneous modulation of the phase (polarity) and position of half-sine wave pulses. The amplifier is fed by a dc voltage source (V_{IN}) to ideally create a current source through a choke for what is essentially a switched parallel-resonant circuit. A push-pull configuration is advantageous because ground-referenced gate drives can be used, hence obviating the difficulties in level shifting and floating gate drives at higher frequencies. Resonance is achieved through the center-taps of two transformers; although the use of transformers as combiners in RF power amplifiers is well-known [79,86], consideration and analysis in their design for a particular topology is required.

In the proceeding design equations, approximations are used so that intuition towards design tradeoffs are less encumbered.

The basic operation is illustrated in Figure 3-16. In this simplified model, the current through the choke is dc and i_R and v_R are the resonant current and voltages,



(a) Dual-Switch Push-Pull



(b) Proposed Quad-Switch Push-Pull Topology

Figure 3-15: Inverse Class D Derived Amplifiers with Wireless Power Transfer Loads.

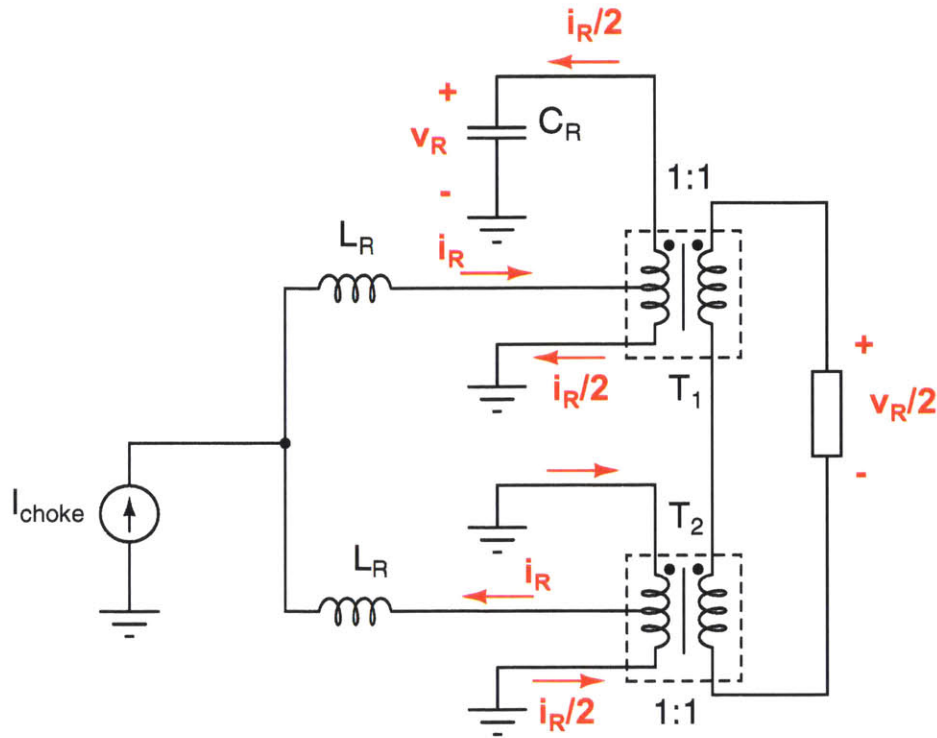


Figure 3-16: Resonant Operation of QSPP Amplifier

respectively. This results in a half-sine voltage pulse to the output that is half the amplitude of the capacitor resonant voltage with a resonant frequency given by,

$$\omega_0 = \frac{1}{\sqrt{L_R C_R}}. \quad (3.48)$$

Referring to Figure 3-15, during the zero duration interval t_{zd} , all the switches are ON and the resonant current i_R in Figure 3-16 is constant and the voltages (including v_R) are zero. During a pulse, only a single switch is OFF, v_R resonates, and all the other switch behave as synchronous rectifiers so there is no diode voltage drop. After a resonant pulse, v_R is zero and the switch is turned ON at zero voltage switching. The timing margin for turning the switch ON is relatively relaxed because the reversing resonant current $i_R/2$ can turn the GaN FET body diode ON with only a small voltage drop (~ 2 V) for a short period of time corresponding to the timing error; as previously mentioned, no reverse recovery loss is incurred.

The switching pattern must alternate between the switches on $T_1:(S_1, S_2)$ and $T_2:(S_3, S_4)$ in Figure 3-16 because the resonant current i_R alternates, i.e. only one of the switches necessarily on T_1 can be OFF to block positive i_R and charge the resonant

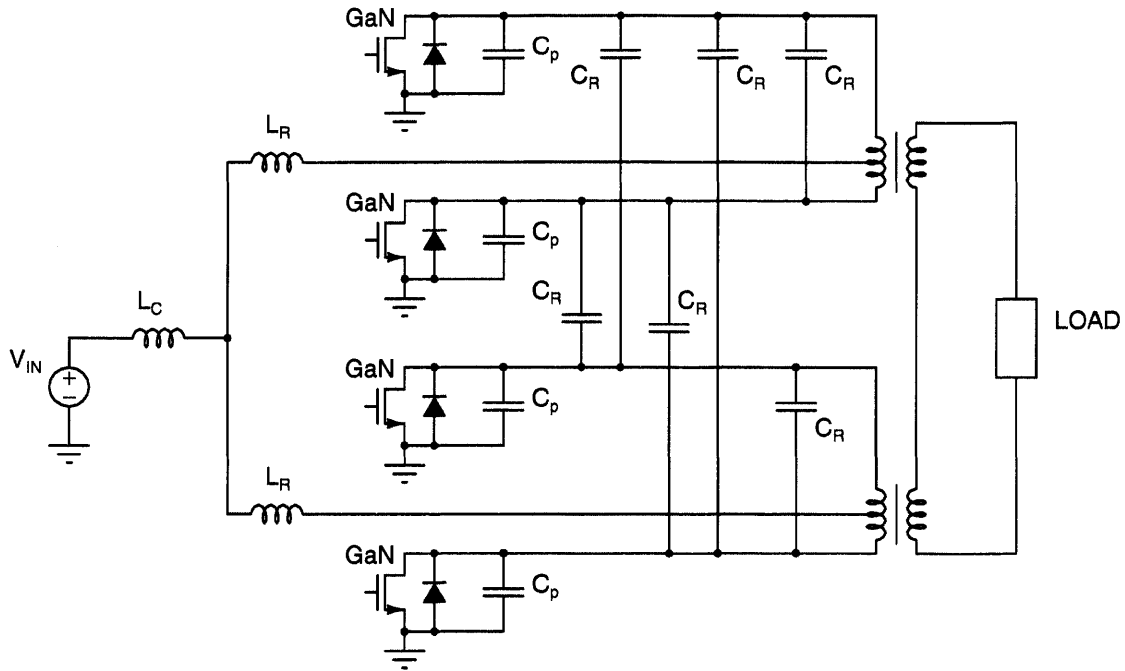


Figure 3-17: Proposed Quad-Switch Amplifier with Cross-Coupling Capacitors to Reduce Switch RMS Current.

capacitance, and vice-versa for negative i_R . Another constraint is that the time average of volt-seconds (or flux) in the transformers must be zero. One interesting consequence is that a symmetrical sine wave cannot be constructed. This can also result in a resonant current distortion from the magnetizing current that is dependent on the accumulated volt-seconds from the switching pattern. The construction of the switching pattern is described in [12]: the switching pattern is constructed from a dictionary of subsequences each with zero average volt-seconds.

By using a cross-coupling capacitor, as in Figure 3-15a, part of the resonant current is diverted from the switch ON resistance $R_{ds,on}$; to first-order, i.e. $R_{ds,on} \ll \sqrt{L_R/C_R}$,

$$i_{sw,on} = \frac{C_p}{C_p + C_R} i_R. \quad (3.49)$$

The idea of a cross-coupling capacitor can be generalized from the two-switch amplifier, to the quad-switch amplifier in Figure 3-17. By placing the cross-coupled capacitors on the switch side of the transformer, the leakage inductance can be absorbed into the resonant inductors L_R . The switch current for this topology is

$$i_{sw,on} = \frac{C_p}{C_p + 3C_R} \frac{i_R}{2} \quad (3.50)$$

and the pulse resonant frequency is given by

$$\omega_0 = \frac{1}{\sqrt{L_R(C_p + 3C_R)}}. \quad (3.51)$$

The Q of the pulse parallel-resonance can be calculated from the output load,

$$Q = \frac{N^2 R_{LOAD}}{\sqrt{L_{R,eff}/C_{R,eff}}}, \quad (3.52)$$

where $N^2 R_{LOAD}$ is the load resistance reflected to the resonant terminal (C_{node} in Figure 3-19); $L_{R,eff}$ and $C_{R,eff}$ are the effective resonant inductance and capacitance, respectively. For the QSPP topology with a trifilar-wound transformer ($N = 2$) and a 50Ω load in Figure 3-21, $Q \approx 3.5$.

The input choke L_C in Figure 3-15b is typically designed with an inductance L_{choke} so that the current ripple is small, and hence must be designed for the largest zero duration $T_{z,max}$ for the sequence (see Figure 3-14). The maximum current ripple is

$$\max \Delta I = \frac{V_{dc}}{L_{choke}} T_{zd,max}. \quad (3.53)$$

Also, by observing that the average voltage across the inductor L_C must be zero, V_{dc} is equal to the time-average of the sum of the drain voltages. For sinusoidal drain voltages with zero durations by overlapping switch ON-states,

$$V_{ds,pk} = \frac{2\pi V_{dc}}{D_p}, \quad (3.54)$$

where $D_p = T_p/(T_{zd} + T_p)$ is the pulse duty-cycle. This results in a voltage boost from the duty-cycle, similar to a boost converter, which can be advantageous in some applications.

3.4.3 Transformer Design and Prototype

A simple, broadband model with no resistances, which can be derived from [58,110] for a trifilar-wound transformer because of inherent symmetries, is illustrated in Figure 3-18. This model exposes how most of the transformer inductances and capacitances can be absorbed into a second-order resonator.

If we replace the ideal transformers in Figure 3-16 with the model in Figure 3-18, we can arrive at the simplified model in Figure 3-19. We're interested in the

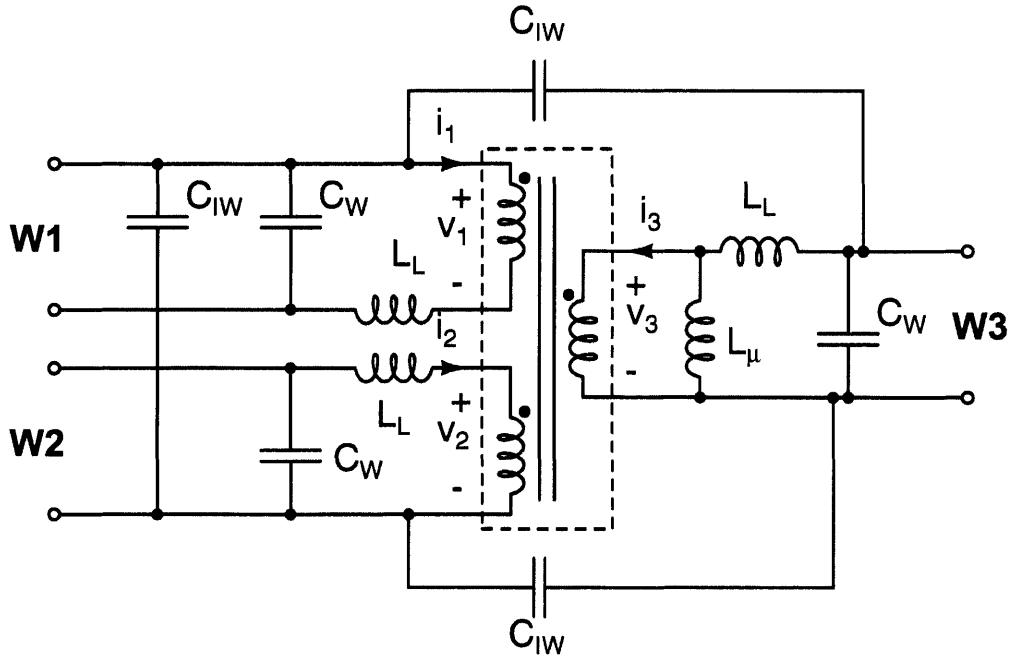


Figure 3-18: Broadband Transformer Model.

three denoted terminals: $L_{R,eff}$ —the effective resonant inductance from explicit inductors, transformer inductances, and transformer behavior; C_{node} —the added capacitance from the transformer parasitics, and Z_{out} —the imaginary portion of the output impedance.

If the terminal loading at Z_{out} is open, $L_{\mu} \gg L_L$, and we ignore the capacitances,

$$L_{R,eff} = 8L_R + 4L_L, \quad (3.55)$$

where the boxed $L_L/2$ is the terminal inductance from T_2 . The assumption that the output is open is a good approximation for the design of an amplifier with low output spectrum distortion; this means $Q > \approx 3$ and in the case of an output inductor for wireless power transfer, $L_{out} \gg L_L$.

$C_{node} \approx C_{IW}$ because typically $C_W \ll C_{IW}$ and we focus on the germane resonance and ignore the higher order LC effect, which is justified below when examining a more complete model using SPICE ac analysis. The effective resonant capacitance is

$$C_{R,eff} = C_P + 3C_R + C_{IW}, \quad (3.56)$$

where the device capacitance C_P includes both the GaNFET and clamp diode capacitances.

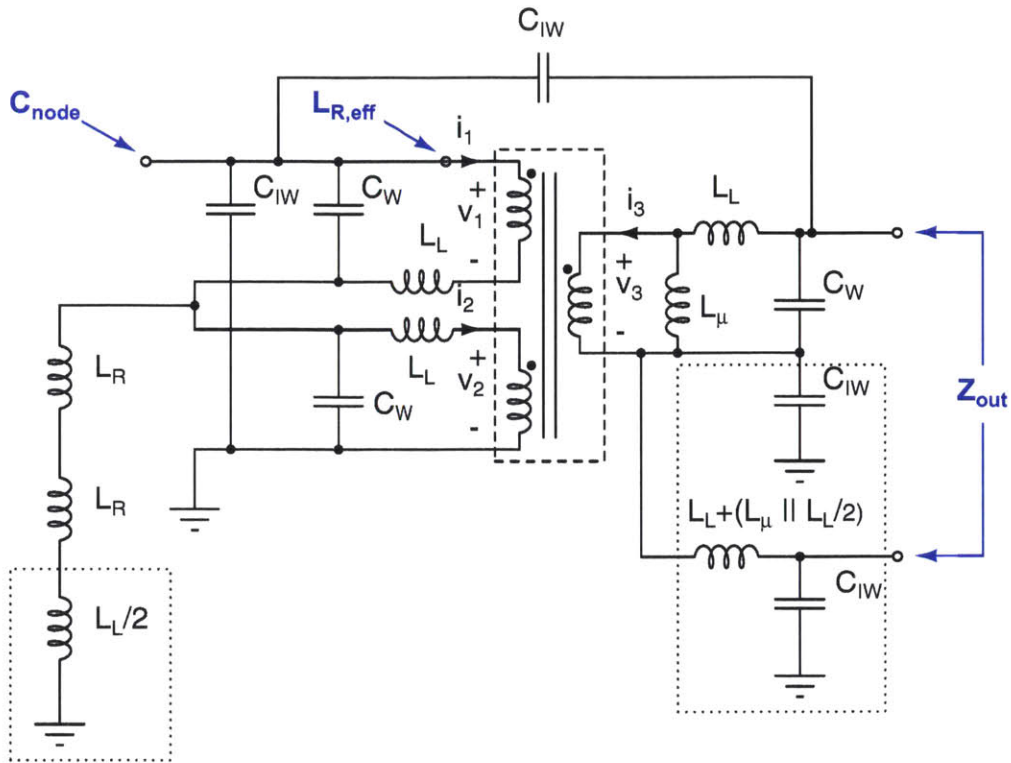


Figure 3-19: Stacked Transformer Model.

The useful bandwidth of the transformer is largely determined by the terminal resonance ω_T at Z_{out} and load matching, the Z_{out} characteristic impedance. Typically, the transformer resonance ω_T is designed to be much higher than the pulse resonance ω_P . In this case effective capacitance $C_{R,eff}$, which includes the terminal capacitance at C_{node} , is in essence a short at ω_P . In this case, the output appears as a parallel resonance with

$$L_{out} = 3L_L, \quad L_\mu \gg L_L, \quad (3.57)$$

$$C_{out} = \frac{C_{IW}}{2}, \quad C_W \ll C_{IW}. \quad (3.58)$$

To verify the modeling as well as some of the approximations, an ac analysis was performed in LTSpice for the switch configuration corresponding to $S1:OFF$. As illustrated in Figure 3-20, this model uses nominal values for inductances, capacitances, and resistances that were measured from the transformer, gathered from datasheets for the devices, and estimated for trace parasitics.

To examine the pulse resonance, the short across C19 in Figure 3-20 is removed and I1 is placed across it instead. The impedance seen at this S1-node is plotted

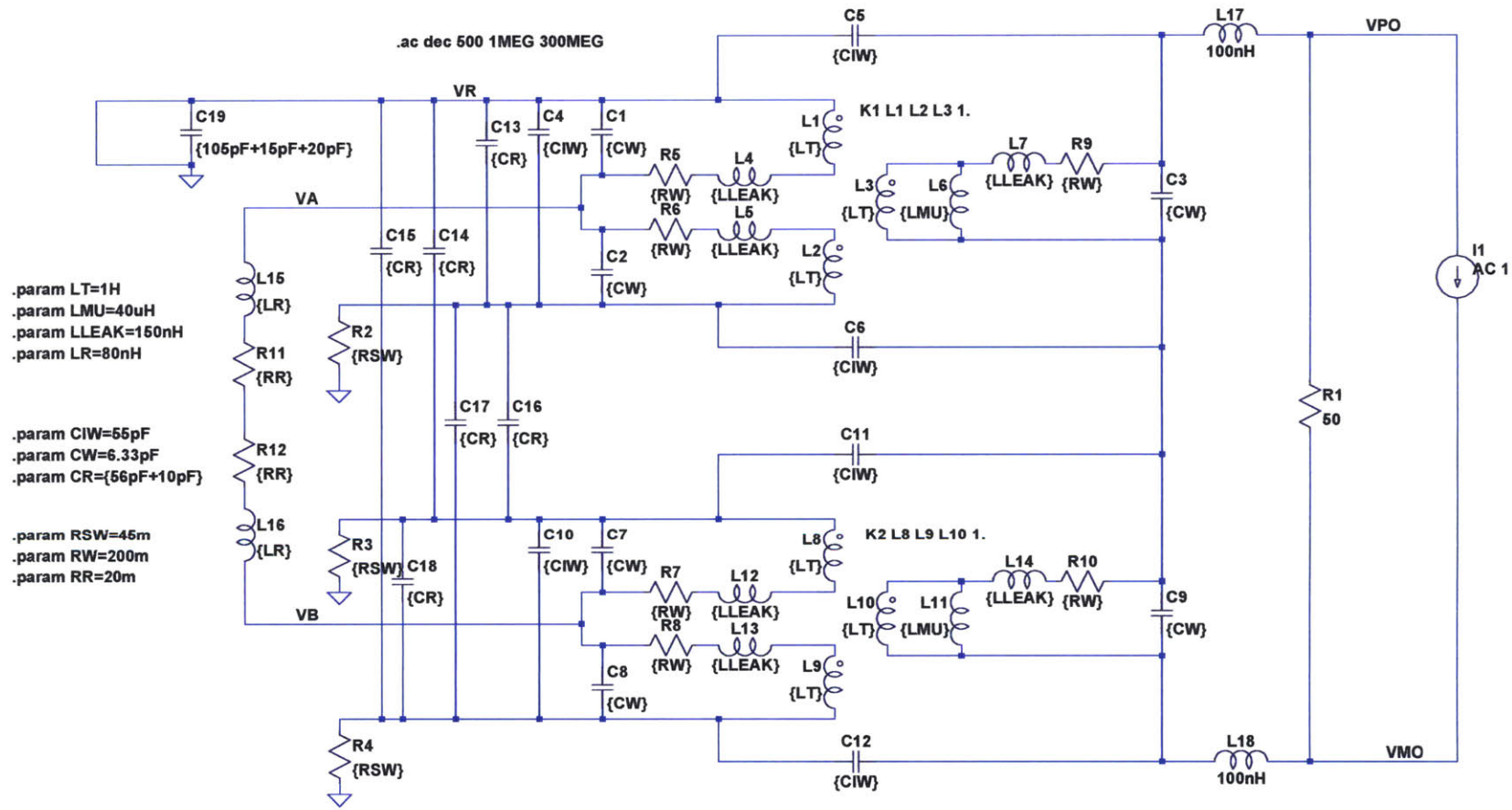


Figure 3-20: LTspice AC Analysis Model.

Section 3.4 : Quad-Switched Push-Pull Amplifier (QSPP)

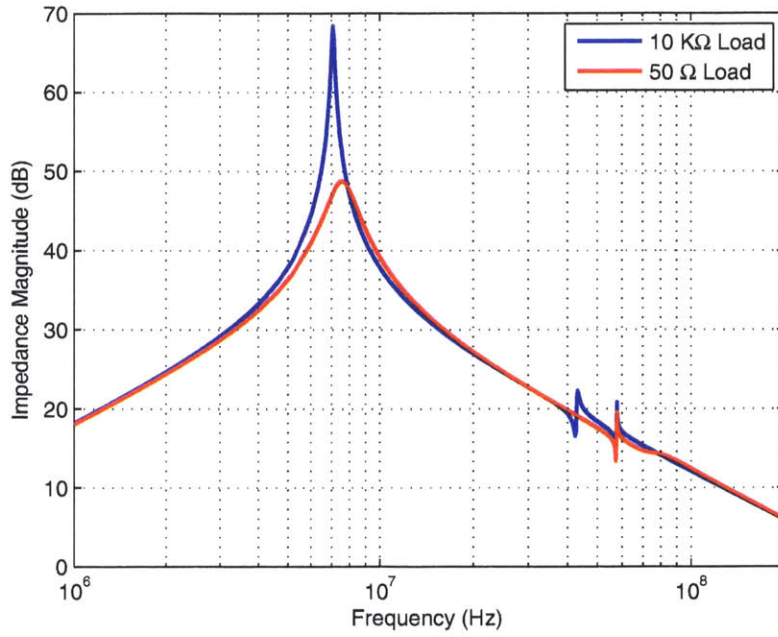


Figure 3-21: Simulated Impedance at Resonant Capacitor Node for Lightly Loaded (10 kΩ) and Fully-Loaded (50Ω) Output.

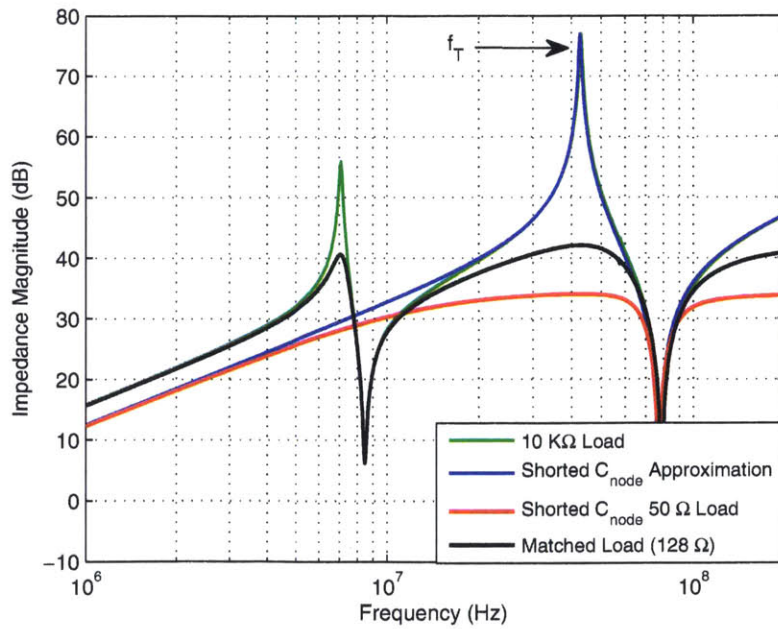


Figure 3-22: Simulated Output Impedance.

Table 3.2: Comparison of Analytical Calculation and Simulation

| Parameter | Analytical | Simulated | Experiment |
|-------------|--------------------|--------------------|------------|
| $L_{R,eff}$ | 1.24 μH | 1.25 μH | |
| $C_{R,eff}$ | 393 pF | 400 pF | |
| f_P | 7.2 MHz | 7.53 MHz | 7.35 MHz |
| L_{out} | 450 nH | 455 nH | |
| C_{out} | 27.5 pF | 26 pF | |
| Z_{out} | 128 Ω | | |
| f_T | 45.2 MHz | 43.21 MHz | |

in Figure 3-21 for both light load (10 k Ω) and full load (50 Ω). The peak in the lightly loaded condition nearly corresponds to the model natural frequency in (3.56) and the shift in the peak corresponds to higher loading. L17 and L18 correspond to layout and lead inductance to the load; these inductance are neglected in some of the analysis for simplification because the perturbation (9.2 Ω at 7.35 MHz) does not impact the calculation significantly.

The correspondence of the shorted-node approximation used in (3.57) to the more accurate model in Figure 3-20 is illustrated in the lightly-loaded (10 k Ω) higher frequency peak in Figure 3-22. It is also apparent from this figure that 50 Ω loading is overdamped and a matched load (128 Ω) is shown for comparison. A comparison of approximate analytical calculations and values derived from the LTspice simulations, illustrated in Table 3.2, shows good agreement; f_P corresponds to the pulse natural frequency and f_T to the output's natural resonant frequency.

Several transformers were designed and built using toroids (1015-1) of the M-material ($\mu = 125$), which is a NiZn ferrite from National Magnetics Group, Inc. Three promising designs are illustrated in Table 3.3. The cores were configured in a binocular-style and stacked. PTFE-insulated, stranded wire was used for low permittivity and loss, hence lower per unit capacitance and resistance: 24 ga. (19/36 strand) Alpha 5854 and 20 ga. (19/32 strand) Alpha 5856. The final prototype used the "2x24ga-Trifilar" design, which consisted of 2 pairs of 24 ga. trifilar windings paired in parallel with windings matched for the smallest interwinding capacitance C_{IW} . The parallel windings resulted in a lower winding resistance, but traded off a

Table 3.3: Measurement of Three Transformer Designs

| Parameter | 2x24ga-Trifilar | 20ga-Trifilar | 24ga-Trifilar |
|-------------------|-----------------|-------------------|-------------------|
| Core ¹ | 5x2 | 4x2 | 3x2 |
| Turns | 6 | 7 | 8 |
| L_{μ} | 40 μ H | 39 μ H | 43.7 μ H |
| L_{LEAK} | 150 nH | 195 nH | 276 nH |
| C_{IW} | 55 pF | 20 pF | 30 pF |
| C_W | 6.6 pF | 0 pF [†] | 0 pF [†] |
| R_W^2 | 0.25 Ω | 0.45 Ω | 0.5 Ω |
| R_W^3 | 0.06 Ω | 0.1 Ω | 0.15 Ω |

¹ m stacked toroidal cores X 2 (binocular-style).

² Approximate resistance at 10 MHz.

³ Approximate resistance at 1 MHz.

[†] Not measured.

higher interwinding capacitance.

3.4.4 23 W Amplifier Prototype

A 23 W prototype illustrated in Figure 3-23 was constructed with a resonant frequency nominally at 7.4 MHz, spreading power over 1–20 MHz. The prototype includes a 4-layer PCB module with the quad GaNFETs, their associated gate drives, and cross-coupling capacitors in a tight layout to minimize drain inductance. The magnetics, drain protection, and probe points are contained in the main 2-layer pc board.

The amplifier switches are controlled by an external board with a Xilinx Spartan 6 XC8SLX16 FPGA that stores the ternary sequences and zero durations timings using programmed timers and state machines to determine switching state. The FPGA clock frequency of 280 MHz, along with digital timing constraints limits the basic time resolution. Alternatively, a simple integrated circuit could be developed with a triggered ROM or EEPROM to store the modulation encoding, high speed counters, and digital delays enabling much higher operating frequencies.

3.4.5 Hardware Design

Input Choke

The input choke consists series connection of 16-turns of 20 gauge wire wrapped on a stack of 3, M-material toroids (1015-1) from National Magnetics and 2 paralleled 56 μH inductors from the EPCOS B82111E Series.

Resonant Components

56 pF, 500 V, high Q resonant capacitors (E-series from Johanson Technology). No explicit L_R inductors were used; instead, transformer leakages and board parasitics provided the required resonant inductance.

Semiconductor Switches

EPC2019 GaN (gallium nitride) FETs from EPC.

Gate Drives

Each FET is driven by three SN74LVC2GU04DCKR dual logic inverters.

Drain Clamps

DFLS1200 Schottky diode rated for 200 V, 1 A, nominal capacitance of 23 pF, in series with a 1SMB5953BT3 150 V, 3 W zener.

Quad GaNFET Module

The critical components including the GaNFETs, gate drives, and cross-coupling capacitors are assembled on a small pc board. This eases prototyping by allowing a high density of components to be assembled on a board which is easily manipulated. In addition, because the module is not directly bonded to the main board, it is tolerant of board flex from the heavier components and connections. The module was designed to minimize drain inductance and therefore trades this off for greater layout capacitances, which are not detrimental because they are absorbed into the D^{-1} topology's 2nd order resonance. The layout capacitance to ground from the coupling capacitors is 10 pF and the added drain capacitance is 20 pF.

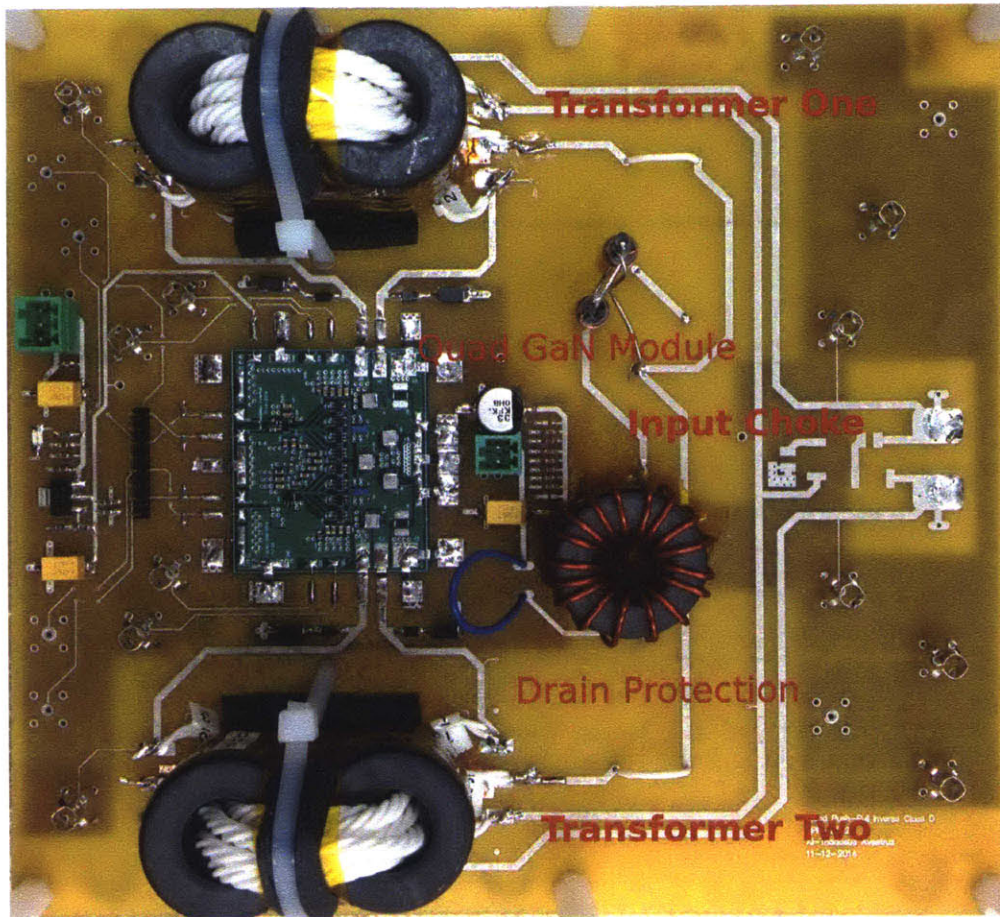


Figure 3-23: Prototype of the QSPP Spread Spectrum Amplifier.

3.4.6 Experimental Results

The amplifier drain voltages are shown in Figure 3-24. The waveforms were measured with Tektronix TPP1000 probes and a 1 GHz MSO4104B oscilloscope. The waveforms show no spurious oscillations and good zero voltage switching.

The output voltage waveform is shown in Figure 3-25 using a 200 MHz THDP0200 Tektronix Differential Probe. Peak-to-peak voltage is approximately 120 V and an output power of about 20 W into a 50 Ω load. From previous discussion, the output loading at 50 Ω is such that the output resonance is overdamped, which causes some distortion in the zero crossings at phase reversals. However, this distortion does not appear to significantly impact the spectrum shown in Figure 3-26, which is derived from the experimental waveform in Figure 3-25. The spectrum is plotted from 150 kHz to 30 MHz, which is the relevant CISPR 22 frequency range and requires a 9 kHz resolution bandwidth. When plotted similarly and compared, the experimen-

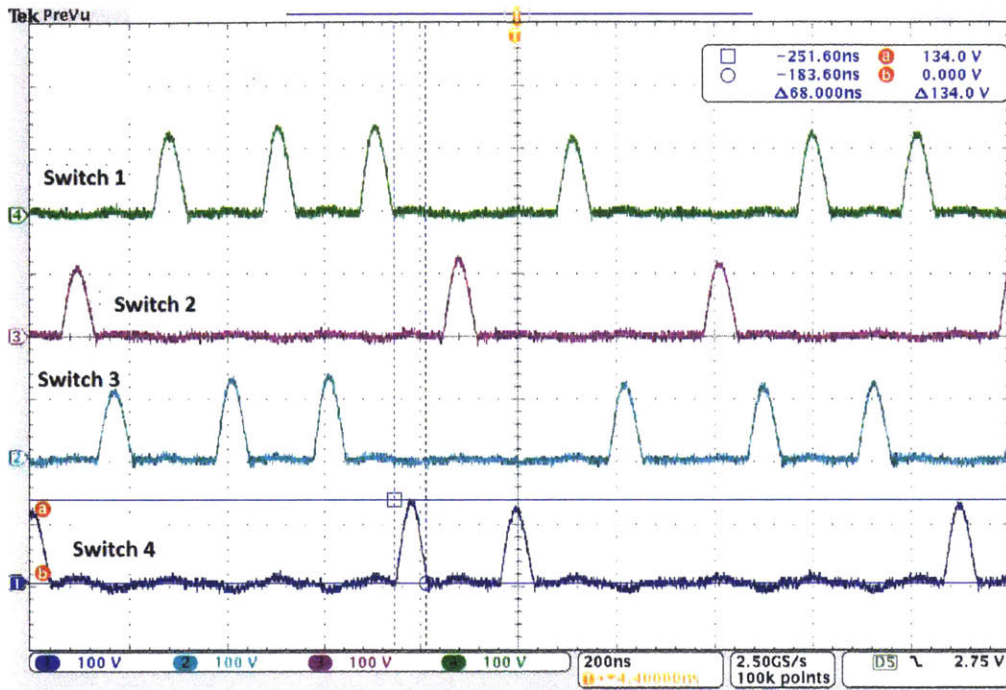


Figure 3-24: Drain Voltages for the amplifier prototype operating at 23 W into a 50 Ω Load.

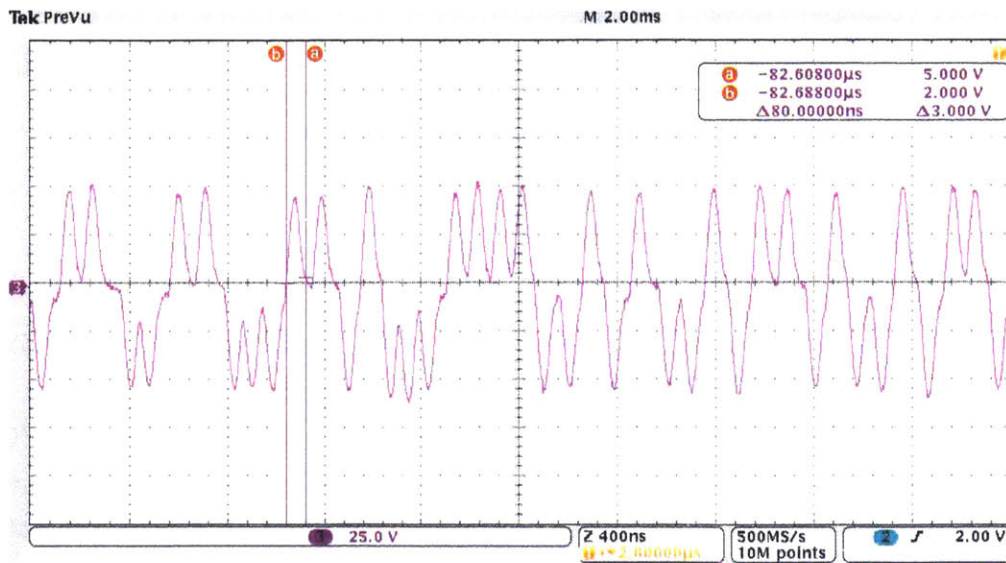


Figure 3-25: Output Voltage.

tal output spectrum in Figure 3-26 is in good agreement with the predicted output spectrum in Figure 3-13.

The amplifier efficiency, $\eta = P_{out}/(P_{dc} + P_{gate})$ shown in Figure 3-27 includes the

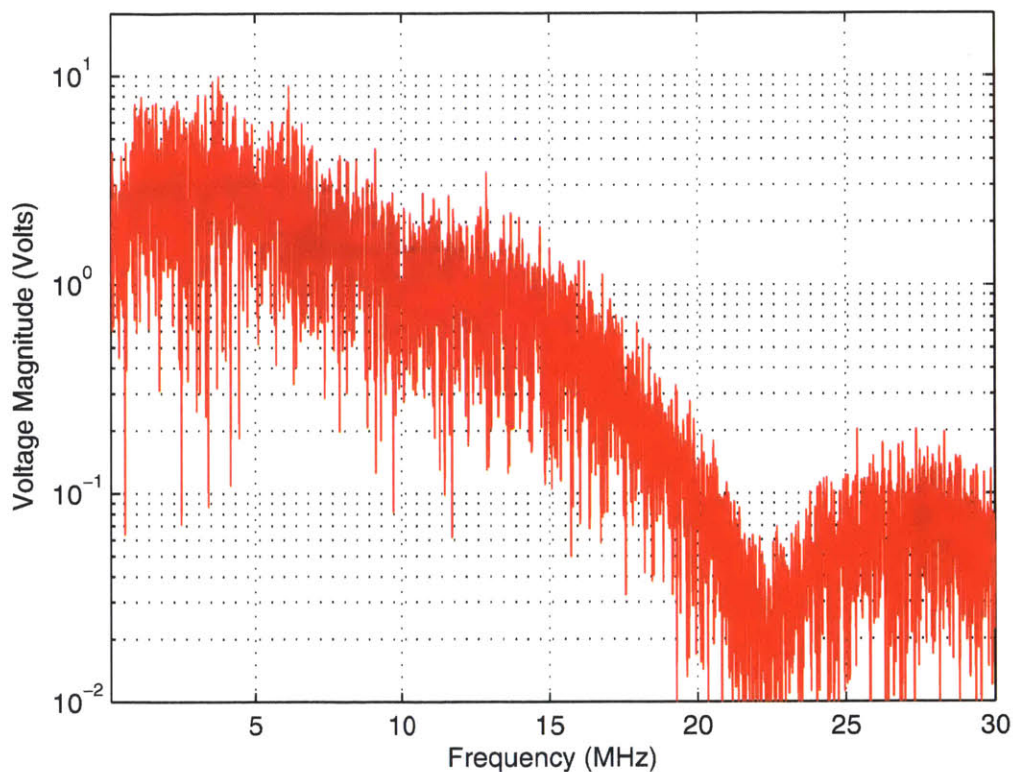


Figure 3-26: Output spectrum using an FFT of the experimental output voltage with a RBW = 9 kHz and a Gaussian window with 50 MHz bandwidth.

loss from the gate drive, which is 156 mW at 23 W and corresponds to the highest average operating frequency and drain voltage; the efficiency error bars are estimated to span about 2%. Above a certain power level, the drain clamps conduct, hence reducing efficiency. The drain clamps use a 3 W, 150 V Zener with a high voltage Schottky in series, which is conservative for the 200 V GaN FETs.

Over the variation in power and for a fixed $50\ \Omega$ load, the output voltage and hence the peak drain voltage vary. Because the device capacitances are voltage dependent, from (3.56) the resonant frequency of the pulse changes, resulting in an error in the zero durations, excessive body diode turn-on time, and subsequent pulse duty-cycle error. This results in decreased efficiency if switch timing is not corrected for drain voltage as illustrated in Figure 3-27. With this timing correction, which can be performed programmatically by the controller, an efficiency of up to 80% can be achieved.

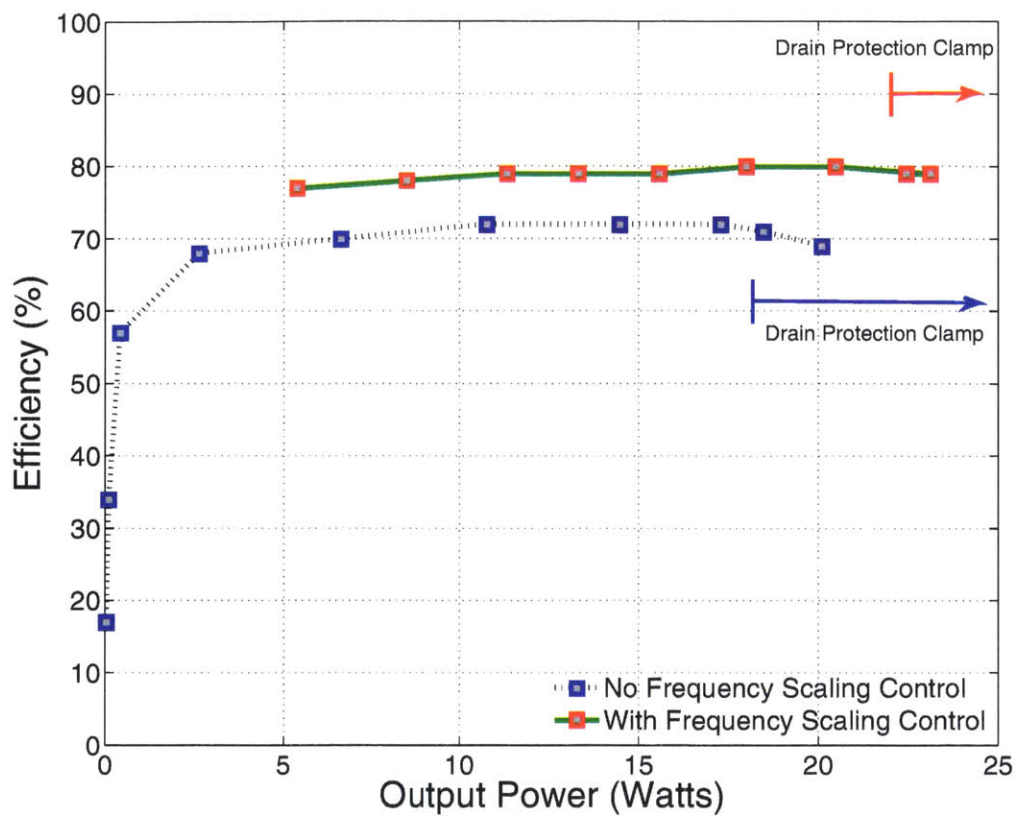


Figure 3-27: Efficiency.

3.4.7 QSPP Summary

We presented a new RF amplifier topology for spread spectrum power applications. This resonant topology improves on prior designs to operate at high frequency: zero voltage switching, a reduction in switch rms current, and absorption of device capacitance. Most of the transformer parasitics such as leakage inductance and most of the capacitances are also absorbed, while those that cannot can be made negligible. A 23 W prototype was demonstrated that operates at up to 80% efficiency, and over 90% of the power from 1–20 MHz. The amplifier uses a spreading sequence to control the switches so that both phase and pulse-position are directly modulated.

Applications for this technology include wireless power transfer, RFID, and electronic ballasts where EMI is an important concern, not only in critical applications such as medical environments, but also in portable and wearable applications.

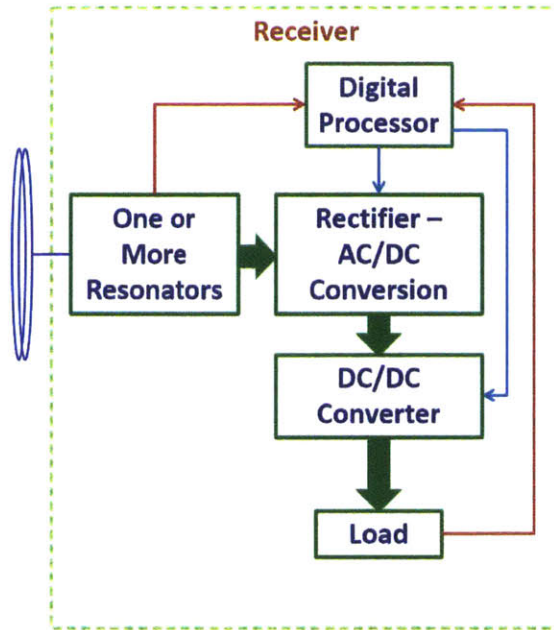


Figure 3-28: Passive Receiver Architecture

3.5 *Passive Spread-Spectrum Power Receivers*

To reduce the complexity of the receiver, passive energy conversion through a class of bandpass rectifiers was investigated. A conventional receiver architecture for wireless power transfer is shown in Figure 3-28. Although there is a plethora of work analyzing resonant rectifiers including [39, 51, 54], which have a resemblance to parts of this bandpass rectifier circuit, together with off-resonance operation and especially with spread-spectrum, where the main difficulty in analysis is that in higher order topologies, multiple diodes are used with inputs that are relatively well-coupled and have outputs which are common. We propose a design method that uses a surrogate model for optimization. Surrogate model optimization has been used for the design of microwave networks [65, 120] and in other engineering disciplines, but has not seen as wide of an application in power electronics.

There are different ways of receiving spread-spectrum power and converting it to dc; the simplest use passive tuned circuits that are matched to the spread power spectrum. Figure 3-29 illustrates several possibilities.

The bandpass rectifiers shown in Figure 3-29 are optimized for component values

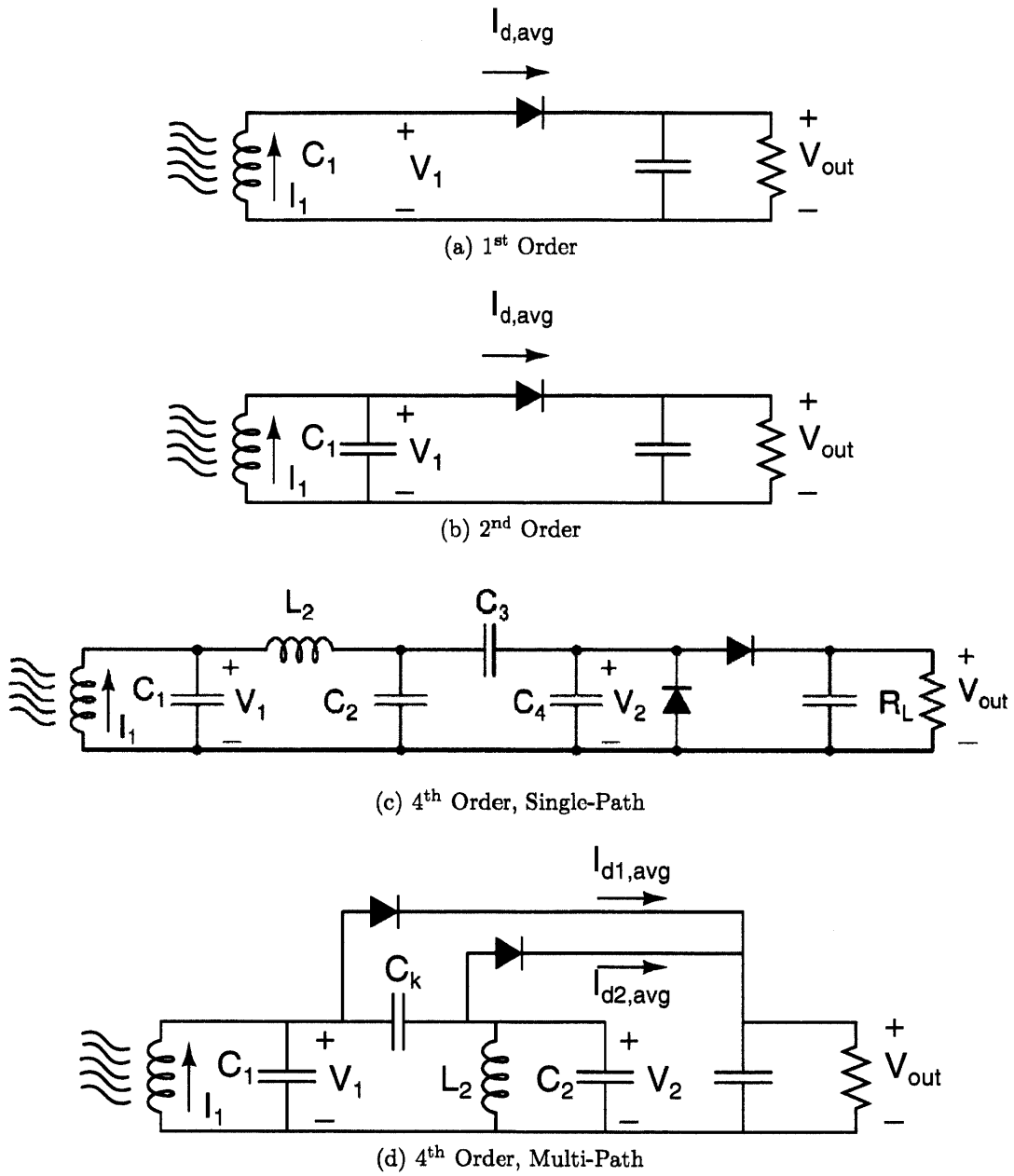


Figure 3-29: Bandpass Rectifiers

x for a given input voltage v_1 in (3.61),

$$\begin{aligned} & \underset{x}{\text{minimize}} && \max_{\omega} U(\omega, x) \\ & \text{subject to} && x_{min} \preceq x \preceq x_{max}. \end{aligned}$$

$$U(\omega, x) = \frac{|NI_p(j\omega, x)| + |I_s(j\omega, x)|}{\sum_{\omega} p(\omega, x)} \quad (3.59)$$

The optimization seeks to minimize the ratio of sum of the magnitudes of the amp-turns in the WPT transformer to the output power constrained by the bounds on the component values x , e.g. $x = (C_1, C_k, L_2, C_2, R_L)$ in Figure 3-29b . By adding the magnitudes of the amp-turns in (3.59), we optimize for a conservative bound on the amount of spurious field.

The primary current is $I_p = V_1/j\omega L_1$; the secondary current I_s and the point power density $p(\omega)$ is calculated from the direct solution of the mesh equations

$$v = (\mathbf{Z} + r\mathbf{I})i,$$

where r is a real parameter equivalent to a resistance for regularization so the conditioning is bounded over the range of trial component values.

3.5.1 Single-Path Rectifier, Fourth-Order Receiver

A principal goal in this thesis is to provide wireless power to biomedical devices such as those illustrated in Table 1.1. The majority of these devices require power below 0.5 W. Figure 3-29c illustrates a 4th-order bandpass rectifier where power is extracted through a single current path. The topologies that require only one rectifier are relatively straightforward in that there is a plethora of work analyzing these types of resonant rectifiers. Although analyses for resonant rectifiers have conventionally been for operation at resonance, based on power balance arguments using the average rectifier current and small enough output voltage ripple, one can still approximate the rectifier load as a resistor over a narrow range of operation. This results in an optimization of a linear system that can be directly tackled using a genetic algorithm. To extend the optimization space, we use an iterative method where one step is to optimize using this linear system approximation followed by a model correction from a non-linear, time-domain SPICE simulation. An illustration of this algorithm is shown in Figure 3-30.

A voltage source is a good approximation to the output of the QSPP amplifier

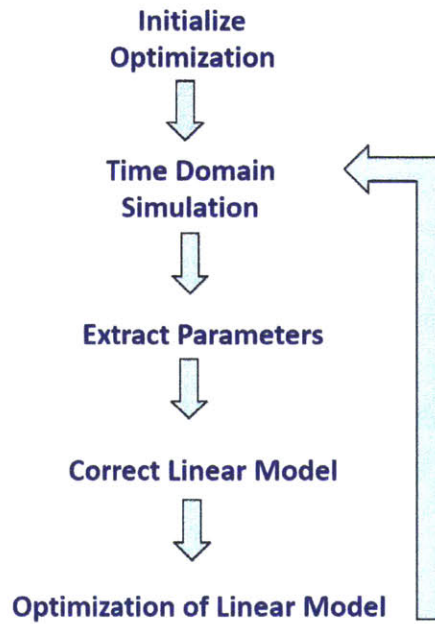


Figure 3-30: Algorithm for rectifier optimization

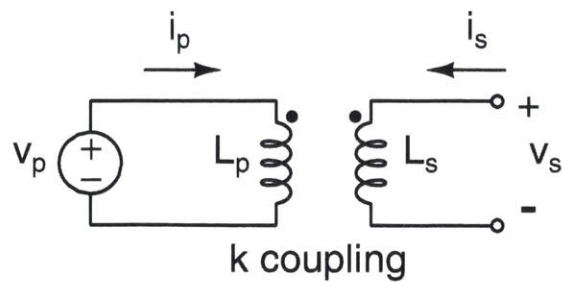


Figure 3-31: Transformer driven by a voltage source with coupling coefficient k .

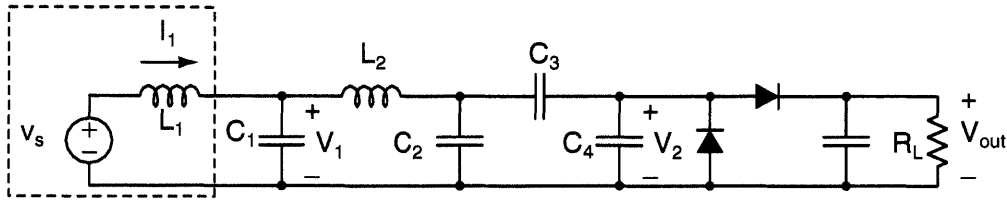


Figure 3-32: Fourth-Order Bandpass Receiver with Single-Path Rectifier

when the Q is high enough ($> \approx 3$) and the resonant inductance is much smaller than the WPT primary L_p . By using this approximation as a model as shown in Figure 3-31, we can reduce these transformer equations,

$$\begin{pmatrix} v_p \\ v_s \end{pmatrix} = L_s \begin{pmatrix} N^2 & kN \\ kN & 1 \end{pmatrix} \frac{d}{dt} \begin{pmatrix} i_p \\ i_s \end{pmatrix}, \quad (3.60)$$

where $N = \sqrt{L_p/L_s}$ is the turns-ratio and k is the magnetic coupling coefficient.

$$v_s = \frac{k}{N} v_p - (1 - k^2) j\omega L_s I_1, \quad (3.61)$$

where I_1 in Figure 3-32 is in the opposite direction of i_s . Equation 3.61 we can optimize resonant circuits using a voltage source $V_{in} = V_p k/N$ in series with an inductor $L_1 = (1 - k^2)L_s$ as the input as shown in Figure 3-32. For small k typical of WPT, L_1 is well-approximated by the secondary inductance L_s .

The circuit in Figure 3-32 is an LC ladder filter followed by a half-wave rectifier. C_2 , C_3 , and C_4 together form the second-stage capacitance of the ladder

$$\bar{C}_2 = C_2 + (C_3 \# C_4),$$

where $\#$ denotes the series capacitor operation². C_3 and C_4 form a 2nd-stage voltage divider that allows the output dc voltage to be lower, even if the resonant Q is high. This permits choosing an output (and consequentially, a rectifier) voltage that could be a better tradeoff. Lower sensitivity to rectifier capacitance can be attained vis-à-vis filter passband if $C_3 \# C_4 \ll C_2$ and vis-à-vis output voltage if $C_{\text{rect}} \ll C_4$.

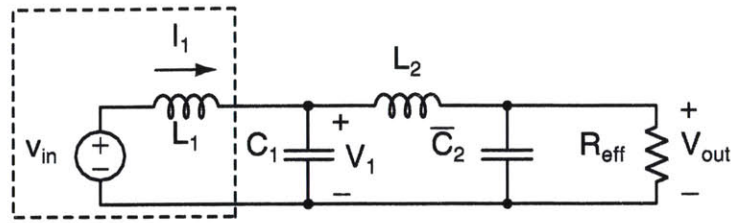


Figure 3-33: Linear Model for Fourth-Order Bandpass Receiver with Single-Path Rectifier

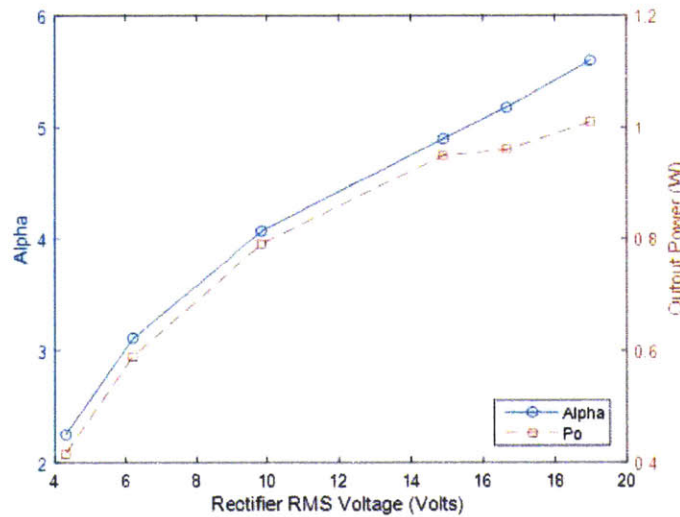


Figure 3-34: Parameter α from SPICE simulation.

Bandpass Rectifier Optimization Using a Genetic Algorithm

The rectifier load can be replaced by an effective resistance R_{eff} and parameterized by α ,

$$\frac{V_{\text{dc,out}}^2}{R_{\text{load}}} = \alpha \frac{V_{\text{rect,acrms}}^2}{R_{\text{eff}}}, \quad (3.62)$$

which is derived from power balance as illustrated in Figure 3-33. This simply means that the power removed from the resonant ladder circuit is simply the power dissipated at the dc load R_{load} . Although α and R_{eff} appear redundant, the separation is required because R_{eff} is a circuit element in the linear circuit and also an optimization variable while R_{load} is a component in the nonlinear circuit. Both reside in different spaces with α connecting: R_{eff} linear in the frequency domain and R_{load} in the nonlinear time domain.

²In general, $a \# b = \frac{ab}{a+b}$.

In Figure 3-34, through time-domain simulation in SPICE, α is calculated with R_{load} and R_{eff} held fixed as input voltage v_s to the bandpass rectifier is swept. What is notable is that α appears monotonic with rectifier rms voltage and also appears to track with output power.

The algorithm can be described as:

1. Perform initial GA optimization on linear model for R_{eff} , C_1 , L_2 , and \bar{C}_2 .
2. Use GA optimization results R_{eff} , C_1 , L_2 , and \bar{C}_2 to run a nonlinear time domain simulation of the real system. R_L can be derived from R_{eff} in (3.62).
3. Use steady-values for $\{V_{out}$ and $V_{2,rms}\}$ to derive α .
4. Run GA optimization for R_{eff} , C_1 , L_2 , and \bar{C}_2 using α to solve for R_L in the objective function.
5. Goto step 2 until stopping criterion is reached, e.g. \mathcal{Z} non-decreasing.

Figure 3-35 shows the response of a 4th-order bandpass receiver that was optimized with a genetic algorithm. In this optimization, both the spectrum of v_{in} and the component values were optimized at the same time. A point-wise optimization of the input voltage spectrum is possible, but computationally intensive because of the number of optimization variables. An alternative would be to optimize over parameters that represent the shape of the spectrum. The input voltage is optimized through a parameterization of the values and locations of the points of a piecewise linear fit; the points reside non-uniformly because the optimization naturally places a higher density of points where the features change the most. This results in a good representation of the spectrum for a relatively small number of points. There are upper and lower bounds on the frequency and these are handled by rejecting points outside of the bounds, which works well in practice; a more computationally intensive algorithm is to reflect the points from the boundaries. The spectrum represented by the piecewise linear approximations is resampled uniformly to calculate the objective function for the optimization with a constraint on the total power from the squared-sum at these points. The component values are listed in Table 3.4. A 70 V schottky diode was used as a rectifier instead of the next-lower 30 V because the peak voltage exceed the lower-rated rectifier at the nominal maximum 1.55 W dc output power.

A transmitter spread-sequence that has a narrower spectrum is a better match for a 4th-order passive receiver as indicated in Figure 3-35. This narrow spectrum can be implemented by optimizing sequence as in §2.1 with a duty-cycle $D = 0.95$. The

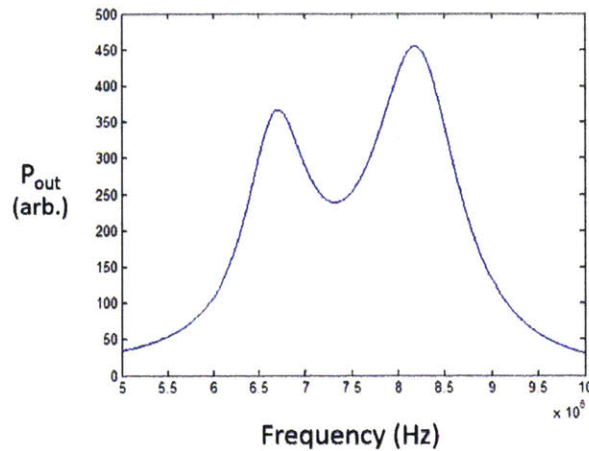


Figure 3-35: Response of a 4th-order bandpass receiver with a single rectifier path that was optimized with a genetic algorithm.

Table 3.4: Receiver Component Values

| Component | Value |
|-----------|-----------------|
| L_1 | 2.2 μ H |
| C_1 | 315 pF |
| L_2 | 22 μ H |
| C_2 | 6.5 pF |
| C_3 | 33 pF |
| C_4 | 100 pF |
| C_{out} | 0.1 μ F |
| R_L | 1.15 k Ω |
| Rectifier | MMSD701LT1 |

top plot in Figure 3-38 is the FFT of the transmitter output measured at the input terminals of the WPT coil. The bottom plot is the spectrum analyzer trace from a Tektronix MDO 4054B with a Beehive 100C large-loop inductive probe.

As we can see from Figure 3-38 for the WPT coils shown in Figure 3-36, the spectrum analyzer was set with a resolution bandwidth (RBW) of 10 kHz. The peak occurs at 6.05 MHz with a value of 35.1 dBm. Using a Beehive 100C inductive mag-

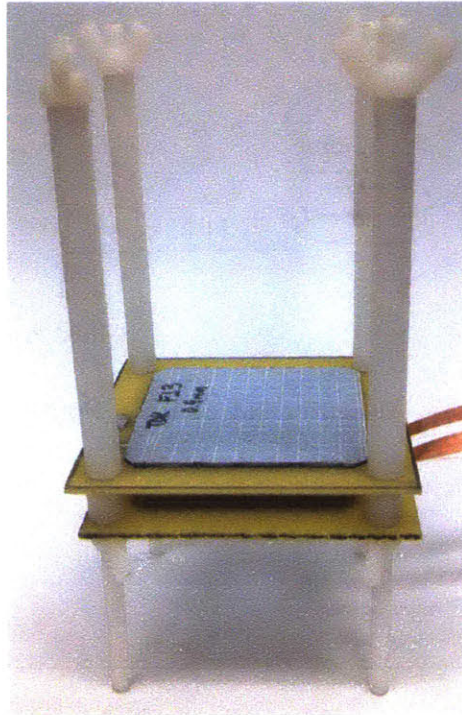


Figure 3-36: Test Setup for Wireless Power Transfer Coils. TDK FJ3 pre-cracked ferrite was used on the posteriors of both the transmit and receive coils.

netic field probe, this corresponds to $0.165 \mu\text{T}$ and in free-space a magnetic field of 0.131 A/m . The magnetic field was measured 11.43 cm away from the WPT coils (3 cm radius) along the axis with the strongest signal (along the coplanar midline of the two coils) as illustrated in Figure 3-37. The CISPR limit is $15 \text{ dB}\mu\text{A/m}$ at 3 m , which corresponds to $5.62 \mu\text{A/m}$ at this distance. Assuming a dipole roll-off ($1/r^3$) in magnetic field, the spurious field from the WPT system transferring 1 W would be $7.25 \mu\text{A/m}$ at 3 m , which is just above the CISPR limit. The power that can be transferred at the CISPR limit for this WPT system would be 0.6 W . The measured and calculated magnetic-coupling coefficient for the configuration is approximately $k = 0.2$.

Experimental results are plotted in Figure 3-39. In Figure 3-39a, dc input voltage to the QSPP transmitter was swept from 5 V to 16 V for a fixed output load resistance of $1.14 \text{ k}\Omega$, which results in an output dc voltage that spans 5 V to 24 V ; power output spans 0.4 W to 1.2 W . Output load is varied from $0.7 \text{ k}\Omega$ to $1.3 \text{ k}\Omega$ in Figure 3-39b with a fixed dc input to the QSPP transmitter of 16 V . This corresponds to a top-end efficiency of about 20% at about 1.55 W .

⁴Frequency shifted to align with spectrum analyzer trace.

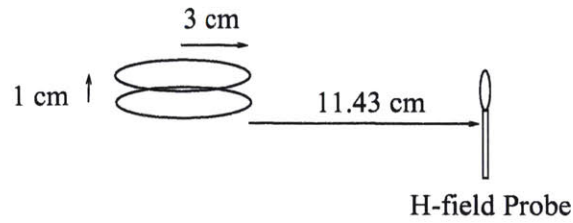


Figure 3-37: Measurement of WPT Spurious Field

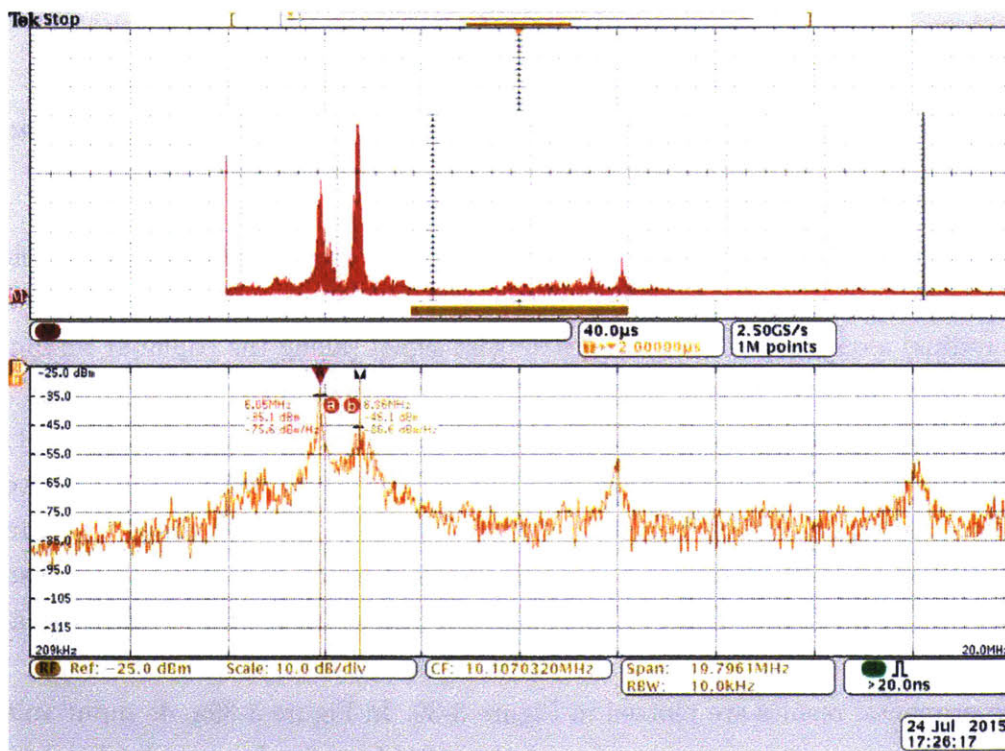
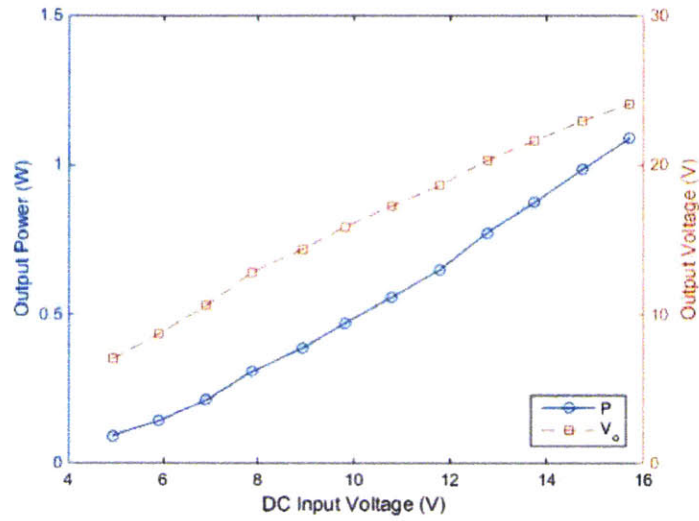
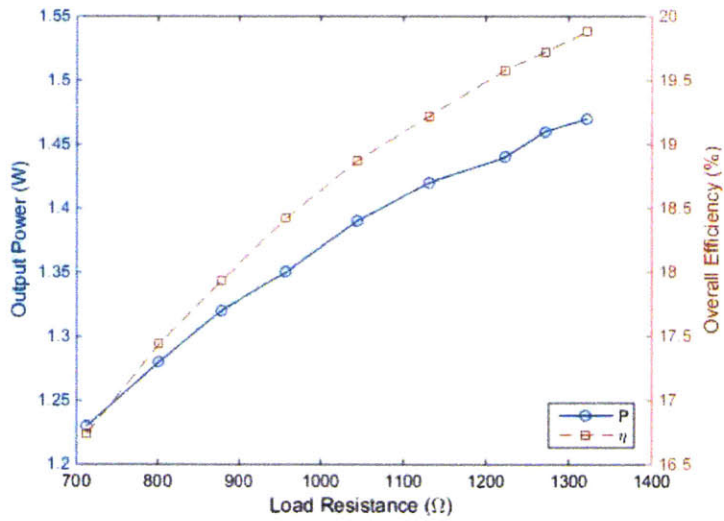


Figure 3-38: Spectrum measurements for narrow sequence with a fourth-order passive filter. $D = 0.95$ and magnetic coupling coefficient $k = 0.25$. Top Trace: FFT of Transmitter Output⁴. Bottom Trace: Spectrum Analyzer Using Inductive EMI Probe.

Section 3.5 : Passive Spread-Spectrum Power Receivers



(a) Input/Output



(b) Load Pull

Figure 3-39: Experiment results of power output from 4th-order, single-path rectifier with narrow spread spectrum.

3.6 Chapter Summary

This chapter encompassed the end-to-end hardware required to accomplish spread-spectrum wireless power transfer. Although the transmitter considerations and design was directed towards the general application of spread-spectrum wireless power transfer, the goal of the overall system design for this thesis pertains to biomedical applications with powering or charging requirements in the hundreds of milliwatts or less while remaining below regulatory standards for electromagnetic interference. Passive bandpass receivers were explored for straightforward implementation and a design is discussed and demonstrated that met the requirements.

A new RF amplifier topology was presented for spread spectrum power applications. This resonant topology improves on prior designs to operate at high frequency: zero voltage switching, a reduction in switch rms current, and absorption of device capacitance. Most of the transformer parasitics such as leakage inductance and most of the capacitances are also absorbed, while those that cannot can be made negligible. A 23 W prototype was demonstrated that operates at up to 80% efficiency, and over 90% of the power from 1–20 MHz. The amplifier uses a spreading sequence to control the switches so that both phase and pulse-position are directly modulated.

Applications for this technology include wireless power transfer, RFID, and electronic ballasts where EMI is an important concern, not only in critical applications such as medical environments, but also in portable and wearable applications.

Chapter 4

Single-Sided, Time-Varying, Spatially-Uniform Magnetic Fields

MAGNETIC delivery of wireless power can be inefficient in the quasistatic regime because typically the effluence of energy is isotropic. In this chapter, we investigate and discuss an approach to project power from only one side of a magnetic surface. We study these methods using induction heating, which in its own right is wireless power transfer, as a surrogate.

The first part of this chapter discusses the consideration, design, and testing of creating an ac magnetic field that is single-sided using an arrangement of layers of windings without a core [10]. We then expand this concept to creating a uniform single-sided field using spatially-orthogonal windings driven by frequency-orthogonal current drives [15].

4.1 Single-Sided, Time-Varying Magnetic Fields

Induction heating is used in industrial [85], medical [76, 108], and home consumer [5, 74] applications. One of the key concerns in induction heating is containing the stray magnetic fields; solutions include both active and passive shielding, which are extrinsic to the induction coil design [94–99].

We demonstrate a new winding arrangement based on a Halbach array, which in an ideal form results in a field on only one side of a geometric surface [43, 67]. These surfaces can be general and along with planar designs, cylindrical and spherical surfaces, among others, are possible [88, 101]. Traditionally, these Halbach configurations

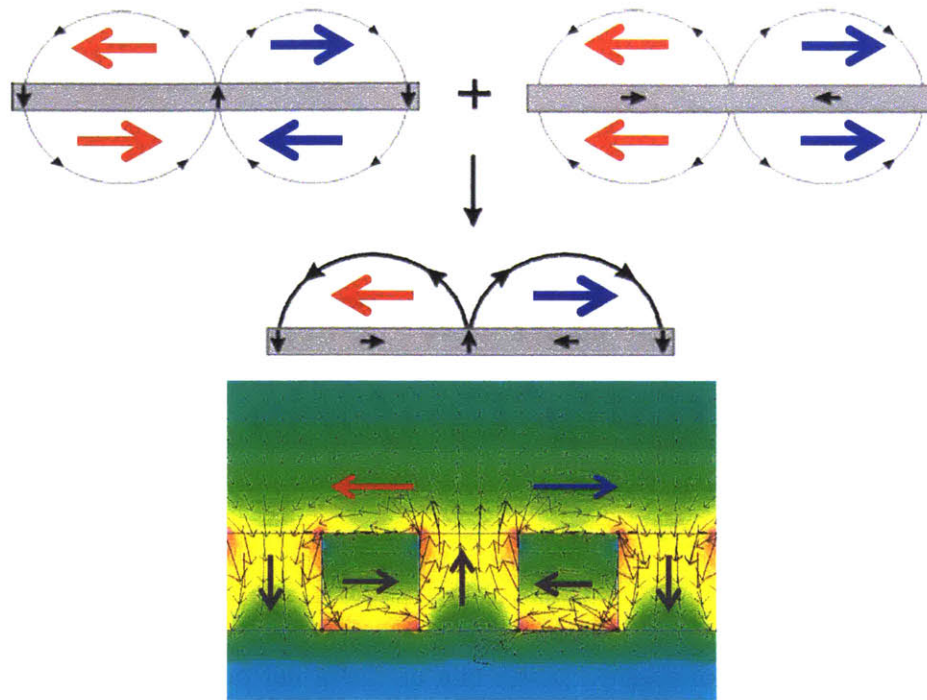


Figure 4-1: DC Halbach Array [114].

have been used to generate dc magnetic fields, but we show that ac fields can also be generated with one-sided characteristics.

In this chapter, we present both finite element simulation and experimental results for a prototype winding arrangement of a planar induction heater based on a two-dimensional Halbach configuration. By using a Halbach winding configuration, the flux cancelation is achieved implicitly without the use of passive shields such as ferrite plates, conductor plates, or active shielding. In doing so, cost, weight, and size are reduced, along with an improvement in mechanical robustness by not using ferrites.

4.1.1 Halbach Winding

Both Halbach [43] and Mallinson [67] independently posited magnetization configurations that elicit one-sided magnetic fluxes. Some of the theory for the ideal cases is derived in [101]; in the ideal case, the field has a sinusoidal variation on the plane of the array, falls off exponentially from the top surface, and is zero below. We can derive the magnetic flux density at a point z above and x along the Halbach surface with thickness d as

$$B = \mu_0 M_0 (1 - e^{-kd}) e^{-kz} \cos kx, \quad (4.1)$$

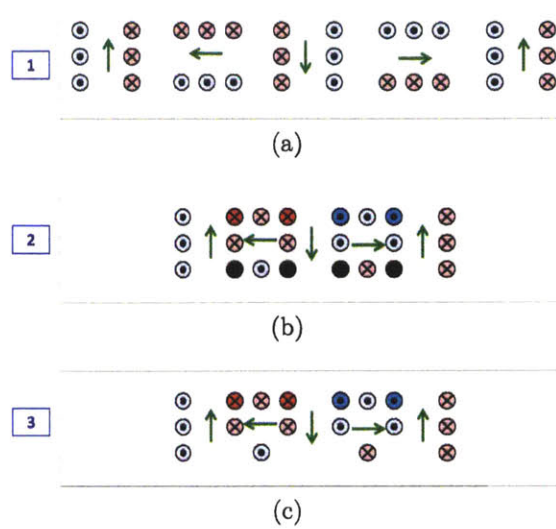


Figure 4-2: Compression of a Unit Cell for a Wound Halbach Array.

where $k = 2\pi/\lambda$ is the radian reciprocal of the array wavelength for a wound Halbach array $M_0 = \alpha kNI$, where NI are the amp-turns and α is a geometric factor.

The faster fall-off in field resulting from a Halbach surface can be advantageous in induction cooking appliances, including wide area, flexible cooking zones [88] because the bottom of the pans are close to the surface so power transfer can be achieved while still minimizing stray fields.

Figure 4-1 illustrates the construction of a one-sided dc field using magnetizations from block permanent magnets. It shows how the superposition of an alternating pattern of vertical and horizontal magnetizations combine to produce twice the field on top and none on the bottom. For this case of a non-sinusoidal magnetization, a spatial Fourier decomposition could be used for analysis similar to [121], with the fundamental component given by Equation 4.1.

An example of a wound dc Halbach array can be found in [121]. In Figure 4-2a, we approximate each magnetization with a three turn winding. If we compress the windings together as in Figure 4-2c, there is a doubling of amp-turns in some of the turns in the top layer, and cancelations on the bottom layer. This arrangement reduces the winding complexity with a decreasing winding density with each layer. Figure 4-3 shows the top layer of a two-dimensional implementation of the array. A two-dimensional approach means that each layer can be wound independently, which results in a reduction in winding and hence manufacturing complexity. Figure 4-4 illustrates the lap windings schematically for each layer.

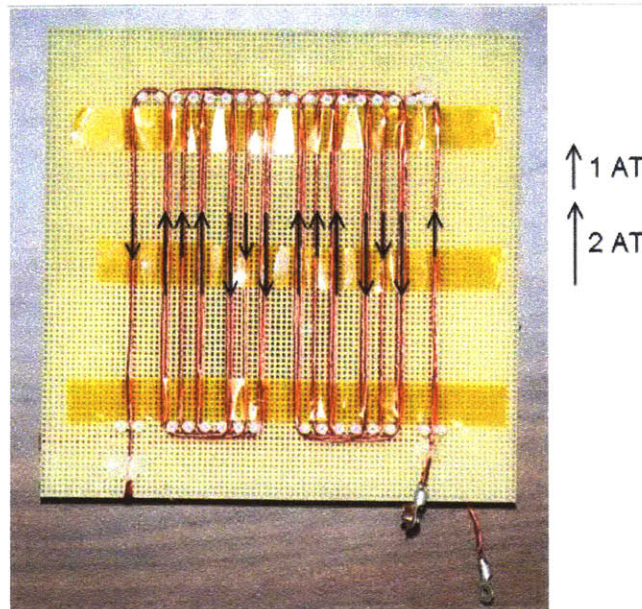


Figure 4-3: Two-Dimensional Winding Halbach Approximation. Arrows indicate per unit ampere-turns for the top layer of the winding structure. \rightarrow 1 AT; \longrightarrow 2 AT.

4.1.2 Finite Element Simulations

We performed finite element simulations in COMSOL for frequency-dependent magnetic induction. In addition, we performed a simulation using a multiphysics model that included heat conduction, convection, and radiation.

Magnetic Field Modeling

We performed simulations at the nominal operating frequency of 500 kHz. By using a thin-wire approximation, skin and proximity effects in the winding can be neglected; this is a valid model for an experiment if the appropriate Litz wire is used.

Figure 4-5 illustrates two-dimensional simulations of the magnetic flux density for several winding configurations. Our three-layer Halbach winding arrangement is shown. What is noticeable is that the additional field below from adding a steel target on top of a Halbach winding is negligible. In addition, one observes that in comparison to a winding where only the top winding layer is used, the complete three-layer Halbach winding has a significantly higher concentration of magnetic flux above and a field that does not extend as far below.

Spiral windings are commonly used in induction stove applications [5]; the configuration shown does not have the typically used ferrite substrate, and thus results in

Section 4.1 : Single-Sided, Time-Varying Magnetic Fields

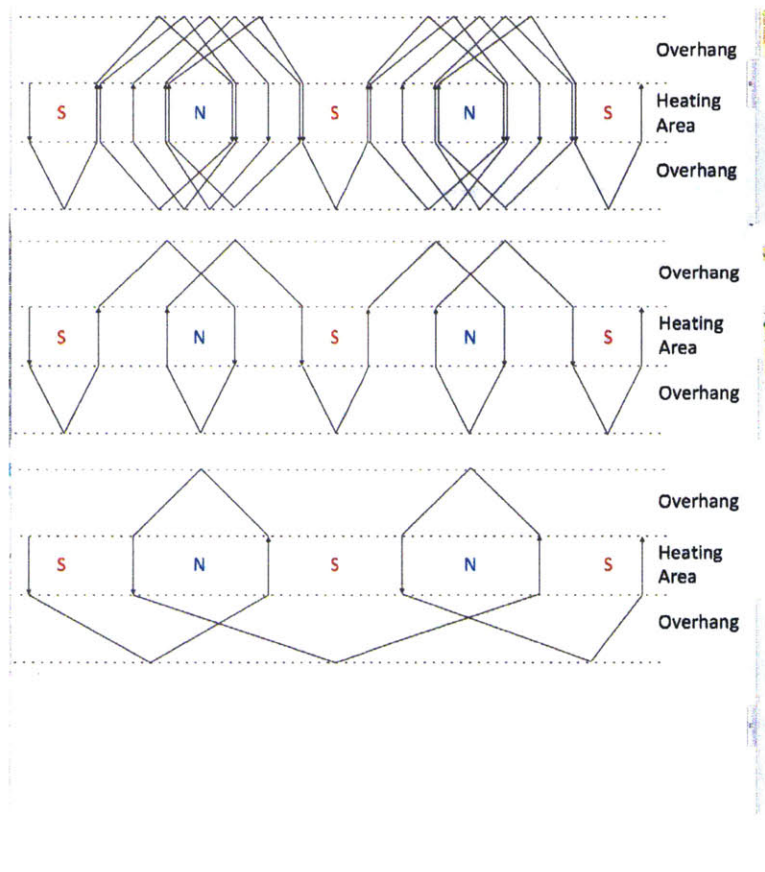


Figure 4-4: . Lap Winding Pattern for the Top, Middle, and Bottom Layers.

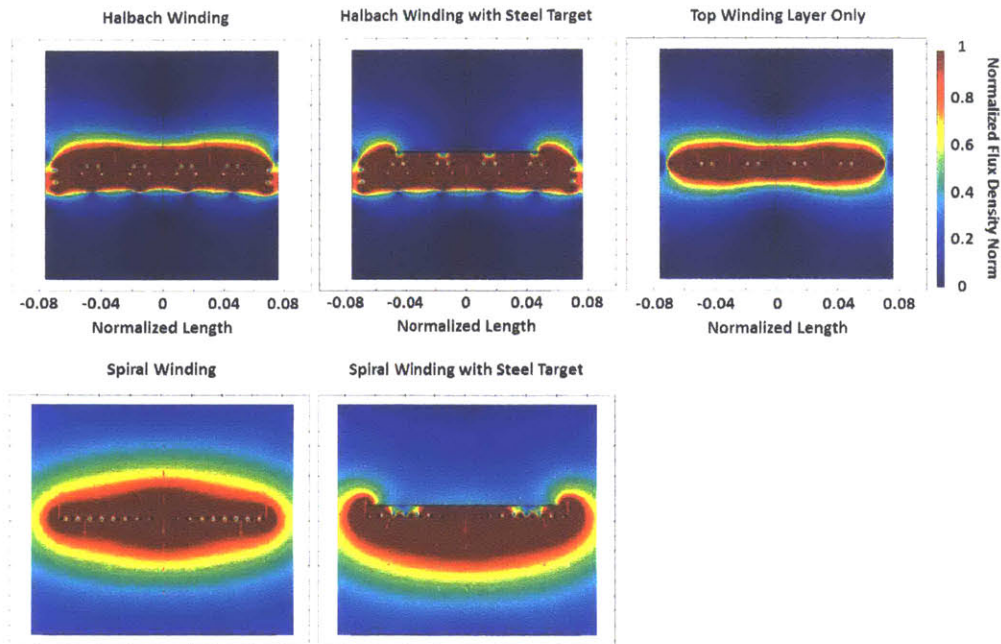


Figure 4-5: Finite Element Simulations of Magnetic Flux Density.

an extensive two-sided field. One observes that in placing a steel target, the flux at bottom increases and extends farther; this can imply that if a ferrite substrate were used on the bottom, the flux density it must carry is larger with a heating target, hence possibly resulting in higher overall loss.

If we use a solid conductor winding and increase the diameter and frequency, proximity effects begin to dominate and distortion in the magnetic field occurs, resulting in decreased flux above and increased field below; this is illustrated in Figure 4-6.

Multiphysics Modeling

We performed a multiphysics simulation in Figure 4-7 that includes models for heat conduction, convection, and radiation. The effect of resistive heating from the winding was discounted in the simulation by enforcing a thermally insulating boundary at the surface of the wire. Temperature dependent target resistivity is included as well. The results are given for steady-state temperature and power level. The simulation deviates from measurements at higher temperatures presumably because of regime changes in the convection model.

Section 4.1 : Single-Sided, Time-Varying Magnetic Fields

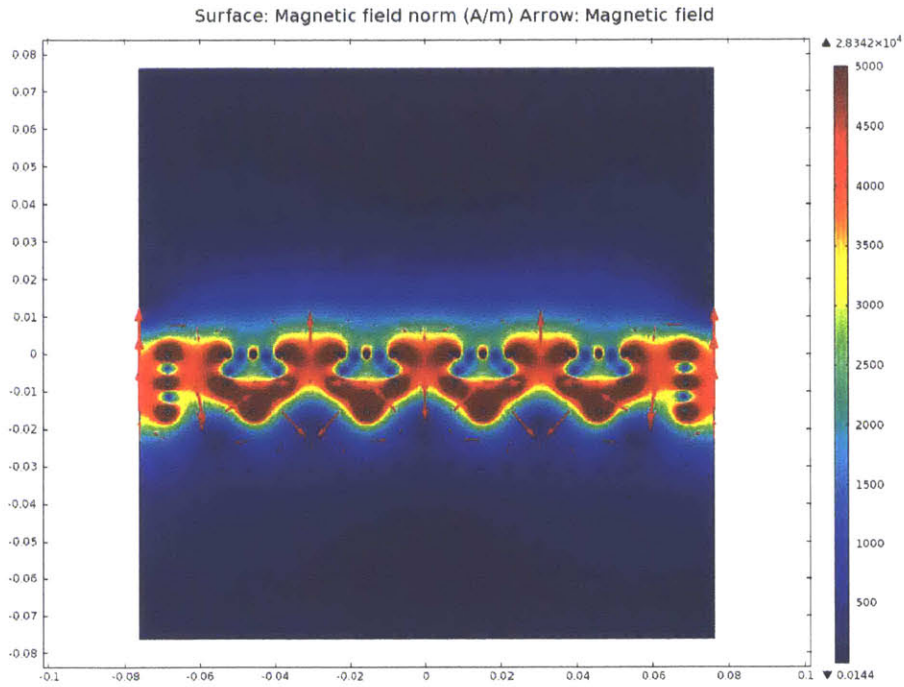


Figure 4-6: Field distortion of the Halbach winding array occurs at 500 kHz because of current density distortion from the proximity effect. Litz wire can minimize the effect.

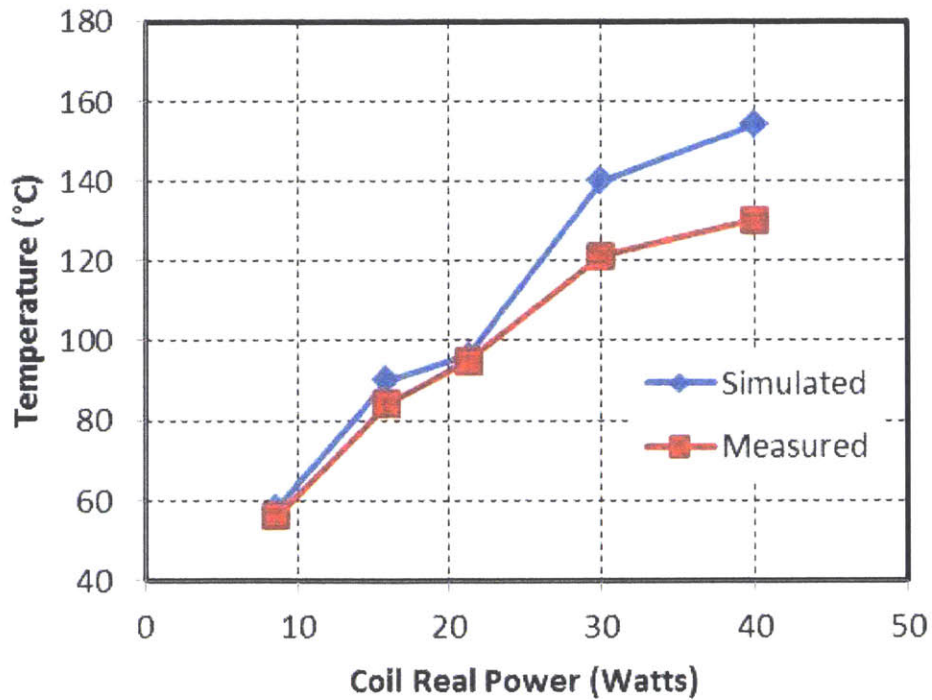


Figure 4-7: Multiphysics finite element model includes heat convection, conduction, and radiation, along with magnetic induction.

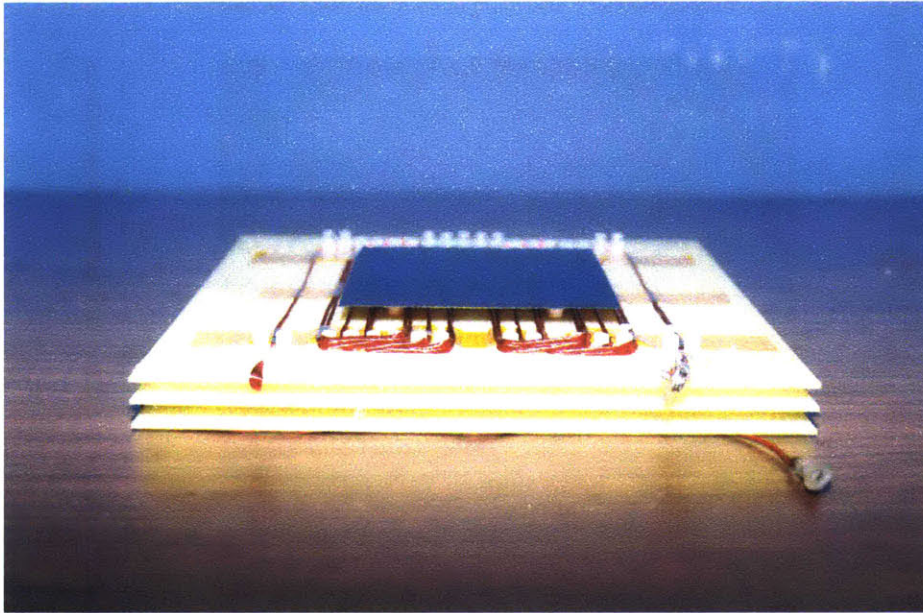


Figure 4-8: Induction coil with steel target showing lap winding structure to minimize end-turn fringing field.

Experimental Results and Discussion

We constructed a prototype Halbach winding array on an FR4 perforated board, which is illustrated in Figure 4-8. It consists of three layers, as in Figure 4-2. By lap winding the end turns, a significant number of the current segments cancel, hence reducing stray fields at the ends. Thin magnetic steel was used as a target to increase the in-plane thermal time constant, so that transient thermal effects could be observed using an infrared camera. Transient thermal behavior, i.e. step response to power, is useful in determining heating distribution and uniformity. The heating distribution is an indicator of the induced currents and hence magnetic flux distribution at the target. The top surface of the target was coated with high temperature black paint and calibrated to a thermocouple to calculate an emissivity of 0.97, which is needed for infrared temperature measurements.

Table I delineates the parameters relevant to the experiments. The nominal operating frequency was chosen to maximize the ratio of the unloaded to the loaded Q for the particular target. This maximizes the target heating relative to the coil resistive loss.

The induction coil was connected as part of a series resonant circuit to a half-bridge MOSFET inverter in Figure 4-9. The series capacitor is a parallel combination of ceramic capacitors for high current capability.

Table 4.1: Induction Heating Parameters

| Coil Parameters | |
|-------------------------------|--|
| Nominal Operating Frequency | 500 kHz |
| Unloaded Q | 78 |
| Front Loaded Q | 26 |
| Rear Loaded Q | 73 |
| Inductance | 8.2 μ H |
| Winding Pitch (inches/mm) | 0.3/7.6 |
| Layer Spacing (inches/mm) | 0.3/7.6 |
| Copper Litz Wire | 175 strands \times 40 ga/0.08 mm |
| Target Parameters | |
| Material | AISI 1008 Steel |
| Thickness | 10 mil/0.25 mm |
| Dimensions (inches/cm) | 4/10.2 \times 4/10.2 \times 4/10.2 |
| Nominal Relative Permeability | 1500 |
| Nominal Resistivity | $130 \times 10^{-9} \Omega \cdot m$ |
| Skin Depth at 500 kHz | 6.6 μ m |
| Thermal Conductivity | 59.5 W/m \cdot K |
| Specific Heat | 481 J/kg \cdot K |
| Density | $7.87 \times 10^3 \text{ kg/m}^3$ |
| Coating Emissivity | 0.97 |
| Gap to Coil (inches/mm) | 3.8/9.5 |

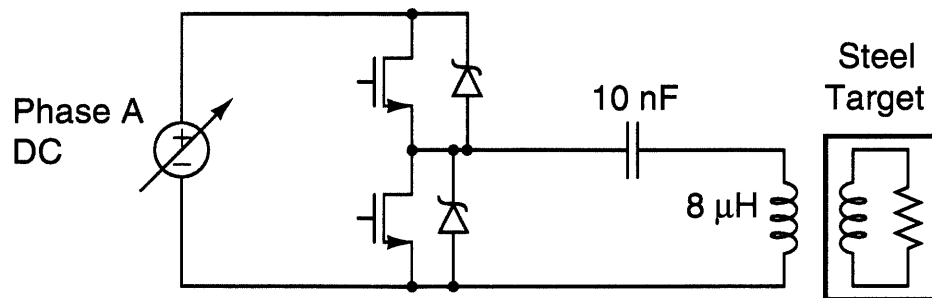


Figure 4-9: Half-bridge inverter is used to drive series resonant circuit.

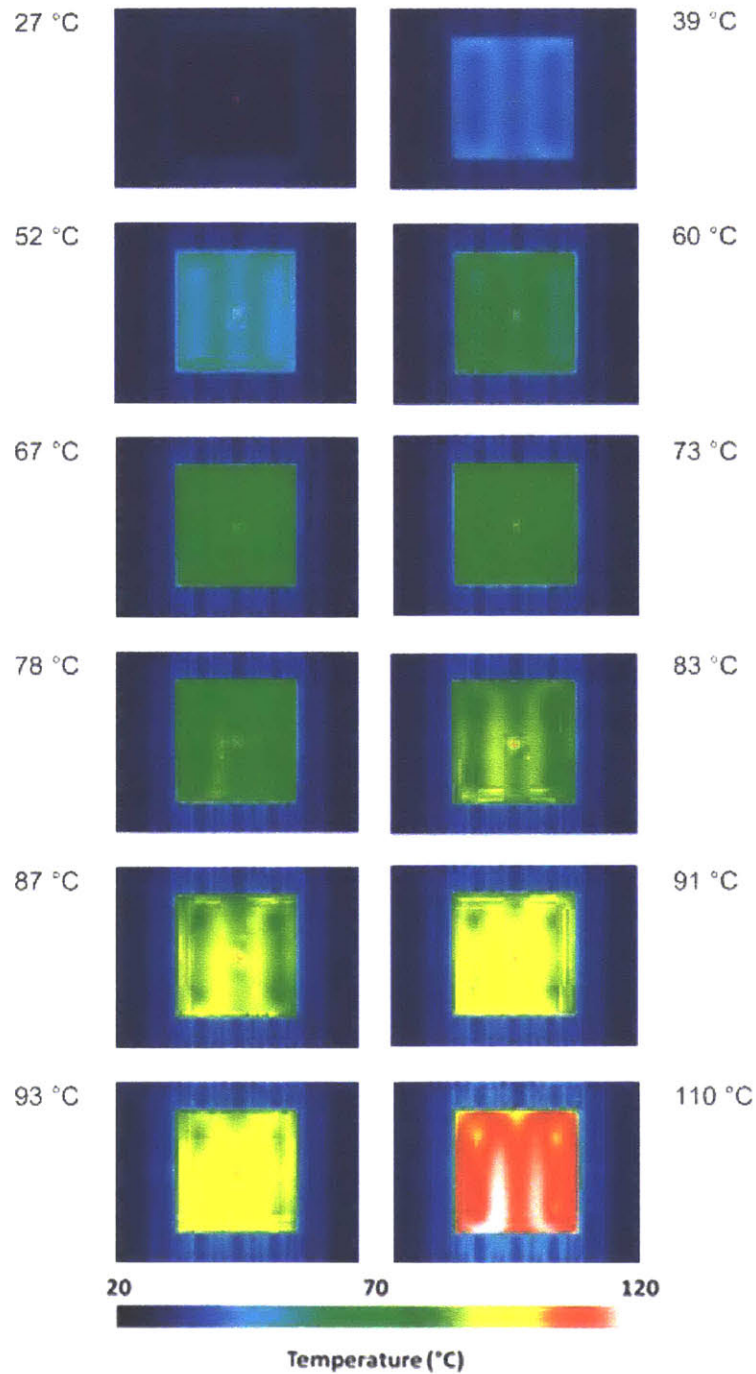


Figure 4-10: Time/Temperature Evolution of Target Heating.

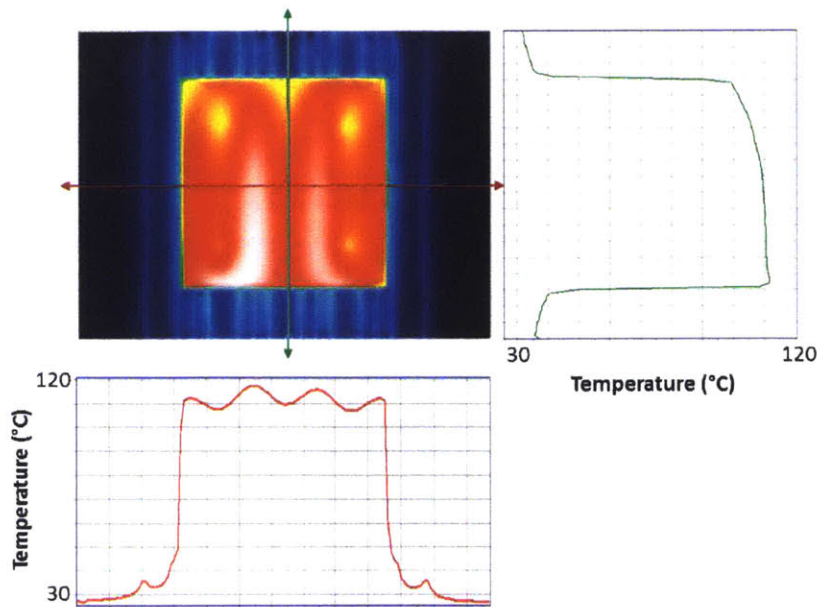


Figure 4-11: Temperature profile of target on top of Halbach winding along the lines bisecting the target. Bisection lines along which the corresponding temperature profiles are measured are shown. The spatial axis of the temperature profile corresponds to that of the image.

We used a Fluke TI 20 to image the target heating in the infrared. Figure 4-10 shows the evolution of heating with a step input in sinusoidal coil current amplitude. This only approximates a step in power because target resistance is a strong function of temperature. There appears to be a small air current from the air conditioning along the top of the target appearing vertically in the figures, which becomes more pronounced at higher temperatures.

From the images, we also extracted the temperature profiles along the two bisecting axes of the target. In Figure 4-11, the temperature profiles along each direction appear relatively uniform. The temperature profile within the heating zone in the horizontal axis shows a sinusoidal variation, which is what is expected from a thermal low-pass of the intensity of the inductively coupled magnetic flux from a Halbach array.

Figure 4-12 is a salient illustration of a single-sided flux. The target is only heated by the resistive losses from the hotter winding. The thermal radiation from the bottom winding is apparent through the perforated FR-4 substrate. No inductive heating pattern is apparent in the temperature profile of the target.

The inductive heating element has a relatively well-defined heating zone, which

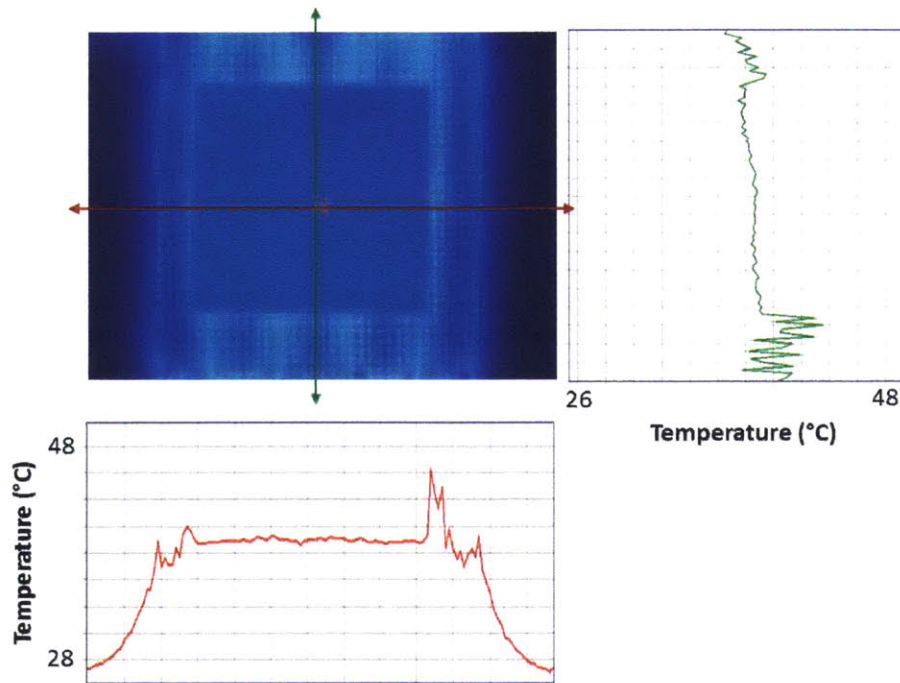


Figure 4-12: Temperature profile of steel target on the bottom side of the Halbach induction winding shows negligible inductive heating. Temperature rise is due to the resistive heating in the winding. Bisection lines along which the corresponding temperature profiles are measured are shown. The spatial axis of the temperature profile corresponds to that of the image.

is illustrated in Figure 13. This is consistent with the magnetic flux distribution on the target in Figure 5. Beyond the heating zone, the expected exponential drop-off from heat diffusion is apparent. This shows that edge effects are not that significant in that a relatively sharp boundary is formed for the heating zone, which is also consistent with the simulations shown in Figure 4-5. Figure 4-13 also serves as a partial illustration and comparison of the heating effects on circular and rectangular targets.

4.2 Spatially-Uniform Magnetic Fields

This section presents a Halbach winding arrangement based on maximizing the ratio of energy distribution on the top compared to the bottom for a given winding configuration. The investigation leads to an optimized Halbach winding with only two layers of conductors. Further, a second two-layered Halbach winding can be superimposed that is spatially orthogonal to the original winding to create a multiphase Halbach winding arrangement. Ideally the two windings are decoupled by the spatial arrangement; using currents that are temporally orthogonal leads to a traveling magnetic field, resulting in uniform heating. Temporal orthogonality is implemented by exciting two currents at the same frequency but 90° out of phase. In practice, a small coupling between the windings exists because of finite tolerances. This leads to difficulty in simultaneously maintaining the phase orthogonality and controlling the individual magnitudes of the two currents. By using two different frequencies, both temporal orthogonality and independent magnitude control can be achieved, enabling a uniform heating profile. An 8 inch x 15 inch prototype designed with the proposed concept is used to demonstrate uniform single sided induction heating along with the associated resonant circuits.

4.2.1 Multi-Phase Halbach Winding Design

Halbach arrangements of permanent magnets have been used in the rotors of permanent magnet motors [27]. These Halbach arrangements are attractive because the back iron of the electrical motor can be eliminated reducing mass and inertia. For induction heating applications, such as an induction cooktop, where only one sided heating is necessary, a Halbach arrangement can significantly reduce the need for magnetic shields at the bottom, which typically consist of ferrites and conductor plates. The magnetic field in the induction cooktop needs to be time-varying to induce cur-

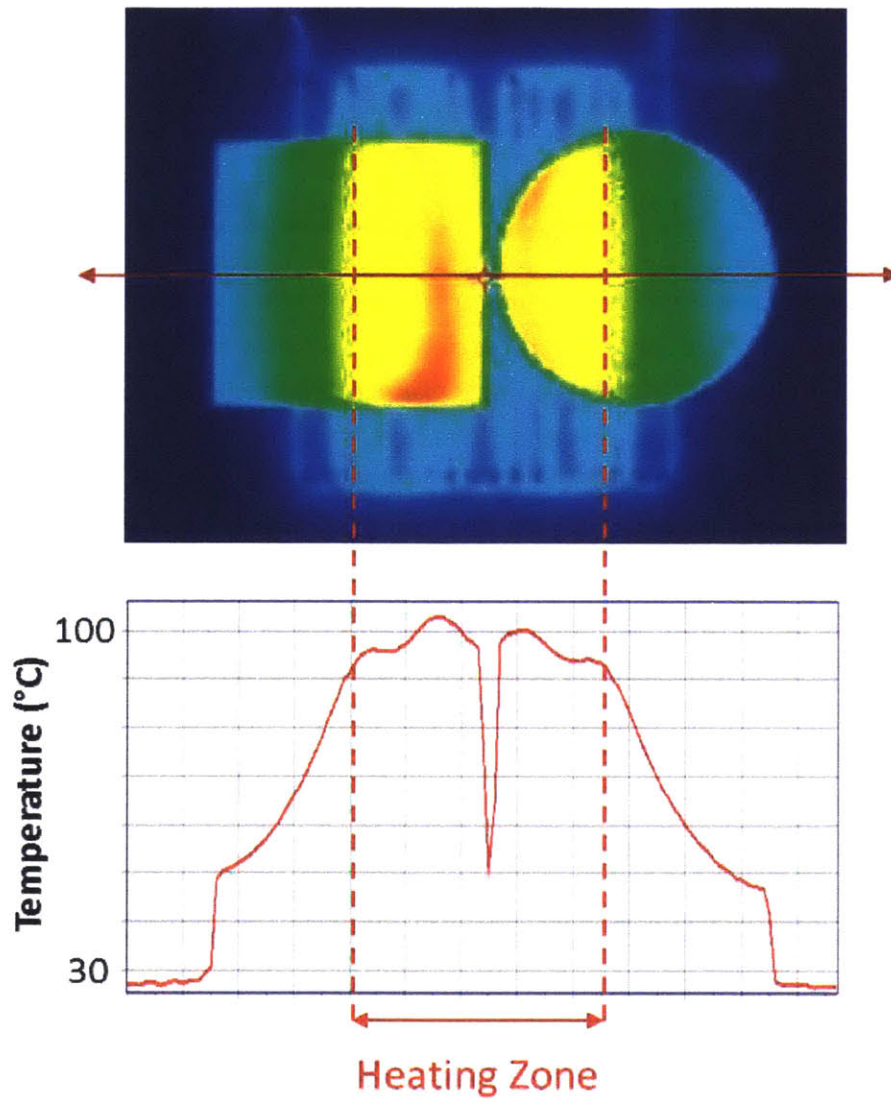


Figure 4-13: Heating Zone. The bisection line along which the corresponding temperature profile is measured is shown. The spatial axis of the temperature profile corresponds to that of the image.

rent on the target for Joule heating. This requires windings that carry time-varying currents placed so that a magnetic field is produced only on a single side.

The following section discusses the design of a winding arrangement that can emulate a Halbach array so that the magnetic field on the top is much greater than the bottom. The design is based on a four-step process. First, the magnetic field and the stored energy are calculated in different sections for an arbitrary arrangement of conductors in an enclosed volume. Second, the conductor ampere-turns (AT) and locations are optimized so that the magnetic energy on the top dominates. Third, the effect of introducing highly permeable materials at the top and bottom of the optimized conductor arrangement is then investigated using a finite element simulation. Finally the conductors are connected so that the appropriate current polarities form a Halbach winding array.

Stored Energy in the Magnetic Field for an Arbitrary Conductor Arrangement

An arbitrary conductor arrangement $(C_1, C_2, C_3, \dots, C_k)$ is considered within a rectangle $ABCD$ of length L and height h as shown in Figure 4-14. In a three-dimensional coordinate frame, the rectangle is assumed to have unity dimension in the z -direction. The conductors carry different amp-turns (ATs), either positive or negative, along the z -direction. The magnetic field at a distance (x, y) due to each of these conductors can be calculated from Ampere's Law. Assuming that the magnetic field has no variation along the z -direction, the net magnetic field at (x, y) due to the complete arrangement can be calculated by superposition and is given by,

$$H_{x,net} = -\frac{1}{2\pi} \sum_{i=1}^K \frac{c_i(y - y_i)}{(x - x_i)^2 + (y - y_i)^2} \quad (4.2)$$

$$H_{y,net} = \frac{1}{2\pi} \sum_{i=1}^K \frac{c_i(x - x_i)}{(x - x_i)^2 + (y - y_i)^2} \quad (4.3)$$

$$\vec{H}_{net} = H_{x,net} \hat{x} + H_{y,net} \hat{y}. \quad (4.4)$$

To emulate the characteristics of a Halbach array, the energy stored on the top section of the conductor arrangement, represented as $ABEF$ in Figure 4-14 must be significantly greater than the energy stored in the bottom section, represented as $DCHG$. Assuming that the conductor arrangement is periodic along the x -direction with periodicity of length L but with alternating polarity of ATs, the boundary con-

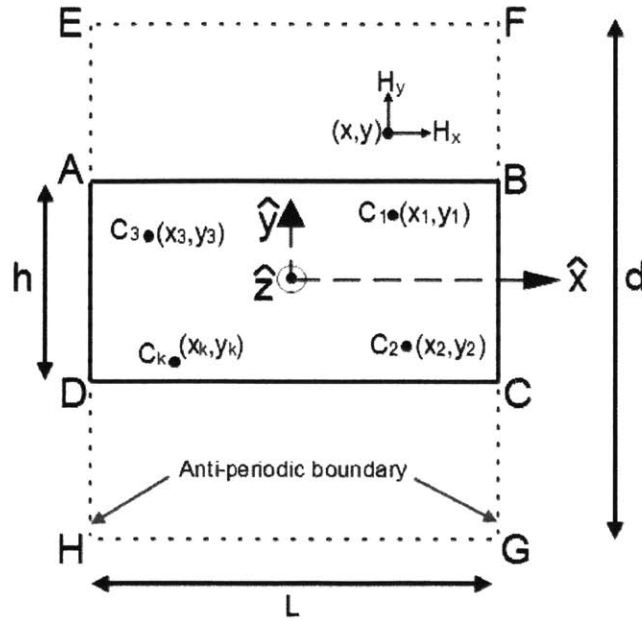


Figure 4-14: Arbitrary arrangement of conductors carrying current in the z -direction in enclosed area $ABCD$.

dition along EH and FG can be applied as

$$H_{x,EH} = H_{x,FG} = 0 \quad (4.5)$$

$$H_{y,EH} = -H_{y,FG}. \quad (4.6)$$

Assuming $EFGH$ is free space, the stored energy in the three sections, top $ABEF$, middle $ABCD$ and bottom $DCGH$, are given by,

$$E_{top} = \frac{\mu_0}{2} \int_{-L/2}^{L/2} \int_{h/2}^{d/2} H_{net}^2 dy dx \quad (4.7)$$

$$E_{bottom} = \frac{\mu_0}{2} \int_{-L/2}^{L/2} \int_{-h/2}^{h/2} H_{net}^2 dy dx \quad (4.8)$$

$$E_{middle} = \frac{\mu_0}{2} \int_{-L/2}^{L/2} \int_{-d/2}^{-h/2} H_{net}^2 dy dx. \quad (4.9)$$

Optimization of Conductor Arrangement Using a Genetic Algorithm

The design goal is to optimize the conductor locations (x_k, y_k) and the ampere-turns C_k of the K conductors in $ABCD$ to maximize the ratio of the magnetic field at the top to the magnetic field at the bottom. Quantitatively, the directional property can be expressed by a parameter Γ , the *Directivity*, which is defined as the ratio of total

magnetic energy on the top to the total magnetic energy in the bottom,

$$\Gamma = \frac{E_{top}}{E_{bottom}}. \quad (4.10)$$

Additionally, the effectiveness of the conductors in transferring energy to the top relative to the energy stored in the middle and the bottom can be indirectly measured using the parameter Λ , the *Effectivity*. This is defined as the ratio of total magnetic energy on top to the sum of the total energies stored in the middle and bottom,

$$\Lambda = \frac{E_{top}}{E_{bottom} + E_{middle}}. \quad (4.11)$$

The reciprocal product of Γ and Λ is used as the cost function for the conductor arrangement optimization. Based on reducing the complexity of the final winding structure and the spatial harmonic content of the magnetic field, three constraints are placed on x_k , y_k and C_k . First, constraining y_k between two discrete levels $+h/2$ and $-h/2$ enforces two layers of conductors to synthesize the winding pattern. This minimizes the amount of copper required, as well as reducing the cost of manufacturing for the overall winding. However, h is a free optimization variable that determines the distance between the two layers. Second, constraining C_k to only signed integer values (\mathbb{Z}) allows the use of a single continuous wire for constructing the winding. Finally, symmetry across the y -axis, shown in Figure 1, is imposed to eliminate the even harmonics in the spatial distribution of the magnetic field. That is, if a conductor is placed at (x_k, y_k) carrying the C_k AT, there must be another conductor placed at $(-x_k, y_k)$ carrying equal AT. The symmetry requirement enforces bounds on x_k between the origin and half of the length. The complete optimization problem is given by,

$$\begin{aligned} & \underset{x_i, y_i, C_i, h}{\text{minimize}} && S = \frac{1}{\Gamma\Lambda} \\ & \text{subject to} && |x_i| < \frac{L}{2}, \\ & && |y_i| \in \left\{ -\frac{h}{2}, \frac{h}{2} \right\}, \\ & && C_i \in \mathbb{Z}, \\ & && (-x_{1+K/2}, y_{1+K/2}, C_{1+K/2}) = (x_i, y_i, C_i), \\ & && i \leq \frac{K}{2}. \end{aligned}$$

Table 4.2: Optimization of an Example Design: Parameters and Variable Bounds

| Parameters | Values |
|------------|------------|
| L | 1.2 inches |
| K | 6 |

| Variables | Lower Bound | Upper Bound |
|-----------|-------------|-------------|
| h | 0.05 inches | 0.4 inches |
| Z | -1 | 1 |

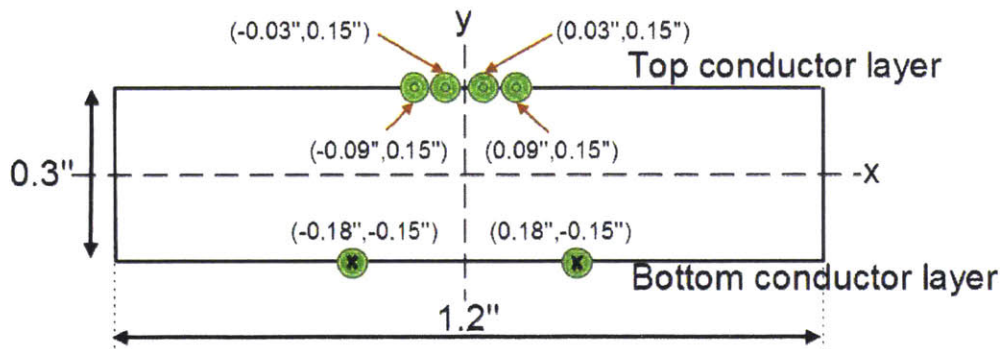


Figure 4-15: Optimized Halbach cell with six conductors for the chosen parameter and geometry bounds.

Table I summarizes the actual values chosen for the different variables for an exemplary design of a Halbach conductor arrangement using six total conductors. The optimization is run in MATLAB using the Genetic Algorithm in the Optimization Toolbox. For ease of numerical integration to evaluate stored energy in different sections using (3), the bounds on the integral are chosen such that they do not enclose the conductors.

Figure 4-15 shows the optimized conductor placement and ATs generated by the genetic algorithm based on the parameters and constraints. The magnitude of the magnetic field, H for the optimized conductor arrangement is calculated using (2). The near-sinusoidal variation of the magnitude along x -direction at a certain distance away from the top layer is shown in Figure 4-16. As expected, the magnitude decreases with an increase in distance in the y -direction. Figure 4 shows the variation of magnitude of the magnetic field as a function of distance along y -direction at $x = 0$. The dashed lines demarcate the location of the top conductor layer and the bottom conductor layer. As expected, the bottom conductor layer drastically improves the

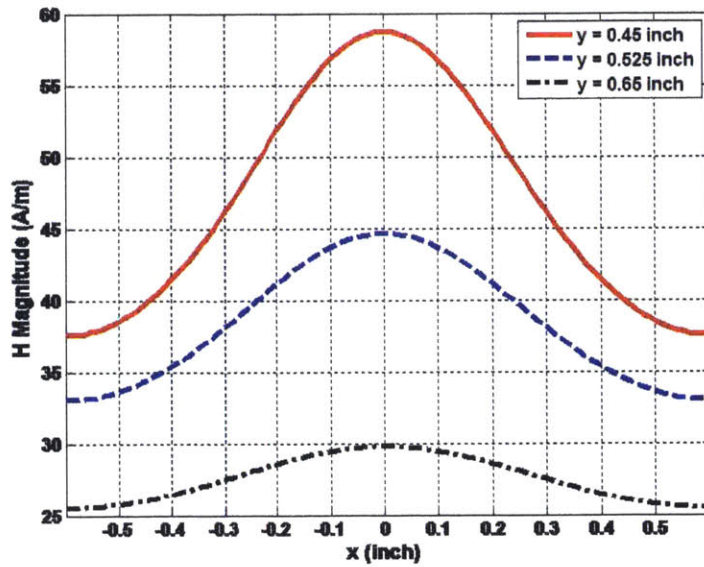


Figure 4-16: Near-sinusoidal variation of the magnetic field along x -direction for the optimized Halbach conductor arrangement using six conductors.

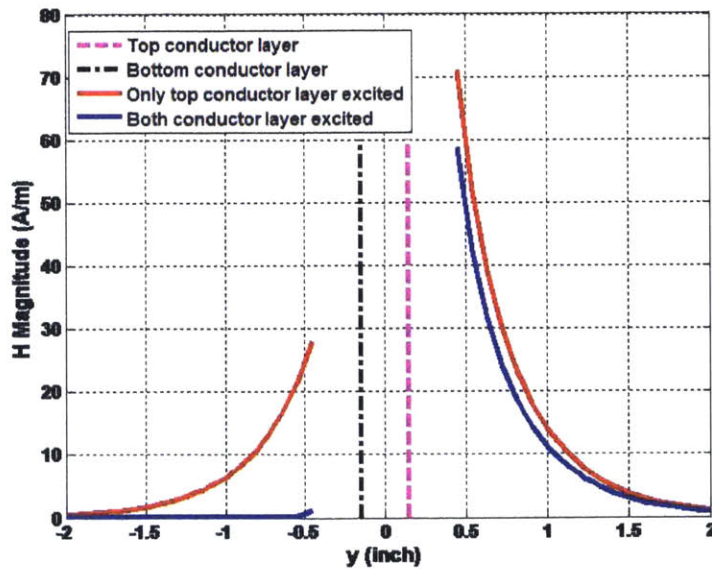


Figure 4-17: . Rapid roll-off of the magnetic field on the bottom of the cell compared to the top in the presence of the bottom conductor layer.

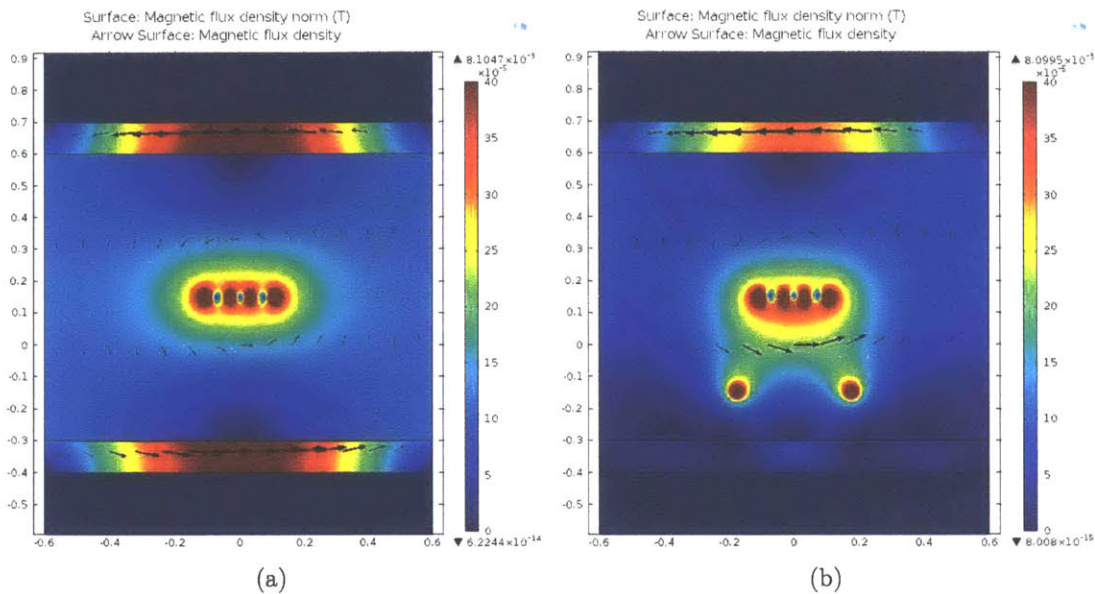


Figure 4-18: Finite element analysis using COMSOL to evaluate presence of high permeable target on the top and the bottom equidistant from the top winding layer (a) Equal flux density on the top and bottom permeable material with unexcited bottom conductor layer (b) Higher flux density on the top compared to bottom with excitation enabled in the bottom conductor layer.

roll off of the magnetic field at the bottom so that it is negligible at 0.5 inches away. It is clear that this effect is not due to the distance as the absence of the bottom conductor layer increases the magnetic field in the bottom. A less significant impact from the bottom conductor layer can be observed on the top side magnetic field. The magnetic field pattern as shown in Figure 4-16 and Figure 4-17 closely resembles the field pattern from an ideal Halbach array [12].

So far the computation of the energy and the optimization has been based on the assumption that the conductors are in free space and without any permeable material (target) in proximity. A static finite element analysis is performed in COMSOL to evaluate the presence of a highly permeable material in proximity to the optimized Halbach cell. Figure 4-18 shows the flux density distribution when two highly permeable (steel) targets are placed equidistantly from the top conductor layer. Without energizing the bottom conductors, equal flux density is observed on both of the targets, as expected. The excitation of the second layer cancels much of the field on the bottom compared to the top. The conductors between the adjacent cells, when connected together with the correct current polarity, form a single-phase winding with multiple cells behaving together to form a complete Halbach array.

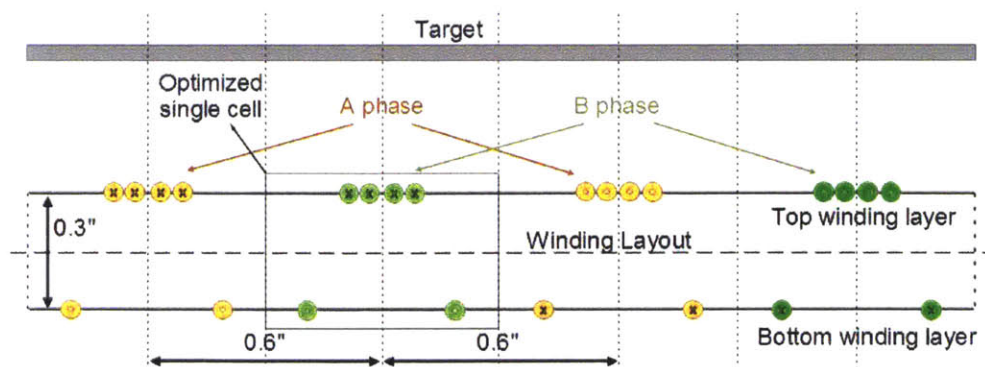


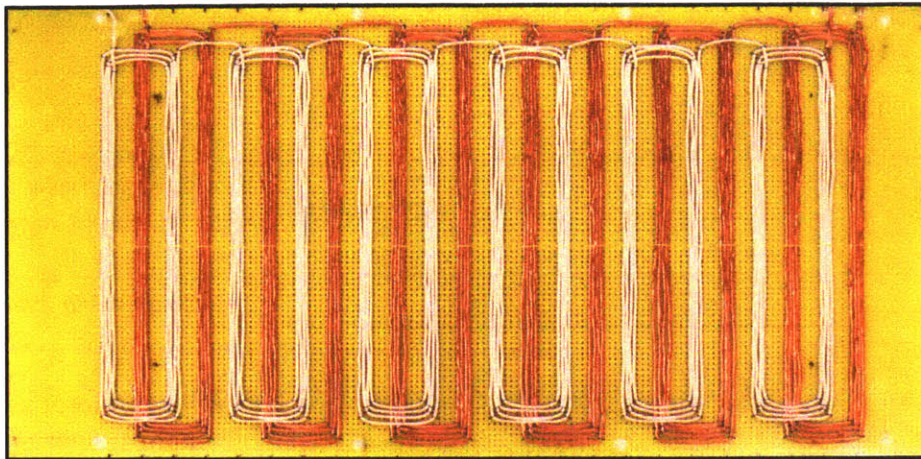
Figure 4-19: Two phase winding layout using optimized Halbach conductor arrangement such that the windings are orthogonal in space to enable uniform heating of the target when placed on top.

Realization of a Two-Phase Halbach Winding for Uniform Heating

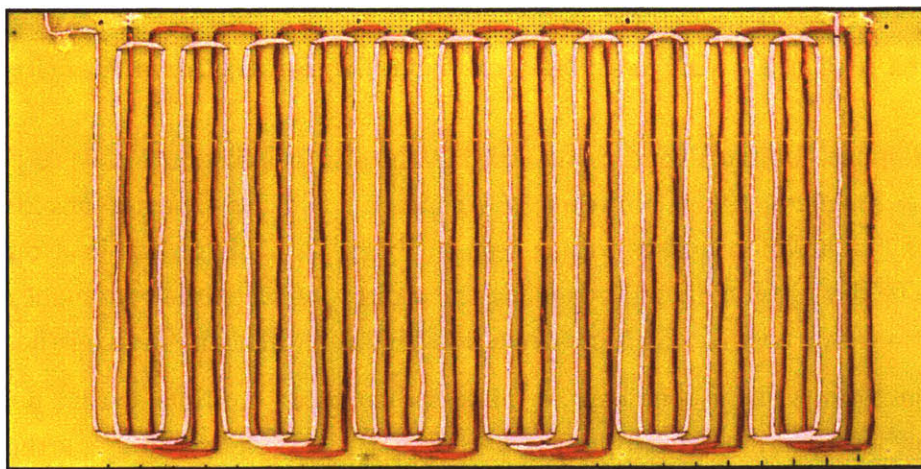
The single-phase Halbach winding designed in the previous section is able to produce directional magnetic fields. However, the magnetic field has a near-sinusoidal variation along x -direction on the top as seen in Figure 3. This results in a pulsating magnetic field of varying magnitude along the x -direction when the winding is excited with time-varying current. This creates a non-uniform heating pattern on the target.

Non-uniformity in heating can be mitigated by using multiple spatial phases of Halbach windings. In the example winding design, a two-phase winding structure is created by interleaving two sets of the Halbach windings such that they are spatially orthogonal, i.e. the flux from one of the phase windings ideally does not couple with the other phase winding. The two-phase windings layout and dimensions are shown in Figure 4-19.

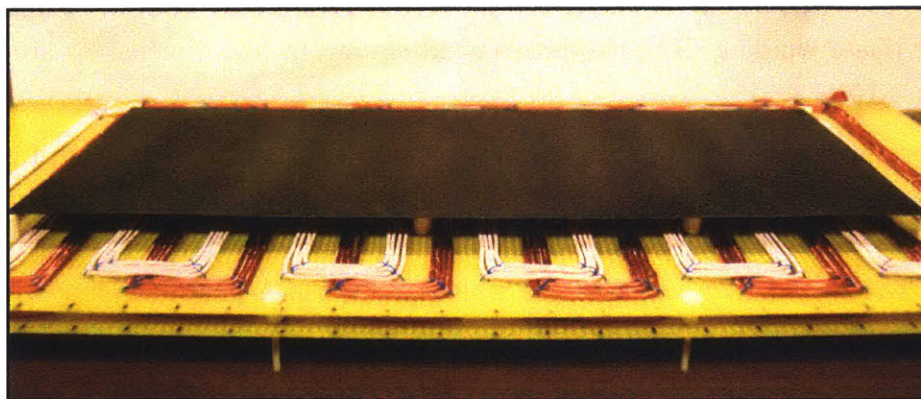
The example winding layout is based on Figure 4-19 constructed using Litz wire (175 strands \times 40 ga) on an 8.5" \times 17" G-10 board. Twelve optimized cells are used for each phase as shown in Figure 4-20 to obtain a demonstrable length of uniform heating. The served Litz wire (seen as white) forms the A-phase winding while the unserved one (seen as red) forms the B-phase winding. Kevlar thread is used to keep the Litz wire in place on the G-10 board. Figure 4-20a shows the top winding layer of the two phases and 4-20b shows the bottom winding layer of two phases. The two winding layers are assembled with a gap of 0.3 inch as shown in Figure 4-20. A steel target is shown on the top of the winding at a distance of 3/8th inch above the top layer.



(a)



(b)



(c)

Figure 4-20: Prototype of the optimized two phase Halbach winding: white—Phase A and red—Phase B (a) Top winding layer (b) Bottom winding layer (c) Assembled winding structure with steel target on top.

4.2.2 Winding Excitation Using a Resonant Inverter

A series resonant circuit operating at hundreds of kHz can excite the currents in an induction heating coil. The proposed two-phase (A & B) winding structure requires two resonant circuits to excite the individual phases such that the currents in the two phases are orthogonal in time. A simple approach for realizing temporally orthogonal currents in two phases is to drive the phases at same frequency but one with a sine and the other with a cosine excitation. However, because of practical winding imperfections, there is mutual coupling between the two phases, i.e. current is induced in the B-phase even when only the A-phase is energized and vice versa. The mutual coupling makes it challenging to have independent excitation control for each of the phases. Therefore, the two phases are designed to resonate at two different frequencies where the separation in tuning attenuates the effect of mutual coupling. The time orthogonality of the excitation currents is achieved on a time-averaged basis. Since the heating of the target is based on the average power dissipation, the overall excitation for the two phases at different frequencies produces uniform heating.

This section discusses the multi-resonant circuit used to drive the two phases of the winding structure. An ac analysis is performed in a lumped parameter SPICE model showing the effect of mutual coupling between the two phases when either phase is excited individually. The SPICE model will also be used to show the benefit of exciting the two phases with different frequencies even in the presence of mutual coupling. Finally, an average power transfer model is used to derive the heating pattern on the target based on the magnetic field when the individual phases are excited with different frequencies. The analytical formulation shows that the average power transfer to the target is position independent along x -direction.

Multi-Resonant Excitation of a Two-Phase Winding

Tuning the excitations for the resonances of the two phases, requires measuring the terminal impedances of the prototype winding. The parameters are measured using an impedance analyzer. The measured inductance of the A-phase is 16.12 μH while the measured inductance of the B-phase is 16.85 μH . Additionally, the measured mutual inductance between the two phases is 0.71 μH . Based on these measurements, the coupling coefficient k is calculated to be only 4%.

To evaluate the effect of even a weak mutual coupling between the two phases on resonant excitation, a simplified lumped model of the prototype winding is used in SPICE as shown in Figure 4-21. For simplicity, the distributed capacitive coupling

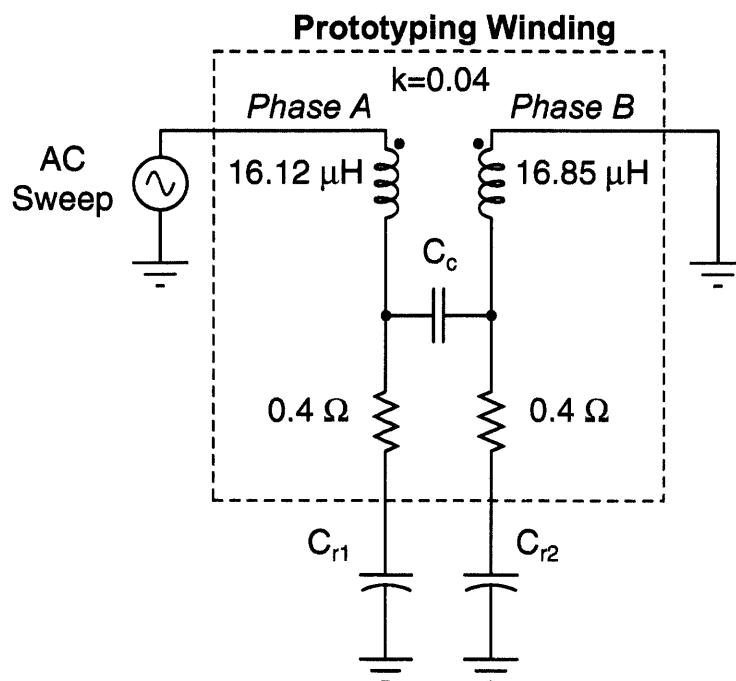


Figure 4-21: Simplified SPICE model to evaluate the effect of stray coupling between the two phases. An ac sweep is performed in the A phase with a shorted B phase.

between the two phase windings, is modeled by a single lumped capacitor C_c in this model. The windings are individually connected to two resonant capacitors C_{r1} and C_{r2} to form the series resonant circuits. An ac sweep is performed on the A-phase with the B-phase shorted, which is the Thevenin equivalent of a voltage source inverter. First equal resonant capacitors for the both phases is examined. For example, with $C_{r1} = C_{r2} = 10\text{nF}$; Figure 9 (top plot) shows the current response in the A and B phases. As expected, the A-phase resonates at 400 kHz, however, significant circulating current is induced in the B-phase at the same frequency due to the mutual coupling. This shows that the A and B-phases cannot be driven independently using two separate voltage sources making it challenging to achieve temporal orthogonality in the phase excitation currents.

However, the cross coupling in the two phase currents can be significantly minimized provided the two phases are tuned to two different frequencies. For example, choosing C_{r1} to be 20 nF while keeping C_{r2} at 10 nF, as shown in Figure 4-21, decouples the resonances between the two phases. With the A-phase resonating at 280 kHz, the impact observed in the B-phase due to the A-phase is negligible, as shown in Figure 4-22 (bottom plot). A symmetrical analysis using ac sweep on B phase with shorted A phase leads to an identical conclusion that the multi-resonant exci-

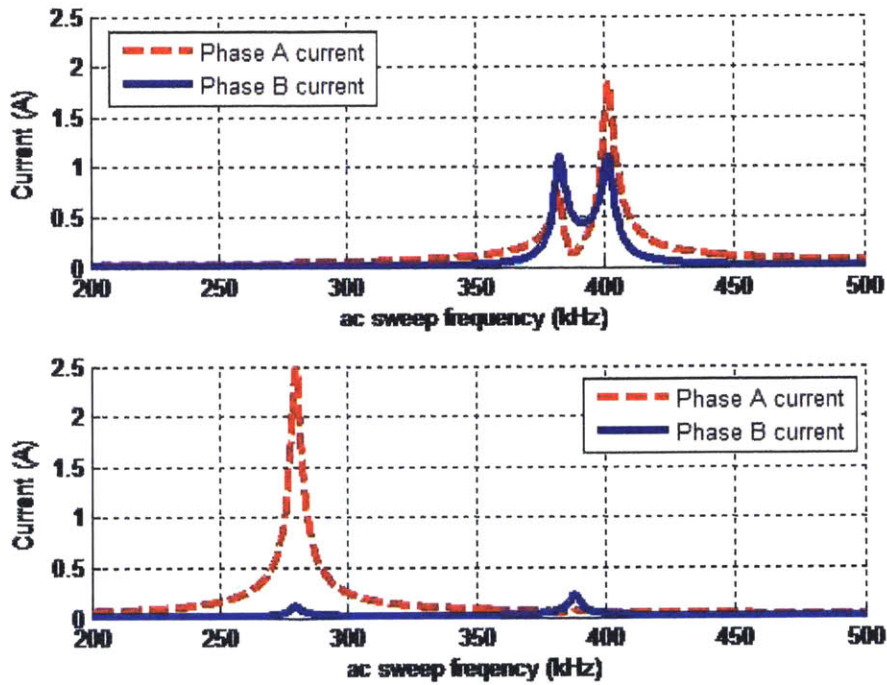


Figure 4-22: SPICE ac sweep result: Effect of stray coupling on B-phase with only A-phase excited. Top: Both phases tuned at 400 kHz. Significant current induced in the B-phase at same frequency. Bottom: A-Phase is tuned at 280 kHz while B-phase is tuned at 387 kHz. Cross-coupling effect is significantly reduced.

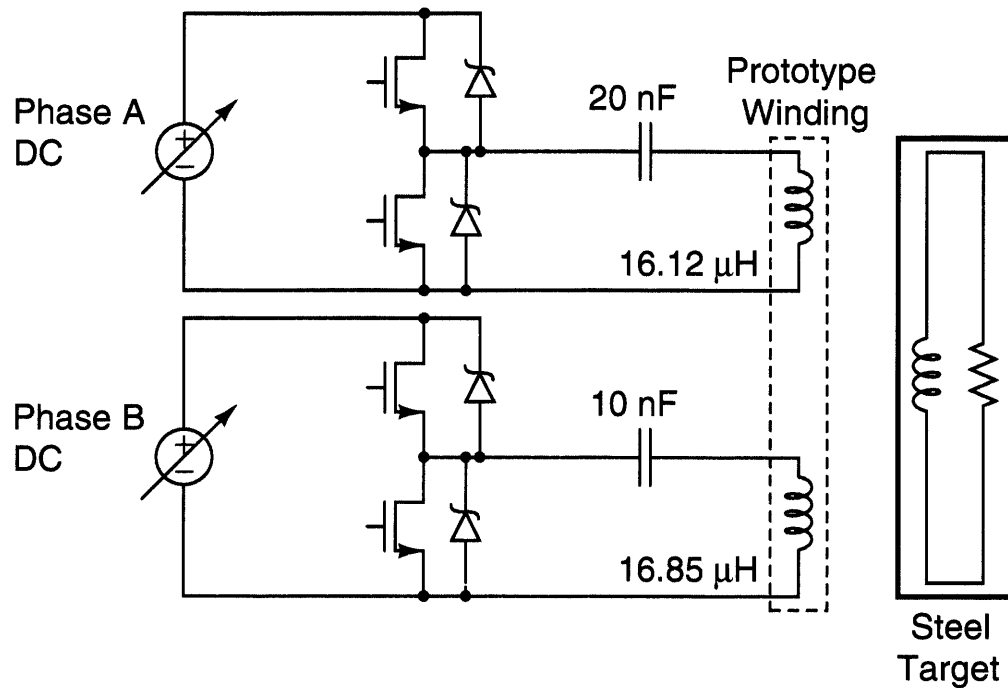


Figure 4-23: Two independent resonant power circuits is used to drive the prototype two phase Halbach windings. Phase A tuned resonant frequency is 280 kHz and Phase B tuned resonant frequency is 387 kHz.

tation of the two phases provides independent control of the phase currents. The multi-resonant power circuit used to excite the two phases for the prototype winding is shown in Figure 4-23.

Average Power Transfer to the Target with a Two-Phase Winding Excited at Different Frequencies

The multi-resonant excitation reduces the effect of stray coupling between and hence enabling independent control of the two phase windings. However, the excitation directly impacts the instantaneous magnetic field produced by the individual windings. So it is worthwhile to investigate this effect on the heating patter at the target. For example, the magnetic flux density of the fundamental spatial frequency of the A-phase at a point y above and x along a Halbach surface with height h can be shown as in [11],

$$B_A = \mu_0 \alpha k N (1 - e^{-kh}) e^{-ky} I_A \cos kx, \quad (4.12)$$

where $k = 2\pi/\lambda$ is the radian reciprocal of the array wavelength or pole pitch, N is the equivalent number of turns, I_A is the current excitation in the A-phase, and \hat{z} is

a geometric factor. Due to the orthogonal placement of the B-phase winding relative to the A-phase, the magnetic flux density of the B phase can be expressed as,

$$B_A = \mu_0 \alpha k N (1 - e^{-kh}) e^{-ky} I_B \sin kx, \quad (4.13)$$

Assuming the windings are identical and with individually controllable phase currents, the total magnetic flux density can be written by superposition as

$$B_T = \mu_0 \alpha k N (1 - e^{-kh}) e^{-ky} [-I_B \sin kx + I_A \cos kx] \quad (4.14)$$

The changing magnetic field due to the time-varying current excitations as computed above will result in eddy currents in the target and thereby dissipate power and heat the target. The power dissipated on the target is proportional to the square of the flux density. Thus, the instantaneous power delivered to the coil can be equivalently written as,

$$P_{Target} = K_B I_B^2 \sin^2 kx + K_A I_A^2 \cos^2 kx - K_B K_A I_B I_A \sin kx \cos kx. \quad (4.15)$$

The terms K_A and K_B take into account the difference in skin depths for the target at different excitation frequencies. Assuming that the current excitation in the A-phase has frequency ω_1 and the current excitation in the B-phase has frequency ω_2 , the average power transferred to the target can be calculated as,

$$\begin{aligned} \langle P_{Target} \rangle = \frac{K_B}{2} |I_B|^2 (1 - \cos 2kx) + \frac{K_A}{2} |I_A|^2 (1 + \cos 2kx) \\ - \frac{K_A K_B}{4} \langle I_B I_A \rangle \sin 2kx. \end{aligned} \quad (4.16)$$

Assuming that equal power is transferred from the two phases to the target and because of the orthogonality of sinusoids with different frequencies, the average power can be simplified to,

$$\langle P_{Target} \rangle = \frac{K_A}{2} |I_A|^2 + \frac{K_B}{2} |I_B|^2. \quad (4.17)$$

The average power transferred to the target is uniform along the x -direction enabling uniform heating on the target.

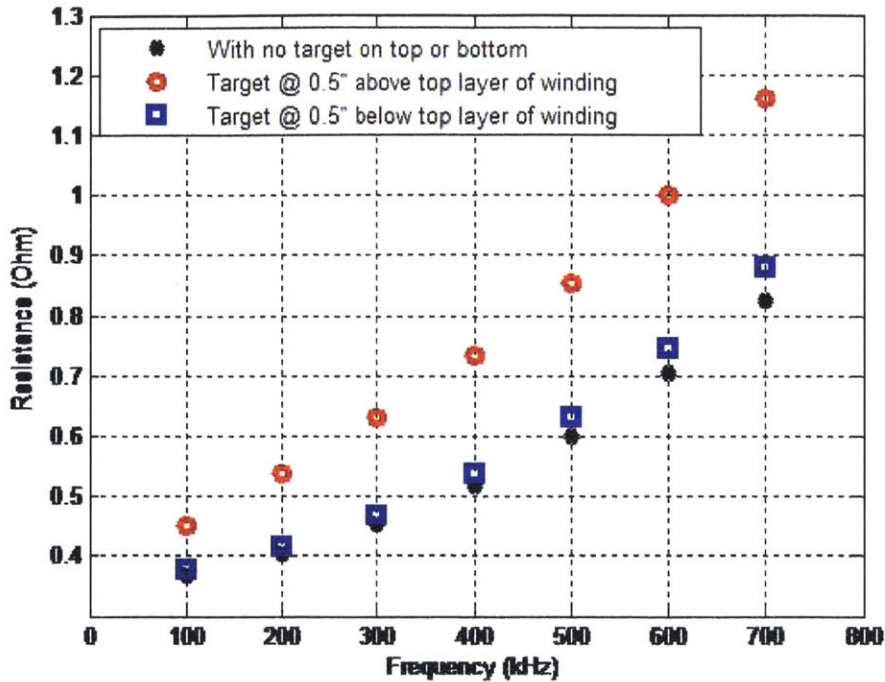


Figure 4-24: Measurement data from impedance analyzer: Change in resistance when a target is placed above the top layer winding is significantly higher compared to the change when the target is placed at same distance below.

4.2.3 Experimental Results

The prototype winding is tested with two different experiments to verify the directionality of the magnetic field produced by the windings and the uniformity of heating that can be achieved using the two phases when excited with the two resonant power circuits. The target used is made of steel of thickness 5 mil and of dimension 12 inches by 7 inches.

Change in Effective Winding Resistance from Target Proximity

The prototype winding as shown in Figure 4-20 is tested for performance in terms of directionality using an impedance analyzer. The resistance of the A-phase winding is measured as a function of excitation frequency and plotted in Figure 4-24. The change in the terminal resistance of the two-layer A-phase winding is much higher when the target is above than an equidistant 0.5 inches below. The difference in the loading effect shows strongly asymmetric magnetic coupling to the target between the top and the bottom, which is expected from a Halbach winding.

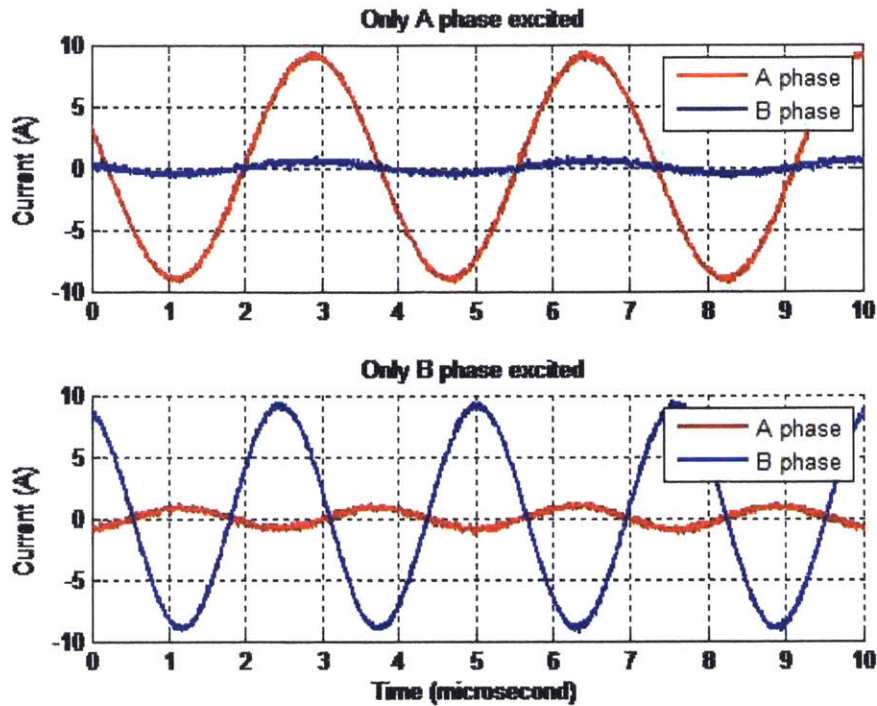


Figure 4-25: Measured current of the A phase and the B phase when excited individually. Tuning the phases at different resonant circuit minimizes the cross coupling of the phases enabling independent excitation possible for the two phases.

Thermal Performance of the Proposed Induction Heater

The prototype windings are excited using two resonant inverters with the steel target at $3/8''$ from the top layer of the winding. Figure 4-25 shows that there is minimal cross coupling of the phase currents because two different resonant frequencies are used for each of the two phases. The surface of the target is coated with a black thermal coating (emissivity = 0.97) for proper thermal imaging and a Fluke TI 20 camera is used to capture the thermal images of the target. The thermal images obtained are shown in Figure 4-26 and Figure 4-27 and the temperature profiles are compared in Figure 4-28 along the center horizontal guide lines (x -dimension) shown in the thermal images. Figures 4-26a and 4-26b show the non-uniform heating on the target when only the A or B phase is individually excited. The pattern has a periodicity of $2kx$ and is shifted by 180° in space as expected due to the flux density pattern of the individual phases. Figure 4-26c shows the uniform heating along the surface of the target when both the phases are excited together. Fringing of the magnetic field at the edges of the windings causes non-uniform heating there.

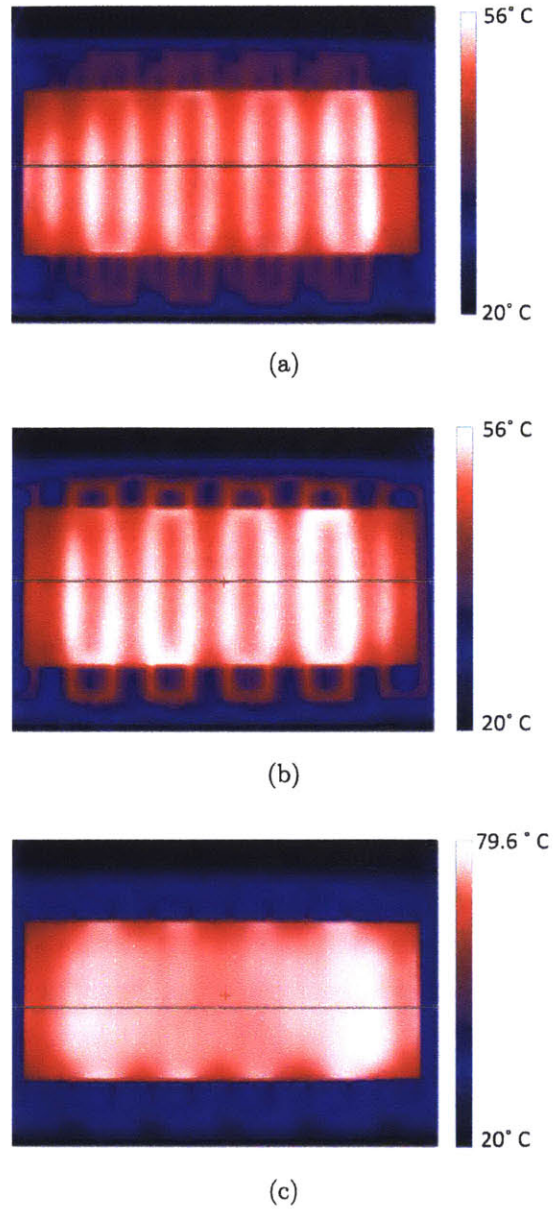


Figure 4-26: Thermal images of the steel target placed 3/8 inch above the top layer of the prototype. (a) Only A-phase is excited—Input Power = 38 W. (b) Only B-phase is excited—input power = 37.3 W. (c) Both phases are excited—Input Power: Phase A = 38.2 W & Phase B = 37.8 W.

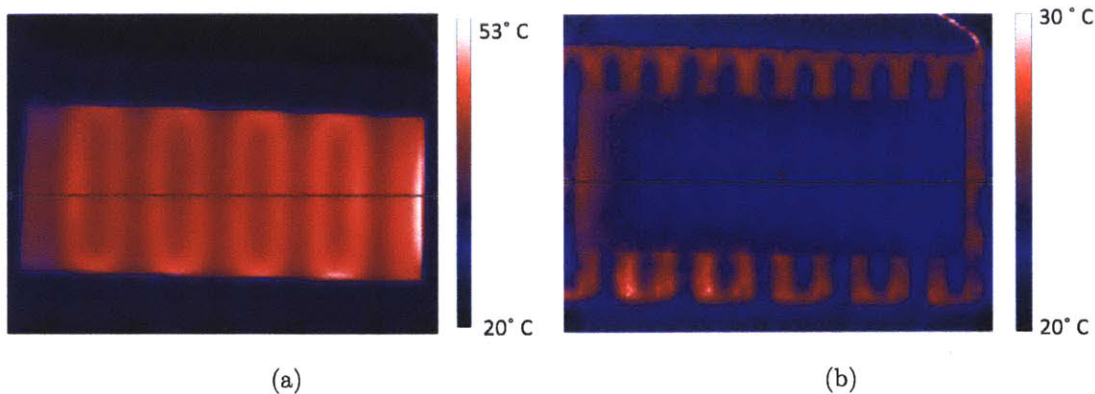


Figure 4-27: Thermal image of an additional steel target when placed at 0.4 inches below the top layer of the prototype with Phase A excitation. (a) With bottom layer of the winding disconnected. Resonant frequency adjusted to 349 kHz. Input Power = 44.2 W. (b) With top and bottom winding layer connected. Input Power = 44.7 W.

With uniform heating obtained on top, another identical target is then placed on the back of the winding at a distance 0.4 inch from the top winding layer to evaluate the directionality of the heating. The A-phase is first excited with a disconnected bottom layer. As the inductance of the winding changes due to the removal of bottom layer connection, the resonant frequency is adjusted so that the A-phase still resonates with 20 nF. An average temperature rise of 45 °C, shown in Figure 4-28, is observed on the bottom target while the thermal profile is similar to the top because of single phase excitation as shown in Figure 4-27a. Re-connecting the bottom layer results in no heating of the bottom target as shown in thermal image of Figure 4-27b as well as on the temperature profile in Figure 4-28. The thermal image only shows heating up of the winding relative to the bottom target. This validates that the optimized winding behaves as a Halbach array providing both single side and uniform heating.

4.3 Chapter Summary

This chapter demonstrated an approach for induction heating by using uniform, single-sided magnetic fields, which is enabled by using multiple phases operating at multiple frequencies. The concept overcomes several shortcomings in traditional designs, including stray magnetic fields below the winding and non-uniform heating without requiring ferrites or other types of magnetic shielding. A design methodology for more efficient and lower cost windings for single-sided fields was also developed

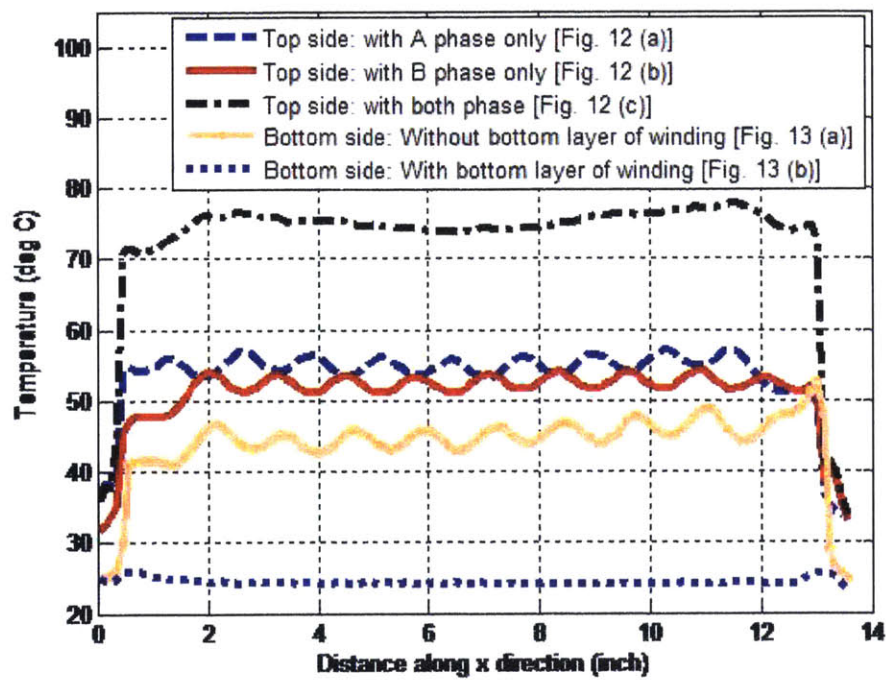


Figure 4-28: Temperature profiles along the center lines drawn on the thermal images of Figures 4-26 and 4-27. While uniform heating is obtained on the top, no heating is produced on the bottom of the fully functional winding structure.

along with basic theoretical analysis and validation through simulation and experiments. The concept generalizes to other geometries and applications, extending the application space from consumer cooktops to chargers and non-contact power sources for transportation, industrial, and medical applications.

The extension of uniform single-sided fields from its initial exploration in induction heating towards wireless power transfer is a topic for future work. The concept of orthogonal drives for windings had been broadened to include multiple frequencies. With spread-spectrum power, the possible of driving the windings with orthogonal codes is a future endeavor.

Chapter 4 : Single-Sided, Time-Varying, Spatially-Uniform Magnetic Fields

Chapter 5

Ultralow Power Neural Sensing for Closed-Loop Stimulation

NEUROMODULATION or the actuation of the nervous system with electrical stimulation, is a rapidly developing field melding electrical engineering with neuroscience. This chapter describes an amplification and spectral processing IC for extracting key bioelectrical signals, or *biomarkers*, which are expressed in the brain's field potentials. The intent is to explore using these biomarkers to drive prosthetic actuators or titrate therapy devices such as a deep-brain neurostimulator. The prototype IC uses $5 \mu\text{W}/\text{channel}$ to resolve signals on the order of $1 \mu\text{V}_{\text{rms}}$. The four channels on the device provide independent spectral analysis from dc to 1 kHz, with variable bandwidth and power filtering characteristics. The noise floor and flexible spectral processing support a broad range of potential applications including sleep staging, Parkinson's disease, detection of movement intention for neuroprosthesis, and detection of high frequency *fast ripples* for exploring seizure prediction. To fully demonstrate the IC's functionality, we include results from a prototype *closed-loop* neurostimulator implementing adaptive titration of therapy based on measured field potential activity.

5.1 Introduction

Neuromodulation for deep-brain stimulation (DBS) is currently approved for the treatment of movement disorders such as Parkinson's disease, essential tremor and dystonia, and a number of studies are underway exploring new therapy opportunities. The major components of DBS are shown in Figure 5-1. An implantable pulse generator (IPG) is placed into the pectoral region of the chest. The IPG contains the

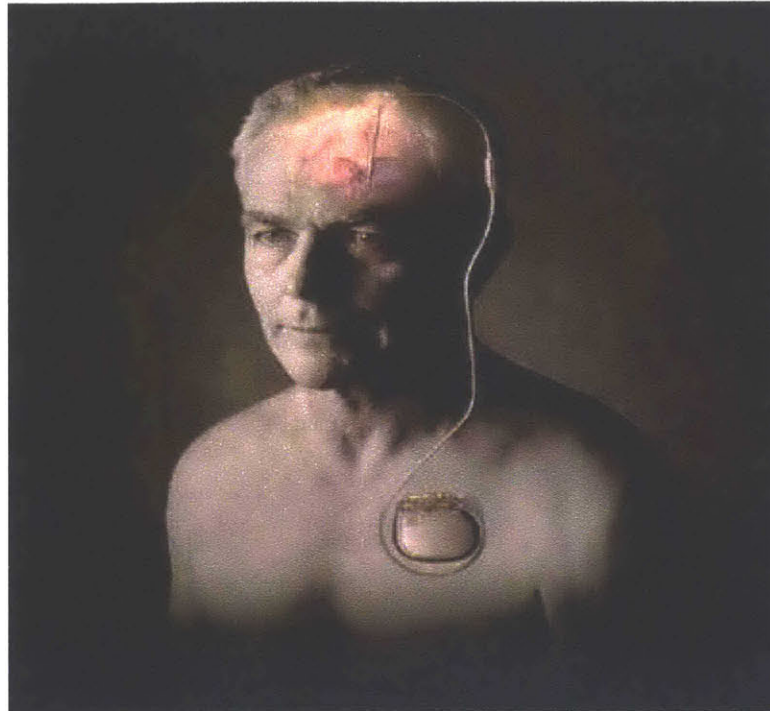


Figure 5-1: Key elements of a deep brain stimulator. The battery and circuitry form the IPG, which is implanted in the chest. The electrodes are placed into a specific neural circuit into the brain. Connections are made between the IPG and electrodes via a lead system placed in the neck.

energy for stimulation within its battery, as well as the circuitry to provide stimulation pulses. The IPG interfaces to neural tissue through a series of electrodes placed in a specific physiological target in the brain (e.g., subthalamic nucleus for Parkinson's disease). Stimulation pulses from the IPG are localized to the vicinity of the electrodes, providing targeted modulation of the firing pattern in a specific neural circuit.

Current DBS systems work without the benefit of in-vivo sensing. The *feedback loop* for titrating therapy requires observation of clinical symptoms by a physician, who then adjusts stimulation settings from an external instrument using wireless telemetry. This is essentially a one-way brain-machine interface (BMI), providing therapeutic modulation to the brain via the electrode.

Future progress in DBS and neuroprosthesis could hinge on making the BMI bidirectional, by adding the ability to detect and decode information directly from the nervous system, and several research groups have already explored acute sensing of neurological conditions using external hardware [60, 68, 82, 83]. One area of focus is

sensing the response of neural activity to stimulation to help understand the fundamental mechanisms for existing therapies, and hence better identify optimal stimulation electrode parameters. In addition, real-time measurement is being considered for adaptive titration of therapy or other actuator based on quantitative biomarkers. The objective of this system is to extend device longevity while optimizing therapeutic benefit. To be implemented within an implantable device, however, the sensing and control strategy must be proven practical in terms of technical constraints like power and area, as well as be chronically safe and reliable.

In this chapter, we discuss the prototype of a bidirectional brain-machine interface capable of adaptive titration of neuromodulation, particularly focusing on a neural spectral-processing IC (NPIC) that amplifies and processes neuronal activity. First, we motivate the requirements for the NPIC by considering the signals that represent pertinent neurological activity, as well as the partition of the control system that we are exploring for adaptive neuromodulation. Next, we discuss the design of the NPIC that merges the principles of chopper-stabilization and heterodyne conversion to achieve power efficient extraction of neuronal biomarkers. Finally, we present the NPIC prototype results and demonstrate the functionality of this design within a total system including electrodes and a modeled biological environment. Although the IC was developed with neural sensing in mind, the circuit techniques are quite general and can be adapted for a number of low-power applications involving spectral analysis.

5.1.1 Brain Sensing Strategy in Generalized "Prosthesis" Applications

The foundation of this architecture is based on the choice of neural signal used as a biomarker. Neuronal activity can be measured through a number of electrical techniques, ranging in resolution from recordings of single-cell action potentials to electroencephalography (EEG) for gross cortical behavior. Each technique has its tradeoffs and the choice of approach is motivated by a number of practical system constraints: desired neurophysiological information, spatial resolution of electrodes, and available power for sensing, control, and telemetry. Table I summarizes a number of these engineering tradeoffs from references discussing motor prosthesis [7,8,93]; the same analysis holds for most DBS systems.

Local field potentials (LFPs) represent a good technical compromise for chronic applications such as closed-loop neuromodulation and implantable neuroprosthesis.

Table 5.1: Engineering Tradeoffs for Various Electrical Sensing Methods, summarized from [5-7].

| Sensing Method | Chronic Recording Capability | Information Quality | Power and Telemetry Requirements |
|-------------------------------|---|---|----------------------------------|
| Single Unit Action Potentials | Challenging issues for measurement stability | Highest fidelity with measurements over several units | ~10 mW >100 kbps |
| LFPs/(EcoG) | More robust chronic interface and stability | Medium fidelity, but processing context | ~10 μ W <1 kbps |
| Surface EEG | Minimally invasive, but most susceptible to artifacts | Lowest fidelity and limited processing information | External system, minimal concern |

LFPs sample the average potential in the vicinity of the electrode, superimposing signals from a number of cells; note that electrocortigraphy (ECoG) is a similar technique, measuring field averages on the surface of the cortex. Because LFPs render the ensemble activity of thousands to millions of cells, their recording often avoids the difficulties with chronic in-vivo measurement such as tissue encapsulation and micromotion [7, 8, 93]. In neuromodulation, the stimulation electrodes can also be used for LFP measurements because the relatively large geometry (order of a few mm) offers the spatial average of electrical activity [22]. Most importantly, there is growing evidence that both normal processing states and many neurological diseases are marked by synchronously coherent oscillations within a neural circuit [18]. This synchrony results in biomarkers encoded as field potential fluctuations with characteristic spectral patterns, if the sensing electrodes are placed within the appropriate neural circuit [30, 60, 68, 82, 83].

Coherence in neural circuits is reflected in LFP spectral fluctuations, providing information about circuit activity near the electrode. In particular, the key information we wish to extract from the signal is the power fluctuations within discrete frequency bands—essentially an analog to AM demodulation in communication circuits. These spectral fluctuations encode a broad range of activity in the brain, and are useful

Table 5.2: Sample of Field Potential Biomarkers of Interest for DBS. Note that the bands listed represent the rough limits of interest, and the actual bandwidth for an individual is generally more compact.

| Neurological State (Method) | Frequency Band (Brain Wave Categorization) | Comments/References |
|---|--|---|
| Visual Processing (EEG) | 8-12 Hz (α) | Event-Related Desynchronization [8] |
| Motor Planning (EEG) | 8-12 Hz (α) | Event-Related Desynchronization [14, 15] |
| Motor Planning (EcoG/LFP) | \sim 140-160 Hz (hi- γ) | Event-Related Synchronization [13, 16-18] |
| Epilepsy Seizure Detection (EEG/EcoG) | 8-40++ Hz (α - β) | Event Detection [19] |
| Epilepsy Seizure Prediction? (EcoG/LFP) | 50 \rightarrow 200 ++ Hz | Fast Ripples [10-12] |
| Depression (EEG) | 8-40 Hz (α - γ) | Hemispheric Power Imbalance [20] |
| Parkinsons (EcoG/LFP) | 15-30 Hz (β) | Pathological State [1, 3, 4] |
| Olfactory Processing | 40-80 Hz (γ) | Odor Discrimination [21, 22] |
| Sleep (EEG/EcoG) | 0.5-25 Hz (δ - β) | Sleep Stage Detection [23] |

for discerning both neurological and disease states. Table II delineates some of the useful biomarkers for DBS applications and prosthesis. As shown, LFP biomarkers span a broad frequency spectrum, from 1 Hz oscillations in deep sleep to 500 Hz “fast ripples” in the hippocampus, and show wide bandwidth variations. Note that bands are often listed as broad spectrums that would imply low effective Q ; this can occur because biomarkers are defined as the average across several patients, and the actual band for a given individual is often more compact.

The science of field potential spectral processing is still evolving, with a common theme being the discovery of higher frequency bands signaling processing states that have been previously filtered out in surface EEG [28, 48, 103, 116]. In addition to raw spectral power measurements, there is also increasing interest in the relative phase of signals between sites, which can provide additional information on disease states or information for prosthesis [59]. Monitoring spectral band activity, including relative phase, provides key information on the state of a neural circuit which can help actively

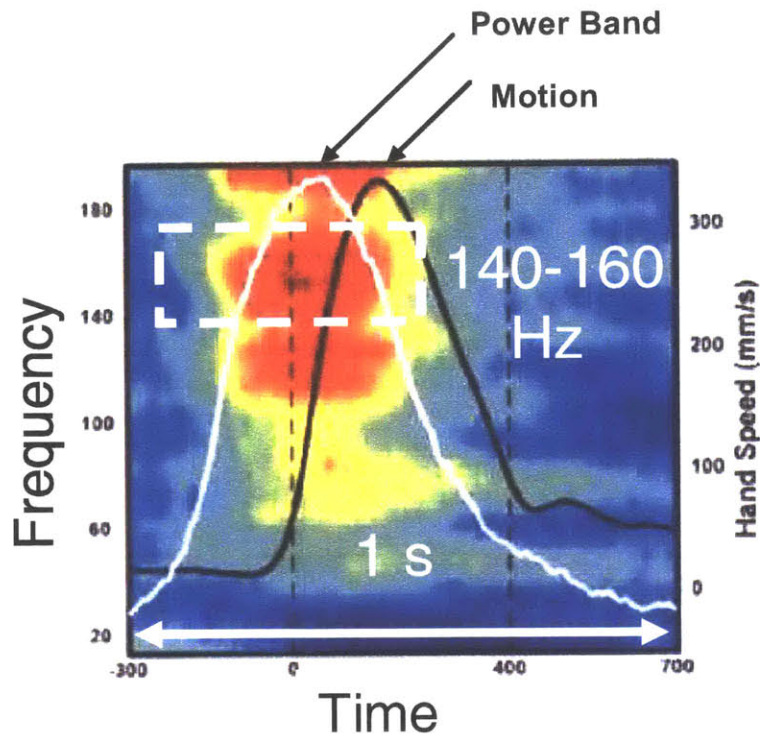


Figure 5-2: An example of LFP spectral band fluctuations in the motor cortex preceding motion; this is a useful biomarker for signaling a patient's 'desire to move.' Reprinted from [14].

control an actuator or other therapy device.

The application of field potentials for brain-machine interfacing and prosthetic control has already been reduced to practice. Figure 5-2 shows the fluctuations in the high-gamma band power within the pre-motor cortex, correlated with motor planning prior to actual muscle motion taken from a primate model [48]; this band has also been observed in humans [72]. The ability of primates to modulate consciously the higher gamma bands has motivated its use as the control input for a prosthetic actuator [63,91]. A controller monitors the low-frequency beta and gamma power fluctuations (order of 1 Hz) at two electrodes, and maps that power to a cursor coordinate using an integral controller. Although this system may appear crude compared to a "spike-based" prosthesis system measuring the discrete activity of a population of cells, the LFP-based system actually provides unique neural state information that can be advantageous for control [7,8].

The information capacity of neuronal signals has been estimated by a number of authors, with a number of varying assumptions. In [33], the mean information rate is estimated to be 3.6 bits/s for spike recordings and 4.3 bits/s for LFPs along a one

dimensional channel, assuming additive white Gaussian noise and using an optimal Kalman filter. This is counter-intuitive because we expect that the higher bandwidth spike recordings would have a higher rate of information. This suggests that the noise distribution is probably not Gaussian for spikes and that the Kalman filter may not be optimal. At the same time, we expect LFPs to be closer to Gaussian because of the convergence dictated by the central limit theorem for a larger ensemble of neurons. Nonetheless, the data implies the usability of LFPs for BMIs and that the information rate from LFPs may not be all that much smaller than that from spike recordings. In summary, the performance of existing field potential-based prostheses, the technical benefits outlined in Table I, and the observation that many disease states are disruptions of large neural pathways and not single-cell events per Table II, motivates our focus on LFP spectral fluctuations as our primary sensing modality.

5.1.2 Adaptive Titration Considerations for Neuromodulation

The hurdles to implementing adaptive titration of neurostimulators do not stop at sensing, however-the implementation of the control algorithms for the closed-loop titration of therapy must also be included in the system design for the NPIC. Figure 5-3 offers a dynamical systems view of a controller and plant model for the neural circuit. Conceptually, the inputs $\mathbf{u}(t)$ to the neural circuit include sensory inputs, pharmaceuticals, and electrical stimulation. $\mathbf{f}(\mathbf{u}(t))$ contains the dynamics of the neural circuit as well as the effects of inputs such as electrical stimulation on the neural state. $\mathbf{g}(\mathbf{x}, \mathbf{u}, t)$ encapsulates the measurement of biomarkers $\mathbf{y}(t)$ as well as the effects of any input to the measurement. In general, the controller $\mathbf{K}(\mathbf{y}, t)$ can be time-varying, nonlinear, and adaptive.

The objective is to estimate the neural states \mathbf{x} from the biomarkers \mathbf{y} despite the corruptions contained in \mathbf{g} . These corruptions include feedforward interference from electrical stimulation, as well as artifacts from other parts of the nervous system, and physical motion. In the measurement of LFPs, \mathbf{g} might include the aggregation and low-pass filtering of signals from individual neuron firings. A dynamical systems point of view is valuable in that it motivates the fundamental design strategy as well as potential caveats.

Another design driver that one must consider is the practical constraints on implementing an adaptive modulation scheme. The first consideration is our desire to make the system ambulatory, and hence cannot require an external power supply [17].

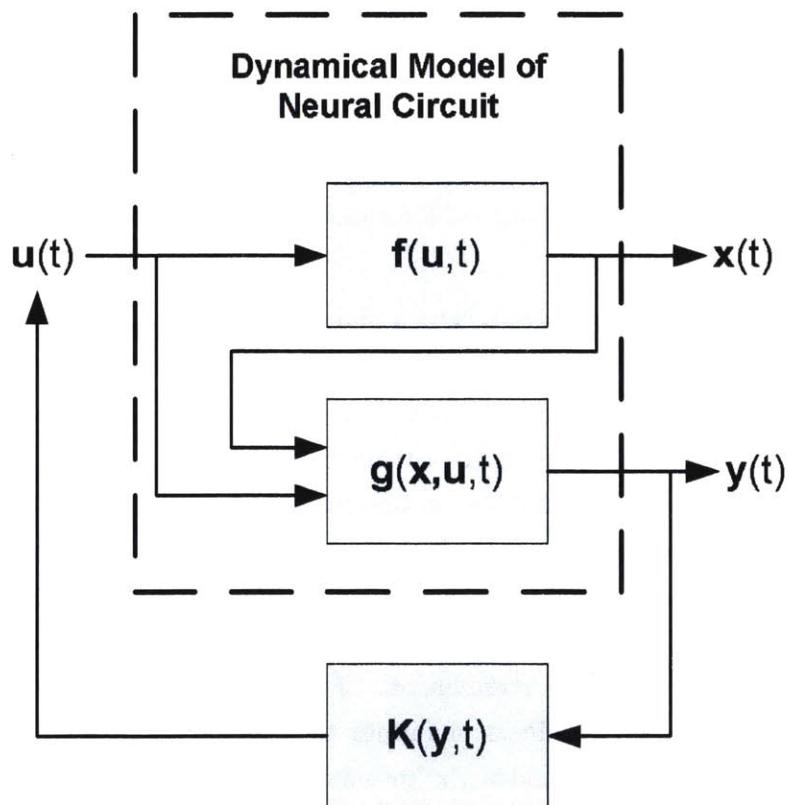


Figure 5-3: Closed-loop dynamical system where $u(t)$ is a vector of inputs to the neural circuit such as electrical stimulation, $x(t)$ are the neural circuit states, and $y(t)$ are the outputs such as biomarkers. f is the function that maps the inputs to the neural states and g maps the states to the biomarker outputs. K is the controller that senses and processes the outputs and actuates updates to electrical stimulation and drug delivery, among others.

Our benchmark is that a typical DBS therapy requires roughly 250 μW , on average, to be delivered to the tissue to provide therapeutic benefit. To justify the addition of sensing and control to therapies that already provide therapeutic benefit, one needs to keep power consumption of the feedback controller on the order of 10 $\mu\text{W}/\text{channel}$ to avoid undermining device longevity; we have assumed at least two channels will be active at any time, one per hemisphere. Next, we need the control system to be flexible. The knowledge of neural circuit dynamics, therapeutically relevant biomarkers, and closed-loop neuromodulation algorithms is still evolving, hence motivating a highly flexible and programmable architecture that allows the fine-tuning of the neuromodulation controller with minimal hardware effort. Finally, and most importantly, the implementation of the sensing and adaptive control algorithm must be safe and reliable. By safe, we mean that the NPIC does not corrupt existing therapeutic stimulation, is single-fault tolerant to ESD and electrosurgery events, and maintains dc electrode leakage under 100 nA. Similarly, by reliable, we mean that the circuit's performance is set by well-controlled parameters, such as ratios of stable components, which can preferably be calibrated in the field to guarantee the consistent performance of these algorithms, and that the circuit is immune from common EMI sources. These considerations help drive our system definition and detailed specifications for the NPIC.

5.2 System and Circuit Theory of Operation

To explore the practicality of adaptive neuromodulation technologies, we designed a prototype closed-loop neurostimulator based on a bidirectional brain-machine interface. This prototype uses the custom sensing and an auxiliary microprocessor as the titration controller for an existing approved device. Figure 5-4 shows the system block diagram with the sensing and control extension interconnected with the existing neurostimulator's circuits and electrodes. The sensing and control extension requires three key blocks: the NPIC that connects to the electrodes and conditions field potentials; a microprocessor or microcontroller for performing algorithms on the signal based on feature extraction; and a memory unit for recording events and general data-logging. Command and control between the sensing extension and the existing stimulator is made through an interrupt vector and interface. The digital communication port allows the sensing extension to send commands for titration to the neurostimulator based on the algorithm. Connections between the sensing extension and the electrodes are made through a protection network that isolates the

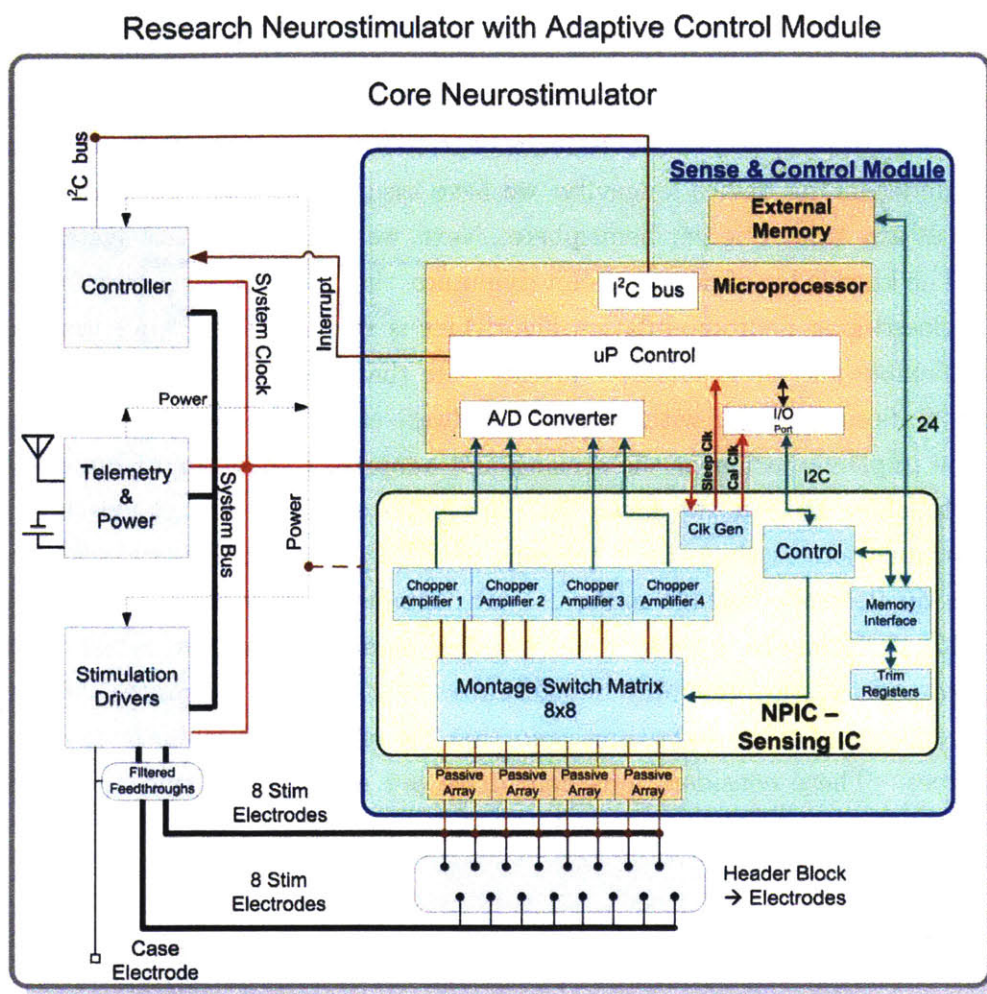


Figure 5-4: Architecture for a neurostimulator feasibility research tool based on a bidirectional BMI, with a sensing and control extension for exploring diagnostics and closed-loop algorithms.

sensing IC from stimulation and blocks dc currents to the tissue.

The nature of LFP information coding motivated a circuit architecture that directly extracts neuronal signal energy at key frequency bands and tracks the relatively slow power fluctuations—much as an AM radio produces audio signals from a high-frequency carrier. By partitioning the system so that relevant power fluctuations are extracted at the analog interface, the back-end requirements for sampling, digital processing, memory, and telemetry are mitigated in ways similar to those explored for cardiac pacemakers [40, 41], motor [47], and cochlear prosthesis [89, 90]. These strategies take advantage of the separate strengths of analog and digital processing to minimize power, while maintaining acceptable flexibility and robustness.

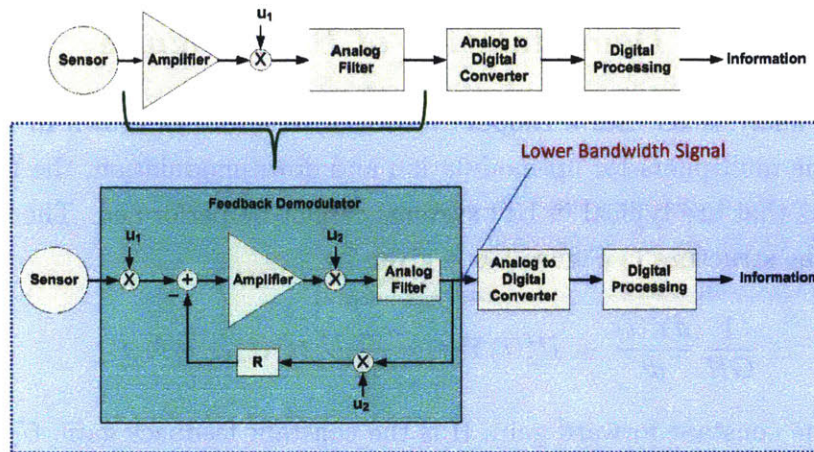


Figure 5-5: *Feedback Demodulator* embeds demodulation into amplification.

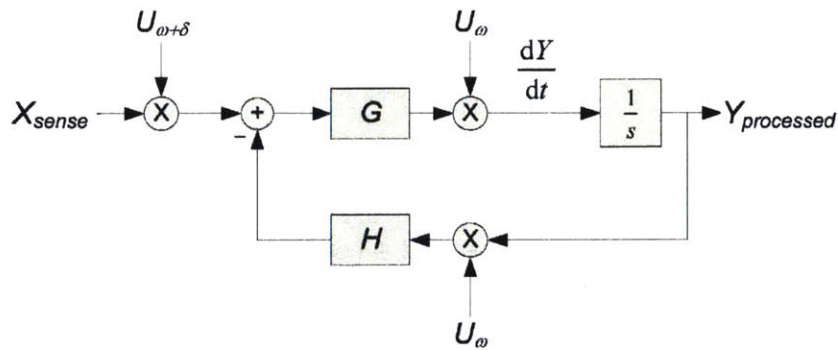


Figure 5-6: Feedback heterodyning block diagram

We partitioned the signal chain to extract the low-frequency signal power in a physiological band using analog preprocessing for the input BMI. The analog spectral processing decreases the bandwidth and dynamic range of data conversion and digital processing. After digitization, the kernel for controlling the output BMI can be implemented in software using an off-the-shelf digital processor, or microcontroller. The processor provides the mechanism for flexible algorithmic control through telemetry reprogramming, but with the ability to run at a reduced bandwidth to keep the total power down to the microwatt level. With this system partitioning, the design problem largely focuses on the custom analog NPIC.

5.2.1 Feedback Demodulation of Brain Signals

The spectral analysis IC uses a chopper feedback structure as shown in Figure 5-5. Because of the multipliers for up-modulation and down-modulation, the usual block manipulations that are typical in LTI systems cannot be performed. The differential equation of the structure in Figure 5-6 is given by

$$\frac{1}{GH} \frac{dY(t)}{dt} + U_{\omega}^2(t) Y(t) = \frac{1}{H} U_{\omega}(t) U_{\omega+\delta}(t) X(t), \quad (5.1)$$

where G is the constant forward gain, H is the constant feedback gain, U_{ω} and $U_{\omega+\delta}$ are the chopping harmonics at ω and $\omega + \delta$, respectively. In the following, we analyze this differential equation by harmonic decomposition.

Let's look at the limiting case where the loop gain GH goes to infinity. $1/H$ is the closed-loop constant gain from the input to the output, which we choose to be unity for simplicity. Equation 5.1 simplifies to

$$U_{\omega}(t) Y(t) = U_{\omega+\delta}(t) X(t). \quad (5.2)$$

If $U_{\omega} = \sin \omega t$, $U_{\omega+\delta} = \sin(\omega + \delta)t$, and $X(t) = \cos \omega_s t$, then

$$Y(t) = \cos(\delta + \omega_s)t + \cos(\delta - \omega_s)t, \quad (5.3)$$

a result which is equivalent to direct sinewave demodulation [102].

Square Wave Chopping

If U_{ω} is a unit square wave with zero mean, then $U_{\omega}^2 = 1$, which is a constant. Equation 5.1 then reduces to

$$\frac{1}{GH} \frac{dY(t)}{dt} + Y(t) = \frac{1}{H} U_{\omega}(t) U_{\omega+\delta}(t) X(t), \quad (5.4)$$

which is a driven first-order system if we make the change of variables $\bar{X}(t) = U_{\omega} U_{\omega+\delta}(t) X(t)$. In the Laplace domain, 5.4 becomes

$$Y(s) = \frac{1}{H} \frac{1}{\tau s + 1} \bar{X}(s), \quad (5.5)$$

where $\tau = 1/GH$ and $\bar{X}(s)$ is the Laplace transform of $U_{\omega}(t) U_{\omega+\delta}(t) X(t)$.

The chopping harmonics are derived from square waves,

$$U_{\omega}(t) = \frac{4}{\pi} \sum_{m \text{ odd}} \frac{1}{m} \sin m\omega t, \quad (5.6)$$

$$U_{\omega+\delta}(t) = \frac{4}{\pi} \sum_{n \text{ odd}} \frac{1}{n} \sin n(\omega + \delta)t. \quad (5.7)$$

When expanded

$$U_{\omega}U_{\omega+\delta} = \left(\frac{4}{\pi}\right)^2 \left(\frac{1}{2}\right) \left\{ \sum_{k \text{ odd}} \frac{1}{k^2} [\cos k\delta t - \cos k(2\omega + \delta)t] \right. \\ \left. + \sum_{m \text{ odd}} \sum_{n \text{ odd}} \delta_{m \neq n} \frac{1}{mn} [\cos[(m-n)\omega + m\delta]t - \cos[(m+n)\omega + m\delta]t] \right\}, \quad (5.8)$$

where $\delta_{m \neq n}$ is the indicator function. We notice that the odd δ harmonics fall off as the inverse square of the harmonic number. All the other terms are the odd δ harmonics that are the frequency translated by the even harmonics of ω ; these fall off with an upper bound that is inversely proportional to the harmonic number. If $\omega \gg \delta$ and ω (approximately $4 \text{ kHz} \times 2\pi$) is much greater than the band of interest ($100 \text{ Hz} \times 2\pi$ for brain sensing), then *feedback demodulation* reduces the effects of the non-fundamental δ harmonics in comparison to *direct demodulation* as we will see in the following section.

The stimulation harmonics are derived from square pulses,

$$X_{stim} = \frac{\sqrt{2}}{\pi} \sum_k \frac{1}{k} (1 - \cos k\omega_s d)^{1/2} \cos k\omega_s t, \quad (5.9)$$

where ω_s is the stimulation angular frequency and d is the pulse width. The stimulation harmonics fall off inversely proportionally to the harmonic number k and for pulses that are not 50% duty cycle, include both even and odd harmonics; at 50% duty cycle, the nulls occur exactly at the even harmonics, which result in only odd harmonics. The envelope of these harmonics is shown in Figure 5-7.

For $\omega_s \ll \omega$, demodulation of stimulation harmonics to baseband is reduced using feedback demodulation. There is however a $2/\pi$ gain disadvantage with the feedback demodulator.

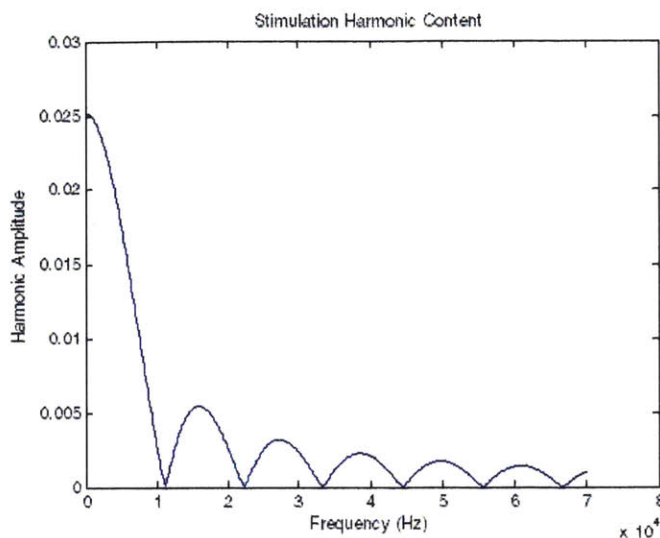


Figure 5-7: Spectrum envelope of stimulation harmonics for unit pulses with $f_{stim} = 140$ Hz pulse width of $90 \mu s$.

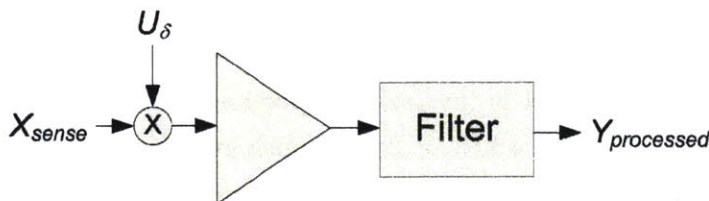


Figure 5-8: Classic heterodyning

Direct Demodulation Using a Chopper

If in Figure 5-6, we replace the input multiplication of $U_{\omega+\delta}$ with $U_{\omega} U_{\delta}$, the system reduces to a δ chopper followed by a chopper-stabilized amplifier, as illustrated in Figure 5-8, with

$$U_{\delta} = \frac{4}{\pi} \sum_{n \text{ odd}} \frac{1}{n} \sin n\delta t. \quad (5.10)$$

Calculating the harmonic content from stimulation is easier in this case because only the harmonics are involved. However, these harmonics demodulate signals in the brain sensing band and hence reduce selectivity. For example, when using a $\delta = 20 / \text{Hz}$ to detect beta band activity, spurious ambient $60 / \text{Hz}$ interference may be admitted because it coincides with the 3rd δ harmonic. Feedback demodulation offers another 9.5 dB of attenuation. Figure 5-9 shows a sweep of the stimulation frequency and the resulting stimulation interference from a direct demodulation.

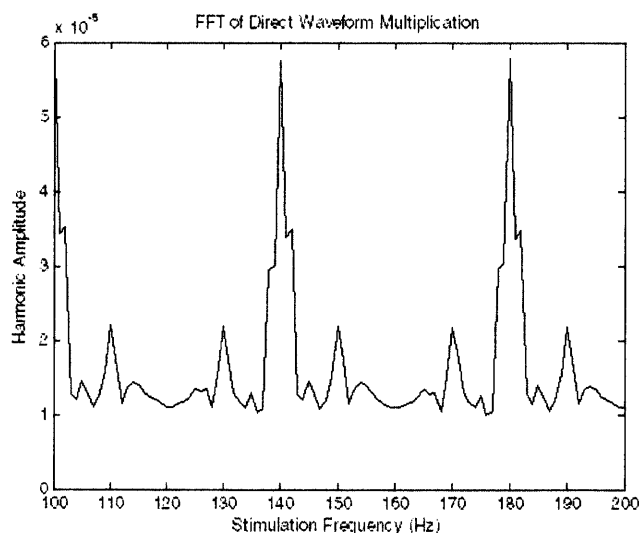


Figure 5-9: Harmonic interference. FFT of the product of the time domain waveforms from a chopper operating at $\delta = 20$ Hz and $90 \mu\text{s}$ stimulation pulse width.

Validating the Feedback Demodulation Model

The sense-stimulation harmonic contributions to the spectral power output can be determined computationally in several ways: 1) analytical calculation of the resulting truncated Fourier series of the modulation products; 2) FFT of the time domain waveforms; and 3) Simulink behavioral model of the spectral IC.

The computational cost of the analytical calculation roughly scales as $N^3 \cdot N_{stim}$, which is the cost of collecting the amplitudes for the three even harmonic terms and the cost of multiplying those terms with the stimulation harmonics. It is important in this calculation to truncate the stimulation harmonic series well before the series for the demodulation; otherwise, the amplitudes that multiply the stimulation harmonics will be incorrect.

The FFT computation cost scales as $N \log N$ of the number of time domain data points. The stimulation pulse width is the important factor in the selection of the time resolution. For the time duration, the base bandwidth is the determining factor. With a $90 \mu\text{s}$ pulse width, a $1 \mu\text{s}$ time resolution is used, and for baseband of 2.5 Hz, a 100 second time duration is chosen. This corresponds to an FFT of a 100 million point time series at each stimulation frequency point. A brick wall filter at 2.5 Hz is used, which is easily implemented in the frequency domain. Having a longer time series duration means that the frequency resolution over the 2.5 Hz is higher; it then follows that there will be a larger number of points over which to integrate the

spectral power.

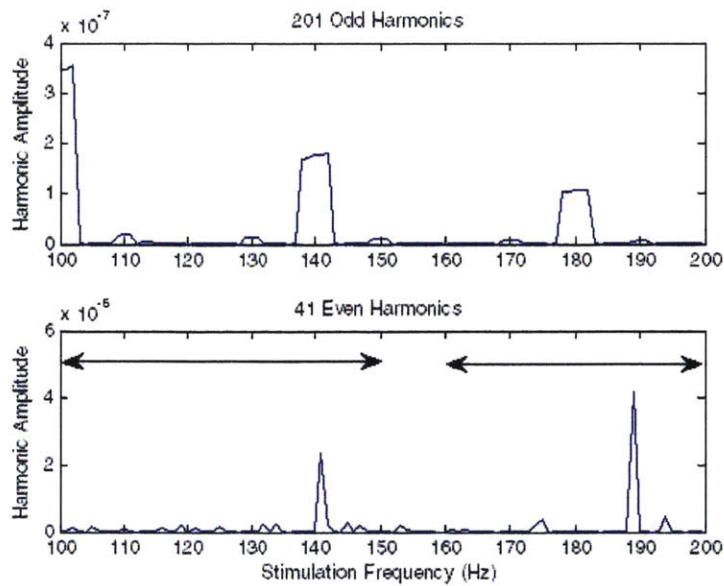
The Simulink behavioral model is the slowest and least accurate quantitatively. The time scales are widely different between the chopping and the desired low frequency behavior so small time steps are required relative to the total simulated time. In addition, settling of the time domain filters increases the time series over which to simulate.

Validation focused on two δ frequencies, 20 Hz and 80 Hz, because these are currently the bands used for the detection of epilepsy.

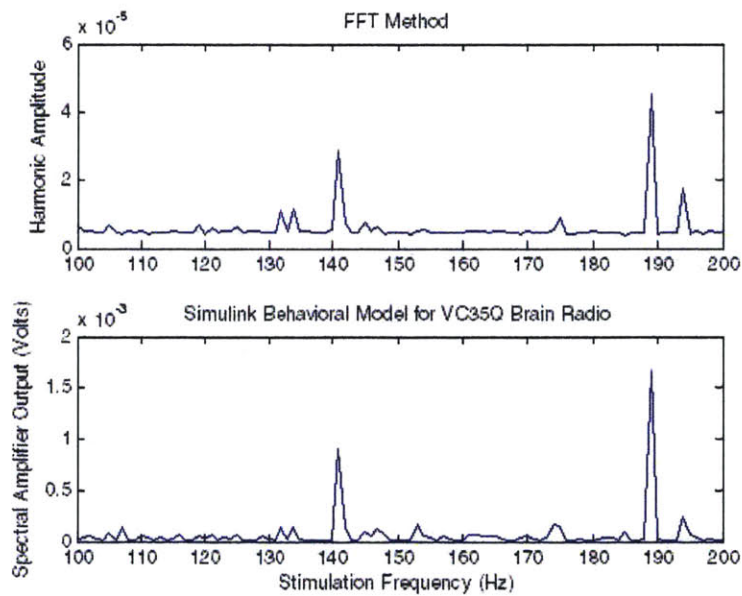
Discussion of Validation Results

Limitations of Simulink Results The model was run over a simulated time period of 2 seconds using the ode23t integration algorithm (for stiff systems), iterated over stimulation frequency at 1 Hz intervals. The results shown in Figures 5-10 and 5-11 are the last sampled data point of the 2 second interval. Originally, this test was conducted to obtain order of magnitude estimates of the amplitudes and frequency locations for stimulation interference peaks. Fluctuations in the spectral power output along with a possible incomplete settling time contribute to amplitude errors up to a factor of 2 or 3. Solutions including running over a longer simulation time and then averaging over a time interval, but already long simulations would become prohibitive. In using the Simulink output as a validation, the peak locations coincide with the demodulation model, and the amplitudes are in fair agreement.

Limitations of FFT Results Spectral leakage and dc offset from using a window that is not an integer number of periods. Because stimulation frequency is swept with multiple waveforms being multiplied, the correct window size for periodicity is difficult to determine, especially when one is considering errors of the order of 1 in 10^6 . A relatively long duration (100 second) time series is used to minimize the window effect; this also results in a frequency resolution of 0.01 Hz and for a 2.5 Hz brickwall filter, an integration of 250 points. A time resolution of 1 μ s is used to help capture the 90 us pulses accurately, but could result in errors in as much as 1 part in 90. At 100 million data points, a stimulation frequency from 100 Hz to 200 Hz at 1 Hz intervals could almost three hours. The results shown for both $\delta = 20$ Hz and $\delta = 80$ Hz show that the peak locations coincide with the Fourier spectral calculation, and that the amplitudes are in fair agreement.

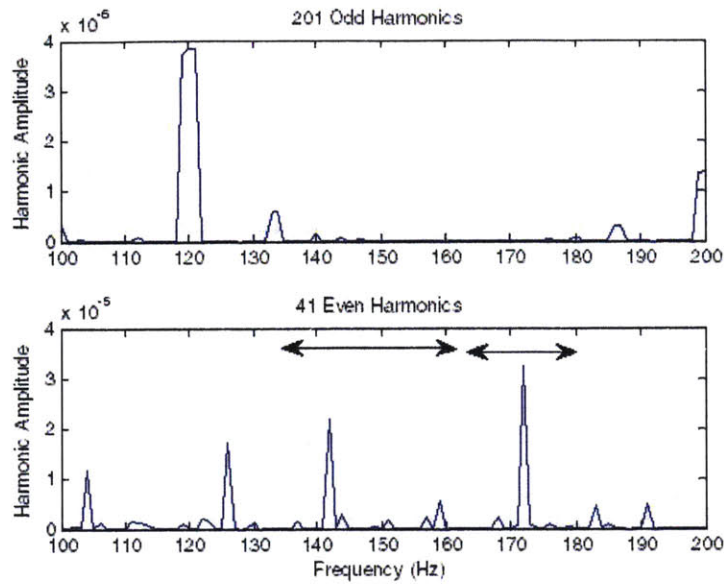


(a) From truncated Fourier series using 501 stim harmonics. Spectral power calculated from 2.5 Hz brickwall filter at 1 Hz steps. Note even harmonics dominate.

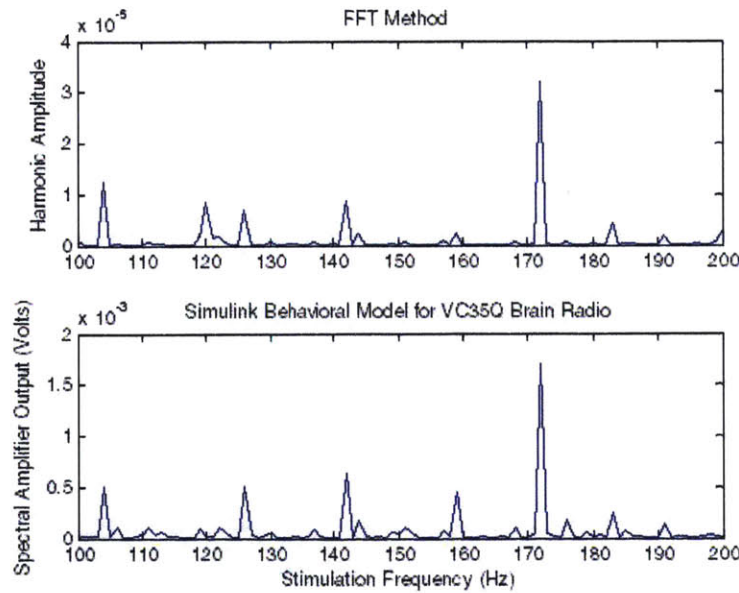


(b) FFT over 100 s at $1 \mu\text{s}$ resolution. 2.5 Hz brickwall filter after directly multiplied time domain waveforms. Simulink behavioral model included for comparison using 0.1 V stimulation.

Figure 5-10: Stimulation interference sensitivity for $\delta = 20 \text{ Hz}$. Unit stimulation pulses, $90 \mu\text{s}$ pulse width and master clock at 4432 Hz. Arrows indicate range over which experimental results are matched.



(a) From truncated Fourier series using 501 stim harmonics. Spectral power calculated from 2.5 Hz brickwall filter at 1 Hz steps. Note even harmonics dominate.



(b) FFT over 100 s at 1 μ s resolution. 2.5 Hz brickwall filter after directly multiplied time domain waveforms. Simulink behavioral model included for comparison using 0.1 V stimulation.

Figure 5-11: Stimulation interference sensitivity for $\delta = 80$ Hz. Unit stimulation pulses, 90 μ s pulse width and master clock at 4432 Hz. Arrows indicate range over which experimental results are matched.

Choosing the Master Clock at the Stimulation Harmonic Nulls

We can choose the master clock frequency, and the stimulation frequency and pulse width to minimize the effects of stimulation down-modulation.

We notice from Equation 5.9 that a null in the stimulation harmonics occurs at

$$k\omega_s d = n \frac{\pi}{2}, \quad \text{where } 2\pi f_{stim} = \omega_s, \quad (5.11)$$

which means that the stimulation period should be a multiple of the pulse width. For a pulse width of $d = 90 \mu\text{s}$,

$$f_{stim} = 2.778 \text{ kHz} \times \frac{n}{k}.$$

So, for a stimulation frequency between 100 and 200 Hz, $f_{stim} = 139 \text{ Hz}$ would be appropriate. To align the p_2 harmonic of ω to the null,

$$2 f_{mclk} = \frac{m}{4d}, \quad m \in \mathbb{Z}^+ \text{ and } 2\pi f_{mclk} = \omega.$$

For $f_{stim} = 139 \text{ Hz}$ and $d = 90 \mu\text{s}$ and a master clock which is close to the original 4 kHz,

$$f_{mclk} = 5.556 \text{ kHz}.$$

We chose to align the ω even harmonics so that the sidebands are near the nulls. Because, in general, stimulation harmonics are both even and odd, it is advantageous to choose d and hence f_{stim} so that f_{stim} is not a multiple of the δ frequency so that the sidebands do not coincide with the stimulation harmonics. In addition, a margin that is at least the power bandwidth should be included.

A note about frequency alignment in the face of input filtering (e.g. common-mode LPF, electrode-electrolyte, etc.): these are LTI systems so the original harmonic alignment is maintained. In addition, from summer research on Volterra systems, outputs from nonlinear time-invariant systems are strictly multiples of the input harmonics, so alignment should also be maintained. Other considerations include the accuracy of the master clock relative to the frequency generator for the stimulator.

Simulink Behavioral Model with Tanh Transconductor Model

The hyperbolic tangent model is appropriate for a transconductor operating in the subthreshold. The purpose of including this in the Simulink model is to investigate the effects in sensing of the saturating non-linearity from a high amplitude stimulation

pulse superposed on a brain signal.

The model assumes a subthreshold constant κ of 1/2.5. First order dynamics is also assumed at the input of the transconductor with a pole at 100 kHz. In Figure 9, one observes that the amplifier is saturated with stimulator pulses between 1 and 2 Volts. Estimates of the nominal input stimulation voltage is 0.8 V and could be higher from electrode impedance mismatches. Saturation does not appear to change the interference spectrum significantly. Additional work could include a filter at the front end to represent the electrode-electrolyte dynamics, and an additional cascading low pass filter to represent the off-chip common-mode filter.

5.2.2 Analog Circuit Design Specifications

The requirements for the NPIC, listed in Table III, were driven by several design inputs. These include:

- nominally resolving $< \approx 5 \mu\text{V}_{\text{rms}}$ biomarkers that indicate neural circuit state, with the ability to configure the channel for a broad range of possible spectral distributions and amplitude levels;
- providing multiple channels and modes of neural information, including time-domain data on the field potentials and relative phasing between two electrodes;
- compatibility with existing neurostimulator pulse amplitudes, supply levels and supply noise;
- protecting against single-fault failures, minimizing leakage current, and being robust to hazards in the field and during deployment like ESD or electrosurgery energy.

5.2.3 NPIC Spectral Analysis and Chopping Strategy

Analog preprocessing is used to extract key biomarker information from the neural field potential prior to digitization. To achieve this function, the signal chain must extract the energy from a specified band defined by the band-center δ with a bandwidth about δ defined by BW . Because the science of field potentials is rapidly evolving, we would like to maintain the most flexibility in setting δ and BW .

The following mathematical treatment for spectral analysis helps to motivate our circuit architecture. The spectral density of the desired signal is derived from the

Table 5.3: Key Requirements for NPIC Sensing ASIC.

| Specification | Value | Units/Comments |
|---|----------------|---|
| Supply Voltage | 1.7 to 2.1 | Volts |
| Supply Current | 2.5 | $\mu\text{A}/\text{channel}$; nominally trimmable with adaptive first stage biasing |
| Functional Modes | — | Time-domain ECoG, bandpower and relative phase |
| Number of Channels | 4 | Partitioned 2 per brain hemisphere |
| Switch Matrix | 8 to 8 | Electrode to amplifier multiplexor for setting sensing vector |
| Noise (time-domain ECoG mode) | 1 | μV_{rms} , 0.5-100 Hz noise BW; nominally trimmable with adaptive first stage biasing |
| Noise (bandpower mode) | <5 | μV_{rms} , 10 Hz voltage BW, 1 Hz output signal power BW |
| CMRR/PSRR | >80 | dB (DC to 500 Hz), driven by stim. supply noise |
| Functional Temperature Range | 20 to 45 | Celsius |
| High-Pass Corners | dc, 0.5, 2.5,8 | Hz, external 100 nF blocking cap. for safety, on-chip resistors |
| Band-center frequency | dc to 1 kHz | Hz in 4 Hz steps |
| Bandwidth | 5 to 25 | Hz in 2 Hz steps, 2 nd and 3 rd order roll-off |
| Power Bandwidth | 1, 10 | Hz, programmable |
| Amplifier Input Impedance | >5 | $\text{M}\Omega$ at dc using 5 mm ² Pt-Ir electrodes |
| Impedance to Stimulator/ Blanking Isolation | >500 | $\text{k}\Omega$ at 100 Hz nominal, preventing loading of therapy stimulation |
| Input Voltage Range/ Blanking Standoff | ± 10 | Volts |

conjugate product of the Fourier transform, which includes a windowing function $w(t)$ that embeds the bandwidth BW :

$$\varphi(f) \frac{X(f)^* X(f)}{2\pi}, \quad (5.12)$$

$$\text{where } X(f) \int_{-\infty}^{\infty} x(t)w(t)e^{-j2\pi ft} dt. \quad (5.13)$$

Expanding the spectral power $\varphi(f)$ using Euler's identity, we see that the net signal energy can be represented by the superposition of two orthogonal signal sources, *in-phase* and *quadrature* (90° out-of-phase)

$$\varphi(f) = \left| \int_{-\infty}^{\infty} x(t)w(t) \cos 2\pi ftdt \right|^2 + \left| \int_{-\infty}^{\infty} x(t)w(t) \sin 2\pi ftdt \right|^2 \quad (5.14)$$

Both terms ought to be considered since the phase relationship between the neural circuit and the interface IC are not correlated; note that this is the same phase ambiguity encountered with an incoherent AM communication system.

Equation 5.14 motivates the design of an analog signal chain for flexible spectral analysis. Along with significantly amplifying the neural signals, one needs to multiply the input neural signal by a sine and cosine term at the band-center, $\delta = 2\pi f$, window or equivalently set the effective bandwidth, square the signals, and then add them together with a final low-pass filter prior to digitization. Arguably, the most challenging portion is a pure multiplication of the neural signal $x(t)$ with the tone at δ ; by a minor manipulation of the chopper amplifier design in [22, 23], we can achieve both robust amplification and spectral extraction that is both highly flexible and robust to process variations with acceptable power consumption, modest noise penalty and minimal addition of silicon area.

5.2.4 Spectral Extraction Architecture Design

Chopper stabilization is a well-known noise-eliminating and power efficient architecture for amplifying low-frequency neural signals in micropower biomedical applications [22, 23, 119]. As previously discussed in [11], chopper-stabilized amplifiers can be adapted to provide wide dynamic range, high-Q filters. The key design difference from [24] is the offset of clock frequencies within the chopper amplifier to re-center a targeted signal band to dc in a manner similar to superheterodyne AM receivers [102]. As shown at node V_A in Figure 5-12, we use a modulation strategy equivalent to classical chopper stabilization such that the initial F_{clk} modulation frequency places the

signal well above the excess low-frequency noise corners (1/f, popcorn) [35]. After amplification, as a diversion from the classical chopper, demodulation is performed with a second clock of frequency, $F_{clk2} = F_{clk} + \delta$, that is shifted from the first clock by the desired band-center. The frequency convolution of the modulated signal with the second clock re-centers the neural signal initially at δ to dc and 2δ at the node V_B . Since the biomarkers are encoded as low frequency fluctuations of the spectral power, we filter out the 2δ component with an on-chip low-pass filter with a bandwidth defined as $BW/2$; signals on either side of δ are folded into the passband at V_{OUT} . The heterodyning chopper suppresses harmonics as the square of the harmonic order, to yield a net transfer function of

$$V_{out}(f) = \frac{4}{\pi^2} \sum_{n \text{ odd}} \frac{1}{n^2} V_{in}(f + \delta n) \cos \phi \quad (5.15)$$

where denotes n the harmonic order, and ϕ is the phase between the clock and the field potential input. Appendix A offers a short derivation of this operation.

To first order, the proposed chopper heterodynes the frequency content of the signal by the clock separation, δ , with a scale factor of $4/\pi^2$. The robustness of this design comes from the same features that make heterodyning attractive for AM radio applications-the center frequency is set by a programmable clock difference, which is relatively simple to synthesize on-chip, while the bandwidth and effective Q are set independently by a programmable low-pass filter.

The NPIC also allows us to perform a generalized spectral analysis by providing us with an analog electronic method to perform an inner product

$$Y_n(t) = \int_{-\infty}^{\infty} X(t)K_n(t)W(t)dt, \quad (5.16)$$

where $X(t)$ is the input signal, $K_n(t)$ is the n^{th} kernel or basis function, and is the time window. This operation is useful in the context of neural signal processing. For example, if the kernel is time-varying, we can directly extract joint time-frequency information such as how the spectral envelope evolves over time. In addition, this operation can be used to find time-windowed correlation between signals, or more generally, a “filtering” stage that can be made adaptive. Using these types of methods, where information is garnered in one step, reduces the amount of digital post-processing and helps ease power consumption requirements.

The operation shown in Equation is implemented in Figure 5-13 with parallel in-phase (I) and quadrature (Q) paths, using clocks derived from a master at twice the

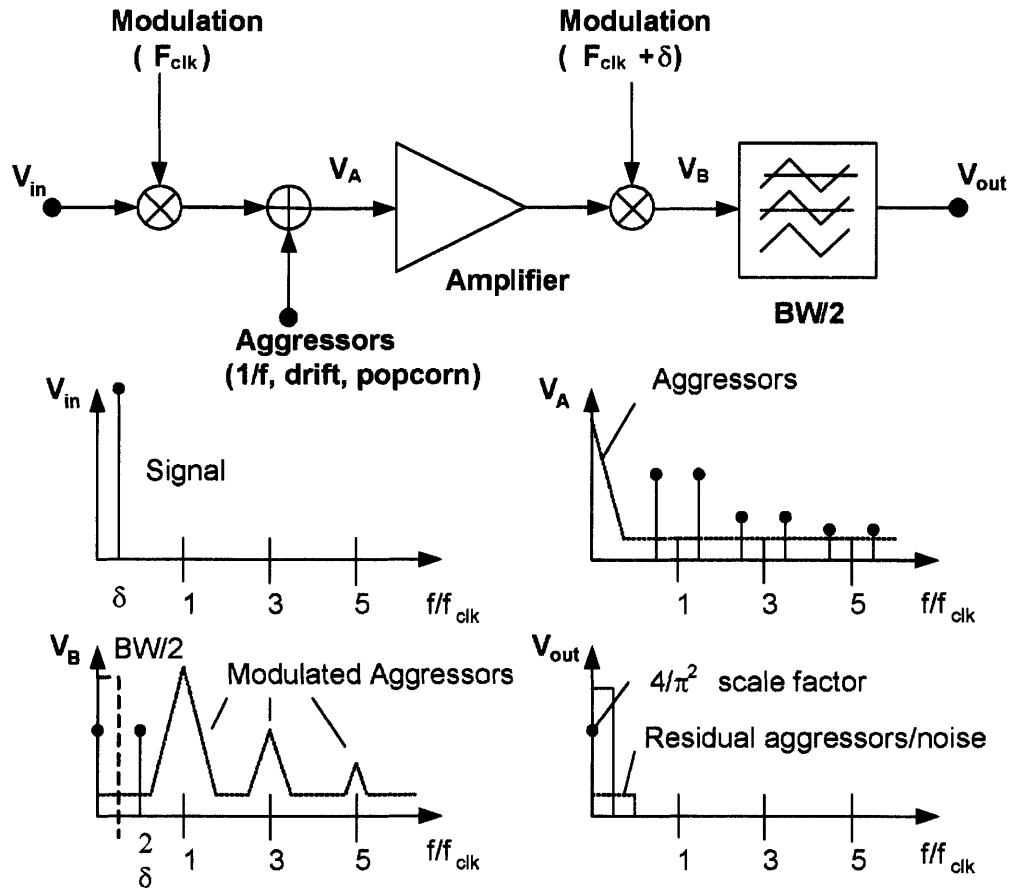


Figure 5-12: Concept of merging heterodyning and chopper stabilization for flexible bandpass selection.

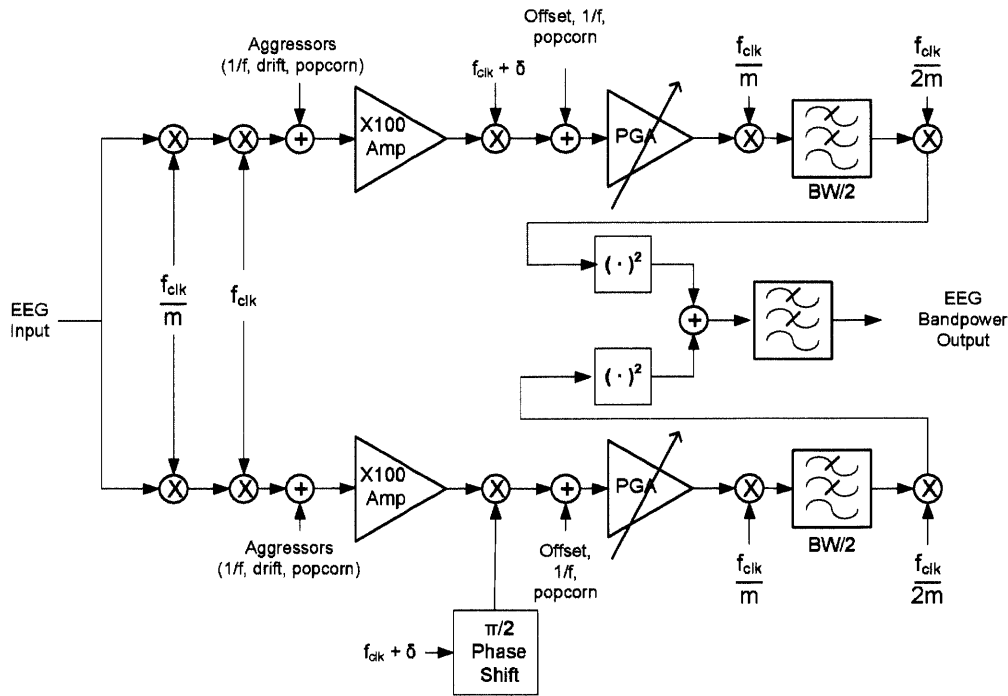


Figure 5-13: Tunable heterodyning EEG receiver extracts signal power within the physiologically relevant band. The dual-nested chopper architecture uses two different chopper frequencies to improve the power-bandwidth tradeoff while eliminating offsets and low frequency noise.

chopper frequency. As shown in the block diagram of the signal chain in Figure 5-13, the final power extraction is achieved with the superposition of the squared in-phase and quadrature signals, yielding a transfer function for the entire signal chain of

$$V_{\text{EEG_Power}}(f) \propto \left[\frac{4}{\pi^2} \sum_{n \text{ odd}} \frac{1}{n^2} V_{in}(f + \delta n) \right]^2. \quad (5.17)$$

The residual sensitivity to odd harmonics is not a major concern in our application because the signal power in the cortical circuits generally falls off with a 1/f law [31]. This means that the net measured power of the neuronal signals at the third harmonic is effectively down by 48 dB, hence maintaining an acceptable selectivity to the pertinent band. For applications that require better harmonic attenuation, one can implement a notched clock strategy to suppress higher order harmonic content [100].

5.2.5 Chopper Modulation Strategy for the NPIC

Several chopper modulation techniques are required to achieve microvolt signal resolution with the NPIC's spectral analysis strategy. The total signal chain with modulation is detailed in Figure 5-13. As discussed in the previous section, the “core” chopper modulation, with two clocks separated by δ provides the mechanism for selecting the band of interest. Although this does achieve the necessary frequency heterodyning, two practical issues remain.

The first issue is that the residual offsets in the core chopper can be on the order of several microvolts. The problem with this residual offset is that it is superimposed on the signal of interest, which causes significant signal perturbations in the output signal as the phase of the biomarker beats against the δ clock per (4). To fix this problem, we implemented a “nested” chopper switch set [14] before the first chopper amplifier, and after the programmable gain amplifier (PGA). The small residual offsets are then up-modulated and filtered out using the $BW/2$ selection filter. The nested loop runs slow enough ($F_{clk}/64$, 128 Hz), to minimize residual charge injection offset, but fast enough to minimize perturbations to low-frequency dynamics [14]. Note that since the PGA is also embedded in the loop, its residual $1/f$ noise and offset is also suppressed at the lower rate. The use of the passive low-pass architecture in the $BW/2$ -selection block minimizes additional contributions of offset to the signal chain after the nested chopper.

The second issue is that residual offsets in the output multiplier blocks create an intermodulation product that also creates significant distortion when trying to resolve microvolt signals. The use of a low-frequency chopper prior to multiplication corrects that issue; note that since the multiplier squares the signal, we do not require a subsequent down-modulation block. Recent work has used similar techniques to stabilize multiplication circuits and mixers [42]. The details of this design will be discussed in the transistor-level description of the multiplier.

5.2.6 Adapting the NPIC for Time-Domain ECOG and Impedance Measurements

In addition to bandpower extraction, the heterodyning chopper amplifier has several uses when the clock difference, δ , is set to zero. One application involves measuring the raw time-domain neural signal without preprocessing to provide standard EEG or ECoG/LFP recordings. This mode of operation can be especially useful for pre-screening the waveforms to identify the pertinent spectral biomarkers and to confirm

algorithm functionality using classical time-domain techniques [8]. Another application involves measuring the impedance by the addition of a $10\ \mu\text{A}$ current stimulation injected across electrodes at the chopper clock frequency and fixing the state of the front-end modulators. Tapping the signal output of the in-phase channel provides the resistive component of the impedance, while the quadrature output is the imaginary part. This complex impedance measurement is useful for characterizing the electrode-tissue interface and ensuring lead integrity. This feature will not be discussed further due to limited space.

5.3 Transistor-Level NPIC Design

5.3.1 Overall NPIC Architecture

The NPIC provides a streamlined conditioning interface between the electrodes, the microcontroller, and the loop recording memory. As shown in Figure 5-4, the NPIC has three primary blocks: four independently configurable analog spectral analyzers, an electrode switch matrix that allows the flexible selection of the electrode vector for measurement after electrode placement, and a digital core for interfacing to both the microprocessor for processing and configuration, and the loop recorder for memory storage. Although a fully-differential design is possible, power consumption tradeoffs and the need to drive single-ended low-power A/Ds led us to this single-ended design.

The remaining sections provide the transistor-level details for the core blocks in the analog spectral processing chain illustrated in Figure 5-13. In particular, we will focus on the design of the heterodyning chopper amplifier for selecting the band-center δ , the PGA embedded in the nested chopper for supplemental gain, the programmable low-pass filter for setting the filter bandwidth parameter $BW/2$, and the extraction circuit for merging the two phases of the signal and providing the net signal bandpower. Key support circuits like the electrode-tissue interface, the memory interface and the clock generation will also be briefly discussed.

5.3.2 Electrode Interfacing to the NPIC

Neural tissue safety is paramount in the interface between the sensing IC and the electrodes. The primary concern is to minimize the probability of dc current flowing through the electrode-sense IC interface to avoid corrosion and pH imbalance [41]. To block dc current, the sense IC input connects to the platinum-iridium electrodes

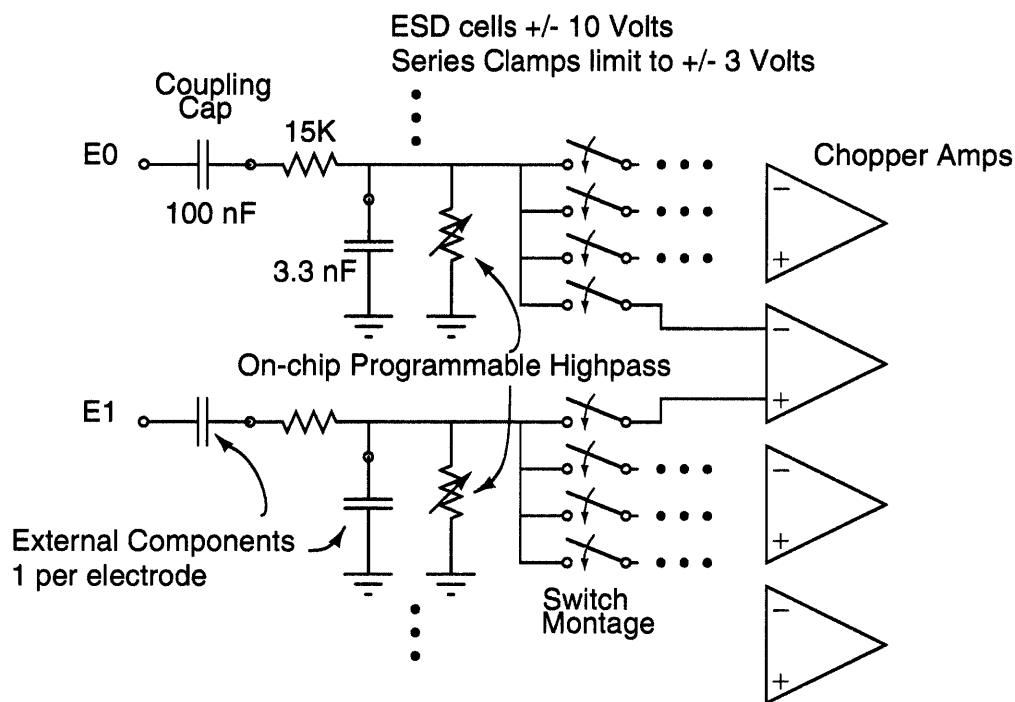


Figure 5-14: The interface between the sensing front-end and the electrodes. Off-chip capacitors are used to isolate the sensing IC from the electrodes.

through a passive coupling array shown in Figure 5-14. The passive array consists of one off-chip 100 nF capacitor for each electrode that is placed in series between the electrode and the sense IC input pad. Although this capacitor is effective at blocking dc currents, it can undermine CMRR if the loading is unbalanced at the amplifier inputs. The high common-mode input impedance of the chopper amplifier, however, minimizes this as a practical concern, and the 80 dB CMRR is essentially set by the matching that can be achieved with the external 100 nF passive array.

Another safety constraint is that the addition of sensing functionality must not affect the core stimulation therapy. To ensure compatibility with stimulation, on-chip ESD cells and input limiting clamps maintain high impedance over a 10 V differential drive across an electrode pair. The combination of coupling capacitors and high input impedance minimizes the parallel load of the sensing interface when compared to the neighboring tissue shunting the electrode vector.

Signal fidelity was also considered in the design of the electrode-NPIC interface. In particular, attention was paid to avoid rectification in nonlinearities that might confound measurements. Pre-filtering the signal at the front-end, prior to the silicon junctions, helps to minimize the rectification of high-bandwidth signals from sources

like telemetry links. To implement this, a series on-chip $15\text{ k}\Omega$ resistor is shunted by an off-chip 3.3 nF capacitor, one per channel, in front of all low-voltage rectifying junctions like the limiting clamp or switch multiplexer. In addition, to avoid beating of clock frequencies from each of the four channels at the nonlinear electrode-tissue interface, the front-end choppers use a common clock. The tunable clock for each channel is placed at the back end of the signal chain, where it is well isolated from the tissue interface.

Although the use of off-chip capacitors does create a penalty in total hybrid area, we erred on the side of caution in this research prototype to maximize safety and to enhance probability of obtaining robust signals. We did take advantage of the blocking capacitors to provide the low-frequency high-pass filtering of the signal chain. The 100 nF blocking capacitors are used in combination with a programmable resistor on the sensing IC to set the high-pass corner for the signal chain. The high-pass corner can be selected by the microcontroller as 0.5 , 2.5 , and 8 Hz , with an additional dc test mode.

5.3.3 Heterodyning Chopper Amplifier Front-End

The system requirements budget in Table III motivates the following specifications for the front-end: amplify the differential signal from the electrodes by 32 dB , with a noise floor below $150\text{ nV}/\sqrt{\text{Hz}}$ while drawing 750 nA , while translating the relevant band-center δ to dc. In this design, both noise and bandwidth are trimmable by adjustable first-stage biasing and compensation capacitors.

Heterodyning with the chopper amplifier, as described in Section II, required only minor changes to the core circuitry in [22, 23]. As illustrated in Figure 5-15, the amplifier still works by balancing an up-modulated charge from the differential input voltage with an up-modulated feedback charge, with the net gain set by the relative scaling of the input and feedback capacitors. However, a small change allows us to heterodyne the signal by running the front-end modulation clock independently of that for the demodulation amplifier and the feedback network.

As discussed previously, the relative clock difference δ between the two clocks translates the relative frequency of the input signal by an equivalent amount. The suppression of the $1/f$ noise and popcorn noise is still integral to the design, but we achieve the desired heterodyning transfer function with an additional amplification set by on-chip capacitor ratios. In our design, the ratio of input and feedback capacitors was set to $20\text{ pF}/200\text{ fF}$ to provide 32 dB of net gain before the second stage of

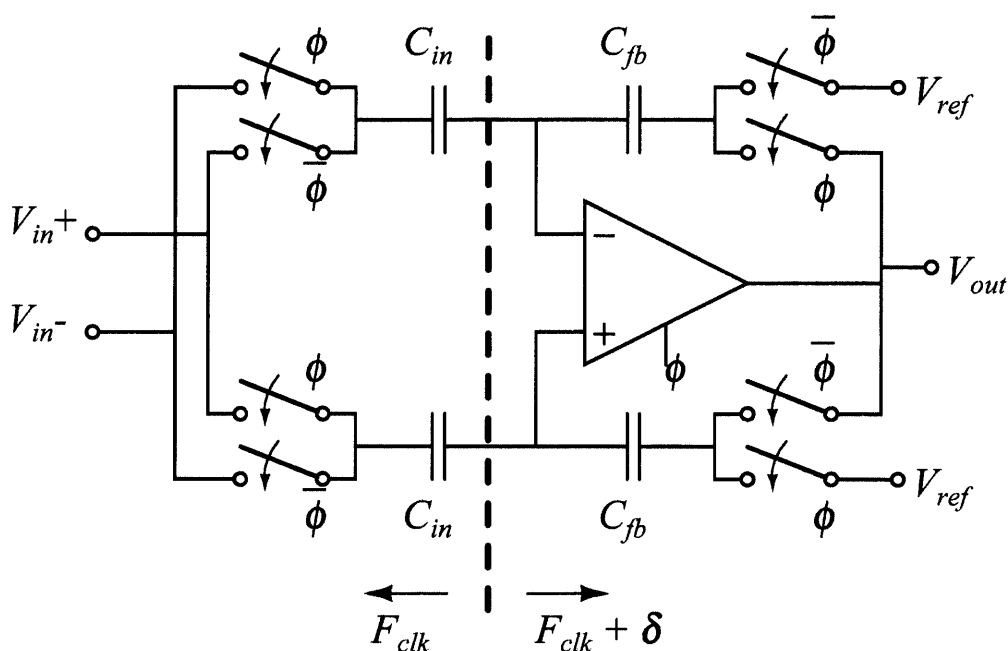


Figure 5-15: The basic chopper stabilized instrumentation amplifier presented in [8]. The only modification was to partition the input modulation clock to be independent of the amplifier and feedback modulation clock.

amplification (recall the 0.4 scale factor in (3)). The quadrature path uses the same circuit design, but with that chains $F_{clk} + \delta$ clock phase shifted by 90° .

The design of the demodulation and amplification block within the heterodyning instrumentation amplifier aims for low noise while operating at a low supply voltage. The design was based on the folded-cascode architecture described in [42], which adds two sets of CMOS switches to the classical folded-cascode to implement chopper stabilization by steering currents at low impedance nodes. The schematic shown in Figure 5-16 is similar to that in [23], with a modification to the differential second stage, which results in a better PSRR.

The benefit of the current-mode switch architecture is that the transients from chopper modulation are orders of magnitude faster than the chopper clock period. This separation of dynamics helps to suppress second harmonic distortion and amplification errors seen in many micropower designs [23]. Since the output of the transconductance stage is at baseband, the integrator can both compensate the feedback loop and filter up-modulated noise and offsets. As an additional advantage from heterodyning, the pertinent band is also shifted to dc at this point in the signal chain, so the remaining circuitry can run at a reduced bandwidth to minimize power.

The transistor-level design of the demodulation amplifier focused on minimizing

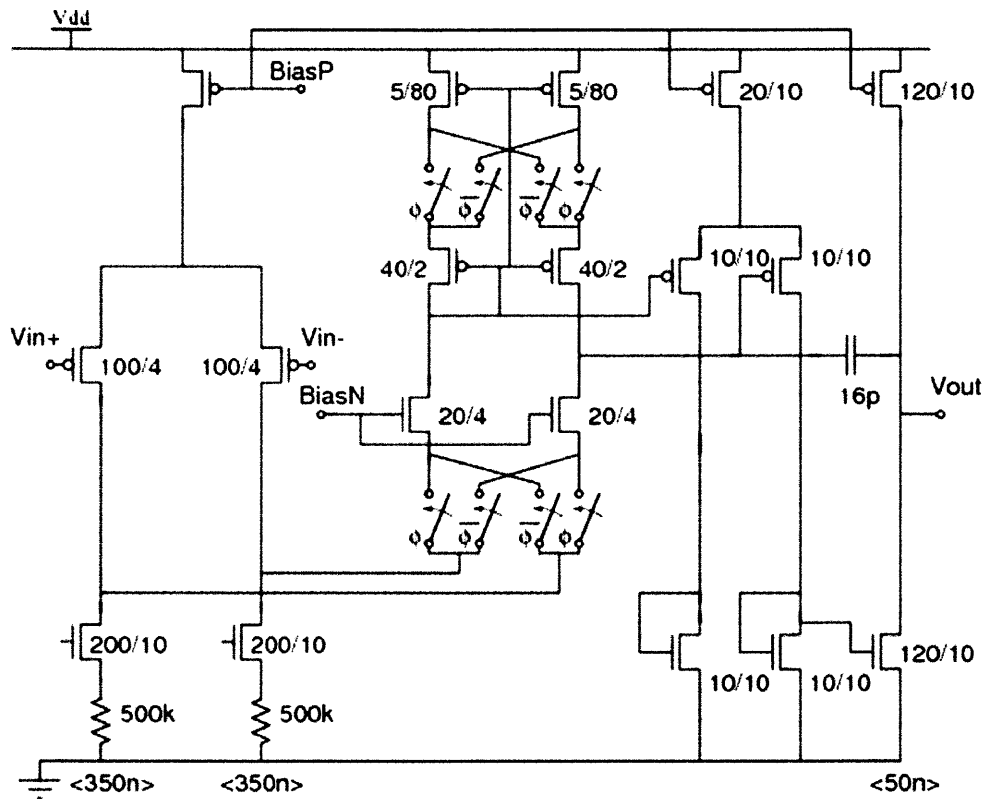


Figure 5-16: The core chopper instrumentation amplifier from [23] that provides both amplification and heterodyning of the input signal down to dc.

noise. An advantage of a folded cascode is that currents can be partitioned to improve noise performance. In this design, we allocated 600 nA of tail current for the input pair, 50 nA to flow through each leg of the folded cascode, 50 nA for the output stage, and 50 nA for bias generation and distribution. This partitioning places the majority of current into the input pair to maximize transconductance in comparison to the other FETs in the amplifier, while still biasing the transistors in sub-threshold. To suppress the relative noise contribution from the biasing NFETs, they were scaled to be relatively large to reduce the effective $1/f$ noise along with an additional 500 k Ω of source degeneration to lower their effective transconductance relative to the input pair.

Compensation of the heterodyning chopper's feedback loop was also designed into the folded-cascode amplifier. The output stage of the amplifier serves as an integrator for stabilizing the feedback loop. Since the chopper modulation in the amplifier is correlated with that in the feedback path, the overall feedback path of Figure 5-15 can be compensated as a typical g_m/C amplifier. The 16 pF compensation capacitor stabilizes the amplifier as an equivalent first-order system; the choice of open-loop gain eliminated the need for a compensation zero. We designed for a minimum bandwidth of 500 Hz with the 40 dB gain to provide adequate gain-bandwidth for time-domain recording. Note that for loop compensation design, the scaling of the feedback path is equivalent to a gain ratio of 100—the $4/\pi^2$ heterodyning scale factor that results from the clock differential between the input and feedback path is not part of the synchronous loop gain.

At this stage of the signal chain, the input band is both preamplified with a fixed gain with a translated frequency that is centered about dc, with residual modulation at 128 Hz from the nested chopper. The next stage further amplifies the signal to the level appropriate for analog-to-digital conversion, using programmable gain amplification for a wider dynamic range.

5.3.4 Programmable Differential Gain Amplifier

The goal of this block is two-fold: first, to convert the single-ended signal from the previous stage to a differential output so that nested chopping described in Section II-D can be implemented; second, to amplify the physiological signal to minimize the dynamic range requirements of the ADC in the microcontroller. Since the gain required from this block is dependent on several factors including specific patient characteristics, electrode location, and intended control algorithm, we designed the

amplifier to be configured from a signal fed back from a control algorithm running on a microcontroller. The block requires programmable, yet stable gain characteristics ($\times 5$, $\times 10$, $\times 20$, and $\times 40$, with $\pm 5\%$ accuracy), $< 0.5\%$ distortion with a 100 mV input, modest noise ($< 1 \mu\text{V}/\sqrt{\text{Hz}}$), 200 nA current consumption, and a high enough input impedance to avoid loading the chopper amplifier. These requirements were derived from behavioral modeling of the analog spectral analyzer and digital algorithms using sampled ECoG recordings for applications like those described in [60].

The programmable gain amplifier is based on a linear instrumentation amplifier with stable gain characteristics. The circuit design, illustrated in Figure 5-17, was adapted from a micropower MEMS accelerometer [25,26]. The key design concept of this circuit is that the current through the front-end FETs is held constant by a minor servo loop. The servo forces the differential voltage at the inputs to fall predominantly across the source resistor, minimizing distortion from a variable gate-source voltage. The source resistor is programmable from 1 M Ω to 8 M Ω using switches that shunt the CrSi resistors. By mirroring the topside servo currents to an output resistor tap, we can achieve a gain set by resistor ratios that is stable across process corners and temperature. By supplying a reference to the mid-point of the resistor string, we can also set an arbitrary bias point on the amplifier's output depending on the requirements of the next stage. The tradeoff of this design is an increase in noise from the source degeneration resistor and the low current mirrors. Since this is a second-stage amplifier, the block provides adequate noise margin with 200 nA of supply current.

At this stage, the signal is fully amplified and the band-center translated to dc after the nested chopper modulator. The next stage of the analog spectral processor is to band-limit the signal to set the filter bandwidth, and suppress residual up-modulated offset and noise from the nested chopper.

5.3.5 Programmable Bandwidth Selection Filter

The goal of this block is to select the effective bandwidth, BW, prior to the stages that extract signal power. The requirements are to create a 2-pole or 3-pole low-pass filter, with a corner frequency that is variable from 5 to 25 Hz, or 3 to 15 Hz, respectively. The trim step size should be in 4 and 2 Hz increments, respectively. Once again, these requirements were derived from behavioral modeling of the signal chain based on recorded waveforms of ECoG activity, and the need to compensate for common process variations in the passive components.

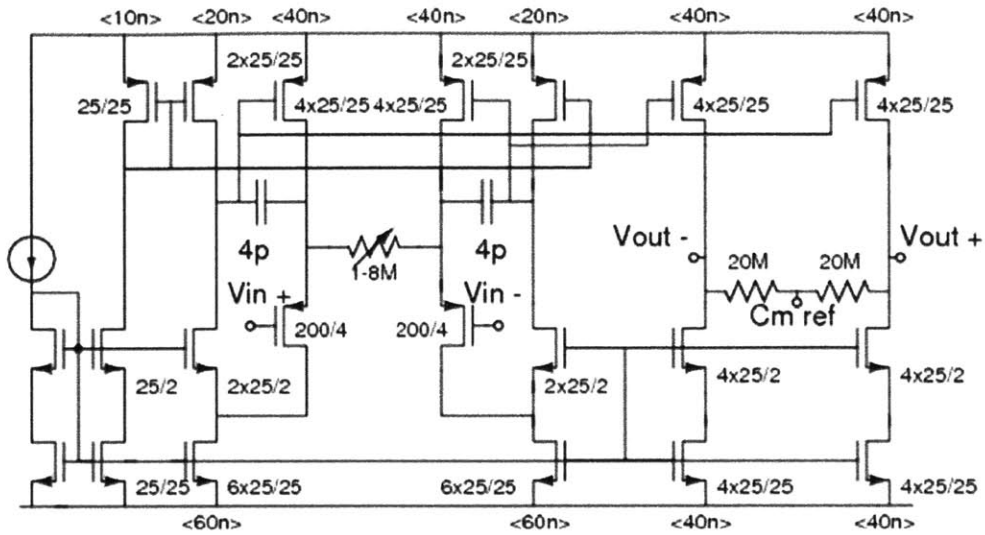


Figure 5-17: Differential programmable instrumentation amplifier.

The design implementation takes advantage of our high resistance CrSi layer to build an on-chip passive low-pass filter. Referring to Figure 5-18, the signal chain is a simple stagger-tuned chain of RC filters. We chose this approach to maximize the linearity and headroom of the filter while minimizing the power dissipation. The trimming is achieved with FET switches to shunt elements of the CrSi resistor string. The sizing of the components was such that the CrSi could be deposited on top of the poly-poly capacitor's top plate to share the same form factor. The other design element is that the time constant scaling can be trimmed for a quasi-Gaussian profile to help minimize the time-frequency duality limits of the Fourier transform [102]. Note that both parallel chains in the spectral processor, in-phase and quadrature, share the same low-pass filter control register.

At this stage, the band center for the relevant frequencies is selected by the heterodyning chopper, fully amplified, and the bandwidth independently selected with the low-pass filter. The final stage of the spectral processor is to extract the signal power in the band by superimposing the in-phase and quadrature components.

5.3.6 Chopper-Stabilized Power Measurement

The purpose of this block is to extract the net signal power in the relevant physiological band. This involves two operations: first, squaring the signal in the band; second, adding the two squared signals to obtain the net signal power. Additional

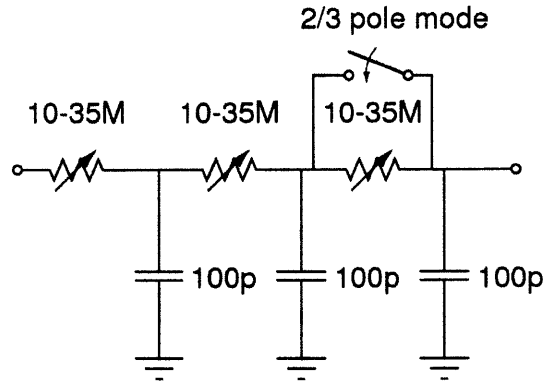


Figure 5-18: The programmable lowpass filter for independently selecting the bandwidth of the chain.

operations include programmable low-pass filtering of the signal power output with corner frequencies that can be varied between 1 and 10 Hz, and to achieve a net gain of about $1V/V^2$ with a nominal input signal of 10 mV while using only 120 nA total bias.

The implementation of the block uses a modified multiplier circuit described in [46]. As shown in Figure 5-19, the multiplier uses the self-biased cascade architecture to provide the necessary level shifting to drive the inputs to the tangent-squaring circuit. Each phase uses the same multiplier architecture, and their outputs are superimposed onto a shunt resistor to provide a rail-to-rail drive. The net transfer function is

$$V_{out} = I_b R \tanh^2 \left(\frac{V_{in}(t)}{2\eta V_{th}} \right). \quad (5.18)$$

Equation 5.18 suggests that the phase sensitivity of the signal chain is ideally eliminated during this power estimation step. This transfer function achieves the requirement of the $1V/V^2$ scaling assuming a differential pair bias I_b of 60 nA and load resistor R of 60 M Ω , 10 mV at the input and subthreshold factor η of 1.5 for the process with the thermal voltage $V_{th} \approx 25$ mV.

Although the core multiplier circuit provides the nominal function of power extraction, errors make it insufficient for our application. The issue is that as the multipliers have intrinsic offsets, V_{off} , on the order of millivolts, which are not trivial compared to our microvolt biomarkers. When these are added to the input signal,

$$V_{out}(t) \propto V_{in}^2(t) + V_{off}^2(t) + 2V_{in}V_{off}, \quad (5.19)$$

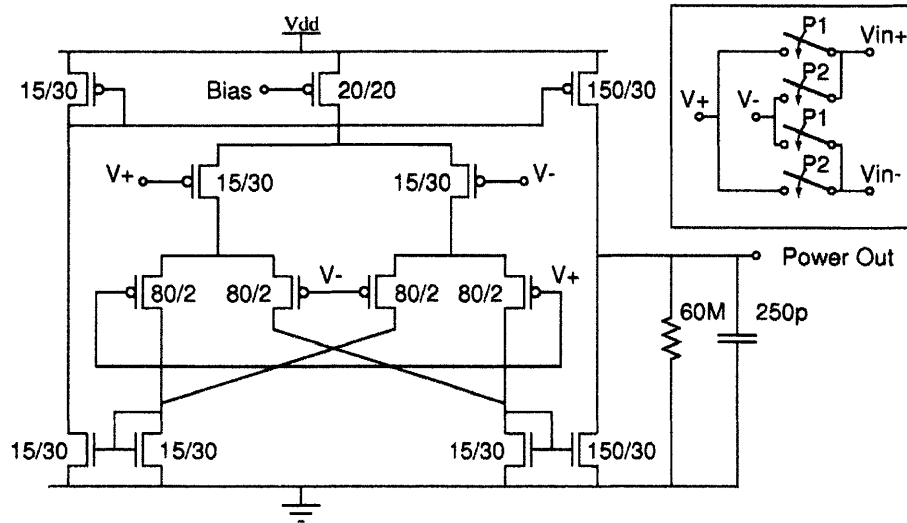


Figure 5-19: One phase of the power extraction block; the two phases are added as currents onto the “power out” node.

they form a product that adds a relative amplitude scaling that is dependent on the multiplier’s offset and can be different among the channels. As a signal beats between the in-phase and quadrature channels, the scaling mismatch creates a significant distortion that would confound our algorithms and make monitoring power fluctuations difficult since we cannot easily discriminate beating from neuronal biomarkers. To provide the accuracy required for biomarker detection, chopper stabilization of the multipliers is also employed. The inputs are modulated at $F_{clk}/128$ (64 Hz) with an input chopper, and the net transfer function through the multiplier is then modified to

$$V_{out}(t) \propto V_{in}^2(t) + V_{off}^2 + 2DV_{in}V_{off} - (1 - D)V_{in}V_{off}, \quad (5.20)$$

where D is the duty cycle of the chopper. As long as the duty cycle is 0.5, and the output of the power block can low-pass filter the 64 Hz modulation product, then the cross-term is eliminated and the offset is limited to a static offset term can be programmatically trimmed during a calibration process. This circuit uses techniques similar to those discussed in [42, 66].

The output of the power block has an on-chip capacitor to limit the power bandwidth to 10 Hz at the power output node, when the pad and interconnect parasitics are included. Additional filtering can be added by switching in an off-chip capacitor, depending on the application needs.

At this stage, the LFP signal has been amplified and the power from the relevant physiological band has been extracted using a heterodyned chopper amplifier, programmable gain amplifier, low-pass filter and power extraction block. The power envelope now holds the key biomarker information, and the ADC and digital processing requires minimal bandwidth and dynamic range to perform its algorithms. This is the boundary of the sensing IC, and the signals are now passed to the microprocessor for digitization and algorithmic processing.

5.3.7 Differential Clock Generation

The clock tree is designed such that the four channels share a common 4 kHz F_{clk} driver for the front-end modulators. Each sensing channel also has a dedicated local clock to create the $F_{clk} + \delta$ reference for the back-end chopper block. The clocks are trimmed to twice their nominal value and then down-sampled to provide the in-phase and quadrature clocking.

The clock design is a simple relaxation oscillator and will not be reviewed in detail here. The clocks were designed to provide a nominal 50% duty cycle to suppress sensitivity to even harmonics. To minimize the impact on the power budget, the clock was allocated 200 nA/channel. The clock frequency is adjustable with capacitive trims to achieve the 4 Hz step sizes from dc to 500 Hz. The trims are accessible through the register port and to minimize drift, the microprocessor routinely calibrates the clocks by comparing periods with the crystal oscillator embedded within the existing neurostimulator. Relative clock matching is critical for robust operation of the circuit, and our results will demonstrate that we can achieve acceptable performance for our application.

5.3.8 Digital Control Interface

The sense IC contains a digital interface that enables the microprocessor control of the sense channels through memory-mapped registers. Parameters such as gain and trim states can be adjusted. Also included in this block is a port expander that is used to interface the microcontroller to the 1 MB loop-recording SRAM. Another support function is a sample clock for the ADCs, which allows the processor to enter a low power sleep mode between samples, allowing the net processor duty cycle to be reduced to as low as 1% for digitization and algorithms.

5.3.9 Layout and Die Photo

Because the sensing IC is mixed-signal, the layout is partitioned to ensure signal integrity and to enable the efficient use of area. In reference to Figure 5-20, the analog connections to the electrode coupling array are routed to the top of the chip, with analog small signal nodes restricted to the top pad row. The electrode inputs feed into the switch matrix, then route into four slices of spectral processor chains. The δ clock signals are generated and routed locally within each processor slice to minimize the probability of cross-channel coupling. The digital interface for register and memory control is restricted to the bottom portion of the IC, separated from the sensitive analog with substantial isolation rings. The analog outputs and interfaces to the microcontroller form the bottom row of pads. The two horizontal rows are bonded to the SRAM memory, upon which this IC is stacked to form a complete module that is then packaged for solder bumping on the hybrid. The total die area is $6700\ \mu\text{m}$ by $6700\ \mu\text{m}$ and each analog spectral processor requires $5\ \text{mm}^2$.

5.4 Sense Channel Prototype Results

The mixed signal sensing IC was prototyped in a $0.8\ \mu\text{m}$ CMOS process; Table IV summarizes the results. In this section, we discuss the key results of this custom IC as a stand-alone circuit, with particular emphasis on the signal extraction characteristics of the signal chain as an input BMI. Section V is a detail of the results of the bidirectional BMI within a typical neurostimulator environment.

5.4.1 General Performance of the Analog Spectral Analyzer

The combined amplification and analog signal processing circuits enable chronic sensing to be powered by a primary cell battery by keeping consumption to roughly $5\ \mu\text{W}$ per channel. The total current draw of the prototype was measured to be $2.5\ \mu\text{A}$ per channel from a $1.8\ \text{V}$ supply: $2.2\ \mu\text{A}$ for the two phases of the heterodyning chopper amplifier and power extraction circuit, and $0.3\ \mu\text{A}$ for shared support circuitry like the common input clock and reference biasing. The design for low voltage headroom allows “half-battery” operation from a lithium battery for improved noise efficiency [45].

The filtering properties of the signal chain support the detection of a broad range of field potential biomarkers. Figure 5-21 illustrates the spectral tuning capabilities

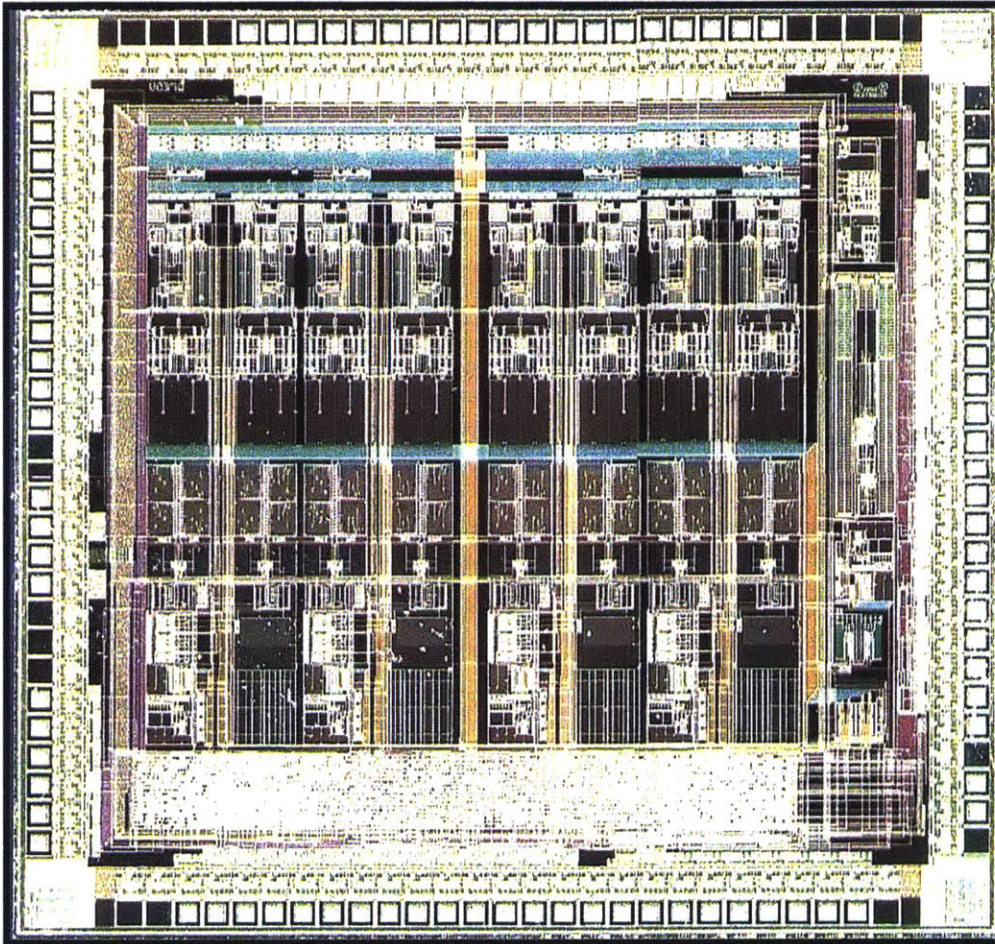


Figure 5-20: Die photo of the NPIC fabricated in a 0.8 μm CMOS process. The total die area is 6700 μm by 6700 μm , and each analog spectral processor requires roughly 5 mm^2 .

Table 5.4: Key Sensing and Processing IC Results

| Specification | Value | Units/Comments |
|--|---------------|---|
| Supply Voltage | 1.4 to 3.3 | Volts |
| Supply Power | 4.5 | μ W/channel (1.8V) |
| Total Channel Gain | 54 to 80 | dB, programmable |
| Signal Power Noise Floor (min detection) | ~ 1.5 | μ V _{rms} 3σ -resolution floor , 10 Hz noise bandwidth, 1 Hz power band (trimmable w/ first stage bias current) |
| CMRR, PSRR | > 80 | dB (DC to 500Hz) |
| Bandpower Center (δ) | DC to 500 | Hz |
| Trim Step Size | 5 | Hz |
| Bandpower | 5 to 25, | Hz (2-pole) |
| Bandwidth (BW/2) | 3 to 15 | Hz (3-pole) |
| Trim Step Size | 4,2 \pm 15% | Hz (2, 3 pole) |
| High-Pass Corners | 0.4, 2.5, 8 | Hz |
| Clock Jitter | < \pm 1 | Hz, 4σ |
| Clock Drift | < 0.1, 0.5 | Hz / $^{\circ}$ C (mean, 4σ) |
| Linearity (Pre-power) | < -65 dB | THD (0.001-1 mV input) |

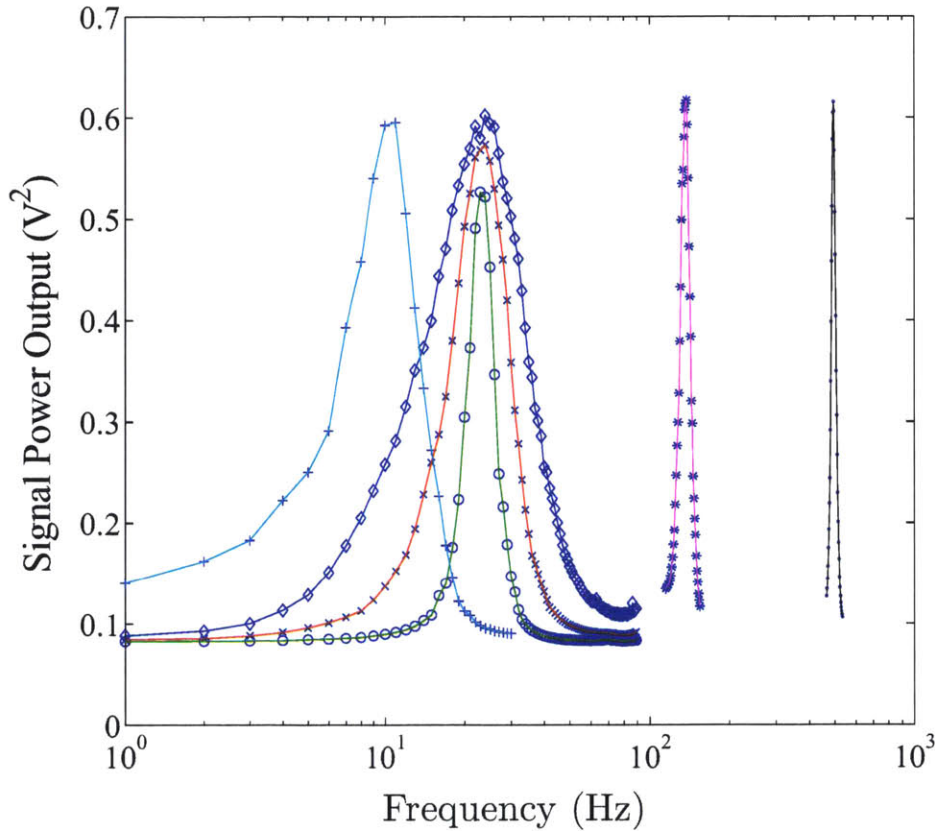


Figure 5-21: Demonstration of band selectivity with the sensing IC across a broad selection of physiologically relevant frequencies, using a 50 μV test tone. (+) $\delta = 10$ Hz, $Q \approx 1.25$; (\diamond) $\delta = 24$ Hz, $Q \approx 1$; (\times) $\delta = 24$ Hz, $Q \approx 1.5$; (\circ) $\delta = 24$ Hz, $Q \approx 3.5$; (*) $\delta = 136$, $Q \approx 20$; (\cdot) $\delta = 500$ Hz, $Q \approx 18$.

of the amplifier for signals between 10 Hz and 500 Hz. This range of programmability, in 5 Hz steps, covers both known biomarkers detectable in surface EEG, as well as significantly higher frequency biomarkers like those described in [48, 116]. Figure 5-21 also highlights the independent bandwidth tuning about a targeted frequency, providing highly flexible Q tuning over the broad physiological range of interest.

The analog preprocessing IC maintains flexibility and robustness through digital configuration and calibration via the system microprocessor. Trim states are programmed with an I^2C interface, and can be either adjusted as part of an algorithmic search process, e.g., a swept-sine spectrogram, or a spectral sensing state can be set and held. An automatic trim routine for selecting bands was implemented by passing the on-chip clocks to the microprocessor on a digital test bus and then using the neurostimulator's crystal-based clock as a reference. This allows periodic calibration of the channel in the field, if needed, to maintain accurate filtering characteristics

over the lifetime of the implant.

5.4.2 Noise Floor and Biomarker Resolution

A low noise floor for the IC ensures the ability to detect biomarkers for neural states. Resolution is limited by the noise floor of the heterodyned chopper amplifier, which when running in a mode as a standard chopper has a noise floor of $100 \text{ nV}/\sqrt{\text{Hz}}$ [22]. With heterodyning and the addition of the in-phase and quadrature channels, the noise is folded into a dc component per Appendix B. The power spectral density spread over the bandwidth BW and scaled by the cyclostationary noise factor $\alpha = 3/8$ [84]:

$$V_{n,\text{out}} \approx \alpha \left(\frac{\pi^2}{4} \right)^2 e_n^2 BW [V^2], \quad (5.21)$$

predicting a small-signal rms noise floor for signal power detection of $\sigma \approx 0.5 \mu\text{V}_{\text{rms}}$ with channel parameters programmed for measuring 1 Hz (BW_{power}) signal power variations of a 10 Hz (BW) band of frequencies. As we discuss in Section V, the long-term background subtraction removes the dc term from the detection algorithm, making the variance of the signal power deviations the main source of detection error.

On-off keying of test tones in Figure 5-22b roughly demonstrates the minimum detectable signal of the entire signal chain, defined as a shift in mean power amplitude greater than the peak-to-peak power noise floor, by showing a resolvable signal that is approximately $1.4 \mu\text{V}_{\text{rms}}$ above the noise floor, with channel parameters of $BW = 10 \text{ Hz}$, and $BW_{\text{power}} = 1 \text{ Hz}$. This agrees with the theoretical expectation that a $1.5 \mu\text{V}_{\text{rms}}$ signal can be resolved in $0.5 \mu\text{V}_{\text{rms}}$ of noise, which is suitable for detecting most relevant biomarkers for neuroprosthesis and adaptively controlled deep-brain stimulators per Table II. For the smallest biomarkers, the signal-to-noise ratio is improved by increasing the input stage bias current. Figure 5-22b illustrates that by increasing the bias current of the input stage by a factor of three, biomarkers on the order of $0.5 \mu\text{V}$ are resolvable.

There are a number of additional considerations for implementing a robust hardware system suitable for biomarker detection. Figure 5-22a demonstrates that the output fits the expected square law ($R > 0.99$) over two decades of input voltage. However, we point out that in Figure 5-23, the noise is larger when the tone is keyed on than when it is off; the noise characteristic of the circuit is nonlinear in that the output rms noise is proportional to the input signal level, while the output level varies quadratically, which is the result of squaring an input with an additive noise.

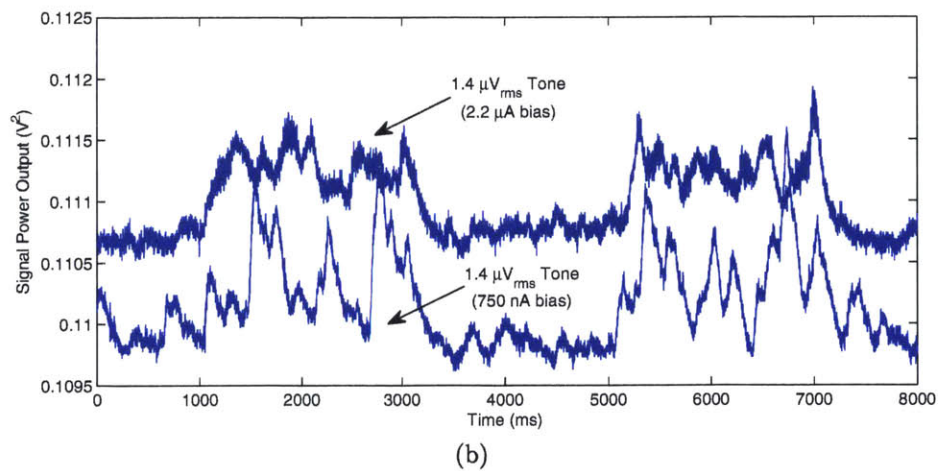
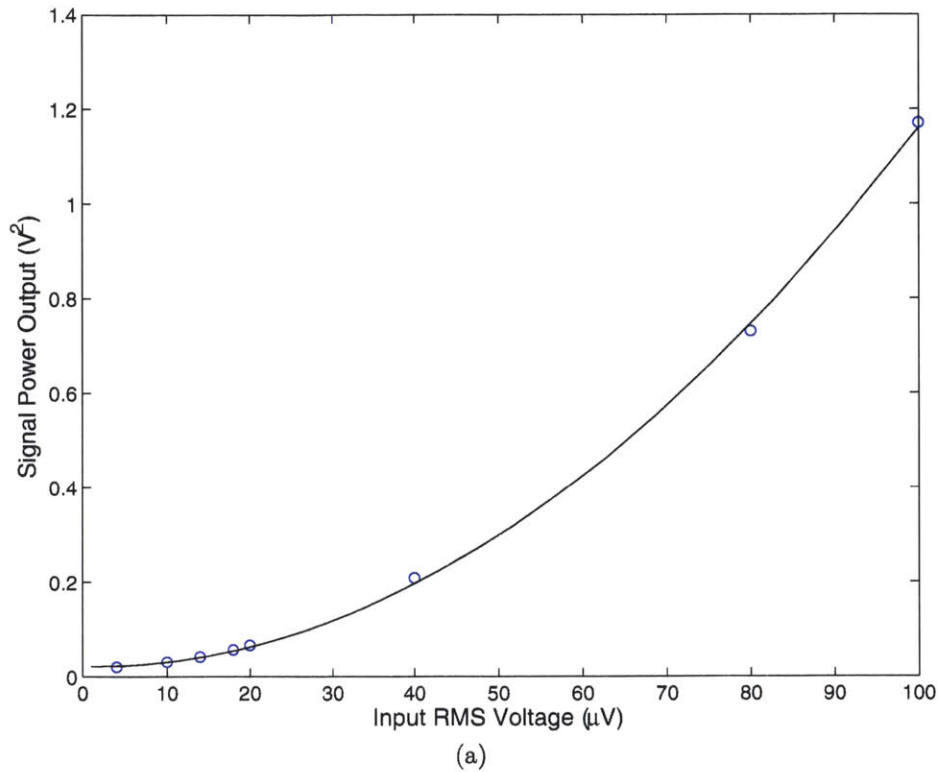


Figure 5-22: (a) Bandpower output from 90 Hz input tone shows the expected parabolic response with a systematic input-referred offset of $1.27 \mu\text{V}$ and voltage gain of 10,800. (b) Bandpower output from 100 Hz tone at two different input bias points; the 2 sec. tone was initiated at the 1 sec. mark. Higher input stage bias current results in higher g_m and hence proportionally lower noise at the power output.

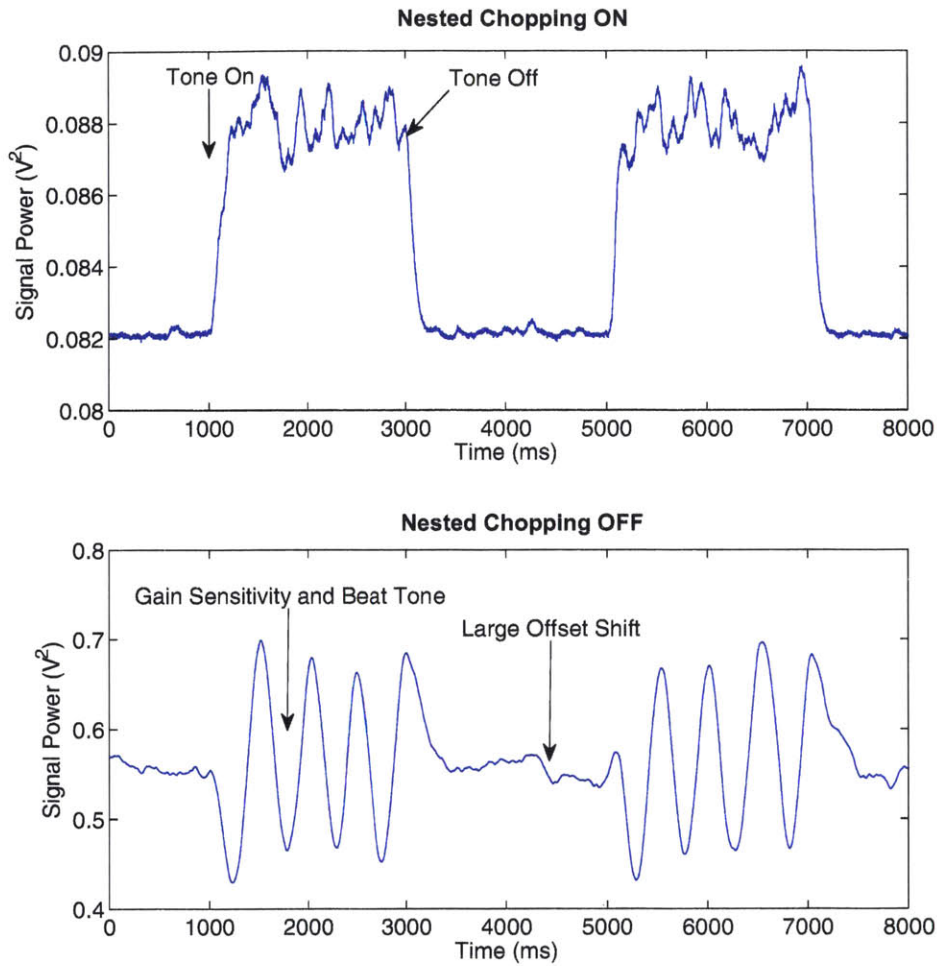


Figure 5-23: Bandpower extraction with and without the benefit of nested chopping—note the severe beat tone as the residual offsets from the heterodyned chopper are superimposed on the small input tone.

Another hindrance to signal resolution is the contamination of the signal chain by supply perturbations and external noise sources. The PSRR was measured to be greater than 80 dB over frequencies that are at risk of mixing into the signal power output. Because the maximum supply perturbation during stimulation was measured to be below 10 mV on our stimulator, the total channel mean square error will be limited by the heterodyning chopper’s thermal noise. The minimal CMRR of 80 dB provides adequate attenuation of common-mode sources like ac powerline noise based on saline tank evaluations discussed in Section IV-C.

5.4.3 Offset Suppression with Nested Chopping

As stated earlier, the resolution of the signal chain can be compromised by residual offsets as opposed to the noise in the circuit. The analog signal chain relies on the nested chopper architecture to ensure that residual offsets from the inner heterodyning chopper do not interfere with the resolution floor. The problem is that the signal from the biomarker is superimposed on this offset, leading to significant beat tones as the signal phase rotates with respect to the on-chip oscillator. Based on results from measuring 22 different channels, our residual offset mean through the entire signal chain was $0.25 \mu\text{V}$, $1 \mu\text{V}$ maximum, statistically ensuring that we could maintain net channel floor on the order of $1 \mu\text{V}_{\text{rms}}$.

To illustrate the critical function of the nested chopper, we disabled it per Figure 5-23. The resulting sensitivity skewing and beat tones clearly undermine the resolution of the signal chain to a pure spectral tone. For a penalty of only four additional switches and a down-sampled clock, we improve the resolvable floor by more than an order of magnitude.

5.4.4 Differential Clock Matching Stability

The performance of the differential clock is critical to the proper operation of the analog signal chain. The finite of the on-chip oscillator beat clock is convolved with the heterodyning chain to form an effective bandpass characteristic.

The maximum differential clock jitter was measured and bounded (4σ) to $\pm 1 \text{ Hz}$ using a total oscillator bias current of 200 nA ; the clock drift was $0.5 \text{ Hz}/^\circ\text{C}$, with a mean of $0.1 \text{ Hz}/^\circ\text{C}$.

To illustrate the clock-matching on the IC, a spectral plot of the beat tone at the output was characterized. The clock on the channel was set to 100 Hz , and a 105 Hz test tone was fed into the channel input, creating a 5 Hz beat tone at the output of the test bus. This signal was buffered and passed to an HP89410A spectrum analyzer. The output of the spectral response, sampled over a 60 minute window, is shown in Figure 5-24. The peak is clearly seen at 5 Hz with signal power down by -20 dB at $\pm 1 \text{ Hz}$. Based on practical algorithm studies, the measured clock tolerance provides acceptable tuning within the normal physiological temperature range ($37 \pm 2^\circ\text{C}$) and ensures that we maintain band tuning with adequate precision.

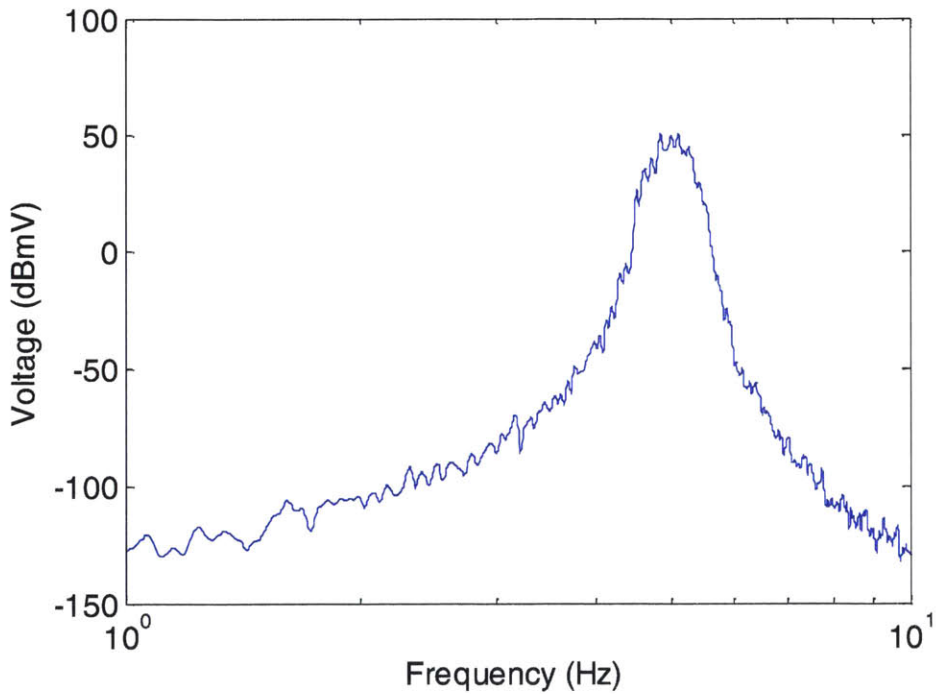


Figure 5-24: Spectral response of a 5 Hz beat tone, using a 100 Hz bandcenter and a 105 Hz tone, shows suitable on-chip clock matching. The tone's -20 dB skirt of ± 1 Hz is adequate for our neural sensing applications, considering this response is convolved with filters of $BW/2$, -3 dB corners >1 Hz.

5.4.5 Closed-Loop Neurostimulator Prototype Results

As discussed in Section I, the design of the NPIC was part of a total system architecture that merges the considerations for biomarker properties, signal processing, and algorithm control for the adaptive control of a neurostimulator. Given the importance of these considerations, the benefits of appropriate system partitioning and sense IC design are best illustrated within the context of the complete closed-loop stimulator prototype.

To illustrate a potentially useful application, our prototype system initiates stimulation upon the detection of a burst of field potential energy in the “ β -band” (15 to 40 Hz), which is indicative of several pathological events as listed in Table II. For the purposes of the demonstration, one channel of the NPIC was programmed to extract the β -band, while another was configured to simply amplify time-domain LFP data for analysis of the bandpower channel.

With reference to Figure 5-25, a recorded signal from a patient data file was fed into a saline tank. LFP signals within the saline were extracted by standard DBS electrodes (Medtronic model 3387) placed across the appropriate electrode vector, with a parallel set of stimulation electrodes placed within 1 cm of the sensing electrode; the stimulation return was provided with a far-field titanium electrode that represents the IPG case. Electrode interconnects were attached to the header block signals shown in Figure 5-4. The salinity of the tank solution was adjusted to mimic the electrical properties of brain tissue.

After amplification and bandpower extraction with the NPIC, the microprocessor sampled the signals at 200 Hz for the time-domain signal, and 5 Hz for the bandpower signal. These data are in Figure 5-26(a) and (b). The microprocessor algorithm ran at 5 Hz, using bandpower processing only. The control algorithm normalizes the mean energy in the last 2 seconds to the median energy over the last 30 minutes (Figure 5-26(c)). When this ratio exceeded a preset threshold for a fixed time span (indicative of a pathological event), a detection flag was passed to the stimulation controller over the I^2C bus, and stimulation at 140 Hz was initiated on the stimulation electrode set (Figure 5-26(d)). Stimulation continued for the duration of elevated β -band energy, to demonstrate the process of stimulating a target based on the detection of a pathological event. The frequency separation between stimulation and LFP biomarker energy allowed us to maintain sensitivity to the LFP even in the presence of stimulation from an electrode only 1 cm away [82]. Note that all data shown in Figure 5-26 was downloaded from the loop-recorder SRAM post-event; although only

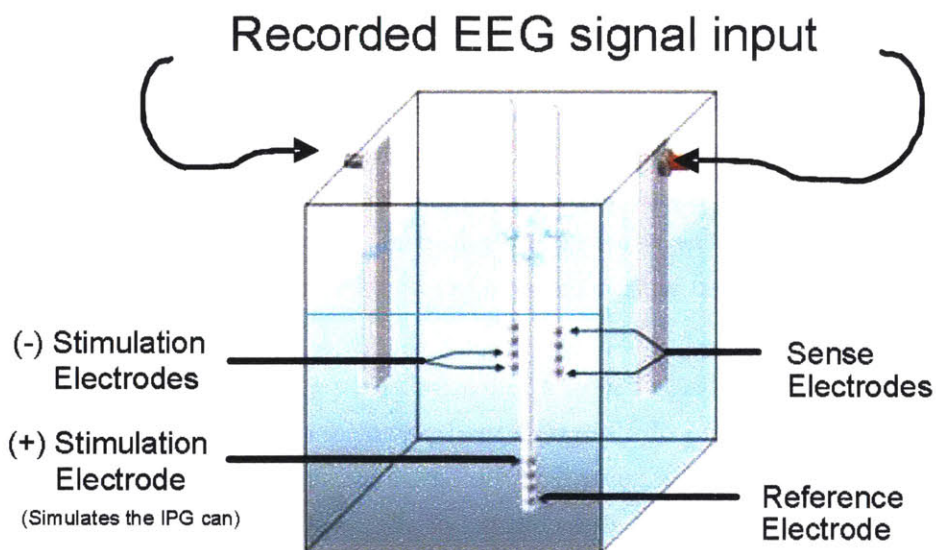


Figure 5-25: Diagram of the saline tank model for evaluating the closed-loop neurostimulator prototype.

two minutes of data are shown, the recorder can store up to 24 hours of spectrogram data in its buffer.

This system demonstration shows that this architecture helps address the major challenges of an adaptive neuromodulation control system described in the introduction. The system is built around the electrical biomarker of band fluctuations, and partitioning the signal chain to extract the relevant signal with a total current draw for both analog sensing and algorithmic processing on the order of $10 \mu\text{W}/\text{channel}$ ($5 \mu\text{W}$ NPIC, $5 \mu\text{W}$ spectrally-based algorithm at 5 Hz), making it practical to implement within a chronic implantable neuromodulation system.

5.5 Discussion

5.5.1 Practical Brain-Machine Interfaces and Closed-Loop Stimulators

The objective of the NPIC is to implement a practical interface to the nervous system for chronic sensing along with adaptive titration or actuation control. In particular, the design of the NPIC was driven by important system considerations: identifying a science-based biomarker that is both useful and robust, building a system around extracting, processing, and recording the biomarker, and finally real-time titration

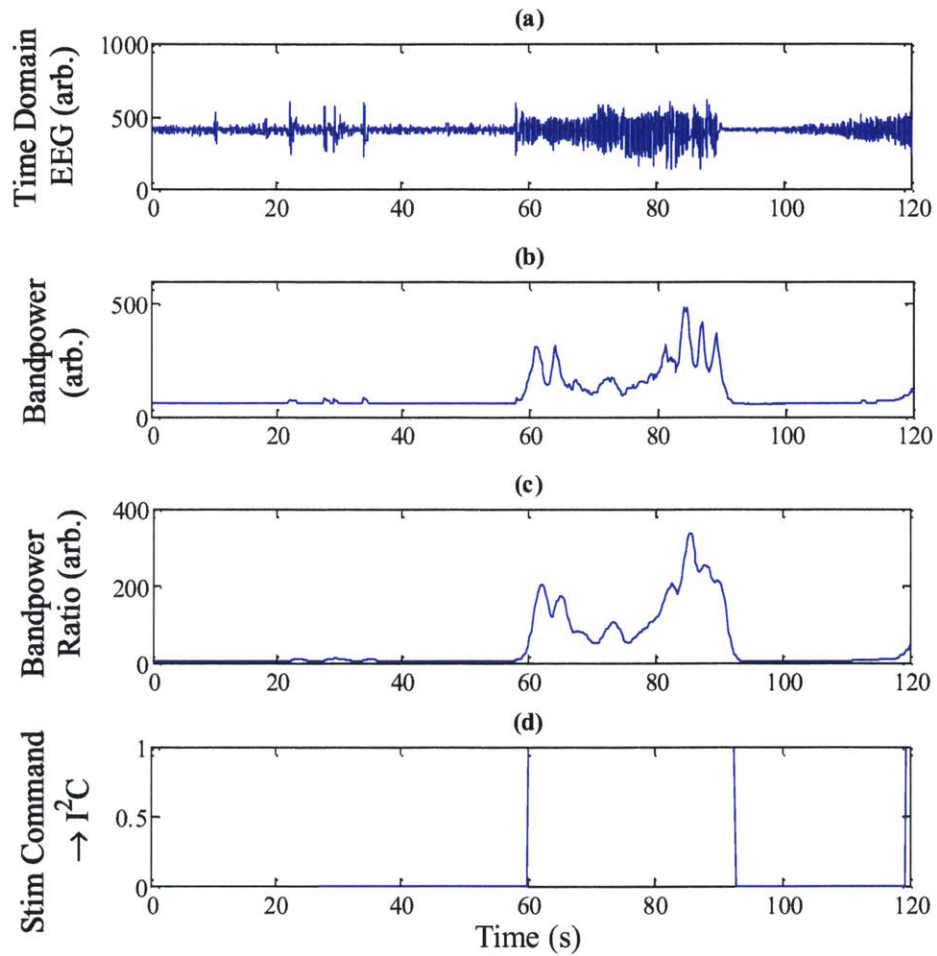


Figure 5-26: Closed loop prototype neurostimulator responding to an extended burst of energy in the β -band ($200 \mu\text{V}_{\text{peak-to-peak}}$) corresponding to a pathological neural event.

of a neurostimulator— all within acceptable power constraints. Although the NPIC is not strictly the most “efficient” design for noise and power, the design choices were selected based on their robustness and appropriate scale for the application. For example, although bandpass filters in subthreshold are achievable for only 5 nW [46], the therapy power itself is five orders of magnitude higher than this level. The power benefits of such a low power design are not outweighed by other considerations, such as device matching and long-term reliability of using bias currents on the order of junction leakage currents. In a similar vein, we have a paramount concern for safety—although this design includes external devices that require extra area when compared to many published motor prostheses, it was engineered to be robust to ESD, single faults, and similar design concerns for long-term reliability. Without these considerations, even the best circuit ideas are at risk of never translating into feasible designs..

Recent publications have discussed similar concepts for closed-loop neurostimulators for DBS. Reference [61] in particular documents both a sensing and stimulation IC, consuming 9 μ W/channel for sensing both action potentials and field potentials, as well as digitizing signals. On the same order of this channel’s total power consumption, the implementation of control with a microprocessor is not discussed, which can easily dominate the system power without prior analog data compression, particularly when analyzing action potentials [47]. Our design considered the implementation and partitioning of the control strategy as part of the definition of the IC to ensure that the impact to total system power was constrained to the order of 10 μ W/channel including full algorithm computation and loop recording. Another advantage of our implementation is that it is built on a proven neurostimulator. This allows us to focus on the issues of sensing and adaptive titration of stimulation for therapy, while avoiding the issues of unproven stimulation efficacy as an additional experimental variable.

5.5.2 Heterodyned Chopping as an Analog Spectral Analysis Technique

In this design, we partitioned the gain and bandpower extraction of field potentials with a heterodyning chopper amplifier. While previous designs have explored the use of continuous-time analog preprocessing for extracting neuronal or equivalent bandpowers [46,87], we chose the heterodyning-chopper architecture for its enhanced tunability and robustness to manufacturing process corners. In particular, this ar-

chitecture provides an independent adjustment of δ and Q over our wide spectrum of biomarkers with parameters well within process tolerances. These parameters can be easily adjusted over broad ranges through microprocessor control. After the bandwidth of the signal is reduced to the order of 1 Hz, using an off-the-shelf microprocessor is now feasible for digitization and flexible algorithmic processing. At these low data-rates, CPU overhead is minimal, while digital signal processing like median filtering along with algorithms and finally loop recording can be achieved for power of the order of $10 \mu\text{W}$.

Another consideration is the required silicon area, which is $5 \text{ mm}^2/\text{channel}$ for our implementation. For a complete micropower analog spectral analyzer, the design is on par with state-of-the-art designs such as that presented in [87,89], which requires a net die area of roughly 88.4 mm^2 to implement a 16-channel “bionic ear processor.” Although not an exact functional comparison—for example, our relative ESD cell penalty is quite large for patient safety—the similarity of the processing shows that our 4-channel design, with an additional gain factor of up to 80 dB through the signal chain, shares a similar area-performance scale. Once again, considering the system perspective, the sensing IC is stacked onto the loop recording SRAM, further reducing the impact of the channel size on the overall footprint of the sensing, control and memory module.

5.5.3 Considerations for a Noise and Power Tradeoff

The noise-power tradeoff of the heterodyning chopper is filter-dependent. By combining amplification and filtering in the heterodyning chopper, a noise tradeoff is inherent in the selection of one side lobe in the demodulation process. A rough derivation in Appendix B shows that for a fixed SNR, the heterodyning chopper amplifier uses less power than an equivalent amplified bandpass filter for a modest $Q \geq \sim 5.58$, reasonably assuming that system noise floor and power is dominated by the front-end amplifier. If the system noise is dominated by the input signal, e.g., for a pre-amplified sensor signal, then the Q requirement is relaxed further, to the order of $Q \geq \sim 2$. Although this is a rough calculation and should not be overly stated, it does help validate the design as a practical solution when the other benefits of the architecture are considered.

It can be argued that an optional use of power would include adaptively biasing the first stage relative to the noise content of the sensed field potentials; this strategy is in the same vein as [90,113], and was employed in this design as well. In particular,

higher bands might require broader bandwidths for dynamically tracking biomarkers. However, these bands might also have smaller amplitudes, requiring better resolution in the presence of greater noise bandwidth. Dynamic biasing is relatively straightforward, since the white noise floor of the signal chain is largely determined by the g_m of the first-stage differential pair, once other issues like $1/f$ noise, offsets and charge injection are resolved with nested, heterodyned chopping. The appropriate sense of optimality is of course dependent on the noise statistics of the field potentials along with the statistical requirements of detection algorithms.

Calculation of SNR Metric for Comparing Narrowbanding Strategies in Signal Power Measurement

From Figure 5-13, the output power is given by

$$Y = X_I^2 + X_Q^2,$$

where $X_I = s_I + n_I$ and $X_Q = s_Q + n_Q$ are the low-pass and hence bandlimited outputs of the in-phase and quadrature choppers, respective. The noise-free and hence deterministic portions are s_I and s_Q ; n_I and n_Q are IID (independent and identically distributed) Gaussian noise variables with zero mean. Note that the squaring of a Gaussian random variable results in a χ^2 distribution.

The definition for signal-to-noise ratio that we choose is given by

$$\text{SNR} = 10 \log \left| \frac{E[y]_{n=0}}{E[Y] - E[y]_{n=0}} \right|,$$

where

$$E[Y] = s_I^2 + s_Q^2 + E[n_I^2] + E[n_Q^2] + 2s_I \underbrace{E[n_I]}_{\text{zero}} + 2s_Q \underbrace{E[n_Q]}_{\text{zero}}$$

is the expectation of Y and $E[Y]_{n=0} = s_I^2 + s_Q^2$ is the value of Y with a noise-free input. Therefore, the SNR is then the output (signal power measurement) with noise free input divided by the expected mean square error in the measurement. Although this relatively coarse metric is achieved by ignoring the second moment of the χ^2 distributions, it provides a basis for comparison among different narrowbanding approaches to signal power extraction.

Given our definition, we can compare the power requirements of a heterodyning chopper with an equivalent amplifier-then-bandpass filter for a fixed SNR; we assume that the power consumption is proportional to the bandwidth of amplification. Be-

cause signals are folded to the baseband in the chopper, the bandwidth is $BW/2$ for the amplification of a single sideband, but a factor of two penalty is incurred for power because both in-phase and quadrature channels are required. In an equivalent bandpass filter system, the bandwidth of the amplifier is $\omega_0 + BW/2$.

The mean square noise for the heterodyning chopper is $E[n^2] = 2e_n^2 (BW/2)$ and $E[n^2] = e_n^2 BW$ for a bandpass filter, where we assume that, the noise densities e_n are equal in all channels. The power per SNR for the chopper is given by

$$\eta_{\text{chop}} = \frac{\text{Power}}{\text{SNR}} = \frac{2 \times (BW/2)}{\frac{(4/\pi^2)^2 V_s^2}{2e_n^2 (BW/2)}}$$

where V_s is the magnitude of the noise-free input and $4/\pi^2$ is the square wave chopping factor derived in §5.2.1. For the amplified bandpass filter,

$$\eta_{\text{BPF}} = \frac{\omega_0 + (BW/2)}{\frac{V_s^2}{e_n^2 BW}}$$

The chopper does better in terms of power consumption than the amplified bandpass filter for $\eta_{\text{chop}} < \eta_{\text{BPF}}$, which is equivalent to

$$\frac{BW}{(4/\pi^2)^2} < \omega_0 + \frac{BW}{2},$$

or for $Q = \omega_0/BW$,

$$\boxed{Q > 5.58}.$$

5.6 Chapter Summary

This chapter discussed the design and results for a prototype IC enabling a bidirectional brain-machine interface for exploring adaptive neuromodulation concepts. The design focuses on efficiently extracting neuronal biomarkers embedded in field potentials using analog preprocessing prior to data conversion and digital processing. The architecture enabled by this IC allows broad “tuning” to a range of biomarkers and provides robustness with modest tradeoffs in noise and area, as well as having the ability to run flexible control algorithms for titration of therapy along with the monitoring of diagnostics. The sensing IC also interfaces to an off-chip SRAM to streamline loop recording of chronic biometric data. With this research tool, researchers can explore advanced neuromodulation therapy strategies based on therapeutically relevant

Chapter 5 : Ultralow Power Neural Sensing for Closed-Loop Stimulation

biomarkers, as well as the fundamental mechanisms by which deep-brain stimulation achieves efficacy.

Chapter 6

Conclusions and Future Work

ENERGY stewardship is vital especially in biomedical devices. The important measures of physical size and device lifetime are critically dependent on how well both power delivery and consumption are managed. The bilateral approach engendered in this thesis of advancing the state of the art in power delivery and consumption culminated in an investigation that spanned of topics from spread-spectrum wireless power transfer to single-sided uniform fields to neural sensing.

6.1 Thesis Summary

Chapter 1 introduces the challenges in power management in medical implants and discusses the bilateral strategy of wireless power transfer and closed-loop therapy through sensing circuits. An overview of the state of the art and conventional solutions are delineated and the restrictions imposed by government regulations in wireless power transfer are explained.

Chapter 2 considers the design, tradeoffs, and optimization of half-sine pulse sequences for spread-spectrum wireless power transfer. Constraints imposed by hardware are also discussed and the construction of custom functions for genetic algorithm optimization are described.

Chapter 3 details the end-to-end hardware design for spread-spectrum wireless power transfer. A treatment on the operation and design of the inverse or current-mode class D amplifier, which leads to a generalization, a *Quad-Switch Push-Pull Amplifier*, which is used to generate power in a manner that is both ‘spread-spectrum and resonant.’ The chapter concludes with the design of a passive bandpass receiver with the capability to accept power in a spread-spectrum system that satisfies the requirements for both biomedical applications and electromagnetic interference regulations.

Chapter 4 investigates the use of uniform single-sided magnetic fields for wireless power delivery. Induction heating is used as the experimental surrogate and a detailed design methodology with a number of new approaches are presented.

Chapter 5 discusses the design of a micropower neural sensing integrated circuit for closed-loop stimulation. This circuit is currently used in deep brain stimulation for the treatment of Parkinson's disease and epilepsy.

6.2 Thesis Conclusions

Technology advancement in power and energy requires end-to-end system solutions with seemingly disparate subject combining to attain or surpass an elusive bourn. This is especially true in biomedical devices where the stakes are consequential. Departures from the conventional approaches were undertaken to extend the capability and flexibility of wireless power transfer, magnetics, and therapy. Concepts from power, control, communications, and circuits were combined or appropriated to devise such ideas as the freezing of states in resonant converters, broader notions of orthogonality, or feedback demodulation.

6.3 Future Work

Some of the work in this thesis can be considered the inception of a number of concepts. The advancement of spread-spectrum wireless power transfer to higher frequencies and the design of a broadband receiver would expand the usefulness of the technology. The embedding of higher bandwidth communication than was previously possible in wireless power transfer is now a potential with spread-spectrum modulation and offers several avenues for study including the power/information tradeoff.

Within power delivery using uniform single-sided magnetic fields, the direct application of orthogonal spread-spectrum drives is a future endeavor as will the design of other magnetic configurations towards the reduction of edge-effects and end-turns.

With neural sensing, methods to expand the notion of demodulation onto a basis set which is essentially sinusoidal in its current incarnation towards arbitrary or even learned sets has applications in information compression at the front end, which provides other options for partitioning power in signal and ultimately information processing.

Concepts for ubiquitous wireless power transfer are especially for medical implant recipients and is illustrated in Figure 6-1, where power is available from different



Figure 6-1: Ubiquitous Wireless Power Transfer

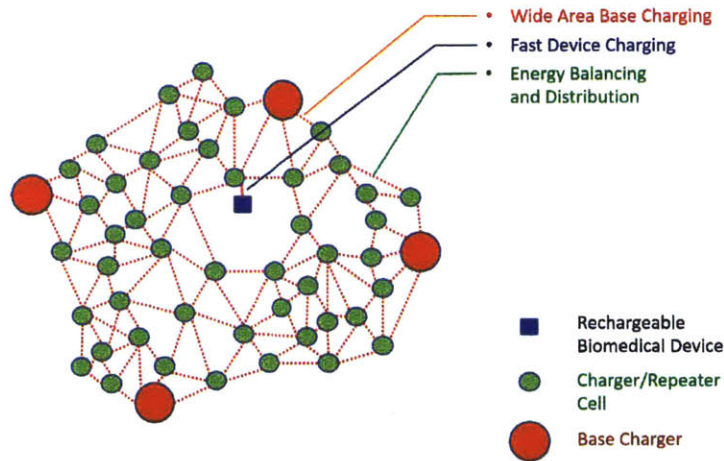


Figure 6-2: Wireless Power Transfer 'Grid'

surfaces. A wireless power transfer 'grid' as conceptually shown in Figure 6-2 is an abstraction of how resources might be distributed in a WPT environment.

Chapter 6 : Conclusions and Future Work

Chapter A
Device Figure of Merit Data

| Part | Vm (pk) | Im (rms) | Csw (pF) | Rds | Ciss (pF) | Qg (pC) | wc | fc (Hz) | PO (W) | Q0 | wP | wPQ | |
|-----------------|---------|----------|----------|----------|-----------|---------|----|----------|----------|----------|----------|----------|----------|
| EPC8004 | 40 | 4.4 | 17 | 0.125 | | 358 | | 1.29E+10 | 2.06E+09 | 79.22765 | 36.36364 | 1.03E+12 | 3.73E+13 |
| | 8007 | 40 | 3.8 | 14 | 0.16 | 302 | | 1.36E+10 | 2.16E+09 | 68.42388 | 32.89474 | 9.29E+11 | 3.05E+13 |
| | 8006 | 40 | 3.1 | 9.5 | 0.25 | 211 | | 1.63E+10 | 2.60E+09 | 55.81948 | 25.80645 | 9.11E+11 | 2.35E+13 |
| | 8008 | 40 | 2.7 | 8 | 0.325 | 177 | | 1.69E+10 | 2.69E+09 | 48.61697 | 22.79202 | 8.20E+11 | 1.87E+13 |
| | 8009 | 65 | 4.1 | 17 | 0.138 | 380 | | 7.42E+09 | 1.18E+09 | 119.9669 | 57.44079 | 8.90E+11 | 5.11E+13 |
| | 8005 | 65 | 2.9 | 9.7 | 0.275 | 218 | | 9.20E+09 | 1.46E+09 | 84.85461 | 40.75235 | 7.81E+11 | 3.18E+13 |
| | 8002 | 65 | 2 | 5.9 | 0.53 | 141 | | 1.04E+10 | 1.66E+09 | 58.52042 | 30.66038 | 6.10E+11 | 1.87E+13 |
| | 8003 | 100 | 2.5 | 18 | 0.3 | 315 | | 2.78E+09 | 4.42E+08 | 112.5393 | 66.66667 | 3.13E+11 | 2.08E+13 |
| EPC2015 | 40 | 33 | 750 | 0.004 | | 3000 | | 2.20E+09 | 3.50E+08 | 594.2074 | 151.5152 | 1.31E+12 | 1.98E+14 |
| | 2815 | 40 | 33 | 750 | 0.004 | 3000 | | 2.20E+09 | 3.50E+08 | 594.2074 | 151.5152 | 1.31E+12 | 1.98E+14 |
| | 2014 | 40 | 10 | 170 | 0.016 | 670 | | 2.94E+09 | 4.68E+08 | 180.0628 | 125 | 5.30E+11 | 6.62E+13 |
| | 2001 | 100 | 25 | 525 | 0.007 | 2300 | | 9.52E+08 | 1.52E+08 | 1125.393 | 285.7143 | 1.07E+12 | 3.06E+14 |
| | 2801 | 100 | 25 | 525 | 0.007 | 2300 | | 9.52E+08 | 1.52E+08 | 1125.393 | 285.7143 | 1.07E+12 | 3.06E+14 |
| | 2016 | 100 | 11 | 280 | 0.016 | 990 | | 7.86E+08 | 1.25E+08 | 495.1728 | 284.0909 | 3.89E+11 | 1.11E+14 |
| | 2207 | 100 | 6 | 140 | 0.03 | 500 | | 8.57E+08 | 1.36E+08 | 270.0943 | 277.7778 | 2.32E+11 | 6.43E+13 |
| | 2018 | 150 | 12 | 350 | 0.025 | 1300 | | 4.57E+08 | 7.28E+07 | 810.2828 | 250 | 3.70E+11 | 9.26E+13 |
| | 2818 | 150 | 12 | 350 | 0.025 | 1300 | | 4.57E+08 | 7.28E+07 | 810.2828 | 250 | 3.70E+11 | 9.26E+13 |
| | 2019 | 200 | 8.5 | 150 | 0.05 | 1800 | | 5.67E+08 | 9.02E+07 | 765.2671 | 235.2941 | 4.34E+11 | 1.02E+14 |
| 2010C | 200 | 22 | 320 | 0.018 | | 3700 | | 6.88E+08 | 1.09E+08 | 1980.691 | 252.5253 | 1.36E+12 | 3.44E+14 |
| | 2010 | 200 | 12 | 350 | 0.025 | 1300 | | 3.43E+08 | 5.46E+07 | 1080.377 | 333.3333 | 3.70E+11 | 1.23E+14 |
| | 2012 | 200 | 3 | 95 | 0.1 | 330 | | 3.16E+08 | 5.03E+07 | 270.0943 | 333.3333 | 8.53E+10 | 2.84E+13 |
| IRF6641 | 200 | 5.5 | 240 | 0.051 | | 34000 | | 2.29E+08 | 3.65E+07 | 495.1728 | 356.5062 | 1.13E+11 | 4.05E+13 |
| Si7462DP | 200 | 3.9 | 100 | 0.142 | | 20000 | | 3.90E+08 | 6.21E+07 | 351.1225 | 180.5706 | 1.37E+11 | 2.47E+13 |
| FDMS2672 | 200 | 3.7 | 125 | 0.088 | | 42000 | | 2.96E+08 | 4.71E+07 | 333.1163 | 307.1253 | 9.86E+10 | 3.03E+13 |
| Pilawa FDV303N | 25 | 0.68 | 28 | 0.45 | | 2300 | | 1.94E+09 | 3.09E+08 | 7.652671 | 40.84967 | 1.49E+10 | 6.07E+11 |
| MRF6S9060 LDMOS | 28 | 2 | 33 | 0.266667 | | 1060 | | 4.33E+09 | 6.89E+08 | 25.2088 | 26.25 | 1.09E+11 | 2.86E+12 |
| MRF6VP21KHR6 | 100 | | 147 | | | | | | | | | | |
| MRF6P24190HR6 | 60 | 2.2 | | 0.136364 | | | | | | | | | |
| Polyfet | | | | | | | | | | | | | |

| | | | | | | | | | | | | |
|------------------------|-----|-----|-----|--------|------|-------|----------|----------|----------|-----------|----------|----------|
| LY942 | 100 | 20 | 230 | 0.2 | | 2400 | 1.74E+09 | 2.77E+08 | 900.3142 | 12.5 | 1.57E+12 | 1.96E+13 |
| LX141 | 100 | 4.5 | 30 | 0.5 | 30 | 7500 | 3.00E+09 | 4.77E+08 | 202.5707 | 22.222222 | 6.08E+11 | 1.35E+13 |
| SX501 VDMOS | 70 | 28 | 230 | 0.12 | 250 | 2500 | 3.48E+09 | 5.54E+08 | 882.3079 | 10.41667 | 3.07E+12 | 3.20E+13 |
| Perreault Warren Paper | | | | | | | | | | | | |
| IRF1902 | 20 | 4 | 190 | 0.085 | 480 | 7500 | 2.11E+09 | 3.35E+08 | 36.01257 | 29.41176 | 7.58E+10 | 2.23E+12 |
| Si4346DY | 30 | 7.5 | 175 | 0.025 | 1100 | 6500 | 2.86E+09 | 4.55E+08 | 101.2853 | 80 | 2.89E+11 | 2.32E+13 |
| FDN361AN | 30 | 1.8 | 60 | 0.15 | 280 | 4000 | 2.00E+09 | 3.18E+08 | 24.30848 | 55.55556 | 4.86E+10 | 2.70E+12 |
| Si4940 | 40 | 4.4 | 150 | 0.059 | 550 | 4500 | 1.47E+09 | 2.33E+08 | 79.22765 | 77.0416 | 1.16E+11 | 8.95E+12 |
| Si4940 | 40 | 5.7 | 150 | 0.036 | 550 | 14000 | 1.90E+09 | 3.02E+08 | 102.6358 | 97.46589 | 1.95E+11 | 1.90E+13 |
| IRFL014N | 55 | 2.7 | 100 | 0.16 | 290 | 11000 | 9.82E+08 | 1.56E+08 | 66.84833 | 63.65741 | 6.56E+10 | 4.18E+12 |
| IRFZ24NS | 55 | 17 | 190 | 0.07 | 560 | 20000 | 3.25E+09 | 5.18E+08 | 420.8969 | 23.10924 | 1.37E+12 | 3.16E+13 |
| FDS5672 | 60 | 10 | 500 | 0.012 | 2900 | 22500 | 6.67E+08 | 1.06E+08 | 270.0943 | 250 | 1.80E+11 | 4.50E+13 |
| FDS5672 | 60 | 12 | 500 | 0.0088 | 2900 | 45000 | 8.00E+08 | 1.27E+08 | 324.1131 | 284.0909 | 2.59E+11 | 7.37E+13 |
| PD57060 | 65 | 7 | 65 | 0.233 | 190 | 1900 | 3.31E+09 | 5.27E+08 | 204.8215 | 19.92643 | 6.79E+11 | 1.35E+13 |
| DE150-201N09A | 200 | 15 | 190 | 0.2 | 1200 | 39000 | 7.89E+08 | 1.26E+08 | 1350.471 | 33.33333 | 1.07E+12 | 3.55E+13 |
| ARF449A | 450 | 5 | 95 | 0.8 | 1100 | 11000 | 2.34E+08 | 3.72E+07 | 1012.853 | 56.25 | 2.37E+11 | 1.33E+13 |
| ARF521 | 500 | 8 | 85 | 0.56 | 1000 | 10000 | 3.76E+08 | 5.99E+07 | 1800.628 | 55.80357 | 6.78E+11 | 3.78E+13 |

Chapter A : Device Figure of Merit Data

Chapter B

Verilog Code for Digital Controller

B.1 Xilinx Device Information

Spartan 6 FPGA Device: XC6SLX16 Package: FTG256 Speed: -2
Synthesis Tool: XST (Verilog)
Development Environment: Xilinx ISE ver. 14.7

B.2 Top Level

```
1 //  
  → //////////////////////////////////////  
  →  
  // Company: MIT  
3 // Engineer: Al Thaddeus Avestruz  
  //  
5 // Create Date:      18:03:17 01/28/2011  
  // Design Name:  
7 // Module Name:     TOP_SSRC_Controller  
  // Project Name:          Spread Spectrum Resonant Charging  
9 // Target Devices:  
  // Tool versions:  
11 // Description:  
  //  
13 // Dependencies:  
  //
```

Chapter B : Verilog Code for Digital Controller

```
15 // Revision :
    // Revision 0.01   File Created
17 // Revision 2.00   Added okHost functionality
    // Revision 3.00   Migrated from Test11; cycloconverter update
    ↪ 12 8 12
19 //       Revision 4.00   ISE 14.4
    // Revision 5.00   Add bit sequence RAM functionality
21 //       Revision 6.00   Variable zero duration functionality
    //
23 // Additional Comments:
    // ISE 14.4 CoreGen Workaround set env XIL_CG_LOAD_ALL_FAMILIES=
    ↪ True
25 // ISE 14.7
    // 9 29 2014 Fixed error in data_ready in Slow2Fast() module.
27 //                               Added ~update_sbuf to
    ↪ buffer state machine to prevent lock up on missing
    ↪ data_ready.
    // 12 5 2014 Reverse switches 3&4 on XBUS gate drive for board
    ↪ CPP ICDv2.1
29 //
    //
    ↪ //////////////////////////////////////
    ↪
31 module TOP_SSRC_Controller(
    input wire clk1, //PLL Clock 1
33    input wire clk2, //PLL Clock 2
    input wire [3:0] button,
35
    output wire [13:0] zbus,
37    output wire [35:1] ybus,
    output wire [35:0] xbus,
39
    //LEDs
    output wire [7:0] led,
43
    //OK Host
45    input wire [7:0] hi_in,
```



```

47     output wire [1:0] hi_out ,
        inout wire [15:0] hi_inout ,

49     output wire          hi_muxsel

51 );

53

55

57 //
    ↪ *****
    ↪
// PARAMETER DEFINITIONS
59 //
    ↪ *****
    ↪

61 //parameter CLK_IN_FREQ          = 150_0;          //MHz
    //parameter E_FREQUENCY        = 10_0;           //MHz
63 //parameter E_DUTY              = 50;
    ↪ //
    //parameter SEQ_LENGTH         = 16'd15;
    ↪ //4096 bits max
65 parameter CLOCK_DIV              = 8;
    parameter ECMPR1                = 16'd4;
67 parameter ECMPR2                = 16'd10;
    ↪ //16'd2 == 37.5 MHz w 150 MHz main clk
    //parameter SEQ_LENGTH         = 15'd7; // actually ,
    ↪ last address of the sequence
69 //parameter SEQ_LENGTH         = 15'd2047; // actually ,
    ↪ last address of the sequence (16 bits for 16 bit counter)
    parameter SEQ_LENGTH           = 16'd2047; // actually ,
    ↪ last address of the sequence bitstream2.coe
71 //parameter SEQ_LENGTH         = 16'd3; // actually ,
    ↪ last address of the sequence bitstream2.coe
    //parameter SEQ_LENGTH         = 15'd510; // actually ,

```

Chapter B : Verilog Code for Digital Controller

```
    ↪ last address of the sequence bitstream2.coe
73 //parameter SEQ_LENGTH          = 15'd15; // actually ,
    ↪ last address of the sequence bitstream1.coe

75 parameter DEBOUNCE_DELAY      = {1'b0,{23{1'b1}}};
    //parameter DEBOUNCE_DELAY    = 24'd100; //Shorter Delay for
    ↪ the purposes of simulation
77
    //defparam
79 //      Debounce_Button.dbutton1.DELAY = 100,
    //      Debounce_Button.dbutton2.DELAY = 100,
81 //      Debounce_Button.dbutton3.DELAY = 100,
    //      Debounce_Button.dbutton4.DELAY = 100;
83

85 //
    ↪ *****
    ↪
    // REG DECLARATIONS
87 //
    ↪ *****
    ↪

89
    //
    ↪ *****
    ↪

91 // WIRE DECLARATIONS
    //
    ↪ *****
    ↪

93
    // Input Buffers
95 wire button1;
    wire button2;
97 wire button3;
    wire button4;
99
```

```

101     wire [13:10] zbus_i;

103 // Output Buffers
     wire [7:0] led_o;
105 wire zclk1_o;
     wire zclk2_o;

107
     wire [13:0] zbus_o;
109 wire [35:1] ybus_o;
     wire [35:0] xbus_o;

111

113 // ROM
     wire [13:0] qdoutROM;
115 wire [12:0] addrROM;

117 // Switch Signals
     wire [3:0] switches_1;
119 wire [3:0] switches_2;

121
     // Fault Signals

123

125
     /* INSTANTIATE INPUT AND OUTPUT BUFFERS */

127
     'include "I_O_Buffers.v"

129

131 //
     ↪ *****
     ↪
     // Constants
133 //
     ↪ *****
     ↪

```

Chapter B : Verilog Code for Digital Controller

```
135 //
    ↳ *****
    ↳
137 // CODE
    ↳ *****
    ↳
139 //Master Clock
141 //
    ↳
    ↳
// "Output Output Phase Duty Pk to Pk
    ↳ Phase "
143 // "Clock Freq (MHz) (degrees) Cycle (%) Jitter (ps) Error (
    ↳ ps) "
//
    ↳
    ↳
145 // CLK_OUT1__100.000__0.000__50.0__185.872__160
    ↳ .159
// CLK_OUT2__200.000__0.000__50.0__163.074__160
    ↳ .159
147 // CLK_OUT3__333.333__0.000__50.0__149.456__160
    ↳ .159
// CLK_OUT4__333.333__0.000__50.0__149.456__160
    ↳ .159
149 // CLK_OUT5__333.333__90.000__50.0__149.456__160
    ↳ .159
// CLK_OUT6__250.000__0.000__50.0__156.946__160
    ↳ .159
151 //
//
    ↳
    ↳
153 // "Input Clock Freq (MHz) Input Jitter (UI)"
```

```

//
    ↪
    ↪
155 // __primary_____100.000_____0.025

157 wire rst_mclk;
    wire mclk_locked;
159 assign rst_mclk = 0;

161 wire clk250I;
    wire clk250Q;
163 wire clk250X;

165 //Clock Assignment
    ↪ *****

    assign clk_fast = clk300;
167 assign clk_slow = clk200;
    assign clk_slow_slow = clk100;

169

171 MasterClock masterClock
    (// Clock in ports
173     .CLK_IN1(clk1),      // IN
    // Clock out ports
175     .CLK_OUT1(clk100),  // OUT
     .CLK_OUT2(clk200),  // OUT
177     .CLK_OUT3(clk300),  // OUT
     .CLK_OUT4(clk250I),  // OUT
179     .CLK_OUT5(clk250Q),  // OUT
     .CLK_OUT6(clk250X),  // OUT
181     // Status and control signals
     .RESET(rst_mclk), // IN
183     .LOCKED(mclk_locked)); // OUT

185

187 // Clk Debug
    reg rclk100 = 0;

```

Chapter B : Verilog Code for Digital Controller

```
189 reg rclk200 = 0;
    reg rclk300 = 0;
191 reg rclk250I = 0;

193 always @(posedge clk100) rclk100 <= ~rclk100;
    always @(posedge clk200) rclk200 <= ~rclk200;
195 always @(posedge clk300) rclk300 <= ~rclk300;
    always @(posedge clk250I) rclk250I <= ~rclk250I;
197

199 assign zbus_o[10] = rclk100;
    assign zbus_o[11] = rclk200;
201 assign zbus_o[12] = rclk300;
    assign zbus_o[13] = rclk250I;
203

205
    //Startup Procedure
    ↪ *****
    ↪

207
    StartUp MasterStartup (
209     .clk(clk_fast),
        .clk_ready(mclk_locked),
211     .rst_in(~mclk_locked),
        .rst_out(master_reset)
213     );

215 //Master Reset to Slow Domain
    ↪ *****
    ↪

    wire out_master_reset_slow;
217 reg master_reset_slow = 0;
    reg master_reset_ff = 0;
219 always@(posedge clk_fast) master_reset_ff <= master_reset;

221 Signal_CrossDomain master_reset2slow (
        .clkA(clk_fast),
```

```

223     .SignalIn(master_reset_ff),
        .clkB(clk_slow),
225     .SignalOut(out_master_reset_slow)
        );
227

229 always@(posedge clk_slow) master_reset_slow <=
        ↪ out_master_reset_slow;

231
    assign zbus_o[9:8] = 0;
233

235 //Debounce Buttons    Active Low
    Debounce_Button #(DEBOUNCE_DELAY) dbutton1 (
237     .clk(clk_slow_slow),
        .PB(button1),
239     .PB_state(button1_state),
        .PB_up(button1_up),
241     .PB_down(button1_down)
        );
243 Debounce_Button #(DEBOUNCE_DELAY) dbutton2 (
        .clk(clk_slow_slow),
245     .PB(button2),
        .PB_state(button2_state),
247     .PB_up(button2_up),
        .PB_down(button2_down)
249     );
    Debounce_Button #(DEBOUNCE_DELAY) dbutton3 (
251     .clk(clk_slow_slow),
        .PB(button3),
253     .PB_state(button3_state),
        .PB_up(button3_up),
255     .PB_down(button3_down)
        );
257 Debounce_Button #(DEBOUNCE_DELAY) dbutton4 (
        .clk(clk_slow_slow),
259     .PB(button4),

```

Chapter B : Verilog Code for Digital Controller

```
        .PB_state(button4_state),
261    .PB_up(button4_up),
        .PB_down(button4_down)
263    );

265
    // Instantiate ROM
267
    wire incROM;
269 wire rstROM; //To do: Test set rst = 0; Normal should be = 1
    wire [13:0] qdout_slow;
271 wire ROM_data_ready;
    wire SEQ_start;
273 wire SEQ_start_signal;

275
    ROM_stream2 #(.SEQ_LEN(SEQ_LENGTH)) ROM_bit_stream (
277    .clk_fast(clk_fast),
        .clk_slow(clk_slow),
279    .incr(incROMROM),
        .rst(rstROM),
281    .addrout(addrROM),
        .qdout(qdoutROM),
283    .qdout_slow(qdout_slow),
        .data_ready(ROM_data_ready),
285    .seq_start(SEQ_start)
    );

287

289 // ***** Switching Controller *****

291 wire cyclo_clk;
    wire dready_timeout;
293
    assign cyclo_clk = clk_fast;
295
    SpreadSwitchingOne SwitchingController (
297    .clk(cyclo_clk),
```



```

        .reset (rstCyclo) ,
299     .pzd_word (qdoutROM) ,
        .seq_start_flag (SEQ_start) ,
301     .data_ready (ROM_data_ready) ,
        .shutdown (0) ,
303     .incROM (incROMcyclo) ,
        .switches (switches_1) ,
305     .fault (cyclo_fault) ,
        .signal_data_ready_timeout (dready_timeout) ,
307     .seq_start_signal (SEQ_start_signal)
    );
309

311
    /*
    ↪ *****
    ↪ */
313
    // Assign External Ports
315
    /*
    ↪ *****
    ↪ */
317
    // SEQ_Start Signals Start of Sequence
319 assign ybus_o[2] = SEQ_start; // This
    ↪ signal is out of the ROM

321 // SEQ_Start pipeline
    //reg delayed_SEQ_start_signal=0;
323 //always @(cyclo_clk) delayed_SEQ_start_signal <=
    ↪ SEQ_start_signal;

325 assign ybus_o[4] = SEQ_start_signal; // This signal is out of
    ↪ the switch state machine
assign ybus_o[13] = SEQ_start_signal; // Ports and signals need
    ↪ to be physically next to each other to route together and
    ↪ maintain timing

```

Chapter B : Verilog Code for Digital Controller

```
327 assign xbus_o[29:25] = 0;
    //assign xbus_o[25]= 0;
329
    assign zbus_o[3:0] = switches_1;
331 assign zbus_o[6] = 0;

333 // Diagnostic Ports

335
    assign ybus_o[32] = 0;
        ↪ // Ground
337 assign ybus_o[33] = 0;
        ↪ // Ground

339 // Gate Drive Signals
    assign xbus_o[35] = switches_1[2]; //Reverse
        ↪ switches 3&4 12 5 2014
341 assign xbus_o[34] = switches_1[3];
    assign xbus_o[33] = switches_1[1];
343 assign xbus_o[32] = switches_1[0];

345 assign xbus_o[5:0] = cyclo_fault; //6 bits // 1 State Machine
        ↪ Fault 2 Memory Fault 4 Buffer Fault 8 Buffer State
        ↪ Machine Fault 16 RW_FAULT 32 Fault Aggregate
    assign xbus_o[17:6] = addrROM[11:0]; //12 bits
347 assign xbus_o[20:18] = qdoutROMreg;

349 always @(posedge cyclo_clk) qdoutROMreg <= qdoutROM;

351
    // External Inputs
        ↪ //////////////////////////////////////
        ↪

353

355
    // External Outputs
        ↪ //////////////////////////////////////
```

```

    ↪
357 // Zbus

359 reg [2:0] qdoutROMreg = 0;

361
    // External Event Handling
363
    wire full_f2leds;
365 wire empty_f2leds;
    wire [7:0] led_ss;
367 wire [7:0] led_slow;
    wire [4:0] addrROM_ss;
369 wire [2:0] qdoutROM_ss;

371 SyncFIFO_8bits slow2leds (
    .rst(master_reset_slow), // input rst
373 .wr_clk(clk_slow), // input wr_clk
    .rd_clk(clk_slow_slow), // input rd_clk
375 .din(led_slow), // input [7 : 0] din
    .wr_en(1'b1), // input wr_en
377 .rd_en(1'b1), // input rd_en
    .dout(led_ss), // output [7 : 0] dout
379 .full(full_f2leds), // output full
    .empty(empty_f2leds) // output empty
381 );

383 assign {addrROM_ss[4:0], qdoutROM_ss} = led_ss;
    assign led_slow = {addrROM[4:0], qdout_slow};
385
    assign led_o[2:0] = ~qdoutROM_ss;
387 assign led_o[7:3] = ~addrROM_ss[4:0];

389 //Buttons

391 wire full_ss2f;
    wire empty_ss2f;
393 wire [3:0] fst_start_signals;

```

Chapter B : Verilog Code for Digital Controller

```
    wire [3:0] ss_start_signals;
395 reg master_reset_ss = 1;

397 SyncFIFO_4bits_simple Slow_slow2Fast (
    .rst(master_reset_ss), // input rst
399 .wr_clk(clk_slow_slow), // input wr_clk
    .rd_clk(cyclo_clk), // input rd_clk
401 .din(ss_start_signals), // input [3 : 0] din
    .wr_en(1'b1), // input wr_en
403 .rd_en(1'b1), // input rd_en
    .dout(fst_start_signals), // output [3 : 0] dout
405 .full(full_ss2f), // output full
    .empty(empty_ss2f) // output empty
407 );

409 reg rstROM_ss, rstCyclo_ss, EclkEN_ss, incROM_ss = 0;

411 assign {rstROM, rstCyclo} = ~fst_start_signals[3:2]; //Default
    ↪ startup of FIFO is zero. This makes sure rst is high during
    ↪ startup.
    assign {EclkEN, incROM} = fst_start_signals[1:0];
413 assign ss_start_signals =      {~rstROM_ss, ~rstCyclo_ss,
    ↪ EclkEN_ss, incROM_ss};

415 //Master Reset to Slow Slow Domain
    ↪ *****
    ↪
    Signal_CrossDomain master_reset2ss (
417 .clkA(cyclo_clk),
    .SignalIn(master_reset),
419 .clkB(clk_slow_slow),
    .SignalOut(out_master_reset_ss)
421 );

423
    always@(posedge clk_slow_slow) master_reset_ss <=
    ↪ out_master_reset_ss;
425
```

```

//
↳ *****
↳
427 //Debug pins
429
always@(posedge clk_slow_slow) //Button priorities and startup
↳ sequence **Button has a long debounce period * To do:
↳ defparam the debounce period for debug
431   begin
           incROM_ss <= 0; //Temp placeholder if wanted to
           ↳ externally increment ROM
433   if (master_reset_ss == 1)
           begin
435               rstROM_ss <= 1;
               rstCyclo_ss <= 1;
437               EclkEN_ss <= 0; //To do: Add
               ↳ EclkEN timer
           end
439   else if (button1_down) EclkEN_ss <= ~EclkEN_ss;
           ↳ //Toggle Eclk On/Off
   else if (button2_state) //Resets ROM
441       begin
               rstROM_ss <= 1;
443               rstCyclo_ss <= 1;
               EclkEN_ss <= 0;
445       end
   else if (button3_down) //Converter turn on
           ↳ sequence
447       begin
               rstROM_ss <= 0;
449               rstCyclo_ss <= 0;
               EclkEN_ss <= 1;
451       end
   else if (button4_down) //Reset Cycloconverter
           ↳ State Machine
453       begin
               rstROM_ss <= 1; //Active high

```

Chapter B : Verilog Code for Digital Controller

```
455             rstCyclo_ss <= 1; //Active high
              EclkEN_ss <= 1;
457             end
459         end
461
463 //Gate Modules with External Events
      assign incROMROM = incROM | incROMcyclo; //Increment ROM from
          ↪ cycloconverter or external event
465
      assign ybus_o[1] = incROMROM;
467 assign ybus_o[3] = 0;
      assign ybus_o[16:14] = 0;
469 assign ybus_o[12:5] = 0;
      assign ybus_o[25:17] = 0;
471
473
      /* Test Waveform Generators */
475
477 'include "Test_Waveform_Generators.v"
479
481 /* OK Communications */
483 // Instantiate OK Host and Endpoints
      // USB2.0 interface requires a clock speed of 48 MHz (20.83 ns
          ↪ clock period)
485
      'include "Ok_Comms.v"
487
489
      'include "Reference_Code.v"
```

491 ///
endmodule

B.3 Sequence Memory

```
1 //
  ↪ //////////////////////////////////////
  ↪
  // Company: MIT
3 // Engineer: Al Thaddeus Avestruz
  //
5 // Create Date:    19:35:47 02/15/2011
  // Design Name:
7 // Module Name:    ROM_stream
  // Project Name:
9 // Target Devices:
  // Tool versions:
11 // Description: Simplified ROM machine
  //
13 // Dependencies:
  //
15 // Revision:
  // Revision 0.01   File Created
17 // Additional Comments:
  // 1.29.2014   Modified to 14 bits , and data_ready added.
19 // 1.30.2014   Behavior sim checks okay
  //      10.8.2014   Added seq_start
21 //      12.3.2014   Removed unnecessary latencies   incROM >
  ↪ data_ready     9 fast_clk pulses
  //
23 //
  ↪ //////////////////////////////////////
  ↪
module ROM_stream2 #(parameter SEQ_LEN = 16'd1023)(
25   input wire clk_fast ,
       input wire clk_slow ,
27   input wire incr ,           // fast domain
       input wire rst ,
29
       output [12:0] addrout , //clk_slow domain,
31   output [13:0] qdout , // clk_fast domain
```



```

    output [13:0] qdout_slow, //clk_slow domain
33    output data_ready, //clk_fast domain
    output seq_start      // signal seq start
        ↪ // Used in debug pin
35    );

37 //
    ↪ *****
    ↪
    // PARAMETER DEFINITIONS
39 //
    ↪ *****
    ↪

41 //
    ↪ *****
    ↪

43 // REG DECLARATIONS
    //
    ↪ *****
    ↪

45 //ROM
47 reg clkROM1 = 0;
    reg clkROM2 = 0;
49 reg clkROM3 = 0;
    reg [12:0] addrROM = 0;
51 reg [12:0] addrROM0 = 0;
    //reg clkROM;
53 //reg [1:0] incr_state;
    //reg sclr = 0;
55 //reg [15:0] addrROMcnt;
    reg RstROM = 0;
57 reg incr0 = 0;
    reg incr1 = 0;
59
    reg [13:0] qdout_s = 0;

```

Chapter B : Verilog Code for Digital Controller

```
61 reg seq_start0 = 0;

63
    //Counters
65 //reg clrROMcnt;

67

69 //
    ↪ *****
    ↪
    // WIRE DECLARATIONS
71 //
    ↪ *****
    ↪

73 //ROM
    //wire RstROM;
75 wire clkROM;
    wire [13:0] qdout0;
77
    wire [12:0] addrout_s;
79
    //Counters
81 //wire [11:0] addrROM;
    wire [15:0] addrROMcnt;
83 //wire updateRomClock;
    wire updateROM;
85
    //
    ↪ *****
    ↪
87 // Constants
    //
    ↪ *****
    ↪
89 initial
    begin
```

Section B.3 : Sequence Memory

```
91 //      seq_length <= 15; //Sequence_Length  1;  Maximum
      ↪ sequence length 8192
      //      seq_length <= 15; //Sequence_Length  1;  Maximum
      ↪ sequence length 4096 for hotROM
93 //      RstROM = 0;
      //      clkROM = 0;
95 //      addrROMcnt = 0; //initialize ROM address

97 //      incr_state = 0;
      //      qdout = 0;
99 //      RstROM = 0;
end
101 //
      ↪ *****
      ↪
103 //  CODE
      //
      ↪ *****
      ↪
105
assign seq_start = seq_start0; // Signal Start of Sequence
107
wire incr_pulse;
109
reg incr_ff = 0; //Pipeline Clock Increment
111

113 // Send the incr pulse as a level from fast to slow domain.  And
      ↪ then construct
      // the rising edge pulse in the slow domain.
115
reg incr_slow=0;
117 (* ASYNC_REG="TRUE" *) reg [1:0] sreg;
      always @(posedge clk_slow) begin
119     incr_slow <= sreg[1];
        sreg <= {sreg[0], incr};
121 end
```

Chapter B : Verilog Code for Digital Controller

```
123 reg rst_delayed = 1'b1;
125 multi_cycl_oneshot Reset_ROM_Fast (
127     .clk(clk_fast),
        .signal(rst),
129     .rst(rst),
        .pulse(out_rst_delayed)
131 );

133 always@(posedge clk_fast) rst_delayed <= out_rst_delayed;

135 async_input_sync Reset_Slow (
        .clk(clk_slow),
137     .async_in(rst_delayed),
        .sync_out(rst_s)
139 );

141 //Slow Clock Domain
    ↪ *****
    ↪
143 rising_edge_detect Increment_ROM_Slow (
145     .clk(clk_slow),
        .signal(incr_slow),
147     .rst(rst_s),
        .pulse(clkROM_s)
149 );

151 reg incr_s = 0;
    always @(posedge clk_slow) incr_s <= incr_slow;
153
    //Synchronize Input to Fast Clock Domain
155 //Data Out Synchronizer

157 reg update_transfer_slow = 0;
```

```

159 Slow2Fast_14bits Slow2Fast_Data (
    .rst_fast(rst),
161   .clk_slow(clk_slow),
    .clk_fast(clk_fast),
163   .din(qdout_s),
        .update_slow(update_transfer_slow),
165   .dout(qdout),
    .data_ready(data_ready)
167   );

169
    assign qdout_slow = qdout_s;
171
    always @(posedge clk_slow) update_transfer_slow <= clkROM3;
        ↪           // 12 3 2014
173

175 //Instantiate ROM

177 ROM_14bit_8192 seq_data_ROM (
    .clka(clk_slow), // input clka
179   .rsta(rst_s), // input rsta
    .regcea(updateROM), // input regcea
181   .addra(addrROM0), // input [12 : 0] addra
    .douta(qdout0) // output [13 : 0] douta
183 );

185

187

189 //////////////////////////////////////////////////////////////////// Need
        ↪ a glitch free counter and comparator
    //16 bit counter steps ROM from external event
191

193 counter_16bit_noreg cntrROMaddr (

```

Chapter B : Verilog Code for Digital Controller

```
    .clk(clk_slow), // input clk
195  .ce(clkROM3), // input ce
    .sclr(RstROM), // input sclr
197  .q(addrROMcnt) // output [15 : 0] q
    );
199

201  always @(posedge clk_slow)
        begin
203            if (addrROM == 0) seq_start0 <= 1;
                ↪ // Signal Beginning of Sequence
            else seq_start0 <= 0;
205        end

207 //Update ROM
    //assign addrROM[11:0] = addrROMcnt[11:0];
209
    //assign addrout_s[11:0] = addrROM[11:0];
211
    assign addrout[12:0] = addrROM[12:0]; //clk_slow domain to
        ↪ output
213 //assign addrout[15:12] = 0;

215

217 always @(posedge clk_slow) addrROM0[12:0] <= addrROMcnt[12:0]; //
        ↪ Register the output of counter / only use 12 bits

219 //Pipeline ROM Output
    always @(posedge clk_slow) qdout_s <= qdout0; //Extra output
        ↪ register
221 always @(posedge clk_slow)
        begin
223            if (updateROM == 1)
                begin
225                    addrROM <= addrROM0;
                end
            end
227        end
```

```

229 //One shot no delay
231 always @(posedge clk_slow)
        begin
233         clkROM3 <= clkROM_s; // 12 3 2014
        end
235
237 //Clock ROM Output buffer
        always @(posedge clk_slow)
239         begin
                incr0 <= ~incr_s;
241         end
243
        assign updateROM = clkROM_s; // 12 3 2014 saves one cycle
245
247 reg rst0 = 0;
        reg rst1 = 0;
249 always @(posedge clk_slow)
        begin
251         if (rst_s == 1) RstROM <= 1;
                else if (clkROM_s == 1) RstROM <= rst1;
253         if
                (addrROMcnt > (SEQ_LEN 16'd1)) rst0 <=
                ↪ 1;
255         else
                if ((clkROM_s == 1) && rst0 == 1)
257                 begin
                        RstROM <= 0;
259                         rst0 <= 0;
                end
                rst1 <= rst0;
261         end
263

```

Chapter B : Verilog Code for Digital Controller

265

////////////////////////////////////

267 endmodule

B.4 Controller State Machine

```

1 //
  ↪ //////////////////////////////////////
  ↪
// Company:
3 // Engineer:
  //
5 // Create Date:    14:06:59 01/21/2014
  // Design Name:    Inverse Class D Spread Spectrum
  ↪ Controller
7 // Module Name:    SpreadSwitchingOne
  // Project Name:    Spread Spectrum Wireless Power
9 // Target Devices:    Spartan 6
  // Tool versions:    ISE 4.7
11 // Description:
  //
13 // Dependencies:
  //
15 // Revision:
  // Revision 0.01    File Created
17 // Additional Comments:
  // To do:    Correct minimum zero duration
19 // To do:    Correct de synchronization of data update and switch
  ↪ update    use separate read and write index;
  //
  ↪ increase buffer depth and pre
  ↪ load more data.    There is a state transition latency
  ↪ ambiguity.
21 //    9 27 2014 Fixed the bug in switch polarities
  //    12 2 2014 Note:    Set MIN_POLARITY_DURATION
23 //    12 3 2014 Modified ROM_stream2.v to remove unnecessary
  ↪ latencies    update_sbuf_pulse > data_ready = 14 fast_clk
  ↪ pulses
  //    6 12 2015 Removed extra register after zd_timeout
25 //    6 12 2015 Moved the start zd_counting<= 0 (i.e. disable zd
  ↪ counting) to ALL_ON state exit
  //    6 12 2015 Removed 1 zd offset.
27 //    6 12 2015 Appended Sequence Start Flag to symbol buffer field.

```

Chapter B : Verilog Code for Digital Controller

```

//
↳ //////////////////////////////////////
↳
29 module SpreadSwitchingOne(
    input clk ,
31    input reset ,
    input [13:0] pzd_word, // ROM Symbol    MSB sign bit is
        ↳ polarity; Binary Zero Delay for All Other Bits
33    input seq_start_flag ,
        input data_ready ,
35    input shutdown ,

37    output reg incROM,
    output reg [3:0] switches = 4'b0000 ,
39    output reg [5:0] fault = 6'b0, // 1    State Machine Fault 2
        ↳ Memory Fault 4    Buffer Fault 8    Buffer State Machine
        ↳ Fault 16    RW_FAULT 32    Fault Aggregate
        output reg signal_data_ready_timeout = 0,
41    output reg seq_start_signal = 0
    );

43
    // Constants
45 parameter PZD_BUSWIDTH = 14;
    parameter COUNT_LATENCY = 13'd1; // Counter latency
47 parameter MIN_ZERO_DURATION = 13'd1;
    parameter MAX_ZERO_DURATION = 13'd300; //d26
49 //parameter MIN_POLARITY_DURATION = 13'd32; // 30+2 used to set
        ↳ polarity duration *****
    //parameter MIN_POLARITY_DURATION = 13'd18; // 18+2 used to set
        ↳ polarity duration *****
51 parameter MIN_POLARITY_DURATION = 13'd23; // 6 11 2015 for ~68ns
        ↳ Tpol at fastest clock
    parameter MAX_POLARITY_DURATION = 13'd32; // not used
53 parameter ZERO_DURATION_WIDTH = 13; // Bit widths
    parameter POLARITY_DURATION_WIDTH = 13;
55

57 // Registers

```

```

    reg symbol_buffer_initialized = 0;
59 reg update_sbuf = 0;
    //reg [12:0] zero_duration = MIN_ZERO_DURATION;
61 reg [5:0] mfault = 6'b0;    // Memory Fault
    reg mfault_signal = 0;
63
    reg clk_Pload = 0;
65 reg clk_Zdload = 0;

67 // Counter Control Registers
    reg start_pcounting = 0;
69 reg load_pcounter = 0;
    //reg [12:0] polarity_duration = 0;
71 reg start_zdcounting = 0;
    reg load_zdcounter = 0;
73 //reg [12:0] zero_duration = 0;

75
    // Wires
77 wire update_sbuf_pulse;
    wire load_pcounter_pulse;
79 wire load_zdcounter_pulse;

81

83 // One Clock Delay      Delay only falling edge
    wire zd_kick;
85 reg [1:0] zd_delay = 0;

87 always@(posedge clk) begin
        zd_delay[0] <= load_zdcounter;
89        zd_delay[1] <= zd_delay[0];
    end

91
    assign zd_load_delayed = zd_delay[1];
93
    // Edge Detection
95

```

Chapter B : Verilog Code for Digital Controller

```
    rising_edge_detect Update_SBUF (  
97      .clk (clk),  
        .signal (update_sbuf),  
99      .rst (reset),  
        .pulse (update_sbuf_pulse)  
101     );  
  
103 rising_edge_detect Load_PCOUNTER (  
        .clk (clk),  
105     .signal (load_pcounter),  
        .rst (reset),  
107     .pulse (load_pcounter_pulse)  
        );  
109  
    rising_edge_detect Clock_PLoad (  
111     .clk (clk),  
        .signal (clk_Pload),  
113     .rst (reset),  
        .pulse (clk_Pload_pulse)  
115     );  
  
117 rising_edge_detect Load_ZDCOUNTER (  
        .clk (clk),  
119     .signal (zd_load_delayed),  
        .rst (reset),  
121     .pulse (load_zdcounter_pulse)  
        );  
123  
    rising_edge_detect Clock_ZdLoad (  
125     .clk (clk),  
        .signal (zd_load_delayed),  
127     .rst (reset),  
        .pulse (clk_Zdload_pulse)  
129     );  
  
131 rising_edge_detect ZdTimeout0 (  
        .clk (clk),  
133     .signal (zd_timeout0),
```

```

        .rst(reset),
135     .pulse(zd_timeout0_pulse)
        );

137
    rising_edge_detect DataReady (
139     .clk(clk),
        .signal(data_ready),
141     .rst(reset),
        .pulse(data_ready_pulse)
143     );

145
    //***** Eight deep Symbol Circular Buffer *****
147 parameter SBUFFER_DEPTH = 8; //
    parameter SBUFFER_IDX_WIDTH = 3; // 2^SBUFFER_IDX_WIDTH =
        ↪ SBUFFER_DEPTH
149 parameter BUFFER_RW_DISTANCE = 3;
    parameter BUFFER_STATE_DELAY = 2;
151 parameter DATA_READY_TIMEOUT = 8'd50;
    parameter SPZD_BUSWIDTH = PZD_BUSWIDTH + 1; // To include the
        ↪ SEQ START FLAG
153

155 //reg [PZD_BUSWIDTH 1:0] symbol_buffer [0:SBUFFER_DEPTH 1]; //
        ↪ This should initialize to zero..
    reg [SPZD_BUSWIDTH 1:0] symbol_buffer [0:SBUFFER_DEPTH 1]; //
        ↪ This should initialize to zero..
157 reg [SBUFFER_IDX_WIDTH 1:0] sbuf_idx = 0;
    reg [SBUFFER_IDX_WIDTH 1:0] read_idx = 0;
159 reg sbuf_initializing = 0;
    reg [5:0] bfault = 6'b0; // Buffer Fault
161 reg bfault_signal = 0;
    reg [7:0] data_ready_timer = DATA_READY_TIMEOUT;
163
    parameter INITIALIZING = 8'b00000001; // 1
165 parameter DATA_READY_TIMEOUT_STATE = 8'b00000010; //2
    parameter INITIAL_UPDATE_BUFFER = 8'b00000100; //4
167 parameter WAIT = 8'b00001000; // 8

```

Chapter B : Verilog Code for Digital Controller

```
parameter UPDATE_BUFFER = 8'b00010000; // 16
169 parameter COPY2BUFFER = 8'b00100000; //32
parameter FAULT = 8'b01000000;
171 parameter RW_FAULT = 8'b10000000;

173 (* FSM_ENCODING="ONE HOT" , SAFE_IMPLEMENTATION="YES" ,
    ↪ SAFE_RECOVERY_STATE="FAULT" *) reg [7:0] bstate =
    ↪ INITIALIZING;

175 always@(posedge clk)
    if (reset) begin
177         bstate <= INITIALIZING;
        symbol_buffer_initialized <= 0;
179         sbuf_idx = 3'd0;
        incROM <= 0;
181         data_ready_timer <= DATA_READY_TIMEOUT;
        signal_data_ready_timeout <= 0;
183         bfault <= 6'b0;
        bfault_signal <= 0;

185     end
    else
187         (* PARALLEL_CASE *) case (bstate)
            INITIALIZING : begin
                ↪ // bstate 1
189                 if (data_ready_pulse) begin
                    bstate <=
                        ↪ INITIAL_UPDATE_BUFFER
                        ↪ ;
191                 symbol_buffer[sbuf_idx]
                    ↪ <= {seq_start_flag ,
                    ↪ pzd_word};
                    ↪ // Update buffer for
                    ↪ ROM output to this
                    ↪ Module and
                    ↪ concatenate Seq
                    ↪ Start Flag
                    //incROM <= 0;
193                 end
```

Section B.4 : Controller State Machine

```

else if (data_ready_timer==0)
  ↪ begin
195
                                bstate <=
                                ↪ DATA_READY_TIMEOUT_STATE
                                ↪ ;

                                end
197
else
                                bstate <= INITIALIZING;
199
incROM <= 1;
symbol_buffer_initialized <= 0;
201
signal_data_ready_timeout <= 0;
data_ready_timer <=
  ↪ data_ready_timer 1;
203
end
DATA_READY_TIMEOUT_STATE : begin //
  ↪ bstate 2
205
  if (signal_data_ready_timeout ==
  ↪ 1)
                                bstate <= INITIALIZING;
207
  else
                                bstate <=
                                ↪ DATA_READY_TIMEOUT_STATE
                                ↪ ;
209
incROM <= 0;
data_ready_timer <=
  ↪ DATA_READY_TIMEOUT;
211
signal_data_ready_timeout <= 1;
end
213
INITIAL_UPDATE_BUFFER : begin
  ↪ // bstate 4
                                if (sbuf_idx > BUFFER_RW_DISTANCE
  ↪ )
  ↪ // if buffer
  ↪ preloaded
215
                                bstate <= WAIT;
                                else
217
                                bstate <= INITIALIZING;
                                sbuf_idx = sbuf_idx + 1;

```

Chapter B : Verilog Code for Digital Controller

```
219         incROM <= 0;
           data_ready_timer <=
             ↪ DATA_READY_TIMEOUT;
221     end
    WAIT : begin
        ↪ // bstate 8
223         if (update_sbuf_pulse) // wait
            ↪ for signal from switch state
            ↪ machine
            bstate <= UPDATE_BUFFER;
225         else
            bstate <= WAIT;
227         symbol_buffer_initialized <= 1;
    end
    UPDATE_BUFFER : begin
        ↪ // bstate 16
229         if (data_ready || ~update_sbuf)
            bstate <= COPY2BUFFER;
231         else
233             bstate <= UPDATE_BUFFER;
            incROM <= 1;
235     end
    COPY2BUFFER : begin
        ↪ // bstate 32
237         if (sbuf_idx == read_idx)
            bstate <= RW_FAULT;
239         else if (!incROM) begin
            bstate <= WAIT;
241             sbuf_idx = sbuf_idx + 1;
            end
243         else
            bstate <= COPY2BUFFER;
245         incROM <= 0;
            symbol_buffer[sbuf_idx] <= {
                ↪ seq_start_flag, pzd_word};
247     end
    FAULT : begin
249         bstate <= FAULT;
```



```

251         bfault <= 6'b000100;
        bfault_signal <= 1;
        end
253     RW_FAULT: begin // bstate 128
        bstate <= RW_FAULT;
255     bfault <= 6'b001000;
        ↪ // Assert buffer fault
        bfault_signal <= 1;
257     end
        default: begin // Fault Recovery
259     bstate <= FAULT;
        bfault_signal <= 1;
261     end
        endcase
263
265 // ***** Fault Handler *****
    reg [5:0] agfault = 6'b0;
267 always@(posedge clk) begin
        if (reset) fault <= 6'b00000;
269     else begin
            fault <= fault | agfault | bfault | sfault |
                ↪ mfault;
271     if (|fault == 1) agfault <= 6'b100000;
        else agfault <= 0;
273     end
    end
275
277 // Memory Error Trapping
    wire [12:0] zd_raw;
279 assign zd_raw = pzd_word[12:0];
281 always@(posedge clk) begin
        if (reset) mfault_signal <= 0;
283     else if (data_ready_pulse) begin
        if ((zd_raw < MIN_ZERO_DURATION) || (zd_raw >
            ↪ MAX_ZERO_DURATION)) begin

```

Chapter B : Verilog Code for Digital Controller

```
285         mfault <= 6'b000010;
           mfault_signal <= 1;
287         end
           end
289         end
291
293 wire [POLARITY_DURATION_WIDTH 1:0] polarity_duration; /**
           wire [ZERO_DURATION_WIDTH 1:0] zero_duration; /**
295
           wire [POLARITY_DURATION_WIDTH 1:0] qP;
297 wire [ZERO_DURATION_WIDTH 1:0] qZd;
299
           assign zero_duration = symbol_buffer[read_idx][
               ↪ ZERO_DURATION_WIDTH 1:0] ; // Preload on previous state
               ↪ compensates counter latency //6/12/15 Removed zd neg offset
301 assign polarity_duration = MIN_POLARITY_DURATION 1
               ↪ COUNT_LATENCY;
           assign ceP = (start_pcounting | clk_Pload_pulse); // No glitches
               ↪ here because logic inputs are spaced in time
303 assign ceZd = (start_zdcounting | clk_Zdload_pulse);
               ↪ // Clock enable Zd counter
305 // Increment Buffer Read Index on Switch OFF states
           // Buffer corrects ROM and switch state synchronization
307 always@(posedge clk) begin
           if (reset) read_idx <= 0;
309           else if (update_sbuf_pulse) read_idx <= read_idx + 1;
           else read_idx <= read_idx;
311 end
           // ***** Switching State Counters *****
313 counter_13bit_loadable PolarityCounter (
           .clk(clk), // input clk
315           .ce(ceP), // input ce
           // .sclr(1'b0), // input sclr
317           // .sset(1'b0), // input sset
```

```

    .load(load_pcounter_pulse), // input load
319 .l(polarity_duration), // input [12 : 0] l
    .thresh0(polarity_timeout), // output thresh0
321 .q(qP) // output [12 : 0] q
    );
323
    counter_13bit_loadable ZeroDurationCounter (
325 .clk(clk), // input clk
    .ce(ceZd), // input ce
327 // .sclr(1'b0), // input sclr
    // .sset(1'b0), // input sset
329 .load(load_zdcounter_pulse), // input load
    .l(zero_duration), // input [12 : 0] l
331 .thresh0(zd_timeout), // output thresh0
    .q(qZd) // output [12 : 0] q
333 );

335 assign zd_timeout0 = (qZd == 0);

337 //reg zd_timeout_reg = 0;
    //always @(posedge clk) zd_timeout_reg = zd_timeout;
339 wire zd_timeout_reg;
    assign zd_timeout_reg = zd_timeout;
341
    // Switching State Machine
343 parameter all_on = 4'b1111;
    parameter all_off = 4'b0000;
345
    parameter ALL_OFF =          8'b00000001; //1
347 parameter PRELOAD =          8'b00000010; //2
    parameter ALL_ON_ONE = 8'b00000100; //4
349 parameter S1_OFF =          8'b00001000; // 8
    parameter S2_OFF =          8'b00010000; ///16
351 parameter ALL_ON_TWO = 8'b00100000; //32
    parameter S3_OFF =          8'b01000000; //64
353 parameter S4_OFF =          8'b10000000;

355 reg [5:0] sfault = 6'b0;

```

Chapter B : Verilog Code for Digital Controller

```
reg [2:0] delaycnt = 0;
357 reg polarity = 0; // Polarity > 0==> Positive , 1==> Negative
parameter POLARITY_BIT = PZD_BUSWIDTH 1;
359 parameter POSITIVE = 0;
parameter NEGATIVE = 1;
361 parameter SEQ_START_BIT = SPZD_BUSWIDTH 1; // Location of flag
    ↪ for sequence start

363

365 (* FSM_ENCODING="ONE HOT" , SAFE_IMPLEMENTATION="YES" ,
    ↪ SAFE_RECOVERY_STATE="SFAULT" *) reg [7:0] state = ALL_OFF;

367 always@(posedge clk)
    if (reset) begin
369         state <= ALL_OFF;
            start_pcounting <= 0;
371         start_zdcounting <=0;
            delaycnt <= 0;
373         //polarity_duration <= MIN_POLARITY_DURATION;
            //zero_duration <= MIN_ZERO_DURATION;
375         update_sbuf <= 0;
            sfault <= 6'b0;
377         switches <= all_off;

            end
379         else

            (* PARALLEL_CASE *) case (state)
381             ALL_OFF : begin
                    if (bfault_signal ||
                        ↪ mfault_signal)
383                 state <= ALL_OFF;

                    else if (
                        ↪ symbol_buffer_initialized)
                        ↪ begin
385                             state <= PRELOAD;
                                end
387             else

                    state <= ALL_OFF;
```

Section B.4 : Controller State Machine

```

389         delaycnt <= 0;
          switches <= all_off;
391     end
PRELOAD: begin
393         if (delaycnt > 3'd5) begin
          state <= ALL_ON_ONE;
395         end
          else
397             state <= PRELOAD;
          delaycnt <= delaycnt + 1;
399         load_zdcounter <= 1;
          clk_Zdload <= 1;
401         switches <= all_off;
    end
403 ALL_ON_ONE : begin
          if (bfault_signal ||
405             ↪ mfault_signal)
          state <= ALL_OFF;
          else if (zd_timeout_reg && (
407             ↪ polarity==POSITIVE)) begin
          state <= S1_OFF;
          start_zdcounting <= 0; //
          ↪ **
409         end
          else if (zd_timeout_reg && (
411             ↪ polarity==NEGATIVE)) begin
          state <= S2_OFF;
          start_zdcounting <= 0; //
          ↪ **
413         end
          else begin
415             state <= ALL_ON_ONE;
          start_zdcounting <= 1;
417         end
          load_zdcounter <= 0;
419         clk_Zdload <= 0;
          load_pcounter <= 0;
421         clk_Pload <= 0;

```

```

423 // start_zdcounting <= 1; /**
start_pcounting <= 0;
polarity <= symbol_buffer [
    ↪ read_idx][POLARITY_BIT];
425 seq_start_signal <= symbol_buffer
    ↪ [read_idx][SEQ_START_BIT];
update_sbuf <= 0;
427 switches <= all_on;

end
429 S1_OFF : begin
    if (polarity_timeout)
431         state <= ALL_ON_TWO;

    else
433         state <= S1_OFF;
//polarity <= symbol_buffer [
    ↪ active_idx][POLARITY_BIT];
435 load_zdcounter <= 1; //
    ↪ Downstream explicit 1 cycle
    ↪ delay
clk_Zdload <= 1; // Downstream
    ↪ explicit 1 cycle delay
437 load_pcounter <= 1;
clk_Pload <= 1;
439 start_zdcounting <= 0;
//load_zdcounter <= 0;
start_pcounting <= 1;
441 update_sbuf <= 1;
switches <= 4'b1110;

end
445 S2_OFF : begin
    if (polarity_timeout)
447         state <= ALL_ON_TWO;

    else
449         state <= S2_OFF;
//polarity <= symbol_buffer [
    ↪ active_idx][POLARITY_BIT];
451 load_zdcounter <= 1;
clk_Zdload <= 1;

```

Section B.4 : Controller State Machine

```
453     load_pcounter <= 1;
        clk_Pload <= 1;
455     start_zdcounting <= 0;
        //load_zdcounter <= 0;
457     start_pcounting <= 1;
        update_sbuf <= 1;
459     switches <= 4'b1101;

    end
461 ALL_ON_TWO : begin
        if (bfault_signal ||
            ↪ mfault_signal)
463             state <= ALL_OFF;
        else if (zd_timeout_reg && (
            ↪ polarity==POSITIVE)) begin
465             state <= S3_OFF;
                start_zdcounting <= 0; //
                    ↪ **
467             end
        else if (zd_timeout_reg && (
            ↪ polarity==NEGATIVE)) begin
469             state <= S4_OFF;
                start_zdcounting <= 0;
471             end
        else begin
473             state <= ALL_ON_TWO;
                start_zdcounting <= 1;
475             end
        load_zdcounter <= 0;
477     clk_Zdload <= 0;
        //start_zdcounting <= 1; //**
479     start_pcounting <= 0;
        load_pcounter <= 0;
481     clk_Pload <= 0;
        polarity <= symbol_buffer [
            ↪ read_idx][POLARITY_BIT];
483     seq_start_signal <= symbol_buffer
            ↪ [read_idx][SEQ_START_BIT];
        update_sbuf <= 0;
```

Chapter B : Verilog Code for Digital Controller

```
485         switches <= all_on;
         end
487     S3_OFF : begin
         if (polarity_timeout)
489             state <= ALL_ON_ONE;
         else
491             state <= S3_OFF;
         //polarity <= symbol_buffer [
         ↪ active_idx][POLARITY_BIT];
493     load_zdcounter <= 1;
         clk_Zdload <= 1;
495     load_pcounter <= 1;
         clk_Pload <= 1;
497     start_zdcounting <= 0;
         //load_zdcounter <= 0;
499     start_pcounting <= 1;
         update_sbuf <= 1;
501     switches <= 4'b1011;
         end
503     S4_OFF : begin
         if (polarity_timeout)
505             state <= ALL_ON_ONE;
         else
507             state <= S4_OFF;
         //polarity <= symbol_buffer [
         ↪ active_idx][POLARITY_BIT];
509     load_zdcounter <= 1;
         clk_Zdload <= 1;
511     load_pcounter <= 1;
         clk_Pload <= 1;
513     start_zdcounting <= 0;
         //load_zdcounter <= 0;
515     start_pcounting <= 1;
         update_sbuf <= 1;
517     switches <= 4'b0111;
         end
519     default: begin // Fault Recovery
         state <= ALL_OFF;
```


Section B.4 : Controller State Machine

```
521          switches <= all_off;  
          sfault <= 6'b000001;  
523      end  
          endcase  
525  
527 endmodule
```


Chapter C

Schematics and Layout

C.1 Quad-Switched Push-Pull Amplifier

C.1.1 Schematics

C.1.2 Printed Circuit Board Layout

C.2 Quad GaN Board

C.2.1 Schematics

C.2.2 Printed Circuit Board Layout

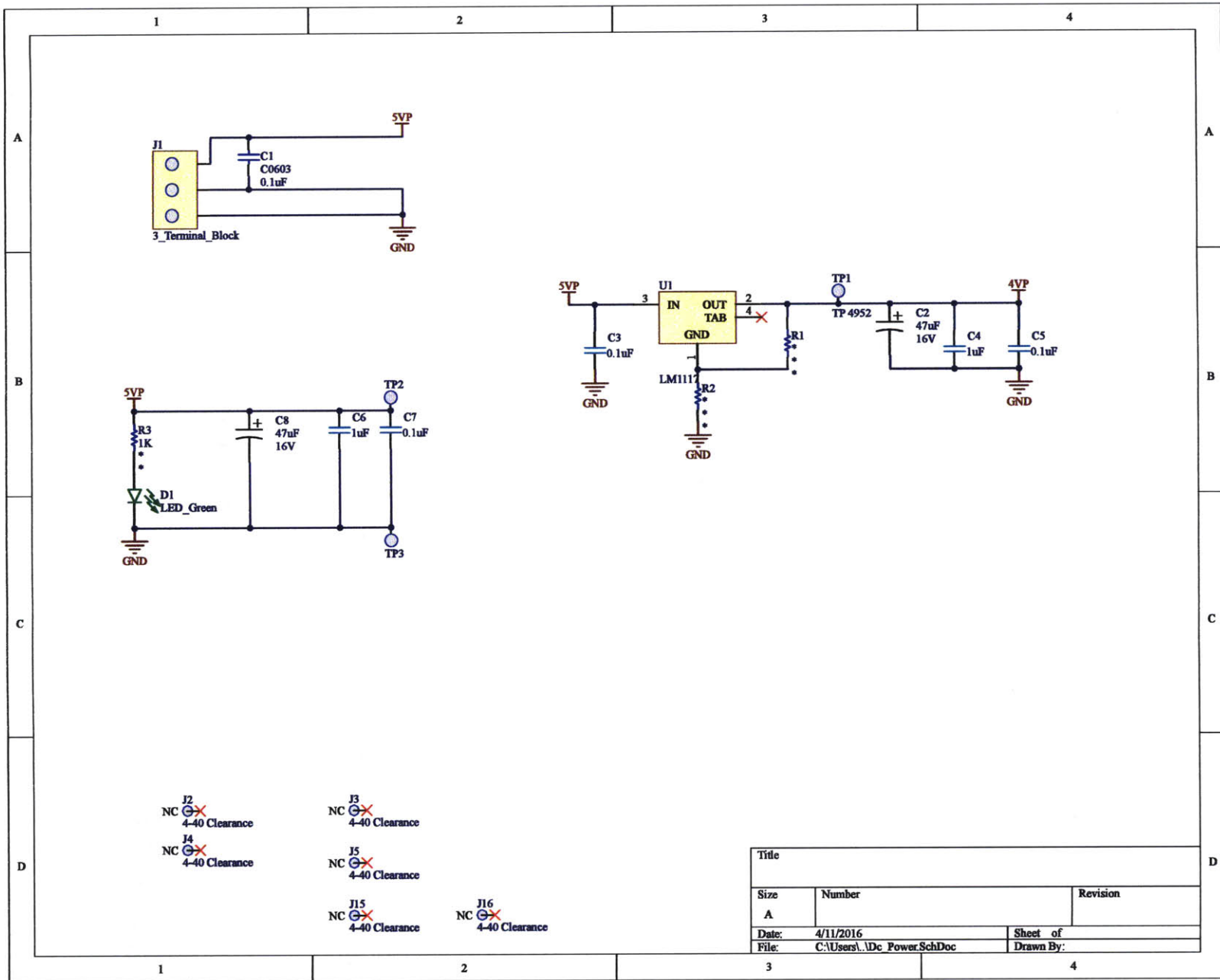
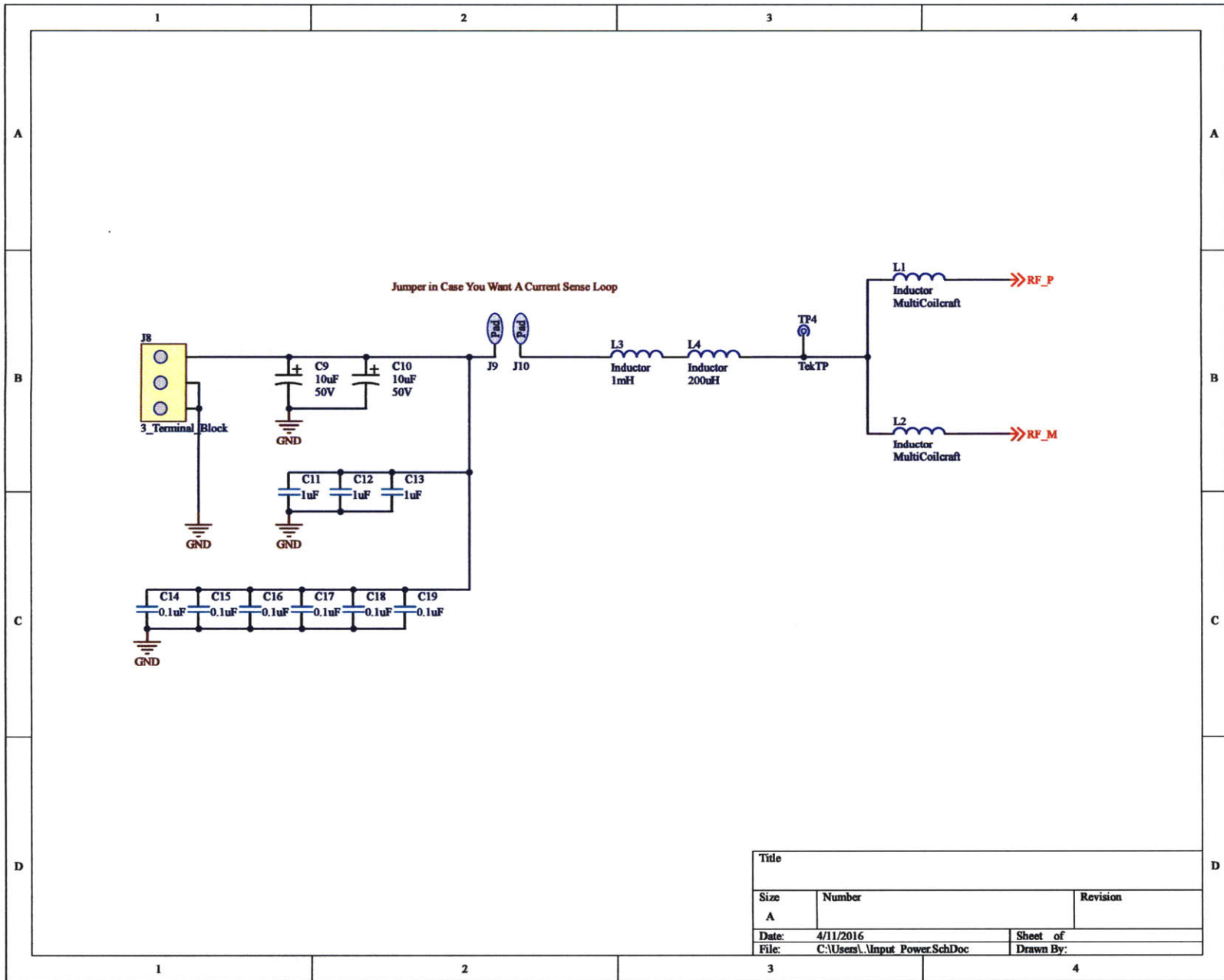


Figure C-1: Auxiliary DC Power Schematic for QSPF Amplifier.

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| | | |
|-------|--------------------------------|-----------|
| Title | | |
| Size | Number | Revision |
| A | | |
| Date: | 4/11/2016 | Sheet of |
| File: | C:\Users\...Input Power.SchDoc | Drawn By: |

Section C.2 : Quad GaN Board

Figure C-2: Input DC Power Schematic for QSPD Amplifier.

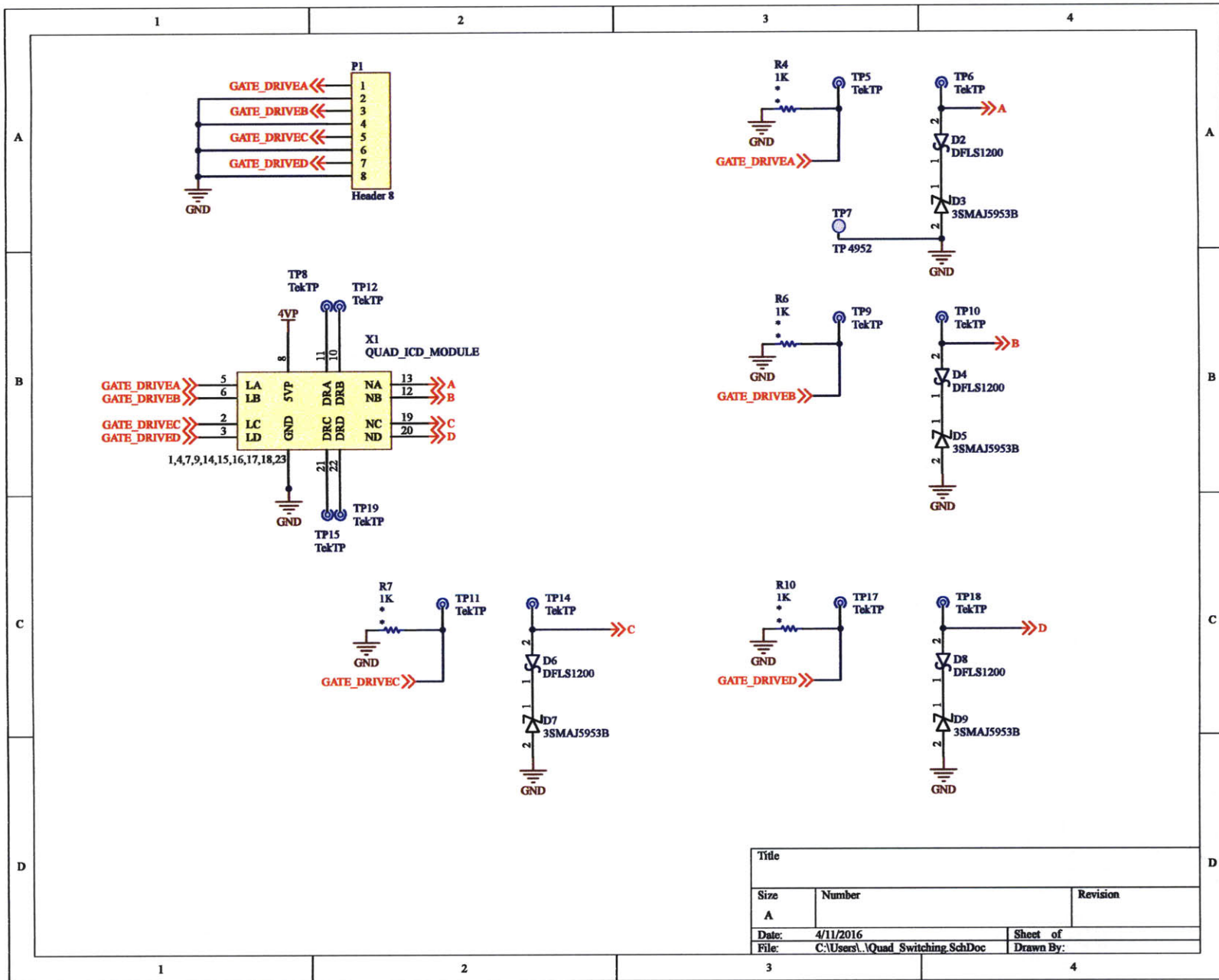
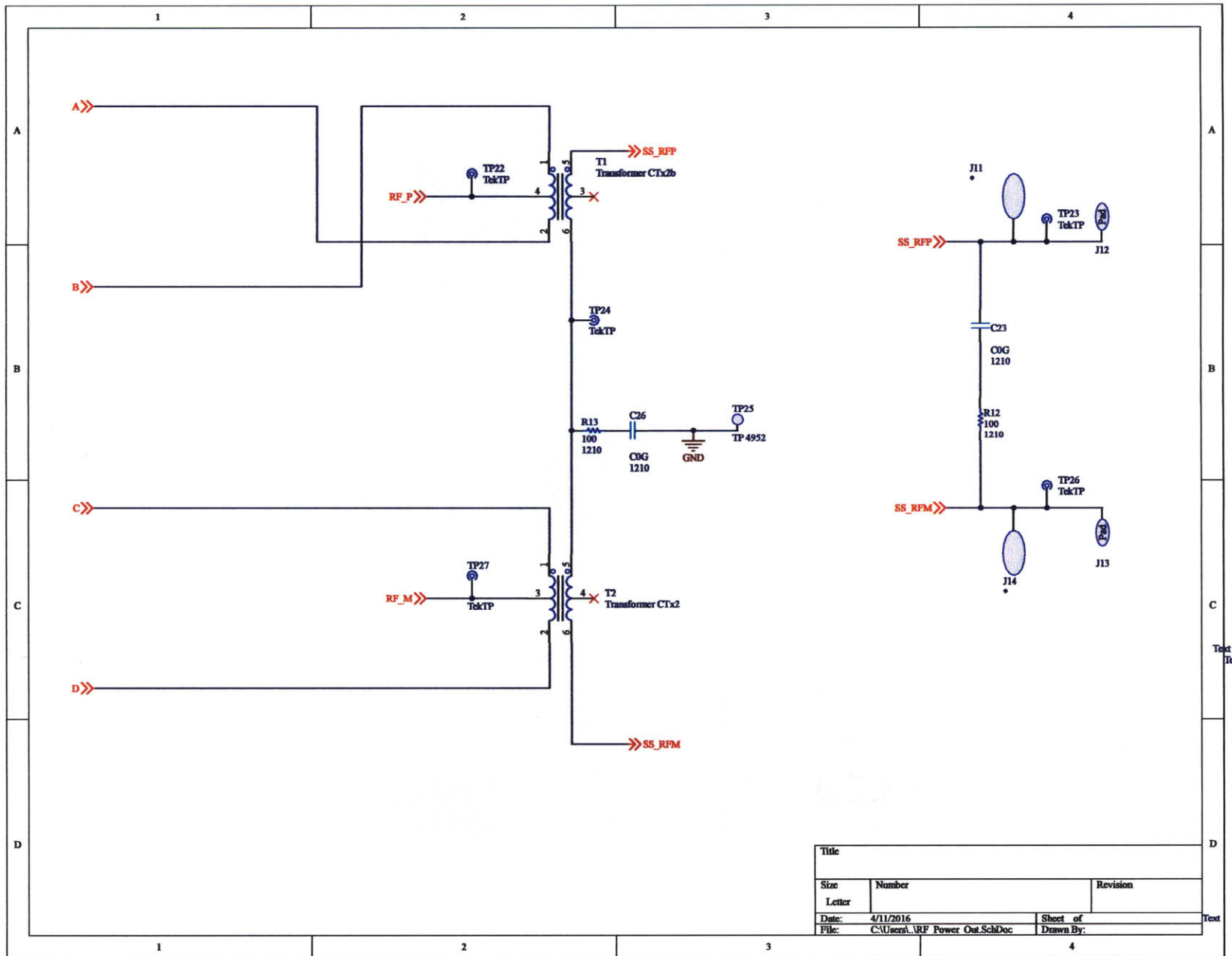


Figure C-3: Switch Module Support Schematic for QSPD Amplifier

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Section C.2 : Quad GaN Board

Figure C-4: RF Output Schematic for QSPD Amplifier

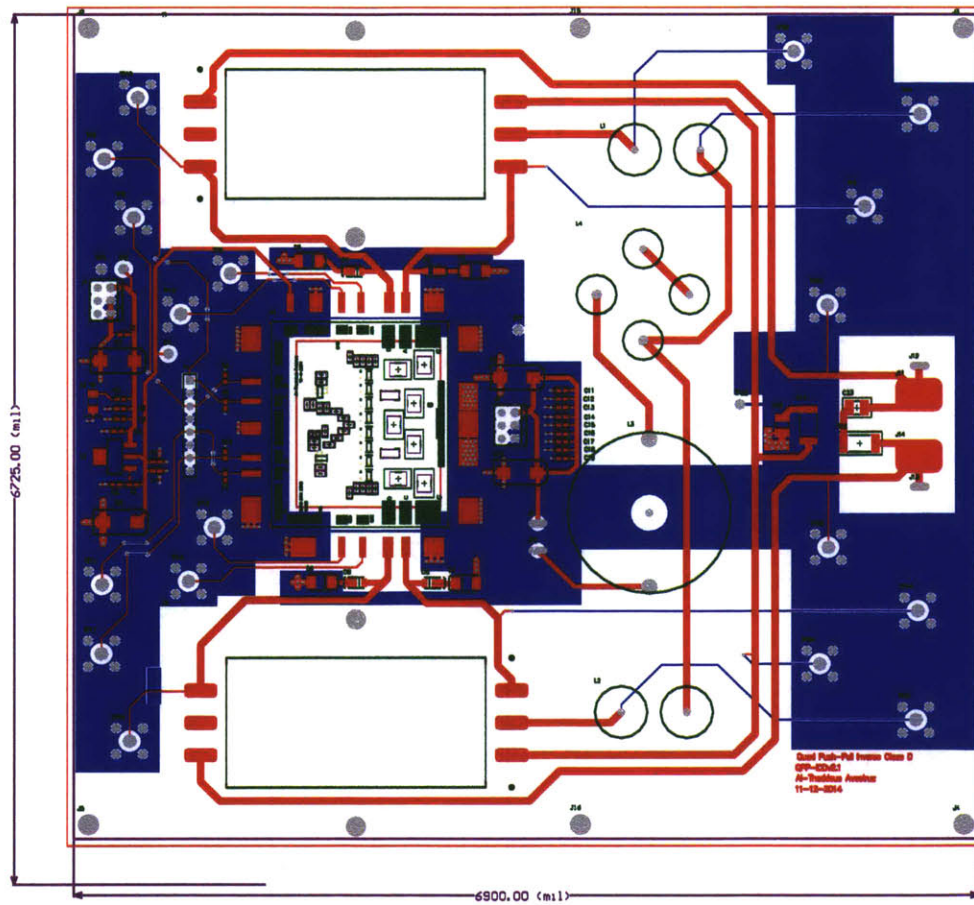
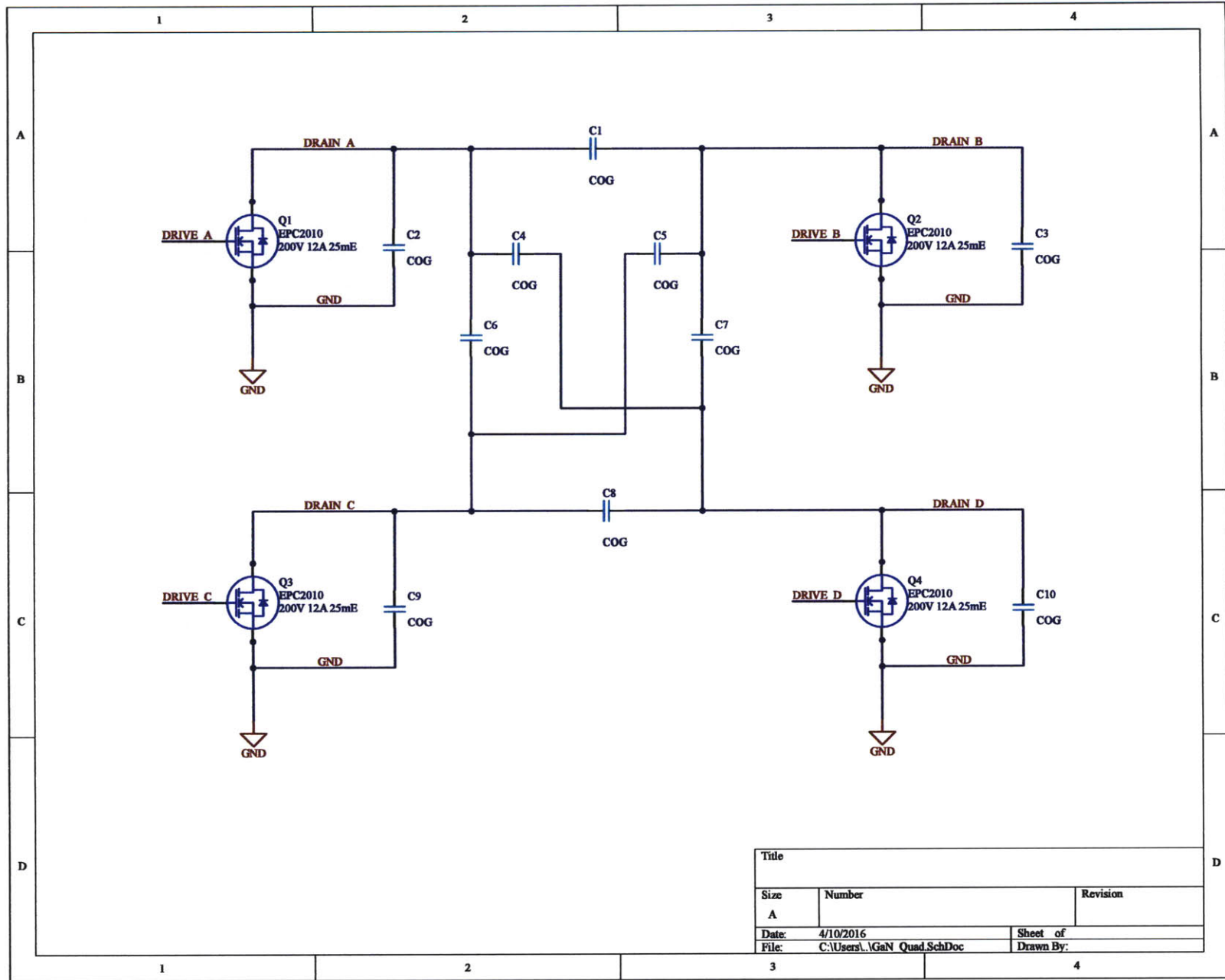


Figure C-5: PCB Layout for QSPD Amplifier

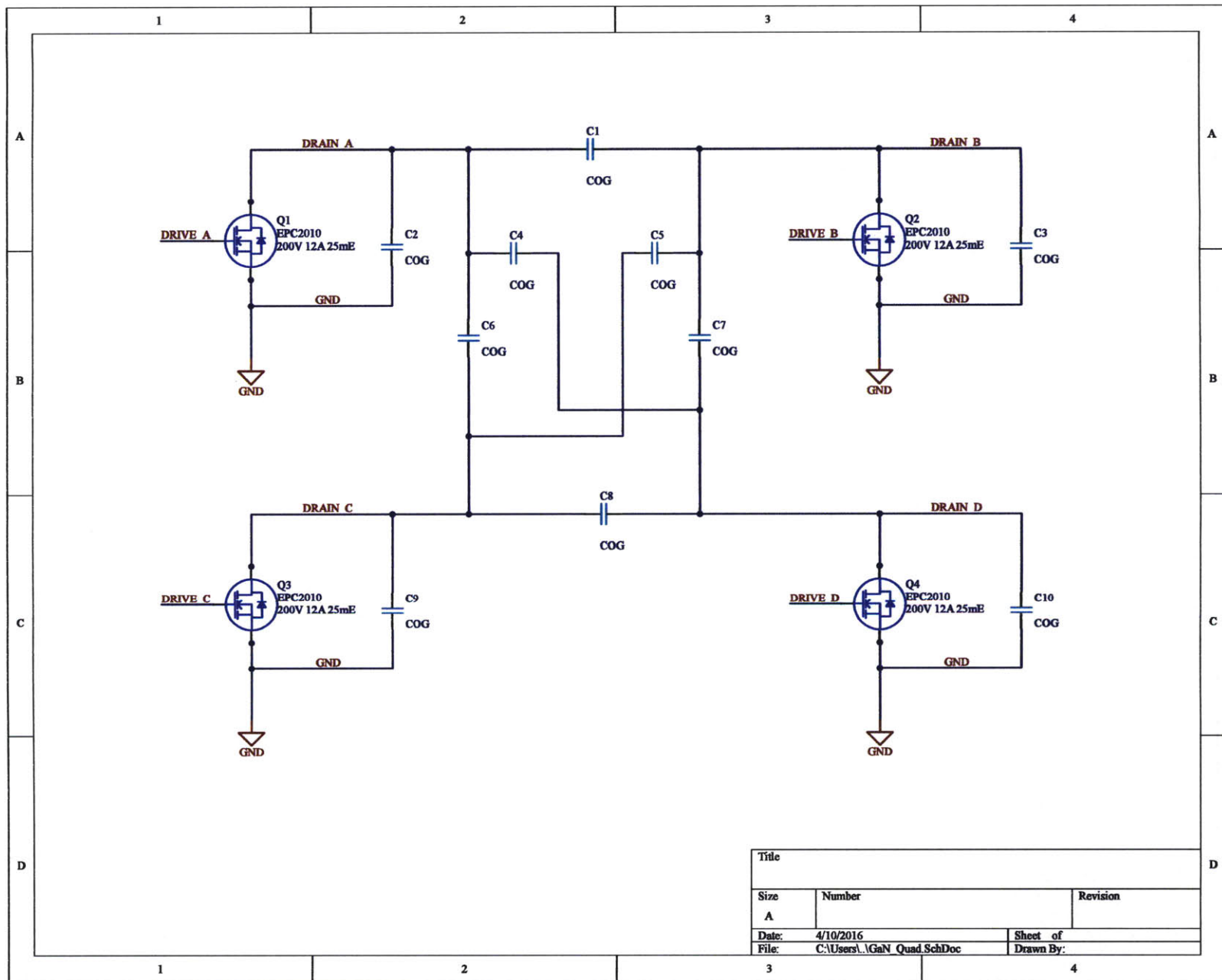
~ 249 ~



Section C.2 : Quad GaN Board

| | | |
|-------|-----------------------------|-----------|
| Title | | |
| Size | Number | Revision |
| A | | |
| Date: | 4/10/2016 | Sheet of |
| File: | C:\Users\l.\GaN_Quad.SchDoc | Drawn By: |

Figure C-6: Main Schematic for Quad GaN Board



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Figure C-7: Single Channel of Gate Driver Subpage for Quad GaN Board

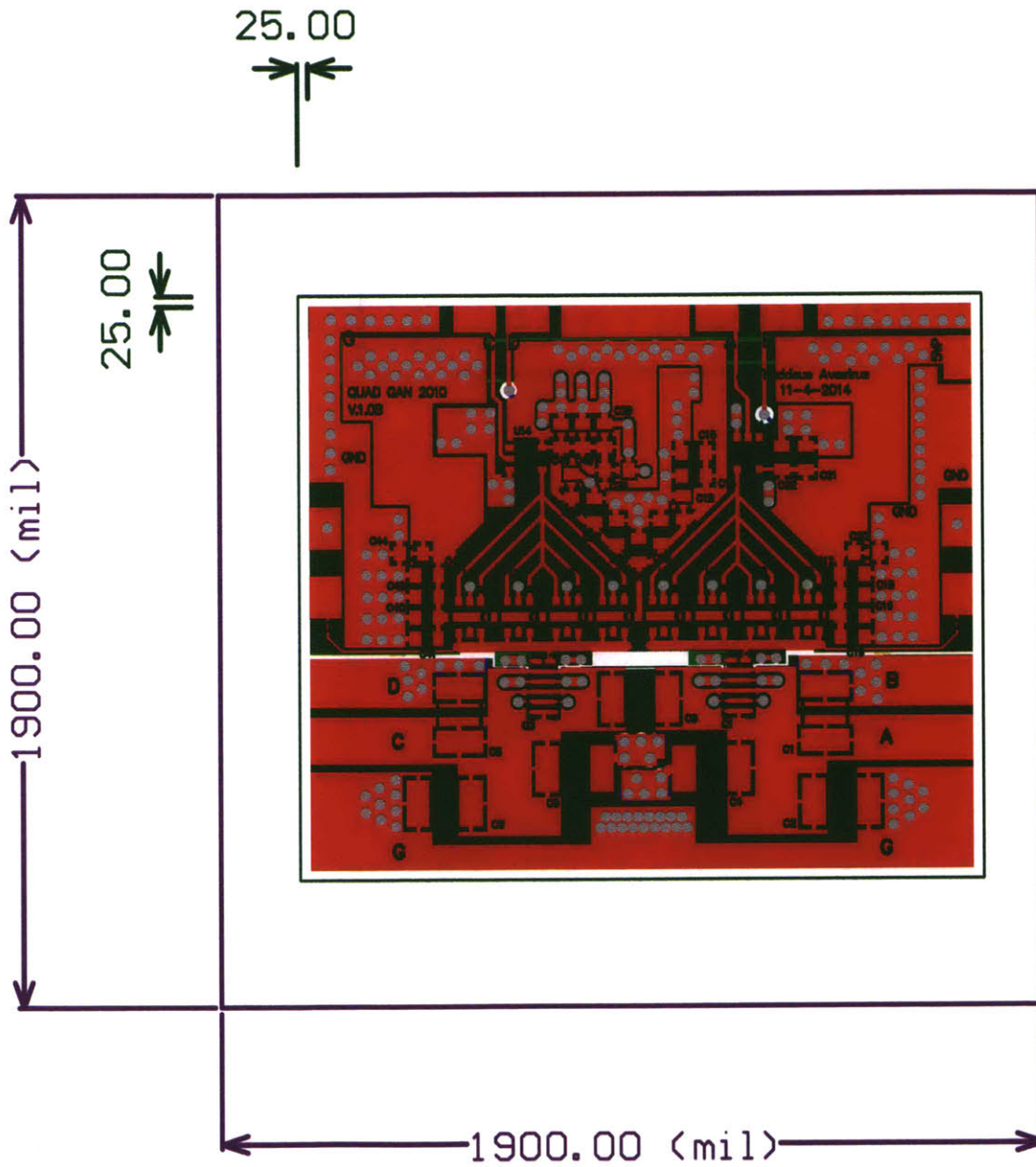


Figure C-8: GaN Quad Top Layer

Chapter D

MATLAB Code for Sequence Optimization

D.1 Top Level Optimization Routine

```
1 % Runs optimizations and analyses related to a ternary sequence
  % optimization whose goal it is to minimize peak to average ratio
  % ↪ of its
3 % analog envelope and low (zero) synchronization error.
  %
5 % The script is divided into sections that can be run "
  % ↪ independently" in
  % the sense that if results from one section are precomputed (e.g
  % ↪ ., loaded
7 % from a MAT file), later sections that can run. Useful in the
  % ↪ case of a
  % very good optimization result emerging and wanting to run
  % ↪ multiple
9 % analyses on it.
  %
11 % Note: The optimization optimizes the entire length of a ternary
  % sequence
13 % that is converted to an analog sequence. Making the length of
  % ↪ the
  % sequence equal to the FCC restrictions should suffice.
15 %
  % REVISION HISTORY
```

Chapter D : MATLAB Code for Sequence Optimization

```
17 % 2013.02.03: Created
    % 2013.02.05: Added spectrum weighting to objective function
19 % 2013.2.14: Made GA output integers; also made RBW settable
    ↪ for peak
    % resolution
21 % 2014.1.18: Random Search and GA for variable length zero
    ↪ durations
    % 2014.5.5: New Dictionary and fix() instead MATLAB GA Int Opt
23 % 2014.5.12: Rewrote w_construct() and fixed bugs. Also in
    % analyzeGavec().
25 % 2014.6.14: Added Zd only optimization functions
    % 2015.3.31: Added and debug windowed optimization
27
    % TO DO:
29 % 2105.4.11 Fix zeros in Zd for windowed optimization ( check
    ↪ crossover
    % and mutation).
31
%% Initialization
33 close all;
    clear;
35 clc;

37 %% User Settings for Optimization and Analysis Parameters

39 optParams = struct(...
    'OptType',          'zdfixed', ...          % 'wpower'
    ↪ windowed power, 'zdfixed' total zd fixed
41 'NsubSeqs',          128, ...                % (64) Number of
    ↪ Subsequences 1024,512,32,256
    'TmDuration',      2^21, ...                % Time Duration for
    ↪ Sampling 2^18, 2^17, 2^20
43 'Upsample',          10^3, ...
    'Dict',             [], ...                % Subsequence
    ↪ Dictionary
45 'PC',                8, ...                  % Number of Sequence
    ↪ Columns per Parfor Iteration
    'PW',               16, ...                % (16) Maximum Number
```

```

    ↪ of CPU Workers for Parallel Processing
47 'gpuFitnessFcn', @gpuFitness, ... % Handle Fitness
    ↪ Function for GPU
'gpuDev', [], ... % GPU Device Handle
49 'gpuCols', 512, ... % Number of
    ↪ Sequence Columns per GPU Iteration
'cpuCores', 16, ... % Number of CPU Cores
51 'ZdIntegers', 1, ... % 1 = Zero Durations
    ↪ (Zd) are integer valued
'ZdMultiplier', 1/18, ... % Mult Zero
    ↪ Durations Useful for Integer Zero Duration Genome (
    ↪ default 15)
53 'ZdLB', 1, ... % Zero Duration Lower
    ↪ Bound
'ZdUB', 50, ... % (50) Zero Duration
    ↪ Upper Bound (+1 for fix() continuous to integer
    ↪ conversion (12+1)
55 'PowerBW', 4e6, ... % For Bandshaped
    ↪ Optimization Bandwidth over which to calculate
'kalpha', 0.5, ... % For Bandshaped
    ↪ Optimization Efficiency Tradeoff Exponent
57 'symbolFrequency', 10e6, ... % In Hz
'lowerFrequency', 2e6, ... % Lower frequency
    ↪ cutoff for spread in Hz
59 'upperFrequency', 5e6, ... % Upper frequency
    ↪ cutoff for spread
'k', 2, ... % Cut off Order
61 'lowerFsens', 100e3, ... % Frequency below
    ↪ which peaks for interference do not matter, but power is
    ↪ not transferrable
'RBW', 3e3, ... % Resolution
    ↪ Bandwidth
63 'ksr', 1, ... % Sequence Repeat
'altSeq', 0, ... % Alternating
    ↪ Sequence = 1; Non Alternating = 0
65 'objFcnHandle', @objFcn2, ... % Handle to objective
    ↪ function for optimization
'useGPU', 1 ... % Use GPU for matrix

```

Chapter D : MATLAB Code for Sequence Optimization

```

        ↪ calculations
67 );

69 optRandSearch = struct (...
    'NSubPops',      512, ...           % Number in
        ↪ subpopulation batch test
71    'NBatches',    200, ...           % Number of batches of
        ↪ NSubPops to test
    'Dummy',        [] ...            % Dummy
73 );

75 optGASetup = struct (...             % Structure to Setup
    ↪ GA
    'NVars',        [], ...           % Number GA variables
        ↪ calculated in gaSetup4Dict()
77    'IntCon',      [], ...           % Integer Constraints
        ↪ Vector calculated in gaSetup4Dict()
    'LB',           [], ...           % Vector of GA
        ↪ variable lower bounds
79    'UB',          [], ...           % Vector of GA
        ↪ variable upper bounds
    'Dummy',        [] ...
81 );

83 optPSSetup = struct (...
    'NVars',        [], ...           % Number PS variables
        ↪ calculated in gaSetup4Dict()
85    'S',           [], ...           % Column Vector of
        ↪ Sequence Dictionary Entries
    'LB',           [], ...           % Vector of PS
        ↪ variable lower bounds
87    'UB',          [], ...           % Vector of PS
        ↪ variable upper bounds
    'InitialPt',   [], ...           % Starting point for
        ↪ PS
89    'Dummy',        [] ...
    );
91

```



```

% Dictionary Setup
93
%dict_B = [1 1 1 1; 1 1 1 1];
95 %dict_B = [1 1; 1 1];      % dict = m symbols x n
    ↪ subsequences
% dict_B = [1; 1];      % dict = m symbols x n subsequences
97 %dict_B = [1 1];      % dict = m symbols x n subsequences

99 % Default for two quadrant sequences
% dict_B = [1 1; 1 1];      % dict = m symbols x n
    ↪ subsequences (last entry is a dummy for fix())
101 % optParams.Dict = dict_B;

103 %optParams.Dict = make_Dictionary16();      % 16 symbol
    ↪ dictionary
%load('Dict283sqz.mat');      % Subsequences with at most one 2
    ↪ flux excursion
105 load('Dict1221.mat');      % Subsequences with only 2 flux
    ↪ excursions
%load('DictHF32.mat');      % Subsequences with HF content
107 %load('DictHF10.mat');      % Subsequences with HF content
optParams.Dict = [U zeros(size(U,1),1)];      % 16 symbol
    ↪ dictionary

109
% GA Setup Modifications
111 optGASetup = gaSetup4Dict(optParams.Dict, optParams); % GA Setup
    ↪ from Parameters
%optGASetup = gaSetup4DictZdOnly(optParams.Dict, optParams); %
    ↪ Setup for Zero Duration Optimization Only
113 %optGASetup = gaSetup4DictPOnly(optParams.Dict, optParams); %
    ↪ Setup for Polarity Optimization Only

115
% Pattern Search Setup
117
optParams.psOpt = psoptimset(...      % Pattern Search
    ↪ Setup
119 'Cache', 'on', ...

```

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```

    'CacheSize',      1e5, ...
121  'CacheTol',      0.5, ...           % Cache tolerance is
    ↪ loose because of fix() for all ga test vectors
    'CompletePoll',  'on', ...
123  'CompleteSearch', 'on', ...
    'Display',      'iter', ...
125  'PlotFcns',     @psplotbestf,...
    'MeshRotate',   'on', ...
127  'OutputFcns',   [], ...           % Output Funcs to
    ↪ call at every iteration fhandle or fhandle cell array
    ...%'PollMethod',    [], ...
129  ...%'SearchMethod',  [], ...
    'TolFun',       1e4, ...
131  'UseParallel',  false, ...
    'Vectorized',   'on' ...
133 );

135 optParams.gaOpt = gaoptimset(...           % GA Setup
    'Display',      'iter', ...
137  'Generations',  500, ...           % Default 10^4 or 200
    ↪ or 500
    'InitialPopulation', [], ...
139  'PopulationSize', 1024, ...           % 512, 1024
    'TimeLimit',    10*60*60,... % Time limit (e.g.,
    ↪ 5*60*60 = 5 hours)
141  'StallGenLimit',  200, ... % Default 1000
    'TolFun',       1e16, ...
143  'PlotFcns',     @gaplotbestf, ...
    'MutationFcn',  {@mutationuniform, 0.05}, ...
145  ...%'MutationFcn',    @mutationadaptfeasible, ...
    'EliteCount',   16,...           % Default 2,16,32
147  'CrossoverFraction', 0.6, ... % Default 0.8
    'CrossoverFcn', @crossoverscattered,...
149  ...%'CrossoverFcn',    @crossovertwopoint,...
    'FitnessScalingFcn', @fitscalingprop,...
151  'SelectionFcn',  @selectionroulette,...
    'HybridFcn',    {@patternsearch, optParams.psOpt},
    ↪ ...

```

Section D.1 : Top Level Optimization Routine

```
153     'Vectorized',          'on', ...
      'UseParallel',       'never' ...
155 );

157

159 % Changing analysisParams does not require re running
      ↪ optimization. If
      % these are changes, the analysis at the end can be re run on its
      ↪ own.
161 analysisParams = struct (...
      'nSymbols',          8, ...      % Number of symbols
      ↪ communicated in the sequence; power of 2 (8)
163     'nShortsPerBlock', 16, ...      % Number of shorts per block
      ↪ (there must be enough non zero indices per symbol block
      ↪ to short)
      'pShort',           3, ...      % Analog power of a short (
      ↪ set to 1 to turn off)
165     'nAvg',             10^5, ...    % Number of simulations of
      ↪ communication to simulate (10^5 is very intense, 10^4
      ↪ could be ok)
      'quantBits',       7 ...      % Number of bits to quantize
      ↪ for FFT post analysis sim of a spectrum analyzer
167 );

169

171 %% Calculate some of the optimization parameters from other
      ↪ parameters
      %optParams.ksr = ceil(optParams.symbolFrequency / (optParams.RBW
      ↪ * optParams.ternarySeqLength));
173

175 %% Initialize Objective Function
      % disp('Initializing Objective Function');
177 % tic;
      % optParams.objFcnHandle([], optParams);
179
```

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```
181 %% Run Random Search Optimization
    % This is a direct search for a good initial seed for a genetic
    % ↪ algorithm
183 optSoln.randSearch.ternarySeq = [];
    optSoln.randSearch.analogSeq = [];
185 optSoln.randSearch.fMag = [];
    optSoln.randSearch.objectiveValue = [];
187
    % Remember to reseed random number generator if re running
189
    disp( 'Running Random Search Optimization' );
191 tic;
    dict_RS = [1; 1];
193 optParams.gpuDev = gpuDevice;
    reset(optParams.gpuDev);
195 rsFitnessFcn = @(v) gaFitnessParams(v, dict_RS, optParams);

197 [optSoln.randSearch.ternarySeq, optSoln.randSearch.analogSeq,
    % ↪ optSoln.randSearch.objectiveValue] ...
    = randsearchW(rsFitnessFcn, optParams, optRandSearch, optSoln
    % ↪ );
199

201 % [optSoln.randSearch.fMag, optSoln.randSearch.ternarySeq,
    % ↪ optSoln.randSearch.analogSeq, ~, optSoln.randSearch.
    % ↪ objectiveValue] ...
    % = randomSequenceSearch(optParams.ternarySeqLength, 1,
    % ↪ optParams.analogUpsample, ...
203 % 0, [1/3 1/3 1/3], 0, optParams.
    % ↪ objFcnHandle, optParams.nIterCoarse, optParams);
    fprintf( 'Completed random search optimization (%d sec) with
    % ↪ objective fcn value %d\n', toc, optSoln.randSearch.
    % ↪ objectiveValue);
205

%% Run Genetic Algorithm
207 % Search the solution space leveraging the solution from the
    % ↪ random search
```

```

209 %rng('shuffle')
    rng('default')
211
    %optParams.gaOpt.InitialPopulation = [];
213 %optParams.gaOpt.InitialPopulation = load('2014_1_16_12_26_29.mat
    ↪ ', 'optSoln.gaSearch.ternarySeq');
    %Stmp = load('2014_1_19_5_34_4.mat', 'optSoln');
215 %optParams.gaOpt.InitialPopulation = Stmp.optSoln.gaSearch.
    ↪ ternarySeq;
    %optParams.gaOpt.InitialPopulation = Stmp.optSoln.randSearch.
    ↪ ternarySeq;
217 optParams.gaOpt.InitialPopulation = [];
    %clear Stmp;
219
    %gaFitnessFcn([], optParams); % Set parameters for the GA fitness
    ↪ functions
221 %optParams.gpuDev = gpuDevice;
    %reset(optParams.gpuDev);
223 gaFitnessFcn = @(v) gaFitnessParams(v, optParams.Dict, optParams)
    ↪ ;
    %gaFitnessFcn = @(v) gaFitnessParams(v, optParams.Dict, optParams
    ↪ ); % Optimize both P and Zd
225 %gaFitnessFcn = @(v) gaFitnessZdOnly(v, [], optParams.Dict,
    ↪ optParams); % Optimize Zd Only
    % gaFitnessFcn = @(v) gaFitnessPOnly(v, ...
227 %     2*ones(1, optGASetup.NVars * size(optParams.Dict,1)), ...
    %     optParams.Dict, optParams); % Optimize P Only
229
    optGASetup.IntCon=[]; % Disable Integer Constraints
231 optParams.gaOpt.HybridFcn = []; % Disables Hybrid Function
    ↪ Option
    optSoln.gaSearch.ternarySeq = [];
233
    window_power = 0; % If window_power==1, frequency window
    ↪ optimization
235 run setup_script_ZdGA;

```

```

237 disp( 'Running Genetic Algorithm' );
    tic;
239 [optSoln.gaSearch.ternarySeq, optSoln.gaSearch.objectiveValue] =
    ↪ ...
        ga(gaFitnessFcn, optGASetup.NVars, [], [], [], [], ...
241     optGASetup.LB, optGASetup.UB, [], optGASetup.IntCon,
        ↪ optParams.gaOpt);

243 if window_power==1; run post_windowopt_script; end

245 % For Zd Only Optimization
    % optSoln.gaSearch.ternarySeq = encodeGAVec(...
247 %     ones(1,optGASetup.NVars/size(optParams.Dict,1) ), ...
    %     optSoln.gaSearch.ternarySeq, optParams.Dict);
249 % [optSoln.gaSearch.analogSeq, optSoln.gaSearch.fMag] = ...
    %     analyzeGAVec(fix(optSoln.gaSearch.ternarySeq), optParams.
        ↪ Dict, optParams);

251 toc;
    fprintf( 'Completed genetic algorithm optimization (%d sec) with
        ↪ objective fcn value %d\n', toc, optSoln.gaSearch.
        ↪ objectiveValue);

253
    %% Run Pattern Search for Zd Only
255 rng('default')

257 % Use this for full format .ternarySeq = {dicEntry1,Zd1,Zd2
    ↪ ,... ,...}
    % [ optPSSetup.S,optPSSetup.InitialPt ] = decodeGAVec(fix(optSoln
    ↪ .gaSearch.ternarySeq), ...
259 %     optParams.Dict);

261 [ optPSSetup.S,optPSSetup.InitialPt ] = single_deconstruct_GAVec(
    ↪ fix(optSoln.gaSearch.ternarySeq), ...
    optParams.Dict);

263
    % Use this for P only .ternarySeq = {dictEntry1, dictEntry2,...}
265 % optPSSetup.S = [fix(optSoln.gaSearch.ternarySeq)];
    %

```

```

267 optPSSetup.NVars = size(optParams.Dict,1) * length(optPSSetup.S);
    optPSSetup.LB = 2*ones(1,optPSSetup.NVars);
269 optPSSetup.UB = 25*ones(1,optPSSetup.NVars);

271 % Use this for full format .ternarySeq = {dicEntry1,Zd1,Zd2
    ↪ ,...,...}
    %optPSSetup.InitialPt = optPSSetup.LB;
273
    %gaFitnessFcn([], optParams); % Set parameters for the GA fitness
    ↪ functions
275 %optParams.gpuDev = gpuDevice;
    %reset(optParams.gpuDev);
277 %gaFitnessFcn = @(v) gaFitnessParams(v, optParams.Dict, optParams
    ↪ ); % Optimize both P and Zd
    psFitnessFcn = @(v) gaFitnessZdOnly(v,...
279     optPSSetup.S, optParams.Dict, optParams); % Optimize Zd
    ↪ Only
    % gaFitnessFcn = @(v) gaFitnessPOnly(v,...
281 %     2*ones(1, optGASetup.NVars * size(optParams.Dict,1)), ...
    %     optParams.Dict, optParams); % Optimize P Only
283
    disp( 'Running Pattern Search ' )
285 [optSoln.psSearch.xopt, optSoln.psSearch.objectiveValue] = ...
    patternsearch(psFitnessFcn, optPSSetup.InitialPt
    ↪ ,[],[],[],[],...
287     optPSSetup.LB,optPSSetup.UB,[],optParams.psOpt);

289 %For Zd Only Optimization
    %optSoln.psSearch.xopt = optSoln.psSearch.ternarySeq;
291
    % optSoln.psSearch.ternarySeq = encodeGAVec(...
293 %     ones(1,optGASetup.NVars/size(optParams.Dict,1)), ...
    %     optSoln.psSearch.xopt, optParams.Dict);
295 % [optSoln.psSearch.analogSeq, optSoln.psSearch.fMag] = ...
    %     analyzeGAVec(fix(optSoln.psSearch.ternarySeq), optParams.
    ↪ Dict, optParams);
297

```

Chapter D : MATLAB Code for Sequence Optimization

```
299 %% Analyze Sequence
    %[ objval ,upsample ,r , u1 , u2 , rbw ] = analyzeSequence( optSoln ,
        ↪ optParams,2^23 );
301 %[ objval ,r , u1 , u2 ,rbw , Lseq ,PwN ] = analyzeSequenceZpad(
        ↪ optSoln ,optParams,2^23 , 10^3 );
    [ objval ,r , u1 , u2 ,rbw , Lseq ,PwN ] = analyzeSequenceZpad( optSoln
        ↪ ,optParams,2^26 , 1633 );
303

305 %% Plot Results
    disp( 'Plotting results ... ');
307 figure(2)
    plot(optSoln.gaSearch.analogSeq)
309 %plot(optSoln.randSearch.analogSeq)
    figure(3)
311 plot(optSoln.gaSearch.fMag)
    %plot(optSoln.randSearch.fMag)
313 figure(4)
    semilogy(optSoln.gaSearch.fMag)
315 %semilogy(optSoln.randSearch.fMag)
    figure(5)
317 stem(optSoln.gaSearch.analogSeq)
    %stem(optSoln.randSearch.analogSeq)
319
    % analysisParams.quantBits = 5;
321 %
    % plotResults(optSoln , analysisResults , optParams , analysisParams
        ↪ );
323

%% Save the results
325 c = int64(clock);
    filename = [num2str(c(1)) '_' num2str(c(2)) '_' num2str(c(3)) '_'
        ↪ num2str(c(4)) '_' num2str(c(5)) '_' num2str(c(6))];
327 save(filename);
```

D.2 createZdPopulation.m

```
function [Population] = createZdPopulation( GenomeLength,
```



```

    ↪ FitnessFcn , ...
2   options , optionsZd)
   %Population = createZdPopulation( GenomeLength, FitnessFcn , ...
4   %   options , optionsZd)
   %   Detailed explanation goes here
6   % New Version ATA 9 15 2014
   %   Based on Dirichlet Process
8   % Tested with testscript_Zd_Functions.m 9 15 2014
   % 9 18 2014 Added and tested quantization error corrector.
10  % 9 25 2014 Corrected Definition of Duty in T

12  optz = optionsZd;

14  % Symbol and Zd parameters
   TSymbol = optz.TSymbol;    % Polarity Duration
16  Zdmin = optz.Zdmin;
   Zdmax = optz.Zdmax;
18  Duty = optz.Duty;
   NPop = optz.NPop;
20  dict = optz.Dict;

22  % Length Parameters
   NSubseqs = optz.NSubseqs;
24  DictNSubseqs = size(dict ,2);
   DictNSymbols = size(dict ,1);
26  SeqLen = optz.NSubseqs*DictNSymbols;

28  % Zd Parameters
   %Γ = round((1 Duty)*SeqLen*TSymbol); % Zd Total
30  T = round((1 Duty)*SeqLen*TSymbol/Duty); % Zd Total
   Tcmin = SeqLen * Zdmin;

32
   % Check Values
34  assert (T>Tcmin, 'Duty Cycle Too Large for Min Zd');
   assert (T<SeqLen*Zdmax, 'Duty Cycle Too Small for Max Zd');

36
   % Dirichlet Parameters
38  % alpha = optz.Alpha;

```

Chapter D : MATLAB Code for Sequence Optimization

```

% scale = optz.Scale;
40
42 % Make the Dictionary Entries
S = fix(1 + (DictNSubseqs - 1)*rand(NSubseqs,NPop)); % Column
    ↪ Vectors of Dictionary Indices
44
% Make the Zero Durations
46 %Zd = zeros(SeqLen,NPop);
    Zd = [];
48 N = NPop;

50 for k=1:optz.IterLimit
    rpn = randfixedsum(SeqLen,N,T,Zdmin,Zdmax);
52    rpn = round(rpn);

54 % Fix Quantization Error: Randomly Spread Remainder over the
    ↪ Sequence
rmd = T * sum(rpn); % Row vector
56 for m=1:N
    if abs(rmd(m))>0.1
58        idmrd = randperm(SeqLen,abs(rmd(m))); % Non
            ↪ repeating indices
        rpn(idmrd,m) = sign(rmd(m))+ rpn(idmrd,m);
60        if sum(rpn(:,m))~= T
            warning('stuff_broke')
62        end
    end
64 end

66 % Accept Columns within bounds
idxMaxOK = max(rpn)<=Zdmax;
68 idxMinOK = min(rpn)>=Zdmin;
%sumOK = sum(rpn)==T;
70 idxOK = idxMaxOK & idxMinOK;
    Zd = [Zd rpn(:,idxOK)]; % Column Vectors of Zero Durations
72

```

```

74  if size(Zd,2)==NPop;
      break
76  else N = NPop  size(Zd,2);
      end
78  % Redraw to add fill the columns
      end
80
      % S is in columns; Zd is in columns
82
      % Construct Population
84  Population = encodeGVec(S,Zd',dict); % S in columns, Zd in rows
      ↪ (i.e. Zd')

86
      end

```

D.3 crossoverZd_windowopt.m

```

function xoverKids = crossoverZd_windowopt( parents , options , nvars
      ↪ , FitnessFcn , ...
2    unused , thisPopulation , optionsZd )
      % xoverKids = crossoverZd( parents , options , nvars , FitnessFcn , ...
4    %    unused , thisPopulation , optionsZd )
      % Detailed explanation goes here
6    % Created ATA 9 5 2014
      % Tested including both Zd crossover functions 9 15 2014 in
8    % testscript_Zd_Functions.m
      % 9 25 2014 Corrected Definition of Duty in T
10   % 3 23 2015 Dynamically windowed power optimization added.

12  optz = optionsZd;
      options.LinearConstr.type = 'unconstrained';
14  ratio = optionsZd.xInterRatio;

16  % Parse Population
      Cf = thisPopulation(:,end); % Separate out end column vector of
      ↪ center frequency candidates
18  SZdPopulation = thisPopulation(:,1:end 1);

```

Chapter D : MATLAB Code for Sequence Optimization

```
%[~,Zd,S] = decodeGAVec(thisPopulation , optz.Dict); % P,Zd,S are
    ↪ column vector sequences
20 [S,Zd] = decodeSZd(SZdPopulation , optz.Dict);
    % S and Z are in columns if thisPopulation is well formed
22
    %% Crossover Dictionary Indices
24 %% XOVERKIDS = CROSSOVERSCATTERED(PARENTS,OPTIONS,GENOMELENGTH
    ↪ , ...
    %% FITNESSFCN,SCORES,THISPOPULATION)
26 % S_xoverKids = crossoverscattered(parents , ...
    % options , size(S,1),FitnessFcn ,unused ,S');
28

30 % Crossover Dictionary Indices and Center Frequencies
    SCf_xoverKids = crossoverscattered(parents , ...
32 options , size(S,1)+1,FitnessFcn ,unused ,[S' Cf]);

34 S_xoverKids = SCf_xoverKids(:,1:end 1);
    Cf_xoverKids = SCf_xoverKids(:,end);
36

38
    % Crossover Zd
40 % Kids are average of parents
    %Zd_xoverKids = crossoverarithmetic(parents , options , size(Zd,1)
    ↪ ,[],[],Zd');
42 % Kids are a random convex combination of parents
    Zd_xoverKids = crossoverintermediate(parents , options , size(Zd,1)
    ↪ ,...
44 [],[],Zd',ratio);

46 Zd_xoverKids = round(Zd_xoverKids); % These are in rows

48 % Fix Quantization Error: Randomly Spread Remainder over the
    ↪ Sequence
    optz = optionsZd;
50
    % Symbol and Zd parameters
```

```

52 TSymbol = optz.TSymbol;    % Polarity Duration
    Duty = optz.Duty;
54 dict = optz.Dict;

56 % Length Parameters
    DictNSymbols = size(dict,1);
58 SeqLen = optz.NSubseqs*DictNSymbols;
    N = size(Zd_xoverKids,1);    % Number of sequences
60
    % Zd Parameters
62 T = round((1/Duty)*SeqLen*TSymbol/Duty); % Zd Total

64 rpn = Zd_xoverKids';
    rmd = T sum(rpn); % Row vector
66 for m=1:N
        if abs(rmd(m))>0.1
68            idmrd = randperm(SeqLen,abs(rmd(m)));
            rpn(idmrd,m) = sign(rmd(m))+rpn(idmrd,m);
70
            if sum(rpn(:,m))~=T
72                warning('stuff_broke')
            end
74        end
    end
76

78 % Re encode Gene
    Zd_xoverKids=rpn'; %encodeGAVec() Zd are row vectors, S are
        ↪ column vectors
80 xoverKids_SZd = encodeGAVec(S_xoverKids,Zd_xoverKids,optz.Dict);
    xoverKids = [xoverKids_SZd Cf_xoverKids];
82

84 end

```

D.4 mutationZd.m

```

1 function mutationChildren = mutationZd( parents, options, nvars,

```

Chapter D : MATLAB Code for Sequence Optimization

```
↪ ...
    FitnessFcn, state, thisScore, thisPopulation, mutationrate,
    ↪ ...
3    optionsZd)
    %mutationChildren = mutationZd( parents, options, nvars, ...
5    %    FitnessFcn, state, thisScore, thisPopulation, mutationrate,
    ↪ ...
    %    optionsZd)
7    %    Created ATA 9 15 2014
    %    9 19 2014 Tested with Dirichlet. Replaced and retested with
9    %    randfixedsum().
    %    9 25 2014 Added check for zero N
11    %    9 25 2014 Change S_muKids from round() to fix() and
    ↪ decodeGAvec() to
    %    decodeSZd()
13    %    9 26 2014 Fixed Zdmax bug causing possible premature GA
    ↪ convergence

15
    optz = optionsZd;
17    options.LinearConstr.type = 'unconstrained';
    options.PopulationType = 'doubleVector';    % For S indices
19    options.PopInitRange = [1; size(optz.Dict,2) 1];

21    % Parse Population
    [S,Zd] = decodeSZd(thisPopulation, optz.Dict); % S,Zd are column
    ↪ vectors of sequences

23
    % Mutate Dictionary Indices
25    S_muKids = mutationuniform(parents, ...
        options, size(S,1), FitnessFcn, state, thisScore, S', ...
27    mutationrate);

29    S_muKids = fix(S_muKids);

31    % Mutate Zd
    Zd_muKids = zeros(length(parents), size(Zd,1));
33
```

```

Zdmin = optz.Zdmin;
35
for i=1:length(parents)
37   Zdmax = optz.Zdmax;
   child = Zd(:,parents(i));
39   % Each element of the genome has mutationRate chance of being
      ↪ mutated.
   mutationPoints = find(rand(1,length(child)) < optz.
      ↪ mutateRateZd);
41
   % Fixed Sum Mutation
43   N = length(mutationPoints);
   Sum = sum(child(mutationPoints));
45
   % Create Replacement Vector;
47
   iterLimit = optz.IterLimit;
49   if Zdmax>Sum
      Zdmax=Sum;
51   else Zdmax = optz.Zdmax;
      end
53
   if N>0
55       for k=1:iterLimit
           rpn = randfixedsum(N,1,Sum,Zdmin,Zdmax);
57           rpn = round(rpn);

59           % Randomly Add The Remainder to rpn to fix
              ↪ quantization error and get exact sum
           rmd = Sum - sum(rpn);
61           if abs(rmd)>0.1
               idmrd = randperm(N,abs(rmd));
63               rpn(idmrd) = sign(rmd)+rpn(idmrd);
               end
65
           if (max(rpn)<=Zdmax && min(rpn)>=Zdmin)
67               break;
           end

```

Chapter D : MATLAB Code for Sequence Optimization

```
69         end
71         % If iterLimit exceeded, don't mutate and send message
           if k<iterLimit
73             child(mutationPoints) = rpn; % Column vectors
           else warning('Mutation1 Failure: IterLimit Exceeded.'
75                 ↪ )
           end
       end
77
       Zd_muKids(i,:) = child'; % These are row vectors
79
       end
81
       mutationChildren = encodeGAVec(S_muKids, Zd_muKids, optz.Dict); %
       ↪ S columns, Zd rows
83
85 end
```


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