Tradeoffs of the use of SiGe buffer layers in tandem GaAsP/Si solar cells

by

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Abstract

III-V multi-junction solar cells currently have the highest reported theoretical and experimental energy conversion efficiency but their cost, mainly attributed to the use of expensive substrates, limits their widespread use for terrestrial applications. Successful integration of III–V’s on a Si substrate to enable a III–V/Si tandem cell can lower the cost of energy by combining the high-efficiency of the III–V materials with the low-cost and abundance of the Si substrate. A maximum theoretical efficiency of 44.8% from a tandem cell on Si can be achieved by using a GaAsP (E_g=1.7 eV) as the top cell. Out of several possible integration routes, the use of a linearly graded SiGe buffer as interfacial layer between the two cells potentially yields the highest quality for the epitaxial GaAsP layer, an essential requirement for realization of high-efficiency solar cells.

In this thesis, the impact of the SiGe buffer layer on the optical and electrical characteristics of the bottom Si cell of a GaAsP/Si tandem solar cell was assessed via experimental work. The growth of a SiGe buffer layer was shown to increase the threading dislocation density and as a result the leakage current of the bottom Si cell by about 10x. In addition, the low-bandgap SiGe absorbs more than 80% of the light that is intended for the Si sub-cell, reducing the short-circuit current of the Si cell from 33 mA/cm^2 to only 6 mA/cm^2. By using a step-cell design, in which the SiGe was partially etched to allow more light to reach the bottom cell, the current was increased to 20 mA/cm^2.

To quantify the merits of the studied approach as well as evaluate other approaches, we have carried out a theoretical study of absorbed irradiance in a Si single-junction cell, a bonded GaAsP/Si tandem cell, a GaAsP/SiGe/Si tandem cell as well as the step-cell design. The GaAsP/Si bonded tandem cell showed 24% relative improvement in light absorption over a single-junction Si cell. The addition of a SiGe graded buffer was shown to reduce the total absorption by 25%, bringing the efficiency of GaAsP/SiGe/Si tandem cell under that of the Si single-junction cell. The step-cell design, even though successful in increasing light absorption, was not found effective in achieving a higher absorbed power density than that of the Si cell. These results suggest that any future work on integrating GaAsP cells on Si towards a high-performance tandem cell should be focused on using a higher-bandgap material as a graded buffer or using a wafer bonding technique.

Thesis supervisor: Judy L. Hoyt
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Thesis supervisor: Jesús A. del Alamo
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Chapter 1

Background

1.1 Single-junction vs. multi-junction solar cells

Single-junction solar cells absorb light only in a portion of the solar spectrum which limits their efficiency. In the case of single-junction Si solar cells, around 20% of the incident solar radiation power is lost due to photons with energy below the band-gap that are transmitted straight through the device and 35% is lost through thermalization of high-energy photons (Fig. 1.1, reproduced from [1]). Thermalization occurs when photons above the bandgap energy are absorbed and the excess energy causes electrons to transition to higher energy levels. These electrons relax back to the band edges and the excess energy is wasted as heat. In the multi-junction cells these losses are reduced by splitting the solar spectrum and using materials optimized to absorb the different portions of the spectrum. This is shown schematically in Fig. 1.2 (reproduced from [2]). The material with the higher bandgap is placed on top allowing all lower-energy photons to be transmitted through it and absorbed in the lower-bandgap material. This high-bandgap material absorbs the high-energy photons, producing usable power, with less thermalization loss compared to the same photons being absorbed in a smaller-bandgap material. By using multi-junction cell design each layer extracts energy from photons closest to its band gap thereby minimizing the total thermalization losses of the stack.

A schematic cross-section of a dual-junction (tandem) cell is shown in Fig. 1.3. The cells are connected in series via tunnel junctions meant to provide electrical connection with a very low
series resistance. With the individual cells being connected in series, the current is limited by the
cell that generates the least amount of current. This reduced current can be somewhat compensated
for by an increase in operating voltage since the operating voltages of each cell add up. To get the
maximum efficiency out of a tandem cell the current in each individual cell at the respective peak
efficiency points has to be equal. This is referred to as current matching. Since the photo-generated
current depends on the number of photons being absorbed in each cell, it can be adjusted by
optimizing the thickness of each cell. The bandgap, absorptivity and doping of the material must
be taken into consideration when optimizing the thickness of the cell.

Fig. 1.1: Illustration of the losses in a single-junction silicon solar cell, associated with the sub-bandgap
(transparency) losses of low-energy photons and the thermalization losses of high-energy photons.
Reproduced from [1].
Currently multi-junction (MJ) solar cells have the highest reported theoretical and experimental efficiencies (Fig. 1.4)[3]. MJ III–V solar cells not only hold the current world record experimental efficiency of 46% for a four-junction cell at 508x concentrated light [4] but have also shown a steady increase in efficiency since 2000. In comparison, the performance of single-junction, non-concentrator Si solar cells has almost saturated at around 25% for the past 15 years, with the highest efficiency of 25.6% reported in 2014 [5]. The highest reported efficiency from a Si solar cell altogether is 27.6% under concentrated light of 92x. Nevertheless, Si solar cells still dominate the solar cell market with about 90% of the installed units due to its highly developed processing technology and low cost. Most MJ cells are integrated on III-V or Ge substrates that are significantly more expensive than Si substrates which limits their widespread use for terrestrial
applications. Successful integration of III–V solar cells on Si substrate can lower the cost of energy by combining the high-efficiency of the III–V materials with the low-cost and abundance of the Si substrate.

![Best Research-Cell Efficiencies](image)

**Fig. 1.4:** Best reported solar cell efficiencies for given technology from 1975 to present. Single- and multi-junction III-V cells (purple) hold the highest achieved efficiencies for over 25 years. Reproduced from NREL[3].

### 1.2 Motivation for GaAsP/Si tandem cells

When choosing materials for a tandem solar cell, one of the key considerations is their potential for achieving maximum conversion efficiency. Previous works on the modeling of the Shockley–Queisser limit in a dual-junction cell have shown a maximum theoretical efficiency between 42.2% and 45.7% (1 sun, AM1.5G) for materials with bandgaps of 1.6-1.64 eV for the top and 0.94-0.964 eV for the bottom cell [6]–[8]. Optimum bandgap combinations slightly differ from one study to the other due to the difference in the models and assumptions used for
calculations. These optimum tandem cell designs require the use of III-V materials and are still mostly limited to applications in space and concentrated solar power due to their inherently high costs. In order to make dual-junction solar cells commercially available, efforts are being made to achieve high conversion efficiency at a lower cost by using abundant materials such as Si.

A contour plot of the simulated maximum efficiencies as a function of the top and bottom bandgaps is shown in Fig. 1.5 (reproduced from [9]). It can be seen that the maximum theoretical efficiency achievable from Si-based solar cell (1.12 eV) is only 1% less than the most optimal design – 44.8% compared to 45.6%, making it a viable option for high-efficiency, low-cost solar cell. In order to reach the optimal efficiency, the top cell must have a bandgap of ~1.7 eV.

There are multiple semiconductors with a band gap of 1.7 eV that could be implemented in this dual-junction solar cell. Fig. 1.6 shows the energy gap vs. lattice constant diagram for common semiconductor materials. A number of compounds cross the 1.7-eV line (GaAsP, InGaP, AlGaAs) but none of them is latticed-matched to Si. Lattice mismatch represents one of the greatest challenges in the integration of III-V materials on Si. If not properly accounted for, even a 1% lattice mismatch can lead to nucleation of a large number of dislocations which is detrimental to solar cell performance. As seen from the figure, the material with the least amount of lattice mismatch with respect to Si is GaAsP, making it the best candidate for Si integration. However, this still results in a ~4% lattice mismatch that requires the use of compositionally graded buffers to move the lattice constant from Si to that of GaAsP.

There are two main approaches to integrate GaAsP on a Si substrate: using GaAsP buffers or using SiGe buffers, indicated with the red and green arrows, respectively, in Fig. 1.6. The specific growth techniques and problems associated with each integration route will be covered next.
Fig. 1.5: Simulated theoretical efficiency of a dual-junction solar cell for different top and bottom cell bandgap combinations. A maximum efficiency of 45.6% can be achieved with top and bottom cells with bandgaps of 1.6 eV and 0.95 eV, respectively. [9] The maximum achievable efficiency when using Si as the bottom cell is 44.8%.

Fig. 1.6: Energy gap vs lattice constant diagram. The optimal bandgaps of 1.1 eV and 1.7 eV for the maximum theoretical efficiency of a dual-junction solar cell are shown.

1.3 Techniques for III-V integration on Si

High-quality III-V materials cannot be directly grown on top of a Si wafer due to the difference in their lattice constants as well as coefficients of thermal expansion that leads to the creation of
threading dislocations and other defects that compromise device performance. The two commonly used routes for integrating III-V materials and Si substrates are mechanical stacking techniques and graded buffer approaches.

When it comes to mechanical stacking, different groups have experimented with direct fusion bonding [10], surface activated direct wafer bonding [11], [12] and direct metal interconnect [13]. Both bonding methods require the top cell to be grown on a separate handle wafer, flipped over and bonded upside-down to the Si substrate (Fig. 1.7). The handle wafer is then removed by chemical-mechanical polishing (CMP). In the direct fusion bonding method, the top of the Si wafer and the bottom of the III-V cell are very heavily doped prior to the bonding. The bonding of the two wafers is then done at relatively high temperature - 300ºC. The major challenge of this method is the selection of interfacial layers with appropriate polarity and doping concentration which might restrict the design of the solar cell. In addition, the high temperature required for bonding may lead to structural changes and decomposition of the III-V materials.

The surface activated wafer bonding method is similar to the direct fusion method but it can be performed at lower temperatures – room temperature to 200ºC. The surface activation prior to bonding is done by cleaning the surface via fast atom bombardment (argon, xenon). Since there is always a certain amount of tilt and twist in the orientation of the wafers during bonding, the atom rearrangement is not perfect, resembling a grain boundary at the bonded interface. This imperfect arrangement increases the series resistance of the interface and may limit the use of the Si cell as an active cell. There is also an additional cost component associated with the carrier wafers and extra CMP and surface activation steps.
In the direct metal interconnect method, the two cells are fabricated in separate processes and are stacked mechanically via transparent epoxy with a metal-to-metal interconnect providing the electrical contact between the two sub-cells (Fig. 1.8). One of the major challenges when using a mechanical stacking technique is that the different materials can have significantly different coefficients of thermal expansion (CTE) which can lead to the formation of cracks and defects in both cells and reduce the overall efficiency and compromise the long term reliability. In addition, due to the use of multiple wafers and additional steps and processes, mechanical stacking approaches are more suited for applications where the cost of the final cell is less of an issue.

Fig. 1.8: Illustration of direct metal interconnect (DMI) technique. The two solar cells are fabricated in two separate processes and stacked together via epoxy. The fingers on the bottom of the top cell and the top of the bottom cell have a 90° offset to form cross-grid interconnection.
The graded buffer technique utilizes an additional layer that is epitaxially grown in between the two cells and helps span the difference between the lattice constants of both cells. This is possible due to the fact that graded buffers consist of a compound semiconductor with a composition that can be linearly graded during their growth. As the composition of the buffer layer changes, its lattice constant also changes. The starting composition of the graded buffer is chosen to have a lattice constant close to that of the substrate and the grading is stopped when the desired lattice constant of the top layer is reached. This helps reduce the lattice mismatch between the two cells and significantly improves the quality of the top cell. Furthermore, since the graded buffers are grown directly on a Si substrate, this method bypasses the additional cost associated with the use of more expensive handle wafers.

1.4 Growing GaAsP on Si

There are two different integration routes available for growing GaAsP layers on Si – through the use of GaP and GaAsP buffers and through the use of SiGe buffers.

The first approach involves direct deposition of GaP on Si followed by compressive grading of GaAsP. The lattice constant of GaP is closest to that of Si and the effect of lattice mismatch on the buffer growth is expected to be relatively small. One of the advantages of using this approach for the dual-junction solar cells is that the GaP film and the graded buffer of GaAsP will have band gaps larger than 1.7eV. This means that the buffer layers will be transparent to the light that is intended for the bottom Si cell which should increase the efficiency from the tandem cell. However, achieving high-quality GaP/Si interface has been challenging mostly due to the thermal
expansion mismatch between the GaP and Si and the polar/non-polar interface [14], [15]. In addition, GaAsP top cells grown on GaP/Si virtual substrates have been shown to have high threading dislocation density (TDD) of $1 \times 10^{17} - 2 \times 10^{18} \text{cm}^{-2}$ [16], [17].

Another route to integrate GaAsP on Si substrate is through the use of SiGe graded buffers. SiGe is the most advanced and well-established relaxed graded buffer technology. It can be used to extend the lattice constant from Si to any composition of SiGe, providing a virtual substrate for a lattice-matched GaAsP growth. The biggest advantage of using SiGe graded buffers is that the SiGe growth can been optimized to yield a very low threading dislocation density (TDD). Achieving low TDD in the epitaxially grown layers is one of the most essential requirements for the realization of high-efficiency tandem cells. In fact, Sharma has shown that material quality is more important for device performance than the number of junctions used [18]. If there are a lot of defects and dislocations in the top GaAsP layer, they will act as recombination centers for the minority carriers and will deteriorate device performance. Yamaguchi and others have shown that for TDD of $10^6 \text{ cm}^{-2}$ and lower, the solar cell efficiency is no longer limited by the dislocation density [19][20]. This is due to the fact that at this density the minority carrier diffusion length is significantly smaller than the average distance between two dislocations. Milakovich has successfully grown GaAsP layers on a SiGe buffer with a threading dislocation density of $1-2 \times 10^6 \text{ cm}^{-2}$ showing the great promise of SiGe buffers in accomplishing high-quality GaAsP/Si solar cells capable of reaching efficiency exceeding that of Si cells [21], [22].

The goal of this thesis is to assess the tradeoffs of the use of SiGe buffer layers in GaAsP/Si cells. On one hand, the SiGe is capable of delivering the highest possible quality of the top GaAsP layer, which as an essential requirement for making the integration of GaAsP cell on Si
worthwhile. In addition, the monolithic growth of all materials provides electrically active interface – a necessary condition for using the Si as an active cell in a two-terminal solar cell configuration. On the other hand, the use of a SiGe graded buffer will result in some absorption of the photons with energy below 1.7 eV because of the smaller bandgap of the SiGe alloy. In this work, the extent to which SiGe impacts the performance of the bottom Si cell will be explored.

1.5 Thesis organization

The fabrication of the bottom Si solar cell will be covered in Chapter 2. The design of the base and the anti-reflection coating (ARC) will be carried out by simulations and the optimal emitter thickness and doping levels will be determined through characterization of fabricated Si solar cells. The designed Si-cell will then be subjected to a SiGe buffer layer growth and the impact of this growth on the device characteristics with respect to leakage current, TDD and series resistance will be covered in Chapter 3. Chapter 4 will describe the fabrication of SiGe/Si solar cell and the analysis of the optical impact of the SiGe buffer layer on the characteristics of the Si cell. A step-cell design in which the SiGe layer is partially etched to allow more light to reach the Si sub-cell will be presented. In chapter 5, simulations of the maximum efficiency available from a GaAsP/Si tandem cell with and without SiGe buffer will be presented. Chapter 6 will summarize important contributions from this work and will outline future studies necessary for realizing high-efficiency and low cost GaAsP-Si tandem solar cells.
Chapter 2

Bottom Si solar cell design and fabrication

Before the impact of the SiGe growth on the bottom Si cell can be studied and quantified, the Si sub-cell itself must be designed and fabricated. In this chapter, key aspects of Si sub-cell design are discussed. In particular, the optimal doping level and ARC thickness were determined with the use of simulations. The chapter also describes a process for fabrication of the Si sub-cell as well as characterization results. Emitter design splits were performed out of which an optimum design emerged.

2.1 Simulations

The simulations were performed using the one-dimensional solar simulator PC1D [23]. The following input parameters must be specified: base doping and thickness, emitter doping and thickness, contact implantation parameters, minority carrier lifetime in both regions, device area, optical coating and surface recombination velocities, among others. The solar spectrum and the excitation conditions (in our case, AM1.5G, 1 sun) are loaded from an external text file. PC1D provides the short-circuit current ($J_{sc}$), open-circuit voltage ($V_{oc}$) and the efficiency of the cell as outputs from the simulation.
2.1.1 Design of the base

The simulated structure is shown in Fig. 2.1. In this work, the n-on-p structure was adopted due to the higher surface quality of n-doped Si which enables higher quality for the subsequent epitaxial growths. In addition, the mobility of electrons is higher than that of holes which increases the diffusion length and the collection probability of carriers generated in the base. The n-type doping of the emitter was chosen to be $6 \times 10^{18}$ cm$^{-3}$ in order to achieve a sheet resistance of 100 Ω/□ at 1 μm thickness, often quoted in literature. The thickness of the emitter (1 μm) was chosen to be sufficiently smaller than the diffusion length at this doping level (6.5 μm) to guarantee collection of the carriers generated in this region. The base width was made equal to the standard thickness of a 6-inch wafer (650 μm). The doping of the base was varied between $10^{15}$ cm$^{-3}$ and $10^{18}$ cm$^{-3}$.

![Simulated structure](image)

Fig. 2.1: Cross-section of the simulated structure.

In order to pick the optimal base design, one must look into how the doping level of the base affects $J_{sc}$ and $V_{oc}$; ideally both must be as high as possible for greatest cell performance. However, often these two parameters cannot be maximized at once. On one hand, as the doping of the base is increased, $J_{sc}$ decreases as a result of the shorter minority carrier diffusion length. On the other hand, $V_{oc}$ increases by the natural logarithm of the doping level in the base. After reaching a certain
doping level, $V_{oc}$ no longer increases because the higher doping level increases the chances of recombination, i.e., increases the dark current. This is shown in Fig. 2.2 for different surface recombination velocities ($S$).

The surface recombination velocity represents the readiness with which the carriers recombine at the semiconductor surface. A perfectly passivated surface will have $S=0$. This can be achieved by growing SiO$_2$ on the wafer surface, for example. Under the metal contacts, the surface recombination velocity will be significantly higher due to disruptions in the semiconductor lattice. In these simulations, the front surface recombination velocity was varied from 0 to 1000 cm/s to capture the ideal case and the differences in the simulated parameters caused by the disruptions under the metal contacts. The back surface recombination velocity was not taken into consideration ($S = 0$ cm/s). It can be seen that $S$ affects mainly $V_{oc}$ - an expected result given that $V_{oc}$ depends on the dark current which increases with the amount of recombination in the device.

![Simulated open-circuit voltage ($V_{oc}$) and short-circuit current ($J_{sc}$) as a function of substrate doping for different surface recombination velocity at the top surface ($S$).](image)

**Fig. 2.2:** Simulated open-circuit voltage ($V_{oc}$) and short-circuit current ($J_{sc}$) as a function of substrate doping for different surface recombination velocity at the top surface ($S$).
To assist in the selection of base doping, the cell’s efficiency will be utilized as it is an overall metric for performance encompassing both $J_{sc}$ and $V_{oc}$. Fig. 2.3 shows the efficiency as a function of base doping level. It can be seen that a doping level between $5 \times 10^{15}$ cm$^{-3}$ and $1 \times 10^{16}$ cm$^{-3}$ provides the highest efficiency. The closest doping level available from the vendor was $2 \times 10^{16}$ cm$^{-3}$, which was used in the following simulations.

![Image of efficiency graph](image)

**Fig. 2.3:** Simulated efficiency as a function of substrate doping for different surface recombination velocity ($S$).

### 2.1.2 Design of the anti-reflection coating

A bare Si surface reflects more than 30% of incoming solar light. In order to reduce reflections, an anti-reflection coating (ARC) must be applied to the surface. The ARC consists of a thin layer of dielectric material, with a thickness chosen to minimize the net reflected energy. The ARC reduces reflected energy because the interference effects in the coating causes the wave reflected from the anti-reflection coating top surface to be out of phase with the wave reflected from the semiconductor surface. Double-layer ARC is used to minimize the reflection even further [2], [24]. In the process of designing the bottom Si cell, SiO$_2$ and Si$_3$N$_4$ are chosen because they are readily available and can provide a high quality ARC layers.
Fig. 2.4 shows the cross-section of the simulated structure in (a) and the simulated efficiency as a function of SiO$_2$ thickness with Si$_3$N$_4$ thickness as a parameter in (b). For each Si$_3$N$_4$ thickness there is an optimum SiO$_2$ that provides minimum reflected energy. The reflected energy depends on the reflection coefficients and the thicknesses of the two materials and it is minimized when the optimal thicknesses ratio is achieved. The minimum in reflected energy corresponds to a maximum in efficiency which explains the shape of the curves in the figure. The overall optimal thickness ratio is then chosen from the maximum efficiency among all curves. The simulation results show a maximum efficiency of 19.2% for an anti-reflection coating consisting of 20 nm of SiO$_2$ and 50 nm of Si$_3$N$_4$, so this coating composition was used moving forward.

2.2 Fabrication of Si solar cell

2.2.1 Si cell structure and process splits

The structure of the Si cell and the process splits are shown in Fig. 2.5. The structure consists of an n-type emitter, grown on p-type base. The devices are isolated from one another via mesas. An n+ implant is included for the top contact and p+ back-surface field (BSF) and contact implants
are included on the back side of the wafer. Titanium/aluminum was used as top metal and aluminum was used for the back contact.

There are six splits designed to explore the impact of emitter doping and thickness, presence of contact implants and back-surface field (BSF), and the presence of an optional boron-doped layer. The top contact implant is expected to reduce the contact resistance and as a result the overall series resistance of the cells. The BSF is a highly-doped layer that creates an energy barrier to keep the carriers away from the back of the wafer where the metal contact presents a high surface recombination velocity. The optional boron-doped layer is grown on the wafer surface prior to emitter growth and it is intended to bury any residual impurities and yield a pristine growth surface where the p-n junction is to be placed.

![Diagram](image)

**Fig. 2.5:** Si bottom cell design: (a) Cross-section of the fabricated structure; (b) Process splits showing varying emitter thickness, doping level, addition of boron-doped layers and contact implants.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>P-type epi-layer</th>
<th>Emitter doping, cm⁻³</th>
<th>Emitter thickness, μm</th>
<th>BSF and N+ contact implant</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No</td>
<td>6e+18</td>
<td>0.5</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>No</td>
<td>6e+18</td>
<td>1</td>
<td>No</td>
</tr>
<tr>
<td>3</td>
<td>No</td>
<td>6e+18</td>
<td>1</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>Yes</td>
<td>6e+18</td>
<td>1</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>No</td>
<td>1.2e+19</td>
<td>0.5</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>No</td>
<td>2.5e+19</td>
<td>0.25</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Fig. 2.6 shows the top metal layout of the cells. There are three different designs of the metal fingers for the 4x4 mm² cell and two different designs for the 8x8 mm² cell. The percentage of metal shading is given under each design. Due to the limited number of devices with each metal pattern (4 for each of the 4x4 mm² designs and 2 for each of the 8x8 mm² designs), all devices of each size were characterized, regardless of the metal pattern. Due to this, some spread in the data is expected.
Fig. 2.6: Top layout of the metal fingers for the different cell sizes.

2.2.2 Process flow

The main steps of the process flow are illustrated in Fig. 2.7. The starting wafers were p-type Si wafers with a doping level of $2 \times 10^{16}$ cm$^{-3}$. Prior to epitaxial growth, the wafers were subjected to a standard RCA clean with a final HF dip (50:1 H$_2$O:HF). The final HF dip ensures the wafer surface is hydrogen-terminated which prevents surface oxidation while transferring the wafers into the epitaxial reactor.

The epitaxial layers were grown in a Low Pressure Chemical Vapor Deposition (LPCVD) system. Where existent (sample #4), a 1-µm-thick boron-doped layer was first grown at a doping level of $1 \times 10^{17}$ cm$^{-3}$ prior to emitter growth. The purpose of this layer is to move the PN-junction away from the wafer surface and possible imperfections and contamination which could affect the device performance. Emitter layers were then grown with the emitter thickness and doping shown in the split table (Fig. 2.5.b).
The front side of the epitaxially grown wafers was then coated with photoresist and the backside epi-layer was etched in LAM 490 plasma etching system. The photoresist was then stripped and re-applied for the subsequent mesa etch photolithography. The mesa was etched in AME5000 using Cl₂/HBr chemistry. The wafers were then cleaned in piranha (3:1 H₂SO₄:H₂O₂), followed by RCA clean, immediately prior to ARC deposition. This consisted of a 20-nm-thick thermal oxide that was first grown (30 min, dry oxidation, 950 °C), followed by 50 nm of LPCVD nitride (30 min, 775 °C). The wafers were then patterned to open windows for contact implantation. Phosphorus at an energy of 35 keV was implanted for the front contacts. Two boron implantations were done at energies 100 keV for the BSF and at 10 keV for the backside contacts. The implantation activation was done at 900 °C for 15 minutes.

The oxide was then etched from the contacts and metal was sputtered on the front and back side of the wafers. The top metal comprised of a 100 nm thick layer of titanium with a 1 µm thick layer of aluminum on top and the backside metal was a 1 µm thick layer of aluminum. The front
metal was then patterned and etched in the Applied Materials Rainbow plasma etching tool. A final forming-gas anneal (H₂/N₂) at 430 ºC was performed to improve the metal to silicon contact.

### 2.3 Characterization results

The solar cells were characterized at the Masdar Institute of Science and Technology by the Nayfeh group. The I-V characteristics were measured under 1 sun (AM1.5G) by solar sun simulator, IV5 model, from PV Measurements Inc. [25]. This system is composed of a light source and I-V measurement setup. Prior to device measurements, light intensity and uniformity were calibrated using a silicon reference cell. The External Quantum Efficiency (EQE) of the solar cells was measured by QEX10 Quantum Efficiency / Spectral Response (SR)/ Incident Photon to Current Conversion Efficiency (IPCE) Measurement System from PV Measurements Inc. The QEX10 system provides monochromatic probe light with 300 nm to 1100 nm wavelength range. Prior to every measurement, the Si photodiode was used for calibration of the setup. All measurements were done at room temperature.

Fig. 2.8 shows the impact of the emitter thickness on device parameters under 1 sun (AM1.5G) for emitter thicknesses of 0.5 µm and 1 µm and cell sizes of 4x4 mm² and 8x8 mm². The Vₘᵋ does not seem to be affected by the emitter thickness. The small difference of about 20 mV between the different cell sizes could be due to differences in the metal shading area, variations in the fabrication process, and/or a lack of a statistically significant sample range (4 devices with size 8x8 mm² and 12 devices with size 4x4 mm² were measured from each wafer).

There is a large spread in the Jₛₑ data for the thicker emitter due to the larger range of samples measured, but overall the current is not greatly affected by the emitter thickness. The fill factor
(FF) is also not affected by the emitter thickness either, however it does depend on the size of the cell. The FF describes the “square-ness” of the JV curve under illumination, which is reduced by increasing the series resistance of the cell. Smaller solar cells show higher FF due to their smaller resistance relative to their area. Overall, the emitter thickness for this particular doping (6×10\(^{18}\) cm\(^{-3}\)) does not seem to affect the device performance significantly. Since the minority carrier diffusion length at this doping level (6.5 µm) is much longer than both emitter thicknesses, this result is not surprising.

![Graph showing impact of emitter thickness on various parameters under 1 sun AM1.5G.](image)

**Fig. 2.8:** Impact of emitter thickness on \(V_{oc}\), \(J_{sc}\), FF and efficiency under 1 sun AM1.5G.

Fig. 2.9 shows the impact of emitter doping on device parameters for doping levels of 6×10\(^{18}\) cm\(^{-3}\) and 1.2×10\(^{19}\) cm\(^{-3}\) and for different cell sizes. The emitter doping is expected to affect the minority carrier diffusion length but even in the case of the higher doping level, the diffusion length is sufficiently long (3.5 µm) to allow carriers to reach the junction. The results shown in
Fig. 2.9 confirm that the emitter doping does not seem to affect most device parameters in a statistically significant way. The only somehow significant change is in $J_{sc}$ which could be explained by the lower recombination at the top surface due to the higher emitter doping. It must be noted that the increase in $J_{sc}$ is only noticeable for the 8x8 mm$^2$ cell and could be due to the large difference in the shading percentage for the two different cell designs (see Fig. 2.6) and the limited number of cells measured and therefore may not be statistically significant. In the case of the 4x4 mm$^2$ cells the efficiency increases by 4% mostly due to the contribution of the FF as the $J_{sc}$ change is less than 1%. The larger cells have higher marginally $V_{oc}$ but lower FF compared to the smaller cells resulting in similar efficiencies for two sizes.

![Graphs showing the impact of emitter doping on $V_{oc}$, $J_{sc}$, FF, and efficiency under 1 sun AM1.5G.](image)

**Fig. 2.9:** Impact of emitter doping on $V_{oc}$, $J_{sc}$, FF and efficiency under 1 sun AM1.5G.
Fig. 2.10 shows the effect of both the emitter thickness and doping on device parameters under 1 sun (AM1.5G) for cell sizes 4x4 mm$^2$ and 8x8 mm$^2$. As the doping is increased and the thickness is decreased, all device parameters deteriorate. $J_{sc}$ is reduced by up to 3.5%, $V_{oc}$ by up to 3.3%, FF by up to 2.4%, and the efficiency by up to 8.8%. It can be postulated that the thinner emitter brings carriers closer to the surface where they recombine before being collected by the pn junction. This reduces both $V_{oc}$ and $J_{sc}$. The change in the FF seems to be consistent with the difference in the sheet resistance for the three cases (77, 95 and 107 $\Omega/\square$ for emitter doping of $6\times10^{18}$, $1.2\times10^{19}$ and $2.5\times10^{16}$ cm$^{-3}$, respectively). As a result, the overall cell efficiency is also seen to decrease.

Fig. 2.11 shows the impact of the introduction of an epitaxial boron-doped layer on device parameters. Introduction of B-doped layer leads to a decrease of all device parameters: $J_{sc}$ – by up
to 4.4%, $V_{oc}$ - by up to 3.2%, FF - by 1%, Efficiency – by up to 9.8%. These results imply that the device parameters are more strongly affected by the p-type side, rather than the n-type side of the junction. The preeminence of base parameters is also consistent with the weak sensitivity to emitter parameters that we have noted in the previous paragraphs. The higher doping level on the p-type side seem to increase recombination hence damaging $J_{sc}$ and $V_{oc}$. This lowers the overall efficiency of the device.

Fig. 2.11: Impact of the presence of boron-doped layer on $V_{oc}$, $J_{sc}$, FF and efficiency (AM1.5G)

Fig. 2.12 shows the impact of the contact implants on device characteristics. With the addition of the contact implants, the contact resistance and therefore the total series resistance of the device is reduced. As a result the FF of the cells increases by 9.3%. In addition, recombination at the metal-semiconductor interfaces is also reduced. This results in increased $J_{sc}$ and $V_{oc}$. Altogether, the efficiency increases by a very significant 10%.
A summary of efficiency distribution for all six samples (refer to Fig. 2.5.b) is shown in Fig. 2.13. Sample 3 exhibits the maximum median efficiency and one of the cells in sample 2 has the maximum efficiency that has been measured. Both of these samples have emitter thickness of 1 µm and doping of $6 \times 10^{18}$ cm$^{-3}$. These are the values that were chosen for the optimal design that is further investigated in Ch. 3.
The resulting J-V characteristics of the optimal design (sample #3) are shown in Fig. 2.14.

**Fig. 2.14: J-V characteristics of the optimal emitter design (AM1.5G).**

### 2.4 Chapter summary

In this section, the design of a standalone Si solar cell was conducted. Simulations showed that base doping level between $5 \times 10^{16}$ and $1 \times 10^{17}$ cm$^{-3}$ was optimal for achieving high $V_{oc}$ and efficiency. A fabrication process was developed in which the emitter was grown by an epitaxial technique. The impact of emitter thickness and doping as well as the addition of boron-doped layer and contact implants were evaluated. The base design was shown to affect device performance to a larger extent than the emitter design. The optimal design had emitter thickness of 1 µm and doping of $6 \times 10^{18}$ cm$^{-3}$. This was the design that yielded the highest efficiency among all samples - 16.95%.
Chapter 3

Dislocations and Series resistance in SiGe/Si cells

In this chapter, two of the major concerns regarding the use of graded buffers in tandem solar cells will be addressed – creation of threading dislocations in the bottom cell and increased series resistance of the cells. As already described in Chapter 1, growing SiGe graded buffers on Si substrates may lead to threading dislocations being punched down into the Si sub-cell. These dislocations work as recombination centers and will likely increase the leakage current of the devices. Furthermore, growing thick SiGe buffers with high level of defects may lead to increased series resistance of the solar cells. This section aims to investigate the impact of growing SiGe layers on Si cells with respect to leakage current and series resistance by fabricating and characterizing device test structures.

3.1 Impact of dislocations

In this section the impact of the threading dislocations is quantified through the fabrication and characterization of diodes on Si wafers with and without prior SiGe growth. The leakage current of both types of structures is extracted and compared. The difference in leakage current is then related to the measured threading dislocation density (TDD) in both wafers.
3.1.1 Fabrication of the test structures

In an initial experiment performed by the Fitzgerald group, Si$_{0.4}$Ge$_{0.6}$ graded buffers were grown on Si substrates to evaluate the quality of the graded buffer growth. The growth was performed with ultra-high vacuum chemical vapor deposition (UHVCVD) reactor. The growth temperature and the growth rate of the graded buffers were 900°C and 10 %/µm, respectively. The structure was examined for threading dislocations via transmission electron microscopy (TEM).

Fig. 3.1 shows the cross-section of the structure and the TEM image with the Si$_{0.4}$Ge$_{0.6}$/Si interface indicated with an arrow. A dislocation, penetrating to a 1-µm depth into the Si substrate, is clearly visible in the image. Since all devices fabricated throughout this thesis have emitter thickness of 1 µm or smaller, it is essential to evaluate the extent to which these dislocations affect cell performance.

Fig. 3.1: TEM of a p-Si substrate with a SiGe buffer grown on top, showing the presence of dislocations in the Si (Wafers growths and TEM image courtesy of the Fitzgerald group).
In order to evaluate the impact of the dislocations on the leakage current, two device wafers were grown (Fig. 3.2). The starting wafers were p-type Si wafers with doping level of $2 \times 10^{16}$ cm$^{-3}$. The epitaxial layers were grown in a Low Pressure Chemical Vapor Deposition (LPCVD) system. A 1-µm p-type layer with target doping of $1 \times 10^{17}$ cm$^{-3}$ was initially grown to provide defect-free surface for subsequent emitter growth. N-type emitters were epitaxially grown on both wafers at 936°C and growth rate of 4 nm/sec to a thickness of 1 µm. Next, a Si$_{0.4}$Ge$_{0.6}$ graded buffer was grown on top of the Si emitter on only one of the wafers, also at 936°C. The Si$_{0.4}$Ge$_{0.6}$ buffer was linearly graded from 2 to 60% at a rate of 10%/µm, resulting in ~6 µm thick layer. Both the emitter and the buffer layer were doped in-situ with phosphorus to a doping level of $6 \times 10^{18}$ cm$^{-3}$.

A timed etch in Cl$_2$/HBr chemistry was used to etch through the entire SiGe thickness, down to the Si surface. A step height measurement was made to determine the etch depth. For this, photoresist was applied and patterned in one quarter of the wafer. Following this, the entire wafer was subjected to the etching process and the remaining step was measured. Subsequently, both wafers were processed into diodes, simultaneously, following the process flow described in Chapter 2. The cross-section and top view of the devices are shown in Fig. 3.3.

Fig. 3.2: Experiment to evaluate the effect of dislocations on the junction quality of the bottom cell. Wafers with and without prior SiGe growth were fabricated into devices. The wafers with prior SiGe growth are likely to have threading dislocations that penetrate into the p-n junction and increase the leakage current.
3.1.2 Leakage current extraction

Two different methods for leakage current extraction were explored. The first method employed linear fit of the device’s J-V curve, under reverse bias, as shown in Fig. 3.4. The intercept of this linear fit with the V=0 axis provides an estimate of the saturation current density, $J_s$. It must be noted that the extracted value represents the non-ideal component of the current due to the increased space-charge region recombination as a result of the defects in the semiconductor. The ideal component of the saturation current is not considered. One drawback of this method is that results depend on the range of values chosen for the linear fit. Selecting these values require that the curve be inspected to determine the start of the linear region. This process is often prone to error and thus hard to automate.
Fig. 3.4: Linear fit method for leakage current \((J_s)\) extraction.

The second method begins with the ideal diode equation:

\[
J = J_s \left( e^{\frac{qV_D}{nkT}} - 1 \right) \tag{3.1}
\]

where \(J\) is the total current density, \(J_s\) is the saturation current density, \(V_D\) is the voltage across the diode, \(q\) is the electron charge, \(k\) is Boltzmann constant, \(T\) is the temperature in K, and \(n\) is the ideality factor. For \(V_D\) close to zero a Taylor series expansion can be performed, resulting in:

\[
J = J_s \left( 1 + \frac{qV_D}{nkT} - 1 \right) = J_s \frac{qV_D}{nkT} \tag{3.2}
\]

Next, both sides are divided by \(V_D\) and the thermal voltage relation is used to achieve:

\[
\frac{J}{V_D} = \frac{J_s}{n\varphi_t} \tag{3.3}
\]

where \(\varphi_t = kT/q\) is the thermal voltage.

Eq. 3.3 shows that the conductance of the diode around \(V_D=0\) is a constant given by \(J_s/n\varphi_t\). This suggests a simple extraction process in which \(J/V_D\) is plotted as a function of voltage and \(J_s/n\).
is extracted at $V_D = 0$ V. An example is shown in Fig. 3.5. Indeed, we find that the conductance of the diode is a weakly dependent function of $V_D$ around $V_D = 0$. $J_s/n\phi_i$ is easily extracted.

It should be noted that unlike the linear fit method, the $J/V$ method gives the value of $J_s/n$ instead of $J_s$. Given that the ideality factor takes values between 1 and 2, it is not expected to greatly affect the final extracted value. Further, for this method, the first two data-points on both sides of $V_D = 0$ were used and the conductance was averaged. This makes the process easily automated and unambiguous. Selecting a greater number of data-points for the linear fit was found to have little effect on the results.

![Graph showing J/V method for leakage current (J_s) extraction.](image)

**Fig. 3.5: J/V method for leakage current ($J_s$) extraction.**

The leakage current extraction results using the two methods are compared in Fig. 3.6 for the Si wafer (no prior SiGe growth) for the different cell sizes. The linear fit method is represented by open symbols and the $J/V$ method by closed symbols. It can be seen that the two methods yield comparable results for all device sizes. However, since the $J/V$ technique presents reduced ambiguity this is the method that will be used moving forward.
Fig. 3.6: Comparison between the two methods for leakage current extraction for different device sizes for the Si wafer without prior SiGe growth. The open symbols represent the linear fit method and the closed symbols – the J/V method. Both methods yield similar results for all device sizes.

Fig. 3.7 shows the dark J-V characteristics for pn diodes on a Si wafer (no SiGe buffer) and SiGe wafer (SiGe buffer grown and etched) for 1x1 mm$^2$ device size. More than 20 devices were measured on each of the wafers. The SiGe/Si diodes (in blue) exhibit less ideal behavior compared to the Si devices (in red) which can be seen from the increased current in forward and reverse bias for $|V_D| < 0.5$ V. This behavior is consistent with increased recombination and generation in the space-charge region of the pn diode. As threading dislocations may trap impurities and create mid-gap traps, it is possible that the increased recombination is related to the presence of dislocations in the Si.

Fig. 3.8 shows the extracted leakage current spread for different cell sizes. The dots represent the median values of all measurements (~10 devices of each size). It can be seen that the leakage current of the SiGe wafers is at least 2 decades higher than that of the Si wafers.
Fig. 3.7: J/V characteristics for PN diodes in Si and SiGe wafers from different lots.

Fig. 3.8: Leakage current spread for PN diodes in Si and SiGe wafers from different lots. Diodes in the SiGe wafer show 2 decades higher leakage current

The two wafers shown in Figs. 3.7 and 3.8 were processed in different lots and that opens the possibility that the differences that are observed could be due to variations in the processing conditions. To eliminate this uncertainty, the experiment was repeated with two wafers being processed simultaneously.
Fig. 3.9 shows the J-V characteristics for pn diodes on a Si wafer (no SiGe buffer) and SiGe wafer (SiGe buffer grown and etched) from the same process lot (Lot 3). The characteristics of the SiGe/Si (in blue) and Si (in red) diodes have a similar non-ideal behavior in forward bias and slightly higher leakage current in reverse bias, indicating that the growth of SiGe buffer mostly affects carrier generation in the space-charge region.

![J/V characteristics for PN diodes in Si and SiGe wafers from the same lot.](image)

Fig. 3.10 shows the spread of the extracted leakage current for the two wafers from Lot 3. The leakage current of the diodes in the SiGe wafer was comparable to that measured in the devices from Lot 2. The leakage current of the diodes in the Si reference wafer, on the other hand, was higher than that of Lot 1 but still a decade lower than the diodes in the SiGe wafer. This result strongly suggests that dislocations or other defects have been formed in the Si substrate as a result of SiGe epitaxial growth. These defects clearly affect the leakage current of the devices.
Fig. 3.10: Leakage current spread for PN diodes in Si and SiGe wafers from the same lot. SiGe wafers show a median leakage current 10 times higher than the Si wafers.

3.1.3 Analysis of excess saturation current.

The leakage values shown in Fig. 3.10 represent the total leakage current from each device which is comprised of an area component as well as a perimeter component. The threading dislocation density (TDD), on the other hand, scales only with the area of the device. This requires a separation between the area and perimeter components of the saturation current in order to find the correlation between leakage current and TDD. The total saturation current was broken down into its area and perimeter components, according to:

\[ I_S = J_{SA}A + J_{SP}P \]  \hspace{1cm} (3.4)

where \( J_{SA} \) is the leakage current due to the area of the device and \( J_{SP} \) is the leakage current due to the perimeter of the device, \( A \) is the area and \( P \) is the perimeter of the device. Dividing the equation by the area of the device yields:

\[ J_S = J_{SA} + J_{SP} \frac{P}{A} \]  \hspace{1cm} (3.5)
When the saturation current density is plotted vs. P/A for a range of different size devices, the slope of the line corresponds to the perimeter component of the leakage current and the \( y \)-intercept corresponds to the area component. Fig. 3.11 shows the plots of \( J_S \) vs. P/A for both the Si sample with and without prior SiGe growth for all four device sizes (1x1, 2x2, 4x4, 8x8 mm\(^2\) with corresponding P/A ratios of 40, 20, 10, 5).

![Fig. 3.11: Perimeter/Area analysis of the leakage current for Si devices without (a) and with (b) prior SiGe growth. The high leakage current in the larger devices (8x8, 4x4 mm\(^2\)) lead to a negative slope and no solution for \( J_{SA} \) and \( J_{SP} \) components.](image-url)

It can be seen from the figure that the calculations including all four sizes lead to a negative slope of the trendline due to the unexpectedly high leakage current associated with the larger devices (4x4 and 8x8 mm\(^2\)). It can be speculated that another type of catastrophic defect might be present with very low density across the wafer. Such defects would affect the larger devices to a greater extent than the small devices and lead to increased leakage currents mostly in the larger devices. Due to the random nature of these defects, they do not scale with area and perimeter and would introduce an error to the analysis. Therefore only sizes 1x1 mm\(^2\) and 2x2 mm\(^2\) were used for the extraction of the parameters of interest.
Fig. 3.12 shows the $J_{\text{total}}$ as a function of $P/A$ ratio for the two sizes. It can be seen from the figure that the perimeter components for the devices with and without SiGe growth are similar. This perimeter leakage current is due to the excess generation and recombination at the mesa walls and it is expected to be similar for both devices as it scales only with periphery and is not related to TDD. The area component, on the other hand, is almost two decades higher in the devices with prior SiGe growth, suggesting higher TDD in these devices. In the next section, the TDD are extracted and compared to the area leakage current of the two types of devices.

![Fig. 3.12: Perimeter/Area analysis of the leakage current for Si devices without (a) and with (b) prior SiGe growth. The $J_{SP}$ parameter of both devices are similar, whereas the $J_{SA}$ component is almost 2 decades higher in the devices with the SiGe buffer growth.](image)

### 3.1.4 TDD extraction and correlation with the leakage current

TDD of the Si wafers with and without prior SiGe growth was quantified via Etch Pit Density (EPD) technique [26]. In the EPD technique, the sample is submerged in an etchant that preferentially attacks disruptions to the crystal structure. The etchant used in this experiment was the Schimmel etch: a solution of hydrofluoric acid, chromium trioxide and water (8g CrO$_3$, 200 ml HF, 250 ml H$_2$O) [27], [28]. The samples were etched for 2 minutes. Due to the difference in the etch rate between the substrate and the dislocation, pits are formed around the dislocations.
These pits were then observed and quantified in Nomarski microscope (Fig. 3.13). Threading dislocation density (TDD) was calculated as the number of pits divided by the observation area. Five images were taken on each of the two samples with average dislocations count of 395 per image for the Si wafer with prior SiGe growth and 4.5 per image for the Si wafer without prior SiGe growth. The viewing area was 240x190 µm².

Fig. 3.13: Etch pits seen in Si (left) and SiGe/Si (right) wafer after EPD. The circles in the photograph on the left indicate the location of the three dislocations found on the Si wafer.

Fig. 3.14: Threading dislocation densities of Si wafer with and without prior SiGe growth. The wafer with prior SiGe growth shows 2 decades higher TDD.

Fig. 3.14 graphs the TDD for the Si samples with and without prior SiGe growth. The samples with prior SiGe growth show almost 2 decades higher TDD. This confirms that the nearly two
order of magnitude higher area leakage component extracted from these devices (see Fig.3.12) is likely a result of the larger density of dislocations.

### 3.2 Series resistance in SiGe/Si structures

Another major concern that arises from the addition of SiGe buffer layers is the possibility of increased series resistance. The total series resistance measured between the terminals of the device is a sum of the emitter and base resistances, the contact resistance between the metal contact and the semiconductor, and the resistance of the top and rear metal contacts. Since the SiGe graded buffer will be added to the design in the final tandem cell, its contribution to the overall device resistance needs to be quantified.

In order to experimentally quantify the series resistance contribution of the SiGe buffer layer, the series resistance of devices with and without SiGe buffer were extracted and compared.

Fig. 3.15 shows the cross-section of the two wafer structures used in this study. The SiGe/Si wafer was fabricated specifically for this experiment. A Si control wafer was initially included in the same lot but it was damaged during the initial stages of the fabrication. This required the comparison to be done with a previously fabricated wafer that most closely matches the design of the SiGe/Si wafer. Both wafers have the same base and emitter design. Boron-doped Si wafers with a doping level of $2 \times 10^{16}$ cm$^{-3}$ were used for the base of the diodes. The emitters on both wafers were epitaxially grown to a thickness of 1 µm and in-situ doped with Phosphorus to a level of $6 \times 10^{18}$ cm$^{-3}$. The second wafer had an additional 2-60% linearly graded SiGe buffer layer grown on top of the Si emitter and was capped with 0.5 µm of Si$_{0.4}$Ge$_{0.6}$ (not shown). The cap provides a
higher quality surface for the subsequent layer growths and it is a standard step in all SiGe graded buffer growths. The emitters, the graded buffer and the SiGe cap were grown at 936°C.

In earlier experiments contacts were built directly onto the SiGe surface which resulted in very high contact resistance. Implantation was also attempted which did not improve the contact resistance, likely due to a non-optimized implant activation process. In the current experiment instead of contact implantation, two highly-doped contact layers were grown on top of the SiGe buffer. The 30-nm-thick 20% SiGe layer is used to create a surface on which the strained-Si cap could be grown. In order to achieve a quality Si-cap, without many defects, a low concentration of Ge must be used. For large Ge concentrations, the thickness of the Si-cap must be limited to prevent it from relaxing and creating defects. Both contact layers were grown at 680°C and doped with phosphorus to a doping level $2 \times 10^{19}$ cm$^{-3}$ to mimic the surface concentration expected as a result from the ion implantation. It must be noted that the SiGe/Si wafer was not subjected to a p+-back side implantation in order to simplify the fabrication process. This could potentially result in

![Fig. 3.15: Cross-section of the test wafers used for series resistance extraction. The n+ implantation in the Si control wafer was substituted for contact layer growth in the SiGe/Si wafer. No p+ implantation was performed on the SiGe/Si.](image-url)
higher overall series resistance for the SiGe/Si wafer and it must be taken into account when comparing the results from the two structures. It also must be noted that the two wafers had a slightly different mask design and the different shading areas must also be accounted for.

The I-V measurements were done on devices with sizes 1x1 mm$^2$, 4x4 mm$^2$, and 8x8 mm$^2$ as designs with similar shading area could be found for those sizes. The series resistance of the diodes was extracted from the J-V characteristics in forward bias, as shown in Fig. 3.16. A straight line was fitted to the curve at current close to 100 mA and the series resistance was calculated from the slope of the line. As the measurements reach compliance at 100 mA, each extraction was done manually for the points closest to the 100 mA point without reaching it.

![Fig. 3.16: Series resistance extraction methodology.](image)

Fig. 3.17 shows the series resistance extraction results for devices with area 1x1, 4x4 and 8x8 mm$^2$. The series resistance was normalized by the device area. There is no apparent difference between the Si and SiGe/Si devices of the same cell size. The larger devices in both cases exhibit higher series resistance.
Fig. 3.17: Series resistance extraction results for Si and SiGe/Si cells. There is no significant difference between Si and SiGe/Si cells. Larger cells exhibit higher series resistance.

Fig. 3.18: Mask design and shading percentage for each wafer and different sizes

In order to understand these results, Fig. 3.18 shows the different top metal designs used in the various samples with information on shading percentage for each cell size. The shading percentage is the ratio of top metal area to the total junction area. It can be seen that there are small differences in the shading for the SiGe/Si and Si cells but significant differences as the cell area changes. All this explains the results in Fig. 3.17. For larger shading percentages there is a larger metal area,
thus less contact resistance and as a result less total series resistance. These observations indicate that the SiGe graded buffer does not contribute to the overall series resistance of the cells.

### 3.3 Chapter summary

In this chapter, the impact of SiGe graded buffer growth on the performance of Si solar cells was evaluated with respect to leakage current and series resistance. Devices with and without prior SiGe growth were fabricated and it was shown that the SiGe growth increases the median leakage current of pn junction in the Si substrate by at least a decade, indicating possible increase in the threading dislocation density as a result of the SiGe buffer growth.

Furthermore, the series resistances of devices fabricated on a SiGe/Si wafer was extracted and compared to those of devices fabricated on a Si control wafer (without SiGe layer). There was no indication that the addition of the SiGe buffer negatively affected the series resistance of the solar cells.
Chapter 4

Optical absorption in SiGe graded buffers

4.1 Introduction

Chapter 1 motivated the use of SiGe graded buffers as a transition layer between the Si bottom cell and GaAsP top cell. SiGe allows the growth of GaAsP layers on Si with low threading dislocation densities (TDD). Low TDD ensures highest possible quality of the top cell and possibility of achieving the theoretical efficiency limit of 44.8% under AM1.5G.

One problem with utilizing SiGe as a transition layer between GaAsP and Si is that the narrow-bandgap SiGe will absorb most of the light intended for the Si sub-cell. This is expected to reduce the photo-generated current from the Si cell and the overall efficiency of the tandem cell. In the following sections we will explore the impact of the SiGe buffer layer on the optical absorption of the underlying Si cell and look into a step-cell design for increased photogeneration in the Si subcell.

4.2 Absorption in SiGe/Si cells

To evaluate the impact of SiGe buffer layers on the optical absorption of the bottom Si cell, two test structures were fabricated (Fig. 4.1). The silicon control structure is shown in Fig. 4.1a and it is similar to the optimized Si solar cell, presented in Chapter 2. The second structure shown in Fig. 4.1b has an additional SiGe buffer layer epitaxially grown on top of the Si emitter. Both
structures were fabricated using the process flow, described in Section 2.2. A timed etch in Cl₂/HBr plasma was used for the SiGe buffer layer etch. However, it should be noted that an additional photoresist-coated Si wafer was used to facilitate the measurement of the photoresist thickness after each etch step. The reason for that is that ellipsometry on wafers with multiple layers with different refractive indices can yield inconclusive results and an attempt to measure the photoresist thickness on top of the SiGe buffer would likely result in an error.

![Diagram](image)

**Fig. 4.1:** Test structures (a) with and (b) without SiGe graded buffer grown on top of the Si solar cell.

The fabricated devices were measured under AM1.5G spectrum at Masdar Institute of Science and Technology by Prof. Nayfeh’s group. The J/V characteristics are shown in Fig. 4.2. Adding the SiGe graded buffer leads to decrease in $J_{sc}$ from 33 mA/cm$^2$ to 6 mA/cm$^2$ which corresponds to a decrease in efficiency from 16% to 3%. This result is consistent with a simulation model that accounts for the optical losses in the SiGe layer, to be shown below in section 4.4. This result demonstrates the need to increase the current from the Si cell in order to enable its use in a high-efficiency tandem cell. The next section introduces a cell design intended to accomplish this.
Fig. 4.2: J/V characteristics of the cells shown in Fig. 4.1 under AM1.5G conditions. There is a decrease in the short-circuit current from 33 mA/cm² for the Si cell to 6 mA/cm² for the SiGe/Si cell.

4.3 Step-cell concept and design

One way to mitigate the impact of the SiGe layers is to use a step-cell design [29]. The concept of the step-cell design is illustrated in Fig. 4.3 for the complete GaAsP/Si cell. The top GaAsP cell and the SiGe graded buffer are partially etched to allow more light to reach the underlying Si sub-cell. The area of the remaining GaAsP and SiGe region is referred to as $A_{\text{top}}$ and the total cell area is referred to as $A_{\text{tot}}$. By increasing the $A_{\text{tot}}/A_{\text{top}}$ ratio, the $J_{\text{sc}}$ of the bottom cell and, in turn the overall tandem cell efficiency, should increase. Achieving maximum current from the Si cell is a critical step for the ultimate implementation into the GaAsP/Si tandem cell. It must be noted that as the area of the top cell is reduced, the efficiency of the top cell is reduced in exchange for a higher current from the bottom cell. It is then reasonable to expect an optimal $A_{\text{tot}}/A_{\text{top}}$ ratio past which the overall tandem cell efficiency decreases due to the loss of efficiency from the top cell.
To estimate the expected improvement over the conventional tandem cell, the GaAsP/SiGe/Si step-cell was initially simulated for different $A_{\text{tot}}/A_{\text{top}}$ ratios [30]. The 2D simulations were carried out using Sentaurus TCAD by Synopsys. A cross-section of the simulated structure is shown in Fig. 4.4. The Si solar cell has a 1 $\mu$m n$^+$- emitter doped at a level of $1 \times 10^{19}$ cm$^{-3}$. The linearly graded SiGe buffer was represented by six SiGe layers each 1-$\mu$m-thick with constant composition to simplify the model. The doping of the SiGe layers is also set to $1 \times 10^{19}$ cm$^{-3}$. The GaAs$_{0.71}$P$_{0.29}$ top cell has a 2-$\mu$m-thick p-type base and 100-nm-thick n-type emitter with doping levels of $1 \times 10^{18}$ cm$^{-3}$ and $5 \times 10^{18}$ cm$^{-3}$, respectively. A 70-nm-thick Si$_3$N$_4$ layer is used as anti-reflective coating (ARC). Complex refractive indices of GaAs$_{0.71}$P$_{0.29}$ were obtained by measurements of MOCVD-grown 2-$\mu$m-thick layers. Optical properties of other materials used in simulations were obtained from the Sopra website [31]. Lifetime, $\tau$, of Si was modeled as doping dependent with the intrinsic value set to 1 ms, as reported for high quality c-Si wafer [32]. A lifetime of 10 ns was chosen for both n- and p-GaAs$_{0.71}$P$_{0.29}$ which is consistent with values reported for epitaxial GaAs on SiGe graded buffers [33]. The bandgaps of GaAs$_{0.71}$P$_{0.29}$ and the different compositions of SiGe were
taken from [34] and [35] respectively. The tunnel junction between the two cells is simulated as a thin, highly conductive region. Optical and resistive losses in the tunnel junction were not considered. Interface surface recombination velocity was set to 1000 cm/s for the following interfaces: ARC/GaAsP emitter, GaAsP base/TD, 10% SiGe/Si emitter and ARC/Si emitter.

![Cross-section diagram](image)

**Fig. 4.4:** Cross-section of the simulated GaAs$_{0.71}$P$_{0.29}$/Si tandem step-cell with 0-60% SiGe buffer (reproduced from [10]).

The results for the simulated $J_{sc}$ and efficiency for the different $A_{tot}/A_{top}$ ratios are shown in Fig. 4.5. It can be observed from the plot that the optimum efficiency increases from $\sim$3% for the conventional tandem cell ($A_{tot}/A_{top}=1$) to a maximum of $\sim$23% for the step cell with a ratio $A_{tot}/A_{top}=1.3$.

In this section, a step-cell design was presented as means to increase the current from the bottom Si cell and compensate for the absorption of light in the thick SiGe layer. An absolute increase of 20% in efficiency can be achieved at the optimal $A_{tot}/A_{top}$ ratio of 1.3 using this the step-cell design. The following sections will focus on experimentally characterizing the impact of the narrow-bandgap SiGe overlayers on Si solar cell performance when using the step-cell
structure to alleviate the losses. The dependence of the solar cell characteristics ($V_{oc}$, $J_{sc}$, FF and efficiency) on the cell layout and cell size will be explored.

Fig. 4.5: Simulated Efficiency and $J_{sc}$ for 2 μm GaAs$_{0.71}$P$_{0.29}$/Si tandem step-cell with 0-60% SiGe buffer layer showing increase of the overall tandem cell efficiency when the Si bottom cell is partially exposed (reproduced from [30]).

4.4 Step-cell fabrication

4.4.1 Epitaxial growth

P-type Si wafers with resistivity of 0.6-0.8 Ω.cm are used as starting substrates. The epitaxial layers were grown in a Low Pressure Chemical Vapor Deposition (LPCVD) system. A 1-μm-thick boron-doped Si layer with doping level $10^{17}$ cm$^{-3}$ was first grown on all wafers in order to provide a defect-free interface for the P-N junction (not shown). A 1-μm-thick phosphorus-doped emitter was then grown at a doping level of $6\times10^{18}$ cm$^{-3}$. A 6-μm-thick graded SiGe buffer was then grown on top of the Si emitter with a starting concentration of 2% Ge and the percentage was linearly increased to a final composition of 60% Ge, to minimize the dislocations at the surface of the graded buffer [36][37]. A 500-nm-thick relaxed Si$_{0.4}$Ge$_{0.6}$ layer was grown on the graded
buffer to minimize the dislocations in the subsequently grown layers. To reduce series resistance, the graded buffer and the relaxed layer were in-situ doped with phosphorus to a nominal doping level of $6 \times 10^{18}$ cm$^{-3}$ during epitaxial growth. Finally, a set of contact layers consisting of 30-nm Si$_{0.8}$Ge$_{0.2}$ and 30-nm Si doped to $2 \times 10^{19}$ cm$^{-3}$ were grown to reduce the contact resistance of the aluminum to n-type SiGe layers that has been problematic in earlier experiments.

4.4.2 Device fabrication

The fabrication process of the step cells closely follows that of the Si bottom cell described in Chapter 2 with a few changes related to the double mesa etch that are going to be covered in this section.

The top and bottom mesas were etched in an AME5000 plasma etching system. Unlike the isolation mesa between the devices (bottom mesa), which could be substantially over-etched, the top mesa etch had to be precisely timed in order to stop at the Si emitter as soon as the SiGe layer is etched away. As the etch rate depends on the SiGe composition, step height measurements had to be done after every etch step and etch times had to be adjusted in accordance to the latest etch rate and the expected change in the rate. A photoresist-coated Si wafer was run through the same etch steps and used to estimate the photoresist thickness on the SiGe wafers. The photoresist thickness was measured via ellipsometry. The total step height was measured with a profilometer and the photoresist thickness was subtracted from the total height to estimate the etch depth. Due to the possible difference in the photoresist thickness between the Si wafer and the SiGe wafer and measurement errors of both tools, the etch depth was underestimated. That led to final Si emitter thickness in the exposed areas from 0.7-0.9 µm of the designed 1 µm.
Anti-reflection coating consisting of 30-nm-thick low-temperature oxide (LTO) and 50-nm-thick LPCVD nitride was then deposited. Ti/Al (50 nm/500 nm) was deposited on the front side of the wafers and etched in Cl₂/BCl₃ plasma to form the top contacts of the solar cells. A backside contact was formed via deposition of 1 µm Al. Finally, a 30-min sinter anneal was performed at 420 °C in H₂/N₂ ambient. The final structure of the device as well as the process flow are shown in Fig. 4.6. The changes made to the Si-cell process, presented in chapter 2, are reflected in the figure.

![Cross-section and process flow for the step cell.](image)

4.4.3 Cell layout

Fig. 4.7 shows the layout of the two different step-cell designs used in this work. The standard design uses a rectangular-shaped mesa. In an attempt to reduce the series resistance, a finger mesa design was also explored. The finger design allows for longer metal fingers and shorter path...
through the thick SiGe buffer layer for electrons generated in the Si between the fingers. The top mesa in both designs defines the area of the SiGe layer. The bottom mesa defines the total area of the cell. The finger cells have an $A_{\text{tot}}/A_{\text{top}}$ ratio varying from 1.2 to 2 and the rectangular cells – from 1 to 2. Cells with total bottom area of 4 mm x 4 mm and 8 mm x 8 mm were characterized in this work.

![Diagram of solar cell designs](image)

**Fig. 4.7**: Mask layout of the solar cells. The $A_{\text{tot}}/A_{\text{top}}$ ratio was varied from 1 to 2 for the rectangular and from 1.2 to 2 for the finger design.

### 4.5 Step-cell characterization

Fabricated solar cells were measured at 1 sun with AM1.5G standard by solar sun simulator, IV5 model, from PV Measurements Inc. [25]. This system is composed of the light source and the measurement equipment needed to measure I-V curves for solar cells up to 5 cm × 5 cm. Light intensity and uniformity are calibrated using silicon reference cell and irradiance monitor. Furthermore, External Quantum Efficiency (EQE) of solar cells was measured by QEX10 Quantum Efficiency / Spectral Response (SR)/ Incident Photon to Current Conversion Efficiency (IPCE) Measurement System from PV Measurements Inc. The QEX10 system uses a xenon arc
lamp source, monochromator, filters and reflective optics to provide stable monochromatic light. Prior to every measurement, the Si photodiode is used for calibration of the setup.

Fig. 4.8 shows the measured J-V characteristics of SiGe/Si step cells with rectangular design for different $A_{\text{tot}}/A_{\text{top}}$ ratios under 1 sun conditions. The short-circuit current increases from 7 mA/cm$^2$ to 20 mA/cm$^2$ with increasing the $A_{\text{tot}}/A_{\text{top}}$ ratio from 1 to 2, demonstrating the promise of the step-cell design in increasing the overall cell efficiency.

The measured short-circuit current was compared to 2D simulations with Sentaurus TCAD by Synopsys (reported in [30] and reproduced in Fig. 4.9). The same model as the one described in section 4.3 was used for the Si sub-cell and the SiGe buffer layer - 1-μm-thick Si emitter, 6 μm SiGe buffer modeled as six 1-μm-thick layers with uniform composition. The doping of all layers was set to n-type and doping density of 1x10$^{19}$ cm$^{-3}$. The experimental curve represents the measured median values for each $A_{\text{tot}}/A_{\text{top}}$ ratio. The median values were calculated based on
measurements from 7 devices for each $A_{\text{tot}}/A_{\text{top}}$ ratio. As a reference, the values for an $A_{\text{tot}}/A_{\text{top}}$ ratio taken to infinity (i.e. no top cell) are also given. The measured short-circuit current is in a good agreement with the simulations for all $A_{\text{tot}}/A_{\text{top}}$ ratios considered.

![Graph showing measured and simulated $J_{sc}$ of SiGe/Si solar cells for different $A_{\text{tot}}/A_{\text{top}}$ ratios. The $J_{sc}$ values for $A_{\text{tot}}/A_{\text{top}}$ going towards infinity (i.e. no top cell) are also given.]

**Fig. 4.9:** Measured and simulated $J_{sc}$ of SiGe/Si solar cells for different $A_{\text{tot}}/A_{\text{top}}$ ratios. The $J_{sc}$ values for $A_{\text{tot}}/A_{\text{top}}$ going towards infinity (i.e. no top cell) are also given.

Fig. 4.10 shows the effect of the mesa design on the J-V characteristics. Figures 4.10a and 4.10b show the J-V characteristics of 8 mm x 8 mm cells for different $A_{\text{tot}}/A_{\text{top}}$ ratios for finger and rectangular designs, respectively. As expected, the finger design shows better fill factor (FF) compared to the rectangular design, likely due to the lower series resistance.

Fig. 4.11 shows the impact of the mesa design on all device parameters under illumination, for different $A_{\text{tot}}/A_{\text{top}}$ ratios. With the use of finger design and by increasing the $A_{\text{tot}}/A_{\text{top}}$ ratio, the average path to the metal fingers is reduced and therefore the chance of recombination events taking place also decreases. This in turn leads to higher $V_{oc}$ for the devices with finger design and with higher $A_{\text{tot}}/A_{\text{top}}$ ratios. The FF is also higher in the devices with finger mesa design, likely
due to its smaller series resistance. As the $A_{\text{top}}/A_{\text{tot}}$ ratio increases, the area of the exposed Si and the chance of light collection and photo-generation also increases, leading to an increase in $J_{\text{sc}}$. As a result of the increased $V_{\text{oc}}$ and FF, efficiency of the finger design also increases in comparison with the rectangular design.

![Fig. 4.10: J-V characteristics of SiGe/Si cells with rectangular and finger layout of the top (SiGe) mesa under 1 sun illumination (AM1.5G). The finger design improves the fill factor of the cells.](image1)

![Fig. 4.11: Impact of mesa design and step-cell area ratios on device characteristics under AM1.5G. The finger design improves $V_{\text{oc}}$, FF and efficiency.](image2)
Fig. 4.12 shows the J-V characteristics of 8 mm x 8 mm (a) and 4 mm x 4 mm (b) cells with finger design. The smaller cells show better fill factor compared to the larger ones, likely due to the lower series resistance.

Fig. 4.12: J-V characteristics of finger SiGe/Si cells with different areas under 1 sun illumination (AM1.5G). The smaller cells show better fill factor.

Fig. 4.13 shows the impact of the cell size on all device parameters under illumination, for different $A_{tot}/A_{top}$ ratios in mesa design cells. The larger cells, as it was already shown in chapter 3, have higher leakage current, leading to decrease in $V_{oc}$. The series resistance of the larger cells is also higher, leading to lower FF. The decrease in both FF and $V_{oc}$ results in lower efficiency of the larger cells.

Overall, the step-cell design was proven beneficial in achieving a larger short-circuit current compared to that of a solar cell that utilizes a full graded buffer. In addition, the mesa design was shown to impact the $V_{oc}$, FF and efficiency with the finger mesa design outperforming the rectangular design. Next, the spectral response of the step cells for different $A_{tot}/A_{top}$ ratios will be examined to fully characterize the impact of the step-cell.
Fig. 4.13: Impact of cell size on characteristics of mesa design devices under AM1.5G. The smaller size has higher V$_{oc}$, FF and efficiency.

4.6 Spectral response of step cells

The step-cell design of the SiGe/Si solar cell was introduced to reduce the absorption of the SiGe layer. The benefits of the step-cell design have been demonstrated with regards to short-circuit current. This section will compare the spectral response of SiGe step-cells to that of a full buffer layer. Measuring the spectral response of the cells provides detailed information on which wavelengths are absorbed by the SiGe buffer and how the responsivity of the solar cell improves by introducing the step-cell concept.
Measuring the spectral response of the step-cells proved to be challenging due to their varying topography with specific SiGe-to-Si area ratios. In order to compare the effect of the different step-cell area ratios on quantum efficiency, uniform illumination across the cell is required. This provides all regions of the cell with the same photon input and facilitates comparison between different cells. However, due to the difficulty of adjusting the size of the photon beam to the exact area of the cell, the measurements were done with certain amount of photon “spillover”, as illustrated in Fig. 4.14 (a). Under these conditions, measured external quantum efficiency (EQE) values are underestimated as some incident photons are lost in the area surrounding the cell, but the effect of the $A_{\text{tot}}/A_{\text{top}}$ ratio is preserved. Therefore, normalized values of the EQE are used to show proof of concept, rather than the actual EQE values. All data points were normalized by the absolute maximum of the EQE for a design with $A_{\text{tot}}/A_{\text{top}} = 2$. The maximum occurred at $\lambda \sim 900$ nm.

The effect of the step-cell design on the normalized EQE is shown in Fig. 4.14 (b) for rectangular cells. The wavelengths, corresponding to the bandgaps of Si and SiGe are indicated in the figure. It can be noted that the short wavelengths are entirely absorbed by the SiGe layer at $A_{\text{tot}}/A_{\text{top}}$ ratio of 1 (no exposed Si). This is indicated by the lack of optical response for wavelengths of 300 to 600 nm. Photons with longer wavelengths, however, can travel deeper into the material, before getting absorbed. The measurements indicate that above 700 nm some light is able to reach the underlying Si cell and get collected by the junction, increasing the response in the range 700-1100 nm. As the area of the exposed Si increases ($A_{\text{tot}}/A_{\text{top}} > 1$), both short and long wavelengths reach the silicon and as a result the maximum EQE also increases. These results show the potential of the step-cell design in increasing the overall EQE. Thinning down the SiGe buffer layer in addition to the use of the step-cell design is likely to improve the efficiency even further.
4.7 Chapter Summary

In this chapter we explored the impact of narrow-bandgap SiGe overlayers on Si solar cells for a step-cell design. We first show that introducing a SiGe overlayer drastically cuts down on short-circuit current and efficiency of the bottom Si solar cell in a tandem cell design. With a step-cell design, the short circuit current increased from 5 to 20 mA/cm$^2$ when the $A_{\text{tot}}/A_{\text{top}}$ ratio increased from 1 to 2. The response at short wavelengths and as a consequence the overall EQE was also shown to increase with increasing area of the exposed Si. These results demonstrate that the step-cell design is effective in increasing the current of the Si sub-cell and therefore improving the overall efficiency.
Chapter 5

Spectral absorption analysis for Si, GaAsP/Si and GaAsP/SiGe/Si solar cells

In the previous chapter, the impact of SiGe buffer on the electrical and optical characteristics of the underlying Si cell was explored. The SiGe buffer was shown to filter out a significant portion of the incoming light and reduce both $J_{sc}$ and EQE of the Si solar cell. The introduction of the step-cell design improved the characteristics of the SiGe/Si stack to some extent. To better understand the impact the SiGe layer would have on a tandem cell, the absorption of a hypothetical GaAsP/Si cell fabricated by bonding (no SiGe buffer layer) was modeled and compared to the single-junction Si cell and the GaAsP/SiGe/Si cell. The step-cell design was also modeled, as a linear combination of GaAsP/SiGe/Si cell and Si cell. The goal of this analysis is to help determine if the step-cell design is able to compensate for the opacity of the SiGe layer or if a bonded structure is the only viable option for high-efficiency GaAsP/Si cells.

5.1 Light absorption calculations

The spectral irradiance as a function of photon wavelength is the most common way of characterizing a light source. This will be used throughout this chapter for comparison between the different solar cell structures. For the calculations in this chapter, AM1.5G spectrum was used as the input solar spectrum [38]. This is shown in Fig 5.1.
To facilitate comparison between the different graphs and modeled structures, the integrated irradiance over the wavelength range of interest will be used throughout this section. This results in a single number in the units for power density (W/m²). Integrating the irradiance over the wavelength range of 300 to 2500 nm results in a spectral power density of $P_{\text{AM1.5G}}$ of 992.6 W/m².

![Graph showing spectral irradiance for AM1.5G spectrum. Integrating the spectral irradiance yields spectral power density $P_{\text{AM1.5G}}$ of 992.6 W/m².](image)

Fig. 5.1: Spectral irradiance for AM1.5G spectrum. Integrating the spectral irradiance yields spectral power density $P_{\text{AM1.5G}}$ of 992.6 W/m².

Figure 5.2 shows the breakdown of the input solar spectrum upon a contact with a solar cell. A fraction of the spectrum will be absorbed and a fraction will be transmitted through the material. The use of total absorption and transmission is necessary when calculating the available spectrum after the light passes through a given sub-cell. This provides the total input spectrum for the subsequent sub-cells, if any. Some of the absorbed light can be converted into useful energy (usable spectrum) by the solar cell. However, not all of the absorbed light is converted into useful energy, as shown in the diagram in Fig. 5.2. The fraction of the light that can be converted into energy is captured by the usable irradiance. The usable irradiance can be calculated from the total
absorbed irradiance after the thermalization losses have been accounted for. As already mentioned in chapter 1, thermalization losses are due to the inefficient absorption of photons with energy significantly higher than the bandgap of the material. Only, at most, a bandgap’s worth of energy can be extracted from these photons with the rest being dissipated as heat. Besides the thermal losses there may also be other losses, like those related to sub-bandgap absorption in GaAsP that need to be accounted for. These are also noted in Fig. 5.2.

![Diagram](image)

**Fig. 5.2:** Breakdown of input solar spectrum indicating the absorbed and the transmitted portions. The absorbed spectrum consists of a usable fraction and losses (thermal and sub-bandgap losses). The corresponding notations for the irradiance (F) and the power density (P) associated with each spectrum are also shown.

In order to calculate the fraction of the spectrum absorbed by a given multi-junction cell, the absorbed and transmitted irradiance must be calculated for each of the sub-cells.

The absorbed irradiance in a sub-cell of a given material, can be calculated using the Beer-Lambert law:

$$F_{abs}(\lambda) = F_{in}(\lambda) \left(1 - e^{-\alpha_M(\lambda)x_M}\right)$$  \hspace{1cm} (5.1)

where $F_{abs}$ is the absorbed irradiance for the given wavelength, $F_{in}$ is the input irradiance, $\alpha_M$ is the absorption coefficient of the material and $x_M$ is the total thickness of the sub-cell of given material.
The expression assumes uniform material properties. It must be noted that the total absorbed irradiance from equation 5.1 includes thermal losses and sub-bandgap losses, when the latter are present.

The solar irradiance that is transmitted through the material is then given by:

\[
F_{\text{trans}}(\lambda) = F_{\text{in}}(\lambda) - F_{\text{abs}}(\lambda) = F_{\text{in}}(\lambda)e^{-\alpha_M(\lambda)x_M}
\]  

(5.2)

The usable irradiance is a fraction of the absorbed irradiance. Only a bandgap worth of energy can at most be converted to electrical power (for \(E_{\text{ph}}>E_g\)) is:

\[
F_{\text{usable}}(\lambda < \lambda_g) = F_{\text{abs}}(\lambda < \lambda_g) \frac{E_g}{E_{\text{ph}}(\lambda < \lambda_g)} = \\
= F_{\text{in}}(\lambda < \lambda_g) \frac{E_g}{E_{\text{ph}}(\lambda < \lambda_g)}(1 - e^{-\alpha_M(\lambda<\lambda_g)x_M})
\]  

(5.3)

where \(E_g\) is the bandgap of the material and \(E_{\text{ph}}(\lambda)\) is the photon energy at the particular wavelength and \(\lambda_g\) is the wavelength, corresponding to the material’s bandgap. This means that only a fraction of the solar spectrum can be converted into usable energy by a given single-junction solar cell.

The rest of the absorbed irradiance is dissipated in the form of heat:

\[
F_{\text{thermal}}(\lambda < \lambda_g) = F_{\text{abs}}(\lambda < \lambda_g) - F_{\text{usable}}(\lambda < \lambda_g) = \\
= F_{\text{in}}(\lambda < \lambda_g) \left(1 - \frac{E_g}{E_{\text{ph}}(\lambda < \lambda_g)}\right)(1 - e^{-\alpha_M(\lambda<\lambda_g)x_M})
\]  

(5.4)

The sub-bandgap absorption can be expressed as:

\[
F_{\text{sub}}(\lambda) = F_{\text{abs}}(\lambda > \lambda_g) = F_{\text{in}}(\lambda > \lambda_g)(1 - e^{-\alpha_M(\lambda>\lambda_g)x_M})
\]  

(5.5)
In the following sections three main device structures will be analyzed with respect to light absorption efficiency – Silicon single-junction case, GaAsP/Si (bonded case) and GaAsP/SiGe/Si case. Finally, the step-cell design as a linear combination of the GaAsP/SiGe/Si and Si SJ cell will also be presented.

5.2 Absorption in Single-Junction Si solar cell

The single-junction Si cell was modeled as a 600-μm-thick Si wafer assuming an ideal anti-reflection coating (no reflection losses). The thickness was chosen based on the calculated diffusion length in the base of the solar cell at a doping level of 2x10^{-16} cm^{-3}. The absorption coefficient as a function of the wavelength was taken from the SOPRA website [31]. The missing values for the absorption coefficient were found as a linear interpolation between any given two points. The usable power density (P_{usable_Si}), which is the integral of the usable spectral irradiance, was then calculated from the input AM1.5G spectral irradiance, according to:

\[ P_{usable_Si} = \int_0^{\lambda_g} F_{usable_Si}(\lambda) d\lambda = E_{g, Si} \int_0^{\lambda_g} \frac{F_{AM1.5G}(\lambda)}{E_{ph}(\lambda)} \left(1 - e^{-\alpha_{Si}(\lambda) x_{Si}}\right) d\lambda \]  \hspace{1cm} (5.6)

Fig. 5.3 shows the cross-section of the structure and the input AM1.5G irradiance F_{AM1.5G} and usable irradiance F_{usable_Si}. The usable power density P_{usable_Si} is 467.7 W/m² which translates into 47.1% of the power density of the AM1.5G spectrum in the wavelength range of interest P_{AM1.5G} (992.6 W/m², as determined above).
The thermalization losses in the Si cell were calculated according to:

\[
P_{\text{thermal, Si}} = \int_0^\lambda g F_{\text{thermal, Si}}(\lambda) d\lambda =
\]

\[
= \int_0^\lambda g F_{\text{AM1.5G}}(\lambda) \left(1 - \frac{E_{g,\text{Si}}}{E_{\text{ph}}(\lambda)}\right) \left(1 - e^{-\alpha_{\text{Si}}(\lambda)x_{\text{Si}}}\right) d\lambda
\]

Integrating the equation above yielded thermal losses for the Si single-junction cell of 316.6 W/m².

The transmission losses were calculated using:

\[
P_{\text{trans, Si}} = P_{\text{AM1.5G}} - P_{\text{abs}} = P_{\text{AM1.5G}} - P_{\text{usable, Si}} - P_{\text{thermal, Si}}
\]

The transmission losses account for 208.3 W/m² of the solar spectrum.
Adding GaAsP as a top cell is expected to decrease the thermalization losses and increase the light absorption compared to the Si cell. In the following sub-section a similar analysis is performed for GaAsP/Si dual-junction cell.

### 5.3 Absorption in GaAsP/Si cell

The following model refers to a hypothetical bonded GaAsP/Si structure without any interfacial layers contributing to the optical or electrical losses between the two cells. The calculation of the absorption in the GaAsP/Si cell was performed in two steps. First, the absorbed and transmitted portions of the spectral irradiance was calculated for the GaAsP cell. The transmitted portion was then used as the input for the Si sub-cell. The model assumes ideal ARC and no reflection losses at material interfaces.

The usable irradiance was calculated from input AM1.5G spectrum according to:

\[
P_{usable_{GaAsP}} = \int_{0}^{\lambda_{g,GaAsP}} F_{usable_{GaAsP}}(\lambda) d\lambda =
\]

\[
= E_{g,GaAsP} \int_{0}^{\lambda_{g,GaAsP}} \frac{F_{AM1.5G}(\lambda)}{E_{ph}(\lambda)} (1 - e^{-\alpha_{GaAsP}(\lambda) x_{GaAsP}}) d\lambda
\]

(5.9)

Fig. 5.4 shows the usable irradiance \( F_{usable_{GaAsP}} \) for a 1.2-\( \mu \)m-thick GaAs\(_{0.77}\)P\(_{0.23}\) cell (\( E_g=1.7 \) eV). The absorption coefficient of the GaAs\(_{0.77}\)P\(_{0.23}\) as a function of wavelength was experimentally determined by Milakovich [21] and used in this model. The calculated power density \( P_{usable_{GaAsP}} \) is 373.3 W/m\(^2\).
Fig. 5.4: The fraction of the AM1.5 spectrum that can be converted into a usable energy by the GaAsP cell and the actual absorbed portion of it. Total useful absorbed power density 373.3 W/m$^2$ (37.6 % of the power density of the available AM1.5G spectrum)

The thermalization losses in the GaAsP cell were calculated according to:

$$P_{thermal_{GaAsP}} = \int_0^{\lambda_{g, GaAsP}} F_{thermal_{GaAsP}}(\lambda) d\lambda =$$

$$= \int_0^{\lambda_{g, GaAsP}} F_{AM1.5G}(\lambda) \left( 1 - \frac{E_{g, GaAsP}}{E_{ph}(\lambda)} \right) \left( 1 - e^{-\alpha_{GaAsP}(\lambda) x_{GaAsP}} \right) d\lambda$$  \(5.10\)

Integrating the equation above yielded thermal losses for the GaAsP top cell of 128.7 W/m$^2$.

The GaAsP has been shown to have sub-bandgap absorption [21] which does not contribute to the useful energy of the GaAsP cell but is also no longer available for the next cell and must be subtracted. The sub-bandgap absorption losses were calculated using:
\[ P_{sub_{GaAsP}}(\lambda) = P_{abs_{GaAsP}}(\lambda > \lambda_g) = \]
\[ = \int_{\lambda_g, GaAsP}^{\infty} F_{AM1.5G}(\lambda > \lambda_g) \left( 1 - e^{-a_{GaAsP}(\lambda > \lambda_g)x_{GaAsP}} \right) d\lambda \tag{5.11} \]

These sub-bandgap losses accounted for 32.1 W/m².

The irradiance not absorbed in the GaAsP cell will be transmitted through the cell and used as the input spectrum for the Si sub-cell.

\[ F_{trans_{GaAsP}}(\lambda) = F_{in_{Si}}(\lambda) = F_{AM1.5G}(\lambda)e^{-a_{GaAsP}(\lambda)x_{GaAsP}} \tag{5.12} \]

It must be noted that this expression is equivalent to subtracting the total absorbed irradiance in the GaAsP cell from the AM1.5G spectrum. The absorbed irradiance in the GaAsP cell includes thermalization and sub-bandgap absorption losses in addition to the usable irradiance (see Fig. 5.2). Even though the irradiance associated with these two loss components does not contribute to the usable irradiance of the GaAsP cell, it must be subtracted from the available spectrum for the next cell as it is still absorbed in the GaAsP.

The usable irradiance in the Si cell was then calculated according to:

\[ P_{usable_{Si}} = \int_{0}^{\lambda_{g, Si}} F_{usable_{Si}}(\lambda) d\lambda = \]
\[ = E_{g, Si} \int_{0}^{\lambda_{g, Si}} \frac{F_{trans_{GaAsP}}(\lambda)}{E_{ph}(\lambda)} \left( 1 - e^{-a_{Si}(\lambda)x_{Si}} \right) d\lambda \tag{5.13} \]

This yields a usable power density of 200.1 W/m².

The thermalization losses in the Si sub-cell were calculated according to:
\[ P_{thermal\_Si} = \int_{\lambda_{g,\text{Si}}}^{\lambda_{g,\text{Si}}} F_{thermal\_Si}(\lambda) d\lambda = \]

\[ = \int_{0}^{\lambda_{g,\text{Si}}} F_{trans\_GaAsP}(\lambda) \left( 1 - \frac{E_{g,\text{Si}}}{E_{\text{ph}}(\lambda)} \right) \left( 1 - e^{-\sigma_{Si}(\lambda) x_{Si}} \right) d\lambda \]  \hspace{1cm} (5.14)

Integrating the equation above yielded thermal losses for the Si sub-cell of 50.1 W/m².

The transmission losses were calculated using:

\[ P_{trans\_Si} = P_{trans\_GaAsP} - P_{abs\_Si} = P_{trans\_GaAsP} - P_{usable\_Si} - P_{thermal\_Si} \]  \hspace{1cm} (5.15)

The transmission losses account for 208.3 W/m².

Fig. 5.5 shows the transmitted irradiance through the GaAsP cell \( F_{trans\_GaAsP} \) and the usable irradiance of the Si sub-cell \( F_{usable\_Si} \), accounting for thermalization losses in the Si. The calculated usable power density of the Si sub-cell \( P_{usable\_Si} \) is 200.1 W/m² which is 20.9% of the power density of available AM1.5G spectrum \( P_{AM1.5G} \).

![Figure 5.5: Total solar spectrum transmitted through the GaAsP cell and fraction absorbed in the Si sub-cell. The usable power density \( P_{usable\_Si} \) is 200.1 W/m² (20.9% of the power density of the AM1.5G spectrum).](image)
The usable irradiance of the GaAsP and the Si cell was then added and the result is plotted in Fig. 5.6. The two curves result in a total usable power density of 573.4 W/m² which represents 57.8% of the total AM1.5G spectrum and it is 22.6% improvement over the single-junction Si cell, modeled in section 5.2.

![Absorbed spectral irradiance in bonded GaAsP/Si cell](image)

This result suggests that integration of GaAsP on Si is advantageous with respect to increasing the absorption and therefore the efficiency of the solar cell compared to Si single-junction cells. Next, the impact of adding a SiGe buffer layer between the two sub-cells is presented.

### 5.4 Absorption in GaAsP/SiGe/Si cell

The calculation of the absorption in the GaAsP/SiGe/Si cell was performed in three steps, following the same procedure used for the modeling of the absorption in the tandem cell in section
5.3. The transmitted light from one cell is used as an input for the next cell and all absorbed light from each cell is added together.

The GaAsP cell and the absorbed and transmitted light through it was modeled as outlined in previous section.

The 6-μm-thick Si$_{0.4}$Ge$_{0.6}$ graded buffer was modeled as a discrete stack of 200-nm-thick layers of SiGe with changing composition by 2%. The absorption coefficient for each discrete composition was calculated by interpolation from the measured absorption coefficients of a few known concentrations in the literature for relaxed SiGe (11%, 22%, 39%, 51% and 64% SiGe) [31]. The absorbed spectral irradiance at each wavelength was calculated from the irradiance transmitted through the GaAsP cell, according to:

$$F_{abs_{SiGe}}(\lambda) = F_{trans_{GaAsP}}(\lambda) \left(1 - \prod_{i=1}^{30} e^{-\alpha_{SiGe,i}(\lambda) x_{SiGe}}\right)$$  \hspace{1cm} (5.16)

where $\alpha_{SiGe,i}$ is the i-th layer comprising the SiGe stack, $x_{SiGe}$ is the thickness of each layer – 200 nm and i=30 is the number of layers.

The absorbed solar irradiance in the SiGe layer is shown in Fig. 5.7. This irradiance is assumed to be lost due to the very high recombination in the crystallographic defects in addition to its large thickness and heavy doping. The power density of the losses in the SiGe buffer layer was calculated by integrating the irradiance from eq. 5.16:

$$P_{abs_{SiGe}} = \int_{0}^{\lambda_{g,SiGe}} F_{abs_{SiGe}}(\lambda)d\lambda$$  \hspace{1cm} (5.17)

This results in a total absorbed power density in the SiGe buffer layer of 152.7 W/m$^2$. 
Fig. 5.7: Total available solar spectrum transmitted through the GaAsP cell and fraction lost in the SiGe buffer layer. Total power density loss 152.7 W/m² (15.4% of the power density of the available AM1.5G spectrum)

The irradiance transmitted through the buffer was used as the input spectrum for the Si sub-cell and was calculated according to:

\[ F_{\text{trans, SiGe}}(\lambda) = F_{\text{in, Si}}(\lambda) = F_{\text{trans, GaAsP}}(\lambda) \prod_{i=1}^{30} e^{-\alpha_{\text{SiGe,}i}(\lambda) x_{\text{SiGe}}} \]  

(5.18)

By integrating equation 5.18, the total transmitted power density through the SiGe was calculated:

\[ P_{\text{trans, SiGe}} = \int_{0}^{\lambda_{\text{SiGe}}} F_{\text{trans, SiGe}}(\lambda) d\lambda = \]  

\[ = \int_{0}^{\lambda_{\text{SiGe}}} F_{\text{trans, GaAsP}}(\lambda) \prod_{i=1}^{30} e^{-\alpha_{\text{SiGe,}i}(\lambda) x_{\text{SiGe}}} d\lambda \]  

(5.19)
$P_{\text{trans}_{\text{SiGe}}}$ is 305.8 W/m$^2$ and it was used as the input power density for the Si sub-cell.

The thermalization losses in the Si sub-cell were first calculated according to:

$$P_{\text{thermal}_{\text{Si}}} = \int_{0}^{\lambda_{g,\text{SiGe}}} F_{\text{thermal}_{\text{Si}}} (\lambda) d\lambda =$$

$$= \int_{0}^{\lambda_{g,\text{SiGe}}} F_{\text{trans}_{\text{SiGe}}} (\lambda) \left( 1 - \frac{E_{g,\text{Si}}}{E_{ph}(\lambda)} \right) \left( 1 - e^{-\alpha_{\text{SiGe}}(\lambda)x_{\text{SiGe}}} \right) d\lambda \quad (5.20)$$

Integrating the equation above yields thermal losses for the Si sub-cell of 13.5 W/m$^2$.

The usable irradiance in the Si cell, accounting for thermalization and transmission was calculated using:

$$P_{\text{usable}_{\text{Si}}} = \int_{0}^{\lambda_{g,\text{Si}}} F_{\text{usable}_{\text{Si}}} (\lambda) d\lambda = E_{g,\text{Si}} \int_{0}^{\lambda_{g,\text{Si}}} \frac{F_{\text{trans}_{\text{SiGe}}} (\lambda)}{E_{ph}(\lambda)} \left( 1 - e^{-\alpha_{\text{Si}}(\lambda)x_{\text{Si}}} \right) d\lambda \quad (5.21)$$

This results in $P_{\text{usable}_{\text{Si}}}$ of 87.3 W/m$^2$.

The irradiance that reaches the Si sub-cell ($F_{\text{trans}_{\text{SiGe}}}$) and the usable portion of it ($F_{\text{usable}_{\text{Si}}}$) are shown in Fig. 5.8.

The transmission losses were calculated using:

$$P_{\text{trans}_{\text{Si}}} = P_{\text{trans}_{\text{SiGe}}} - P_{\text{abs}_{\text{Si}}} = P_{\text{trans}_{\text{SiGe}}} - P_{\text{usable}_{\text{Si}}} - P_{\text{thermal}_{\text{Si}}} \quad (5.22)$$

The transmission losses account for 205.1 W/m$^2$ of the total AM1.5G spectrum.
Fig. 5.8: Irradiance transmitted through the SiGe buffer and the usable by the Si sub-cell fraction of it. Total usable power density is 87.3 W/m² (8.8% of the power density of the available AM1.5G spectrum)

Combining the usable spectral irradiance in the GaAsP and Si cells results in the plot in Fig. 5.9. The total usable power density is 460.6 W/m² which is 1.5% less than the 467.7 W/m², calculated for the Si single-junction cell in section 5.2. This result shows that the use of thick SiGe buffer is very detrimental to the tandem cell operation.

Fig. 5.9: Absorbed spectral irradiance in GaAsP/SiGe/Si solar cell. Large portion of the light, intended for the Si sub-cell is lost in the SiGe buffer layer. Total useful absorbed power density is 460.6 W/m² (46.4% of the power density of the available AM1.5G spectrum).
The usable absorption and the losses in the different sub-cells for all modeled structures are summarized in Table 5.1.

**Table 5.1. Summary of power density absorption and losses in the different solar cell structures (rounded to the whole number). Total available spectral power density $P_{AM1.5G}=993 \text{ W/m}^2$.**

<table>
<thead>
<tr>
<th>Sub-cell</th>
<th>Thermalization Losses, W/m²</th>
<th>Sub-bandgap absorption Losses, W/m²</th>
<th>Transmission Losses, W/m²</th>
<th>Loss in SiGe, W/m²</th>
<th>Usable, W/m²</th>
<th>Total usable, W/m²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si SJ cell</td>
<td>317</td>
<td>-</td>
<td>208</td>
<td>-</td>
<td>468</td>
<td>468</td>
</tr>
<tr>
<td>GaAsP/Si (no SiGe buffer)</td>
<td>129</td>
<td>32</td>
<td>-</td>
<td>-</td>
<td>373</td>
<td>573</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>-</td>
<td>208</td>
<td>-</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>GaAsP/SiGe/Si</td>
<td>129</td>
<td>32</td>
<td>-</td>
<td>153</td>
<td>460</td>
<td></td>
</tr>
<tr>
<td>Si</td>
<td>14</td>
<td>-</td>
<td>205</td>
<td>-</td>
<td>87</td>
<td></td>
</tr>
</tbody>
</table>

5.5 **Step-cell design for improved light absorption in GaAsP/SiGe/Si solar cell**

The step-cell is modeled as a linear combination of the GaAsP/SiGe/Si cell (section 5.4) and the Si cell (section 5.2). The ratio of the areas for the two cells is varied from 1 to 2. The case with area ratio of 1 is the case discussed in the previous section. The results are shown in Fig. 5.10.
As expected, it can be seen that as more silicon is exposed to the light, the response to the wavelengths otherwise absorbed by the SiGe buffer layer, increases. This comes at a cost, though, as the absorption in the GaAsP cell decreases, leading to only a small increase in the overall absorption. Fig. 5.11 shows the summary of power density of usable and lost irradiance for $A_{\text{tot}}/A_{\text{top}}$ ratios of 1 to 2.

The power density of the total absorbed light increases from 460.6 W/m$^2$ to 464.1 W/m$^2$, which is still less than the power density achievable from a Si single-junction cell (467.7 W/m$^2$). This result suggests that efforts must be made to decrease the thickness or eliminate the SiGe buffer layer from the structure of the GaAsP/Si cell in order for its integration to be worthwhile.
Fig. 5.11: Summary of the losses and usable power density of step-cell GaAsP/SiGe/Si solar cell for $A_{\text{tot}}/A_{\text{top}}$ ratio from 1 to 2. The total usable spectral density increases from 460.6 to 464.1 W/m$^2$ and the total losses (sum of transmission, thermalization, sub-bandgap and losses in SiGe) decrease from 532 to 528.5 W/m$^2$.

5.6 Chapter summary

In this chapter the light absorption for four different cell designs of interest was modeled. The GaAsP/Si bonded tandem cell showed 24% relative improvement in light absorption over a single-junction Si cell (573.4 W/m$^2$ vs 467.7 W/m$^2$ absorbed power density). When the GaAsP cell is integrated with the use of SiGe buffer layer, due to its smaller bandgap, a decrease of 1.5% in absorption was calculated compared to the Si cell (460.7 vs 467.7 W/m$^2$). The use of a step cell design improves the absorption in the wavelength range most affected by the presence of the SiGe buffer layer but it also decreases the absorption in the high-efficiency top cell and altogether does not increase the efficiency beyond that of the Si cell. These results suggest that removing the SiGe buffer layer, using a wide bandgap buffer layer or adopting a layer transfer technique could be the only viable routes for creating higher efficiency solar cells on a Si platform.
Chapter 6

Conclusions and future work

6.1 Summary of results

This thesis has experimentally and theoretically explored the implications of growing a GaAsP solar cell on top of an active Si sub-cell via the use of an epitaxially grown SiGe buffer layer.

The impact of SiGe graded buffer growth on the performance of an underlying Si solar cell was experimentally evaluated with respect to series resistance and leakage current. The extraction of the series resistance gave no indication that the addition of the SiGe buffer negatively affected the series resistance of the solar cells. However, it was shown that the SiGe growth increases the leakage current of the Si sub-cell by at least a decade which was related to an increase in the number of threading dislocations being punched down into the Si substrate. Limiting the propagation of threading dislocations into the Si sub-cell would reduce the leakage current and lead to increase in $V_{oc}$ of the cell and overall efficiency.

The impact of the narrow-bandgap SiGe layer on the optical characteristics of the underlying Si solar cell was quantified. Introducing a SiGe buffer layer has shown to drastically reduce the short-circuit current and efficiency of the bottom Si solar cell. In an attempt to mitigate this, a step-cell design was introduced in which portion of the SiGe buffer is etched away to allow more light to reach the Si sub-cell. With the use of a step-cell design, the short circuit current was increased from 5 to 20 mA/cm$^2$ when the $A_{tot}/A_{top}$ ratio increased from 1 to 2. The response at short
wavelengths and as a consequence the overall external quantum efficiency (EQE) was also shown to increase with increasing area of the exposed Si cell. These initial results demonstrate the effectiveness of the step-cell design in increasing the current contributed by the Si sub-cell and is therefore expected to improve the overall tandem cell efficiency.

The theoretical absorbed irradiance for Si single-junction cell, a bonded GaAsP/Si cell, a GaAsP/SiGe/Si cell and the step-cell design was modeled. The GaAsP/Si bonded tandem cell showed 24% relative improvement in light absorption over a single-junction (SJ) Si cell which could potentially lead to a solar-cell efficiency of up to 35% (based on a maximum reported Si single-junction solar cell efficiencies of ~28% [3][39]). The addition of a SiGe graded buffer reduced the usable absorption of the solar cell significantly, bringing it under that of the Si SJ cell. Even though the step-cell design was able to compensate for some of the losses in the SiGe, there seemed to be almost as equal increase in transmission losses and altogether the design did not increase the efficiency beyond that of the Si cell. These results suggest that a combination of thinning down the SiGe buffer and the use of a moderate $A_{\text{tot}}/A_{\text{top}}$ ratio for the step-cell design, using a high-bandgap material as a buffer layer or using layer transfer approach could be the only possible route for creating higher efficiency solar cells on a Si platform.

6.2 Suggestions for future work

6.2.1 Bonding of GaAsP and Si cells

With the SiGe absorbing almost 20% of the available light, bonding GaAsP cells directly on Si without a buffer layer seems to be one of the logical choices for fabricating GaAsP/Si tandem cells. The GaAsP cell can still be grown on SiGe layers on Si, ensuring high quality of the material,
while keeping the cost of the substrates down. The grown structure can then be flipped over and bonded to the Si sub cell. The wafers two cells can then be bonded and the SiGe can be removed via chemical mechanical polishing (CMP). Alternatively, a sacrificial layer (for example AlAsP or AlGaAs) can be grown between the GaAsP cell and the underlying SiGe buffer during the epitaxial growth that can then be etched away [40]–[42]. This would allow the SiGe virtual substrate to be reused for the deposition of GaAsP films, reducing the cost of the fabrication process. The main challenge of this approach is achieving an electrically-active, high-quality bonded interface, necessary for realizing two-terminal tandem cell configuration. An additional CMP step during SiGe growth will also be needed to ensure low surface roughness of the GaAsP layer being bonded.

6.2.2 Using high-bandgap buffer layer

Using a buffer layer with a higher bandgap than that of the bottom Si cell (i.e. GaP), could help with some of the challenges, associated with the direct bonding approach and the SiGe-buffer approach. The monolithic growth of all the materials ensures a high-quality electrical bond. Unlike the bonding approach, no additional wafers and CMP steps will be necessary, cutting down the cost of the final cell. GaP can be grown directly on Si due to the minimal lattice mismatch between the two materials. The higher bandgap of the GaP (2.2 eV) makes a graded buffer layer based on this material (i.e. GaAsP, InGaP) transparent to the light transmitted through the GaAsP top cell and most of it will then reach the Si sub-cell. The main challenge, associated with growing GaAsP and InGaP graded buffers on GaP is the relatively high density of threading dislocations in these films (>$8\times10^{16}$ cm$^{-2}$), limiting the efficiency of the top cell. It has been shown that in order for the
integration of GaAsP top cell and Si to be worthwhile, the threading dislocation density of the top cell needs to be in the order of $10^6 \text{ cm}^{-2}$, currently only achievable with SiGe buffer layers.

### 6.2.3 Triple-junction cells

The introduction of a second junction (GaAsP) to a Si solar cell was shown to reduce the total thermalization losses from 317 W/m$^2$ to 179 W/m$^2$. However, the remaining thermalization losses still account for 20% of the available AM1.5G spectrum. The integration of a third junction has the potential to reduce the thermalization losses even further and to increase the overall efficiency of the cell. Some possible top cell materials include InGaP and AlInGaP since they can be lattice matched to the underlying GaAsP layer and provide bandgaps in the order of 2 eV. Grassman et al. [8] have calculated the efficiency of a III-V/Si triple junction as a function of the top cell and middle cell band gap. These calculations show that theoretical efficiencies approaching 50% are achievable for a lattice matched InGaP/GaAsP/Si triple junction cell—representing a 10% relative increase in efficiency compared to a GaAsP/Si tandem cell. Even higher efficiencies are theoretically achievable with an increasing the number of junctions.
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