Bias Temperature Instability (BTI) in GaN MOSFETs

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Abstract:

GaN is a promising alternative to Si for transistors for power electronics. For high-voltage applications, the GaN high electron mobility transistor with insulated gate (MIS-HEMT) is an attractive transistor structure because of its high breakdown voltage combined with low gate leakage current. Impressive device performance has recently been reported. However, before GaN MIS-HEMTs can be deployed in the field, reliability and stability issues need to be solved. In particular, the threshold voltage ($V_T$) instability under high voltage and temperature stress, sometimes referred to as bias-temperature instability (BTI), is a serious concern. The physical mechanisms responsible for BTI in GaN MIS-HEMT are not well understood. This is mainly because of the complex gate stack with multiple layers and interfaces, which presents many trapping sites with complex dynamics. In this work, a simpler GaN MOSFET structure is used to isolate the role of the gate oxide and the oxide/GaN interface in BTI.

Using a carefully designed benign characterization approach, we have studied in detail the response to positive and negative gate bias stress of GaN MOSFETs with various gate dielectrics. This has allowed us to postulate relevant physical mechanisms. For positive gate stress (PBTI), positive $V_T$ shifts are caused by a combination of electron trapping in pre-existing oxide traps and trap generation either at the oxide/GaN interface ($SiO_2$/GaN) or in the oxide close to the interface ($Al_2O_3$/GaN). For negative gate stress (NBTI), three degradation mechanisms are proposed. In low-stress regime, recoverable electron detrapping from pre-existing oxide traps takes place resulting a temporary negative $V_T$ shift. In mid-stress regime, a transient positive $V_T$ shift is probably caused by electron trapping in the GaN channel under the edges of the gate. In high-stress regime, there is a permanent negative $V_T$ shift, which is consistent with interface state generation. In addition, we have confirmed that for benign positive and negative gate bias stress, there is a unified reversible mechanism that accounts for the device dynamics and that is electron trapping/detrapping in pre-existing oxide traps. This work provides fundamental understanding to elucidate the reliability and instability of high-voltage GaN MIS-HEMTs.

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Chapter 1. Introduction

1.1. Motivation of Reliability Study of GaN MIS-HEMT

1.1.1. Overview of GaN MIS-HEMT technology

AlGaN/GaN high electron mobility transistors (HEMTs) are promising to replace conventional silicon devices for high-voltage switching applications [1], [2]. This is because the wide energy band gap of GaN (3.4 eV versus 1.14 eV for silicon) enables a very high breakdown field (3.5 MV/cm), which makes GaN devices the superior choice for high voltage operation. In addition, the spontaneous piezoelectric effect in the AlGaN/GaN heterostructure creates a two-dimensional electron gas (2DEG) with a density above $10^{13}$ cm$^{-2}$, forming a highly conducting channel without the need of doping [2]. These device properties allow low ON-resistance operation, which significantly reduces power loss and make AlGaN/GaN HEMTs attractive for many power electronic applications [1][3]–[6].

On the other hand, the AlGaN/GaN HEMT structure has two main limitations. First, gate leakage is a major problem. Because GaN HEMTs are normally-ON, they are subjected to large negative bias in the OFF-state. As a result, gate leakage becomes important when measuring the OFF-state power loss. This also results in a reduction of the breakdown voltage [7]. It is difficult to suppress gate leakage using a Schottky gate structure [8]. Second, most of the
AlGaN/GaN HEMTs demonstrated so far have normally-ON (depletion mode) characteristics with a negative threshold voltage \( (V_T) \). This is not ideal for power applications because it increases power loss during switching and also requires an additional driving circuit to ensure a fail-safe system [9], [10].

To mitigate these two drawbacks, the AlGaN/GaN HEMT with an inserted insulating layer, i.e., metal-insulator-semiconductor high-electron-mobility-transistor (MIS-HEMT) was introduced [11]. With the added insulator, GaN MIS-HEMTs can achieve much lower gate leakage current and in turn enable higher breakdown voltage than GaN HEMTs with a Schottky gate [12]. In addition, GaN MIS-HEMTs also allow for \( V_T \) modification to achieve enhancement-mode (E-mode) operation \( (V_T > 0) \) [13]. The increased breakdown voltage and the possibilities of enhancement-mode operation make GaN MIS-HEMTs extremely desirable for power switching applications. Recently, many studies have demonstrated GaN MIS-HEMTs with superior performance over GaN HEMTs, and some studies have shown enhancement-mode operation using gate insulating layers such as \( \text{SiO}_2 \), \( \text{Al}_2\text{O}_3 \), \( \text{HfO}_2 \) and \( \text{AlN} \) [14]–[16].

The new promising features of GaN MIS-HEMTs have attracted growing interest in technology commercialization. However, the insulating layer also adds complexity to the gate stack and introduces unwanted device instabilities on top of those existing in GaN HEMTs. In the next section, we will discuss these reliability issues in detail.

1.1.2. Reliability challenges of GaN MIS-HEMTs

Reliability issues surrounding GaN MIS-HEMTs can cause temporary or permanent device degradation, and this is detrimental to circuit performance and device lifetime. For example, GaN MIS-HEMTs are normally operated under high drain-gate bias voltage, which often results in charge trapping in the gate and the drain region. This trapping behavior could
cause current collapse and an increase in ON-resistance [13][17]. Trapping at the dielectric/semiconductor interface can also cause threshold voltage ($V_T$) shift under various biasing conditions [18]. Time dependent dielectric breakdown (TDDB) is another failure mode that is critical to gate stack reliability [19]. These instabilities and reliability issues significantly limit the usability of GaN MIS-HEMTs especially for high voltage and high frequency operations.

There have been extensive studies on the subject of AlGaN/GaN HEMT reliability, but very limited work has focused on the reliability of GaN MIS-HEMTs, especially in relation to the gate stack [20]. Trapping and degradation mechanisms in GaN MIS-HEMTs are complicated and not well understood. Figure 1-1 shows the cross section of a typical GaN MIS-HEMT structure. The gate stack consists of the metal gate, the oxide layer, the GaN cap, the AlGaN barrier and the GaN channel. As we can see from Figure 1-1, with the addition of an insulating layer, the gate stack is quite complex with multiple interfaces. Studies on gate stack reliability of GaN MIS-HEMTs have suggested multiple trapping sites in different layers and interfaces. For example, Meneghini studied GaN MIS-HEMT with $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ dielectrics ($\text{Si}_3\text{N}_4$ next to AlGaN barrier layer) and found trapping behavior related to defects in the gate-drain region and under the gate [21]. Imada observed recoverable ON-resistance and threshold voltage shift under positive gate stress of a recessed gate GaN MIS-HEMT with $\text{Al}_2\text{O}_3$ dielectric, which he attributed to trapping at the gate recess region [22]. Marcon focused on the time dependent dielectric breakdown of GaN MIS-HEMTs with $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ dielectrics ($\text{Si}_3\text{N}_4$ next to AlGaN barrier layer), and proposed the mechanism of electron trapping below the gate [23]. Nevertheless, the physical origins of different trapping mechanisms are still unclear and needs to be investigated in detail.
In this thesis, we focus on the $V_T$ instability due to gate bias stress. This phenomenon is often referred to as bias temperature instability (BTI) in standard CMOS technologies [24]. For GaN MIS-HEMTs, both depletion-mode (D-mode) and E-mode devices are subjected to gate bias stress during normal operating conditions. As such, $V_T$ shift under gate stress is a serious concern and needs to be studied carefully. In addition, it has been reported that BTI in GaN MIS-HEMTs is worse when compared to GaN HEMTs [25]. Therefore, it is important to understand the contribution of the insulating layer and its interfaces to BTI of GaN MIS-HEMTs.

1.2. Bias Temperature Instability (BTI) in GaN MIS-HEMTs

1.2.1. BTI in Si, SiC and other III-V systems

BTI has been a critical reliability issue in MOSFETs made out of many material systems such as Si, SiC and InGaAs. First observation of BTI for Si MOS transistors were made in 1966 [26]. However, not until 2000’s did BTI, particularly negative-bias temperature instability
(NBTI), become a serious concern. This happened because the introduction of nitrogen into the MOS fabrication process was found to enhance NBTI [27]-[29]. In advanced Si CMOS technology, NBTI has the greatest impact on p-FET devices due to the generation of positive oxide charge and interface traps in MOS structures under negative gate bias, especially at elevated temperature (100° to 250°) [30], [31]. An increase in the absolute threshold voltage, mobility degradation, drain current reduction and transconductance decrease are observed due to NBTI [32]. One of the popular theoretical models for NBTI is the reaction-diffusion model (R-D model) [27], [30], [33], [34]. In this model, the holes in the inversion layer interact with the Si-H bonds at the oxide/Si interface. This interaction weakens the Si-H bonds and leads to dissociation of H atoms with the corresponding generation of interface traps. In the diffusion phase, hydrogen diffuses from the interface to the oxide. More recently, the R-D model has been challenged by charge-trapping dominated theories such as the elastic hole trapping [35] and switching oxide traps theory [36], where NBTI is explained by charge trapping and detrapping in the oxide during the stress and recovery phases.

As CMOS technology continues to scale down, the use of high-k metal gate (HKMG) becomes the key to extend Moore's law. Generally, a thin SiO₂ interface layer is needed between the high-k dielectric and the channel to maintain high channel mobility [37]. High-k dielectrics have created new challenges for the understanding of BTI, mainly due to pre-existing traps in the oxide bulk [38]-[40]. Two separate models are proposed for the possible location of these oxide traps [38], [41], as shown in Figure 1-2.
To decide if the trapped charges are located in the bulk of the high-k film or at the high-k/interfacial layer, Young et al. performed hysteresis measurements on devices with different high-k thickness, and confirmed that trapping occurs mostly within the oxide bulk since less trapping in thinner high-k films is observed [42]. In a separate work, it has also been reported that under negative and positive gate bias, defects are charged and discharged through tunneling [43], suggesting that the responsible traps are very close to the device channel.

The methodologies and theoretical models developed for BTI in Si transistors constitute the foundation for reliability studies in newer material systems such as SiC and other III-V compound based devices. For example, in SiC MOSFETs, it is observed that an alternating positive/negative gate stress with an electric field of 1 to 2 MV/cm across the oxide results in a repeatable $V_T$ shift/recovery [44]. This is consistent with the BTI charge trapping theory for Si MOSFETs discussed earlier, and it is attributed to the large amount of near-interface oxide bulk traps tunneling in and out of the oxide. It is also reported that a decrease in the minority carrier
generation lifetime (partially recoverable) and increase in interface state density take place after negative gate voltage stress in SiC MOS capacitors [45].

For other III-V devices such as InGaAs MOSFETs with high-k dielectric, it is found that electron trapping at the pre-existing defects in the oxide contributes to a fast, recoverable positive $V_T$ shift under positive gate stress [46]–[48]. In addition, stress-generated defects also occur inside the oxide ($Al_2O_3$) in the near-interface region for InGaAs n-MOSFETs [47][48]. Studies on other high-mobility channel devices with high-k dielectrics also show similar charge trapping phenomenon under positive gate stress [49]. In the meantime, a study on ZrO$_2$/Al$_2$O$_3$/InGaAs MOSFETs shows that a combination of trap-discharge and interface degradation under NBTI caused a negative $V_T$ shift [50]. These BTI findings in SiC and InGaAs transistors are largely consistent with those demonstrated in Si MOSFETs.

1.2.2. Current understanding of BTI in GaN MIS-HEMTs

Compared to other material systems, the understanding of BTI in GaN MIS-HEMTs is very limited. There are a few studies that report $V_T$ shifts due to BTI in AlGaN/GaN MIS-HEMTs [18], [51], [52]. In [18] and [51], authors use the concepts of CET maps to demonstrate traps with a broad distribution of time constants, but the nature of the defect states is inconclusive. It is suggested that the complex gate structure with multiple layers and interfaces makes it challenging to isolate trapping effects from different layers and trapping sites. Figure 1-3 shows the complex nature of these trapping sites in the energy band diagram of a MIS-HEMT structure. A few potential defect centers are suggested to contribute to $V_T$ drift: oxide bulk defects, defects at the oxide/GaN interface and AlGaN barrier layer traps. A separate work studied PBTI in GaN MIS-HEMTs [52]. Here, authors indicate that the oxide traps and the related parasitic transport and charge trapping mechanisms may play a key role in PBTI of GaN.
MIS-HEMTs. However, the experimental data is limited to hysteresis analysis and the detailed trapping process is unclear.

The complex nature of the gate stack makes it challenging to tackle the BTI problem in GaN MIS-HEMTs. As such, the key to identify the physical origin of BTI in GaN MIS-HEMTs is to isolate each trapping site and study their respective contributions to $V_T$ instability.

![Diagram](image)

Figure 1-3. (a) Overview of potential defect centers in the oxide/barrier gate-stack of a GaN MIS-HEMT device. (b) Bias effect on defect energy position of bulk oxide defects as a function of the depth $x$ [18].

1.2.3. Advantage of GaN MOSFET structure

What we have seen so far indicates that there are multiple trapping sites within the gate stack that could contribute to BTI in GaN MIS-HEMTs, and traps in the oxide layer and at the oxide/semiconductor interface are some of the key trapping mechanisms to investigate in order to understand BTI in these devices. In this thesis, we use a simpler GaN MOSFET structure to isolate the roles of oxide and the oxide/GaN interface to device instability in GaN MIS-HEMTs.
Figure 1-4 shows the cross section of the GaN MOSFET studied in this work. In this structure, the gate is recessed and the AlGaN barrier layer is etched away underneath the gate. As a result, the GaN channel is located immediately below the gate oxide. The locations for trapping are minimized and we can focus on the role of the oxide and the oxide/GaN interface. This structure on its own is also a strong candidate for power electronic applications [53], [54].

![Image](image-url)

**Figure 1-4.** GaN MOSFET structure used in this thesis.

### 1.3. Thesis Goal and Organization

BTI is a major roadblock for technology commercialization of GaN MIS-HEMTs in high-voltage power applications. This thesis takes a new approach to investigate BTI in GaN MIS-HEMTs by focusing on the role of the oxide and the oxide/GaN interface using a simple GaN MOSFET structure. The goal of this thesis is to provide a solid physical understanding that can be used to mitigate BTI in GaN MOSFETs and MIS-HEMTs.

In chapter 2, we discuss the development of a benign characterization scheme that allows for accurate and reproducible measurements in a manner that does not affect the device. First,
the device figures of merit are described. Then, we present the details of the experimental setup and the design process of our stress-recovery experiment flow.

Chapter 3-5 focus on experimental results and analysis of our BTI study. In chapter 3, we present detailed experimental study of PBTI in GaN MOSFETs with SiO\textsubscript{2} and SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} gate dielectrics. First, stress/recovery data of PBTI for various stress voltages and temperatures in SiO\textsubscript{2} MOSFETS are discussed. Next, we compare SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} MOSFETs against SiO\textsubscript{2} MOSFETs and summarize their similarities and differences. We then perform a detailed analysis of the experimental data and formulate hypothesis of the physical mechanisms behind PBTI.

In chapter 4, we study NBTI in GaN MOSFETs. An overview of a three-regime behavior of NBTI in SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} MOSFETs is discussed first. Then, detailed experimental studies of each of the three regimes in SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} MOSFETs are presented. The hypotheses for mechanisms behind the three regimes are discussed in detail. Next, we compare NBTI stress in SiO\textsubscript{2} versus SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} MOSFETs, and summarize our general findings.

Chapter 5 discusses a symmetrical continuum of PBTI and NBTI for low gate-bias stress conditions. We show detailed measurement results of SiO\textsubscript{2}/Al\textsubscript{2}O\textsubscript{3} MOSFETs for various low gate stress voltage and temperature values and explain the physics behind the PBTI-NBTI continuum.

Chapter 6 summarizes our key contributions to the understanding of BTI in GaN MOSFETs. It also includes suggestions for future work to improve BTI and other device instabilities for GaN MOSFETs and MIS-HEMTs.
Chapter 2. Experimental

2.1. Introduction

This chapter describes the experimental details of our BTI study on GaN MOSFETs. We first developed a stress and characterization scheme for our test chips. This scheme allows us to extract accurately device parameters before, during and after stress without affecting the device figures of merit. This is important because device characterization itself could introduce unwanted stress and shift device parameters.

This chapter is organized as follows. First, the GaN MOSFET structures used in this work are presented. Next, we define the device’s figures of merit that have been used to characterize the effect of BTI. We then explain the details of a benign characterization scheme we developed for this study. Following that, the standard experiment flow and measurement variations for PBTI and NBTI are presented.

2.2. Device Structure and Figures of Merit

As stated in chapter 1, GaN MOSFETs constitute an excellent vehicle to study BTI in GaN power FETs because it isolates the contributions of the gate oxide and the oxide/semiconductor interface to device instability. The GaN MOSFETs utilized in this work
are industrial prototype devices with a simple AlGaN/GaN recessed gate structures. The cross-section of the device structure is shown in Figure 2-1. The AlGaN barrier layer is removed from the intrinsic gate region so that the gate oxide layer is in direct contact with the GaN channel. The gate stack consists of either SiO₂ or composite SiO₂/Al₂O₃ dielectric (Al₂O₃ next to semiconductor). The devices have channel width/length of 100 μm/1 μm.

![Figure 2-1. Cross section of GaN MOSFET used in this work.](image)

In this work, we characterize the impact of gate bias stress at various temperatures on device behavior through figures of merit defined in the linear operating region (at a drain-source voltage (V_DS) of 0.1 V). In particular, we focus our interest on the stability of three device parameters: threshold voltage, \( V_T \), is defined at drain current \( I_D = 1 \mu A/mm \); subthreshold swing, \( S \), is defined at \( I_D = 0.1 \mu A/mm \); and the maximum transconductance, \( g_{m,max} \), is defined as the maximum \( dI_D/dV_{GS} \) obtained in an \( I_D-V_{GS} \) sweep. These three parameters are chosen to help us understand how gate bias stress impacts charge control in the gate stack as well as channel mobility so that the fundamental device degradation mechanisms as a result of BTI can be identified.
For the most part, the devices under study have $V_T$ around 0 V. However, throughout this study, the fabrication process for our test chips has gone through various iterations. As a result, there is batch to batch variations of $V_T$, $S$, and $g_{m,max}$. In virgin devices, $V_T$ ranges from -1 to 2 V, $S$ from 100 to 250 mV/dec, and $g_{m,max}$ from 0.4 to 0.85 mS/mm. In subsequent chapters, we will describe the exact values of $V_T$, $S$, and $g_{m,max}$ for the devices used in each experiment.

2.3. Experimental Setup

The schematic diagram of our experimental setup is shown in Figure 2-2. Device characterization is performed using Keysight B1500a semiconductor device analyzer connected to a Cascade Microtech probe station. To avoid device oscillations, we use Picoprobe GSG 125 um microwave probes for all of our measurements. A temperature controller unit is connected to the chuck on the probe station with a temperature range of -45°C to 200°C. During
measurements, devices under test (DUT) are kept in a closed chamber so that characterizations can be done in the dark and under nitrogen gas if needed.

In our experiments, we have adopted a characterization suite written in Microsoft Visual C++ to automatically measure device parameters before, during and after stress [55]. Throughout our study, we have made various modifications to the characterization suite to fit our testing needs. For example, during some of the NBTI experiments, $V_T$ shifts can be quite large, and a fixed $V_{GS}$ range throughout a stress experiment could introduce unwanted stress. Therefore, we developed an $I_D-V_{GS}$ sweep scheme with a dynamic $V_{GS}$ range, where the starting point and the end point of $V_{GS}$ are adjusted based on measured $V_T$ value of the previous run (i.e., $V_{GS,\text{stress}}$ starts at $V_T - 1$ V and stops at $V_T + 1.5$ V).

2.4. Experimental Design

2.4.1. The need for a benign BTI characterization scheme

In order to accurately measure BTI in GaN MOSFETs, we first need to develop a benign characterization scheme to accurately extract device parameters before stress, during stress, during recovery, and at the same time do not introduce additional stress to devices under test. Second, we also need to have a stable reference point to compare device characteristics after BTI and distinguish transient vs. permanent degradation of device parameters.

Because BTI is largely caused by trapping and defect generation in the gate oxide and at the oxide/semiconductor interface, the accuracy of device parameter extractions during stress and recovery depends heavily on the time constant ($\tau$) of charge trapping, detrapping and defect generation. Figure 2-3 shows the effect of measurement delay on the accuracy of $V_T$ extraction in SiON/Poly-Si pFETs during NBTI stress [56]. Here, because the recovery time constant is
much smaller than 1 s, the fast (delay time = 100 μS) and slow (delay time = 1 s) measurements give very different $V_T$ shift values, especially for shorter stress time. For this reason, it is important to consider the recovery characteristics while designing BTI measurements. In addition, in many cases, the characterization itself could introduce unwanted stress and cause device parameter shift, and the extraction of FOMs needs to be carefully calibrated to ensure the characterization itself is benign.

Figure 2-3. (Symbols) Comparison of $V_T$ shifts during NBTI stress for fast ($t_{\text{delay}} = 100\mu$s) and slow ($t_{\text{delay}} = 1$s) sensing at stress voltages of $-1.5$V and $-2.5$ V. The (lines) values $n$ are determined by a fit to a power law $\Delta V_T \sim t^n$ [56].

In addition to finding a benign FOM extraction method, it is also important to find a reference point so we can compare device parameters before and after BTI stress. This reference point will also help us distinguish transient vs. permanent phenomena due to BTI. Transient instabilities are normally the result of charge trapping/detrapping, while permanent degradation is often caused by broken bonds. Separating temporary instabilities from permanent degradation
helps us understand the physical mechanisms behind BTI and allows us to apply the corresponding mathematical models to the experimental results.

In the next section, we highlight methodologies we developed to accurately characterize BTI in GaN MOSFETs.

2.4.2. FOM extraction, device detrapping, and initialization

We first developed a benign characterization scheme to extract \( V_T \) and \( S \) before, during and after stress experiments. The characterization consists of an \( I_D-V_{GS} \) sweep at \( V_{DS} = 0.1 \) V that starts at a \( V_{GS} \) value \( \sim 1 \) V below \( V_T \) and stops at \( I_D = 1 \) \( \mu \)A/mm. From this, we extract \( V_T \) and the subthreshold swing \( S \), as defined earlier. This characterization itself does not introduce significant stress as proven by minor changes in device characteristics after 50 sweeps (\( \Delta V_T < 10 \) mV, \( \Delta S < 6 \) mV/dec) as shown in Figure 2-4. Using this characterization scheme, the first measurement of \( V_T \) and \( S \) comes 1 to 2 s after the removal of stress, which is “fast” compared to the recovery time constants we are dealing with (typically > 100 s).

![Figure 2-4. Minimal \( \Delta V_T \) and \( \Delta S \) after 50 continuous short \( I_D-V_{GS} \) sweeps.](image-url)
Figure 2-5. Room temperature subthreshold characteristics in the linear regime (V_{DS} = 0.1 V) before stress, after stress, after thermal detrapping (TD), and after 4 months of storage.

Next, we developed an initialization/detrapping step to finding the initial reference point and "reset" the devices after stress. We found that thermal baking (baking the samples in an oven at a fixed temperature for a certain period) was the most effective in detrapping the devices after stress. We identified a thermal detrapping condition that can detrap the device quickly and completely to a stable state after experiments performed under different temperature/duration conditions sequentially on the same device. To confirm that this thermal detrapping is effective and complete, in several cases, we have periodically re-measured a stressed and thermally detrapped device after storage at room temperature for various lengths of time. We have not observed any significant additional recovery of V_T within 10^7 s (Figure 2-5). We then consider the residual \Delta V_T, \Delta S, and \Delta G_{in,max} after thermal detrapping permanent (the permanent degradation here refers to device degradation that is either non-recoverable at all, or recoverable but has a very large recovery time constant). We also use this thermal detrapping step at the
beginning of an experiment to initialize a virgin device and create a reference point for subsequent stress/recovery experiments. We use a single set of thermal detrapping conditions throughout this work. Initialization typically results in a small change in device characteristics ($V_T < 30 \text{ mV}$).

### 2.4.2. Standard experiment flow

The standard experiment flow is shown in Figure 2-6. In a typical experiment, a device is first “initialized” and then characterized (“screened”). Then, we start the stress experiment, during which we apply a DC bias stress on the gate ($V_{GS,\text{stress}}$) with the source, drain and body grounded. During this stress period, we periodically pause the stress and perform a measurement of the $I_D$-$V_{GS}$ characteristics to extract device FOM. After the stress period, we continue to monitor device recovery through measurements of the $I_D$-$V_{GS}$ characteristics for a period of time before subjecting the device to thermal detrapping to reset it. Finally, we perform another $I_D$-$V_{GS}$ sweep to extract final FOM. We explain each of the above steps in more detail below.

The device initialization process consists of flushing the device for 5 minutes under microscope light, followed by a thermal detrapping step, as described in the previous section. After initialization, we characterize the device with a complete $I_D$-$V_{GS}$ sweep at $V_{DS} = 0.1 \text{ V}$ that starts at a $V_{GS}$ value below the threshold and stops at a $V_{GS}$ value above $V_T$ where $I_D$ saturates. From this sweep, we extract the initial $V_T$, $S$, and $g_{m,max}$. Next, the thermal detrapping step is repeated to reset the device again. We then re-measure the device with a shorter, benign $I_D$-$V_{GS}$ sweep as described in the previous section to confirm that the device characteristics are stable. At this point, the stress/recovery experiments can start.
Device screening and initialization

Stress and characterization

Recovery and characterization

Thermal detrapping

Characterization

Increase stress voltage or temperature

Figure 2-6. Experiment flow

The BTI stress and recovery sequence are shown in Figure 2-7. The stress phase consists of a series of stress segments of increasing length, $t_{stress}$, during which the device is subject to a constant gate stress ($V_{GS, stress}$), with the source, drain and substrate grounded. Throughout the

Figure 2-7. Stress and recovery sequence and device FOM extraction during ramps. (a) Continuous $I_D-V_{GS}$ sweeps for FOM extraction during recovery. (b) During recovery, the gate and drain voltage are forced to be 0 V. $I_D-V_{GS}$ sweeps are periodically measured during recovery.
course of our study, $V_{GS,\text{stress}}$ between -70 and 15 V and $t_{\text{stress}}$ between 1 and 10,000 seconds have been studied at various temperatures from -40°C to 175°C. During the stress period, we periodically pause the stress and perform either a full $I_D-V_{GS}$ sweep ($V_{GS}$ starts below $V_T$ and stops at $V_T + 2$ V, typically used when we need to extract $g_{m,\text{max}}$ in addition to $V_T$ and $S$, more details are discussed in 2.4.2), or a short $I_D-V_{GS}$ sweep ($V_{GS}$ starts below $V_T$ and stops when $I_D = 1 \mu\text{A/mm}$, used in extraction for $V_T$ and $S$ only). After stress, for PBTI we perform continuous $I_D-V_{GS}$ sweeps (Figure 2-7 (a)) to monitor device recovery. For NBTI, we used either continuous $I_D-V_{GS}$ sweeps, or a recovery sequence shown in Figure 2-7 (b), where we bias the gate and drain at 0 V, and periodically measure $I_D-V_{GS}$ characteristics during recovery. The recovery sequence in Figure 2-6 (b) was introduced to align recovery data with stress data on the same time scale for modeling purposes. The two measurement sequences do not introduce measurement discrepancies.

At the end of each stress/recovery sequence, the device is reinitialized using thermal detrapping and then a complete characterization is performed. If the device is completely recovered, i.e., $V_T$, $S$, and $g_{m,\text{max}}$ are restored to their initial values after thermal detrapping, we use the same device for subsequent BTI experiments. If permanent damage occurs after a stress step, i.e., $V_T$, $S$, and $g_{m,\text{max}}$ are not restored to their initial values after thermal detrapping, we switch to a new device with well-matched initial characteristics.

2.4.2. Experiment flow variations

The standard experiment flow described in 2.4.1 is adjusted for some stress conditions to fit different measurement needs of PBTI and NBTI experiments, while keeping the characterization benign.
For PBTI, in one set of experiments we used the standard flow to extract $V_T$ and $S$ only using short $I_D$-$V_{GS}$ sweeps. In a separate set of experiments we used a fresh collection of devices to study the behavior of $g_{m,\text{max}}$. For this, we performed a similar set of stress and recovery experiments but immediately after each stress segment we carried out a one-time, downward sweep of $I_D$-$V_{GS}$ in the linear region ($V_{DS} = 0.1$ V) that starts at $V_{GS} = 5$ V and stops at $V_{GS} = 0.5$ V. Because in PBTI experiments we study $V_{GS,\text{stress}}$ values of at least 5 V, this sweep should not introduce any additional damage to the device. Since the maximum transconductance point tends to occur between $V_{GS} = 2.5$ V and 4 V, this sweep yields a measurement of $g_{m,\text{max}}$ in the linear regime.

In our NBTI studies, measurements of $g_{m,\text{max}}$ need extra care compared to PBTI. This is because $V_{GS,\text{stress}}$ is negative but a positive gate voltage above $V_T$ is needed to extract $g_{m,\text{max}}$. This by itself results in a $V_T$ shift, affects the extracted value of $g_m$ and complicates further experiments on the same device. To minimize this effect, we first calibrate the gate voltage needed to extract $g_{m,\text{max}}$, which is found to be $\sim 1.5$ V above $V_T$. We find that this point is stable after low- and mid-tress conditions. Then, to extract $g_{m,\text{max}}$ in stress experiments of this kind, we use $V_T + 1.5$ V as the upper bound of an $I_D$-$V_{GS}$ sweep. We verified this approach by carrying out parallel sets of stress experiments on identical samples up to $V_{GS,\text{stress}} = -30$ V for $10^3$ seconds. In one case, only $V_T$ and $S$ measurements were performed. In the second one, $g_{m,\text{max}}$ was additionally extracted. The difference in the measured values of $V_T$ and $S$ in these paired sets of experiments was less than 5%.

Under harsh stress conditions in NBTI, as we show in Chapter 4, there is non-recoverable damage in the device after stress. In particular, there is a significant $S$ increase. This implies that a larger $V_{GS}$ sweep range is needed to obtain $g_{m,\text{max}}$. This is a problem because it causes a
significant change in the extracted figures of merit. As a solution, in harsh stress experiments, we use two identical devices for each stress period. From one of them we extract $V_T$ and $S$ using short $I_D-V_{GS}$ sweeps, from the second one we extract $g_{m,max}$ using an extended $V_{GS}$ range as needed.

In order to understand further the impact of electrical stress on the electrostatics of the device, we have also performed C-V characterization as part of NBTI experiments. In these experiments, we measure either the gate voltage dependence of the capacitance between the gate and source/drain while keeping the body floating ($C_{G,SD}-V_G$), or the capacitance between the gate and source/drain/body ($C_{G-V_G}$). This is done before, after stress experiments, and after device detrapping.

2.5. Chapter Summary

To investigate BTI of GaN MOSFETs, it is important to develop a benign measurement scheme to set an initial reference point and accurately extract device parameters during stress and recovery. We have designed a characterization scheme that meets these requirements. In this chapter, we outlined the device structure, definition of device figures of merits, measurement environment, and the experimental flow and variations. We have also explained the details of a benign $I_D-V_{GS}$ characterization scheme and an effective and benign detrapping scheme.

The experimental scheme we developed serves as the basis of our subsequent work. In chapter 3, 4 and 5 we focus on measurement results, analysis and modeling of BTI behavior using the experimental scheme presented here. It is worth mentioning that the measurement protocol developed for this work is specially designed for the GaN MOSFET structure from our
industrial collaborators and will need to be modified for testing of devices with different characteristics.
Chapter 3. Positive-Bias Temperature Instability (PBTI)

3.1. Introduction

In the previous chapter, we have discussed the experimental scheme, definition of key figures of merits, and the experimental methodology for studying BTI of GaN MOSFETs. In this chapter, we use the experimental scheme developed in chapter 2 to investigate the stability of the gate stack of GaN MOSFETs under positive gate stress (PBTI). We first present experimental results of PBTI in SiO$_2$ devices. Then, we discuss the similarities and differences of PBTI in SiO$_2$/Al$_2$O$_3$ composite dielectric devices compared to SiO$_2$ dielectric. From these experimental data, we propose the physical mechanisms behind PBTI in GaN MOSFETs and model the experimental results with well-established BTI models.

The devices studied in this PBTI work have the structure as shown in Figure 2-1. Standard figures of merit in the saturation regime ($V_{DS} = 10$ V) are as following. For SiO$_2$ devices, $V_T \sim -1.0$ V, $S \sim 175$ mV/dec, $g_{m,max} \sim 20$ mS/mm; for SiO$_2$/Al$_2$O$_3$ devices: $V_T \sim -0.7$ V, $S \sim 170$ mV/dec, $g_{m,max} \sim 30$ mS/mm. As stated in chapter 2, we focus our interest on the stability of $V_T$, $S$ and $g_{m,max}$ in the linear region (defined at $V_{DS} = 0.1$ V). Virgin devices used for the PBTI study exhibit values of $V_T = 0.06$ V with a standard deviation of 0.096 V, $S = 110$
mV/dec, \( g_{m,\text{max}} = 0.65 \, \text{mS/mm} \) for SiO\(_2\) MOSFETs and \( V_T = 0.16 \, \text{V} \) with a standard deviation of 0.06 V, \( S = 100 \, \text{mV/dec} \), \( g_{m,\text{max}} = 0.56 \, \text{mS/mm} \) for SiO\(_2\)/Al\(_2\)O\(_3\) MOSFETs. Figure 3-1 shows the subthreshold and transconductance characteristics at different temperatures of fresh SiO\(_2\) and SiO\(_2\)/Al\(_2\)O\(_3\) transistors in the linear regime (\( V_{DS} = 0.1 \, \text{V} \)).

Figure 3-1. Subthreshold and transconductance characteristics of (a) SiO\(_2\) and (b) SiO\(_2\)/Al\(_2\)O\(_3\) GaN MOSFETs in the linear regime (\( V_{DS} = 0.1 \, \text{V} \)) at different temperatures.

In this PBTI study, \( V_{GS,\text{stress}} \) between 5 and 15 V and \( t_{\text{stress}} \) between 10 and 10,000 seconds have been studied at -40\(^\circ\)C, room temperature (RT) and 75\(^\circ\)C. As described in chapter 2, we use one set of devices to trace the evolution of \( V_T \) and \( S \) using short \( I_D-V_{GS} \) sweeps, and another set of devices to study the behavior of \( g_{m,\text{max}} \).
3.2. Experimental Results of SiO$_2$ Devices

3.2.1. Effect of positive gate bias stress at room temperature

Figure 3-2 shows the stress time evolution of $\Delta V_T$ and $\Delta S$ under positive gate stress for SiO$_2$ GaN MOSFETs at RT. Data points are extracted 1 sec after the stress is paused. We observe a positive $\Delta V_T$ that increases with $t_{\text{stress}}$ and $V_{GS,\text{stress}}$, and see minimal change in $S$ for $V_{GS,\text{stress}} = 5$ and 10 V, but a clear increase for $V_{GS,\text{stress}} = 15$ V. The open symbols in Figure 3-2 show final values of $\Delta V_T$ and $\Delta S$ after 10,000 sec stress segments followed by thermal detrapping.

Figure 3-3 shows the dynamics of $V_T$ and $S$ recovery at RT after $V_{GS,\text{stress}} = 5$ V and 15 V for $t_{\text{stress}} = 10,000$ s. The devices experience a nearly complete recovery after 5 V stress, but only partial recovery after 15 V stress. Notably, $\Delta S$ after 15 V stress did not recover at all. $I_D-V_{GS}$
curves before stress and after stress and thermal detrapping for $V_{GS,stress} = 15$ V are shown in Figure 3-4. We can clearly see the positive, permanent $V_T$ shift accompanied by a degraded $S$.

![Graph showing $\Delta V_T$ and $\Delta S$ vs. $t_{recovery}$ for different $V_{GS,stress}$ values.](image1)

**Figure 3-3.** Stress time evolution of $\Delta V_T$ and $\Delta S$ for SiO$_2$ GaN MOSFETs stressed at three different voltages at room temperature. The first data point in the sequence is taken 1 sec after the stress is halted. The last set of points (open symbols) are $\Delta V_T$ and $\Delta S$ after thermal detrapping following a stress experiment with $t_{stres} = 10,000$ s.

![Graph showing subthreshold and transconductance characteristics.](image2)

**Figure 3-4.** Room temperature subthreshold and transconductance characteristics before and after $V_{GS,stress} = 15$ V stress followed by thermal detrapping (TD) of SiO$_2$ GaN MOSFETs in the linear regime ($V_{DS} = 0.1$ V).
In general, in all SiO$_2$ devices, we find no significant permanent $V_T$ shift after $V_{GS,\text{stress}} \leq 10$ V, but a permanent component for $V_{GS,\text{stress}} = 15$ V. $S$ degrades after 15 V stress and is not recoverable. This suggests the introduction of permanent damage to these devices.

During each stress segment, we also monitor the evolution of the gate current ($I_G$). Figure 3-5 shows $I_G$ as a function of stress time for $t_{\text{stress}} = 10,000$ sec experiments. $I_G$ tends to decrease slightly with stress time. This is consistent with other studies on charge trapping in pre-existing oxide traps. It also indicates that no new trap generation inside the oxide is occurring.

![Figure 3-5. Stress time evolution of $I_G$ for SiO$_2$ GaN MOSFETs stressed at three different voltages at room temperature.](image)

Figure 3-6 shows the evolution of $g_{m,\text{max}}$ degradation ($\Delta g_{m,\text{max}}/g_{m,\text{max}0}$) $\sim$ 1 sec after stress (closed symbols) and after subsequent thermal detrapping (open symbols) in a separate set of experiments from those of Figure 3-2 to Figure 3-5. We see higher $g_{m,\text{max}}$ degradation with
higher $V_{GS, stress}$ and longer $t_{stress}$. At $V_{GS, stress} = 5$ V, $g_{m,max}$ degradation is minimal. For all three stress voltages, $g_{m,max}$ is completely recovered after thermal detrapping.

![Graph showing stress time evolution of $\Delta g_{m,max}/g_{m,max}$](image)

**Figure 3-6.** Stress time evolution of $\Delta g_{m,max}/g_{m,max}$ for SiO$_2$ GaN MOSFETs stressed at three different voltages at room temperature. Data points are taken ~1 sec after the stress is paused. The last set of points (open symbols) are $\Delta g_{m,max}/g_{m,max}$ after thermal detrapping following a $t_{stress} = 10,000$ s stress experiment.

### 3.2.2. Impact of stress temperature

We have also studied the role of stress temperature during electrical stress. Figure 3-7 and Figure 3-8 show $\Delta V_T$ and $\Delta S$ for $V_{GS, stress} = 10$ and 15 V as a function of stress time at different temperatures. Both $\Delta V_T$ and $\Delta S$ increase with $T$, and the increase is more prominent at high $T$ (75°C).

The recovery dynamics of $V_T$ and $S$ after $V_{GS, stress} = 10$ V and 15 V at different $T$ are graphed in Figure 3-9. Note that both the stress and recovery phases take place at the same
temperature. The recovery time constants of SiO₂ devices appear rather independent of temperature. The final values of $\Delta V_T$ and $\Delta S$ after thermal detrapping for $t_{stress} = 10,000$ sec at various T are marked as open symbols (also summarized in Figure 3-7 and Figure 3-8, open symbols). Device characterization after thermal detrapping is made at the same temperature as the stress and recovery phases of the experiment.

For $V_{GS, stress} = 10$ V, after thermal detrapping, the SiO₂ transistors recover for $T \leq RT$ and only partially recover for $T = 75^\circ$C. Also at $75^\circ$C, S exhibits some permanent damage. For $V_{GS, stress} = 15$ V, after thermal detrapping, $\Delta V_T$ partially recovers at all T, and there is more recovery for $T \leq RT$ than for $T = 75^\circ$C. S exhibits permanent damage at all T, and the permanent damage increases with T.
Figure 3-8. Stress time evolution of $\Delta V_T$ and $\Delta S$ for SiO$_2$ GaN MOSFETs at different T. $V_{GS,\text{stress}} = 15$ V. Data points are taken 1 sec after the stress. The last set of points (open symbols) are $\Delta V_T$ and $\Delta S$ after a thermal detrapping step that follows stress experiments with $t_{\text{stress}} = 10,000$ s.

Figure 3-9. Recovery of $\Delta V_T$ and $\Delta S$ after a 10,000 sec stress at $V_{GS,\text{stress}} = 10$ and 15 V for SiO$_2$ GaN MOSFETs at 40°C, RT and 75°C. The last set of points (open symbols) is $\Delta V_T$ and $\Delta S$ after subsequent thermal detrapping step.
3.2.3. SiO$_2$ devices summary

We have reported the experimental results of PBTI stress in SiO$_2$ GaN MOSFETs, and the summary of device behavior is as following:

- The devices show positive $\Delta V_T$ after positive gate bias stress. Values of $\Delta V_T$ increase with stress voltage, time and temperature.
- $\Delta V_T$ is recoverable under benign stress conditions ($V_{GS, stress} \leq 10 \, \text{V}, \, T \leq RT$).
- $\Delta V_T$ is partially recoverable under harsh stress conditions ($V_{GS, stress} = 15 \, \text{V}, \, T > RT$).
- $\Delta S$ are minimal under benign stress conditions.
- Under harsh stress conditions ($V_{GS, stress} = 15 \, \text{V}, \, T > RT$), positive $\Delta S$ increases with stress voltage, time and temperature, and it is not recoverable.
- $\Delta g_{m, max}$ is minimal under benign stress conditions.
- Under harsh stress conditions ($V_{GS, stress} = 15 \, \text{V}, \, T > RT$), $g_{m, max}$ decreases. $|\Delta g_{m, max}|$ increases with stress voltage, time and temperature. It is completely recovered after thermal detrapping.

3.3. Experimental Results of SiO$_2$/Al$_2$O$_3$ vs. SiO$_2$ Devices

Now we compare PBTI results of SiO$_2$/Al$_2$O$_3$ devices vs. SiO$_2$ devices. Similar to SiO$_2$, SiO$_2$/Al$_2$O$_3$ devices show positive $V_T$ shift because of PBTI, and $\Delta V_T$ increases with stress voltage, stress time and temperature. In addition, for both dielectrics $\Delta V_T$ is recoverable under benign stress and is partially recoverable under harsh stress. Because we have reported the SiO$_2$ device data in the previous section, in this section we focus on differences between the two dielectrics.
The first difference between SiO$_2$ and SiO$_2$/Al$_2$O$_3$ devices is the temperature dependence of $\Delta V_T$. Figure 3-10 shows the comparison of $\Delta V_T$ for $V_{GS,\text{stress}} = 15$ V as a function of stress time at different temperatures. For SiO$_2$, $\Delta V_T$ and $\Delta S$ increase with $T$, and the increase is more prominent at 75°C. On the other hand, the effect of $T$ is small for SiO$_2$/Al$_2$O$_3$ transistors. In addition, $\Delta V_T$ for $T \leq RT$ for SiO$_2$/Al$_2$O$_3$ transistors is larger than in SiO$_2$ transistors.

![Graph showing $\Delta V_T$ vs Stress Time for SiO$_2$ and SiO$_2$/Al$_2$O$_3$ at different temperatures.](image)

**Figure 3-10.** Stress time evolution of $\Delta V_T$ for SiO$_2$ vs SiO$_2$/Al$_2$O$_3$ GaN MOSFETs at different $T$. $V_{GS,\text{stress}} = 15$ V. Data points are taken 1 sec after the stress. The last set of points (open symbols) are $\Delta V_T$ after a thermal detrapping step that follows stress experiments with $t_{\text{stress}} = 10,000$ s.

Subthreshold swing for SiO$_2$/Al$_2$O$_3$ devices also shows a different behavior compared to SiO$_2$ devices. Figure 3-11 shows the stress time evolution of $\Delta S$ under positive gate stress for SiO$_2$ and SiO$_2$/Al$_2$O$_3$ GaN MOSFETs at RT. Data points are extracted 1 sec after the stress is paused. For SiO$_2$ devices, we see minimal change in $S$ for $V_{GS,\text{stress}} = 5$ and 10 V, but a clear increase for $V_{GS,\text{stress}} = 15$ V. For SiO$_2$/Al$_2$O$_3$ device, we see minimal change in $S$ at all $V_{GS,\text{stress}}$. 

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Figure 3-11. Stress time evolution of $\Delta S$ for SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ GaN MOSFETs stressed at three different voltages at room temperature. Data points are taken 1 sec after the stress. The last set of points (open symbols) are $\Delta S$ after thermal detrapping following a stress experiment with $t_{\text{stress}} = 10,000$ s.

Figure 3-12. Stress time evolution of $\Delta g_{m,\max}/g_{m,\max0}$ for SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ GaN MOSFETs stressed at three different voltages at room temperature. Data points are taken ~1 sec after the stress is stopped. The last set of points (open symbols) are $\Delta g_{m,\max}/g_{m,\max0}$ after thermal detrapping following a $t_{\text{stress}} = 10,000$ s stress experiment.
Another difference between SiO$_2$/Al$_2$O$_3$ and SiO$_2$ devices is the $g_{m,\text{max}}$ degradation. Figure 3-12 shows the evolution of $g_{m,\text{max}}$ degradation for the two dielectrics ~ 1 sec after stress (closed symbols) and after subsequent thermal detrapping (open symbols) in a separate set of experiments from those of Figure 3-2 to Figure 3-5. For both dielectrics, we see higher degree of $g_{m,\text{max}}$ degradation with higher $V_{\text{GS},\text{stress}}$ and longer $t_{\text{stress}}$. At $V_{\text{GS},\text{stress}} = 5$ V, $g_{m,\text{max}}$ degradation is minimal. After thermal detrapping, $g_{m,\text{max}}$ completely recovers in SiO$_2$ MOSFETs, and only partially recovers in SiO$_2$/Al$_2$O$_3$ MOSFETs.

To summarize, SiO$_2$ MOSFETs and SiO$_2$/Al$_2$O$_3$ devices show following similarities and differences:

**Similarities:**
- Positive $\Delta V_T$ under positive gate stress, value of $\Delta V_T$ increases with stress voltage, time and temperature
- $\Delta V_T$ is recoverable under benign stress
- $\Delta V_T$ is partially recoverable under harsh stress

**Differences:**
- SiO$_2$/Al$_2$O$_3$ devices show larger $\Delta V_T$ at $T \leq RT$
- SiO$_2$/Al$_2$O$_3$ devices show weaker T dependence
- Both show non-recoverable $\Delta V_T$ under harsh stress, but
  - SiO$_2$ shows non-recoverable $\Delta S$
  - SiO$_2$/Al$_2$O$_3$ shows non-recoverable $\Delta g_{m,\text{max}}$
3.4. Discussion

3.4.1. Mechanisms responsibility for $V_T$ shift under PBTI

Our experiments allow us to postulate the mechanisms responsible for PBTI in GaN MOSFETs. For both dielectrics, $\Delta V_T$ is a combination of recoverable $\Delta V_T$ ($\Delta V_T_{\text{rec}}$) and non-recoverable $\Delta V_T$ ($\Delta V_T_{\text{perm}}$). As shown in Figure 3-13, $\Delta V_T_{\text{perm}}$ is the $V_T$ shift extracted after thermal detrapping. $\Delta V_T_{\text{rec}}$ is the result of total $V_T$ shift after stress minus $\Delta V_T_{\text{perm}}$. Next, we will discuss in detail the mechanisms behind both $\Delta V_T_{\text{rec}}$ and $\Delta V_T_{\text{perm}}$.

![Graph showing $\Delta V_T$ vs. stress time for SiO$_2$ and SiO$_2$/Al$_2$O$_3$ MOSFETs stressed at $V_{GS,\text{stress}} = 15$ V at room temperature.](image)

**Figure 3-13.** Values of $\Delta V_T$ after stress and final $\Delta V_T$ after thermal detrapping vs. stress time for SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ GaN MOSFETs stressed at $V_{GS,\text{stress}} = 15$ V at room temperature.

Under benign gate bias stress ($V_{GS,\text{stress}} \leq 10$ V, $T \leq RT$), the $V_T$ shift is consistent with electron trapping in pre-existing oxide traps, which is characterized by the recoverable $\Delta V_T_{\text{rec}}$. We conclude this from Figure 3-2 and Figure 3-3 for RT, and Figure 3-7 to Figure 3-10 for
various T. First, these graphs show $\Delta V_T$ 1 sec after different stress times. Within such a short time, little recovery takes place (Figure 3-3 and Figure 3-9 shows long recovery time constant). Second, stress time evolution of $V_T$ follows a saturating log-time dependence, as observed in other MOS systems [44], [46], [47], [57]. Finally, the slight decrease in $I_G$ also indicates that no additional traps are generated in the oxide bulk [57].

![Graphs showing $\Delta V_T$ and $\Delta S$ after thermal detrapping vs. stress time for SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ GaN MOSFETs stressed at three different voltage at room temperature.](image)

Figure 3-14. Final values of (a) $\Delta V_T$ and (b) $\Delta S$ after thermal detrapping vs. stress time for SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ GaN MOSFETs stressed at three different voltage at room temperature.

Under harsher stress ($V_{GS,\text{stress}} = 15$ V), there is an additional permanent $V_T$ shift for both gate dielectrics. Figure 3-14 summarizes the final $\Delta V_T$ and $\Delta S$ after thermal detrapping for each stress segment at room temperature. Notably, SiO$_2$ exhibits a significant permanent increase in $S$
that suggests the generation of interface states. This is clearer in Figure 3-15 that graphs the correlation between the final values of $\Delta V_T$ and $\Delta S$ after thermal detrapping following electrical stress at $V_{GS,\text{stress}} = 15$ V. We see a strong linear correlation between the two. The proportionality constant seems to depend on $T$. Subthreshold swing degradation under PBTI has also been reported in Al$_2$O$_3$/InGaAs and HfO$_2$/GaAs MOSFETs [48], [58]. In our composite oxide samples, the permanent degradation of $S$ is minor and a clear correlation with $\Delta V_T$ does not emerge.

Figure 3-15. Evolution of final values of $\Delta V_T$ vs. $\Delta S$ for SiO$_2$ transistors after $V_{GS,\text{stress}} = 15$ V at different temperatures. All measurements were taken at room temperature after a thermal detrapping step.

An additional interesting observation in our work is that the evolution of $g_{m,\text{max}}$ and $V_T$ also seem correlated. This can be seen in Figure 3-16 that graphs $\Delta g_{m,\text{max}}/g_{m,\text{max}0}$ as a function of $\Delta V_T$ after different stress periods for both dielectrics at room temperature. With the exception of long $t_{\text{stress}}$ in SiO$_2$/Al$_2$O$_3$ transistors, we observe a strong linear correlation between $\Delta g_{m,\text{max}}/g_{m,\text{max}0}$ and $\Delta V_T$ for all $V_{GS,\text{stress}}$ for both dielectrics. This suggests that $\Delta V_T$ mostly
originates in charge trapping in the oxide near the oxide/GaN interface or at the interface itself in interface states. Both are known to affect the mobility [31], [47]. For long stress times, trapping further away from the interface eventually takes place producing an additional $V_T$ shift without a corresponding decrease in $g_{m,max}$.

$\Delta g_{m,max}/g_{m,max0}$ vs. $\Delta V_T$ after thermal detrapping following stress experiments with $t_{stress} = 10,000$ s are also reported in Figure 3-16 (open symbols). We see permanent degradation of $\Delta g_{m,max}/g_{m,max0}$ for the SiO$_2$/Al$_2$O$_3$ transistors after $V_{GS, stress} = 15$ V, which suggests new trap generation in the oxide near the oxide/GaN interface that causes permanent mobility degradation [47], [59], [60]. Because these trap sites are close to the oxide/GaN interface, they are far from the gate metal. As a result, no significant changes are observed in the evolution of $I_G$. This oxide trap generation close to the oxide/GaN interface also explains the incomplete recovery after thermal detrapping of $V_T$ for the SiO$_2$/Al$_2$O$_3$ transistor after $V_{GS, stress} = 15$ V that is apparent in Figure 3-10 and Figure 3-12.

![Figure 3-16](image)

**Figure 3-16.** Evolution of $\Delta g_{m,max}/g_{m,max0}$ vs. $\Delta V_T$ for SiO$_2$ and SiO$_2$/Al$_2$O$_3$ transistors during stress experiments of various durations at room temperature. The open symbols correspond to measurements after a thermal detrapping step following stress experiments with $t_{stress} = 10,000$ s.
3.4.2. Model

The observations that we have made here are largely consistent with similar experiments on Si, SiC and III-V MOSFETs [44], [46]-[48]. $\Delta V_\text{T}$ in our GaN MOSFETs with SiO$_2$ gate dielectric appears to take place due to two mechanisms. One component, $\Delta V_{\text{Tox}}$, arises from electron trapping in the oxide. A second component, $\Delta V_{\text{Th}}$, which correlates to $\Delta S$, originates in interface state generation and population.

We postulate that, to the first order, for SiO$_2$ MOSFETs, $\Delta V_{\text{Th}}$ is the permanent portion of $\Delta V_\text{T}$ that is left after thermal detrapping. This hypothesis is supported by the linear dependence that we observe between the permanent portion of $\Delta V_\text{T}$ and of $\Delta S$ (Figure 3-15) which strongly suggests the generation of interface states. Similar observation of interface state generation has been made in Si systems after radiation [61], and also in FinFETs [62] where the [110] Si surface has a much higher Si-H bond density compared to the [100] surface [63]. It is well known that hydrogen used to passivate dangling bonds at the oxide-semiconductor interface can escape leading to the creation of interface states [64]. The remainder of $\Delta V_\text{T}$ for the SiO$_2$ transistors is $\Delta V_{\text{Tox}}$.

For SiO$_2$/Al$_2$O$_3$ MOSFETs, $\Delta V_{\text{Tox}}$ dominates and the permanent portion of $\Delta V_\text{T}$ is oxide trap generation close to the oxide/GaN interface, as observed in InGaAs n-MOSFETs [47]. The interface state generation in SiO$_2$/Al$_2$O$_3$ appears negligible, which is consistent with literature on high-K dielectrics [57].

With this interpretation, we find that $\Delta V_{\text{Tox}}$ in both transistor types follows a classic saturating log-time dependence, as observed in other MOS systems. The model of this power law relationship is described by [57]:
\[ \Delta V_{Tox} = \Delta V_{max} \cdot \left\{ 1 - \exp \left( -\left( \frac{t_{stress}}{\tau_0} \right)^\beta \right) \right\} \]  

(1)

where \( \Delta V_{Tox} \) is the \( V_T \) shift due to oxide trapping. \( \Delta V_{max} \) is a function of total trap density and the centroid of the trap-charge distribution in space, \( \beta \) describes the trap energy distribution, and \( \tau_0 \) is the time constant of the traps. For the SiO\(_2\)/Al\(_2\)O\(_3\) system, an exponent \( \beta = 0.22 \sim 0.25 \) and \( \tau_0 = 200 \) s gives an excellent fit to the entire data set at all T (Figure 3-17). For the SiO\(_2\) system, \( \beta = 0.25 \) and \( \tau_0 = 150 \) s provides a reasonable match at all T. The \( \beta \) values extracted here are close to those reported in the literature: \( \beta = 0.2 \sim 0.32 \) [44], [46]–[48].

For \( V_{GS, stress} = 15 \) V in SiO\(_2\) MOSFETs, there is an additional component of \( \Delta V_T \) that we attribute to interface state generation (\( \Delta V_{Tit} \)) [61]. As we can see in Figure 3-15, there is a linear dependence between \( \Delta V_{Tit} \) and \( \Delta S \) which is precisely what is expected from a simple model [61].

For SiO\(_2\)/Al\(_2\)O\(_3\) MOSFETs, there is also a non-recoverable \( \Delta V_T \) component for \( V_{GS, stress} = 15 \) V. This permeant \( \Delta V_T \) is accompanied by a non-recoverable \( g_{m, max} \) degradation as shown in Figure 3-12. This indicates permanent mobility degradation. Studies have attributed this to the generation of oxide traps close to the oxide/semiconductor interface [31], [47].
Figure 3-17. Model vs. experiments of $\Delta V_{\text{Tox}}$ evolution with stress time, for $V_{G\text{S, stress}} = 5\, \text{V}, 10\, \text{V}, \text{and } 15\, \text{V}$, at different temperature.
3.5. Chapter Summary

In this chapter, we present a detailed PBTI study of GaN MOSFETs with SiO₂ and SiO₂/Al₂O₃ gate dielectric. We present experimental results of SiO₂ MOSFETs at various stress conditions, and compared with the behavior of SiO₂/Al₂O₃ MOSFETs under the same conditions. Finally, we propose physical mechanisms for and model PBTI in SiO₂ and SiO₂/Al₂O₃ GaN MOSFETs.

We postulate that for SiO₂ MOSFETs, a positive \( \Delta V_T \) is caused by a combination of electron trapping in pre-existing oxide traps and interface trap generation. For SiO₂/Al₂O₃ MOSFETs, a positive \( V_T \) shift arises from electron trapping in pre-existing oxide traps and trap generation near the oxide/GaN interface. Permanent damage after harsh stress is induced in both oxide systems but of a different nature. In SiO₂ transistors, non-recoverable interface state generation takes place. In SiO₂/Al₂O₃ MOSFETs, trap states in the oxide close to the semiconductor interface appear to be created. These findings are consistent with studies on other semiconductor material systems.

In chapter 4, we focus on the study of NBTI. We will discuss measurement results, analysis and modeling of NBTI at various stress voltage and temperatures for both SiO₂ and SiO₂/Al₂O₃ devices.
Chapter 4. Negative-Bias Temperature Instability (NBTI)

4.1. Introduction

In the previous chapter, we have investigated the effect of positive gate bias stress on GaN MOSFETs and compared devices with SiO₂ and SiO₂/Al₂O₃ gate dielectrics. We discussed the experimental results and proposed the physical mechanisms and model for PBTI of GaN MOSFETs. In this chapter, we present a detailed study of negative gate stress on GaN MOSFETs. We again focus our study on the investigation of \( V_T \) shift, \( S \) change, and \( g_{m,max} \) degradation of different stress voltages and stress duration at different temperatures.

This chapter is organized as following. First, we give an overview of a three-regime behavior for NBTI of SiO₂/Al₂O₃ GaN MOSFETs. Next, for each of the three regimes, we discuss in detail the experimental results. We then analyze these results and propose the working mechanisms behind NBTI. In addition, we compare the NBTI experimental results of SiO₂ MOSFETs with SiO₂/Al₂O₃ MOSFETs and discuss their similarities and differences. At the end of this chapter, we summarize our findings for NBTI of GaN MOSFETs.
The GaN MOSFETs used in our NBTI study have the same device structure as shown in Figure 2-1. The devices have the same geometrical dimensions as those used in Chapter 2. However, the fabrication process has been updated since our PBTI study and, as a result, the virgin devices studied in this chapter show different initial characteristics from those used in our PBTI study. In addition, for the present NBTI study, we use two sets of devices from two different fabrication process (process 1 and process 2), which also results in minor differences in our experimental data. We first use one set of devices for our NBTI study described in section 4.2 and 4.3 (SiO$_2$/Al$_2$O$_3$ MOSFETs only, process 1), and then we use a second set of devices to compare SiO$_2$ and SiO$_2$/Al$_2$O$_3$ MOSFETs (process 2).

The standard figures of merit for virgin devices used in our NBTI study in the saturation regime ($V_{DS} = 10$ V) are as follows: SiO$_2$/Al$_2$O$_3$ devices from process 1 used in section 4.2 and 4.3: $V_{Sat} \sim -0.8 \text{ V}$, $S \sim 188 \text{ mV/dec}$, and $g_{m,max} \sim 28 \text{ mS/mm}$. SiO$_2$ devices from process 2 used in section 4.4: $V_T \sim 0.1 \text{ V}$, $S \sim 226 \text{ mV/dec}$, $g_{m,max} \sim 18 \text{ mS/mm}$. SiO$_2$/Al$_2$O$_3$ devices from process 2 used in section 4.4: $V_T \sim -1.9 \text{ V}$, $S \sim 304 \text{ mV/dec}$, $g_{m,max} \sim 16 \text{ mS/mm}$. Similar to our PBTI study, our NBTI work focuses on the impact of negative gate bias stress on device behavior through figures of merit defined in the linear operating region (at $V_{DS} = 0.1$ V). Virgin devices used in this work exhibit values of $V_T = 0.21 \text{ V}$ with a standard deviation of 0.06 V, $S = 157 \text{ mV/dec}$, and $g_{m,max} = 0.85 \text{ mS/mm}$ for SiO$_2$/Al$_2$O$_3$ MOSFETs in section 4.2 and 4.3 (process 1), $V_T = 1.1 \text{ V}$ with a standard deviation of 0.1 V, $S = 175 \text{ mV/dec}$, and $g_{m,max} = 0.55 \text{ mS/mm}$ for SiO$_2$ MOSFETs in section 4.4 (process 2) and $V_T = -2.9 \text{ V}$ with a standard deviation of 0.15 V, $S = 255 \text{ mV/dec}$, and $g_{m,max} = 0.57 \text{ mS/mm}$ for SiO$_2$/Al$_2$O$_3$ MOSFETs in section 4.4 (process 2).

The detailed experiment flow for NBTI stress experiments follows those described in section 2.4. The main variations between NBTI and PBTI experiments are the extraction of
and the added C-V characterization. First, to extract \( g_{m,\text{max}} \) during stress we use \( V_T + 1.5 \) V as the upper bound of \( V_{GS} \) for an \( I_D-V_{GS} \) sweep. For harsh stress conditions where \( S \) is severely degraded and a larger \( V_{GS} \) range is needed to extract \( g_{m,\text{max}} \), we use two identical devices for each stress period and increase the upper bound of \( V_{GS} \) in an \( I_D-V_{GS} \) sweep. In addition, we also perform C-V characterization to understand better the impact of electrical stress on the electrostatics of the device.

### 4.2. Overview: A Three-Regime Behavior

Our study shows a peculiar three-regime behavior for \( V_T \) and \( S \) of GaN MOSFETs under negative gate bias stress. The progression of this behavior can be seen in Figure 4-1. In this experiment, we apply gate stress, \( V_{GS,\text{stress}} = -10 \) V for \( 10^4 \) sec at \( T = 175^\circ \text{C} \), and monitor the stress time evolution of \( V_T \) and \( S \). For short stress time \( (t_{\text{stress}}) \), \( \Delta V_T \) is negative. As \( t_{\text{stress}} \) increases, \( \Delta V_T \) becomes positive and continues to increase with \( t_{\text{stress}} \) until \( t_{\text{stress}} \sim 100 \) s. Beyond 100 sec, \( \Delta V_T \) starts to decrease and eventually becomes negative again. After the removal of stress and after the thermal detrapping step \( (\text{TD}) \), a residual negative \( \Delta V_T \) (open symbol at right) that is not recoverable is observed. In the course of the same experiment, the subthreshold swing \( S \) first increases with stress time, then peaks around 1,000 sec and then starts recovering. At the end of the experiment, after thermal detrapping, a residual degradation of \( S \) is also left. In general, the \( V_T \) shift follows a negative-positive-negative pattern, and our study focuses on each of the three regimes in detail.
4.3. Experimental Results and Discussion of SiO₂/Al₂O₃ Devices

4.3.1. Regime 1 (low-stress)

In Figure 4-1 we see that $V_T$ shift is negative at the beginning of the stress (short $t_{stress}$). This turns out to be true for low $|V_{GS,\text{stress}}|$, low $T$ (room temperature or below) and short $t_{stress}$ conditions, which we call the "low-stress regime". In this regime, we observe a negative $\Delta V_T$ with a magnitude that increases with time. On the other hand, $\Delta S$ is negligible. This is seen in Figure 4-2 where we show $\Delta V_T$ and $\Delta S$ as a function of $t_{stress}$ for $V_{GS,\text{stress}} = -1$, -3 and -5 V, up to $t_{stress} = 10^4$ sec at room temperature. During the stress period, $\Delta V_T$ is negative with a magnitude that increases with $V_{GS,\text{stress}}$ and $t_{stress}$ but eventually saturates. For $V_{GS,\text{stress}} = -5$ V, $\Delta V_T$ peaks and then turns around after $t_{stress} = 1000$ s, which indicates the onset of regime 2. For all three stress voltages, we see minimal $\Delta S$.

The recovery of $\Delta V_T$ and $\Delta S$ after removal of stress are also shown on the right side of Figure 4-2. For $V_{GS,\text{stress}} = -1$ and -3 V, $V_T$ completely recovers at ~ 1000 s. For $V_{GS,\text{stress}} = -5$ V,
$V_T$ first recovers and then overshoots at $t_{\text{stress}} = 300$ sec, and eventually recovers completely after thermal detrapping. The $V_T$ overshoot for $V_{\text{GS,stress}} = -5$ V could be the result of the long recovery time constant of regime 2. This means that as device recovers from the negative $V_T$ shift in regime 1, the positive $V_T$ shift in regime 2 has not recovered, which sum to be a positive $V_T$ shift during recovery. We also find that the change in $g_{\text{n, max}}$ is also minimal and completely recovered (not shown).

![Graphs showing AVT and AS as a function of stress time (extracted 1 s after removal of stress) and during subsequent recovery, for $V_{\text{GS,stress}} = -1$, -3, and -5 V at RT. Open symbols at the end of recovery represent AVT and AS after thermal detrapping (TD).](image)

**Figure 4-2.** $AV_T$ and $AS$ as a function of stress time (extracted 1 s after removal of stress) and during subsequent recovery, for $V_{\text{GS,stress}} = -1$, -3 and -5 V at RT. Open symbols at the end of recovery represent $AV_T$ and $AS$ after thermal detrapping (TD).

In Figure 4-3, we compare $I_D-V_{\text{GS}}$ and $C_g-V_G$ characteristics before stress, after stress and after thermal detrapping for a device subjected to -1 V stress for $10^4$ sec at RT. In both cases, we
see a simple parallel $V_T$ shift that completely recovers. This is consistent with the observation of the transient negative $V_T$ shift in regime 1 with minimal $S$ and $g_{m,max}$ change.

![Figure 4-3. $I_D$-$V_{GS}$ and $C_G$-$V_G$ characteristics of a device before stress, after stress and after thermal detrapping (TD), for $V_{GS,\text{stress}} = -1$ V, $t_{\text{stress}} = 10,000$ s at RT.](image)

We have also studied the impact of temperature in regime 1 by performing NBTI stress experiments for $V_{GS,\text{stress}} = -1$, -1.5 and -2 V at different temperatures. In Figure 4-4 we compare the stress time evolution of $V_T$ for $T = -40^\circ$C, -10°C, and at RT in a log-log plot. In these experiments, we focus only on the $V_T$ and $S$ extraction during stress to shorten experiment time so we can repeat the experiment multiple times to obtain precise data for modeling purposes. In all cases, we see that the data follow a simple power law with exponent $n = 0.28$ to 0.4, and show a weak temperature dependence. This suggests that the trapping process in regime 1 takes place mostly through tunneling.
Figure 4-4. Stress time evolution of $|\Delta V_T|$ for $V_{GS,\text{stress}} = -1$ to $-2$ V, at $-40^\circ C$, $-10^\circ C$ and RT.

All our observations are consistent with electron detrapping from oxide traps close to the oxide/semiconductor interface and subsequent retrapping when the device is brought to rest [65]. Similar NBTI behavior has been reported in Si MOSFETs [57], [66] and SiC MOSFETs [44]. This is, in essence, the inverse process of the positive bias temperature instability (PBTI) studies carried out earlier in similar devices [67]. Interestingly, later we find a symmetrical continuum of $V_T$ shift for PBTI and NBTI for low-stress conditions. The details of the experimental results and modeling of that study are outlined in chapter 5.

4.3.2. Regime 2 (mid-stress)

As stress increases, (higher $V_{GS,\text{stress}}$, longer $t_{\text{stress}}$, or higher $T$), the initial negative $\Delta V_T$ becomes positive, and the device behavior transitions from regime 1 to regime 2 (the “mid-stress regime”). Figure 4-5 shows an example of this transition with $V_{GS,\text{stress}} = -5$ V at $-45^\circ C$, RT and $125^\circ C$, for $t_{\text{stress}} = 10,000$ sec. First, as we increase $T$ from $-45^\circ C$ to RT, we see a negative $V_T$
shift, which is the typical behavior of regime 1. $|\Delta V_T|$ increases with $t_{\text{stress}}$ and $T$ as expected. As $T$ increases from RT to 125°C, the initial negative $\Delta V_T$ turns around and becomes positive, and continue to increase in the positive direction as $t_{\text{stress}}$ increases. At the same time, we also observe an increase in $S$ as the temperature increases from RT to 125°C. $\Delta S$ also increases with $t_{\text{stress}}$ for $T = 125°C$.

In this experiment, both $V_T$ and $S$ are completely recovered after thermal detrapping (open symbols on the right). Another observation from Figure 4-5 is that the time evolution of $\Delta V_T$ and $\Delta S$ seem to follow a similar trend. For that, we plot $\Delta V_T$ vs. $\Delta S$ throughout the stress

![Figure 4-5](image-url)
and recovery periods (Figure 4-6). As expected, $\Delta V_T$ and $\Delta S$ are linearly correlated throughout the entire stress and recovery. This indicates that the temporary positive $V_T$ shift and $S$ increase in regime 2 arise from a common physical origin.

![Figure 4-6. Correlation of $\Delta V_T$ and $\Delta S$ during stress and recovery for $V_{GS,\text{stress}} = -5$ V at 125°C. $\Delta V_T$ and $\Delta S$ are linearly correlated.](image)

Our observation from Figure 4-5 and Figure 4-6 signifies the regime 2 behavior in our NBTI studies: a temporary, positive $V_T$ shift accompanied by a temporary $S$ increase, with $\Delta V_T$ and $\Delta S$ linearly correlated.

In order to study regime 2 in more detail, we find a set of stress conditions to isolate regime 2 from regime 1 and 3. Figure 4-7 summarizes the experimental results under these conditions. We show the stress time evolution of $\Delta V_T$, $\Delta S$, and $\Delta g_{m,\text{max}}$ for $V_{GS,\text{stress}} = -10$ to -20 V at RT, and for $V_{GS,\text{stress}} = -10$ V at 75, 100 and 125°C. In addition to the positive $\Delta V_T$ and the accompanying $\Delta S$, there is a minor $g_{m,\text{max}}$ drop. All three parameter shifts are enhanced by
higher $V_{GS,\text{stress}}$, longer $t_{\text{stress}}$, and high $T$. In addition, $\Delta V_T$ and $\Delta S$ both follow a log-time dependence with a $T$-independent slope. After thermal detrapping, $\Delta V_T$, $\Delta S$, and $\Delta g_{\text{in,max}}$ mostly recover, except for the harshest stress condition of $V_{GS,\text{stress}} = -20$ V at $T = 125^\circ$C, where residual $\Delta V_T$ (negative), $\Delta S$, and $\Delta g_{\text{in,max}}$ are observed. This residual permanent degradation indicates a transition from regime 2 to regime 3.

![Figure 4-7](image)

Figure 4-7. Stress time evolution of $\Delta V_T$, $\Delta S$ and $\Delta g_{\text{in,max}}$ for (a) $V_{GS,\text{stress}} = -10$, -15 and -20 V at RT, and (b) $V_{GS,\text{stress}} = -10$ V at RT, 75°C, 100°C, 125°C

The positive $\Delta V_T$ in regime 2 is in opposite direction from what has been reported for NBTI in other material systems, but it is consistent with a recent study on a similar recessed gate
E-mode GaN MOSFET structure [68]. Authors in [68] observe a positive $V_T$ shift in E-mode GaN MOSFETs with recessed gate, and suggest that electron injection from the metal gate and the subsequent trapping of electrons in the GaN channel is the dominant mechanism for the positive $V_T$ shift. However, this conclusion is solely based on a singular stress condition ($V_{GS,\text{stress}} = -8$ V for 30 sec), and $V_T$ is the only parameter studied. In our studies, gate injection was also considered as a possible mechanism for regime 2; however, we did not observe any change in gate current before and after stress in regime 2, which leads us to believe that there is a different mechanism behind regime 2. In addition, gate electron injection should not result in a recoverable change in the subthreshold swing.

In order to gain a deeper understanding of the temporary positive $V_T$ shift in regime 2, we also measure the $C_{G,SD}$-$V_G$ characteristics before and after stress as shown in Figure 4-8. In this measurement, we focus on the capacitance between the gate and source/drain while keeping the

![Figure 4-8. $C_{G,SD}$-$V_G$ characteristics before and after $V_{GS,\text{stress}} = -20$ V at RT for 1,000 s and after subsequent thermal detrapping. The body is floating.](image-url)

Temporary charge buildup

$V_G$ [V]
body floating. This measurement confirms the temporary positive shift of $V_T$ and reveals the appearance of a temporary charge buildup around threshold after stress, which disappears with subsequent thermal detrapping.

These observations suggest that the increase in $S$ and the shift in $V_T$ in Figure 4-5 and Figure 4-7 could arise from field-induced electron trapping in the GaN channel under both edges of the gate on the source and drain sides [69]. Electron trapping in the channel can take place under high reverse electric-field when electrons tunnel from the valence band to trap states in the GaN channel in a process sometimes referred to as Zener trapping. This is sketched in Figure 4-9. A process of this kind under the edge of the field plate has been shown to result in a total current collapse in GaN MIS-HEMTs after high-voltage OFF-state stress [69].

![Figure 4-9](image)

Figure 4-9. (a) Zener trapping mechanism as suggested in [69]. Electrons tunnel from the valence band into defect states (ET) under high vertical electric field in the GaN channel caused by high reverse bias stress. (b) Electrons are trapped in the GaN channel under the source and drain edges of the gate. (c) High electron trapping lifts up the energy bands at the surface of the GaN channel shifting the threshold voltage positive under the edges of the gate and effectively increasing the local hole concentration. After stress removal, electron detrapping takes place through thermal processes.
In the present work, the electric field at the edges of the gate is quite high, which induces Zener trapping in the GaN substrate. High electron trapping lifts the energy bands up in the GaN channel effectively increasing the local hole concentration under both edges of the gate (Figure 4-9 (b), (c)). This shifts $V_T$ positive as well as increases the subthreshold swing. Both effects are temporary, because, after removal of stress, a thermal process is effective in detrapping electrons, as the thermal barrier is relatively low at the edges of the gate. As electrons detrap, the device eventually relaxes to its original state (Figure 4-9 (c)). This trapping/detrapping process is possibly related to deep C traps with an energy level reported to be 2.85 eV from the conduction band edge of GaN [70]. This mechanism runs in parallel with that of regime 1 and eventually overwhelms it. It is completely recoverable.

**4.3.3. Regime 3 (high-stress)**

For harsh stress conditions, an additional negative $V_T$ shift is non-recoverable, as seen in Figure 4-1 and Figure 4-7. In the course of a stress experiment, this permanent degradation is often masked by regime 2 but it becomes evident after thermal detrapping. As shown in Figure 4-10, this non-recoverable negative $V_T$ shift is accompanied by a non-recoverable increase in $S$ and a permanent decrease in $g_{m,max}$. This permanent degradation is the typical behavior in regime 3. Also observed in Figure 3-7 is that the degradation becomes more severe with higher $t_{stress}$ and $V_{GS,stress}$. The permanent degradation observed in these experiments is also accelerated by $T$, as shown in Figure 4-11, where we plot the final $\Delta V_T$, $\Delta S$, and $\Delta g_{m,max}$ after thermal detrapping for $V_{GS,stress} = -70$ V and $T = -45^\circ C$, RT and 125°C.
Figure 4-10. $\Delta V_T$, $\Delta S$ and $\Delta g_{m,max}$ (a) immediately after stress at RT for $V_{GS,\text{stress}} = -10$, -30, -50 and -70 V, and (b) after thermal detrapping performed along the same experiment.

Figure 4-11. $\Delta V_T$, $\Delta S$ and $\Delta g_{m,max}$ after thermal detrapping at different times in stress experiments. $V_{GS,\text{stress}} = -70$ V and $T = -45^\circ$C, RT and 125$^\circ$C.
Figure 4-12. Correlation of (a) permanent $\Delta V_T$ and permanent $\Delta S$ and (b) permanent $\Delta g_{m,\text{max}}$ and permanent $\Delta S$ for $V_{GS,\text{stress}} = -50$ and -70 V at different T.

In addition, we also see that the permanent shift in $V_T$, $\Delta S$, and $\Delta g_{m,\text{max}}$ are well correlated for $V_{GS,\text{stress}} = -50$ and -70 V at T = -45°C, RT and 125°C as indicated in Figure 4-12.

In Figure 4-13, we see the changes in $I_D$-$V_{GS}$ and $C_V$-$V_{GS}$ characteristics. After stress and thermal
detrapping, there is a prominent negative threshold voltage shift and degradation of $S$ that correlates with a softening of the C-V characteristics around threshold. This is all consistent with the formation of interface states because of, perhaps, broken H bonds at the oxide/semiconductor interface. Similar phenomena are well documented in high-k/Si [9], [10] and Al2O3/InGaAs MOSFETs [11].

To summarize, in this section, we have identified three degradation mechanisms that are responsible for NBTI in SiO2/Al2O3 GaN MOSFETs. Under low-stress (regime 1), recoverable electron detrapping from pre-existing oxide traps close to the oxide/GaN interface takes place, which causes a negative, recoverable $V_T$ shift. Under mid-stress (regime 2), an additional transient positive $V_T$ shift is observed that is accompanied by a temporary increase in $S$. This appears to be caused by electron trapping in the GaN channel under the edges of the gate, and the subsequent detrapping after removal of stress. Under high-stress conditions (regime 3), there is also a permanent negative $V_T$ shift and permanent degradation in $g_{m,max}$ and $S$. This is consistent with interface state generation that is well-studied in Si MOSFETs and other material systems. These findings serve as the foundation to compare NBTI behavior for GaN MOSFETs with different gate dielectrics and should be instrumental in understanding the more complex instability issues of GaN MIS-HEMTs.

4.4. SiO2 vs. SiO2/Al2O3 Devices

In this section, we compare negative-bias temperature instability (NBTI) in GaN MOSFET with SiO2 vs. SiO2/Al2O3 (Al2O3 next to GaN channel) gate dielectric. This study
extends our work of NBTI in SiO₂/Al₂O₃ composite gate dielectric devices (section 4.2 and 4.3). Electrical characteristics of the devices studies in this session are outlined in 4.1.

4.4.1. Effect of Negative Bias Stress at Room Temperature

We first compare NBTI of SiO₂ vs. SiO₂/Al₂O₃ devices at room temperature.

Figure 4-14 shows the stress time evolution of V_T shift (ΔV_T) and change in S (ΔS) of devices subjected to V_{GS, stress} = -20 V at RT for 10³ sec. Both SiO₂ and SiO₂/Al₂O₃ devices show a positive V_T shift accompanied by an increase in S. However, both V_T shift and S changes in SiO₂ are much larger. At the end of the experiment, after thermal detrapping, both V_T and S of SiO₂/Al₂O₃ devices completely recovered. For SiO₂ devices, there is a negative, permanent ΔV_T and a non-recoverable ΔS. For both dielectrics, ΔV_T and ΔS are linearly correlated throughout the stress and recovery cycles (Figure 4-15).

These observations are consistent with the regime 2 behavior reported in section 4.2 and 4.3 in which V_T shift and S increase are both due to electron trapping in the GaN substrate under both edges of the gate. The well-matched evolution of ΔV_T and ΔS in both types of oxides again strongly suggests an oxide-independent trapping mechanism. For SiO₂ devices, we see a larger V_T shift and S increase, and a final permanent negative ΔV_T and finite ΔS. The reason for larger V_T shift and S increase in SiO₂ devices is probably due to the fact that there are less pre-existing SiO₂ traps compared to Al₂O₃ [38], [48]. As a result, SiO₂ devices show a smaller regime 1 effect (negative V_T shift). Indeed, here we see minimal negative V_T shift for SiO₂ devices. As such, the positive V_T shift appears to be larger. The final permanent negative ΔV_T and finite ΔS are in line with transitioning from regime 2 to regime 3, which was attributed to interface state generation. Interestingly, we have also observed more prominent interface state generation in similar SiO₂ devices compared to SiO₂/Al₂O₃ devices during PBTI experiments (chapter 3).
early onset of regime 3 in SiO₂ devices is probably due to faster interface state generation at the SiO₂/GaN interface, which has been reported to have lower quality compared to Al₂O₃/GaN [71].

Figure 4-14. ΔVₜ and ΔS as a function of stress time for V₆₅₆₆stress = -20 V at RT. The open symbols at the end indicate final ΔVₜ and ΔS after a benign thermal detrapping (TD) step.

Figure 4-15. ΔVₜ and ΔS are linearly correlated during stress and recovery for V₆₅₆₆stress = -20 V at RT.
Figure 4-16. $\Delta V_T$ and $\Delta S$ as a function of stress time for $V_{GS,\text{stress}} = -10$ V, -20 V and -30 V at RT. The open symbols at the end indicate final $\Delta V_T$ and $\Delta S$ after a thermal detrapping (TD) step.

Figure 4-17. Correlation of $\Delta V_T$ and $\Delta S$ in SiO$_2$ devices during stress and recovery for $V_{GS,\text{stress}} = -10$ V, -20 V and -30 V at RT. $\Delta V_T$ and $\Delta S$ are linearly correlated.

In Figure 4-16, we compare stress time evolution of $\Delta V_T$ and $\Delta S$ in SiO$_2$ devices at RT for $V_{GS,\text{stress}} = -10$ V, -20 V and -30 V. The positive $\Delta V_T$ and $\Delta S$ are both enhanced by higher
After thermal detrapping, residual $\Delta V_T$ (negative) and $\Delta S$ (positive) are observed for all three stress voltages, and their magnitudes increase with $V_{GS,\text{stress}}$. For all three $V_{GS,\text{stress}}$, $\Delta V_T$ and $\Delta S$ are well correlated throughout stress and recovery (Figure 4-17). These observations are also consistent with our findings for regimes 2 and 3 in sections 4.2 and 4.3.

**4.4.2. Impact of Stress Temperature**

Next, we study the impact of temperature on both SiO₂ and SiO₂/Al₂O₃ devices. We first compare the evolution of $\Delta V_T$ and $\Delta S$ in both dielectrics for $V_{GS,\text{stress}} = -10$ V at 125°C (Figure 4-18). SiO₂/Al₂O₃ devices show a positive $\Delta V_T$ and an increase in $S$. After thermal detrapping, there is a permanent $\Delta V_T$ (negative) and $\Delta S$ (positive) in both devices. For SiO₂ devices, as the stress time increases, $V_T$ first shifts positive and then turns around and eventually becomes negative. $S$ for SiO₂ first decreases, and then increases. After thermal detrapping, there is a permanent, negative $\Delta V_T$ and $S$ increase.

![Figure 4-18. $\Delta V_T$ and $\Delta S$ as a function of stress time for $V_{GS,\text{stress}} = -10$ V at 125°C. The open symbols at the end indicate final $\Delta V_T$ and $\Delta S$ after thermal detrapping.](image-url)
Figure 4-19 shows the correlation of $\Delta V_T$ and $\Delta S$. For the SiO$_2$/Al$_2$O$_3$ device, $\Delta V_T$ and $\Delta S$ are linearly correlated throughout stress and recovery. This behavior again matches what we reported in section 4.2 and 4.3. For the SiO$_2$ device, $\Delta V_T$ and $\Delta S$ seem to be reversely correlated. This is probably due to the early transition from regime 2 to regime 3 for SiO$_2$ MOSFETs, where permanent negative $V_T$ shifts correspond to increased $S$. We also see for the SiO$_2$ device that $V_T$ and $S$ changes are minimal during recovery. This also indicates the regime 3 behavior.

![Graph showing the correlation of $\Delta V_T$ and $\Delta S$](image)

**Figure 4-19.** Correlation of $\Delta V_T$ and $\Delta S$ during stress and recovery for $V_{GS,\text{stress}} = -10$ V at 125°C. For the SiO$_2$/Al$_2$O$_3$ MOSFET, $\Delta V_T$ and $\Delta S$ are linearly correlated. For the SiO$_2$ MOSFET, $\Delta V_T$ and $\Delta S$ seem to be reversely correlated.

Here again, we observed a transition from regime 2 to 3 for both devices, which suggests interface state generation. For SiO$_2$, this transition happens earlier, which is probably due to its worse interface quality compared to Al$_2$O$_3$/GaN. In the case of the composite dielectric, interface state generation can also happen if the stress temperature is high enough.
Figure 4-20. $\Delta V_T$ and $\Delta S$ as a function of stress time for $V_{GS, stress} = -7.5\, V$ at $125^\circ C$, $-10\, V$ at $125^\circ C$ and $-10\, V$ at $175^\circ C$. The open symbols at the end indicate final $\Delta V_T$ and $\Delta S$ after thermal detrapping.

Figure 4-21. Correlation of permanent $\Delta T$ and $\Delta S$ during stress and recovery for all experiments reported in this work.
Figure 4-20. $\Delta V_T$ and $\Delta S$ as a function of stress time for $V_{GS,\text{stress}} = -7.5$ V at 125°C, -10 V at 125°C and -10 V at 175°C. The open symbols at the end indicate final $\Delta V_T$ and $\Delta S$ after thermal detrapping. shows the T dependence of $\Delta V_T$ and $\Delta S$ in SiO$_2$ devices with $V_{GS,\text{stress}} = -10$ V. We see that the transition from regime 2 to regime 3 is accelerated by T. In Figure 4-21, we plot the correlation of all permanent $\Delta V_T$ and $\Delta S$ values reported in this section for both types of devices. The linear correlation that is obtained confirms our attribution to interface state generation from section 4.3.

To summarize, in this section, we have compared NBTI in GaN MOSFETs with SiO$_2$ and SiO$_2$/Al$_2$O$_3$ gate dielectrics. For moderate stress, we find an identical evolution of $V_T$ and $S$ (though at different rates) in both devices consistent with substrate trapping. A significant difference is that SiO$_2$/Al$_2$O$_3$ devices fully recover while SiO$_2$ devices suffer from permanent damage caused by interface state generation. Under harsh stress, both devices exhibit permanent interface state damage (regime 3). However, transition from regime 2 to regime 3 is earlier for SiO$_2$ devices, suggesting a poorer SiO$_2$/GaN interface quality compared to the Al$_2$O$_3$/GaN interface.

### 4.5. Chapter Summary

In this chapter, we present a detailed NBTI study of GaN MOSFETs with SiO$_2$ or SiO$_2$/Al$_2$O$_3$ gate dielectric. We first showed a peculiar three-regime behavior and then presented the experimental results of SiO$_2$/Al$_2$O$_3$ MOSFETs at various stress conditions. With the analysis of the measurement data, we proposed possible mechanisms for each of the three regimes. We
also compared SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ MOSFETs under the same stress conditions and explained the similarities and differences.

We identified three degradation mechanisms that are responsible for NBTI in GaN MOSFETs. In regime 1 (low-stress), recoverable electron detrapping from pre-existing oxide traps close to the oxide/GaN interface takes place resulting a temporary negative $V_T$ shift. In regime 2 (mid-stress), a transient positive $V_T$ shift is observed that is accompanied by a temporary increase in $S$, and is probably caused by electron trapping in the GaN channel under the edges of the gate. In regime 3 (high-stress) there is a permanent negative $V_T$ shift and permanent degradation in $g_{m,max}$ and $S$. This is consistent with interface state generation.

We compared NBTI behavior in GaN MOSFETs with SiO$_2$ and SiO$_2$/Al$_2$O$_3$ gate dielectrics. In summary, both dielectrics show the three-regime behavior though the transitions from regime to regime are different. The SiO$_2$/Al$_2$O$_3$ MOSFET suffers more from the effect of regime 1, which is due to the higher amount of pre-existing oxide traps compared to SiO$_2$. On the other hand, the onset of regime 3 for SiO$_2$ MOSFETs is earlier than that of SiO$_2$/Al$_2$O$_3$ MOSFETs, suggesting a poorer SiO$_2$/GaN interface quality compared to the Al$_2$O$_3$/GaN interface.

These findings should be instrumental in understanding the more complex instability issues of GaN MIS-HEMTs.

In chapter 5, we will investigate a symmetrical continuum phenomenon that extends from PBTI to NBTI for low-stress conditions. We will present detailed measurement results, analysis and modeling of the PBTI-NBTI continuum at various stress conditions focusing on SiO$_2$/Al$_2$O$_3$ GaN MOSFETs.
Chapter 5. PBTI-NBTI Continuum in SiO₂/Al₂O₃ MOSFETs

5.1. Introduction

In chapter 3 and chapter 4, we investigated the effect of positive and negative gate bias stress on GaN MOSFETs with SiO₂ and SiO₂/Al₂O₃ gate dielectrics. Based on extensive experimental data and analysis, the physical mechanisms and models for BTI of GaN MOSFETs were presented. In general, BTI in GaN MOSFETs can cause Vₜ shifts that are either recoverable or permanent. Depending on how harsh the stress conditions are, the Vₜ shift can happen because of charge trapping/detrapping (recoverable) or defect generation (permanent). For PBTI stress (chapter 3), the recoverable Vₜ shift is found to be positive, and it is attributed to electron trapping in pre-existing oxide traps. For NBTI stress, in regime 1 (chapter 4), Vₜ shift is negative and recoverable, and this could be due to electron detrapping from pre-existing oxide traps. Other studies of benign BTI stress of GaN MIS-HEMTs reported similar Vₜ behavior [65], [72]. While some also attribute the Vₜ instability to the trapping/detrapping of pre-existing
oxide traps [47], [48], a few other mechanisms were also proposed. Meneghini et al. studied D-mode SiN/AlGaN/GaN MIS-HEMT, grown on Si substrate. It was suggested that a distribution of defects at the SiN/AlGaN interface and/or in the SiN layer are responsible for the $V_T$ drift due to reverse gate bias [65]. Huang et al. proposed trapping to acceptor-like deep states at Al$_2$O$_3$/GaN interface for the $V_T$ instability in Al$_2$O$_3$/GaN/AlGaN/GaN MIS-HEMTs [73]. Wu et al. studied the slow detrapping phenomena of positive gate bias stress in AlGaN/GaN MIS-HEMTs with a bilayer dielectric (in-situ Si$_3$N$_4$/Al$_2$O$_3$) and attribute $V_T$ shift to trapping/detrapping of donor traps at the interface between the Si$_3$N$_4$/Al$_2$O$_3$ and the AlGaN barrier layer [74]. Nevertheless, from our hypothesis, it makes sense to speculate that the trapping and detrapping phenomena responsible for PBTI and NBTI under benign gate bias stress have a common origin. In this chapter, we carry out a detailed experimental study focusing on this notion and with the goal of identifying the relevant mechanisms.

Evidently, similar investigations of benign BTI for Si and SiC MOSFETs have also suggested reversibility of PBTI and NBTI for benign stress [44], [75]. In irradiated Si MOSFETs, it was found that alternating positive and negative gate stress would cause $V_T$ to shift back and forth as a result of electrons tunneling back and forth from the Si substrate to electron traps associated with a simple oxygen vacancy (an E’ center) in the oxide [75]. This led to a reversibility effect. Similar observations were made in SiC MOSFETs with SiO$_2$ gate oxide [2]. A reversible $V_T$ shift under switching positive and negative gate stress was attributed to electrons directly tunneling to and from near-interfacial oxide traps [44]. To identify the relevant mechanisms in GaN MOSFETs, we dedicate this chapter to PBTI and NBTI under benign gate stress ($V_{GS,\text{stress}}$ from -5 V to 5 V). We study in detail the stress voltage and temperature dependence of the $V_T$ shifts. We focus on devices with SiO$_2$/Al$_2$O$_3$ gate dielectric.
In the rest of this chapter, we first present the experimental results of benign gate bias stresses at RT. Following that, the temperature dependency is discussed. With the analysis of the experimental data, we propose the physical mechanism and model that explains a symmetrical continuum of PBTI-NBTI. At the end of the chapter, a summary of our findings on benign gate bias stress of GaN MOSFETs is provided.

5.2. Experimental Results

The GaN MOSFETs studied in this chapter have the same device structure as those used in chapter 3 and chapter 4. The virgin devices exhibit values of $V_T \sim 1$ V, subthreshold swing $\sim 150$ mV/dec, and $g_{m,\text{max}} \sim 0.78$ mS/mm, all at $V_{DS} = 0.1$ V. We use the benign measurement schemes developed in chapter 2. In this chapter, the measurements of $g_{m,\text{max}}$ for both PBTI and NBTI are carried out using $I_D-V_{GS}$ sweeps that start from $V_{GS} = -0.5$ V and stop at $V_T + 1.5$ V.

5.2.1. Benign gate bias stress at room temperature (RT)

We start our experiments at RT. Figure 5-1 shows the time evolution of $\Delta V_T$ and $\Delta g_{m,\text{max}}$ under gate bias stress from -5 V to 5 V. We use one device for all PBTI experiments and another device for all NBTI experiments, and utilize thermal detrapping to reset the device in between stress voltages.

For positive $V_{GS,\text{stress}}$, $\Delta V_T$ is observed to be positive and its value increases with stress time and stress voltage. $\Delta V_T$ is completely recovered after thermal detrapping. The subthreshold swing change is minimal (not shown). These observations are consistent with what we discussed in chapter 3. We also observe $g_{m,\text{max}}$ degradation that is accelerated by stress time and stress voltage, which is also completely recovered after thermal detrapping.
For negative gate stress, the picture is nearly completely symmetric. $\Delta V_T$ is negative and its magnitude increases with stress time and the magnitude of stress voltage. This is also consistent with regime 1 behavior we discussed in chapter 4. $\Delta g_{m,max}$ under negative gate stress is positive, while $\Delta S$ is minimal (not shown). All $\Delta V_T$ and $\Delta g_{m,max}$ are recovered after thermal detrapping as shown in Figure 5-1. Also note that the regime 2 behavior, a recoverable, positive $V_T$ shift as discussed in chapter 4, starts to take over for higher stress voltages ($V_{GS, stress} = -4$ and -5 V).

Figure 5-1. Stress time evolution of $\Delta V_T$, $\Delta S$ and $\Delta g_{m,max}$ for $V_{GS, stress}$ from -5 V to 5 V at RT. The last set of points (open symbols) are $\Delta V_T$ and $\Delta g_{m,max}$ after thermal detrapping.
Figure 5-2. $\Delta V_T$ and $\Delta g_{m,\text{max}}$ well correlated throughout stress and recovery, indicating similar mechanism. Shows the correlation of $\Delta V_T$ and $\Delta g_{m,\text{max}}$ throughout stress and recovery periods for $V_{GS,\text{stress}}$ from -5 V to 5 V at RT. It is evident that the two parameters are well correlated throughout the PBTI and NBTI regimes, and that the correlation follows a continuous, linear relationship with a nearly constant slope, regardless of stress voltage and stress time. This symmetrical continuum suggests that NBTI and PBTI in GaN MOSFETs under benign stress are the result of a common reversible mechanism.

Figure 5-2. $\Delta V_T$ and $\Delta g_{m,\text{max}}$ well correlated throughout stress and recovery, indicating similar mechanism.

5.2.2. Impact of temperature

We have also investigated the temperature dependence of $\Delta V_T$ under benign gate bias stress. Devices used for the temperature study are different from those used in RT experiments. Again, we use one device for all PBTI experiments and another device for all NBTI experiments with a thermal detrapping step in between different stress voltages Figure 5-3 shows the time
evolution of $\Delta V_T$ during stress and recovery for $V_{GS,\text{stress}} = \pm 2$ V at different temperatures. For $V_{GS,\text{stress}} = 2$ V, $\Delta V_T$ increases as T increases from $-40^\circ$C to $0^\circ$C. For T = 20°C and 40°C, the initial $V_T$ shift is smaller than $\Delta V_T$ at $0^\circ$C. However, $\Delta V_T$ is accelerated for stress times longer than 20 s. The rate of recovery seems to increase with T for T ≥ $0^\circ$C. For $V_{GS,\text{stress}} = -2$ V, $|\Delta V_T|$ increases with T during stress. $V_T$ recovery rate is also accelerated by T, especially for T = 40°C. In addition, there is a fast $V_T$ shift component for PBTI ($\Delta V_T$ at $t_{\text{stress}} = 1$ s is sizable), which is negligible under NBTI stress. This suggests a fast mechanism lurking underneath that is not symmetric. All $V_T$ shifts are completely recovered after thermal detrapping.

![Graphs showing time evolution of $\Delta V_T$ during stress and recovery at different T, for $V_{GS,\text{stress}} = 2$ V and -2 V. The last set of points (open symbols) are $\Delta V_T$ and $\Delta g_m,\text{max}$ after thermal detrapping.](image)

Figure 5-3. Time evolution of $\Delta V_T$ during stress and recovery at different T, for $V_{GS,\text{stress}} = 2$ V and -2 V. The last set of points (open symbols) are $\Delta V_T$ and $\Delta g_m,\text{max}$ after thermal detrapping.
The T dependence is more clearly seen in Figure 5-4, where we re-plot the time evolution of $\Delta V_T$ as follows. For the PBTI stress portion, $t_{\text{stress}} = 1$ s data is subtracted to remove the fast mechanism effect. For the recovery portion of both PBTI and NBTI, data are normalized to the first data point to highlight the general T dependence trend. Figure 5-4 reveals interesting T dependence of $V_T$ shift for BTI stress and recovery of GaN MOSFETs. For PBTI stress, $\Delta V_T$ change rate increases with T after 20-30 s. PBTI recovery is also activated by T. For NBTI, $V_T$ shift during stress shows clear T activated behavior. NBTI recovery, however, is largely T independent.

Figure 5-4. Time evolution of $\Delta V_T$ during stress and recovery at different T, for $V_{GS,\text{stress}} = 2$ V and -2 V. For PBTI stress, the first data points are removed to omit the effect of the fast mechanism. For PBTI and NBTI recovery, data are normalized to the first data points to show T dependence.
To take a closer look at the T dependence shown in Figure 5-4, we show here Arrhenius plot for PBTI/NBTI stress and recovery (Figure 5-5). $R_{VT}$ represents $\Delta V_T$ change rate on $\log (t)$ scale. NBTI stress shows strongest T dependence, while NBTI recovery appears to have the weakest T dependence.

Figure 5-5. Arrhenius plot of $\Delta V_T$ change rate for PBTI/NBTI stress and recovery. $R_{VT}$ represents $\Delta V_T$ change rate on log scale.
5.3. Discussion

5.3.1. Mechanisms and modeling of PBTI-NBTI symmetrical continuum

Our study reveals a symmetrical continuum of $V_T$ shift and recovery because of PBTI and NBTI for gate stress voltage from -5 V to 5 V at RT. We postulate that $V_T$ shift under these benign stress conditions is due to electron trapping in pre-existing oxide traps (PBTI stress and NBTI recovery) and electron detrapping from the same oxide traps (PBTI recovery and NBTI stress). Figure 5-6 shows energy band diagram of PBTI/NBTI stress and recovery, demonstrating that the electron trapping and detrapping are reversible processes. As a result, $V_T$ shifts under these conditions...
conditions are recoverable. Further, during electron trapping, the channel mobility temporarily decreases resulting in \( g_{m,\text{max}} \) degradation. This is probably due to increased electron charge in the near-interface oxide layer causing additional Coulomb scattering. Reversely, during electron detrapping, the channel mobility temporarily improves (\( g_{m,\text{max}} \) increase).

These phenomena align well with BTI studies of Si and SiC devices [31], [44], [75], [76]. They are also supported by PBTI studies of InGaAs MOSFETs with Al\(_2\)O\(_3\) dielectric, where pre-existing defects located in the Al\(_2\)O\(_3\) interfacial layer were found to contribute to a positive, recoverable \( V_T \) shift after PBTI stress [47], [48]. Here we present further evidence and insight on the mechanisms behind BTI under benign stress of GaN MOSFETs.

The physics of electron trapping in pre-existing oxide traps resulting from PBTI has been studied intensively for silicon systems, and the time evolution of \( \Delta V_T \) during stress is often modeled using the following power-law relationship [19]:

\[
\Delta V_{T,\text{ox}} = \Delta V_{\text{max}} \cdot \left\{ 1 - \exp\left(-\left(\frac{t}{\tau_0}\right)^\beta\right) \right\}
\]  

(1)

Where \( \Delta V_{T,\text{ox}} \) is the \( V_T \) shift due to oxide trapping, \( \Delta V_{\text{max}} \) is a function of total trap density and the location of the centroid of the trap-charge distribution inside the oxide. \( \beta \) describes the trap energy distribution, and \( \tau_0 \) is the time constant of the traps.

For NBTI stress, models describing the oxide trap related \( V_T \) shift during stress have a similar formulation as equation (1) [11], [12]\(^1\) The PBTI and NBTI recovery follows an inverse process similar to what is suggested for SiO\(_2\)/Si MOSFETs [78]\(^2\):

\[
\Delta V_{T,\text{ox}} = \Delta V_{\text{max}} \cdot \left\{ \exp\left(-\left(\frac{t}{\tau_0}\right)^\beta\right) \right\}
\]  

(2)

\(^1\) Formulation was derived with \( \beta = 1 \).
\(^2\) Formulation was derived with \( \beta = 1 \).
Using these models, we are able to gain further insights on the stress voltage and temperature dependence of benign BTI stress of GaN MOSFETs. In Figure 5-7, we model \( \Delta V_T \) throughout stress and recovery at RT for \( V_{GS,\text{stress}} \) from -5 V to 5 V. We achieve an excellent fit with parameter values shown in Table 5-1. Summary of fitting parameter values, RT

The \( \beta \) values extracted here are close to those reported in the literature for high-k dielectrics in Si, SiC and InGaAs MOSFETs: \( \beta = 0.2 \sim 0.32 \) [2], [7], [5], [6]. For PBTI stress and NBTI recovery, \( \beta \) values seem to increase with \( V_{GS,\text{stress}} \). For PBTI recovery and NBTI stress, \( \beta \) does not seem to change with \( V_{GS,\text{stress}} \). Since \( \beta \) describes trap energy distribution, this trend suggests the bias voltage dependence of accessible trap energy levels for electron trapping.

**Figure 5-7.** Model vs. experimental data of \( \Delta V_T \) evolution with stress time at RT, for (a) \( V_{GS,\text{stress}} \) from 1 V to 5 V, and (b) \( V_{GS,\text{stress}} \) from -1 V to -5 V. Symbols are the experimental data, and solid lines are the model fitting results.
Figure 5-8. Model vs. experimental data of $\Delta VT$ evolution with stress time and recovery time at $V_{GS, stress} = 2\, V$ and $-2\, V$, for $T$ from $-40^\circ C$ to $40^\circ C$. [79]. On the other hand, PBTI stress and NBTI recovery only show slight $T$ dependence, indicating electron trapping does not have the same strong $T$ dependence as electron detrapping. The temperature dependence of electron trapping and detrapping mechanism has also been reported in BTI studies in GaN MIS-HEMTs [18], [25], and more recent work of BTI in Si MOSFETs [36]. A reasonable explanation of this temperature dependence is an inelastic tunneling process, as suggested by the nonradiative multiphonon (NMP) theory [80], [81]. A more holistic model for this effect in Si MOSFET is a switching oxide trap model described in [82].

### Table 5-1. Summary of fitting parameter values, RT

<table>
<thead>
<tr>
<th>$V_{GS, stress}$ (V)</th>
<th>Stress</th>
<th>Recovery</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\beta$</td>
<td>$\tau_0$ (s)</td>
</tr>
<tr>
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<td>300</td>
</tr>
<tr>
<td>2</td>
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<td>300</td>
</tr>
<tr>
<td>3</td>
<td>0.20</td>
<td>300</td>
</tr>
<tr>
<td>4</td>
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<td>300</td>
</tr>
<tr>
<td>5</td>
<td>0.26</td>
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<table>
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<th>$V_{GS, stress}$ (V)</th>
<th>Stress</th>
<th>Recovery</th>
</tr>
</thead>
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<tr>
<td></td>
<td>$\beta$</td>
<td>$\tau_0$ (s)</td>
</tr>
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<td>500</td>
</tr>
<tr>
<td>-2</td>
<td>0.57</td>
<td>500</td>
</tr>
<tr>
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<td>500</td>
</tr>
<tr>
<td>-4</td>
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</tr>
<tr>
<td>-5</td>
<td>0.52</td>
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</table>
Figure 5-8. Model vs. experimental data of $\Delta V_T$ evolution with stress time and recovery time at $V_{GS,\text{stress}} = 2$ V and -2 V, for T from -40°C to 40°C.

Table 5-2. Summary of fitting parameter values, $V_{GS,\text{stress}} = \pm 2$ V at various T

<table>
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<th>T (°C)</th>
<th>$V_{GS,\text{stress}} = 2$ V</th>
<th></th>
<th>$V_{GS,\text{stress}} = -2$ V</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stress</td>
<td>Recovery</td>
<td>Stress</td>
<td>Recovery</td>
</tr>
<tr>
<td></td>
<td>$\beta$</td>
<td>$\tau_0$ (s)</td>
<td>$\beta$</td>
<td>$\tau_0$ (s)</td>
</tr>
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<td>400</td>
<td>0.16</td>
<td>500</td>
</tr>
<tr>
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<td>0.20</td>
<td>300</td>
<td>0.21</td>
<td>500</td>
</tr>
<tr>
<td>0</td>
<td>0.20</td>
<td>200</td>
<td>0.15</td>
<td>700</td>
</tr>
<tr>
<td>20</td>
<td>0.25</td>
<td>300</td>
<td>0.37</td>
<td>500</td>
</tr>
<tr>
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<td>0.30</td>
<td>300</td>
<td>0.60</td>
<td>200</td>
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</table>
5.4. Chapter Summary

In this chapter, we investigate BTI of GaN MOSFETs with SiO$_2$/Al$_2$O$_3$ dielectric under benign positive and negative gate bias stress. We find that $V_T$ shift and $g_{m,max}$ change under low gate bias stress ($-5 \text{ V} \leq V_{GS,\text{stress}} \leq 5 \text{ V}$) follows a linear, symmetrical continuum at room temperature. This suggests that electron trapping and detrapping in the same type of pre-existing oxide traps are responsible for the reversible $V_T$ shift in the GaN MOSFETs under low gate bias stress. A well-established oxide-trapping model for Si MOSFETs is used to model our experimental data. The fitting parameter values for all of our measurement results are presented. The modeling results further confirm our hypothesis that the behavior of the PBTI-NBTI continuum for GaN MOSFETs under benign gate bias stress is the result of a reversible oxide trapping/detrapping mechanism.

We also investigate the impact of temperature ($T$ from -40 to 40$^\circ$C) for benign gate stress $V_{GS,\text{stress}} = \pm 2 \text{ V}$. Model fitting of the temperature dependence data suggests that electron detrapping has a stronger $T$ dependence compared to electron trapping for BTI of GaN MOSFETs. This temperature dependence can be explained by the NMP theory or a switching oxide trap model proposed for Si MOSFETs.

Our findings of benign BTI stress of GaN MOSFETs in this chapter are consistent with previous studies reported in chapter 3 and chapter 4. Note that the claim of a weak temperature dependence of NBTI regime 1 made in chapter 4 considers temperature range from -40$^\circ$C to RT and uses a simple power law model. Thus, it does not present a conflict with our findings in chapter 5.
Chapter 6. Conclusion

6.1. Thesis Summary and Key Contributions

Our BTI study of GaN MOSFETs has advanced the understanding of device instabilities caused by gate bias stress in this important system. The findings outlined in this thesis are also instrumental in understanding reliability issues surrounding GaN MIS-HEMTs and will ultimately contribute to the commercialization of GaN MIS-HEMT technology in a wide range of power electronic applications.

In this thesis, we have first developed a benign experimental scheme to measure the dynamics of device electrical parameters including $V_T$, $S$ and $g_{m,max}$. There are two key features of this experimental scheme. First, since the trapping and detrapping processes responsible for BTI cover a wide range of time constants, our measurement methodology was designed with appropriate time-resolution. For example, for the extraction of $V_T$ and $S$ during a stress or a recovery period, we used “short” $I_D$-$V_{GS}$ sweeps that stopped at $I_D = 1 \mu A/mm$, the current level at which $V_T$ was defined. This $I_D$-$V_{GS}$ sweep takes ~ 1 to 2 sec, which is much shorter than the recovery time constant of the traps we are dealing with ($>>1 \ sec$). Second, we have incorporated a thermal detrapping step to “reset” the device after a stress experiment. This not
only speeds up the recovery process, but it also helps us distinguish between recoverable and permanent $V_T$ changes in GaN MOSFETs. In addition, we utilized a characterization suite written in C++ to automate the various measurement sequences. As such, we were able to acquire a large amount of experimental data within a short period time. Our experimental setup has given us a toolkit to carry out detailed and comprehensive BTI studies for GaN MOSFETs. Our approach should also be applicable to other device structures, such as the MIS-HEMT.

After developing a benign characterization scheme, we then performed detailed experimental work, analyzed a large amount of experimental data, and formulated hypothesis for the physical mechanisms behind BTI of GaN MOSFETs. The first part of our experimental work has been focused on the effect of positive gate bias stress on $V_T$, $S$ and $g_{m, max}$ (PBTI). We have compared devices with SiO$_2$ vs. SiO$_2$/Al$_2$O$_3$ dielectrics by studying stress conditions with $V_{GS, stress} = 5, 10$ and $15$ V. We have also investigated the impact of stress temperature on device behavior. Under benign stress conditions ($V_{GS, stress} \leq 10$ V, $T \leq RT$), we have observed a positive $V_T$ shift with minimal $S$ and $g_{m, max}$ change for both SiO$_2$ and SiO$_2$/Al$_2$O$_3$ MOSFETs. This positive $V_T$ shift was completely recovered after thermal detrapping. Our analysis suggests that electron trapping in pre-existing oxide traps could be the reason behind this temporary positive $V_T$ shift. Under harsh stress conditions ($V_{GS, stress} = 15$ V, $T \geq RT$), both SiO$_2$ and SiO$_2$/Al$_2$O$_3$ devices showed a non-recoverable, positive $V_T$ shift. We have also observed an increase in $S$ and degradation of $g_{m, max}$ under harsh stress conditions. For SiO$_2$ devices, $g_{m, max}$ was completed recovered after thermal detrapping, and $S$ was not recoverable, and we attribute this to interface state generation. For SiO$_2$/Al$_2$O$_3$ devices, $S$ was completely recovered, but there was a non-recoverable $g_{m, max}$ degradation, which could be a result of trap generation inside the oxide layer close to the oxide/GaN interface.
The second part of our study has been focused on GaN MOSFET device behavior under negative gate bias stress (NBTI). Our NBTI study on SiO$_2$/Al$_2$O$_3$ GaN MOSFETs has revealed a peculiar three-regime behavior of $V_T$, which corresponded to low-, mid- and high-stress regimes. At low-stress regime (regime 1), a negative, recoverable $V_T$ shift was observed. In this regime, $S$ and $g_{m,max}$ both showed minimal change. This was attributed to electron detrapping from pre-existing oxide traps. As stress voltage and temperature increase, we entered the mid-stress regime (regime 2), where a positive, recoverable $V_T$ shifts was observed. In this regime, we have also observed a temporarily increased $S$. Our analysis indicated that this positive $V_T$ shift accompanied by $S$ change could be a result of charge trapping in the GaN channel underneath the drain and source edges of the gate, where the vertical electric field was the highest. This high electric field induces so-called Zener trapping, which caused a temporary positive $V_T$ shift. In high-stress regime (regime 3), the devices show permanent $V_T$ degradation that was negative. In the meantime, $S$ and $g_{m,max}$ also showed a non-recoverable degradation. This permanent degradation was possibly a result of interface trap generation.

Our PBTI and NBTI studies revealed interesting physics behind $V_T$ instabilities of GaN MOSFETs. In general, BTI appears to be a combination of two mechanisms, the recoverable phenomenon that is the result of charge trapping/detrapping, and the permanent $V_T$ shift that is a result of defect generation. As we postulated that the electron trapping and detrapping in pre-existing oxide traps are responsible for the recoverable $V_T$ shift for PBTI and regime 1 behavior for NBTI, we have extended our investigation to the reversibility of this trapping/detrapping phenomenon. Through detailed experimental study, we have found a continuation from PBTI to NBTI under benign gate bias stress. Specifically, as we increased stress voltage from -5 V to 5 V with 1 V step, we have observed that the $V_T$ shift and $g_{m,max}$ change were symmetrical and
continuous. This observation was consistent with our earlier PBTI and NBTI studies and further confirmed that at low-stress regime, PBTI and NBTI in GaN MOSFETs were results of the inverse process of electron trapping and detrapping in the same pre-existing oxide traps.

Reliability issues surrounding GaN MIS-HEMT are major roadblocks for technology commercialization of GaN for high-voltage applications. In order to mitigate these reliability issues, it is crucial to understand the physics behind device instabilities. Our study of BTI of GaN MOSFETs contributes to the overall understanding of physics behind GaN power device instabilities so that steps can be taken to improve device reliability and extend device lifetime. Thus, our BTI study of GaN MOSFETs is crucial in advancing GaN technology and pushes forward the commercialization of GaN MIS-HEMTs for high-voltage electronic applications.

6.2. Suggestions for Future Research

With the BTI studies of GaN MOSFETs that have been carried out in this thesis, we would like to suggest additional areas of investigation for future studies to deepen the understanding of devices instabilities in GaN MIS-HEMTs.

First, it is important to identify the specific defects that are responsible for the degradation in GaN MIS-HEMTs, i.e., to investigate the microscopic origin and reveal the chemical nature of those defects. In the present thesis, we have focused on the electrical characterization of BTI of GaN MOSFETs. We have provided various physical models to describe the dynamics of electronic parameters under gate bias stress. However, defect identification and trap formation process in GaN MOSFETs still need thorough study. To understand the microscopic nature of the defects, a few techniques can be adopted from BTI
studies of Si MOSFETs. One approach is to use variations of magnetic resonance techniques to examine the physical and chemical nature of BTI related defects [83]–[85]. For example, Campbell et al. developed spin-dependent recombination (SDR) and spin-dependent tunneling (SDT) techniques to study NBTI of fully processed Si MOSFETs, and showed a dominant Pb center signal [86]. The atomic-scale defects identified in these measurements were directly linked to NBTI-induced degradation in Si MOSFETs [87], [88]. Another approach using magnetic resonance technique is called the “on-the-fly” electron spin resonance (OTF-ESR) [89], where the creation of significant amounts of E’ centers (positively charged oxygen vacancy sites) during NBTI stress was demonstrated. In addition, the recent development of time-dependent defect spectroscopy (TDDS) allows for the analysis of the capture and emission times of the defects and can be utilized to study the recovery behavior following NBTI in SiO2/Si MOSFETs [81], [90], and PBTI in high-k Si FETs [91], [92]. TDDS has also been used to characterize “border traps” [93]. TDDS work suggested strong temperature dependence of both capture and emission time constants, which will eventually contribute to the understanding of defects responsible for the recoverable component of BTI in Si MOSFETs. Adopting these techniques will bring light into the microscopic study of defects that are responsible for BTI of GaN MOSFETs and GaN MIS-HEMTs.

Second, analysis of BTI using pulsed measurements is also an important area to explore so that we can understand the fast trapping phenomenon. All of our studies on GaN MOSFETs have been based on DC stress and characterization. However, it has been found that VT instabilities in GaN devices with insulating layers also have a fast trapping component [47]. Therefore, the characterization of BTI dynamics using pulsed IV conditions is an important new area of experimental study. Further, to capture accurately fast VT dynamics under various stress
conditions, the development of a customized computer control environment for this pulsed IV system will also be necessary.

Third, device instabilities of GaN MIS-HEMTs due to other failure mechanisms, such as hot carrier injection (HCI) and time-dependence dielectric breakdown (TDDB), also need comprehensive understanding. Both HCI and TDDB have been reported as serious reliability concerns in GaN MIS-HEMTs, and a few recent studies have made significant progress in the understanding of their physics [94][21]. However, a comprehensive understanding of the charge dynamics and physical mechanisms is still lacking. One possible approach is to utilize the simple GaN MOSFET structure presented in this thesis to study HCI and TDDB, so that we can isolate the roles of the gate oxide and the oxide/GaN interface. The systematic study of BTI, HCI, and TDDB of GaN MOSFETs will provide a wholesome understanding of device instabilities in GaN MOSFETs, and ultimately contribute to the overall understanding of GaN MIS-HEMTs reliability issues.

Fourth, improved physical models are needed to describe different aspects of BTI of GaN MOSFETs and GaN MIS-HEMTs. In this thesis, we have used models developed for BTI of Si MOSFETs to describe the trapping/detrapping phenomenon of pre-existing oxide traps. This is appropriate because oxide traps are of similar nature for different material systems [51]. However, comprehensive models need to be developed to describe aspects of BTI that are unique for GaN MOSFETs and GaN MIS-HEMTs. One example is the regime 2 behavior we studied in chapter 4, where we observed a positive $V_T$ shift that was attributed to “Zener trapping” in the GaN channel. Zener trapping model was developed for Si system [95] and needs to be reformulated for GaN MOSFETs. Models describing the physical phenomena of charge trapping and defect generation at oxide/III-V interface are also lacking. To develop the relevant physical
models discussed above, it is useful to review recent models developed for BTI of Si MOSFETs. For PBTI in high-k devices, an empirical formula was recently developed to capture both fast and slow transient of the $V_T$ instability in HKMG nFETs [96]. For NBTI, a two-state model was proposed recently [82]. This model explains degradation and recovery of BTI over a wide range of bias voltages and stress temperatures in SiO$_2$, SiON, and high-k Si MOSFETs, which is a big step forward from the more traditional reaction-diffusion (RD) theory [33] and the extended reaction-dispersive-diffusion (RDD) model [97]–[99]. Similar models for GaN systems are needed to model correctly degradation mechanisms for their BTI phenomena.

Finally, it is also very important to develop appropriate lifetime models for the GaN MIS-HEMTs technology. The lifetime models should account for various physical degradation mechanisms including BTI, HCI, TDDB and other failure modes. The dominant degradation mechanisms should be identified for different processing technologies and processes so we can assess device performance accurately. The development of physical models for various degradation mechanisms will be crucial in developing these lifetime models.
Bibliography


