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Device architecture and lifetime requirements for high efficiency multicrystalline silicon solar cells

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Abstract

We present a numerical simulation study of different multicrystalline silicon materials and solar cell architectures to understand today's efficiency limitations and future efficiency possibilities. We compare conventional full-area BSF and PERC solar cells to future cell designs with a gallium phosphide heteroemitter. For all designs, mc-Si materials with different excess carrier lifetime distributions are used as simulation input parameters to capture a broad range of materials. The results show that conventional solar cell designs are sufficient for generalized mean lifetimes between 40 – 90 μs, but do not give a clear advantage in terms of efficiency for higher mean lifetime mc-Si material because they are often limited by recombination in the phosphorus diffused emitter region. Heteroemitter designs instead increase in cell efficiency considerable up to generalized mean lifetimes of 380 μs because they are significantly less limited by recombination in the emitter and the bulk lifetime becomes more important. In conclusion, to benefit from increasing mc-Si lifetime, new cell designs, especially heteroemitter, are desirable.

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Keywords: multicrystalline silicon, device simulation, PERC solar cell, carrier selective contact, heteroemitter

1. Introduction

The energy conversion efficiency of multicrystalline silicon (mc-Si) solar cells depends strongly on the quality of the wafer material and of the chosen device architecture. The quality of mc-Si wafers has increased significantly in the past decades, especially in the last few years through the refinement of the directional solidification often resulting in higher and more uniform lifetimes across the ingot [1]. An open question is to which degree increased

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lifetimes will translate into higher cell efficiencies, especially as new solar cell device architectures, like carrier selective contacts or heteroemitter designs [2, 3] are developed.

We presented earlier [4] that generalized mean values of mc-Si excess carrier lifetime distributions can be used as a quality criterion. Equation (1) shows the formula for a generalized mean value M_p of $\tau_1,\dots\tau_n$ lifetime values. The exponent p characterizes the mode of mean, e.g. $p = 1$ for the arithmetic mean, or $p = 0$ for the geometric mean. We showed in [4] that no universal p exists to describe mc-Si quality for all materials and device architectures, each mc-wafer and each device architecture have their individual p values. However, the differences are rather small and p = -0.835 is a good approximation for various materials and devices. In other words, to decide which one of two different mc-Si wafers results in a better solar cell performance, Equation (1) with a p of -0.835 can be applied to their excess carrier lifetime distributions.

$$M_p(\tau_1, \dots, \tau_n) = \left(\frac{1}{n}\sum_{i=1}^{n} \tau_i^p\right)^{1/p} \quad (1)$$

To simulate the specific behavior of mc-Si solar cells, the model described in [4] is used here. To predict solar cell efficiencies for different device architectures, numerical simulation models can be used [3-6]. We will focus in this paper on a conventional full-area BSF solar cell architecture, a PERC design with local rear contacts, and a PERC design with a high efficiency heteroemitter made of gallium phosphide [3, 6].

We will use the simple Equation (1) and the more sophisticated simulation models to show limitations of bulk lifetime and device designs.

2. Simulation models

To simulate mc-Si solar cells, the following approach is used [4]: Excess carrier lifetimes from a mc-Si wafer are discretized in a lifetime histogram having a number n of bins with different lifetime values τ_n with corresponding areas A_n. We then simulate a sequence of n monocrystalline Si cells, having a homogenous SRH bulk lifetime $\tau_n = \tau_{n0} = \tau_{p0}$ and obtain their I-V curves $I(V)_{mono,n}$. To obtain the I-V curve of the mc-Si cell, $I(V)_{multi}$, these simulated $I(V)_{mono,n}$ curves are connected in parallel in a numerical spice circuit model, using A_n as area factors.

The wafer's τ_n values are alternatively generated with a random algorithm [4] using MATLAB. Each wafer has 10^6 different lifetime values between 1 – 600 µs, as typically measured. To capture a broad range of possible materials, three generated distributions are used: low quality with M_p = 49 µs, high quality with M_p = 254 µs, and very high quality with M_p = 443 µs, where M_p is calculated using Equation (1) with p = -0.835.

Three different cell architectures are simulated. First, a "standard cell" consisting of a conventional silicon solar cell with a full-area Al-BSF and conventional phosphorus diffused emitter. Second, a "PERC cell" with local laser-fired BSFs and improved phosphorus diffused front emitter. Third, the "GaP/Si cell" [3], which is a c-Si solar cell with the same local laser fired BSFs as in the PERC cell, but a heteroemitter, made of gallium phosphide at the front side. This heteroemitter is highly n-doped and the resulting band structure allows electrons from the Si bulk material to enter the front contact but blocks the holes due to an high valence band offset (holes are the minority carrier in n-type GaP). We like to point out, that this GaP/Si cell represents a cell with an almost ideal emitter and that major technical issues have to be solved to produce these heteroemitters in mass production. The surface recombination velocities for the different devices are: 2.0×10^7 cm/s for the standard cell, 2.5×10^5 cm/s for the PERC cell and 1.0×10^3 cm/s for the GaP cell. The interface recombination velocity between GaP and Si is set to 1.0×10^2 cm/s. We discussed in Ref. [3] the influence of different recombination velocities for the GaP/Si cell and reported that the device efficiency is not strongly influenced for values up to 1.0×10^6 cm/s. These three cell architectures are simulated for 180 µm thick p-type wafers with a boron base doping of 7.2×10^{15} cm^{-3}.

For each cell in the respective cell design, the SRH bulk lifetime τ_i is ramped from 1 µs to 600 µs in steps of 1 µs (hence, we simulate a sequence of n = 600 monocrystalline solar cells, assume homogeneously distributed lifetimes in the Si bulk with $\tau_i = \tau_{n0} = \tau_{p0}$). The high end of this range of lifetimes is achievable in mc-Si after effective gettering of dissolved iron and otherwise low contamination levels, i.e. oxygen and carbon especially [7]. We use this sequence of cells for the above described mc-Si simulation model ($\tau_i = \tau_n$) and to show the individual device efficiency as a function of τ_i SRH bulk lifetime.

All solar cell simulations are carried out at 1 sun and 300 K, using the software Sentaurus Device [8]. The optical generation is calculated assuming random upright pyramids with the software Opal Version 2.6 [9]. For the GaP/Si cell, a 10 nm thin GaP layer on top of the textured silicon is assumed. The resulting *I-V* curves are corrected for metal shading and resistive losses in the metallization, as typically experienced in 15.6 × 15.6 cm^2 solar cells.

3. Simulation results

3.1. Efficiency as a function of bulk lifetime

Figure 1 shows cell efficiency as a function of SRH bulk lifetime τ_i for all three solar cell designs. Triangles represent the results of the mc-Si cell simulation using the three different lifetime distributions: low quality, high quality, and very high quality. Comparing the different cell designs, a slight variation in the triangle's τ_i values (position along the *x*-axis) is observed, and a rather big difference in absolute efficiency. Additionally the generalized mean value M_p of the three distributions is shown as dashed lines. M_p was calculated with Equation (1) with a *p* value of -0.835 and shows good agreement with the simulated results (triangles). For other mc-Si materials, Equation (1) can be used in the same way to estimate the possible efficiency for these three devices.

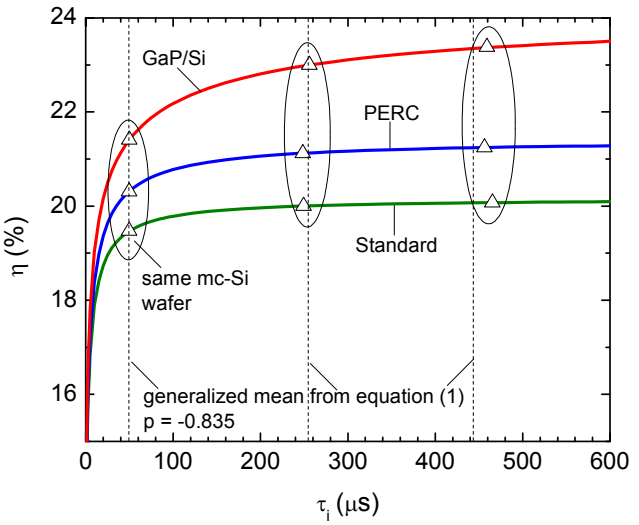

Fig. 1. The lines depict the simulated efficiency of three different solar cell designs as a function of τ_i bulk SRH lifetime. The triangles show the simulated mc-Si solar cells efficiencies for three different lifetime distributions: low quality, high quality, and very high quality. The dashed lines represent the generalized mean values of mc-Si wafers lifetime calculated with Equation (1).

3.2. Limitations of bulk lifetime

As shown in Fig. 1, the efficiency of each device plateaus above a certain critical SRH bulk lifetime τ_i. To determine this plateau as a function of device architecture, we simulate the device efficiency in the absence of bulk defects, assuming a bulk lifetime in Si of $\tau_i = \tau_{n0} = \tau_{p0} = 1$ s, to simulate the case of "infinite" SRH bulk lifetime. We like to point out, that all other recombination paths like Auger or radiative recombination are still active. From the simulated efficiency with $\tau_i = 1$ s, the previous simulated efficiencies (from Fig. 1) are subtracted. Afterwards, the percentage of these subtractions to the efficiency with $\tau_i = 1$ s is calculated and plotted as a function τ_i bulk lifetime in Fig. 2. It can be seen that the standard cell reaches close to maximum efficiency at relatively low lifetimes, followed by the PERC cell, and the GaP/Si cell needs much higher lifetimes to reach its maximum. The triangles

show the results of the above described mc-Si cell simulations, the dashed lines the generalized mean, calculated with Equation (1).

The standard and PERC cell are limited in efficiency at much lower lifetimes than the GaP/Si cell architecture, indicating that processes other than bulk recombination limit their performance. The GaP/Si cell instead continues to increase in efficiency with increasing lifetimes, indicating that other device loss mechanisms are comparable or less dominant than bulk recombination.

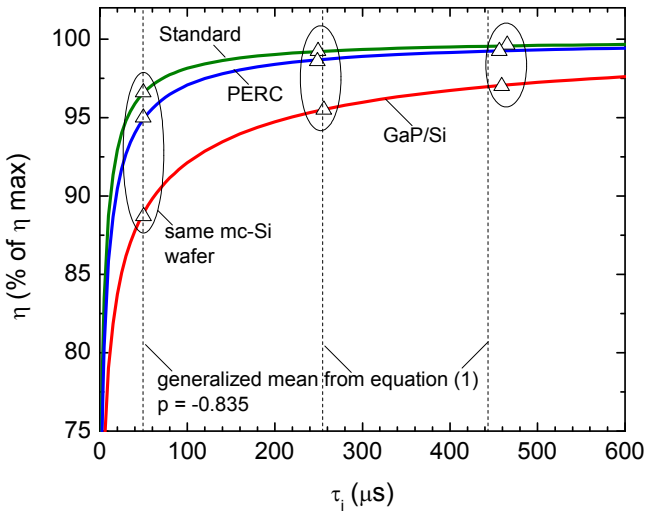

Fig. 2. Percentage of η maximum (assuming a bulk lifetime in Si of $\tau_i = \tau_{n0} = \tau_{p0} = 1$ s) as a function of τ_i bulk lifetime, obtained from Fig. 1.

3.3. Limitations of device architecture

To further understand the efficiency-limiting mechanisms of the different device architectures, we perform a loss analysis as a function of τ_i bulk lifetime for each device architecture. For this analysis, each device is divided into three different regions. The front side contains the emitter, the front passivation, and front contacts. The base region contains the wafer between the emitter and the BSF. The rear side contains the BSF, or the local rear contact, and rear-side passivation. All recombination rates caused by radiative, Auger, and SRH recombination, at the interfaces and contacts are integrated within these separate device regions. The recombination rates are multiplied by the unit charge to arrive at units of current density. In this way, the recombination losses at the front, base and rear side in a cell can be compared. This analysis is performed at the maximum power point (MPP) for each τ_i bulk SRH lifetime. The results are plotted in Fig. 3.

In the standard cell, τ_i bulk SRH lifetime dominates recombination up to approx. 40 µs above which front and rear recombination become dominant. In the PERC design, the improved emitter dominates at approx. 90 µs, and the rear becomes critical much later, at approx. 350 µs. The GaP/Si cell behaves quite differently; the losses in the heteroemitter never dominate the total losses. The rear side becomes dominant at approx. 380 µs. Looking back at Fig. 2, it becomes apparent that the efficiency potential of each given cell design is reached at wafer qualities where the front or the rear region starts to dominate the total losses. The losses at the front and the rear depend on various factors such as the phosphorus-profile, the rear passivation *etc*. and need to be assessed for each manufacturer individually. In this paper, we used the emitters and BSFs described in [3] and [10].

Note that the recombination losses at the front and rear increase with increasing bulk lifetime until the latter is not dominant anymore. This is due to the voltage at the maximum power point increases and, with this, the excess carrier density in the device. Without this non-linear effect, the SRH losses in the wafer would dominate to significantly higher mean lifetime values: up to approx. 50 µs in standard cells, 200 µs in conventional PERC cells, and far above 1 ms in PERC cells comprising a GaP emitter. Hence, such non-linear effects need to be accounted for in perspective studies.

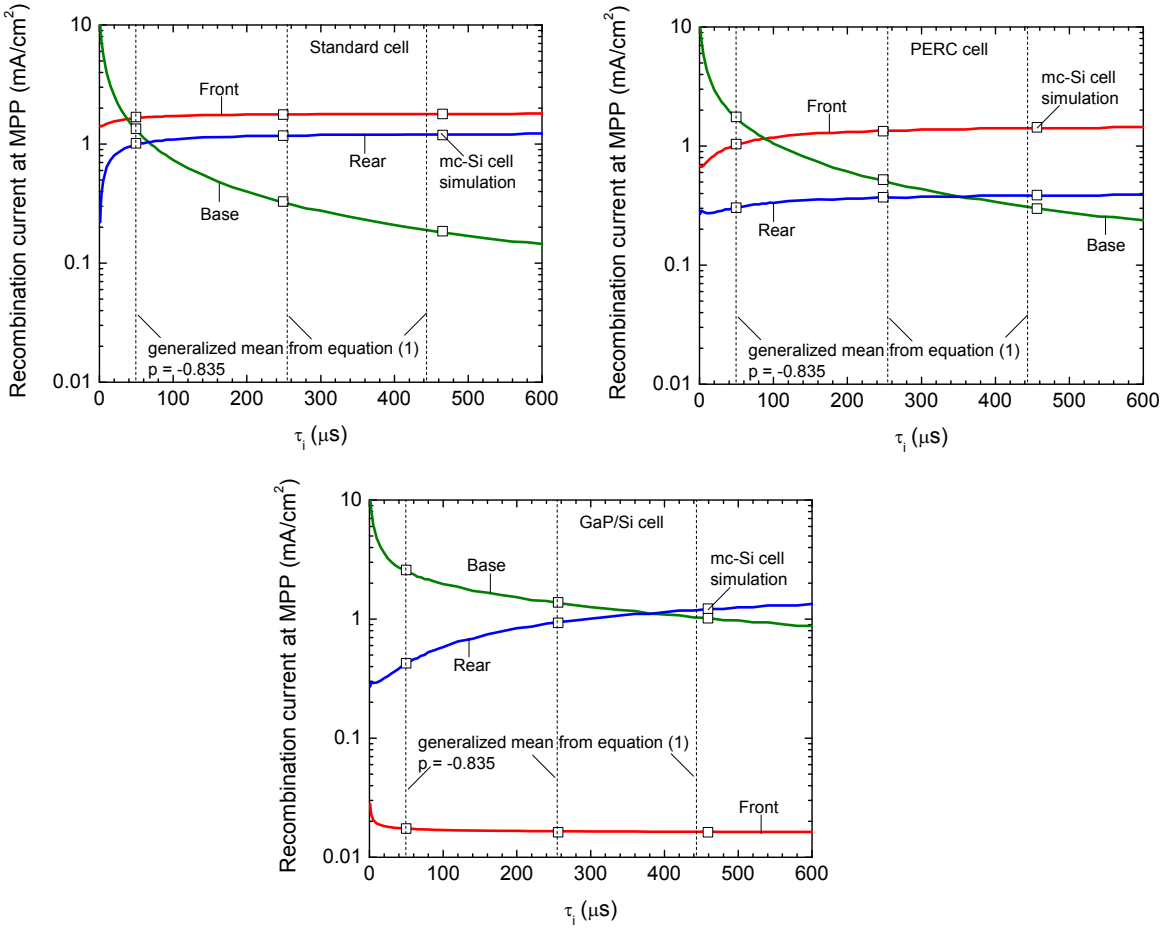

Fig. 3. Loss analysis of the three indicated solar cell architectures as a function of bulk SRH lifetime. The squares show the recombination current at MPP for the simulated mc-Si solar cells for three different lifetime distributions: low quality, high quality, and very high quality. The dashed lines represent the generalized mean values of mc-Si wafers lifetime calculated with Equation (1).

4. Conclusions and outlook

We've described a simulation analysis that reveals the device region most limiting to the device performance for any specific material and device architecture. We examined three exploratory examples of mc-Si cells and showed that their performances are limited by the τ_i SRH bulk lifetime of up to a generalized mean value (with p = -0.835) of approx. 40 µs in case of standard cells, to approx. 90 µs in conventional PERC cells, and up to approx. 380 µs in PERC cells featuring a GaP-heteroemitter emitter. In conclusion, this study emphasizes the importance of bulk

material quality, i.e. bulk lifetime and defect density, for the use in advanced cell architectures. With the lifetimes in fabricated mc-Si wafers and cells expected to be increasing in near future, this simulation study indicates material quality that is sufficient to gain from a switch in device architecture (e.g. BSF to PERC to GaP), thus fundamentally allowing mc-Si solar cells to well surpass 20% efficiency.

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