Electrically Active Defects in Zinc Oxide

by

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Abstract

Electrically active defects in semiconducting zinc oxide were studied in bulk single crystal form or in single crystal thick films deposited on *r*-plane sapphire. Electrically active defects in zinc oxide have been identified to be important factors in the description of the varistor grain boundary effect found in doped polycrystalline ceramics of zinc oxide. The goal of the study was to acquire information that would shed light on the nature of bulk defects as a function of heat treatment and doping. Bulk samples were purchased from a commercial supplier; thick film samples were fabricated using a vapor transport reactor which will have later use in zinc oxide bicrystal fabrication for single grain boundary studies of the varistor effect. Schottky contacts were fabricated on polished surfaces of zinc oxide, and the electrically active defects were evaluated with deep level transient spectroscopy (DLTS). The samples examined were either nominally undoped or, on the other hand, doped with cobalt, a relevant dopant used in commercial zinc oxide varistors. Heat treatments consisted of anneals in oxygen partial pressures of 1 atm and 10^{-4} atm at 1000°C.

Simplified varistor systems of polycrystalline bismuth- and cobalt-doped zinc oxide were also studied. The goal of this research was to evaluate electrically active defects in an actual varistor system and perhaps correlate the findings to those on bulk samples. Furthermore, a previous study has shown that the distributions of bismuth segregation at the grain boundaries in such samples can be controlled by varying microstructure and heat treatment. Current-voltage and deep level transient spectroscopy measurements were done to evaluate the corresponding electrical and defect properties. Low leakage and α values of ~30 were attained, despite the nominal, two-component doping of these simplified varistors. Moreover, by using DLTS these samples show the signature defects that are found in many multi-dopant, commercial devices: two shallow bulk traps at ~0.14 eV and ~0.24 eV and one prominent interfacial trap at ~1 eV.

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1. Introduction

Even though the word defect connotes something that is undesirable, defects play a key role in the engineering of many materials. Semiconductors rely on careful defect engineering to control their electrical conductivity and carrier type so that one is able to build functional devices and integrated circuits. Oxide ceramics, many of which are wide bandgap semiconductors, also rely on defect engineering to attain some of the unusual properties they exhibit. For example, many gas sensors use the defect properties of ceramics to detect potentially harmful emissions from cars or factories. Furthermore, the combination of grain boundaries and point defects has lead to interesting phenomena as found in ZnO varistors, $(Sr,Ba)TiO_3$-based boundary layer capacitors, and positive temperature coefficient (PTC) thermistors. These phenomena are specific to the material's grain boundaries and are not exhibited in their single crystal counterparts.

1.1 Goals of the Thesis

The goal of this thesis is to investigate the nature of electrically active defects in zinc oxide, either in single crystal films or polycrystalline ceramics, as related to its peculiar grain boundary electrical characteristics. The motivation for understanding defects is to gain a deeper understanding of their fundamental roles as "grain boundary activators" in commercial varistors. Understanding the nature of defects and how they affect the grain boundaries is the first step in connecting the grain boundary chemistry with its electrical behavior. Because commercial varistors are often very complicated, consisting of secondary phases and multiple dopants, the work in this thesis centered on examining simpler systems that would yield useful information that could be extended to more complex systems. Single crystals were used to investigate the defect character of doping and processing, and chemically simple polycrystalline ceramics were used to investigate both defect character and I-V electrical properties. The work on single crystal growth of ZnO films was also developed in a way such that bicrystals with large, well-defined single boundaries could later be studied.

1.2 Organization of the Thesis

Having described the motivation for doing this work, the thesis is organized as follows. Chapter 2 gives necessary background information related to zinc oxide and zinc oxide varistors. It presents the accepted model of metal/ZnO and ZnO-ZnO interfacial junctions that is used in explaining the electrical characteristics, a review of the literature concerning deep levels in zinc oxide, and information on vapor transport. Chapter 3 discusses the deep level transient spectroscopy (DLTS) measurement technique as applied to Schottky barriers and electrically active grain boundaries, describing two techniques of using the lock-in amplifier as the DLTS rate window. Computations presented in the literature are extended to our system, and the results prove useful for computing a new set of time constants (detailed in Appendix A). The computations show an important distinction in the phase of the fundamental of the Fourier transform from those found in the literature. The experimental approach is outlined in Chapter 4. Chapter 5 considers vapor phase growth of zinc oxide, including the experimental setup and parameters used in the production of ZnO films on *r*-plane sapphire. X-ray data is presented as an evaluation of the film crystallinity. Also included are the results of I-V, C-V, and DLTS measurements. Chapter 6 provides a description of the simplified, "primitive" BiCo:ZnO varistors and recounts I-V and DLTS measurements attained on these samples. Chapter 7 discusses the results found in the previous two chapters, and Chapters 8 and 9 close this dissertation with a summary and suggestions for future work.

2. Background

2.1 ZnO Varistor Fundamental Electrical Properties

Since the late 1970's, doped polycrystalline zinc oxide has been known to exhibit a nonlinear current-voltage (I-V) characteristic. Because of this striking nonlinearity, this particular electroceramic has served as an overvoltage circuit protector which can sense and limit transient voltage surges repeatedly without being destroyed. The I-V curve resembles that of back-to-back diodes and, hence, limits current in both polarities. These devices can be designed to operate over the range of high voltages for usage in the power industry to low voltages for semiconductor applications. In addition, the speed of these devices and their high nonlinearity factors have made zinc oxide the dominant material for overvoltage applications, supplanting the previously dominant material, silicon carbide. Functionally, as shown in Figure 2.1, at biases below a characteristic breakdown voltage V_B, the device is essentially an insulator.

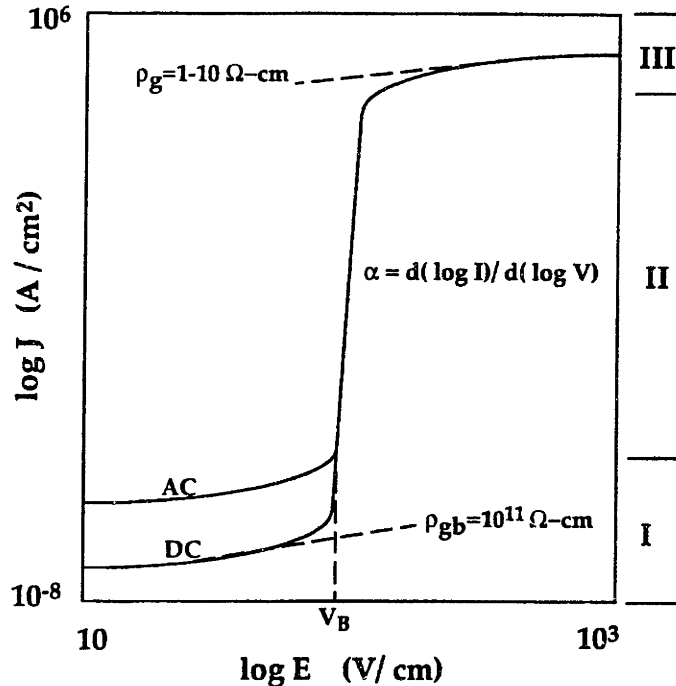


Figure 2.1 A schematic log I-log V curve of a ZnO varistor over a wide current density and electric field range. Region I is the prebreakdown regime; region II is the breakdown regime; and region III is the upturn regime.

Thus, connecting the device in parallel with a load does not disturb the load's normal operation. If, however, transient voltages above V_B were to occur, the resistivity of the device decreases precipitously, shorting the load to protect it from dangerous current levels. When the voltage settles back down below V_B, the device regains its insulator properties, ready for the next voltage surge. Such devices with voltage-dependent resistances have been dubbed "varistors." [1]

Three main regions of operation are evident from Figure 2.1: (I) the prebreakdown regime, (II) the breakdown regime, and (III) the upturn regime. V_B is engineered such that it is very close to the load's normal operating voltage. A normally operating varistor is kept just below V_B in the prebreakdown region and jumps into the breakdown region when a dangerous voltage surge occurs. The striking nonlinearity is a direct consequence of a space charge barrier breakdown located at the grain boundaries in the polycrystalline zinc oxide. Undoped polycrystalline zinc oxide does not manifest this nonlinearity. It is well-established that the nonlinearity can only be induced by the addition of key dopants that activate the boundaries. In general, the key ingredients that have been identified to lead to effective varistor action are: (a) deep donors (e.g. Co, Mn), (b) segregants (e.g. Bi, Pr), and (c) an oxidative anneal with slow cool. The combination of these three factors, either independently or synergistically, cause space charge barriers to form at the grain boundaries. Hence, the prebreakdown regime is dominated by the high resistance of the grain boundaries caused by the presence of electrostatic barriers, and the upturn regime is dominated by the grain resistance, as the grain boundary potential barriers have been overcome at large voltages ($>V_B$). The degree of nonlinearity is quantified by a parameter called the α value, where α is the slope of the log I-log V curve in the breakdown region. The α values can range from ~10 for poor varistors to ~100 for good varistors. Comprehensive reviews of zinc oxide varistors have been given by Gupta [1] and Levinson and Philipp [2].

The grain boundary phenomenon has been widely studied in terms of single boundary-type measurements. The most obvious correspondence of the varistor effect to individual zinc oxide grain boundaries lies in the breakdown voltage V_B. If one varistor is twice as thick as another identically processed one, the thicker varistor's breakdown volt-

age is two times higher than the thinner one's. This is so presumably because the thicker sample has twice as many grain boundaries between the electrodes. Individual measurements on single grain boundaries confirm their role as the determining factor in a device's nonlinearity.

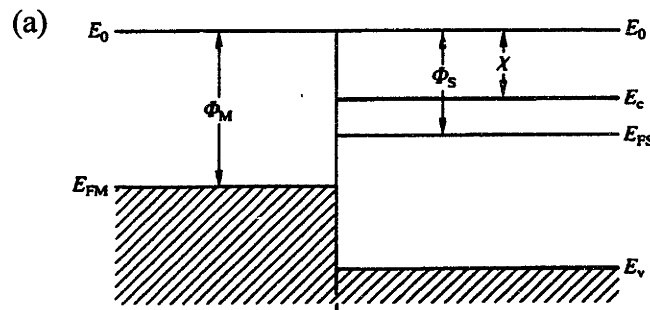
2.2 Zinc Oxide Semiconductor Junctions

Two types of zinc oxide semiconductor junctions are considered in this thesis. The first junction is the metal-semiconductor (Schottky) junction, where a high work function metal like palladium or gold is deposited onto an *n*-type single crystal semiconductor like zinc oxide or arsenic-doped silicon. The second type of junction is the grain-grain homojunction found in polycrystalline materials. The varistor effect is a consequence of the significant band bending that occurs at a doped grain boundary in zinc oxide. Both types of junctions are taken advantage of in order to study electrically active defects in zinc oxide. The principles of these two junction types are presented below, and their application to measuring electrically active defects is explained in Chapter 3.

2.2.1 The Metal-Semiconductor (Schottky) Junction

What follows is a discussion of the fundamentals concerning metal-semiconductor contacts, where the semiconductor is assumed to be defect-free and *n*-type, since zinc oxide is known to be *n*-type. The inclusion of defect levels will be covered in Chapter 3. For those who are familiar with *pn*-junctions, the Schottky junction can be viewed as a limiting case, resembling a p^+n-junction, where the p^+ side emulates a metal. The energy band diagrams for the metal and *n*-type semiconductor are shown in Figure 2.2.

(a)



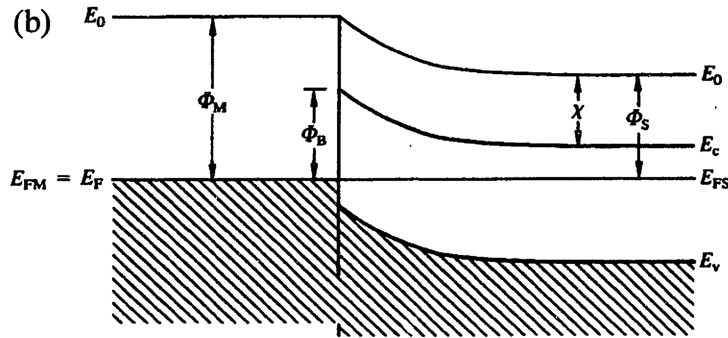


Figure 2.2 Energy band diagrams for metal-semiconductor contact (a) before charge transfer (non-equilibrium) and (b) after charge transfer (equilibrium).

E_0 is the vacuum energy level, a reference point to indicate the amount of energy needed to remove an electron from the metal without any leftover kinetic energy. The difference between the vacuum energy level and the metal's Fermi level is called the work function Φ_M. A similar work function quantity exists for the semiconductor, Φ_S. The electron affinity χ of a semiconductor is defined as $E_0 - E_C$.

The work function Φ_M of a metal and the electron affinity χ of a semiconductor are fundamental materials properties and do not change when constructing a junction. Furthermore, the Fermi level is constant when thermal equilibrium is achieved. (Here, the widely used misnomer of "Fermi level" is somewhat confusing because it is actually the chemical potential. Because it is an accepted misnomer, it will be used throughout this thesis.)3 This property of the Fermi level is a result of its thermodynamic properties. When a metal and semiconductor are brought together as in Figure 2.2a, the higher position of the Fermi level in the semiconductor indicates an excess charge amount relative to the metal. To establish the equilibrium of Figure 2.2b, electrons from the semiconductor must be depleted from the interface and transferred to the metal. Moreover, the fundamental properties Φ_M and χ cannot change. Thus, this charge transfer in the name of thermal equilibrium causes band bending in the semiconductor, whereby electrons in the metal see a potential barrier Φ_B and electrons in the semiconductor see a potential barrier Φ_B-E_C (=Φ_M-Φ_S), where E_C is the conduction band energy far from the junction.

The band bending at the metal-semiconductor interface indicates a depletion of electrons in the *n*-type semiconductor. This depletion of charge results in a depletion ca-

pacitance that will figure importantly in later discussions of measuring defect levels in the semiconductor. To evaluate the length of the depletion region, one usually assumes the "depletion approximation," whereby the depletion region is assumed to end after a finite distance W [cm] into the semiconductor and the semiconductor free carrier concentration is given by N_D [cm^{-3}]. Using Poisson's Equation and the definition of the potential V [Volts],

$$\nabla^2 V = -\frac{\rho}{\varepsilon_S \varepsilon_0} \quad and \quad E = -\nabla V, \tag{2.1}$$

where ρ [C/cm^{-3}] is the charge density, ε_S is the semiconductor's relative dielectric constant, and E [V/cm] is the electric field, one integrates from the interface over the depletion width (i.e. from x=[0,W]) to attain

$$E(x) = -\frac{eN_D}{\varepsilon_S \varepsilon_0}(W - x) \text{ for } x \in [0, W]. \tag{2.2}$$

Arbitrarily choosing the metal to be at "zero potential" and integrating the electric field to obtain the potential as a function of distance

$$V(x) = V_{bi} - \frac{eN_D}{2\varepsilon_S \varepsilon_0}(W - x)^2 \text{ for } x \in [0, W], \tag{2.3}$$

where the built-in potential $V_{bi}=eN_D W^2/2\varepsilon_s\varepsilon_0$ [V]. Using the expression for V_{bi}, the depletion width W [cm] is given by

$$W = \sqrt{\frac{2V_{bi}\varepsilon_S \varepsilon_0}{eN_D}} . \tag{2.4}$$

For conditions under applied bias V_A, the barrier height related to V_{bi} is changed to V_{bi}-V_A. Hence, during conditions of reverse bias (i.e. $V_A < 0$), the bands in the semiconductor are shifted downward, increasing the barrier height accordingly, and the expression for the depletion width becomes

$$W = \sqrt{\frac{2\varepsilon_S \varepsilon_0}{eN_D}(V_{bi} - V_A)} . \tag{2.5}$$

2.2.2 The Double Schottky Barrier Model for Grain Boundaries

To understand the behavior of electrically active grain boundaries, the double Schottky barrier model (DSB) has found widespread acceptance as an archetype for the electronic potential near these interfaces. The DSB is essentially two back-to-back

Schottky barriers. Figure 2.3 shows a schematic energy diagram of an electrically active interface. The potential barrier forms because electrons are trapped by the interface states. This trapping negatively charges the grain boundaries, inducing a local depletion of electrons in the adjacent grains and thereby effectively increasing the resistance of the grain boundary region. Greuter [4] has recently reviewed the key aspects of this model.

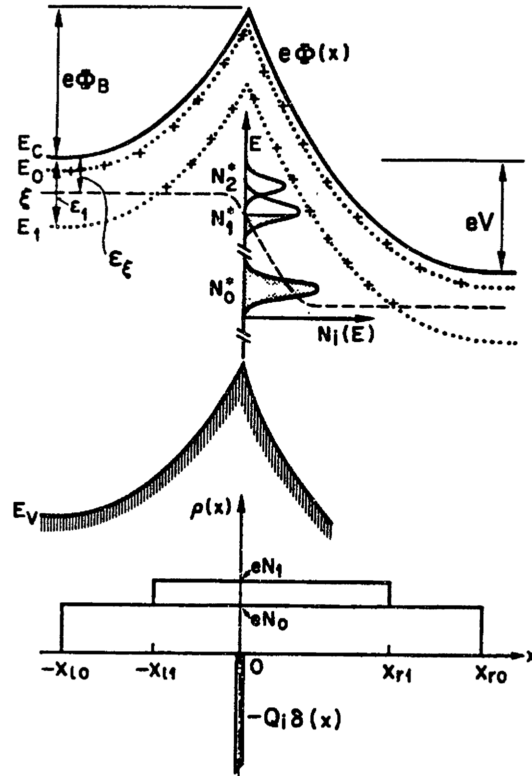


Figure 2.3 Energy band diagram and charge distribution for a double Schottky barrier at an activated grain boundary. $N_i(E)$ is the trap concentration at the interface. Typical zinc oxide varistors feature a zero-bias Φ_B=1 eV, a donor level E_0=50 meV with concentration $N_0=10^{18}$ cm^{-3}, an interface state concentration $N_i^*=10^{12}$-10^{13} cm^{-2} (i=0, 1, 2) and $V_B \leq$ 3.3-3.7 V. (see Ref. 4)

Many researchers have used the DSB model to describe quantitatively the transport of electrons across the barrier. For example, Pike and Seager [5] derived an expression for the thermionic emission current density in the prebreakdown regime:

$$J = A^* T^2 \exp(-\tfrac{\xi+\Phi_B}{kT})\left[1-\exp(-\tfrac{eV}{kT})\right], \tag{2.6}$$

where ξ ($=E_C$-E_F) is the bulk position of the Fermi level with respect to the conduction band, A^* is the effective Richardson constant, V is the applied bias, and Φ_B is the grain boundary potential barrier height. This is analogous to the expression for the thermally

activated current density in metal-semiconductor barriers. Electrical breakdown in regime II occurs when the potential barrier collapses, allowing a huge increase in the current flow from regime I, and Equation 2.6 no longer applies. The mechanism of electrical breakdown is postulated as barrier height (Φ_B) lowering and/or formation of a significant tunnel current due to a strong applied bias [5, 6, 7]. Furthermore, impact ionization has been accepted as a critical mechanism by which the barrier collapses due to an influx of holes at the boundary, as shown in Figure 2.4 [8].

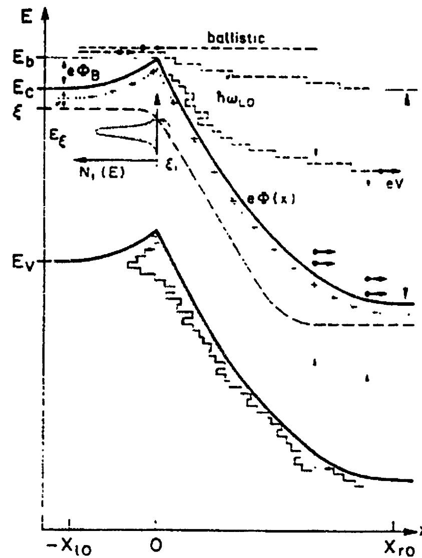


Figure 2.4 Energy band diagram for a DSB under large applied bias, showing holes being collected at the interface, causing the barrier to collapse. [see Ref. 8]

High energy electrons accelerated across the boundary by the large applied bias impact ionize atoms on the other side. Holes from the electron-hole pairs generated from the impact ionization drift and/or diffuse back toward the interface. A hole recombination process is computed to give a stable breakdown and high α values that do not diverge. In essence, the generated holes travel to the interface and depopulate the interface traps which, in turn, cause the barrier to collapse.

2.3 Deep Levels at the Grain Boundaries

Deep level transient spectroscopy (DLTS) has been utilized to study bulk or thin film semiconductors. To an extent, it has also been applied to polycrystalline semiconductors. Defect levels in silicon [9, 10, 11, 12, 13], germanium [14], and gallium arsenide

[15, 16] have been identified in their polycrystalline or bicrystal forms with DLTS. Similar defects at grain boundaries in zinc oxide have been measured. In fact, because zinc oxide varistors can exhibit very large capacitances, DLTS is a natural technique that can be used in attaining grain boundary defect information. (see also Chapter 3)

2.3.1 Previous Studies Using DLTS on ZnO Grain Boundaries

Shohata *et al.* [17] were one of the first to explore DLTS as means for characterizing zinc oxide varistors. They identified two defect levels, E1 (0.24 eV) and E2 (0.33 eV). They also noticed that the E1 signal saturated for large (presumably reverse) applied biases, which means that the E1 trap localized near the grain boundary depletion region. Rohatgi *et al.* [18] examined the defect levels they found in light of the heat treatments they performed on their samples. A figure showing DLTS signal versus temperature for samples with different annealing temperatures is shown in Figure 2.5.

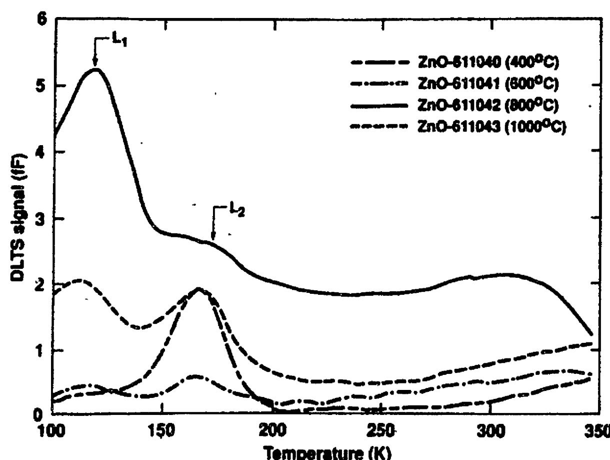


Figure 2.5 DLTS signal versus temperature for samples with different annealing temperatures [Ref. 18]

They made some correlations between the relative heights of the L1 and L2 defect levels (as depicted) and varistor stability. This work is noteworthy for its attempts directly measuring and comparing defect information between samples in order to ascribe a DLTS peak with a specific defect. In this case, the authors ascribe the L2 peak with the zinc interstitial. Gambino *et al.* [19] did DLTS experiments on "simplified" varistors, doped only with bismuth and cobalt. They reported only one energy level between 0.6 and 0.7 eV and ascribed it to interface states caused by large segregated ions. As will be pre-

sented in Chapter 6, our results for a similar system show two more defect levels. Simpson and Cordaro [20] have researched the defect levels in barium-doped zinc oxide. In their study, they also investigated effects that cooling rate might have on the defect densities. Other studies have investigated defect energy levels and various other aspects of the zinc oxide varistor effect such as electrical degradation [21] and doping [22]. A selected list of energy levels identified throughout the literature is presented in Table 2.1.

Table 2.1 Summary of majority carrier traps in ZnO measured by various researchers on a variety of samples.

Energy (eV)	Capture Cross-Section (cm^2)	Reference
0.3	2.6×10^{-14}	20
0.17 0.26	2.6×10^{-17} 7.6×10^{-17}	18
0.32 0.19 0.17	2×10^{-14} 4×10^{-16} 3×10^{-12}	23
0.09 0.16	- -	21
0.18 0.28	8×10^{-18} 1.3×10^{-17}	25

Researchers are interested in finding the important defect levels so that they can ascribe them to a particular chemical specie. In doing so, one is able to understand barrier formation and breakdown behavior (i.e. nonlinearity, α value) of varistors better in terms of doping and heat treatment. Distinguishing between bulk and interface traps seems like a logical prerequisite in order to begin to clarify the origins of the energy levels that have been measured to date. Winston and Cordaro [24], as well as Tsuda and Mukae [25, 26], tried to distinguish between bulk and interface states in their studies. In fact, "reverting" back to single crystal zinc oxide to understand its bulk state behavior seems like a logical course of action; Simpson and Cordaro [27]found a single 0.3 eV trap in a hydrothermally grown, single crystal. Though they conjectured a connection with an oxygen vacancy defect, they did not investigate doping or heat treatment effects, nor they did not use a saturating filling pulse to ensure that all traps were being filled. Experiments that follow up on the findings of Simpson and Cordaro are the main thrust of this thesis.

2.4 Grain Boundary Simplification: Geometry and Chemistry

In an effort to understand better the electronic structure of these doped interfaces and the double Schottky barrier, researchers have sought to isolate electrically active grain boundaries through various techniques. Olsson and Dunlop [28] used microcontacts to characterize individual grain junctions in sintered zinc oxide. Although they identified many different types of grain-grain junctions, their method is not ideal for studying electronic structure because of the complexities of the three-dimensional current network inherent in a polycrystalline matrix. Electrically active secondary phases and uncertain dopant concentrations further add to difficulties in studying specific grain boundaries. To lower the dimensionality of the problem, Schwing and Hoffmann [29] deposited an additive layer between two ZnO single crystals and annealed this construction at high temperatures (see Figure 2.6).

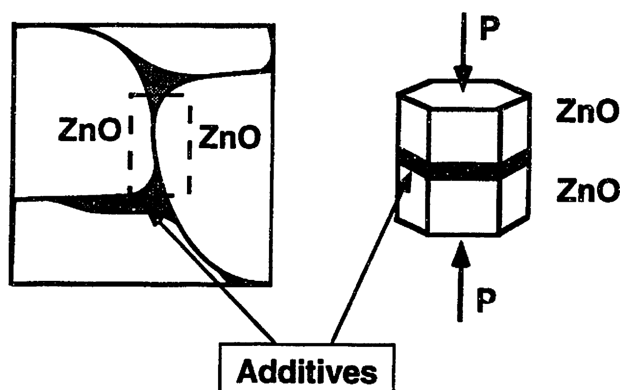


Figure 2.6 left: schematic grain-grain interface in a zinc oxide varistor; right: idealization of this grain-grain varistor interface between two single crystals of ZnO

By the very nature of the sample, current is confined to pass through a well-defined two-dimensional plane. Although this method successfully demonstrated I-V nonlinearity, the nonlinearity was caused by an artificial double heterojunction that forms between the ZnO crystals and the additive oxide (~microns thick) between them. Electron microscopy of typical varistor grain boundaries show that no micron-thick foreign oxide layer is normally present.

The movement toward better controlled interfaces has lead Yano *et al.* [30, 31] to fabricate thin film "sandwiches." Similar to the case of Schwing and Hoffmann, Yano

and co-workers constructed a double heterostructure which demonstrated a symmetrical I-V nonlinearity. Because they used sputtering to deposit poly-ZnO and $PrCoO_x$ films, they did not need high temperature anneals to hold their structures together, and no in-diffusion was done. As mentioned previously, this double heterostructure is not representative of varistor boundaries.

Sukkar [32, 33] and Baek [34, 35] developed surface in-diffusion (SID) "sandwich" structures with poly-ZnO ceramics along the same lines. In appearance, these samples look very similar to those of Schwing and Hoffmann. Again, the current is isolated to pass through an electrically activated two-dimensional plane. In this case, however, the additive layer diffuses down the poly-ZnO grain boundaries into the bulk, leaving a thin area in the middle of the sandwich activated. Here, the heterojunction problem is somewhat alleviated because the additive layer actually diffuses into the bulk crystals. For these specimens, the high temperature sintering that was required to construct the sandwiches often changed the ZnO microstructure. Furthermore, the dopants which were introduced in pairs (e.g. Pr and Co) diffused at different rates, causing possible non-uniformity in the activated layer. This nonuniformity in coverage leads to characterization difficulties because the barrier height is lower in some spots.

Aside from a movement toward increased geometrical control, recent work by Lee and Chiang [36] has succeeded in controlling and quantifying the grain boundary chemistry in hot-pressed bulk BiCo-doped zinc oxide. In terms of the composition, these samples most resemble those of Gambino *et al.* [19]. By careful microanalysis and heat treatment, they have developed a method of controlling bismuth monolayer coverage along grain interfaces. As part of our collaboration with them, we have made correlations between the processing of these materials and their dc leakage currents and α values.

Despite the foundations that have been laid to describe the process of electrical breakdown at grain boundaries and the efforts to apply this description to simplified grain boundary structures, a direct correlation between the chemistry of the boundary and its resultant electrical behavior has not been made. Greuter [4] has stated "The dominant parameters determining the potential barrier, Φ_B, and its dependence, $\Phi_B(V)$, on applied bias are: (i) the doping, N_0, N_t, of the ZnO grains, (ii) the total interface charge, Q_i, and (iii)

the actual distribution, $N_i(E)$, of the interface density of states." (see Figure 2.3) In other words, what kinds of dopants and subsequent processing steps need to be performed to achieve the proper values for N_0, N_t, Q_i, and N_i such that $\Phi_B(V)$ can be predicted with some degree of certainty? As depicted in Figure 2.7, the connection between the chemistry/processing of varistors and their electrical properties is unclear.

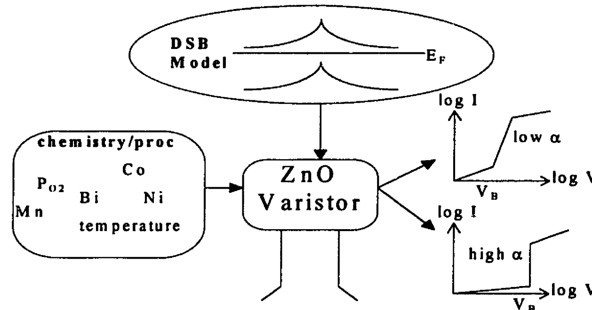


Figure 2.7 Chemistry and processing need to be linked to the electrical properties. Understanding the intrinsic and extrinsic defect characteristics in terms of the DSB model is an important link.

A comprehensive understanding begins with knowledge of the intrinsic and extrinsic defect characteristics in ZnO. That is, knowing the energy level(s) of certain defects and understanding how they behave under various processing conditions allows one to apply directly the DSB model in order to understand the resultant electrical characteristics. Single crystal films of ZnO were grown in order to focus on understanding intrinsic and extrinsic defects. Moreover, the technique of growing single crystal films was conceived such that it could be extended to bicrystal growth in future studies.

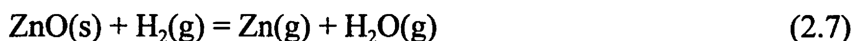
2.5 Vapor Phase Growth of Zinc Oxide

Growth of zinc oxide from zinc vapor has been done since the late 1960's for its optical and piezoelectric properties. Initially, the interest was focused on the ability to grow high quality, free-standing single crystals. Gradually, interest shifted toward growing single crystal zinc oxide on suitable substrates to explore potential integrated circuit and waveguide applications. More recently, as mentioned in the previous section, zinc oxide films have been explored for electrically active grain boundary studies by Yano *et al.* [30, 31]. As applied to our work, single crystal zinc oxide was grown on *r*-plane sapphire so that we could use Schottky barriers and DLTS to investigate the nature of intrin-

sic and extrinsic defects. This section reviews some thermodynamic considerations when growing zinc oxide in an open tube system. Additionally, some previous work on ZnO growth is reviewed.

2.5.1 Thermodynamics of Vapor Transport

In many of the studies encountered in the literature, growth of zinc oxide films focused on reducing zinc oxide powder with hydrogen gas to zinc vapor and water, subsequently transporting it over a negative temperature gradient to a cooler substrate, and then reoxidizing the vapor back to ZnO. Zinc is known to have a high vapor pressure, melting at a relatively low 420°C. Because of zinc's rather high vapor pressure, zinc oxide can be easily transported if it can first be reduced to zinc. The oxidation/reduction behavior of zinc and zinc oxide is summarized in the Ellingham diagram (or Richardson/Jeffes) [37]. The two reactions of interest are



$$ZnO(s) + H_2(g) = Zn(g) + H_2O(g) \quad (2.7)$$

$$2Zn(g) + O_2(g) = 2ZnO(s) \quad (2.8)$$

The first equation, reaction 1, is represented on the Ellingham diagram by the zinc line and the H_2/H_20 ratio data. The second equation, reaction 2, would be represented on the Ellingham diagram as just the zinc line if the zinc were in the solid phase.

Comparing the free energies of these reactions in Figure 2.8, one readily sees that the reaction in Equation 2.8 is much more favorable.

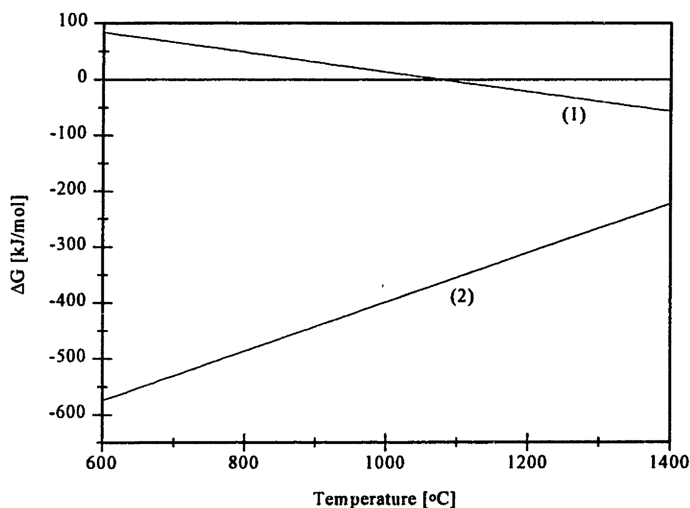


Figure 2.8 ΔG versus temperature for reaction (1) $ZnO(s) + H_2(g) = Zn(g) + H_20(g)$ and reaction (2) $2Zn(g) + O_2(g) = 2ZnO(s)$ (see Ref. 40)

The fact that oxygen is a potent oxidizer is a key consideration when designing a vapor transport system for zinc oxide. Moreover, one may incorrectly guess from Figure 2.8 that temperatures greater than T≈1078°C are necessary to reduce zinc oxide with hydrogen (i.e. to drive reaction 1 rightward). Though reaction 1 appears thermodynamically favorable only above T≈1078°C, one must inspect the equilibrium constant K_1 to determine whether this reaction proceeds leftward or rightward.

$$K_1 = \frac{P_{Zn} P_{H_2O}}{P_{H_2}} \quad (2.9)$$

The Ellingham diagram takes account of the equilibrium constant by including the H_2/H_20 ratio axis, and one sees that zinc oxide can be reduced for sufficiently high H_2/H_20 ratios at temperatures below 1078°C. For example, to reduce zinc oxide at 900°C, one needs an H_2/H_20 ratio greater than 100:1.

2.5.2 Literature Review of Vapor Phase Growth of Zinc Oxide

As stated earlier, zinc oxide's properties as a wide bandgap semiconductor and piezoelectric substance have generated interest in its bulk growth. One of the first to report vapor phase growth of zinc oxide was Scharowsky [38]. Small zinc oxide needles ~0.3 mm in diameter were reported to have grown on the furnace walls, when zinc metal vapor from a metal source at 600°C was carried by a nitrogen and hydrogen gas mixture into a furnace at 1150°C. Nielsen [39] performed a similar experiment but used sintered zinc oxide as the source. Nitrogen and hydrogen were fed into a source tube which contained the ZnO pellets. This end of the tube exited into a zinc oxide cone lining inside the furnace at ~1300°C; oxygen was fed separately into the furnace (see Figure 2.9a). Nielsen notes that the ZnO lining inside the furnace was advantageous to growing large, pure specimens.

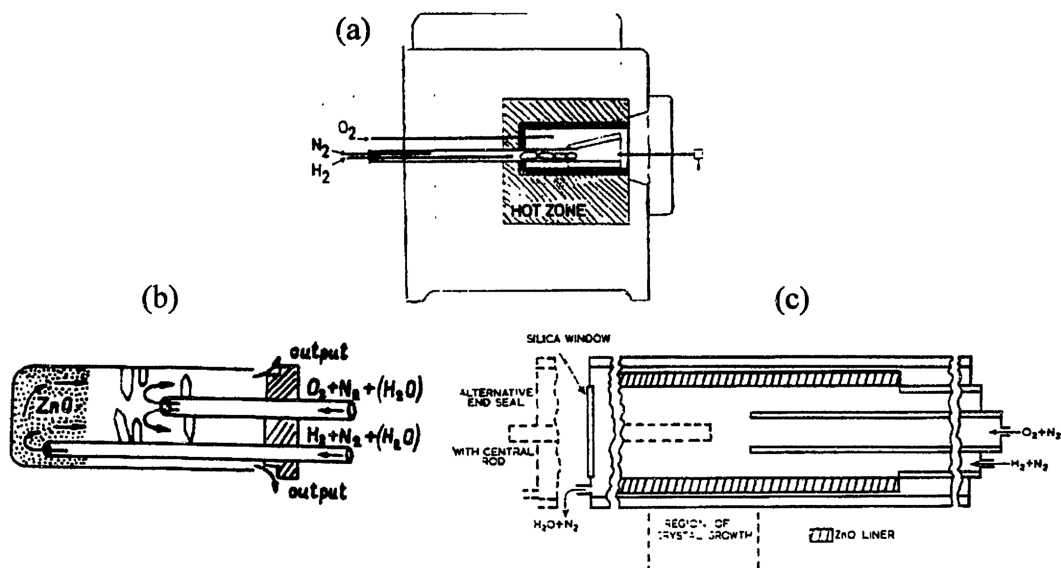


Figure 2.9 Schematic furnace setup used by (a) Nielsen [39], (b) Pas'ko *et al.* [41], and (c) Dodson and Savage [40].

Nielsen also modified the setup to dope his as-grown crystals with copper. Dodson and Savage [40] along with Pas'ko *et al.* [41] used tube furnace setups that were conducive to the control and study of gas flow on crystal quality, as shown in Figure 2.9b and c. Both Dodson and Savage and Pas'ko *et al.* introduced hydrogen through one port and oxygen through another, with the expectation that the crystals would grow in the vicinity of the oxygen port. Furthermore, both use zinc oxide as a source, strategically placed in a manner that allows the hydrogen to have dominant flow over it, minimizing the source's interaction with the oxygen. Both groups featured temperatures in the 1200°C range. Pas'ko *et al.* even characterized the morphology of their specimens against flow rate of water vapor and hydrogen.

Not long after vapor growth of bulk zinc oxide was established, several investigators developed film growth techniques that borrowed many ideas from their bulk counterparts. Some early work on thin ZnO films was done by Channin *et al.* [42] for waveguide studies. Their process simply involved holding a $(1\bar{1}02)$ sapphire substrate (*r*-plane) over a heated zinc oxide powder source (~850°C) in flowing hydrogen. Films of $(11\bar{2}0)$ zinc oxide were produced, but no significant details concerning the growth process were given. Galli and Coker [43] used a chemically more complicated system which involved hydrogen and HCl. They deposited thick ZnO films on a number of sapphire

substrates which included the r-plane orientation. Though their films were of good crystalline quality, they found the film surfaces to be highly textured, sometimes with a 5 μm surface roughness.

Open tube systems were later studied so that gas delivery would be simplified. Reisman and Landstein [44] studied the thermodynamics of such systems, though they did not focus on ZnO growth on sapphire substrates. Kasuga and Ishihara [45] flowed nitrogen, hydrogen, and water through a tube system to grow (11$\underline{2}$0) ZnO on r-plane sapphire, as depicted in Figure 2.10a. They kept their source at 1000°C and their substrates between 650-800°C. Their growth rates were on the order of microns per minute.

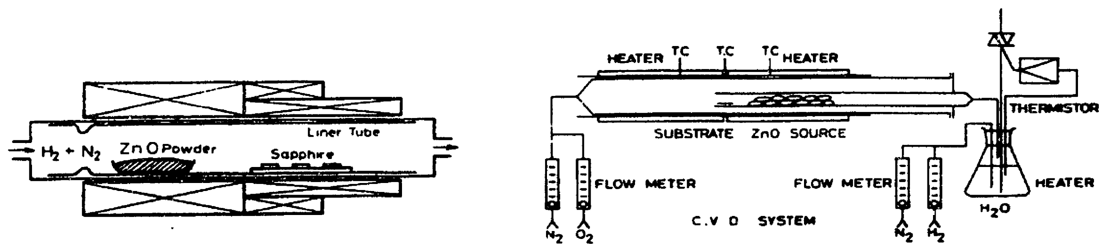


Figure 2.10 Schematic diagram of open tube system for ZnO growth on sapphire used by (a) Kasuga and Ishihara [45] and (b) Ohnishi *et al.* [46]

For the same film-substrate orientations, Ohnishi *et al.* [46] investigated the improvements that added water vapor and an intermediately sputtered ZnO layer had on the final films. Considerably more complicated than the system of Kasuga and Ishihara, the system of Ohnishi *et al.* bubbled hydrogen through water (~90°C) and added an oxygen gas inlet where the substrates were located, similar to the ideas found in bulk crystal growth. They did not observe film growth when oxygen was absent. They used a temperature of 900°C for both source and substrate. Hydrogen and oxygen were flowed at ~40 sccms, and nitrogen (carrier gas) was flowed at a considerably faster rate of ~300 sccms. Most significantly, Ohnishi *et al.* found that a thin (~13 nm) intermediately sputtered zinc oxide film improved the smoothness of the films. Apparently, the amorphous sputtered layer suppresses island formation which leads to uneven polycrystalline growth. Though the pre-sputtered film was amorphous, the subsequent film grown by CVD afterwards was found to be of high crystalline quality. Their film thicknesses ranged from 0.4 to 100 μm. They later compared their results with other chemical systems, namely ZnO-Br_2-O_2 and $ZnCl_2$-O_2 [47], and also tested their films as optical waveguides. [48]

The reactors of Kasuga and Ishihara as well as Ohnishi *et al.* were used as examples when we designed our own system for zinc oxide film growth. Substrate preparation with a thin, pre-sputtered ZnO layer was considered seriously, as the literature clearly indicates that higher quality, smoother films under well-controlled growth conditions are produced with this added step. Water was also considered an essential ingredient to slow the growth rate down. Because adatoms need enough time to find single crystal atomic positions to achieve smooth films of high crystallinity, slow growth rates and high temperatures were chosen to enhance surface mobility. Chapter 5 reviews the specific parameters used in our experiments.

3. DLTS Measurement Technique

Introduced in 1974 by Lang [49], deep level transient spectroscopy (DLTS) has rapidly become a standard evaluation tool for semiconductors. By using the depletion capacitance of a *pn*-junction or Schottky barrier (e.g. metal on *n*-type zinc oxide) to monitor the filling and emission of traps located within the depletion region, one is able to observe a corresponding capacitance transient that is related to the emission of holes into the valence band or electrons into the conduction band. This transient contains fundamental information about the nature of the trap such as (1) its energy level E_T [eV], (2) its capture cross-section σ_T [cm^2], and (3) its concentration N_T [cm^{-3}]. The heart of DLTS lies in analyzing a particular trap's capacitance transient as it changes over a temperature scan. Using the principle of detailed balance and some electronics that are set to give a maximum DLTS signal at a predetermined time constant τ_{max}, a spectrum is produced with peaks that each identify a trap level. DLTS is sensitive to concentrations as low as 10^9 cm^{-3}, where the detection limit is about 10^{-5} times the bulk free carrier concentration.

Many ways of applying DLTS have been developed, and hence, proper analysis and interpretation of DLTS data requires specific understanding of a particular DLTS system. In this chapter, the basic physics of DLTS is reviewed for Schottky barrier and grain boundary (double Schottky barrier) junctions. A description of the two different DLTS methods used in this thesis are presented thereafter. Benton [50] has written an excellent summary of DLTS and has included some demonstrative applications. A thorough review is given by Miller *et al.* [51].

3.1 Review of Fundamental Theory behind DLTS

Because zinc oxide is naturally an *n*-type semiconductor and has not been known to exhibit *p*-type conductivity, discussion of metal/semiconductor junctions will be limited to *n*-type semiconductors. The fundamentals of junction device physics are covered extensively in standard text books [52, 53]. The discussion below is a review of the key concepts relevant to DLTS.

When a metal is brought into intimate contact with a perfect semiconductor surface, the semiconductor undergoes a free charge transfer to the metal such that the Fermi levels in the metal and semiconductor are equal. (see also Section 2.2.1) Due to the absence of majority carrier electrons in the semiconductor, the region adjacent to the metal contact contains a net charge density, and the valence and conduction bands bend upwards as shown in Figure 3.1. A typical approximation is to assume that this space charge in the semiconductor extends a finite distance W (given by $\sqrt{\frac{2\varepsilon_S(V_{bi}-V_A)}{eN_D}}$) beyond which no space charge exists; this is called the depletion approximation. (W is computed through some elementary electrostatics; the terms are described below.)

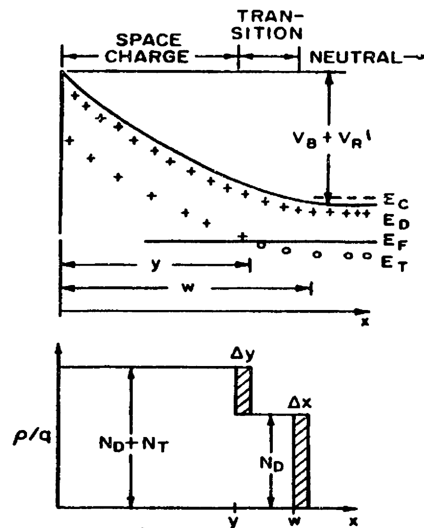


Figure 3.1 Schematic diagram of depletion region at metal and *n*-type semiconductor interface. A depletion region has formed near the metal/semiconductor interface because a charge transfer from the semiconductor has occurred to achieve equilibrium. Here V_B is the built-in voltage and V_R is the applied reverse bias. A single majority carrier trap of concentration N_T is depicted with energy E_T.

As can be seen in Figure 3.1, the donor-like trap level crosses the Fermi level near the depletion region edge. Electron traps above the Fermi level E_F are empty and positively charged; those below are filled and neutral. One should note that the region of empty traps does not identically span the depletion width; it extends to about the point where the energy of the trap state crosses the Fermi level (y) which is a little before the depletion width edge.

3.1.1 Junction Capacitance

An expression for the capacitance of this junction can be computed for space charge regions without traps by using the depletion approximation. Analogous to a parallel plate capacitor with a separation distance given by the depletion width W,

$$C = \frac{\varepsilon_s A}{W} = A\sqrt{\frac{e\varepsilon_s N_D}{2(V_{bi} - V_A)}}, \tag{3.1}$$

where ε_s [F/cm] is the permittivity of the semiconductor ($=\varepsilon_r\varepsilon_0$), e [C] is the unit charge, V_{bi} [V] is the built-in (or flat-band) potential, V_A [V] is the applied voltage across the barrier (negative for a reverse bias), N_D [cm^{-3}] is the donor density, and A [cm^2] is the metal-semiconductor contact area. When considering the presence of traps, the previous equation becomes

$$C = \frac{\varepsilon_s A}{W} = A\sqrt{\frac{e\varepsilon_s (N_D + n_T)}{2(V_{bi} - V_A)}}, \tag{3.2}$$

where n_T [cm^{-3}] is the concentration of filled traps. Thus, filling of traps in the depletion region is detected by a capacitance change. As noted by Kimerling [54], one should remember that the effects of traps on junction capacitance can vary, depending on the frequency of the small signal capacitance; here, one is assuming that the frequency used to measure the small signal capacitance is much larger than the emission or capture rates of the trap. Equation 3.2 can be further rearranged into the Mott-Schottky relation

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_A)}{e\varepsilon_s A^2 (N_D + n_T)}, \tag{3.3}$$

such that $1/C^2$ depends linearly on the applied (reverse) voltage V_A. Typically, N_D is much greater than n_T, and thus, the slope of this plot is proportional to the free carrier concentration N_D.

3.1.2 The DLTS Transient Signal

In a DLTS experiment, the dynamic quantity is the number of traps actually filled with electrons, n_T(t). The rate equation governing the occupancy of electron traps depends on the thermal capture rate for electrons and holes c_n, c_p [s^{-1}] and their corresponding thermal emission rates e_n, e_p [s^{-1}] (neglecting the optical emission rate):

$$\frac{dn_T(t)}{dt} = (c_n + e_p)(N_T - n_T) - (c_p + e_n)n_T. \quad (3.4)$$

The solution of this differential equation for traps initially filled with electrons in the depletion layer $n_T(t=0)=N_T$ is

$$n_T(t) = N_T e^{-e_n t} = N_T e^{-t/\tau_n}, \quad (3.5)$$

where N_T [cm^{-3}] is the total number of electron traps, and τ_n [s] is the characteristic time constant at which the trap empties. Hence, by establishing an initial state where traps in the depletion region are all filled, the capacitance will behave with the time dependence

$$C(t) = A\sqrt{\frac{e\varepsilon_s(N_D + n_T)}{2(V_{bi} - V_A)}} = A\sqrt{\frac{e\varepsilon_s(N_D + N_T e^{-t/\tau_n})}{2(V_{bi} - V_A)}}. \quad (3.6)$$

Taking N_D to be much greater than N_T,

$$C(t) = A\sqrt{\frac{e\varepsilon_s N_D}{2(V_{bi} - V_A)}}\sqrt{1 + \frac{N_T}{N_D} e^{-t/\tau_n}} \approx A\sqrt{\frac{e\varepsilon_s N_D}{2(V_{bi} - V_A)}}(1 + \frac{N_T}{2N_D} e^{-t/\tau_n}). \quad (3.7)$$

By defining the baseline (quiescent reverse bias) capacitance C_∞ and the change in capacitance $\Delta C(t)$,

$$C_\infty \equiv A\sqrt{\frac{e\varepsilon_s N_D}{2(V_{bi} - V_A)}} \quad (3.8)$$

$$\Delta C(t) \equiv C_\infty - C(t), \quad (3.9)$$

equation 3.7 becomes

$$\frac{\Delta C(t)}{C_\infty} \equiv \frac{N_T}{2N_D} e^{-t/\tau_n}. \quad (3.10)$$

Hence, the change in capacitance $\Delta C(t)$ under reverse bias is exponentially dependent on the time as depicted in Figure 3.2, where the voltage pulse establishes the initial condition of filling all the traps in a given segment of the depletion width.

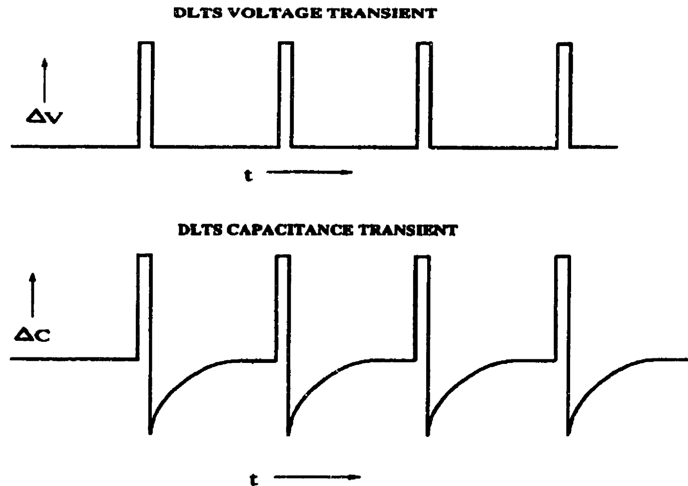


Figure 3.2 Typical time dependence curves for applied voltage and capacitance transient. The voltage pulse should saturate all the traps within a given segment of the depletion region. Here, the transient signal is negative.

3.1.3 The DLTS Rate Window

The time constant of the capacitance transient can be used to determine a trap's energy level E_T, its capture cross-section σ_T, and its concentration N_T. A donor-like trap in the bandgap emits electrons to the conduction band with an emission rate given by the principle of detailed balance:

$$e_n = 1/\tau_n = \frac{\sigma_n \langle v_{th} \rangle N_C}{g} \exp\left(-\frac{E_C - E_T}{k_B T}\right), \tag{3.10}$$

where σ_n [cm^2] is the capture cross-section for electrons of the defect state, v_{th} [cm/s] is the mean thermal velocity of electrons, N_C [cm^{-3}] is the effective density of states in the conduction band, g is the trap degeneracy, and E_C [eV] is the energy of the conduction band edge. Because the emission rate e_n ($=1/\tau_n$) is temperature dependent, so too is the capacitance transient by Equation 3.7. The temperature dependence of the transient is schematically illustrated in Figure 3.3. For low temperatures, carriers are not emitted for lack of thermal energy, and the transient is exceedingly slow. For high temperatures, carriers are emitted quickly, and the transient response is immediate.

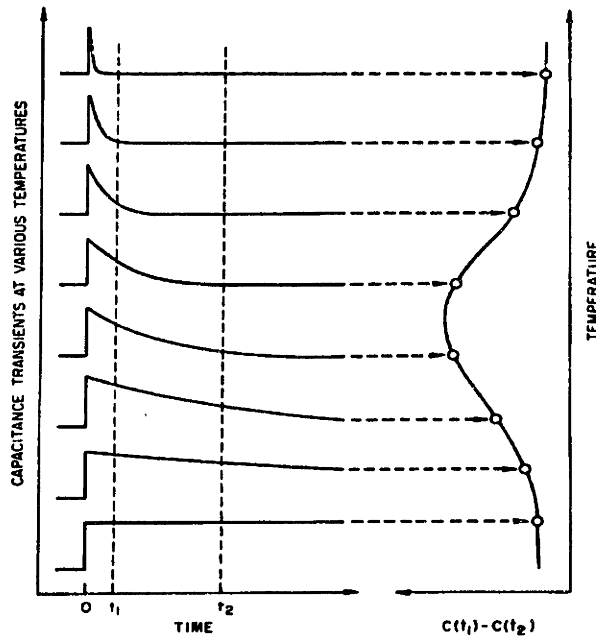


Figure 3.3 Schematic illustration of temperature dependence of positive capacitance transient. A box-car averager sampling window at times t_1 and t_2 are indicated, showing how the choice of these times can result in a spectroscopic peak in the change in capacitance $\Delta C(t)=C(t_1)-C(t_2)$.

The heart of DLTS lies in defining a "rate window" with electronics that will output a maximum DLTS signal ΔC for a specific transient time constant τ_{max}. In other words, during a temperature scan, the capacitance transient will traverse a myriad of time constants τ_n. At some peak temperature T_p at which $\tau_n=\tau_{max}$, the DLTS signal will max out. Changing τ_{max} causes the DLTS signal maximum to shift to other values of T_p. For a given defect, values of τ_n and T_p are tabulated for different settings of τ_{max} to generate an Arrhenius graph of $\ln(e_n/T_p^2)$ versus $1/T_p$, where the slope is proportional to the energy level E_T and the y-intercept is proportional to the capture cross-section σ_n. In the case of Figure 3.3, the rate window is set by sampling the capacitance signal at times t_1 and t_2 which defines a particular time constant τ_{max}. (t_1 and t_2 are measured from the pulse edge.) Changing the values of t_1 and t_2 redefines the value of τ_{max}. Mathematically speaking, τ_{max} for a given t_1 and t_2 can be computed by maximizing the expression for $\Delta C(t_1, t_2)=C(t_1)-C(t_2)$ (Equation 3.9) which can be done by taking its derivative with respect to τ_n and setting it equal to zero. (Note that we are assuming that $C_\infty \approx C(t_1)$.) The result is

$$\tau_{max} = 1/e_{max} = \frac{t_1 - t_2}{\ln(t_1 / t_2)}. \tag{3.11}$$

The concentration can be computed from the height of the DLTS peak ΔC. Assuming that all the traps are filled by the pulse and that $\Delta C \ll C_\infty$, one can use Equation 3.10 with t=0 to get

$$N_T \approx 2N_D \frac{\Delta C}{C_\infty}. \tag{3.12}$$

Here, the expression for N_T is given as an approximation because the filling pulse does not in practice cover the entire depletion width and the sampling window may not cover the entire transient.

3.2 Application of DLTS to Grain Boundary Junctions

Though originally conceived for use on asymmetric Schottky or *pn*-junctions, DLTS has found widespread use in characterizing energy levels at or near grain boundary junctions. DLTS can be used at electrically active grain boundaries, such as the one represented by the double Schottky barrier model, because there is a depletion capacitance associated with band bending. Furthermore, this band bending is bias-dependent so that one is able to populate and depopulate traps in a manner similar to that of a one-sided Schottky barrier. Grain boundaries generally have two kinds of traps: (i) bulk traps located in the adjacent grains and (ii) interface traps located at the grain boundary plane which are mainly responsible for the depletion regions. Because the discussion of the bulk states is identical to the one above for metal-semiconductor junctions, the discussion below will be limited to the application of DLTS to interface states.

3.2.1 Zero Quiescent Bias Case

When the double Schottky barrier is at zero-bias, the Fermi level is flat. Traps below the Fermi level are filled; traps above the Fermi level are empty, including the interface traps. Referring to Figure 2.3, biasing the grain boundary causes the depletion region on one side to enlarge, dropping the Fermi level on that side, raising it on the other. DLTS on Schottky junctions usually involves holding the junctions at a reverse bias, and

pulsing them to near-zero bias for majority carrier filling. Because one wishes to observe emission from interface traps, a different pulsing arrangement is required. In the grain boundary case, referring to Figure 3.4a, if the bias is constantly held at the quiescent bias of zero, the equilibrium occupancy of the interface states is simply determined by the position of the Fermi level E_F.

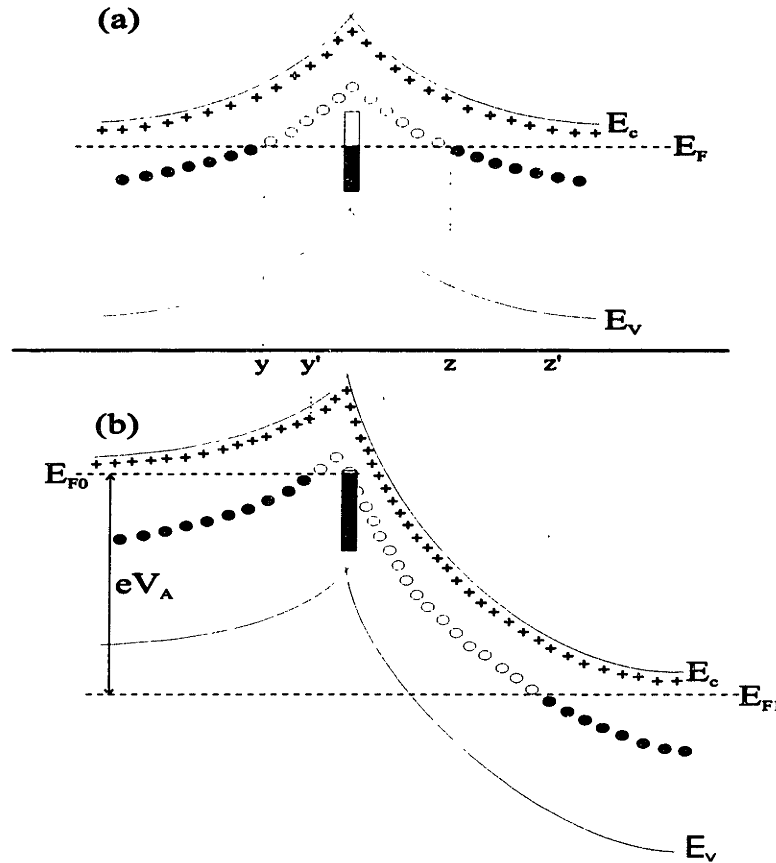


Figure 3.4 (a) Band diagram at zero bias. Interface states up to E_F are filled. (b) Band diagram during filling pulse at bias V_A. Interface states up to E_{F0} are filled, which is somewhat higher than E_F.

During the pulse depicted in Figure 3.4b, the bias is increased to $V_A(>0)$, and the quasi-Fermi levels move in accordance to this new bias. Here, the interface states have a new equilibrium occupancy at E_{F0} which is higher than the quiescent E_F. Thus, during the pulse, the interface states between E_F and E_{F0} are filled. When the pulse ends and the bias returns to zero, carriers in the filled traps above E_F will be emitted to the conduction band, as illustrated in Figure 3.5. Thus, by changing the bias settings to move the Fermi level, one can sweep through a distribution of interface states. In analogy to Equation 3.2,

the filling and unfilling of these interface traps can be monitored by the capacitance change of the grain boundary.

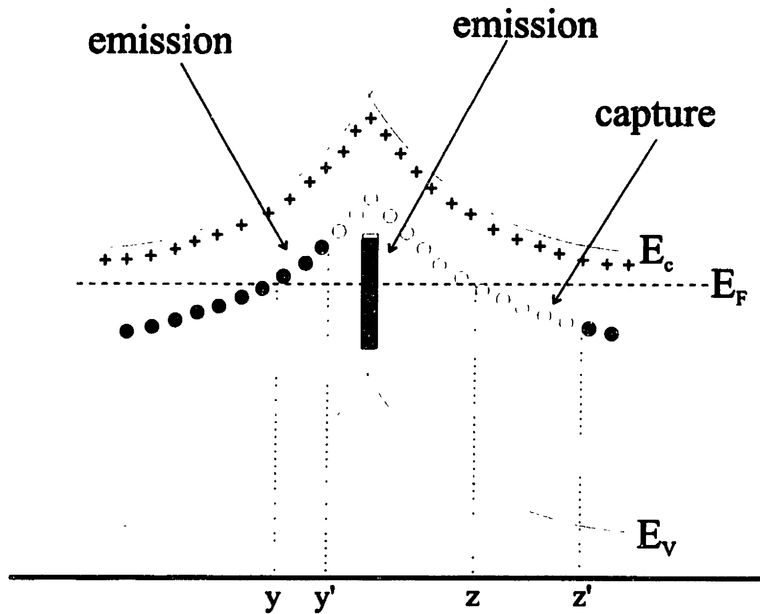


Figure 3.5 Interface states after injection pulse are filled above the Fermi level. Carriers in these traps will be emitted to the conduction band.

A word of caution must be included when interpreting the DLTS signal from grain boundary capacitances. An implicit assumption that bulks states on one side of the interface are identical to those on the other side has been made. As shown in Figure 3.5, the DLTS signal originates from potentially three different sources: (1) a capture signal from the filling of bulk traps on the negatively biased side of the grain boundary, (2) an emission signal from bulk traps on the positively biased side, and (3) the emission signal from the interface traps. Assuming the capture rate (which depends on the cross-section of the traps) to be fast compared to the emission rate (which depends mostly on the temperature), one still needs to discern between bulk and interface states. The next section discusses how a negative quiescent bias remedies this difficulty.

3.2.2 Negative Quiescent Bias Case

The negative quiescent bias case simply involves pulling the dc offset of the pulse generator down so that the situation in Figure 3.4 is reversed. The junction is held as shown in Figure 3.4b at a bias V_A(<0) and pulsed to zero bias as shown in Figure 3.4a. (More accurately, the mirror image of Figure 3.4b is the result of a negative bias V_A, but

since the junction is symmetric, Figure 3.4b can still be used.) When the bias returns to its quiescent value of V_A, the occupancy of the traps are as shown in Figure 3.6.

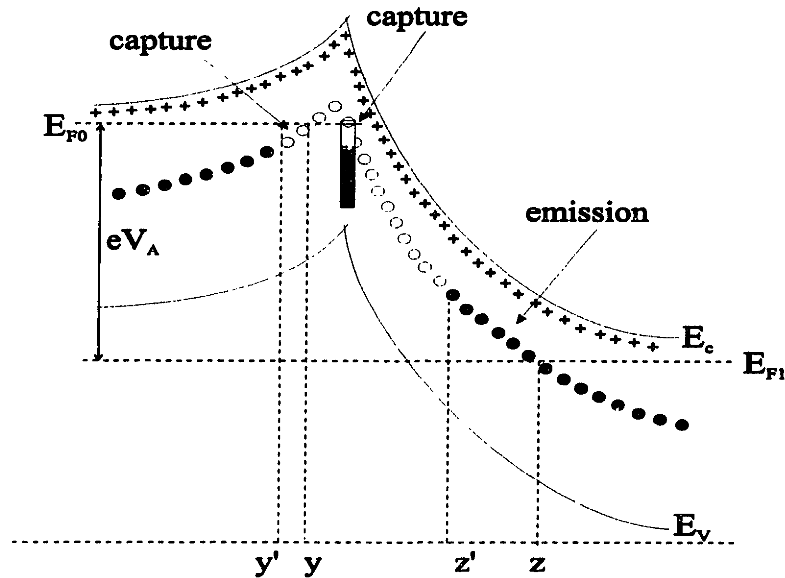


Figure 3.6 Carriers are emitted from bulk traps only when the bias returns to the quiescent value of $V_A(<0)$.

Again, if one can assume that the capture rate can be neglected, one observes emission from bulk traps only on the negatively biased side of the grain boundary. Thus, peaks which show up on zero quiescent bias scans but do not show up on negative quiescent bias scans can, in general, be ascribed to interface states. Peaks which show up on both scans can be ascribed to bulk states. Traps below the zero bias Fermi level cannot be seen with this method.

3.3 A-B Technique: Simulated Box-Car Method with Lock-in Amplifier

The heart of DLTS lies in the definition of the rate window. Part of the work presented in this thesis was originally performed using a two-phase lock-in amplifier to implement the rate window (hereafter denoted as "A-B technique"). A diagram of the DLTS setup is shown in Figure 3.7. The A-B signal ($\propto \Delta C$) sent from the lock-in amplifier to the computer is attained by subtracting the voltage readings from the in-phase and quadrature channels; this is further explained in Section 3.3.1.

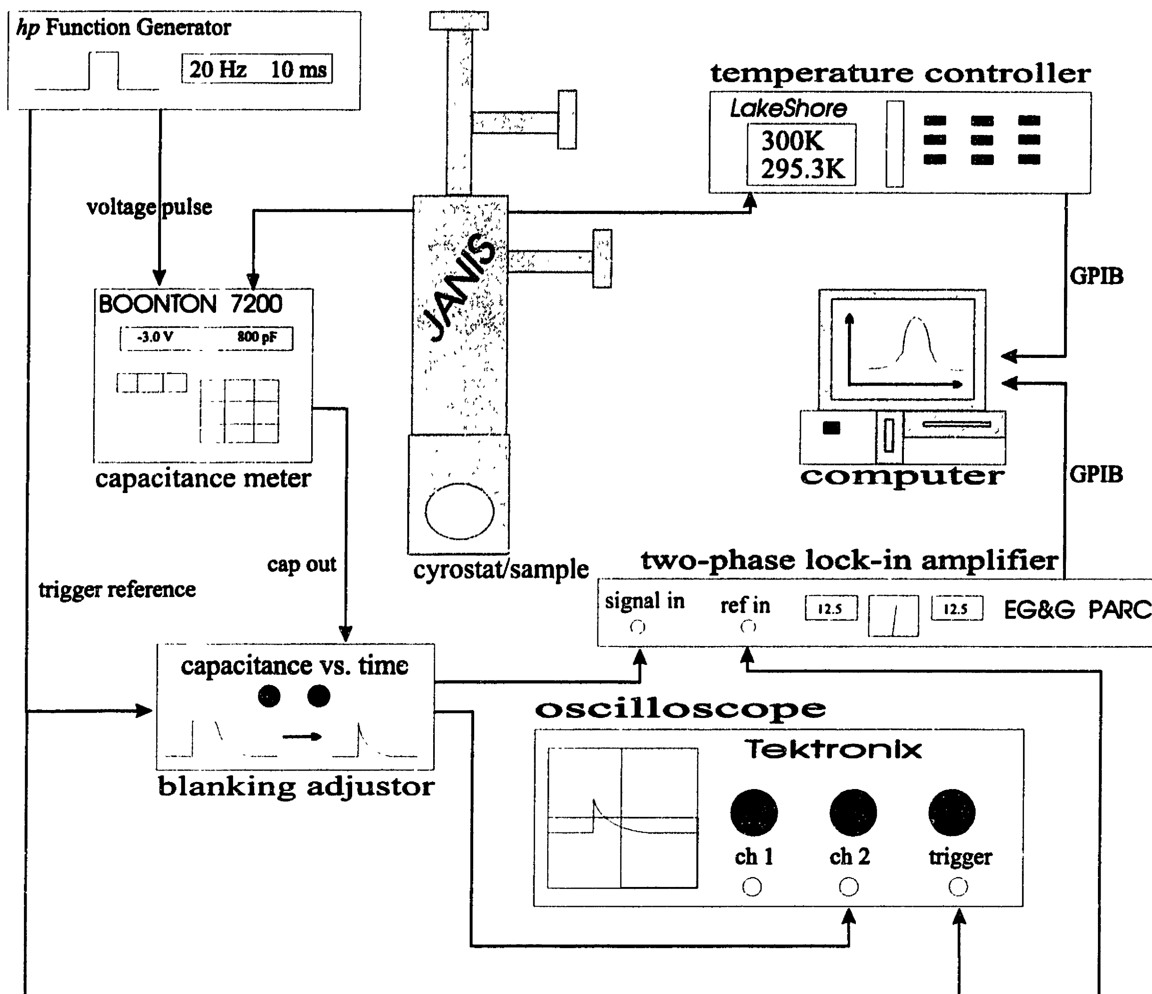


Figure 3.7 Pictorial block diagram of the DLTS system employing a lock-in amplifier. Note directions of arrows which represent flow of electronic signals.

Though simple to analyze and easy to understand in terms of box-car averaging, the sensitivity in A-B technique is heavily frequency dependent and cannot accommodate pulse width changes for a fixed rate window. Pons *et al.* [55] and Broniatowski [13] have applied this technique to study bulk and grain boundary deep levels in semiconductors. Baek [34] has also used this technique specifically to characterize deep levels at activated zinc oxide grain boundaries.

3.3.1 In-phase and Quadrature Channels of the Lock-in Amplifier

By taking the difference in the signals from the in-phase A and quadrature (lagging by $\frac{1}{2}\pi$) B channels of a lock-in amplifier, one is able to simulate the sampling of a double box-car averager as shown in Figure 3.8. The lock-in amplifier output is the in-

tegral of the product of the square-wave weighting function (A or B) and the fundamental Fourier component of the signal S over the period T. By subtracting the outputs of the in-phase and quadrature phase detectors, one can instead think of this output as the integral of the product of the square-wave weighting function A-B and the signal S.

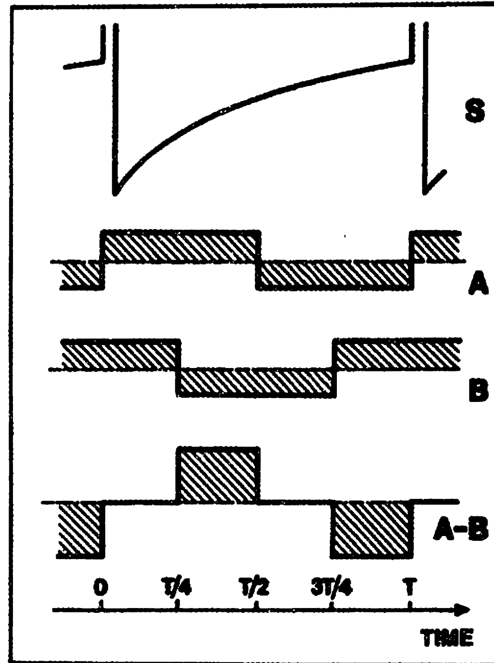


Figure 3.8 A-B technique: signal S is convolved with in-phase weighting function A and quadrature weighting function B and subtracted. This is equivalent to convolving the signal S with effective weighting function A-B.

3.3.2 Rate Window Determination with the A-B Technique

As is evident from Figure 3.8, the weighting function A-B looks identical to a double box-car averager with sampling windows at $t=\frac{3}{8}T$ and $\frac{7}{8}T$, each with a sampling width of $\frac{1}{4}T$. Choosing a pulse width that starts at $t=0$ and ends at $t=\frac{1}{5}T$, the rate window can be computed using the formulas presented in Section 3.1.3, where the times t_1 and t_2 are measured from the pulse edge. When the pulse width equals $\frac{1}{5}T$, $t_1=\frac{7}{40}T$ and $t_2=\frac{27}{40}T$. According to Equation 3.11, the DLTS rate window time constant at which a DLTS peak will occur is

$$\tau_{max} = \frac{t_1 - t_2}{\ln(t_1 / t_2)} = \frac{\frac{7}{40}T - \frac{27}{40}T}{\ln(\frac{7T/40}{27T/40})} = \frac{T}{2\ln(\frac{27}{7})}. \quad (3.13)$$

A table of some commonly used pulsing frequencies and their corresponding time constants is given in Table 3.1.

Table 3.1 DLTS rate window time constants for the lock-in amplifier when used under the A-B technique. The pulse width is fixed at (1/5)T.

Frequency [Hz]	Period [ms]	Pulse Width [ms]	e_{max} [1/s]	τ_{max} [ms]
10	100	20	2.70	370.38
13.33	75	15	36.00	27.78
20	50	10	27.00	37.04
50	20	4	134.99	7.41
100	10	2	269.99	3.70
200	5	1	539.97	1.85

Several important relationships with regard to this electronic rate window setup should be noted. First, the sampling windows of the lock-in amplifier under the A-B technique are strongly dependent on the frequency. With a sampling width that goes as ¼T, higher frequencies will have narrower sampling windows. Higher frequencies will give more accurate measurements of $\Delta C=C(t_1)-C(t_2)$, but they will also be more susceptible to noise. Low frequencies, though advantageous in terms of signal-to-noise, will give less accurate measurements of ΔC because of the extremely wide sampling windows. Secondly, because values of t_1 and t_2 are determined by the period and the pulse edge, changing the pulse width for capture cross-section measurements is impossible since one needs to keep the rate window constant while changing the pulse width for this particular measurement. The A-B technique with the lock-in amplifier does, however, offer a convenient and easily conceptualized way of implementing a DLTS rate window. Because it parallels the box-car averager, rate window time constant determination is easily computed and energy level determinations from an Arrhenius plot can be done quickly.

3.4 Fourier Lock-in Amplifier Method

Because the capacitance transient is a periodic signal, it can be Fourier analyzed. The lock-in amplifier is no more than a tunable one-component Fourier analyzer. By knowing something about the fundamental Fourier component of an exponential transient, one can implement the DLTS rate window with a lock-in amplifier. This method (hereafter "Fourier method") works on a very different principle than the A-B technique. In fact, this method was first developed by Kimerling [56, 57] as alternative to the dual box-car averager method proposed by Lang in an effort to boost the DLTS signal-to-noise ratio. The advantages and disadvantages of each method has been discussed by Miller *et al.* [58], who show that an exponential correlator implements the optimum rate window. Nonetheless, using the lock-in amplifier as the correlator is convenient because it is a common piece of lab equipment.

Unlike the box-car averager which samples at two user-definable points in one period, the lock-in amplifier samples over the entire period. Typical capacitance meters like the Boonton 7200 have an response time of <1 ms. Thus, a capacitance meter has an inherent transient that has nothing to do with the emission of carriers from traps in the sample. In order to use the lock-in amplifier to analyze the capacitance transient, the response limitations of the equipment and subsequent overloading problems need to be negated. With a lock-in amplifier, this can be done with a device that can adjustably gate-off an arbitrary amount of time at the beginning of each cycle, sometimes referred to as a "gating-off period circuit." This type of circuit is unnecessary in dual box-car setups because the sampling windows can be moved sufficiently far away from the problem areas.

The signal response, tuning procedure, and calculation of trap concentrations from peak heights of acquired DLTS spectra have been discussed by Schott *et al.* [59] in the idealized case where the capacitance meter response time is neglected. Day *et al.* [60] have extended the analysis by figuring in the added effects of gating off a portion of the signal. Their analysis uses a signal that is referenced similarly but subtly different from the way our equipment was setup. Using the formulas of Day *et al.* can lead to phase tuning errors which they showed to have serious consequences. The referencing they used is redefined so that it matches our system and the proper time constants are recomputed.

The DLTS system used is shown in Figure 3.7; however, the output from the lock-in amplifier is only from the in-phase component channel. The Boonton 7200 capacitance meter outputs a voltage signal that is proportional to the measured capacitance for the sample located in the cryostat. This voltage signal is fed into the lock-in amplifier which implements the DLTS rate window. The results are displayed on a computer via a GPIB interface.

The lock-in output is the integral of the fundamental Fourier component of the input times the square-wave weighting function, as depicted in Figure 3.9. Time t_d is defined as the amount of time gated off from the front portion of the transient; t_ϕ is the time that corresponds to the phase of the sine-wave fundamental Fourier component; t_θ is the time corresponding to the user-adjustable phase setting on the lock-in amplifier; and t_p is the bias pulse width.

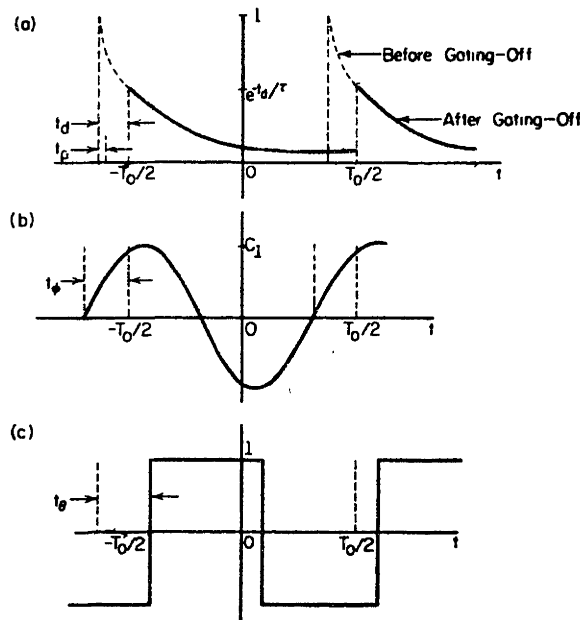


Figure 3.9 Definitions of signal and reference relationships: (a) normalized exponential capacitance transient before and after gating off, (b) fundamental Fourier component of signal in (a), (c) lock-in amplifier weighting function for phase setting θ. Here, t_θ is measured from the same point t_d is measured from above.

If one relabels the time axis so that t=0 coincides with the beginning of t_d, the transient signal of Figure 3.9(a) can be written as

$$f(t) = \exp(-\tfrac{t}{\tau}). \qquad (3.14)$$

The fundamental Fourier component of this function can be found by using standard Fourier analysis. The details of finding the Fourier coefficients can be found in Appendix A, and the basic principles behind the Fourier method are discussed in detail. A summary of the parameters used in this thesis can be found in Table 3.2 and Table 3.3. The time constants are comparable to the ones achieved with the A-B technique.

Table 3.2 DLTS rate window time constants for the lock-in amplifier when used under the Fourier method and bias phase reference mode (t_d=1.6 ms and t_p=20 μs).

Frequency [Hz]	Phase θ	τ_{max} [ms]	normalized output $\frac{C_{actual}}{C_{ideal}}$
5	~0°	84.9	0.937
10	0.1°	42.5	0.933
20	0.1°	21.4	0.918
50	0.4°	8.68	0.822
80	0.6°	5.45	0.672
100	0.7°	4.30	0.554
120	0.9°	3.43	0.429

Table 3.3 DLTS rate window time constants for the lock-in amplifier when used under the Fourier method and bias phase reference mode (t_d=1.6 ms and t_p=1.5 ms).

Frequency [Hz]	Phase θ	τ_{max} [ms]	normalized output $\frac{C_{actual}}{C_{ideal}}$
5	2.7	86.7	0.922
10	5.4	44.2	0.907
20	10.8	23.0	0.877
50	27.0	10.2	0.799
80	43.2	7.04	0.734
100	54.0	5.96	0.697
120	64.8	5.24	0.661

Here, one has the freedom to change the pulse width for capture cross-section determination, so long as $t_p \ll T_0$ and the bias phase reference mode (as discussed in Appendix A) is maintained. In the above tables, one notices that the time constants are not changed much by increasing the pulse length and keeping the gate-off time the same. Table 3.2 is shown to corroborate the results of Day *et al.* [60]; the information in Table 3.3 is used in practice because of the sufficiently long filling pulse needed to saturate traps.

Although an apparent capture cross-section can be deduced from the y-intercept of an Arrhenius plot, the capture cross-section σ_T can be measured directly by varying the length of the majority carrier filling pulse and observing the corresponding change in DLTS signal magnitude at a trap peak. The signal must saturate the traps for long filling pulses. To quote Benton [50], plotting ln[(saturated maximum signal)-(signal at pulse width equal to t)] versus pulse width t gives a slope equal to the capture rate c. The time constant τ [sec] of this trap at the peak temperature is simply $1/c$. The majority carrier capture cross-section σ_T [cm^2] is then given by:

$$\sigma = \frac{1}{\tau v_{th} n} = \left[\tau \times 6.74 \times 10^5 \sqrt{\frac{T}{m^*}} n \right]^{-1}, \qquad (3.15)$$

where m^* is the effective mass fraction for the majority carriers, n [cm^{-3}] is the free carrier concentration, and T [K] is the peak temperature. In this thesis capture cross-sections were measured with the Fourier technique, using a frequency of 10 Hz. The pulse width was changed from 1.5 ms down to 10 μs; to retain the bias phase reference mode (defined in Appendix A), the phase was accordingly adjusted. A summary of the parameters is shown in Table 3.4.

Table 3.4 Pulse widths and corresponding lock-in phase settings for DLTS measurements taken at 10 Hz. The time constant is noted to change slight; hence, a slight shifting of the peak is expected to occur.

Pulse width t_p	lock-in phase angle θ	τ_{max} [ms]	normalized output $\frac{C_{actual}}{C_{ideal}}$
1.5 ms	5.4°	44.2	0.907
1 ms	3.6°	43.6	0.916
500 μs	1.8°	43.1	0.925
100 μs	0.4°	42.6	0.932
10 μs	~0°	42.5	0.933

The time constant is noted to change when the frequency is held at 10 Hz and the pulse width is reduced. Hence, a slight shifting of the peak is expected to occur from run to run. Furthermore, the normalized output is noticed to change somewhat. Since one is measuring the peak height as a function of pulse width, the DLTS signal must be adjusted to avoid a 3% error in its magnitude.

4. Experimental Approach

The main objective of this thesis was to investigate and identify electrically active defects in bulk single crystal zinc oxide and at grain boundaries in simplified polycrystalline zinc oxide varistors. The goal was to understand defects in a simpler, but relevant and related system than those of commercial varistors. Because varistor properties are dependent on additives and subsequent processing, understanding the defect characteristics of zinc oxide is necessary to relate the chemistry of a varistor to its electrical properties.

To that end, bulk single crystals from a commercial source and single crystal films of ZnO were prepared so that DLTS could be performed on samples with different dopants and heat treatments. For the films, samples were grown by a vapor transport method on *r*-plane sapphire substrates which essentially electrically isolates a thin slab of zinc oxide on an insulating substrate. Moreover, thin film specimens have the advantage of shorter diffusion lengths such that the zinc oxide can be doped uniformly. Surface quality of the films were evaluated with environmental scanning electron microscopy (ESEM), and thicknesses were measured with a Dektak 8000 profilometer. Bulk crystal and thick film samples were subsequently doped with cobalt by a drive-in diffusion from a thin film source and/or heat treated in oxygen partial pressures of 10^{-4} atm or 1 atm. These treatments were done in an effort to change the defect concentrations so that these changes could be measured with DLTS. DLTS (Fourier method) was performed by evaporating a palladium Schottky contact on the film, along with two ohmic indium-gallium or aluminum contacts.

"Primitive" varistors with simplified chemistry were also evaluated with DLTS (A-B method). Two-phase bismuth/cobalt-doped zinc oxide was used. In a previous study [61], bismuth was observed to wet and dewet the grain boundaries in zinc oxide, depending on the heat treatment and hot-pressing procedure. DLTS and other electrical measurements were done on samples with different heat treatments whose bismuth coverage at the ZnO-ZnO grain boundaries had previously been assessed.

5. Traps in Zinc Oxide Bulk Crystal and Thick Films

Taking into consideration the zinc oxide thin film work summarized in Section 2.5.2, this chapter first discusses the experimental parameters used in growing our films. Secondly, methods that were used in preparing bulk crystal and thick film surfaces are described. Then, we present some electrical measurements and microscopy done on these films, as well as the corresponding DLTS results for samples that have undergone different heat treatments and doping.

5.1 Equipment Description and Growth Conditions for Thick Films

Growth of zinc oxide films by vapor transport was accomplished by reducing zinc oxide and moving the vapor with a carrier gas to a cooler region where the substrate was located. At the substrate, the zinc vapor was reoxidized into a solid ZnO film. A three-zone tube furnace was used to achieve temperature gradients from 25-50°C [Lindberg Blue/M]. Square centimeter substrates of *r*-plane sapphire [Union Carbide and Commercial Crystal] were used, placed 12-15 inches from the source. Hydrogen (bubbled through water) was used to reduce the zinc oxide powder source, and argon was used as a carrier gas. Oxygen was flowed such that only the substrate region of the furnace was exposed to it, as shown in Figure 5.1. Flow of argon was monitored by a flowmeter [Gilmont], and flow of hydrogen and oxygen were controlled by electronic mass flow controllers [Tylan General].

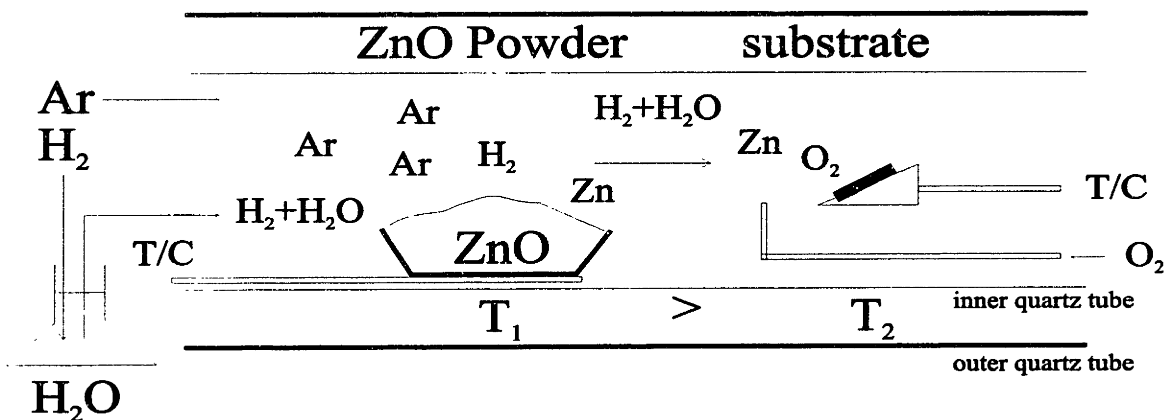


Figure 5.1 Schematic diagram of vapor transport setup used to deposit zinc oxide films. The powder source is kept at temperature T_1, and the sapphire substrates are kept at temperature T_2.

The flow rates and other experimental conditions used are summarized in Table 5.1. An inner quartz tube was used as a lining to protect the outer tube from attack by the zinc oxide at high temperatures. Zinc oxide was observed to deposit significantly only at regions near the oxygen inlet, close to the substrates, and at the very end of the reactor tube which protruded from the furnace.

Table 5.1 Flow rates and other experimental parameters used in growing zinc oxide films. (* 10% Oxygen/Argon gas mixture)

Parameter	Value
Argon flow	200 sccm
Hydrogen flow	10 sccm
Oxygen flow*	16 sccm
Source temperature	825°C
Substrate temperature	~795°C
Deposition time (H_2 on/off)	120 minutes
RF Sputter power	70 W
Sputter time	60 minutes
Argon/Oxygen sputter mix	10 mtorr/10mtorr
Substrate temperature	150-300°C

The substrates were prepared by a standard degreasing regimen. The standard degrease consisted of immersing the substrate into trichloroethylene (TCE), acetone, and methanol for at least five minutes each in an ultrasound bath. The acetone and methanol steps were repeated as necessary, and the substrates were rinsed with deionized water (DI) and dried with pressurized air [Dust-Off]. Occasionally, a chemical etch in diluted phosphoric acid (1:3) was included. The substrates were immediately loaded into the sputtering chamber [Kurt J. Lesker Company] which was pumped down to 4 x 10^{-7} torr. Thin films of zinc oxide were sputtered according to the parameters listed on the bottom half of Table 5.1.

5.2 Polishing and Metal Deposition for Schottky Barriers

As deposited films were subsequently polished to achieve smooth surfaces which are necessary for good Schottky contacts. Course polishing was done with diamond paste [Struers and Buhler] on a polishing wheel. The diamond paste grit size varied from 9 to 1 μm. The most important polishing step was the fine polishing with 0.3 μm and then 0.05 μm alumina paste by hand. Although diamond paste was capable of producing a mirror-like finish on the samples, the amount of surface damage can be further reduced by polishing with fine grit alumina paste. Typically, a sample was polished down to 0.3 μm with alumina paste; any heat treatments or in-diffusion steps were done thereafter. After heat treatment or in-diffusion, the surface was retouched with 0.3 μm and then finally capped off with the 0.05 μm polish. These final polishing steps could not be avoided because high temperature processing steps tended to roughen slightly the prepared surfaces. Obviously, when polishing the surface after a high temperature step, one does not want to polish away the defects or impurities induced during the heat treatment.

Sukkar [32, 62, 63] has shown the influence of oxygen on Schottky contacts on zinc oxide. Her findings show that a low temperature treatment in pure oxygen enhanced the I-V characteristics of her samples. Hence, polished samples were placed in a furnace under flowing oxygen at 120°C for ~5 hours before and after metal deposition to ensure that the surface was saturated with oxygen. Palladium or silver was deposited under a base pressure of ~7.5×10^{-7} torr by thermal evaporation of metal foil [Alfa Aesar] through a copper mask with small holes of diameter 1 mm. Indium-gallium paste or aluminum was typically used as an ohmic back contact.

When an in-diffusion process was involved, such as samples that required cobalt doping, the metal was deposited using an electron beam evaporator. Metal films of ~100Å were deposited onto zinc oxide surfaces and driven-in at a temperature of 1000°C for several days. A typical diffusivity for cobalt in zinc oxide at 1000°C is on the order of 10^{-13} cm^2/s [64]. For a time of 5 days,

$$x \sim \sqrt{D_{Co}t} = \sqrt{(10^{-13}\tfrac{cm^2}{s})(1.8\times10^4 s)} = 4.24\times10^{-5} cm = 0.42\mu m, \qquad (5.1)$$

which is of the order of the depletion width in zinc oxide. Samples that under went high temperature treatments were lightly repolished before Schottky barrier deposition with only 0.05 μm alumina paste. Again, polishing with anything coarser runs the risk of polishing away the in-diffused layer and was avoided where possible.

5.3 Measurement Results

Zinc oxide samples with palladium Schottky contacts had their I-V, C-V and DLTS curves measured. I-V curves were measured to gauge the magnitude of the leakage current. The Schottky contacts discussed here are much leakier than their silicon counterparts but are good enough for DLTS experiments. For example, a commonly used figure of merit for a silicon junction is <40 μA at a reverse bias of -10 V. Because metal-semiconductor junctions on zinc oxide have been known to degrade under high biases [32], the voltages used in this study were limited to -2 V. The corresponding leakage currents were on the order of ~10 μA at room temperature; cooling to 80K obviously resulted in lower leakage currents. C-V curves were taken to measure the background carrier concentration profile [65]. Typical values for the background carrier concentration N_D were 10^{16} to 10^{17} cm^{-3}, where the depletion width was ~0.2 μm. DLTS curves were taken using the Fourier method and the bias phase reference mode (see Section 3.4 and Appendix A); the frequencies used for energy level determination were 5, 10, 20, 50, and 100 Hz. When capture cross-section and concentration profile measurements were taken, the 10 Hz DLTS rate window was used.

5.3.1 Undoped Bulk Zinc Oxide Crystal (2 days at 1000°C under 10^{-4} atm O_2)

The I-V curves [HP4142] for an undoped bulk zinc oxide crystal are shown in Figure 2.1. As stated previously, relatively small reverse voltages were used to prevent electrical degradation of the palladium contacts.

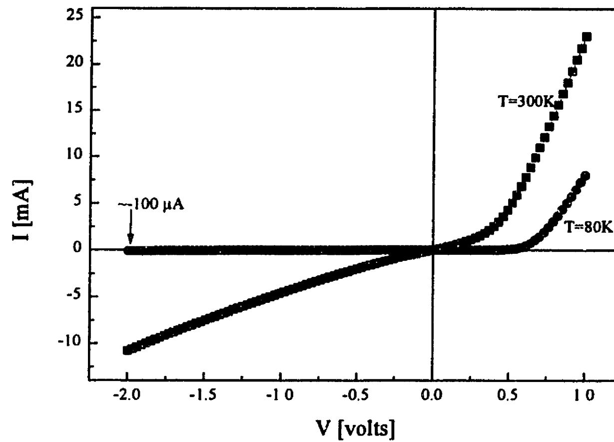


Figure 5.2 I-V curves at low and room temperatures for a Schottky barrier on an undoped bulk zinc oxide crystal heat treated in a reducing atmosphere.

As is apparent in Figure 2.1, the thermally activated leakage current is considerably smaller at low temperatures. The lowest leakage current attained at -2 V was -100 μA at 80K. Room temperature leakage currents were typically in the milliamp range at -2 volts, but some junctions that were fabricated did manifest leakage currents of around -400 μA. Surfaces with no visible surface damage and those that were adequately treated with an oxygen anneal tended to produce better Schottky contacts. Junction I-V curves were noticed to improve as more experience in their preparation was gained. The corresponding C-V plots [Boonton 7200] are shown in Figure 5.3.

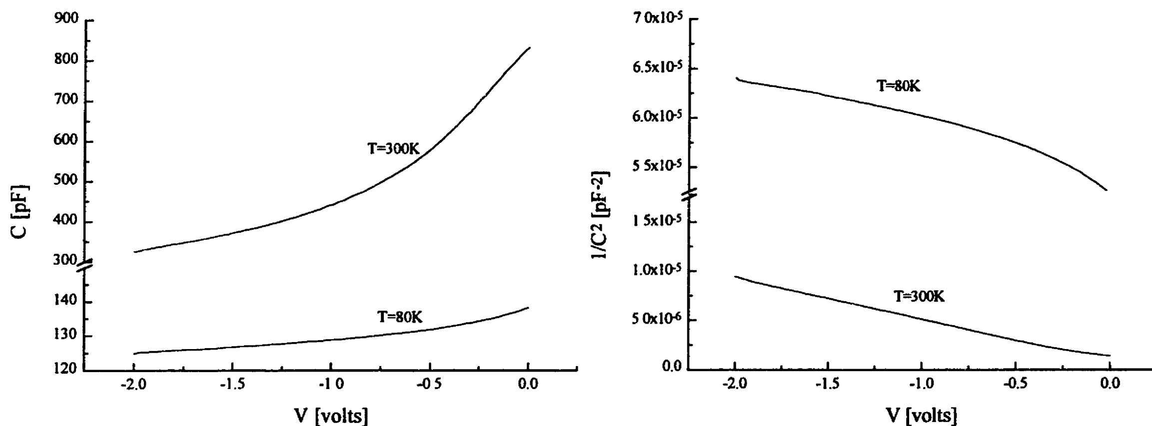


Figure 5.3 left: C-V plots at low and room temperatures for an undoped bulk zinc oxide crystal (reduced); right: Mott-Schottky representation of C-V data with slope that yields $N_D \approx 6\times10^{16}$ cm^{-3}.

The capacitance is observed to change markedly when the temperature is changed, reflecting the strong temperature dependence of the leakage current. Though the leakage

current may obscure the real meaning of the absolute magnitude of the capacitance, the Mott-Schottky slopes indicate similar background carrier concentrations of 6×10^{16} cm^{-3}.

DLTS measurements revealed two prominent defect levels, one at 0.10±0.03 eV and another at 0.20±0.03 eV. A corresponding DLTS plot of ΔC versus temperature with a 10 Hz gating is shown in Figure 5.4. Besides the two peaks prominently displayed on the low temperature side, the signal is observed to grow starting at around 250K. Though this could be interpreted as the onset of a high temperature peak, scans that beyond 350K reveal that this steady increase is most likely caused by the increase in leakage current at higher temperatures. Because the leakage current becomes so high at this point, small peaks in this region are washed out and cannot be detected with this sample.

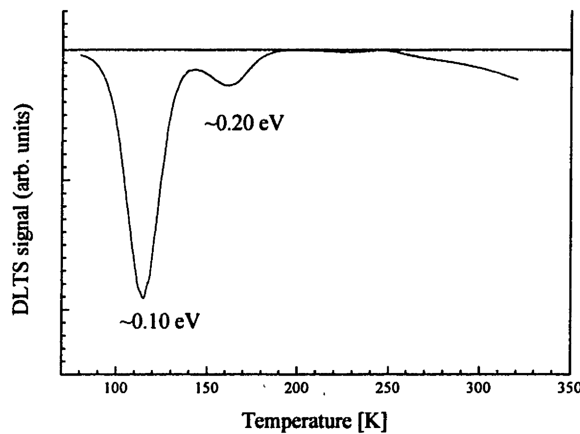


Figure 5.4 DLTS curve for undoped bulk zinc oxide crystal (reduced) with f=10 Hz, τ=44.2 ms gating (t_d=1.6 ms, t_p=1.5 ms).

The capture cross-sections is found to be ~10^{-21} cm^2 for both traps, as deduced from the y-intercepts of the Arrhenius plots. This value is suspect, since typical values cited in Table 2.1 are around 10^{-18} to 10^{-16} cm^2.

5.3.2 Undoped Bulk Zinc Oxide Crystal (2 days at 1000°C under 1 atm O_2)

The undoped bulk zinc oxide specimen was prepared in a similar manner to the previous sample, except for the oxygen partial pressure during heat treatment. Here, the sample was kept under a continuous flow of pure oxygen. The I-V curves are shown in Figure 5.5. Here, the metal used for the Schottky contact was silver, which is much more easily evaporated than palladium.

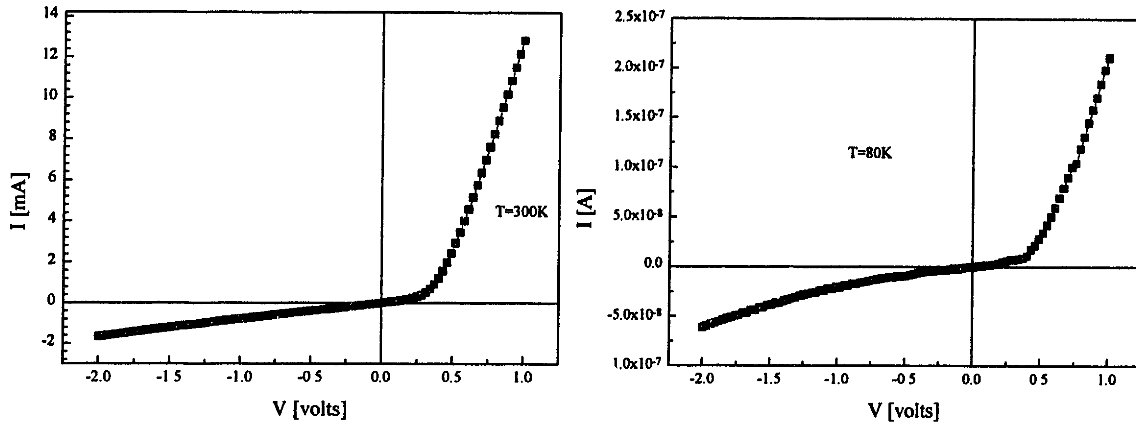


Figure 5.5 I-V curves at low and room temperatures for a Schottky barrier on an undoped bulk zinc oxide crystal heat treated in an oxidizing atmosphere.

Again, a low temperature (120°C) "oxygen soak" was done before and after the metal deposition. The drastic change in the current range for voltages of both polarities seems to indicate a lowering of the overall conductivity by several orders of magnitude. A possible cause for this is the freezing out of carriers from donors states that are dominant for this type of heat treatment. C-V curves are shown in Figure 5.5; however, the capacitance at low temperatures did not respond to applied biases, which is consistent with the low current levels. That is, if carriers in this instance became "frozen in," changes in the applied bias result in minuscule changes in the amount of charge stored which the capacitance meter cannot detect as a capacitance change.

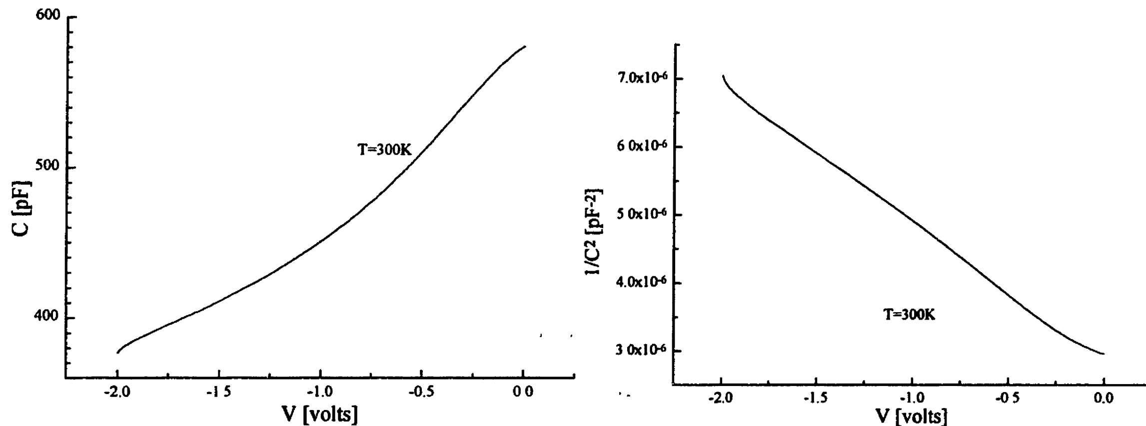


Figure 5.6 left: C-V plots at room temperature for an undoped bulk zinc oxide crystal (oxidized); right: Mott-Schottky representation of C-V data with slope that yields N_D=10^{17} cm^{-3}.

Capacitance data at room temperature indicate a background free carrier concentration of N_D=10^{17} cm^{-3}.

DLTS measurements show a positive peak at 0.23 eV in Figure 5.7. The capture cross-section is estimated at 1.3×10^{-20} cm^2. This presents a mystery as to the cause of a positive DLTS signal from a Schottky barrier. Positive DLTS signals correspond to minority carrier traps, whereas negative DLTS signals correspond to majority carrier traps. Schottky barriers are majority carrier junctions; they do not inject minority carriers as *pn*-junctions do.

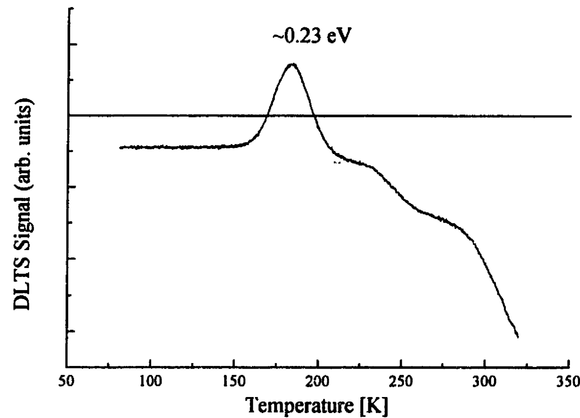


Figure 5.7 DLTS curve for undoped bulk zinc oxide crystal (oxidized) with f=50 Hz, τ=10.2 ms gating (t_d=1.6 ms, t_p=1.5 ms).

The two majority carrier trap peaks found previously in the undoped, reduced sample are not evident. If carriers are frozen out below ~130K, then levels that have peak temperature below that point cannot be seen. Another anomaly is the signal's increase as the temperature increases. This would appear to be the onset of a deep trap signal, but temperature scans out to 450K confirm that the signal continues to increase without turning over. The capacitance meter clearly reads a transient in this temperature range, but the source of this transient has yet to be determined.

5.3.3 Cobalt-Doped Zinc Oxide Crystal (5 days at 1000°C under 10^{-4} atm O_2)

Cobalt doping of zinc oxide crystals was done by using an electron beam (e-beam) evaporator which was equipped with a quartz thickness detector.[†] A 100 Å thin film was deposited from a hearth of cobalt pellets [Alfa Aesar]. This thickness was chosen so that a sufficient amount of cobalt would diffuse into the sample and that the film

[†] Richard Pirelli of the CMSE Microfabrication Lab

would be consumed during the drive-in process. For a five-day anneal at 1000°C the diffusion length is approximately 0.42 μm [64]. The sample exhibited a light green color after the anneal and retained its greenish tinge after a light polish with alumina paste to re-smooth the surface.

The I-V curves for this cobalt-doped sample are shown in Figure 5.8. The leakage is further improved from the previous two samples, but the current level is still within the milliamp, four orders of magnitude higher than preferable.

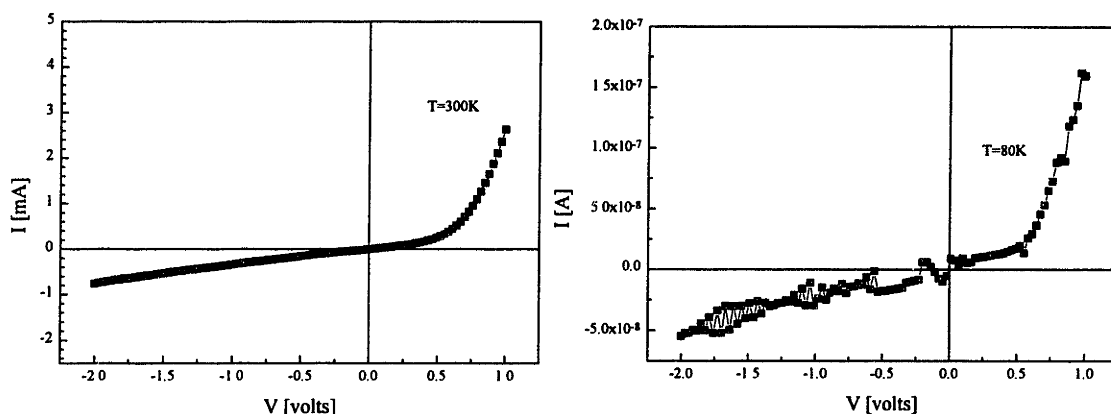


Figure 5.8 I-V curves at low and room temperatures for a Schottky barrier on a cobalt-doped bulk zinc oxide crystal heat treated in a reducing atmosphere.

Capacitance-voltage measurements shown in Figure 5.9 do not deviate significantly from the types of results attained on the previous samples. And again, the capacitance did not respond to biasing at low temperatures. The C-V characteristic is however noticed to be flatter than undoped specimens.

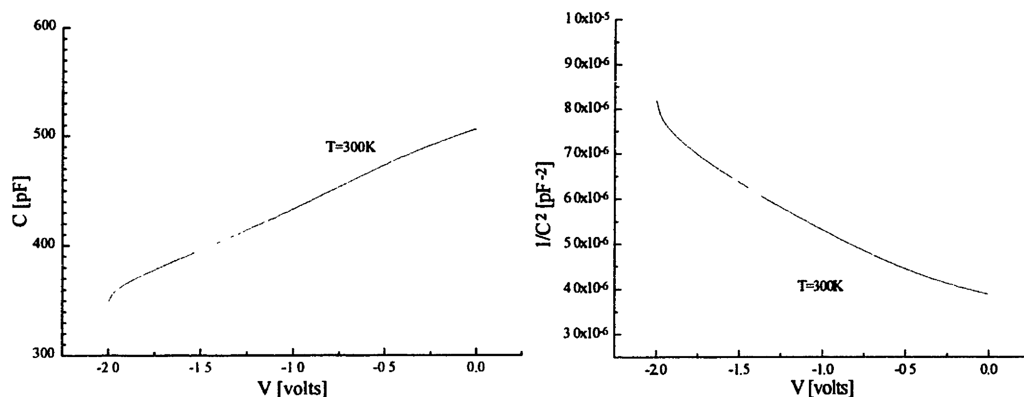


Figure 5.9 left: C-V plots at room temperature for a cobalt-doped bulk zinc oxide crystal (reduced); right: Mott-Schottky slope yields $N_D \approx 6 \times 10^{17}$ cm^{-3}.

The DLTS plot shown in Figure 5.10 resembles the spectrum attained for the undoped, oxidized sample. Again, a positive peak and an increasing negative signal for higher temperatures describe this plot.

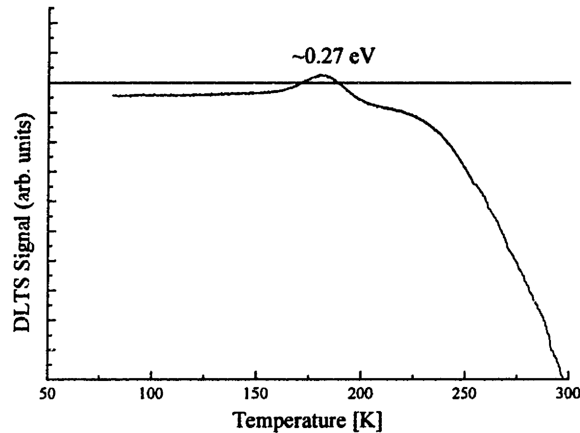


Figure 5.10 DLTS curve for as-grown zinc oxide film with f=50 Hz, τ=10.2 ms gating (t_d=1.6 ms, t_p=1.5 ms).

5.3.4 Undoped Bulk Zinc Oxide Film (as-grown)

Films that were grown by the vapor transport technique described in Section 5.1 were also evaluated for electrically active defects. Bulk defect information in films is necessary if this technique is to be extended to bicrystal studies and studies of defect levels specific to grain boundaries. As-grown samples (1 to 2 microns thick) directly from the furnace on r-plane sapphire all exhibit a regular striation pattern that was previously observed by others [46-48]. Micrographs of the smoothest striated ZnO films $(11\underline{2}0)$ used in this study were attained by environmental scanning electron microscopy (ESEM) and are shown in Figure 5.11.

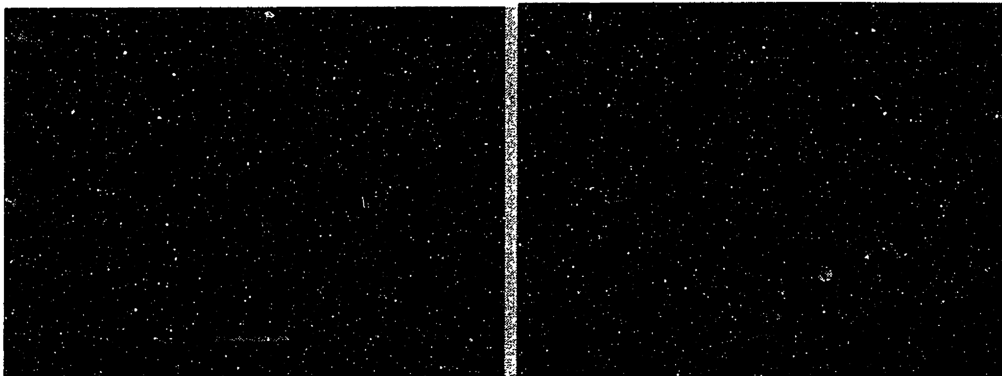


Figure 5.11 left: ESEM picture of as-grown film; right: film after polished to 0.3 µm.

The striated film on the left is too rough as far as Schottky contacts are concerned. Using a profilometer, the roughness was ~0.1 μm, whereas the film thickness was ~2 μm. The films were subsequently polished to 0.3 μm, and the final thickness was 1.5 μm. Films were noted to contain some holes on which no zinc oxide grew; they were usually centered about defects in the substrate. For films that were polished, metal contacts were deposited in a fashion similar to that used for bulk single crystals.

A measure of the film crystallinity was ascertained by using small angle x-ray diffraction.† Aside from the 2θ peak occurring at 56.6° for the (11$\underline{2}$0) orientation in zinc oxide, χ and φ rocking curve patterns were taken, as shown in Figure 5.12.

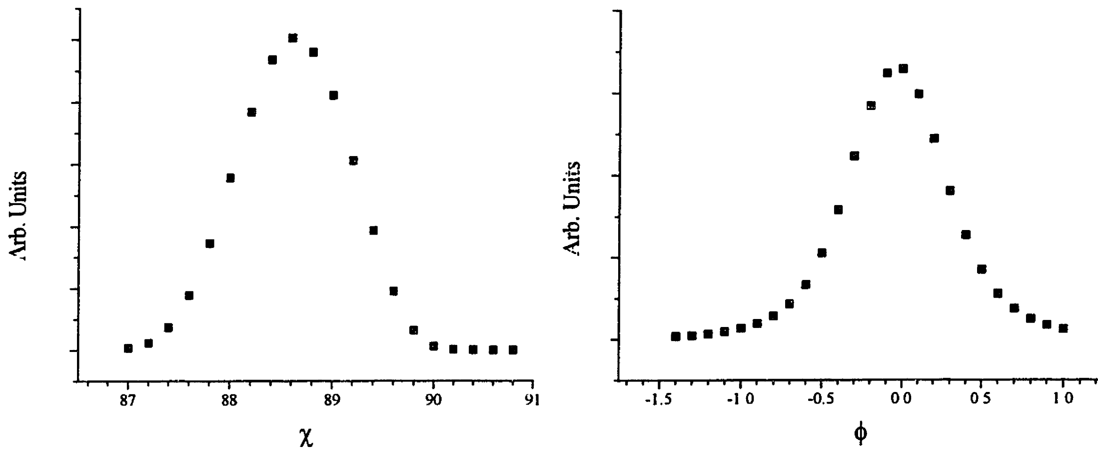


Figure 5.12 χ and φ rocking curve data for (11$\underline{2}$0) zinc oxide films grown on r-plane sapphire.

The full-width/half-max (FWHM) values for χ and φ are roughly 1.2° and 0.7°, respectively. These values approach the measurement resolution of the instrument used; hence, the films are single crystalline and not textured, mosaic polycrystals.

The I-V curves for this cobalt-doped sample are shown in Figure 5.13. Here, note that even though the measurement is taken at room temperature, the current levels are exceedingly small for the film in comparison to the results attained on bulk samples. A sheet resistivity of 100 Ω/□ was measured using a four point prober [Four Dimensions, Inc. Model 101]. For a thickness of 1.5 μm, the corresponding resistivity is 1.5×10^{-2} Ω·cm. For a mobility of 200 $\frac{cm^2}{V \cdot s}$ [66], the carrier concentration is a low 4.7×10^{14} cm^{-3}.

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† Dr. Imtiaz Majid

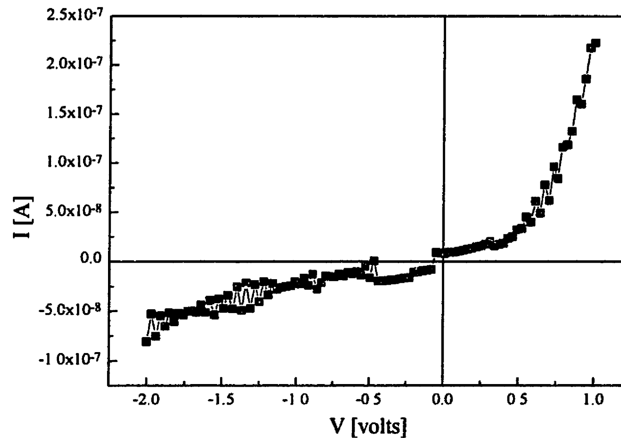

Figure 5.13 I-V curves at room temperature for a Schottky barrier on an undoped, as-grown bulk zinc oxide film.

Needless to say, this very low value for the carrier concentration puts the depletion width beyond the thickness of the sample, and the capacitance (~37 pF) did not respond greatly to the biases used in this study.

Because as-grown samples are relatively insulating, further processing is required to increase the carrier concentration. For example, an equilibrating anneal in a reducing environment could be done to induce oxygen vacancies or zinc interstitials in order to achieve an more useful electron concentration. Extrinsically doping with a shallow donor (e.g. Al) is an attractive alternative because the carrier concentration can be fixed regardless of the heat treatment. Some previous efforts of depositing indium- or aluminum-doped zinc oxide films have been pursued by various techniques [67, 68, 69, 70], but many of these studies focus on polycrystalline thin films, instead of single crystal ones. Donor doping is discussed further in Chapter 7.

6. Simplified Zinc Oxide Varistors

As discussed previously in Section 2.4, researchers have moved toward simplifying varistor system in order to study the nonlinear varistor grain boundary effect. The move to simplified systems, either in geometry and/or chemistry, is made with the intention to understand grain boundary electrical properties in terms of models like the double Schottky barrier introduced in Section 2.2. The ultimate goal is to understand the defect conditions at a given grain boundary so that one is able to predict its electrical characteristics. Work at MIT has pursued both simplification of geometry (Sukkar [32] and Baek [34]) and chemistry (Lee [61]).

6.1 Sample Description

The samples studied here originated from previous studies by Lee and Chiang [36, 61, 71, 72] of Bi segregation in ZnO as a function of composition, microstructure, pressure, and thermal history. The samples were hot-pressed from co-precipitated Bi and Co doped powders into 6.35 mm diameter, 1 mm thick discs. Scanning transmission electron microscopy (STEM) has shown that the grain boundary coverage of Bi can be systematically varied [61, 36]. We electrically characterized two particular sets of samples, both initially fired for 1-2 hours at 1150°C, 1000°C, and 850°C, and then either (a) slow-cooled at 150°C/hr, or (b) slow-cooled at 150°C/hr with an additional arrest at 700°C for 24 hours. The grain sizes of the samples examined varies with the initial firing temperature, while the average value and boundary-to-boundary variability of Bi segregation varies with the cooling procedure [61, 72]. I-V curves were measured for these samples using a HP4041B pA meter/dc voltage source.

DLTS spectra were taken over the temperature range 80-600K, using 1 mm^2 silver paste electrodes. The rate window was implemented by a two-phase lock-in amplifier that simulated a two-channel box-car averager (A-B technique). The rate window time constants ranged from 37 ms to 1.9 ms. The bias settings were a "reverse" voltage of V_R=0V and a forward pulse voltage of V_P=20 V (zero quiescent bias case; see Section 3.2.1).

6.2 DC Electrical and DLTS Measurement Results

Results from Lee and Chiang [61, 72], illustrating the variation in Bi segregation with heat treatment, are shown in Figure 6.1. Heat treatment (a) gives a broad distribution in bismuth segregation from boundary-to-boundary, whereas heat treatment (b) yields highly uniform Bi segregation, due to dewetting of the boundaries at temperatures below the eutectic. The final coverage in the latter case has an average value of Γ_{Bi}=0.88 monolayers, regardless of grain size.

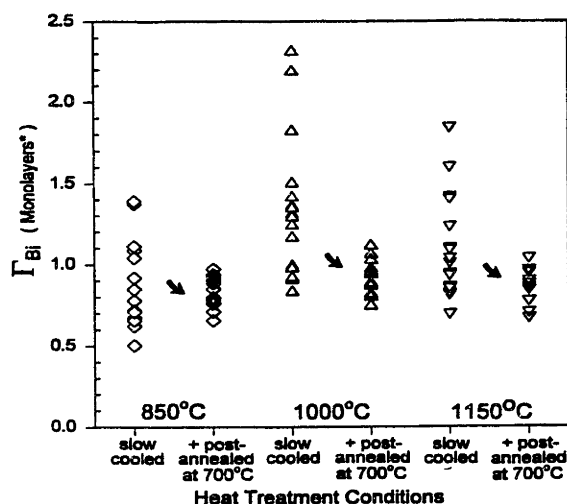

Figure 6.1 Bismuth segregation at zinc oxide grain boundaries as measured by STEM, showing a tightening of the segregation distribution with an added post-anneal below the B_2O_3-ZnO eutectic. [61, 72]

Current-voltage measurements were performed to evaluate the electrical properties of these samples, highlighting the possible effects of grain size and bismuth distribution on leakage current and barrier height.† Samples with and without the 700°C thermal arrest manifest similar I-V characteristics, despite having markedly different bismuth segregation distributions. Figure 6.2 illustrates the I-V curves for samples (a) slow cooled from their initial temperature and (b) slow cooled with an additional 700°C arrest.

† done with Jonq-Ren Lee

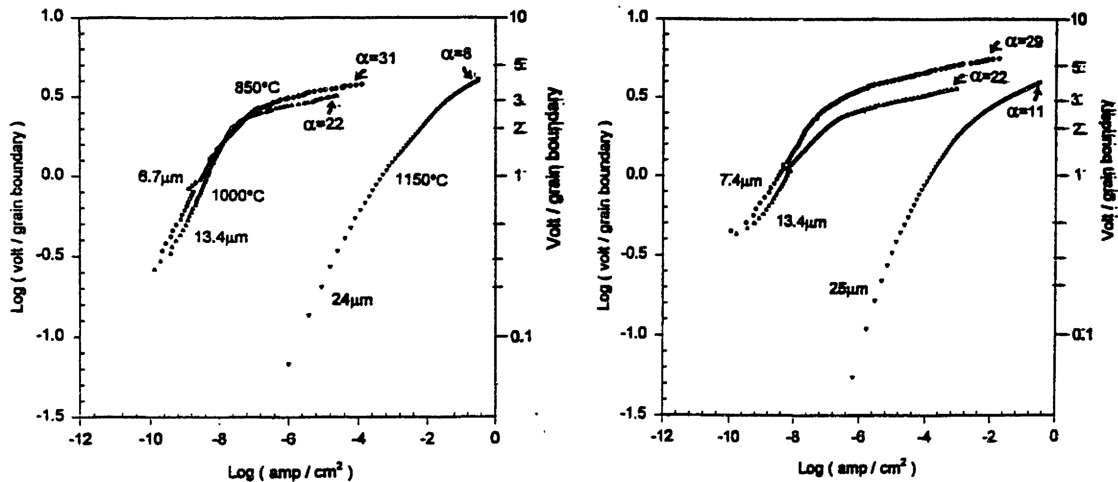

Figure 6.2 I-V curves for samples (a) slow cooled from their initial temperature and (b) slow cooled with an additional 700°C arrest.

Here, one notes the high leakage current for the large grain samples that have seen 1150°C. Indeed, even though these samples contain only the nominal ingredients of commercial varistors, the smallest grained samples still exhibit α values on the order of 30. The low α values and relative leakiness of the large grained samples has been ascribed to thermal expansion anisotropy stresses which may result in uneven oxidation during cooling [61]. Other details of the I-V characteristics are given in reference 61. Furthermore, for a fixed sample thickness, a larger grained sample has fewer boundaries from end to end and would thereby present a higher probability for a leaky pathway. This becomes less of a problem as the number of boundaries across the sample becomes large.

DLTS results in Figure 6.3 and Figure 6.4 show two shallow bulk levels at ~0.14 eV and ~0.24 eV and one prominent interface level at ~1 eV.

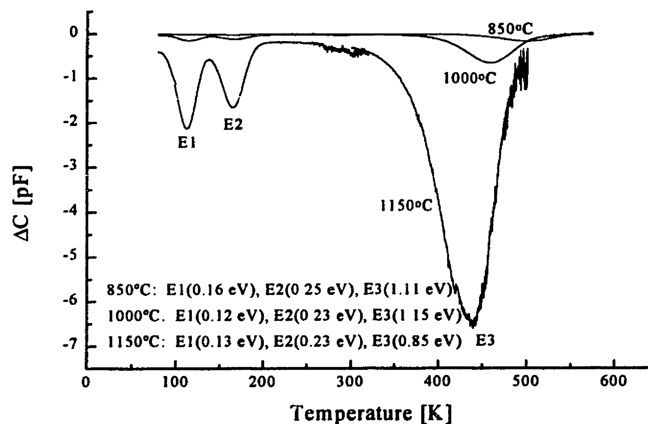

Figure 6.3 DLTS curve of samples slow cooled from their initial annealing temperature without any oxidative post-anneal. (τ=7.41 ms)

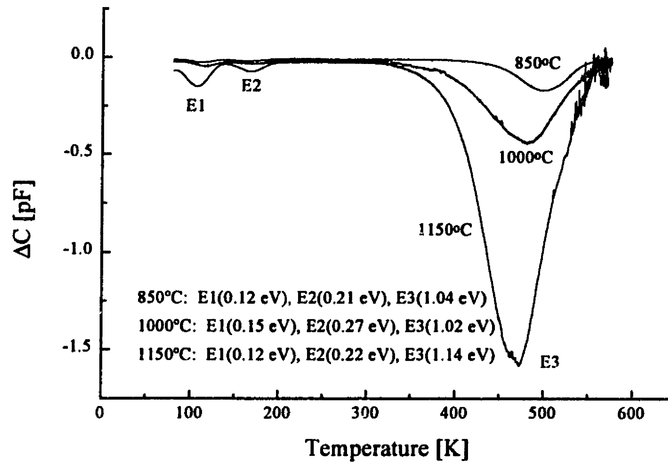

Figure 6.4 DLTS curve of samples slow cooled from their initial annealing temperature with an oxidative post-anneal at 700°C for 24 hours. (τ=7.41 ms)

From the Arrhenius graphs used to determine the energy, the capture cross-section for E1 is ~10^{-18} cm2, ~2×10^{-17} cm^2 for E2, and 10^{-15} to 10^{-12} cm^2 for E3. In spite of having only the nominal chemical components for varistor action, the BiCo-doped zinc oxide exhibits two of the signature defect levels found in many commercial varistors. [4] Further, this three-peak signature is present even when the bismuth distribution at the grain boundaries is dramatically changed. There is a decrease in the DLTS signal magnitude with the additional 700°C post-anneal. Given that the DLTS signal G ~ (N_D-N_A), the background carrier concentration, it is logical that a 700°C anneal for 24 hours would lower the carrier concentration and thus decrease the overall DLTS peak height.

7. Discussion

Previous studies have focused on "real" varistor systems which are polycrystalline and multi-dopant. In these studies defects have been identified as key players in the grain boundary electrical activity, where the origin of these defects can be either intrinsic or extrinsic. To understand the nature of these electrically active defects, simpler systems were sought. Using deep level transient spectroscopy (DLTS), we examined the bulk region near a zinc oxide surface to identify electrically active defects. These defects near the surface of a single crystal of zinc oxide are presumably similar, if not identical, to the bulk defects in the grains of a polycrystalline sample for a given processing condition. A comparison of the findings in the single crystal samples is made with BiCo-doped polycrystalline samples which previously had their grain boundary chemistry evaluated with STEM.

7.1 Defect Levels: DLTS Measurements

DLTS is a powerful technique that can be used to evaluate and identify defects in semiconductors. Its value in silicon processing is well-established, and it has been widely extended to other systems. Although DLTS can determine many defect state parameters such as the energy level, capture cross-section, and concentration, it relies on the definite capacitance of a rectifying junction to give quantitative results. As seen in Chapter 3, the background carrier concentration N_D is an important parameter to keep fixed such that junction capacitances will be well-defined. Variations in background carrier concentration are undesirable when performing DLTS measurements, because background carriers are needed to define the capacitance and to fill the traps.

The DLTS plots are shown in Figure 5.4, Figure 5.7, and Figure 5.10. Each peak on a typical DLTS plot corresponds to a particular trap energy level, where the peak temperature corresponds to the maximum emission rate of the trap for a given DLTS rate window. Of the three figures, only Figure 5.4 for the undoped, reduced sample shows a typical DLTS trace with two peaks in the low temperature range, corresponding to trap levels located at ~0.10 eV and ~0.20 eV. Instead of exhibiting two similar negative peaks,

the following two plots for the undoped, oxidized and cobalt-doped samples each show one positive peak at a slightly higher energy (~0.23 eV and 0.27 eV). As mentioned earlier, positive peaks correspond to minority carrier traps, but the Schottky junction does not involve minority carriers. The meaning of these peaks is unclear, but they seem to occur right after a region of absolutely no signal. The peak in these cases may correspond to the unfreezing of traps from their deep donor states. The presence of deep donor states is discussed in light of current voltage and capacitance-voltage measurements. Figure 5.7 and Figure 5.10 also show a signal that grows more and more negative as the temperature increases; Figure 5.4 also shows a similar, but less severe downward turn. The origin of this transient could be actual emission from surface states, but more work will need to be done to elucidate this phenomenon.

7.1.1 Junction Quality: Current-Voltage Measurements

Detailed studies of Schottky barriers on zinc oxide crystals have previously been studied in the past by Mead [73] and Neville and Mead [74]. Further studies were done by Sukkar [32]. The quality of such barriers is closely tied with its surface preparation. For example, Schottky barriers on silicon are deposited usually after a stringently controlled RCA1, RCA2, and HF dip cleaning cycle (not necessarily in that order) to remove contaminants and any native oxide, as well as to passivate the surface. Schottky barriers of low leakage and high stability are thus fabricated. For marred or dirty wafer surfaces, it is well-known that leaky junctions are formed.

When working in a less "mature" semiconductor such as zinc oxide, one is not afforded the same level of control in sample preparation. As seen in Figure 5.2, Figure 5.5, and Figure 5.8, the resultant I-V curves are all different. Despite similar background carrier concentrations measured via C-V curves, an undoped, reduced ZnO crystal exhibited a 25 mA current at a bias of 1 V, while an undoped, oxidized crystal showed 13 mA. Similarly, the reverse bias leakage current shows a similar variation from sample to sample. Variations in the amount of current passed from sample to sample can come from one of two sources: (1) heat treatments and doping effects which modify the carrier concentration significantly such that the ideal reverse saturation current and bulk conductivity

are affected, or (2) the individual surface preparation for each specimen before metal deposition. That is, if a given sample's surface is wrought with imperfections, resultant surface states at the metal/semiconductor interface often leads to junction leakiness. Each of these effects is discussed individually.

The reverse current is particularly illustrative of the dominance of nonidealities. For an ideal Schottky barrier, the reverse current is

$$J_0 \propto \exp(-\tfrac{\Phi_B}{kT}), \tag{7.1}$$

where Φ_B (~0.6 eV) is the barrier height from the metal to the semiconductor. A comparison of the reverse current at the temperatures 300K and 80K yields the ratio:

$$\frac{J_0(300K)}{J_0(80K)} = \frac{\exp(-\frac{\Phi_B}{k(300)})}{\exp(-\frac{\Phi_B}{k(80)})} = \exp\left[-\tfrac{\Phi_B}{k}\left(\tfrac{1}{300} - \tfrac{1}{80}\right)\right] \sim 5 \times 10^{27}. \tag{7.2}$$

Whereas the ideal reverse saturation current at room temperature is on the order of picoamps at room temperature, the ideal reverse saturation current at liquid nitrogen temperatures is truly minuscule. In Figure 5.2, Figure 5.5, and Figure 5.8 the I-V curves at low temperatures show reverse saturation currents smaller by about six to eight orders of magnitude, still within the measurement range of the measurement machine. This demonstrates that the junctions are nonideal and manifest a leakiness that is probably caused by surface states.

In fact, Gatos [75, 76] has summarized the surface state difficulty for less well-developed semiconductors like zinc oxide. The effect of the surface states is to pin the Fermi level such that the barrier height is different from that predicted by Schottky's theory, presented in Section 2.2.1. If the effect of the surface states is to lower the barrier height, then higher reverse saturation currents (perhaps in the milliamp range) would be expected. For lower barrier heights between 0.1 and 0.2 eV, the ratio between the current densities at 300K and 80K, as in Equation (7.1), is between 10^4 and 10^9.

Previous researchers have prepared junctions by first polishing and then immersing their crystals into concentrated phosphoric acid and/or concentrated hydrochloric acid for 10-15 minutes [20, 32, 74]. Zinc oxide is known to be extremely reactive with these acids and readily etches, even in dilute concentrations. Violently etching the surface of a

semiconductor as preparation for Schottky barrier deposition is antithetical to processing used for silicon. However, such a violent conditioning of the surface may be just the treatment needed to eliminate surface states on zinc oxide. Though this surface preparation method has been successful for others, it was not used in this work because there is no control over the etch rate. Furthermore, because our heat treatments typically occurred in a micron-thick surface layer, such rampant etching would negate any previous heat treatments and doping runs.

7.1.2 Carrier Concentration: Capacitance-Voltage Measurements

Leaky junctions are problematic for capacitance-voltage measurements. The capacitance of a metal/semiconductor junction is measured by the Boonton 7200 at some fixed bias V by superimposing a small 1 MHz oscillating voltage ΔV_{osc}. The depletion width remains approximately constant, while the capacitance is determined by measuring the induced current from the oscillating voltage. Junctions which are too leaky exhibit very high current levels and saturate the meter. Moreover, any extra leakage current may obscure the capacitive component of the current, causing the capacitance to read higher than normal. Though the presently used junctions are not ideal, they were able to yield C-V data as shown in Figure 5.3, Figure 5.6, and Figure 5.9. Nevertheless, the nonideal nature of the junctions are readily seen when extrapolating the Mott-Schottky lines to the x-axis; in the ideal case, the extrapolation would indicate the built-in potential V_{bi}. Mead [73] has shown that ~0.6 V is the ideal value for silver and palladium contacts on ZnO. Because of excessive leakage in our samples, the built-in potential cannot be determined from our data.

No sample used in this study was doped with a shallow donor (e.g. Al) to attain a certain background carrier concentration. The carriers were either (1) from intrinsic defects induced by a heat treatment or doping with cobalt or (2) from an unknown background impurity. The slope of the Mott-Schottky plots indicate carrier concentrations of 10^{16} to 10^{17} cm^{-3}, which seem reasonable in light of the I-V curve data. However, because carriers may originate from an unknown, deeper level, they may have a possibility of freezing out at low temperatures.

Freezing out at low temperatures is likely if the background impurity level is such that the zinc oxide is close to the compensated regime. For an oxidation reaction of the form

$$\tfrac{1}{2}O_2 + V_O^{\bullet\bullet} + 2e' \rightarrow O_O, \tag{7.3}$$

the corresponding equilibrium constant is

$$K_{ox} = \frac{1}{P_{O_2}^{1/2}[V_O^{\bullet\bullet}]n^2}. \tag{7.4}$$

Thus for a partial pressure change from 10^{-4} to 1 atm, the electron concentration is expected to change by a factor of 10. Both the low temperature reverse and forward currents shown in Figure 5.5 exhibit decreases greater than a factor of 10 when compared to the low temperature I-V curve in Figure 5.2. In each case, the leakage decreases a certain amount at low temperatures because the available thermal energy to surmount the junction barrier decreases. However, in the case of Figure 5.5, the number of carriers in the semiconductor is severely reduced because of the presence of compensating impurities. A similar occurrence is probably happening for the cobalt-doped sample.

Hence, at low temperatures, fewer electrons are available to hop through the junction. In fact, if the carrier concentration drops significantly, the depletion width will increase, and the capacitance will drop. If enough carriers are depleted such that the semiconductor is essentially compensated (i.e. an insulator), then the final capacitance will not respond to external biasing. Indeed, this is observed in the undoped, oxidized sample and the cobalt-doped sample. In fact, the capacitance typically dropped from hundreds of picofarads at room temperature to near zero when cooled with liquid nitrogen. A possible solution would be to introduce a shallow donor to fix the background carrier concentration and prevent this freeze out from occurring. For example, arsenic doping of silicon will fix the carrier concentration until about 40K.

7.2 Comparison of Single and Polycrystal Measured Defect Levels

Many of the results attained for BiCo-doped zinc oxide polycrystalline samples have been discussed in Chapter 6. Because bismuth segregation has never before been so well-quantified, these are the first DLTS experiments that have examined defect levels

with controlled boundary chemistry. The samples of Lee and Chiang [71, 72] do not show any significant differences in defect levels, even though some samples have a very broad bismuth distribution and others have a very tight one. The fact that bismuth is a necessary ingredient for varistor formation and yet does not radically change the defect levels or electrical properties seems to indicate that it is there to enhance other effects. For example, bismuth seems to play a role in grain boundary oxygen transport [77], where oxygen adsorbed at the grain boundaries causes the nonlinear electrical properties to occur. Thus, careful control on grain boundary oxygen content may produce visible differences in bulk and interface energy levels.

Thus far, the correspondence between bulk levels found in these polycrystalline samples with those found in single crystal samples is qualitative. There is a good match between the polycrystalline bulk states of 0.14 eV and 0.24 eV and the single crystal bulk states of 0.10 eV and 0.20 eV. These results do not match the findings of Simpson and Cordaro [20], where only one trap located at 0.3 eV was found, though their measurement of a capture cross-section on the order of 10^{-14} cm^2 seems more reasonable than the small cross-sections attained in our study. Differences in sample preparation may have contributed to this discrepancy. In order to pursue understanding of these defects further, a basic understanding of surface preparation must be achieved. If etches in concentrated acids are the only way to prepare zinc oxide surfaces for Schottky barrier deposition, this must be reconciled with the desire to control the bulk defect properties by various heat treatment and doping methods which only penetrate the surface a couple of microns.

8. Summary

Bulk electrically active defects in zinc oxide were studied as a function of heat treatment and doping. Heat treatments consisted of anneals in various oxygen partial pressures over several days at 1000°C. The dopant used in this study was cobalt, a commonly used dopant in commercial zinc oxide varistors. Schottky barriers were deposited on bulk and thick film crystal surfaces in order to use the DLTS technique to evaluate the defect parameters of energy level and capture cross-section. The fabricated junctions were not ideal as evidenced by I-V and C-V measurements. The nonidealities in reverse saturation current are attributed to imperfect surface preparation. DLTS spectra in an undoped, reduced zinc oxide specimen reveal two electrically active traps at $\sim 0.10 \pm 0.03$ eV and $\sim 0.20 \pm 0.03$ eV. DLTS plots on an undoped, oxidized sample and a cobalt-doped, reduced sample show an anomalous positive peak at 0.23 eV and 0.27 eV. All DLTS samples showed a signal that grew more negative with increasing temperature.

Varistor properties have been characterized in BiCo-doped zinc oxide in which the grain boundary coverage of Bi has been systematically varied [36, 61-72]. Samples with considerable boundary-to-boundary variation in Bi coverage have been compared with samples with highly uniform Bi segregation. Despite dramatic change in Bi segregation the I-V characteristics remain about the same in both types of samples, with a maximum α value of 30. DLTS has been used to characterize interfacial and bulk traps in these BiCo-doped varistors. Two shallower bulk levels were found at $\sim 0.14 \pm 0.02$ eV and $\sim 0.24 \pm 0.03$ eV, and one interface level at ~ 1 eV was observed. Though slightly higher than those measured by us in single crystal samples, the energy levels found here give good correspondence to those found in one of the bulk specimens. Despite dramatic changes in bismuth distribution with an additional post-anneal, DLTS peaks show the same defect levels. The relative peak heights of the DLTS signal are consistent with a lowering of the background carrier concentration during an extra oxidative anneal. Taken together with I-V characteristics, these "primitive" varistors manifest key varistor attributes despite their simplification in chemistry.

9. Future Work

Commercial zinc oxide varistors are a complicated systems of dopants and second phases, each influencing the defect structure of the material and, by extension, its electrical properties. The effort to understand the nature of individual electrically active defects has been limited to the study of undoped material and material doped with one or two key dopants such as cobalt and bismuth. These studies can be extended by (1) increasing the range of oxygen partial pressures used, (2) fixing the background carrier concentration of the zinc oxide in single crystal studies by doping with aluminum, (3) doping with other possible electrically active defects (like Mn and Ni) to build a catalog of defects in zinc oxide, and (4) doping with two or more elements. Another course of action is to fabricate zinc oxide bicrystals on sapphire substrates to learn about interface states and grain boundary misorientation. The growth work pursued in this thesis is a first step in fabricating a well-defined boundary that can be activated through standard in-diffusion processes. Once such boundaries can be made, the individual contributions of dopants such as Bi, Co, Mn, Ni, and perhaps oxygen can be analyzed.

Appendix A: Fourier Analysis of Exponential Transient

This appendix follows the material presented by Day *et al.* [60]. The difference in analysis occurs when referencing the lock-in phase angle θ. Though the results as far as the lock-in amplifier is concerned appear to be the same, they differ in the fundamental Fourier phase factor ϕ_1. The coefficients for the Fourier expansion of this function can be found by using the standard formulas:

$$f(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}\left[a_n \cos(\frac{2\pi nt}{T_0}) + b_n \sin(\frac{2\pi nt}{T_0})\right] \quad \text{(A.1)}$$

or

$$f(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty} c_n \cos(\frac{2\pi nt}{T_0} + \phi_n), \quad \text{(A.2)}$$

where

$$a_n = \frac{2}{T_0}\int_0^{T_0} f(t)\cos(\frac{2\pi nt}{T_0})dt \quad \text{(A.3)}$$

$$b_n = \frac{2}{T_0}\int_0^{T_0} f(t)\sin(\frac{2\pi nt}{T_0})dt \quad \text{(A.4)}$$

$$c_n = \sqrt{a_n^2 + b_n^2}\,,\ \phi_n = \tan^{-1}(\frac{a_n}{b_n}) \quad \text{(A.5)}$$

Hence the fundamental Fourier component $f_1(t)$ can be written as $c_1 \cos(\frac{2\pi nt}{T_0} + \phi_1)$. For an exponential transient of the form,

$$f(t) = \exp(-\frac{t}{\tau}) \quad \text{(A.6)}$$

the fundamental's coefficients a_1, b_1, c_1, and ϕ_1 are found by integrating over one period $[t_d, T_0+t_d]$ as defined in Figure 3.9:

$$a_1 = \frac{T_0}{2}\exp(-\frac{t_d}{\tau})\left[\frac{(e^{-T_0/\tau} - 1)(-\frac{1}{\tau}\cos\frac{2\pi t_d}{T_0} + \frac{2\pi}{T_0}\sin\frac{2\pi t_d}{T_0})}{(\frac{T_0}{2\tau})^2 + \pi^2}\right], \quad \text{(A.7)}$$

$$b_1 = -\frac{T_0}{2}\exp(-\frac{t_d}{\tau})\left[\frac{(e^{-T_0/\tau} - 1)(\frac{1}{\tau}\sin\frac{2\pi t_d}{T_0} + \frac{2\pi}{T_0}\cos\frac{2\pi t_d}{T_0})}{(\frac{T_0}{2\tau})^2 + \pi^2}\right], \quad \text{(A.8)}$$

$$c_1 = \frac{\exp(-\frac{t_d}{\tau})(e^{-T_0/\tau} - 1)}{\sqrt{(\frac{T_0}{2\tau})^2 + \pi^2}}, \tag{A.9}$$

$$\phi_1 = \tan^{-1}\left[\frac{\frac{1}{\tau}\cos\frac{2\pi t_d}{T_0} - \frac{2\pi}{T_0}\sin\frac{2\pi t_d}{T_0}}{\frac{1}{\tau}\sin\frac{2\pi t_d}{T_0} + \frac{2\pi}{T_0}\cos\frac{2\pi t_d}{T_0}}\right]. \tag{A.10}$$

Recall that the lock-in output is the integral of the fundamental Fourier component of the input times the square-wave weighting function. To compute the lock-in output G, three integrals covering different time domains need to be calculated:

$$\begin{aligned} G(\tau) &= -\frac{1}{T_0}\int_{t_d}^{t_\theta} f_1(t)dt + \frac{1}{T_0}\int_{t_\theta}^{\frac{T_0}{2}+t_\theta} f_1(t)dt - \frac{1}{T_0}\int_{\frac{T_0}{2}+t_\theta}^{T_0+t_d} f_1(t)dt \\ &= \frac{2}{\pi}\frac{\exp(-\frac{t_d}{\tau})(e^{-T_0/\tau} - 1)}{\sqrt{(\frac{T_0}{2\tau})^2 + \pi^2}}\cos(\theta + \phi_1). \end{aligned} \tag{A.11}$$

Despite the difference in the integration limits, the expression for the lock-in output signal is of the same form as the one derived by Day *et al.* However, ϕ_l in their analysis turns out to be:

$$\phi_1 = \tan^{-1}\frac{T_0}{2\pi\tau}. \tag{A.12}$$

This change of the phase factor ϕ_l is due to the referencing of the lock-in phase; Day *et al.* reference their lock-in phase to the gate-off edge, whereas we reference it all the way back to the start of the pulse. For $t_d \ll T_0$, the ϕ_l given in Equation A.10 converges to the one in Equation A.12.

For a given T_0 and t_d, one is interested in finding the exponential time constant τ_{max} that causes the signal G to be a maximum, similar to the box-car averager situation. The rate window time constants may be computed by taking $dG/d\tau=0$ and solving for τ_{max}, but the result yields an equation that cannot be explicitly solved for τ:

$$\begin{aligned} \exp(-\frac{T_0}{\tau})&\left\{\left[(2 + \frac{2t_d}{T_0})\left((\frac{T_0}{2\tau})^2 + \pi^2\right) + \frac{T_0}{2\tau}\right]\cos(\theta + \phi_1) + \pi\sin(\theta + \phi_1)\right\} \\ &-\left[\frac{2t_d}{T_0}\left((\frac{T_0}{2\tau})^2 + \pi^2\right) + \frac{T_0}{2\tau}\right]\cos(\theta + \phi_1) - \pi\sin(\theta + \phi_1) = 0. \end{aligned} \tag{A.12}$$

For a given gate-off delay time t_d, lock-in frequency $f(=1/T_0)$, and lock-in phase angle θ, this equation can be solved numerically to yield τ_{max}, the time constant of the exponential input signal at which the DLTS (lock-in) signal will be a maximum.

The gate-off delay time t_d and frequency f are both user-defined (e.g. t_d =1.2 ms and f=50 Hz). Day *et al.* have discussed how the lock-in phase angle θ should be set to avoid errors. According to their convention, the "bias phase reference mode" was used. The bias reference mode sets the zero-crossing of the lock-in weighting function to the bias pulse edge (i.e. at $t=t_p$ in Figure 3.9). This convention has been shown to result in the least amount of error. The normalized time constant versus frequency and normalized output signal versus frequency are plotted in Figures A.1 and A.2. They were computed using MatLab 4.2c [The MathWorks, Inc.] These plots may be referred to for time constant determination and relative peak height comparisons as long as $t_d \ll T_0$. Some results are given in Table 3.2 and Table 3.3. The frequency dependence of the time constant and the output magnitude can be minimized for even smaller gate-off delay times.

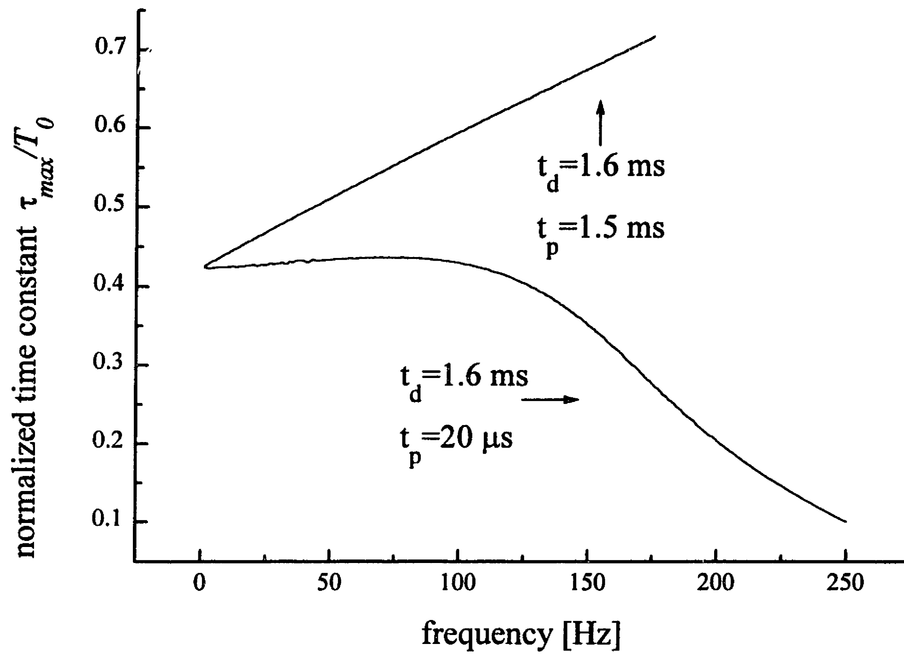

Figure A.9.1 Normalized time constant versus frequency in the bias phase reference mode for two cases: (1) t_d=1.6 ms and t_p =20 μs and (2) t_d=1.6 ms and t_p =1.5 ms.

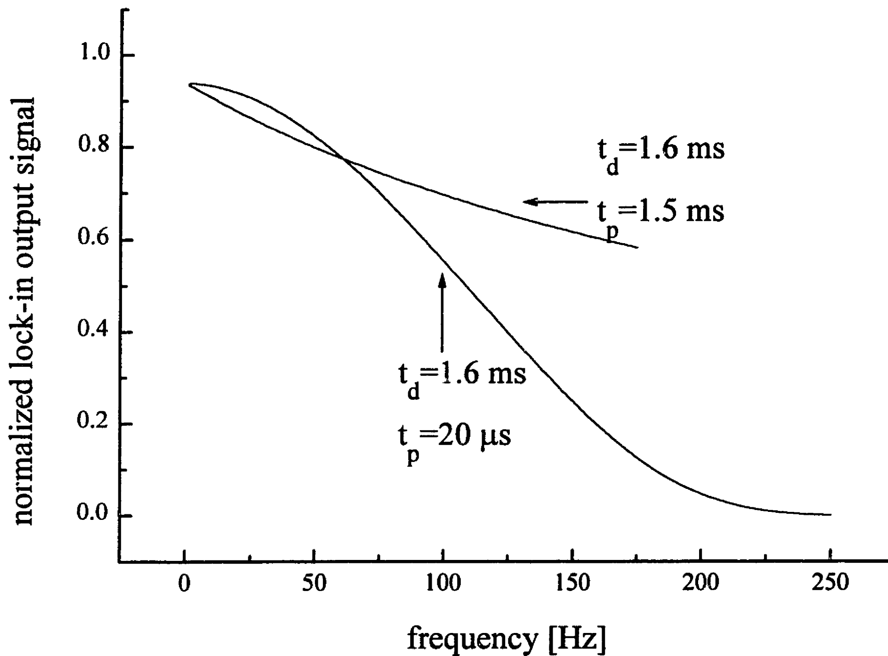

Figure A.9.2 Normalized output signal versus frequency in the bias phase reference mode for two cases: (1) t_d=1.6 ms and t_p =20 μs and (2) t_d=1.6 ms and t_p =1.5 ms. The normalization is to the ideal case where t_d, t_p =0.

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